

## P-Channel Enhancement-Mode Vertical DMOS FET

### Features

- High Input Impedance and High Gain
- Low Power Drive Requirement
- Ease of Paralleling
- Low  $C_{ISS}$  and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- Free from Secondary Breakdown

### Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photo-Voltaic Drives
- Analog Switches
- Power Management
- Telecommunication Switches

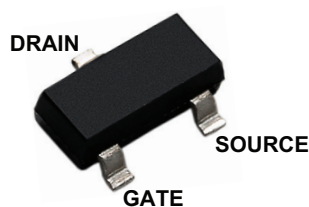
### General Description

The TP0610T is a low-threshold, Enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Type

**3-lead SOT-23 (TO-236AB)**  
(Top view)



See [Table 3-1](#) for pin information.

# TP0610T

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

Drain-to-Source Voltage .....	$BV_{DSS}$
Drain-to-Gate Voltage .....	$BV_{DGS}$
Gate-to-Source Voltage .....	$\pm 20V$
Operating Ambient Temperature, $T_A$ .....	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, $T_S$ .....	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^{\circ}C$  unless otherwise specified. All DC parameters are 100% tested at  $25^{\circ}C$  unless otherwise stated. Pulse test: 300  $\mu s$  pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	$BV_{DSS}$	-60	—	—	V	$V_{GS} = 0V$ , $I_D = -10 \mu A$
Gate Threshold Voltage	$V_{GS(th)}$	-1	—	-2.4	V	$V_{GS} = V_{DS}$ , $I_D = -1 mA$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	6.5	mV/ $^{\circ}C$	$V_{GS} = V_{DS}$ , $I_D = -1 mA$ (Note 1)
Gate Body Leakage	$I_{GSS}$	—	—	$\pm 10$	nA	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$
Zero-Gate Voltage Drain Current	$I_{DSS}$	—	—	-1	$\mu A$	$V_{GS} = 0V$ , $V_{DS} = \text{Maximum rating}$
			—	-200	$\mu A$	$V_{DS} = 0.8 \text{ Maximum rating}$ , $V_{GS} = 0V$ , $T_A = 125^{\circ}C$ (Note 1)
On-State Drain Current	$I_{D(ON)}$	-50	—	—	mA	$V_{GS} = -4.5V$ , $V_{DS} = -10V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	25	$\Omega$	$V_{GS} = -4.5V$ , $I_D = -25 mA$
			—	10	$\Omega$	$V_{GS} = -10V$ , $I_D = -200 mA$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1	%/ $^{\circ}C$	$V_{GS} = -10V$ , $I_D = -200 mA$ (Note 1)

**Note 1:** Specification is obtained by characterization and is not 100% tested.

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:**  $T_A = 25^\circ\text{C}$  unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G <sub>FS</sub>	60	—	—	mmho	V <sub>DS</sub> = −10V, I <sub>D</sub> = −100 mA
Input Capacitance	C <sub>ISS</sub>	—	—	60	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = −25V, f = 1 MHz
Common Source Output Capacitance	C <sub>OSS</sub>	—	—	30	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	—	10	pF	
Turn-On Delay Time	t <sub>d(ON)</sub>	—	—	10	ns	V <sub>DD</sub> = −25V, I <sub>D</sub> = −180 mA, R <sub>GEN</sub> = 25Ω
Rise Time	t <sub>r</sub>	—	—	15	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>	—	—	15	ns	
Fall Time	t <sub>f</sub>	—	—	20	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V <sub>SD</sub>	—	—	−2	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = −120 mA (Note 1)
Reverse Recovery Time	t <sub>rr</sub>	—	400	—	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = −400 mA

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at  $25^\circ\text{C}$ .

Pulse test: 300  $\mu\text{s}$  pulse, 2% duty cycle

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature	$T_A$	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	$T_S$	-55	—	+150	$^\circ\text{C}$	
<b>PACKAGE THERMAL RESISTANCE</b>						
3-lead SOT-23	$\theta_{JA}$	—	203	—	$^\circ\text{C/W}$	

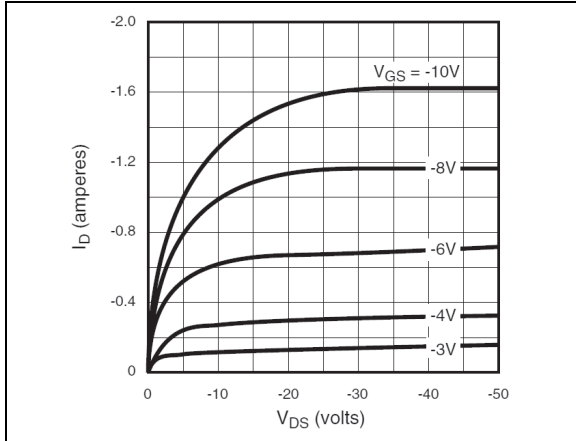
## THERMAL CHARACTERISTICS

Package	$I_D$ ( <b>Note 1</b> ) (Continuous) (mA)	$I_D$ (Pulsed) (mA)	Power Dissipation at $T_A = 25^\circ\text{C}$ (W)	$I_{DR}$ ( <b>Note 1</b> ) (mA)	$I_{DRM}$ (mA)
3-lead SOT-23	-120	-400	0.36	-120	-400

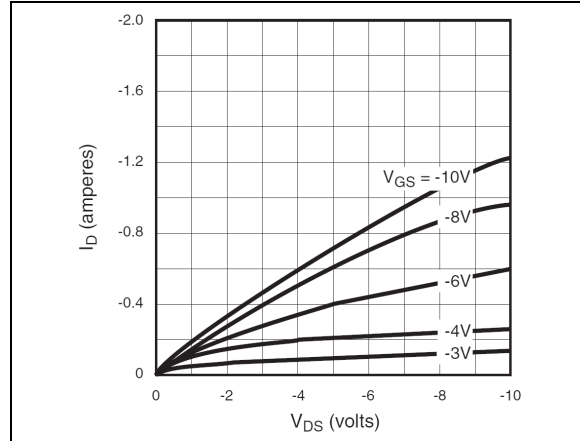
**Note 1:**  $I_D$  (continuous) is limited by maximum  $T_J$ .

## 2.0 TYPICAL PERFORMANCE CURVES

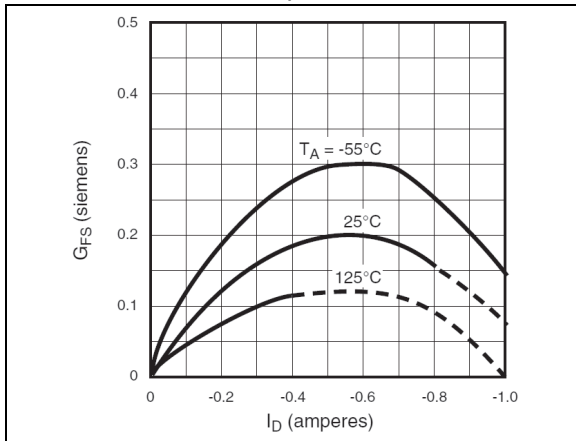
**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.



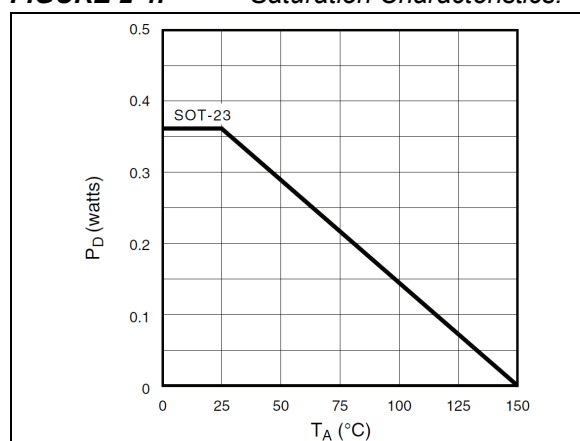
**FIGURE 2-1:** Output Characteristics.



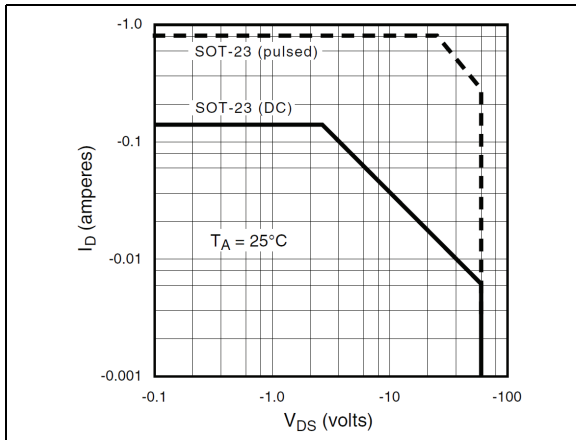
**FIGURE 2-4:** Saturation Characteristics.



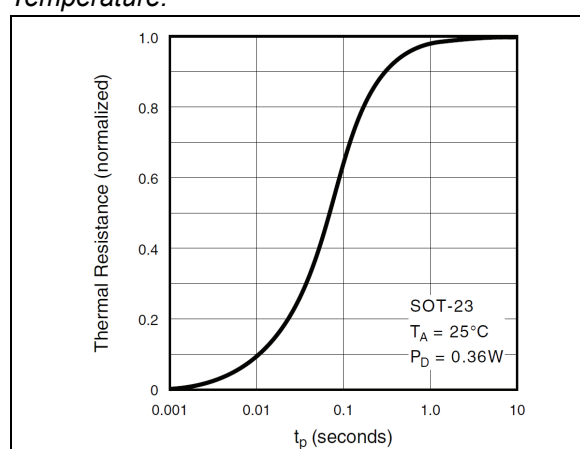
**FIGURE 2-2:** Transconductance vs. Drain Current.



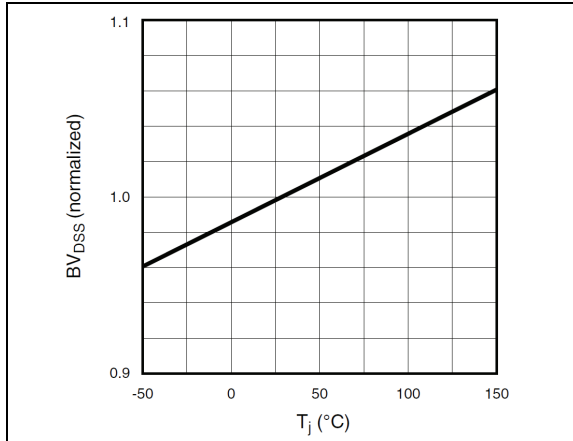
**FIGURE 2-5:** Power Dissipation vs. Temperature.



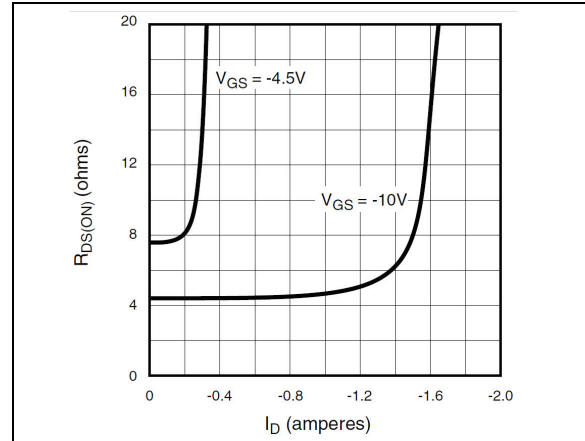
**FIGURE 2-3:** Maximum Rated Safe Operating Area.



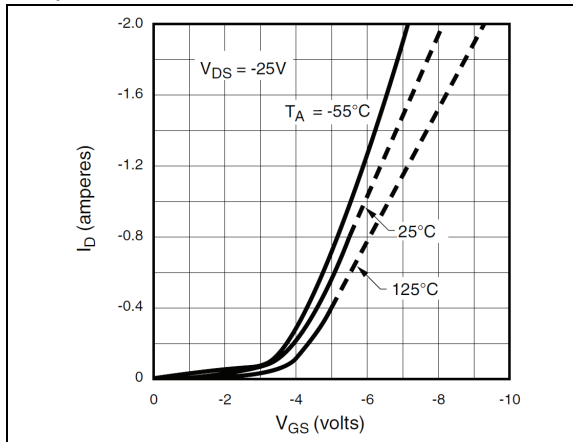
**FIGURE 2-6:** Thermal Response Characteristics.



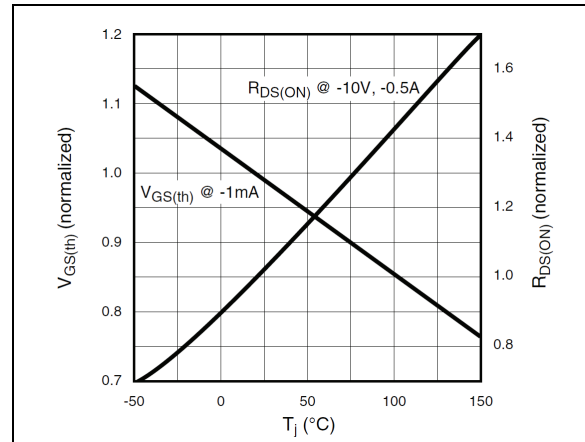
**FIGURE 2-7:**  $BV_{DSS}$  Variation with Temperature.



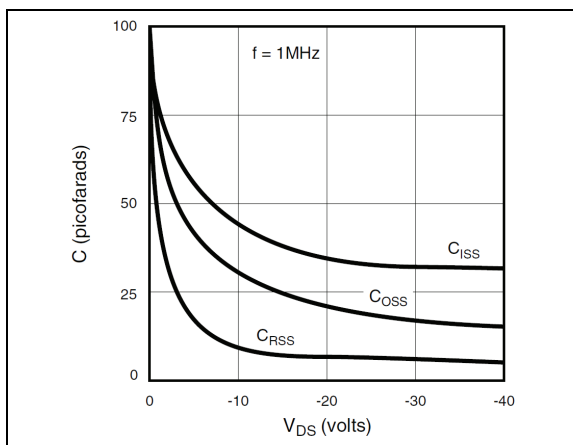
**FIGURE 2-10:** On-Resistance vs. Drain Current.



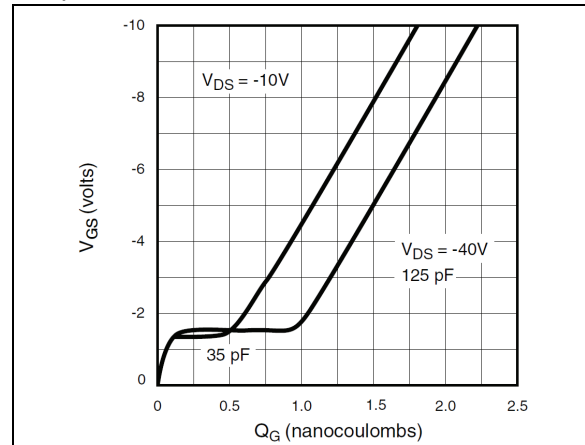
**FIGURE 2-8:** Transfer Characteristics.



**FIGURE 2-11:**  $V_{(th)}$  and  $R_{DS}$  Variation with Temperature.



**FIGURE 2-9:** Capacitance vs. Drain-to-source Voltage.



**FIGURE 2-12:** Gate Drive Dynamic Characteristics.

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## 3.0 PIN DESCRIPTION

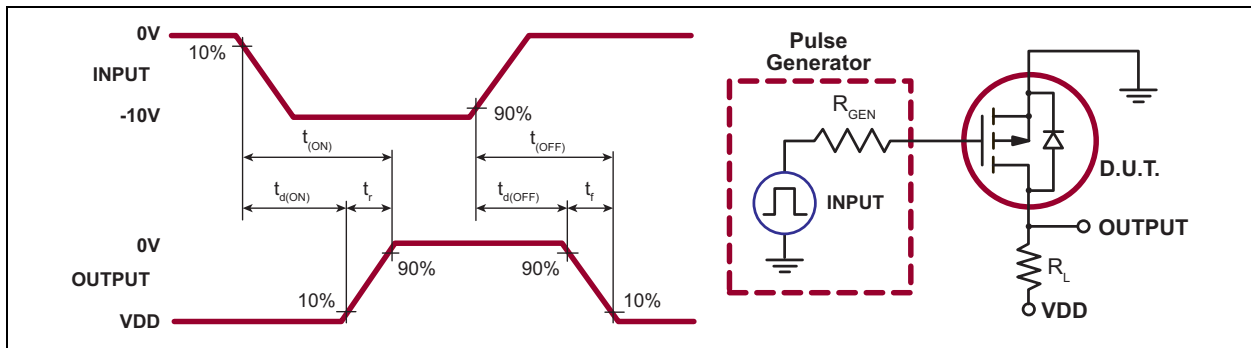
Table 3-1 shows the description of pins in TP0610T SOT-23 (TO-236AB). Refer to [Package Type](#) for the location of pins.

**TABLE 3-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

## 4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TP0610T.



**FIGURE 4-1:** Switching Waveforms and Test Circuit.

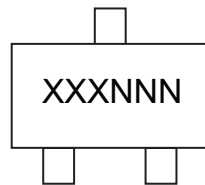
**TABLE 4-1: PRODUCT SUMMARY**

$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (Maximum) ( $\Omega$ )	$V_{GS(th)}$ (Maximum) (mA)
-60	10	-50

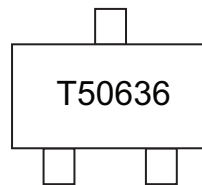
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

3-lead SOT-23



Example

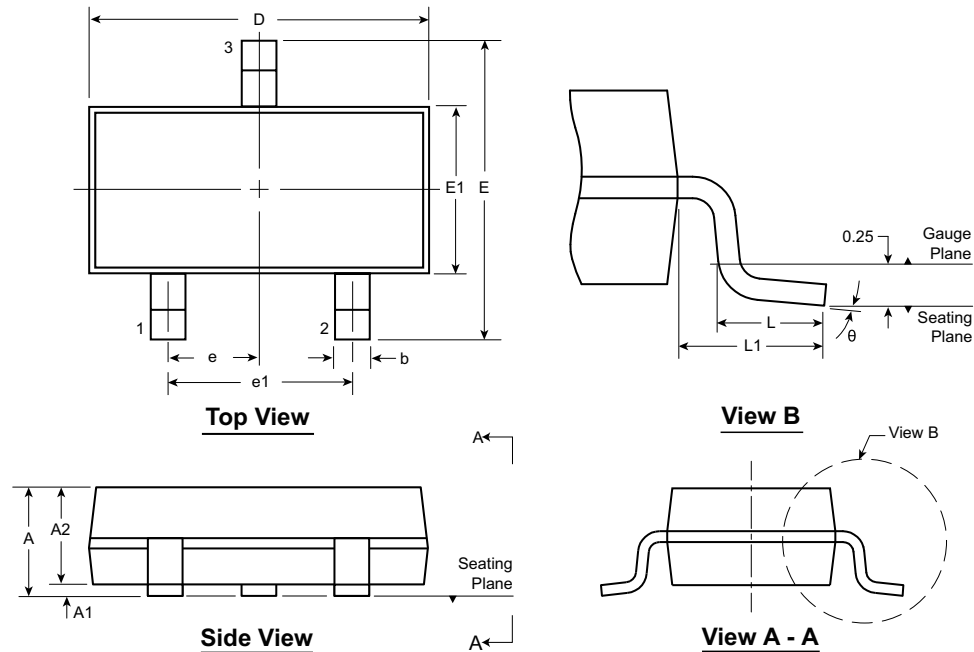


<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.



## 3-Lead TO-236AB (SOT-23) Package Outline (K1/T) 2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 <sup>†</sup>	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

<sup>†</sup> This dimension differs from the JEDEC drawing.

Drawings not to scale.

# TP0610T

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NOTES:

## **APPENDIX A: REVISION HISTORY**

### **Revision A (July 2019)**

- Converted Supertex Doc# DSFP-TP0610T to Microchip DS20005701B
- Corrected the order of the diagrams in the Typical Performance Curves section
- Made minor text changes throughout the document

### **Revision B (February 2020)**

- Changed all Typical Performance Curves in Revision A to the curves shown in this version

# TP0610T

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	TP0610T	=	P-Channel Enhancement-Mode Vertical DMOS FET		
Package:	(blank)	=	3-lead SOT-23		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	3000/Reel for an SOT-23 Package		

**Example:**  
a) TP0610T-G: P-Channel Enhancement-Mode Vertical DMOS FET, 3-lead SOT-23, 3000/Reel

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