SmartFusion2 System-on-Chip FPGAs

Introduction

Microsemi's SmartFusion®2 System-on-Chip (SoC) FPGAs integrate fourth generation flash-based FPGA fabric, an ARM® Cortex™-M3 processor, and high performance communications interfaces on a single chip. The SmartFusion2 FPGA is the industry's lowest power, the most secure, and has the highest reliability of any programmable logic solution. SmartFusion2 offers up to 3.6X the gate density and up to 2X the performance of previous flash-based FPGA families and includes multiple memory blocks and multiply accumulate blocks for DSP processing. The 166 MHz ARM Cortex-M3 processor is enhanced with ETM and 8 Kbyte instruction cache, and additional peripherals including CAN, Gigabit Ethernet, and high speed USB. High speed serial interfaces enable PCIe, XAUI/XGXS plus native SERDES communication while DDR2/DDR3 memory controllers provide high speed memory interfaces.

SmartFusion2 Device Status

Table 1 • **SmartFusion2 Device Status**

Family Devices	Status
M2S005TM2S005	Advance
M2S010T/M2S010	Advance
M2S025T/M2S025	Advance
M2S050T/M2S050	Advance
M2S075T/M2S075	Advance
M2S080T/M2S080	Advance
M2S120T/M2S120	Advance

SmartFusion2 Product Brief and Pin Descriptions

The product brief and pin descriptions are published separately:

SmartFusion2 Product Brief

SmartFusion2 Pin Descriptions

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Stresses beyond those listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2-2 on page 2-2 is not implied.

Table 1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits		Units	Notes
		Min.	Max.		
VDD	DC core supply voltage. Must always power this pin	–0.3	1.32	V	
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	–0.3	3.63	V	
MDDR_PLL_VDDA	Analog power supply for MDDR PLL	–0.3	3.63	V	
FDDR_PLL_VDDA	Analog power supply for FDDR PLL	–0.5	3.63	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0-5	–0.3	3.63	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	–0.3	3.63	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	–0.3	2.75	V	
SERDES_[01]_L[0123]_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. It is a +1.2 V SERDES PMA supply.	–0.3	1.32	V	
SERDES_[01]_VDD	PCIe/PCS Power supply	–0.5	1.32	V	
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O bank	–0.3	3.63	V	
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O banks	–0.3	2.75	V	
VI	I/O Input voltage for MSIO I/O bank	–0.3	3.63	V	
	I/O Input voltage for MSIOD/DDRIO I/O bank	–0.3	2.75	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	–0.3	3.63	V	
T_{STG}	Storage temperature	–65	150	°C	1
T_J	Junction temperature	–	125	°C	

Note:

1. *For flash programming and retention maximum limits, refer to Table 3 on page 9. For recommended operating conditions, refer to Table 2 on page 8.*

Table 2 • **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
T_J	Junction temperature	Commercial	0	25	85	°C	
	Junction temperature	Industrial	–40	25	100	°C	
VDD	DC core supply voltage. Must always power this pin.		1.14	1.2	1.26	V	
VPP	Power supply for charge pumps (for normal operation and programming)	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0 to PLL5	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.		2.375	2.5	2.625	V	
SERDES_[01]_L[0123]_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.		1.14	1.2	1.26	V	
SERDES_[01]_VDD	PCIe/PCS power supply		1.14	1.2	1.26	V	
VDDIx	1.2 V DC supply voltage		1.14	1.2	1.26	V	
	1.5 V DC supply voltage		1.425	1.5	1.575	V	
	1.8 V DC supply voltage		1.71	1.8	1.89	V	
	2.5 V DC supply voltage		2.375	2.5	2.625	V	
	3.3 V DC supply voltage		3.15	3.3	3.45	V	
	LVDS differential I/O		2.375	2.5	3.45	V	
	B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O		2.375	2.5	2.625	V	
	LVPECL differential I/O		3.15	3.3	3.45	V	
VREFx	Reference voltage supply for FDDR (bank 0) and MDDR (bank 5)		0.49 * VDDIx	0.5 * VDDIx	0.51 * VDDIx	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	

Table 3 • **FPGA and Embedded Flash Programming, Storage and Operating Limits**

Product Grade	Storage Temperature	Programming Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T_J = 0°C Max. T_J = 85°C	Min. T_J = 0°C Max. T_J = 85°C	FPGA	500	20 years
		Min. T_J = 0°C Max. T_J = 85°C	Embedded Flash	< 1,000	20 years
				< 10,000	10 years
Industrial	Min. T_J = –40°C Max. T_J = 100°C	Min. T_J = 0°C Max. T_J = 85°C	FPGA	500	20 years
		Min. T_J = –40°C Max. T_J = 100°C	Embedded Flash	< 1,000	20 years
				< 10,000	10 years

Power Supply Sequencing and Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every SmartFusion2 SoC FPGA. These circuits ensure easy transition from the powered-off state to powered-up state of the device. The SmartFusion2 system controller is responsible for systematic power-on reset whenever the device is powered on or reset. All the I/Os are held in a high-impedance state by the system controller until all power supplies are at their required levels and the system controller has completed the reset sequence. The power-on reset circuitry in SmartFusion2 devices requires the VDD and VPP supplies to ramp monotonically from 0 V to the minimum recommended operating voltage within a predefined time. There is no sequencing requirement on VDD and VPP. Four ramp rate options are available during design generation: 50 µs, 1 ms, 10 ms, and 100 ms. Each selection represents the maximum ramp rate to apply to VDD and VPP. The user can set the ramp rate using Libero SoC.

Thermal Characteristics

Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad \text{EQ 1}$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad \text{EQ 2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{EQ 3}$$

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 4 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
M2S050T-FG896	14.7	12.5	10.9	7.2	4.9	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2S050T-FG896 package at commercial temperature and in still air, where

θ_{JA} = 14.7°C/W (taken from Table 4 on page 10).

T_A = 85°C

$$\text{Maximum Power Allowed} = \frac{100°C - 85°C}{14.7°C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculating Power Dissipation

Quiescent Supply Current

Table 5 • **Quiescent Supply Current Characteristics**

Parameter	Modes	M2S050T VDD = 1.2 V	Units
IDC1	Active mode	7.5	mA
IDC2	Standby mode	7.5	mA
IDC3	Flash*Freeze mode	0.387	mA

I/O Power

Table 6 • **Summary of I/O Input Buffer Power (per pin) Using Default Software Setting with Technology Selected**

	MSIO I/O Bank		MSIOD I/O Bank		DDR I/O Bank		
	Static Power PDC8 (mW)	Dynamic Power PAC9 (µW/MHz)	Static Power PDC8 (mW)	Dynamic Power PAC9 (µW/MHz)	Static Power PDC8 (mW)	Dynamic Power PAC9 (µW/MHz)	Notes
Single-Ended I/O Standards							
1.2 V LVCMOS (JESD8-11)	0.00	11.72	0.00	11.72	0.00	11.72	
1.5 V LVCMOS (JESD8-11)	0.00	8.32	0.00	8.32	0.00	8.32	
1.8 V LVCMOS	0.00	10.69	0.00	10.69	0.00	10.69	
2.5 V LVCMOS	0.00	4.14	0.00	4.14	0.00	4.14	
3.3 V LVTTL / 3.3 V LVCMOS	0.00	5.47	–	–	–	–	
3.3 V PCI/PCIX	0.00	1.82	–	–	–	–	
Memory Interface and Voltage Reference Standard							
HSTL 1.5 V	2.21	5.57	2.21	5.57	2.21	5.57	
HSTL 1.5 V – True differential	1.25	47.38	1.25	47.38	1.25	47.38	
SSTL2/DDR	10.02	42.68	10.02	42.68	10.02	42.68	
SSTL2/DDR – True differential	4.39	12.35	4.39	12.35	4.39	12.35	
SSTL18/DDR2	3.88	3.81	3.88	3.81	3.88	3.81	
SSTL18/DDR2 – True differential	1.97	56.80	1.97	56.80	1.97	56.80	
SSTL15/DDR3	–	–	–	–	2.20	18.00	
SSTL15/DDR3 – True differential	–	–	–	–	1.23	46.81	
LPDDR	–	–	–	–	3.88	4.46	
LPDDR – True differential	–	–	–	–	1.97	5.08	
Differential Standards							
LVDS	5.74	17.65	5.74	17.65	–	–	
B-LVDS	5.65	8.76	5.65	8.76	–	–	
M-LVDS	5.65	8.76	5.65	8.76	–	–	
RSDS	5.74	0.93	5.74	0.93	–	–	
Mini-LVDS	TBD	TBD	TBD	TBD	–	–	
LVPECL	TBD	TBD	–	–	–	–	

Table 7 • **Summary of I/O Output Buffer Power (per pin)**
Default Software Setting with Technology selected at Typical conditions: 25°C
VDDI = Typical Voltage

	MSIO I/O Bank		MSIOD I/O Bank		DDR I/O Bank		
	Static Power	Dynamic Power	Static Power	Dynamic Power	Static Power	Dynamic Power	
	PDC9 (mW)	PAC9 (µW/MHz)	PDC9 (mW)	PAC9 (µW/MHz)	PDC9 (mW)	PAC9 (µW/MHz)	Notes
Single-Ended I/O Standards							
1.2 V LVCMOS (JESD8-11)	0.00	16.74	0.00	16.74	0.00	16.74	
1.5 V LVCMOS (JESD8-11)	0.00	26.31	0.00	26.31	0.00	26.31	
1.8 V LVCMOS	0.00	38.23	0.00	38.23	0.00	38.23	
2.5 V LVCMOS	0.00	75.35	0.00	75.35	0.00	75.35	
3.3 V LVTTL / 3.3 V LVCMOS	0.00	137.04	–	–	–	–	
3.3 V PCI/PCIX	0.00	TBD	–	–	–	–	
Memory Interface and Voltage Reference Standard							
HSTL 1.5 V Class I	6.45	60.17	6.45	60.17	6.45	60.17	
HSTL 1.5 V Class I – True differential	12.90	80.30	12.90	80.30	12.90	80.30	
HSTL 1.5 V Class II	–	–	–	–	12.56	104.21	
HSTL 1.5 V Class II – True differential	–	–	–	–	25.08	87.09	
SSTL2 Class I / DDR reduced drive	18.12	76.44	18.12	76.44	18.12	76.44	
SSTL2 Class I / DDR reduced drive – True differential	36.16	218.81	36.16	218.81	36.16	218.81	
SSTL2 Class II / DDR full drive	37.20	317.68	37.20	317.68	37.20	317.68	
SSTL2 Class II / DDR full drive – True differential	74.41	110.90	74.41	110.90	74.41	110.90	
SSTL18 Class I / DDR2 reduced drive	9.06	15.09	9.06	15.09	9.06	15.09	
SSTL18 Class I / DDR2 reduced drive – True differential	18.09	56.33	18.09	56.33	18.09	56.33	
SSTL18 Class II / DDR2 full drive	18.63	170.66	18.63	170.66	18.63	170.66	
SSTL18 Class II / DDR2 full drive – True differential	37.28	9.12	37.28	9.12	37.28	9.12	
SSTL15 Class I / DDR3 reduced drive	–	–	–	–	11.28	62.13	
SSTL15 Class I / DDR3 reduced drive – True differential	–	–	–	–	22.52	131.80	
SSTL15 Class II / DDR3 full drive	–	–	–	–	12.15	47.65	
SSTL15 Class II / DDR3 full drive – True differential	–	–	–	–	24.29	142.98	
LPDDR reduced drive	–	–	–	–	18.62	331.33	
LPDDR reduced drive – True differential	–	–	–	–	37.28	9.12	
LPDDR full drive	–	–	–	–	9.06	46.40	
LPDDR full drive – True differential	–	–	–	–	18.09	56.33	
Differential Standards							
LVDS	13.48	63.84	13.48	63.84	–	–	
B-LVDS	18.37	30.73	–	–	–	–	
M-LVDS	18.37	30.73	–	–	–	–	
RSDS	8.50	82.76	8.50	82.76	–	–	
Mini-LVDS	TBD	TBD	TBD	TBD	–	–	

Power Consumption of Various Internal Resources

Table 8 • **Different Components Contributing to Dynamic Power Consumption in SmartFusion2 Devices under Typical Conditions, 25°C, VDD= 1.2 V**

Param.	Definition	Power Supply		Device	Units	Notes
		Name	Domain	M2S050T		
PAC1	Global clock contribution of a GB	VDD	1.2 V	3.50	µW/MHz	
PAC2	Global clock contribution of a RGB	VDD	1.2 V	0.87	µW/MHz	
PAC3	Global clock contribution of a sequential module.	VDD	1.2 V	0.02	µW/MHz	
PAC4	Clock contribution of a sequential module.	VDD	1.2 V	0.01	µW/MHz	
PAC5	Data contribution of a sequential module.	VDD	1.2 V	0.06965	µW/MHz	
PAC6	Average contribution of a combinatorial module.	VDD	1.2 V	0.709	µW/MHz	
PAC7	Average contribution of a combinatorial module with carry chain.	VDD	1.2 V	0.821657	µW/MHz	
PAC8	Average contribution of a routing net.	VDD	1.2 V	0.87	µW/MHz	
PAC9	Contribution of an I/O input pin (standard dependent)	VDDI	Table 6 on page 12	Table 6 on page 12	–	
PAC10	Contribution of an I/O output pin (standard dependent)	VDDI	Table 7 on page 13	Table 7 on page 13	–	
PAC11	Average contribution of a uSRAM block during a read operation	VDD	1.2 V	2.39	µW/MHz	
PAC12	Average contribution of a uSRAM block during a write operation	VDD	1.2 V	7.01	µW/MHz	
PAC13	Average contribution of a LSRAM block during a read operation	VDD	1.2 V	19.85	µW/MHz	
PAC14	Average contribution of a LSRAM block during a write operation	VDD	1.2 V	24.85	µW/MHz	
PAC15	CCC contribution	VDD	1.2 V	8.00	mW	
PAC16	Main crystal oscillator contribution	VDD	1.2 V	55.51	µW/MHz	
PAC17	1 MHz RC oscillator contribution	VDD	1.2 V	37.2	mW	
PAC18	50 MHz RC oscillator contribution	VDD	1.2 V	7.30	mW	
PAC19	Mathblock contribution	VDD	1.2 V	TBD	mW	
PAC20	MSS dynamic power contribution with MDDR/USB/Ethernet OFF, clock frequency = 100 MHz	VDD	1.2 V	91.986	mW	1
PAC21	MSS dynamic power contribution with USB/Ethernet OFF, clock frequency = 100 MHz, MDDR mode–MSS bridge	VDD	1.2 V	137.43	mW	1

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Dynamic power contribution of FDDR does not include the DDRIO power. Use the specific I/O standard buffer power for calculation of the DDRIO power. For a different use of the FDDR, refer to SmartPower.*
3. *For a different use of the SERDES block, refer to SmartPower.*

Table 8 • Different Components Contributing to Dynamic Power Consumption in SmartFusion2 Devices under Typical Conditions, 25°C, VDD= 1.2 V (continued)

Param.	Definition	Power Supply		Device	Units	Notes
		Name	Domain	M2S050T		
PAC22	FDDR dynamic power contribution with frequency = 100 MHz, DDR clock multiplier = 2	VDD	1.2 V	108.81	mW	2
PAC23	SERDES dynamic power contribution configured as PCIe_GEN1 x1 at 125 MHz	VDD	1.2 V	91.70	mW	3

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Dynamic power contribution of FDDR does not include the DDRIO power. Use the specific I/O standard buffer power for calculation of the DDRIO power. For a different use of the FDDR, refer to SmartPower.*
3. *For a different use of the SERDES block, refer to SmartPower.*

Table 9 • Different Components Contributing to the Static Power Consumption in SmartFusion2 Devices under Typical Conditions, 25°C, VDD = 1.2 V

Param.	Definition	Power Supply			Device	Units
		Name	Domain	Mode	M2S050T	
PDC1	Core static power contribution in active operating mode	VDD	1.2 V	Active	9.000	mW
PDC2	Core static power contribution in standby operating mode	VDD	1.2 V	Standby	9.000	mW
PDC3	Core static power contribution in Flash*Freeze operating mode	VDD	1.2 V	Flash*Freeze	0.465	mW
PDC4	LSRAM static power contribution in Flash*Freeze configured in Sleep state	VDD	1.2 V	Flash*Freeze	1.250	µW
PDC5	LSRAM static power contribution in Flash*Freeze configured in Suspended state	VDD	1.2 V	Flash*Freeze	10.140	µW
PDC6	USRAM static power contribution in Flash*Freeze configured in Sleep state	VDD	1.2 V	Flash*Freeze	0.500	µW
PDC7	USRAM static power contribution in Flash*Freeze configured in Suspend state	VDD	1.2 V	Flash*Freeze	4.970	µW
PDC8	I/O Input static power contribution in active operating mode	VDDI	VDDI	Active	See Table 6 on page 12	µW
PDC9	I/O output static power contribution in active operating mode	VDDI	VDDI	Active	See Table 7 on page 13	µW

Power Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software. The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as the logic module—guidelines are provided in Table 10 on page 20.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 11 on page 20.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 11 on page 20.

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

Active, Standby and Flash*Freeze Mode

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

Active Mode

$P_{STAT} = PDC1 + (N_{INPUTS} * PDC7) + (N_{OUTPUTS} * PDC8) + (N_{PLLS} * PDC9)$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = PDC2$

Flash*Freeze Mode

P_{STAT} = PDC3 + PDC4 + PDC 6 when both LSRAM and uSRAM are configured in Sleep state

P_{STAT} = PDC3 + PDC5 + PDC 7 when both LSRAM and uSRAM are configured in Suspend state

Total Dynamic Power Consumption—P_{DYN}

Active Mode

$P_{DYN} = P_{CLOCK} + P_{LOGIC} + P_{IOS} + P_{MEMORY} + P_{CCC} + P_{MATH} + P_{MSS} + P_{FDDR} + P_{SERDES}$

Flash*Freeze Mode

$P_{DYN} = PDC3 + P_{MEMORY}$

Standby Mode

$P_{DYN} = PDC2$

Global Clock Dynamic Power Contribution—P_{CLOCK}

Active Mode

P_{CLOCK} = (PAC1 + N_{ROWS} * PAC2 + $N_{S\text{-}CELL}$ * PAC3) * F_{CLK}

Where:

N_{ROWS} is the number of global rows used in the design—guidelines are provided in the "Fabric Global Routing Resources" chapter of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of Registers used in the design.

Standby and Flash*Freeze Mode

P_{CLOCK} = 0 W

Logic Module Dynamic Power Contribution—P_{LOGIC}

Active Mode

P_{LOGIC} = P_{SEQ} + P_{LUT} + P_{NET}

Standby and Flash*Freeze Mode

P_{LOGIC} = 0 W

Registers Dynamic Power Contribution—P_{SEQ}

P_{SEQ} = $N_{S\text{-}CELL}$ * PAC4 * F_{CLK} + $N_{S\text{-}CELL}$ * PAC5 * F_{CLK} * α1/2

Where:

$N_{S\text{-}CELL}$ is the number of registers used in the design.

α1 is the toggle rate of the LUT outputs—guidelines are provided in Table 10 on page 20.

F_{CLK} is the global clock signal frequency.

LUTs Dynamic Power Contribution—P_{LUT}

P_{LUT}= (N_{LUT} * PAC6 + N_{CC} * PAC7) * F_{CLK} * α1/2

Where:

N_{LUT} is the number of LUT-4 used as combinatorial modules in the design.

N_{CC} is the number of LUT-4 used with the carry chain in the design.

α1 is the toggle rate of the LUT outputs—guidelines are provided in Table 10 on page 20.

F_{CLK} is the global clock signal frequency.

Routing Net Dynamic Power Contribution—P_{NET}

P_{NET} = ($N_{S\text{-}CELL}$ + N_{LUT} + N_{CC}) * (α1 / 2) * PAC8 * F_{CLK}

Where:

$N_{S\text{-}CELL}$ is the number of registers used in the design.

N_{LUT} is the number of LUT-4 used as combinatorial modules in the design.

N_{CC} is the number of LUT-4 used with the carry chain in the design.

α1 is the toggle rate of the LUT outputs—guidelines are provided in Table 10 on page 20.

F_{CLK} is the global clock signal frequency.

I/O Dynamic Contribution—P_{IOS}

Active Mode

P_{IOS} = P_{INPUTS} + $P_{OUTPUTS}$

Standby and Flash*Freeze Mode

P_{IOS} = 0 W

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

PINPUTS = NINPUTS * (α2 / 2) * β1 * PAC9 * FCLK

Where:

N_{INPUTS} is the number of I/O input buffers used in the design.

α2 is the I/O buffer toggle rate—guidelines are provided in Table 10 on page 20.

β1 is the I/O buffer enable rate—guidelines are provided in Table 11 on page 20.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha2 / 2) * \beta1 * PAC10 * F_{CLK}$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α2 is the I/O buffer toggle rate—guidelines are provided in Table 10 on page 20.

β1 is the I/O buffer enable rate—guidelines are provided in Table 11 on page 20.

F_{CLK} is the global clock signal frequency.

FPGA Fabric SRAM Dynamic Contribution—P_{MEMORY}

Active Mode

$P_{MEMORY} = P_{USRAM} + P_{LSRAM}$

Flash*Freeze Mode

P_{MEMORY} = PDC4 + PDC6 for RAM in "Sleep" State

P_{MEMORY} = PDC5 + PDC7 for RAM in "Suspend" State

Standby Mode

P_{MEMORY} = 0 W

FPGA Fabric uSRAM Dynamic Contribution—P_{USRAM}

$P_{uSRAM} = (N_{uSRAM\_BLK} * PAC13 * \beta2 * F_{uSRAM\text{-}RDCLK}) + (N_{uSRAM\_BLK} * PAC14 * \beta3 * F_{uSRAM\text{-}WRTCLK})$

Where:

Nu_{SRAM_BLK} is the number of uSRAM blocks used in the design.

$F_{uSRAM\text{-}RDCLK}$ is the uSRAM memory read clock frequency.

$F_{uSRAM\text{-}WRTCLK}$ is the uSRAM memory write clock frequency.

β2 is the RAM enable rate for read operations—guidelines are provided in Table 11 on page 20.

β3 the RAM enable rate for write operations—guidelines are provided in Table 11 on page 20.

FPGA Fabric Large SRAM Dynamic Contribution—P_{LSRAM}

$P_{LSRAM} = (N_{LSRAM\_BLK} * PAC13 * \beta2 * F_{LSRAM\text{-}RDCLK}) + (N_{LSRAM\_BLK} * PAC14 * \beta3 * F_{LSRAM\text{-}WRTCLK})$

Where:

N_{LSRAM_BLK} is the number of Large SRAM blocks used in the design.

$F_{LSRAM\text{-}RDCLK}$ is the Large SRAM memory read clock frequency.

$F_{LSRAM\text{-}WRTCLK}$ is the Large SRAM memory write clock frequency.

β2 is the RAM enable rate for read operations—guidelines are provided in Table 11 on page 20.

β3 the RAM enable rate for write operations—guidelines are provided in Table 11 on page 20.

PLL/CCC Dynamic Contribution—P_{PLL}

Active Mode

P_{PLL} = PAC15

Flash*Freeze/Standby Mode

P_{PLL} = 0 W

External Main Crystal Oscillator Dynamic Contribution—$P_{XTL\text{-}OSC}$

Active Mode

$P_{XTL\text{-}OSC}$ = PAC16 * F_{CLK}

Where:

F_{CLK} is the output frequency of the oscillator.

Flash*Freeze/Standby Mode

$P_{XTL\text{-}OSC}$ = 0 W

On-Chip 25/50MHz RC Oscillator Dynamic Contribution—$P_{50RC\text{-}OSC}$

Active Mode/Standby Mode

$P_{50RC\text{-}OSC}$ = 0 W

Flash*Freeze

When used by MSS:

$P_{50RC\text{-}OSC}$ = PAC18

When not used by MSS:

$P_{50RC\text{-}OSC}$ = 0 W

Mathblock Dynamic Power Contribution—P_{MATH}

Active Mode

P_{MATH} = PAC19 * N_{MATH_BLK} * $F_{MATHCLK}$

N_{MATH_BLK} is the number of mathblocks used in the design.

$F_{MATHCLK}$ is the mathblock clock frequency.

Flash*Freeze/Standby Mode

P_{MATH} = 0 W

Microcontroller Subsystem Dynamic Power Contribution—P_{MSS}

Active Mode

With MDDR OFF:

P_{MSS} = PAC20

With MDDR ON:

P_{MSS} = PAC21

Flash*Freeze/Standby Mode

P_{MSS} = 0 W

FDDR Dynamic Power Contribution—P_{FDDR}

Active Mode

PFDDR = PAC22

FDDR Dynamic power contributions do not include the power contributions of the DDR I/O. This should be accounted for in the I/O power calculations.

Flash*Freeze/Standby Mode

P_{FDDR} = 0 W

SERDES Contribution—P_{SERDES}

Active Mode

P_{SERDES} = PAC23

Flash*Freeze/Standby Mode

P_{SERDES} = 0 W

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 10 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α1	Toggle rate of logic module outputs	10%
α2	I/O buffer toggle rate	10%

Table 11 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β1	I/O output buffer enable rate	Toggle rate of the logic driving the output buffer
β2	FPGA fabric SRAM enable rate for read operations	12.50%
β3	FPGA fabric SRAM enable rate for write operations	12.50%
β4	eNVM enable rate for read operations	< 5%

Average Fabric Temperature and Voltage Derating Factors

Table 12 • **Average Temperature and Voltage Derating Factors for Fabric Timing Delays (normalized to T_J = 100°C, worst-case VDD = 1.14 V)**

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.14	TBD	TBD	TBD	TBD	TBD	TBD
1.2	TBD	TBD	TBD	TBD	TBD	TBD
1.26	TBD	TBD	TBD	TBD	TBD	TBD

Timing Model

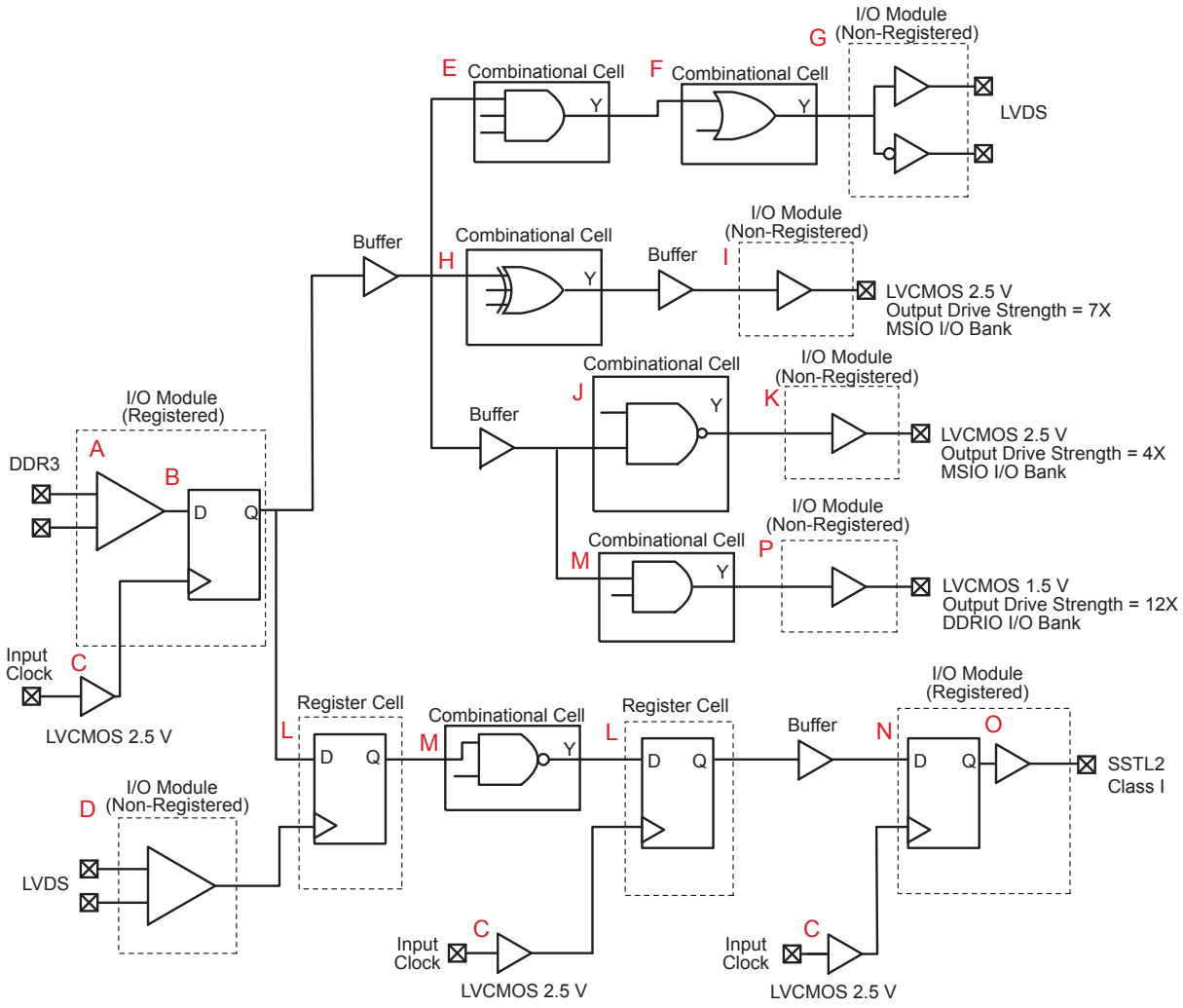


***Figure 1* • Timing Model**

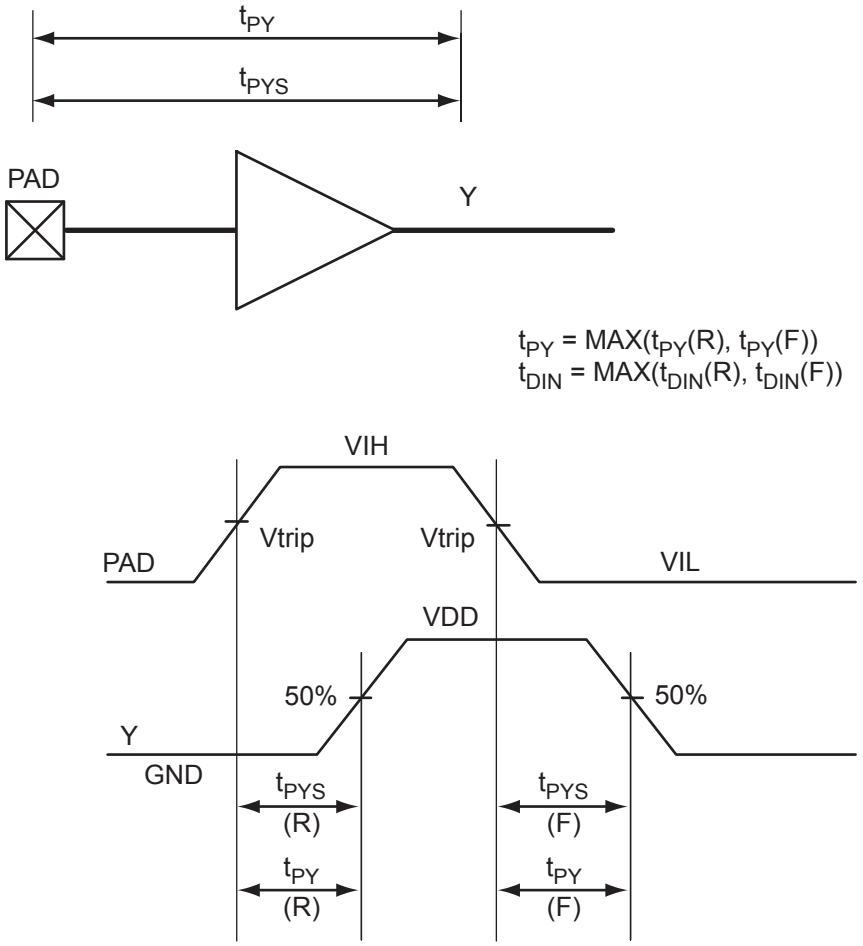
Table 13 • **Timing Model Parameters**

Index	Parameter	Description	Value	Units	Notes
A	t_{PY}	Propagation delay of DDR3 receiver	TBD	ns	Table 62 on page 60
B	t_{ICLKQ}	Clock-to-Q of the Input Data Register	TBD	ns	Table 91 on page 74
	t_{ISUD}	Setup Time of the Input Data Register	TBD	ns	Table 91 on page 74
C	t_{RCKH}	Input High Delay for Global Clock	TBD	ns	Table 97 on page 85
	t_{RCKL}	Input Low Delay for Global Clock	TBD	ns	Table 97 on page 85
D	t_{PY}	Input Propagation Delay of LVDS Receiver	TBD	ns	Table 70 on page 64
E	t_{DP}	Propagation Delay of a three input AND Gate	0.22	ns	Table 95 on page 82
F	t_{DP}	Propagation Delay of a OR Gate	0.172	ns	Table 95 on page 82
G	t_{DP}	Propagation Delay of a LVDS Transmitter	TBD	ns	Table 71 on page 64
H	t_{DP}	Propagation Delay of a three input XOR Gate	0.24	ns	Table 95 on page 82
I	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8X on the MSIO Bank	2.481	ns	Table 28 on page 32
J	t_{DP}	Propagation Delay of a two input MUX gate	0.172	ns	Table 95 on page 82
K	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 4X on the MSIO Bank	2.382	ns	Table 28 on page 32
L	t_{CLKQ}	Clock-to-Q of the Data Register	0.114	ns	Table 96 on page 84
	t_{SUD}	Setup Time of the Data Register	0.267	ns	Table 96 on page 84
M	t_{DP}	Propagation Delay of a two input AND gate	0.172	ns	Table 95 on page 82
N	t_{OCLKQ}	Clock-to-Q of the Output Data Register	TBD	ns	Table 91 on page 74
	t_{OSUD}	Setup Time of the Output Data Register	TBD	ns	Table 91 on page 74
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	TBD	ns	Table 55 on page 52
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 15X on the DDRIO Bank	TBD	ns	Table 38 on page 39

User I/O Characteristics

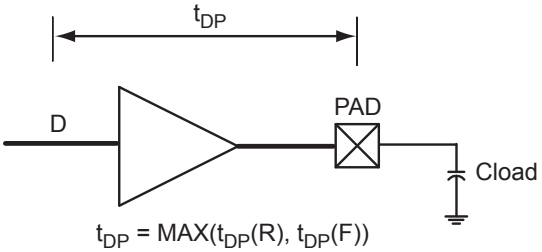
There are three types of I/Os supported in the SmartFusion2 FPGA Family: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the "I/Os" section of the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

Input Buffer and AC Loading



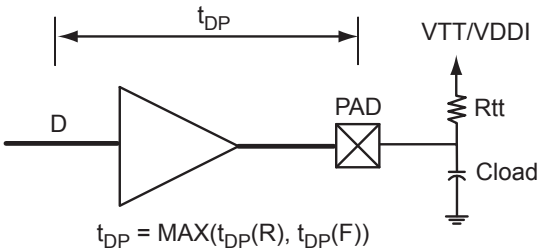
Output Buffer and AC Loading

Single-Ended I/O Test Setup



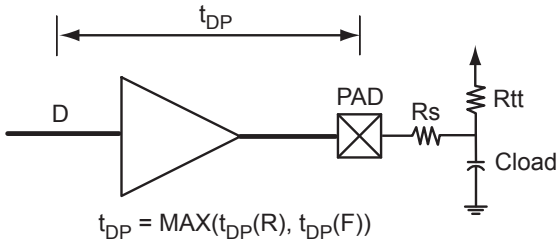
$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

HSTL/PCI Test Setup



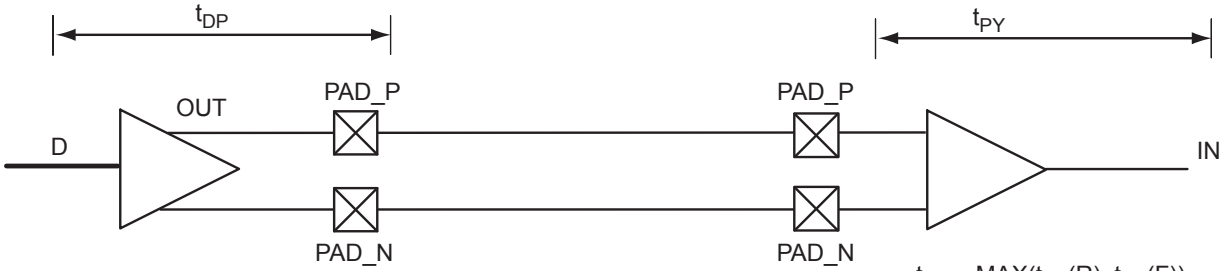
$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

Voltage-Referenced, Singled-Ended I/O Test Setup



$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

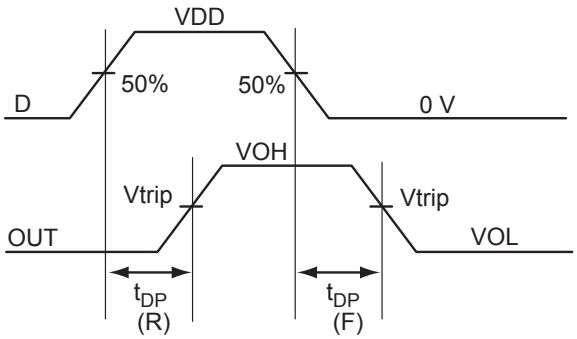
Differential I/O Test Setup



$t_{DP} = MAX(t_{DP}(R), t_{DP}(F))$

$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$

$t_{PYS} = MAX(t_{PYS}(R), t_{PYS}(F))$



Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 2.

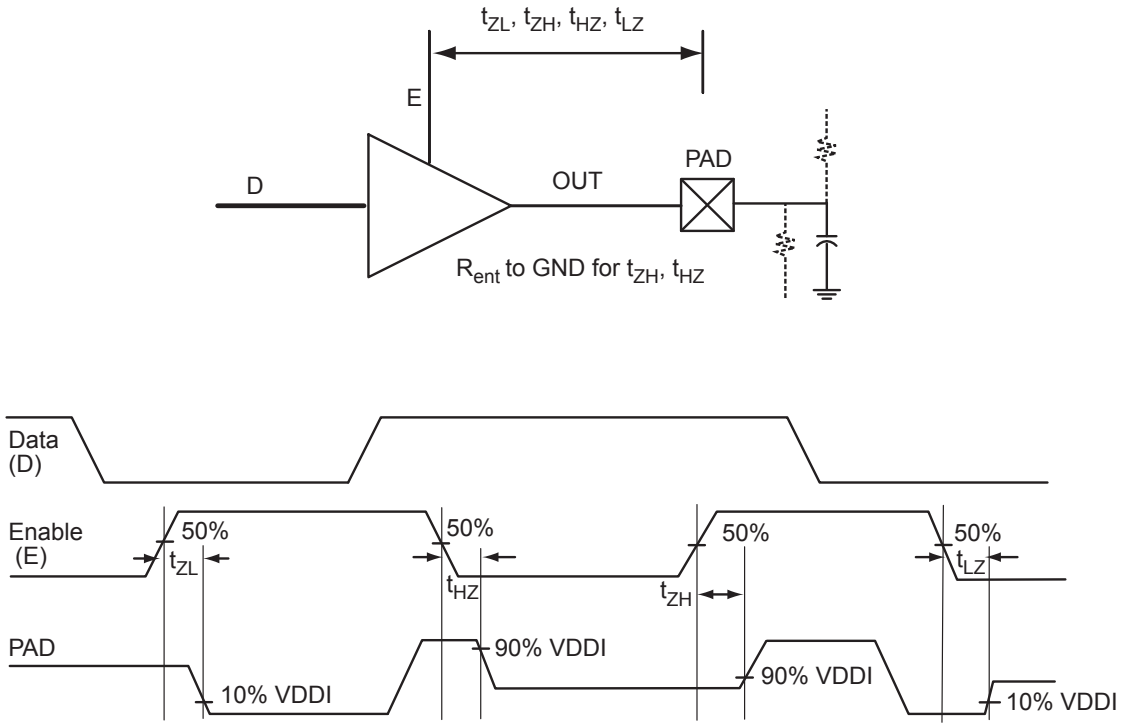


***Figure 2* • Tristate Buffer for Enable Path Test Point**

Detailed I/O Characteristics

Table 14 • Input Capacitance

Symbol	Definition	Conditions	Minimum	Maximum	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz	–	10	pF

Table 15 • I/O Weak Pull-Up/Pull-Down Resistances for DDRIO I/O Bank Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	DDRIO I/O Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	–
2.5 V	10.6 K	17.3 K	10.5 K	18.1 K	1, 2
1.8 V	1.11 K	19.3 K	11.2 K	20.9 K	1, 2
1.5 V	10 K	13.4 K	9.99 K	13.4 K	1, 2
1.2 V	10.3 K	14.5 K	10.3 K	14.7 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

Table 16 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	MSIO I/O Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	9.9 K	14.7 K	10.1 K	15.3 K	–
2.5 V	10.1 K	15.1 K	10.1 K	15.7 K	1, 2
1.8 V	10.4 K	16.2 K	10.4 K	17.3 K	1, 2
1.5 V	10.7 K	17.3 K	10.8 K	18.9 K	1, 2
1.2 V	11.3 K	19.7 K	11.5 K	22.7 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

Table 17 • I/O Weak Pull-Up/Pull-Down Resistances for MSIOD I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		Notes
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	–
2.5 V	9.6 K	14.1 K	9.5 K	13.9 K	1, 2
1.8 V	9.7 K	14.7 K	9.7 K	14.5 K	1, 2
1.5 V	9.9 K	15.3 K	9.8 K	15 K	1, 2
1.2 V	10.3 K	16.7 K	10 K	16.2 K	1, 2

Notes:

1. *R(WEAK PULL-DOWN) = (VOLspec)/I(WEAK PULL-DOWN MAX)*
2. *R(WEAK PULL-UP) = (VDDImax - VOHspec)/I(WEAK PULL-UP MIN)*

Table 18 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical, unless otherwise noted)
3.3 V LVTTL / LVCMOS / PCI / PCI-X	0.05 × VDDI (worst-case)
2.5 V LVCMOS	0.05 × VDDI (worst-case)
1.8 V LVCMOS	0.1 × VDDI (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

Single-Ended I/O Standards

Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in SmartFusion2 SoC FPGAs are LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 19 • LVTTL/LVCMOS 3.3 V DC Voltage Specification

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		0.4	–	–	V	
VOL	DC output logic Low		–	–	2.4	V	

Notes:

1. *The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.*

Table 20 • LVTTL/LVCMOS 3.3 V Minimum and Maximum AC Input and Output Levels

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVTTL/LVCMOS 3.3 V AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	600	Mbps	
LVTTL/LVCMOS 3.3 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.4	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 21 • LVTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications

Output Drive Selection / MSIO I/O Bank	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.4	0.4	2	2	
4 mA	VDDI – 0.4	0.4	4	4	
8 mA	VDDI – 0.4	0.4	8	8	
12 mA	VDDI – 0.4	0.4	12	12	
16 mA	VDDI – 0.4	0.4	16	16	
20 mA	VDDI – 0.4	0.4	20	20	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 22 • LVCMOS 3.3 V Receiver Characteristics

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		–1	Std.	–1	Std.	
LVCMOS 3.3 V (for MSIO I/O bank)	None	2.408	2.833	2.460	2.893	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 23 • LVCMOS 3.3 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 3.3 V (for MSIO I/O bank)												
2 mA	Slow	3.274	3.853	3.459	4.069	3.269	3.845	3.608	4.244	3.419	4.022	ns
4 mA	Slow	2.418	2.845	2.914	3.427	4.35	5.116	3.064	3.604	4.5	5.293	ns
8 mA	Slow	2.221	2.614	4.195	4.935	4.695	5.523	4.345	5.112	4.845	5.7	ns
12 mA	Slow	2.138	2.515	5.555	6.534	5.281	6.212	5.705	6.218	5.431	6.389	ns
16 mA	Slow	2.147	2.526	5.776	6.795	5.451	6.412	5.926	6.972	5.601	6.589	ns
20 mA	Slow	2.228	2.622	5.958	7.009	5.691	6.695	6.108	7.186	5.841	6.872	ns

LVCMOS 2.5 V

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-5A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 24 • LVCMOS 2.5 V DC Voltage Specification

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
LVCMOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		1.7	–	2.625	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		1.7	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.4	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1

Notes:

1. *The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.*

Table 25 • LVCMOS 2.5 V Minimum and Maximum AC Input and Output Levels

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 2.5 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	250	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	410	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	420	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 2.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path			1.2		V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})			2K		Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})			5		pF	
Cload	Capacitive loading for data path (t_{DP})			5		pF	

Table 26 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI – 0.4	0.4	2	2	
4 mA	4 mA	4 mA	VDDI – 0.4	0.4	4	4	
6 mA	6 mA	6 mA	VDDI – 0.4	0.4	6	6	
8 mA	8 mA	8 mA	VDDI – 0.4	0.4	8	8	
12 mA	12 mA	12 mA	VDDI – 0.4	0.4	12	12	
16 mA	N/A	16 mA	VDDI – 0.4	0.4	16	16	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 27 • LVCMOS 2.5 V Receiver Characteristics

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O bank)	None	2.132	2.509	1.943	2.287	ns
LVCMOS 2.5 V (for MSIO I/O bank)	None	3.021	3.554	3.292	3.874	ns
LVCMOS 2.5 V (for MSIOD I/O bank)	None	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 28 • LVCMOS 2.5 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O bank with FIED CODES)												
2 mA	Slow	3.774	4.44	3.928	4.621	3.796	4.466	4.104	4.828	3.702	4.355	ns
	Medium	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Medium fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
4 mA	Slow	3.175	3.736	4.779	5.621	4.303	5.061	4.955	5.828	4.479	5.268	ns
	Medium	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Medium fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
6 mA	Slow	3.058	3.598	4.970	5.846	4.482	5.273	5.146	6.053	4.658	5.48	ns
	Medium	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Medium fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Table 28 • **LVCMOS 2.5 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
8 mA	Slow	2.926	3.443	5.216	6.135	4.706	5.536	5.392	6.342	4.882	5.743	ns
	Medium	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Medium fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
12 mA	Slow	2.804	3.299	5.404	6.357	4.869	5.728	5.58	6.564	5.045	5.935	ns
	Medium	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Medium fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
16 mA	Slow	2.730	3.212	5.584	6.569	5.005	5.887	5.76	6.776	5.181	6.094	ns
	Medium	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Medium fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
	Fast	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
LVCMOS 2.5 V (for MSIO I/O bank)												
2 mA	None	3.534	4.158	3.816	4.489	3.742	4.402	3.888	4.574	3.814	4.487	ns
4 mA	None	2.651	3.118	3.898	4.586	4.625	5.441	3.971	4.672	4.698	5.527	ns
6 mA	None	2.463	2.898	4.794	5.639	4.994	5.875	4.867	5.725	5.067	5.961	ns
8 mA	None	2.382	2.802	5.724	6.734	5.417	6.373	5.797	6.82	5.49	6.459	ns
12 mA	None	2.405	2.829	5.883	6.921	5.593	6.58	5.956	7.007	5.666	6.666	ns
16 mA	None	2.481	2.918	6.281	7.389	5.871	6.907	6.354	7.475	5.944	6.993	ns
LVCMOS 2.5 V (for MSIOD I/O bank)												
2 mA	None	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
4 mA	None	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
6 mA	None	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
8 mA	None	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
12 mA	None	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-7A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 29 • LVCMOS 1.8 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.710	1.8	1.89	V	
LVCMOS 1.8 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		0.65 * VDDI	–	1.89	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 1.8 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI – 0.45	–	–	V	
VOL	DC output logic Low		–	–	0.45	V	

Table 30 • LVCMOS 1.8 V Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.8 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	200	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	295	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	320	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 1.8 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 31 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI – 0.4	0.45	2	2	
4 mA	4 mA	4 mA	VDDI – 0.4	0.45	4	4	
6 mA	6 mA	6 mA	VDDI – 0.4	0.45	6	6	
8 mA	8 mA	8 mA	VDDI – 0.4	0.45	8	8	
10 mA	10 mA	10 mA	VDDI – 0.4	0.45	10	10	
12 mA	N/A	12 mA	VDDI – 0.4	0.45	12	12	
N/A	N/A	16 mA	VDDI – 0.4	0.45	16	16	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 32 • LVCMOS 1.8 V Receiver Characteristics

		t_{DIN}		t_{SCH_DIN}		Units
	On-Die Termination (ODT)	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O bank)	None	2.471	2.908	2.185	2.571	ns
	50	2.625	3.088	2.220	2.612	ns
	75	2.568	3.021	2.209	2.599	ns
	150	2.517	2.961	2.201	2.589	ns
LVCMOS 1.8 V (for MSIO I/O bank)	None	4.121	4.847	4.308	5.068	ns
	50	4.538	5.338	5.015	5.900	ns
	75	4.382	5.154	4.730	5.565	ns
	150	4.240	4.987	4.493	5.285	ns
LVCMOS 1.8 V (for MSIOD I/O bank)	None	3.017	3.549	3.023	3.556	ns
	50	3.156	3.713	3.173	3.733	ns
	75	3.111	3.659	3.119	3.670	ns
	150	3.069	3.610	3.075	3.617	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 33 • LVCMOS 1.8 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O bank)												
2 mA	Slow	4.270	5.024	4.806	5.655	4.298	5.056	5.095	5.994	4.526	5.324	ns
	Medium	3.877	4.562	4.530	5.330	3.919	4.612	4.819	5.669	4.208	4.951	ns
	Medium fast	3.684	4.335	4.386	5.160	3.790	4.459	4.675	5.499	4.079	4.798	ns
	Fast	3.665	4.312	4.376	5.149	3.781	4.448	4.665	5.488	4.070	4.787	ns
4 mA	Slow	3.949	4.647	5.298	6.233	4.688	5.515	5.587	6.572	4.977	5.854	ns
	Medium	3.558	4.187	5.019	5.905	4.357	5.127	5.308	6.244	4.646	5.466	ns
	Medium fast	3.367	3.961	4.877	5.738	4.224	4.970	5.166	6.077	4.513	5.309	ns
	Fast	3.347	3.938	4.868	5.727	4.214	4.959	5.157	6.066	4.503	5.298	ns
6 mA	Slow	3.735	4.394	5.510	6.483	4.867	5.726	5.799	6.822	5.156	6.065	ns
	Medium	3.370	3.965	5.250	6.177	4.565	5.371	5.539	6.516	4.854	5.710	ns
	Medium fast	3.194	3.759	5.116	6.020	4.444	5.228	5.405	6.359	4.733	5.567	ns
	Fast	3.175	3.736	5.110	6.012	4.437	5.221	5.399	6.351	4.726	5.56o	ns
8 mA	Slow	3.640	4.283	5.702	6.708	5.029	5.917	5.991	7.047	5.318	6.256	ns
	Medium	3.278	3.857	5.438	6.399	4.717	5.550	5.727	6.738	5.006	5.889	ns
	Medium fast	3.101	3.649	5.309	6.247	4.593	5.404	5.598	6.586	4.882	5.743	ns
	Fast	3.082	3.627	5.303	6.240	4.587	5.397	5.592	6.579	4.876	5.736	ns
10 mA	Slow	3.515	4.135	5.931	6.979	5.215	6.136	6.220	7.318	5.504	6.475	ns
	Medium	3.165	3.723	5.678	6.681	4.901	5.767	5.967	7.020	5.190	6.106	ns
	Medium fast	2.991	3.519	5.563	6.545	4.781	5.625	5.852	6.884	5.070	5.964	ns
	Fast	2.973	3.497	5.559	6.540	4.773	5.616	5.848	6.879	5.062	5.955	ns
12 mA	Slow	3.446	4.054	5.976	7.032	5.244	6.169	6.265	7.371	5.533	6.508	ns
	Medium	3.113	3.662	5.737	6.750	4.957	5.832	6.026	7.089	5.246	6.171	ns
	Medium fast	2.949	3.470	5.630	6.624	4.846	5.702	5.919	6.963	5.135	6.041	ns
	Fast	2.931	3.449	5.629	6.623	4.840	5.695	5.918	6.962	5.129	6.034	ns
16 mA	Slow	3.388	3.986	6.110	7.189	5.349	6.293	6.399	7.528	5.638	6.632	ns
	Medium	3.065	3.606	5.885	6.924	5.058	5.951	6.174	7.263	5.347	6.290	ns
	Medium fast	2.903	3.416	5.797	6.821	4.950	5.824	6.086	7.160	5.239	6.163	ns
	Fast	2.885	3.395	5.797	6.820	4.944	5.817	6.086	7.159	5.233	6.156	ns

Table 33 • **LVCMOS 1.8 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for MSIO I/O bank)												
2 mA	Slow	3.486	4.101	4.621	5.436	5.107	6.008	4.607	5.419	5.093	5.991	ns
4 mA	Slow	3.244	3.816	5.351	6.295	5.518	6.492	5.337	6.278	5.504	6.475	ns
6 mA	Slow	3.148	3.703	6.320	7.436	5.963	7.015	6.306	7.419	5.949	6.998	ns
8 mA	Slow	3.189	3.752	6.577	7.738	6.131	7.213	6.563	7.721	6.117	7.196	ns
10 mA	Slow	3.241	3.812	6.956	8.184	6.344	7.464	6.942	8.167	6.330	7.447	ns
12 mA	Slow	3.319	3.904	7.076	8.324	6.440	7.577	7.062	8.307	6.426	7.560	ns
LVCMOS 1.8 V (for MSIOD I/O bank)												
2 mA	Slow	2.789	3.282	5.321	6.260	4.980	5.860	5.383	6.333	5.042	5.933	ns
4 mA	Slow	2.332	2.744	5.846	6.878	5.420	6.377	5.908	6.951	5.482	6.450	ns
6 mA	Slow	2.100	2.472	6.497	7.644	5.945	6.994	6.559	7.717	6.007	7.067	ns
8 mA	Slow	2.099	2.470	6.755	7.947	6.142	7.227	6.817	8.020	6.204	7.300	ns
10 mA	Slow	2.136	2.513	7.046	8.290	6.355	7.477	7.108	8.363	6.417	7.550	ns

1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-11A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 34 • LVCMOS 1.5 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
LVCMOS 1.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)		0.65 * VDDI	–	1.575	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC	Input current Low		–	–	10	µA	
LVCMOS 1.5 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI * 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI * 0.25	V	

Table 35 • LVCMOS 1.5 V Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.5 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 5 pF load, maximum drive/slew	–	–	130	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	80	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 10 pF / 500 Ohm load, maximum drive/slew	–	–	170	Mbps	
	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.75	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 36 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)			
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	2 mA	2 mA	VDDI * 0.75	VDDI * 0.25	2	2	
4 mA	4 mA	4 mA	VDDI * 0.75	VDDI * 0.25	4	4	
6 mA	6 mA	6 mA	VDDI * 0.75	VDDI * 0.25	6	6	
8 mA	N/A	8 mA	VDDI * 0.75	VDDI * 0.25	8	8	
N/A	N/A	10 mA	VDDI * 0.75	VDDI * 0.25	10	10	
N/A	N/A	12 mA	VDDI * 0.75	VDDI * 0.25	12	12	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 37 • LVCMOS 1.5 V Receiver Characteristics

		t_{DIN}		t_{SCH_DIN}		
	On-Die Termination (ODT)	–1	Std.	–1	Std.	Units
LVCMOS 1.5 V (for DDRIO I/O bank)	None	2.373	2.792	2.289	2.694	ns
	50	2.495	2.935	2.354	2.770	ns
	75	2.455	2.889	2.344	2.758	ns
	150	2.412	2.838	2.318	2.727	ns
LVCMOS 1.5 V (for MSIO I/O bank)	None	5.219	6.140	5.287	6.221	ns
	50	6.170	7.259	6.477	7.621	ns
	75	5.818	6.845	5.978	7.034	ns
	150	5.489	6.458	5.587	6.573	ns
LVCMOS 1.5 V (for MSIOD I/O bank)	None	3.506	4.125	3.484	4.099	ns
	50	3.831	4.508	3.806	4.478	ns
	75	3.726	4.383	3.700	4.353	ns
	150	3.614	4.251	3.591	4.225	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 38 • LVCMOS 1.5 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.5 V (for DDRIO I/O bank)												
2 mA	Slow	5.122	6.026	5.071	5.966	5.161	6.072	5.453	6.415	4.925	5.795	ns
	Medium	4.611	5.425	4.764	5.605	4.645	5.465	5.146	6.054	4.431	5.213	ns
	Medium fast	4.357	5.127	4.598	5.41	4.391	5.166	4.98	5.859	4.303	5.063	ns
	Fast	4.331	5.096	4.587	5.397	4.365	5.136	4.969	5.846	4.294	5.052	ns

Table 38 • **LVCMOS 1.5 V Transmitter Characteristics (continued)**

Output Drive Selection	Slew Control	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
4 mA	Slow	4.441	5.225	5.816	6.843	5.123	6.028	6.198	7.292	5.505	6.477	ns
	Medium	3.983	4.686	5.571	6.554	4.793	5.639	5.953	7.003	5.175	6.088	ns
	Medium fast	3.756	4.419	5.421	6.378	4.661	5.484	4.803	6.827	5.043	5.933	ns
	Fast	3.732	4.391	5.411	6.366	4.652	5.473	5.793	6.815	5.034	5.922	ns
6 mA	Slow	4.238	4.986	6.212	7.308	5.395	6.348	6.594	7.757	5.777	6.797	ns
	Medium	3.792	4.462	5.909	6.952	5.067	5.962	6.291	7.401	5.449	6.411	ns
	Medium fast	3.566	4.195	5.767	6.785	4.939	5.811	6.149	7.234	5.321	6.26	ns
	Fast	3.543	4.168	5.758	6.774	4.93	5.8	6.14	7.223	5.312	6.249	ns
8 mA	Slow	4.093	4.815	6.387	7.515	5.518	6.493	6.769	7.964	5.9	6.942	ns
	Medium	3.671	4.32	6.116	7.196	5.217	6.139	6.498	7.645	5.599	6.588	ns
	Medium fast	3.454	4.064	5.984	7.04	5.1	6.001	6.366	7.489	5.482	6.45	ns
	Fast	3.43	4.036	5.976	7.031	5.091	5.99	6.358	7.48	5.473	6.439	ns
10 mA	Slow	4.026	4.737	6.536	7.689	5.628	6.622	6.918	8.138	6.01	7.071	ns
	Medium	3.614	4.252	6.27	7.377	5.327	6.268	6.652	7.826	5.709	6.717	ns
	Medium fast	3.399	3.999	6.15	7.235	5.213	6.133	6.532	7.684	5.595	6.582	ns
	Fast	3.376	3.971	6.143	7.227	5.204	6.123	6.525	7.676	5.586	6.572	ns
12 mA	Slow	3.964	4.664	6.639	7.811	5.719	6.729	7.021	8.26	6.101	7.178	ns
	Medium	3.564	4.193	6.387	7.515	5.411	6.366	6.769	7.964	5.793	6.815	ns
	Medium fast	3.357	3.949	6.286	7.396	5.298	6.234	6.668	7.845	5.68	6.683	ns
	Fast	3.334	3.923	6.283	7.392	5.289	6.223	6.665	7.841	5.671	6.672	ns
LVCMOS 1.5 V (for MSIO I/O bank)												
2 mA	Slow	4.437	5.219	5.342	6.285	5.57	6.552	5.295	6.23	5.523	6.497	ns
4 mA	Slow	3.989	4.692	7.006	8.242	6.488	7.633	6.959	8.187	6.441	7.578	ns
6 mA	Slow	4.046	4.76	7.288	8.574	6.664	7.839	7.241	8.519	6.617	7.784	ns
8 mA	Slow	4.226	4.971	7.869	9.257	6.990	8.224	7.822	9.202	6.943	8.169	ns
LVCMOS 1.5 V (for MSIOD I/O bank)												
2 mA	Slow	2.788	3.279	6.125	7.206	5.662	6.661	6.179	7.27	5.716	6.725	ns
4 mA	Slow	2.489	2.927	6.831	8.037	6.24	7.341	6.885	8.101	6.294	7.405	ns
6 mA	Slow	2.508	2.950	7.212	8.484	6.527	7.679	7.266	8.548	6.581	7.743	ns

1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in SmartFusion2 FPGAs in compliance to the JEDEC specification JESD8-12A.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 39 • LVCMOS 1.2 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.14	1.2	1.26	V	
LVCMOS 1.2 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O bank)		0.65 * VDDI	–	1.26	V	
VIH (DC)	DC input logic High (for MSIO I/O bank)		0.65 * VDDI	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.35 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVCMOS 1.2 V DC Output Voltage Specification							
VOH	DC output logic High		VDDI * 0.75	–	–	V	
VOL	DC output logic Low		–	–	VDDI * 0.25	V	

Table 40 • LVCMOS 1.2 V Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.2 V AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: 2 pF load, maximum drive/slew	–	–	75	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2.5 pF load, maximum drive/slew	–	–	50	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 2.5 pF load, maximum drive/slew	–	–	100	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.2 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.6	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 41 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI * 0.75	VDDI * 0.25	2	2	
4 mA	4 mA	4 mA	VDDI * 0.75	VDDI * 0.25	4	4	
N/A	N/A	6 mA	VDDI * 0.75	VDDI * 0.25	6	6	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.14 V

AC Switching Characteristics for Receiver (Input Buffers))

Table 42 • LVCMOS 1.2 V Receiver Characteristics

		t_{DIN}		t_{SCH_DIN}		
	On-Die Termination (ODT)	**–1**	**Std.**	**–1**	**Std.**	**Units**
LVCMOS 1.2 V (for DDRIO I/O bank)	None	2.734	3.218	2.633	3.098	ns
	50	2.931	3.449	2.787	3.28	ns
	75	2.857	3.362	2.735	3.219	ns
	150	2.79	3.284	2.679	3.153	ns
LVCMOS 1.2 V (for MSIO I/O bank)	None	8.548	10.057	8.503	10.004	ns
	50	16.099	18.939	16.646	19.584	ns
	75	12.852	15.121	12.825	15.088	ns
	150	10.345	12.171	10.268	12.080	ns
LVCMOS 1.2 V (for MSIOD I/O bank)	None	4.676	5.502	4.639	5.458	ns
	50	6.485	7.63	6.393	7.522	ns
	75	5.66	6.66	5.599	6.588	ns
	150	5.081	5.978	5.037	5.926	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 43 • LVCMOS 1.2 V Transmitter Characteristics

Output Drive Selection	Slew Control	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.2 V (for DDRIO I/O bank)												
2 mA	Slow	6.003	7.062	6.373	7.498	6.035	7.099	6.879	8.092	5.944	6.992	ns
	Medium	5.32	6.259	6.03	7.094	5.35	6.293	6.536	7.688	5.63	6.622	ns
	Medium fast	4.981	5.86	5.868	6.904	5.005	5.887	6.374	7.498	5.485	6.452	ns
	Fast	4.943	5.816	5.854	6.888	4.958	5.845	6.360	7.482	5.474	6.439	ns
4 mA	Slow	5.446	6.407	7.067	8.314	6.017	7.08	7.573	8.908	6.523	7.674	ns
	Medium	4.814	5.664	6.733	7.922	5.69	6.694	7.239	8.516	6.196	7.288	ns
	Medium fast	4.478	5.269	6.556	7.714	5.548	6.528	7.062	8.308	6.054	7.122	ns
	Fast	4.443	5.227	6.545	7.7	5.538	6.516	7.051	8.294	6.044	7.11	ns
16 mA	Slow	5.241	6.166	7.361	8.661	6.242	7.344	7.867	9.255	6.748	7.938	ns
	Medium	4.644	5.464	7.029	8.269	5.916	6.961	7.535	8.863	6.422	7.555	ns
	Medium fast	4.323	5.086	6.869	8.082	5.779	6.799	7.375	8.676	6.285	7.393	ns
	Fast	4.287	5.044	6.86	8.071	5.77	6.789	7.366	8.665	6.276	7.383	ns
LVCMOS 1.2 V (for MSIO I/O bank)												
2 mA	Slow	5.87	6.905	8.659	10.186	7.563	8.897	8.53	10.035	7.434	8.746	ns
4 mA	Slow	6.215	7.312	9.639	11.339	8.114	9.546	9.51	11.188	7.985	9.395	ns
LVCMOS 1.2 V (for MSIOD I/O bank)												
2 mA	Slow	3.509	4.128	7.29	8.577	6.693	7.874	7.356	8.654	6.759	7.951	ns
4 mA	Slow	3.419	4.022	8.135	9.571	7.347	8.644	8.201	9.648	7.413	8.721	ns

3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 44 • PCI/PCI-X DC Voltage Specification – Applicable to MSIO Bank ONLY

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCIX Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
PCI/PCIX DC Input Voltage Specification							
VI	DC input voltage		0	–	3.45	V	
IIH(DC)	Input current High		–	–	10	µA	
IIL(DC)	Input current Low		–	–	10	µA	
PCI/PCIX DC Output Voltage Specification							
VOH	DC output logic High		Per PCI Specification			V	
VOL	DC output logic Low		Per PCI Specification			V	

Table 45 • PCI/PCI-X Minimum and Maximum AC Input and Output Levels – Applicable to MSIO Bank ONLY

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCI-X AC Specifications							
Fmax	Maximum data rate (MSIO I/O bank)	AC Loading: per JEDEC specifications	–	–	630	Mbps	
PCI/PCI-X AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path (falling edge)		–	0.615 * VDDI	–	V	
Vtrip	Measuring/trip point for data path (rising edge)		–	0.285 * VDDI	–	V	
Rtt_test	Resistance for data test path		–	25	–	Ohms	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 46 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		Speed Grade		Speed Grade		
		–	Std.	–1	Std.	
PCI/PCIX (for MSIO I/O bank)	None	2.25	2.648	2.266	2.667	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 47 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
PCI/PCIX (for MSIO I/O bank)											
	1.995	2.346	5.822	6.849	5.282	6.213	5.992	7.049	5.452	6.413	ns

Memory Interface and Voltage Referenced I/O Standards

High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). SmartFusion2 devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 48 • HSTL DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
VTT	Termination voltage		0.698	0.750	0.803	V	
VREF	Input reference voltage		0.698	0.750	0.803	V	
HSTL DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.1	–	1.575	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	V	
IIL (DC)	Input current Low		–	–	10	V	
HSTL DC Output Voltage Specification							
HSTL Class I							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current (MSIOD I/O bank)		–7.8	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIOD I/O bank)		7.8	–	–	mA	1
IOH at VOH	Output minimum source DC current (MSIO and DDRIO I/O banks)		–8.0	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO and DDRIO I/O banks)		8.0	–	–	mA	
HSTL Class II (Applicable to MSIO and DDRIO I/O Bank Only)							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current		–16.0	–	–	mA	
IOL at VOL	Output minimum sink current		16.0	–	–	mA	
HSTL DC Differential Voltage Specifications							
VID (DC)	DC input differential voltage		0.2	–	–	V	

Notes:

1. *MSIOD I/O bank HSTL Class I does not meet standard JEDEC test point. Use provided lower current values as specified.*

Table 49 • HSTL Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
HSTL AC Differential Voltage Specifications							
VDIFF (AC)	AC input differential voltage		0.4	–	–	V	
Vx (AC)	AC differential cross point voltage		0.68	–	0.9	V	
HSTL AC Specifications							
Fmax	Maximum data rate (DDRIO I/O bank)	AC loading: per JEDEC specifications	–	–	800	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 3 pF / 50 Ohm load	–	–	140	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 3 pF / 50 Ohm load	–	–	180	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistance = 191 Ohms	–	25.5, 47.8	–	Ohms	
RTT	Effective impedance value (with respect to reference resistor of 191 Ohms) (ODT for DDRIO I/O bank only)	Reference resistance = 191 Ohms	–	47.8	–	Ohms	
RTT	Effective impedance value (ODT for MSIO and MSIOD I/O banks only)	Reference resistance = 191 Ohms	–	50, 75, 150	–	Ohms	
HSTL AC Test Parameters Specification							
Vtrip	Measuring/trip point for data path		–	–	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t_{DP})			50		Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 50 • HSTL Receiver Characteristics

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		–1	Std.	–1	Std.	
HSTL (for DDRIO I/O bank)						
Pseudo differential	None	1.739	2.046	1.739	2.046	ns
	47.8	1.745	2.054	1.745	2.054	ns
True differential	None	TBD	TBD	N/A	N/A	ns
	47.8	TBD	TBD	N/A	N/A	ns
HSTL (for MSIO I/O bank)						
Pseudo differential	None	16.01	18.834	9.370	11.023	ns
	50	16.053	18.885	8.986	10.571	ns
	75	16.031	18.859	8.989	10.575	ns
	150	16.015	18.84	9.164	10.781	ns
True differential	None	16.437	19.336	14.424	16.968	ns
	50	16.439	19.339	14.279	16.798	ns
	75	16.391	19.282	14.295	16.817	ns
	150	16.435	19.334	14.357	16.890	ns
HSTL (for MSIOD I/O bank)						
Pseudo differential	None	14.807	17.419	11.828	13.915	ns
	50	14.883	17.508	11.646	13.7	ns
	75	14.832	17.449	11.606	13.654	ns
	150	14.813	17.426	11.572	13.613	ns
True differential	None	13.363	15.721	10.538	12.398	ns
	50	13.555	15.946	10.528	12.386	ns
	75	13.493	15.874	10.436	12.277	ns
	150	13.434	15.804	10.541	12.4	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 51 • HSTL Transmitter Characteristics

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
HSTL Class I											
For DDRIO I/O Bank											
Single-ended	2.753	3.238	2.611	3.072	2.567	3.02	2.623	3.086	2.579	3.034	ns
Differential	2.738	3.221	3.058	3.598	2.998	3.527	3.07	3.612	3.01	3.541	ns
For MSIO I/O Bank											
Single-ended	3.925	4.618	3.401	4	3.333	3.92	3.347	3.938	3.279	3.858	ns
Differential	4.086	4.807	4.043	4.755	3.953	4.649	3.992	4.696	3.902	4.59	ns
For MSIOD I/O Bank											
Single-ended	2.298	2.704	2.308	2.714	2.26	2.658	2.363	2.78	2.315	2.724	ns
Differential	2.49	2.929	2.683	3.156	2.622	3.085	2.739	3.221	2.678	3.15	ns
HSTL Class II											
For DDRIO I/O Bank											
Single-ended	2.649	3.116	2.575	3.03	2.533	2.979	2.587	3.044	2.545	2.993	ns
Differential	2.633	3.098	3.024	3.558	2.965	3.489	3.036	3.572	2.977	3.503	ns

Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in SmartFusion2 devices. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. SmartFusion2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3 and JEDEC standard JESD209A for LPDDR.

Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in SmartFusion2 devices, and also comply with reduced and full drive of double data rate (DDR) standards. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 52 • **DDR1/SSTL2 DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
VTT	Termination voltage		1.164	1.250	1.339	V	
VREF	Input reference voltage		1.164	1.250	1.339	V	
DDR/SSTL2 DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.125	–	2.625	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.15	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Lo		–	–	10	µA	
DDR/SSTL2 DC Output Voltage Specification							
SSTL2 Class I (DDR Reduced Drive)							
VOH	DC output logic High		VTT + 0.608	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.608	V	
IOH at VOH	Output minimum source DC current		8.1	–	–	mA	
IOL at VOL	Output minimum sink current		–8.1	–	–	mA	
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Banks ONLY							
VOH	DC output logic High		VTT + 0.81	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.81	V	
IOH at VOH	Output minimum source DC current		16.2	–	–	mA	
IOL at VOL	Output minimum sink current		–16.2	–	–	mA	
SSTL2 DC Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.3	–	–	V	

Table 53 • DDR1/SSTL2 Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL2 AC Differential Voltage Specification							
VDIFF (AC)	AC input differential voltage		0.7	–	–	V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.2	–	0.5 * VDDI + 0.2	V	
SSTL2 AC Specifications							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specifications	–	–	400	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 10 pF / 50 Ohm load	–	–	575	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 30 pF / 50 Ohm load	–	–	700	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistor = 150 Ohms	–	20, 42	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.25	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL2 Class I (t_{DP})		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL2 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 54 • DDR1/SSTL2 Receiver Characteristics

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		–1	Std.	–1	Std.	
SSTL2 (for DDRIO I/O bank)						
Pseudo differential	None	1.657	1.95	–	–	ns
True differential	None	1.67	1.964	–	–	ns
SSTL2 (for MSIO I/O bank)						
Pseudo differential	None	2.987	3.515	2.805	3.3	ns
True differential	None	2.954	3.474	2.775	3.263	ns
SSTL2 (for MSIOD I/O bank)						
Pseudo differential	None	2.7	3.177	2.545	2.995	ns
True differential	None	2.696	3.172	2.539	2.987	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 55 • DDR1/SSTL2 Transmitter Characteristics

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	
SSTL2 Class I											
For DDRIO I/O Bank											
Single-ended	2.368	2.786	2.216	2.608	2.194	2.581	2.263	2.663	2.241	2.636	ns
Differential	2.383	2.804	2.494	2.934	2.466	2.9	2.54	2.989	2.512	2.955	ns
For MSIO I/O Bank											
Single-ended	2.158	2.539	2.084	2.453	2.063	2.428	2.139	2.517	2.118	2.492	ns
Differential	2.284	2.686	2.436	2.865	2.407	2.832	2.495	2.935	2.466	2.902	ns
For MSIOD I/O Bank											
Single-ended	1.643	1.934	1.689	1.987	1.671	1.966	1.789	2.104	1.771	2.083	ns
Differential	1.786	2.101	1.873	2.204	1.852	2.178	1.973	2.322	1.952	2.296	ns
SSTL2 Class II											
For DDRIO I/O Bank											
Single-ended	2.213	2.604	2.124	2.5	2.104	2.475	2.171	2.555	2.151	2.53	ns
Differential	2.232	2.627	2.45	2.882	2.423	2.85	2.496	2.937	2.469	2.905	ns
For MSIO I/O Bank											
Single-ended	2.383	2.804	2	2.354	1.981	2.331	2.055	2.418	2.036	2.395	ns
Differential	2.502	2.943	2.298	2.704	2.273	2.674	2.357	2.774	2.332	2.744	ns

Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in SmartFusion2 devices, and also comply with the reduced and full drive double date rate (DDR2) standard. SmartFusion2 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 56 • SSTL18 DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.125	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.125	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (MSIO I/O bank only		4.7	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIO I/O bank only)		–4.7	–	–	mA	1
IOH at VOH	Output minimum source DC current (MSIOD I/O bank only		6.3	–	–	mA	1
IOL at VOL	Output minimum sink current (MSIOD I/O bank only)		–6.3	–	–	mA	1
IOH at VOH	Output minimum source DC current (DDRIO I/O bank only		6.5	–	–	mA	1
IOL at VOL	Output minimum sink current (DDRIO I/O bank only)		–6.5	–	–	mA	1

Notes:

1. *MSIO I/O bank SSTL18/DDR2 reduced drive does not have a standard test point. This is defined to fit within the DDR2 reduced drive I/V curve minimums.*
2. *MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.*

Table 56 • SSTL18 DC Voltage Specification (continued)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
STL18 Class II (DDR2 Full Drive) – Applicable to MSIO and DDRIO I/O Banks ONLY							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT– 0.603	V	
IOH at VOH	Output minimum source DC current (MSIO I/O bank only)		9.3	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO I/O bank only)		–9.3	–	–	mA	
IOH at VOH	Output minimum source DC current (DDRIO I/O bank only)		13.4	–	–	mA	
IOL at VOL	Output minimum sink current (DDRIO I/O bank only)		–13.4	–	–	mA	
SSTL18 DC Differential Voltage Specification							
VID (DC	DC input differential voltage		0.3	–	–	V	

Notes:

1. *MSIO I/O bank SSTL18/DDR2 reduced drive does not have a standard test point. This is defined to fit within the DDR2 reduced drive I/V curve minimums.*
2. *MSIO I/O bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.*

Table 57 • SSTL18 Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL18 AC Differential Voltage Specification							
VDIFF (AC)	AC input differential voltage		0.7			V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.175	–	0.5 * VDDI + 0.175	V	
SSTL18 AC Specification							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specification	–	–	800	Mbps	
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 3 pF / 25 Ohm load	–	–	432	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank)	AC loading: 3 pF / 25 Ohm load	–	–	430	Mbps	
Rref	Supported output driver calibrated impedance (for DDRIO I/O bank)	Reference resistor = 150 Ohms	–	20, 42		Ohms	
RTT	Effective impedance value (with respect to reference resistor 150 Ohms) (ODT for DDRIO I/O bank only)	Reference resistor = 150 Ohms	–	50, 75, 150		Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL18 Class I (t_{DP})		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL18 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 58 • DDR2/SSTL18 Receiver Characteristics

	ODT (On-Die Termination)	t_{DIN}		t_{SCH_DIN}		Units
		–1	STD	–1	STD	
SSTL18 (for DDRIO I/O bank)						
Pseudo differential	None	1.7	2.001	N/A	N/A	ns
	50	1.705	2.007	N/A	N/A	ns
	75	1.705	2.007	N/A	N/A	ns
	150	1.705	2.007	N/A	N/A	ns
True differential	None	TBD	TBD	N/A	N/A	ns
	50	TBD	TBD	N/A	N/A	ns
	75	TBD	TBD	N/A	N/A	ns
	150	TBD	TBD	N/A	N/A	ns
SSTL18 (for MSIO I/O bank)						
Pseudo differential	None	5.367	6.315	4.148	4.88	ns
	50	5.438	6.398	4.168	4.904	ns
	75	5.41	6.365	4.148	4.88	ns
	150	5.381	6.331	4.161	4.896	ns
True differential	None	5.664	6.663	5.365	6.312	ns
	50	5.697	6.703	5.308	6.245	ns
	75	5.698	6.704	5.33	6.271	ns
	150	5.688	6.692	5.348	6.292	ns
SSTL18 (for MSIOD I/O bank)						
Pseudo differential	None	4.964	5.84	4.455	5.241	ns
	50	5.027	5.913	4.493	5.285	ns
	75	5.006	5.889	4.48	5.27	ns
	150	4.984	5.862	4.458	5.244	ns
True differential	None	13.396	15.760	11.341	13.342	ns
	50	4.934	5.805	4.45	5.235	ns
	75	4.922	5.791	4.446	5.231	ns
	150	4.908	5.775	4.466	5.255	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 59 • DDR2/SSTL18 Transmitter Characteristics

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	Units
SST18 Class I											
For DDRIO I/O Bank											
Single-ended	2.514	2.957	2.321	2.731	2.287	2.69	2.352	2.768	2.318	2.727	ns
Differential	2.509	2.952	2.865	3.37	2.813	3.309	2.893	3.403	2.841	3.342	ns
For MSIO I/O Bank											
Single-ended	2.791	3.283	2.766	3.254	2.718	3.198	2.749	3.233	2.701	3.177	ns
Differential	2.939	3.458	3.322	3.908	3.256	3.831	3.306	3.888	3.24	3.811	ns
For MSIOD I/O Bank											
Single-ended	1.961	2.306	1.984	2.333	1.948	2.292	2.048	2.409	2.012	2.368	ns
Differential	2.128	2.503	2.24	2.635	2.197	2.584	2.304	2.711	2.261	2.66	ns
SSTL18 Class II											
For DDRIO I/O Bank											
Single-ended	2.409	2.834	2.28	2.682	2.247	2.643	2.311	2.719	2.278	2.68	ns
Differential	2.402	2.826	2.689	3.163	2.643	3.109	2.716	3.196	2.67	3.142	ns
For MSIO I/O Bank											
Single-ended	3.154	3.711	2.675	3.148	2.63	3.095	2.658	3.127	2.613	3.074	ns
Differential	3.286	3.865	3.146	3.701	3.086	3.631	3.13	3.681	3.07	3.611	ns

Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in SmartFusion2 devices, and also comply with the reduced and full drive double data rate (DDR3) standard. SmartFusion2 FPGA I/O supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 60 • SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
VTT	Termination voltage		0.698	0.750	0.803	V	
VREF	Input reference voltage		0.698	0.750	0.803	V	
SSTL15 DC Input Voltage Specification							
VIH(DC)	DC input logic High		VREF + 0.1	–	1.575	V	
VIL(DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
SSTL15 DC Output Voltage Specification							
DDR3/SSTL15 Class I (DDR3 Reduced Drive)							
VOH	DC output logic High		0.8 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current		6.5	–	–	mA	
IOL at VOL	Output minimum sink current		–6.5	–	–	mA	
SSTL15 Class II (DDR3 Full Drive)							
VOH	DC output logic High		0.8 * VDDI	–	–	V	
VOL	DC output logic Low		–	-	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current		7.6	–	–	mA	
IOL at VOL	Output minimum sink current		–7.6	–	–	mA	
SSTL15 Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.2	–	–	V	

Table 61 • SSTL15 Minimum and Maximum AC Input and Output Levels (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL15 Differential Voltage Specification							
VDIFF (AC)	AC input differential voltage		0.7	–	–	V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.150	–	0.5 * VDDI + 0.150	V	
SSTL15 AC Specification							
Fmax	Maximum data rate (for DDRIO I/O bank)	AC loading: per JEDEC specifications			800	Mbps	
Rref	Supported output driver calibrated impedance	Reference resistor = 240 Ohms		34, 40		Ohms	
RTT	Effective impedance value (with respect to reference resistor 240 ohms) (ODT for DDRIO I/O bank only)	Reference resistor = 240 Ohms		20, 30, 40, 60, 120		Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.75	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t_{DP})		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t_{DP})		–	25	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • SSTL15 Receiver Characteristics

	On-Die Termination (ODT)	t_{DIN}		
		–1	Std.	Units
DDR3/SSTL15 (for DDRIO I/O bank)				
Pseudo differential	None	TBD	TBD	ns
	20	1.751	2.060	ns
	30	1.747	2.056	ns
	40	1.753	2.063	ns
	60	1.749	2.058	ns
	120	1.746	2.054	ns
True differential	None	TBD	TBD	ns
	20	TBD	TBD	ns
	30	TBD	TBD	ns
	40	TBD	TBD	ns
	60	TBD	TBD	ns
	120	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 63 • DDR3/SSTL15 Transmitter Characteristics

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	STD	–1	STD	–1	STD	–1	STD	–1	STD	
DDR3 Reduced Drive/SSTL15 Class I											
For DDRIO I/O Bank											
Single-ended	2.689	3.164	2.619	3.082	2.575	3.029	2.63	3.095	2.586	3.042	ns
Differential	2.671	3.142	3.182	3.743	3.118	3.668	3.191	3.754	3.127	3.679	ns
DDR3 Full DriveSSTL15 Class II											
For DDRIO I/O Bank											
Single-ended	2.684	3.158	2.61	3.071	2.566	3.019	2.621	3.094	2.577	3.032	ns
Differential	2.667	3.138	3.178	3.739	3.114	3.664	3.187	3.75	3.123	3.675	ns

Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in SmartFusion2 FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 64 • LPDDR DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input logic High		0.3 * VDDI	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	0.7 * VDDI	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LPDDR DC Output Voltage Specification							
VOH	DC output logic High		0.9 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.1 * VDDI	V	
IOH at VOH	Output minimum source DC current		0.1	–	–	mA	
IOL at VOL	Output minimum sink current		–0.1	–	–	mA	
LPDDR Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.4 * VDDI	–	–	V	
VDIFF (AC)	AC input differential voltage		0.6 * VDDI			V	
Vx (AC)	AC differential cross point voltage		0.4 * VDDI	–	0.6 * VDDI	V	

Table 65 • LPDDR Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LPDDR AC Specifications							
Fmax	Maximum data rate	AC loading: per JEDEC specifications				Mbps	
Rref	Supported output driver calibrated impedance	Reference resistor = 150 Ohms		20, 42		Ohms	
Rtt	Effective impedance value – ODT	Reference resistor = 150 Ohms		50, 70, 150		Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for LPDDR (t_{DP})		–	50	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	Ohms	

AC Switching Characteristics

Table 66 • LPDDR Receiver Characteristics

	On-Die Termination (ODT)	t_{DIN}		Units
		–1	Std.	
LPDDR (for DDRIO I/O Bank)				
Pseudo differential	None	1.707	2.009	ns
	50	1.71	2.012	ns
	75	1.708	2.01	ns
	150	1.707	2.009	ns
True differential	None	1.683	1.98	ns
	50	1.683	1.98	ns
	75	1.683	1.98	ns
	150	1.683	1.98	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 67 • LPDDR Transmitter Characteristics

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LPDDR Reduced Drive											
For DDRIO I/O Bank											
Single-ended	2.455	2.889	2.327	2.737	2.292	2.696	2.358	2.774	2.323	2.733	ns
Differential	2.448	2.88	2.674	3.147	2.628	3.093	2.702	3.18	2.656	3.126	ns
LPDDR Full Drive											
For DDRIO I/O Bank											
Single-ended	2.435	2.865	2.278	2.68	2.245	2.641	2.309	2.717	2.276	2.678	ns
Differential	2.43	2.859	2.774	3.263	2.725	3.205	2.803	3.297	2.754	3.239	ns

Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

Minimum and Maximum Input and Output Levels

Table 68 • **LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	3.45	V	
LVDS DC Input Voltage Specification							
VI	DC Input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		250	350	450	mV	
VOCM	Output common mode voltage		1.125	1.25	1.375	V	
VICM	Input common mode voltage		0.05	1.25	1.375	V	
VID	Input differential voltage		100	350	600	mV	

Table 69 • **LVDS Minimum and Maximum AC Input and Output Levels**

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	535	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – no pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – minimum pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O Bank) – maximum pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance		–	100	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 70 • LVDS Receiver Characteristics

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		–1	Std.	–1	Std.	
LVDS (for MSIO I/O bank)	None	3.034	3.568	2.905	3.417	ns
	100	3.08	3.623	2.883	3.39	ns
LVDS (for MSIOD I/O bank)	None	2.991	3.52	2.68	3.153	ns
	100	3.106	3.655	2.712	3.191	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 71 • LVDS Transmitter Characteristics

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVDS (for MSIO I/O bank)	2.294	2.698	2.493	2.933	2.459	2.892	2.553	3.003	2.519	2.962	ns
LVDS (for MSIOD I/O bank)											
No pre-emphasis	1.765	2.076	1.963	2.31	1.914	2.251	2.063	2.428	2.014	2.369	ns
Min. pre-emphasis	1.666	1.961	1.966	2.313	1.914	2.252	2.066	2.431	2.014	2.37	ns
Max. pre-emphasis	1.616	1.902	1.969	2.317	1.917	2.255	2.069	2.435	2.017	2.373	ns

B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum DC/AC Input and Output Levels Specification

Table 72 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
Bus LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
Bus LVDS DC Output Voltage Specification (for MSIO I/O Bank ONLY)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Bus LVDS Differential Voltage Specification							
VOD	Differential output voltage swing (for MSIO I/O bank ONLY)		240	–	460	mV	
VOCM	Output common mode voltage (for MSIO I/O bank ONLY)		1.1	–	1.5	V	
VICM	Input common mode voltage		0.05	–	2.4 – VID/2	V	
VID	Input differential voltage		100	–	2 * VDDI	mV	

Table 73 • B-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Bus LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank, receiver ONLY)		–	–	–	Mbps	
Rt	Termination resistance		–	27	–	Ohms	
Bus LVDS AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 74 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		Speed Grade		Speed Grade		
		–1	Std.	–1	Std.	
Bus-LVDS (for MSIO I/O Bank)	None	3.024	3.557	2.897	3.407	ns
	100	2.943	3.461	2.834	3.332	ns
Bus-LVDS (for MSIOD I/O Bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 75 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
Bus-LVDS (for MSIO I/O Bank)	2.419	2.846	2.415	2.841	2.383	2.804	2.475	2.911	2.443	2.874	ns

M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

Minimum and Maximum Input and Output Levels

Table 76 • M-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
M-LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	µA	
IIL (DC)	Input current Low		–	–	10	µA	
M-LVDS DC Output Voltage Specification (for MSIO I/O Bank ONLY)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
M-LVDS Differential Voltage Specification							
VOD	Differential output voltage Swing (for MSIO I/O bank ONLY)		480	–	650	mV	
VOCM	Output common mode voltage (for MSIO I/O bank ONLY)		0.3	–	2.1	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		50	–	2400	mV	

Table 77 • M-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Rt	Termination resistance		–	50	–	Ohms	
M-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 78 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		Speed Grade		Speed Grade		
		–1	Std.	–1	Std.	
M-LVDS (for MSIO I/O bank)	None	3.024	3.557	2.898	3.408	ns
	100	2.943	3.462	2.835	3.333	ns
M-LVDS (for MSIOD I/O bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 79 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	Units
M-LVDS (for MSIO I/O bank)	2.419	2.846	2.418	2.845	2.386	2.807	2.478	2.915	2.446	2.877	ns

Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

Mini-LVDS Minimum and Maximum Input and Output Levels

Table 80 • Mini-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
Mini-LVDS DC Input Voltage Specification							
VI	DC Input voltage		0	–	2.925	V	
Mini-LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Mini-LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		300	–	600	mV	
VOCM	Output common mode voltage		1	–	1.4	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		200	–	600	mV	

Table 81 • Mini-LVDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Mini-LVDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank, No pre-emphasis)	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Min. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Med. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Max. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance		50		150	Ohms	
Mini-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 82 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		Speed Grade		Speed Grade		
		–1	Std.	–1	Std.	
Mini-LVDS (for MSIO I/O bank)	None	3.363	3.956	2.95	3.47	ns
	100	3.594	4.228	2.959	3.481	ns
Mini-LVDS (for MSIOD I/O bank)	None	3.439	4.406	2.816	3.313	ns
	100	3.688	4.339	2.839	3.339	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 83 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
Mini-LVDS (for MSIO I/O bank)	2.256	2.654	2.384	2.805	2.354	2.77	2.444	2.875	2.414	2.84	ns
Mini-LVDS (for MSIOD I/O Bank)											
No pre-emphasis	1.775	2.088	1.661	1.953	1.639	1.927	1.76	2.07	1.738	2.044	ns
Min. pre-emphasis	1.765	2.076	1.969	2.317	1.918	2.256	2.069	2.435	2.018	2.374	ns
Med. pre-emphasis	1.666	1.961	1.966	2.313	1.914	2.251	2.066	2.431	2.014	2.369	ns
Max. pre-emphasis	1.616	1.902	1.969	2.317	1.917	2.255	2.069	2.435	2.017	2.373	ns

RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

Minimum and Maximum Input and Output Levels

Table 84 • RSDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
RSDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
RSDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
RSDS Differential Voltage Specification							
VOD	Differential output voltage swing		100	–	600	mV	
VOCM	Output common mode voltage		0.5	–	1.5	V	
VICM	Input common mode voltage		0.3	–	1.5	V	
VID	Input differential voltage		100	–	2 * VDDI	mV	

Table 85 • RSDS Minimum and Maximum AC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
RSDS AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Fmax	Maximum data Rate (for MSIOD I/O banks, No pre-emphasis)	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Min. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Med. pre-emphasis	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Fmax	Maximum data rate (for MSIOD I/O bank) – Max. pre-emphasis)	AC loading: 2 pF / 100 Ohm differential load	–	–	TBD	Mbps	
Rt	Termination resistance			100		Ohms	
AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 86 • AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		Speed Grade		Speed Grade		
		–1	Std.	–1	Std.	
RSDS (for MSIO I/O bank)	None	3.268	3.845	2.955	3.476	ns
	100	3.351	3.942	2.948	3.468	ns
RSDS (for MSIOD I/O bank)	None	2.956	3.477	2.661	3.131	ns
	100	3.231	3.801	2.769	3.258	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 87 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		Units
	–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
RSDS (for MSIO I/O bank)	2.256	2.654	2.384	2.804	2.355	2.77	2.444	2.874	2.415	2.84	ns
RSDS (for MSIOD I/O bank)											
No pre-emphasis	1.775	2.088	1.661	1.953	1.638	1.927	1.76	2.07	1.737	2.044	ns
Min. pre-emphasis	1.765	2.076	1.956	2.313	1.914	2.251	2.066	2.431	2.014	2.369	ns
Med. pre-emphasis	1.666	1.961	1.969	2.317	1.917	2.255	2.069	2.435	2.017	2.373	ns
Max. pre-emphasis	1.616	1.902	1.969	2.316	1.917	2.255	2.069	2.434	2.017	2.373	ns

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. SmartFusion2 devices support only LVPECL receivers and do not support LVPECL transmitters.

Minimum and Maximum Input and Output Levels

Table 88 • LVPECL DC Voltage Specification – Applicable to MSIO I/O Banks Only

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVPECL DC Input Voltage Specification							
VIH (DC)	DC input logic High		–	–	2.3	V	
VIL (DC)	DC input logic Low		1.6	–	–	V	
LVPECL Differential Voltage Specification							
VICM	Input common mode voltage		0.3		2.8	V	
VIDIFF	Input differential voltage		100	300	1,000	mV	

Table 89 • LVPECL Minimum and Maximum AC Input and Output Levels – Applicable to MSIO I/O Banks Only

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVPECL AC Specifications							
Fmax	Maximum data rate (for MSIO I/O bank)		–	–	900	Mbps	

AC Switching Characteristics

Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 90 • LVPECL Receiver Characteristics

	On-Die Termination (ODT)	t_{DIN}		t_{SCH_DIN}		Units
		–1	Std.	–1	Std.	
LVPECL (for MSIO I/O bank)	None	TBD	TBD	TBD	TBD	ns
	100	TBD	TBD	TBD	TBD	ns

I/O Register Specifications

Input Register

Table 91 • Input Data Enable Register Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data register		TBD	TBD	ns
t_{ISUD}	Data Setup Time for the Input Data register		TBD	TBD	ns
t_{IHD}	Data Hold Time for the Input Data register		TBD	TBD	ns
t_{ISUE}	Enable Setup Time for the Input Data register		TBD	TBD	ns
t_{IHE}	Enable Hold Time for the Input Data register		TBD	TBD	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data register		TBD	TBD	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data register		TBD	TBD	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data register		TBD	TBD	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data register		TBD	TBD	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data register		TBD	TBD	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data register		TBD	TBD	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data register		TBD	TBD	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data register		TBD	TBD	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data register		TBD	TBD	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data register		TBD	TBD	ns

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 12 on page 21 for derating values.*

Output/Enable Register

Table 92 • Output Data/Enable Register Propagation Delays
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output/Enable register		TBD	TBD	ns
t_{OSUD}	Data Setup Time for the Output/Enable register		TBD	TBD	ns
t_{OHD}	Data Hold Time for the Output/Enable register		TBD	TBD	ns
t_{OSUE}	Enable Setup Time for the Output/Enable register		TBD	TBD	ns
t_{OHE}	Enable Hold Time for the Output/Enable register		TBD	TBD	ns
t_{OSUSL}	Synchronous Load Setup Time for the Output/Enable register		TBD	TBD	ns
t_{OHSL}	Synchronous Load Hold Time for the Output/Enable register		TBD	TBD	ns
t_{OALn2Q}	Asynchronous Clear-to-Q of the Output/Enable register (ADn = 1)		TBD	TBD	ns
	Asynchronous Preset-to-Q of the Output/Enable register (ADn = 0)		TBD	TBD	ns
$t_{OREMALn}$	Asynchronous Load Removal Time for the Output/Enable register		TBD	TBD	ns
$t_{ORECALn}$	Asynchronous Load Recovery Time for the Output/Enable register		TBD	TBD	ns
t_{OWALn}	Asynchronous Load Minimum Pulse Width for the Output/Enable register		TBD	TBD	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output/Enable register		TBD	TBD	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output/Enable register		TBD	TBD	ns

*Note: *For the derating values at specific junction temperature and voltage supply levels, refer to Table 12 on page 21 for derating values.*

DDR Module Specification

Input DDR Module

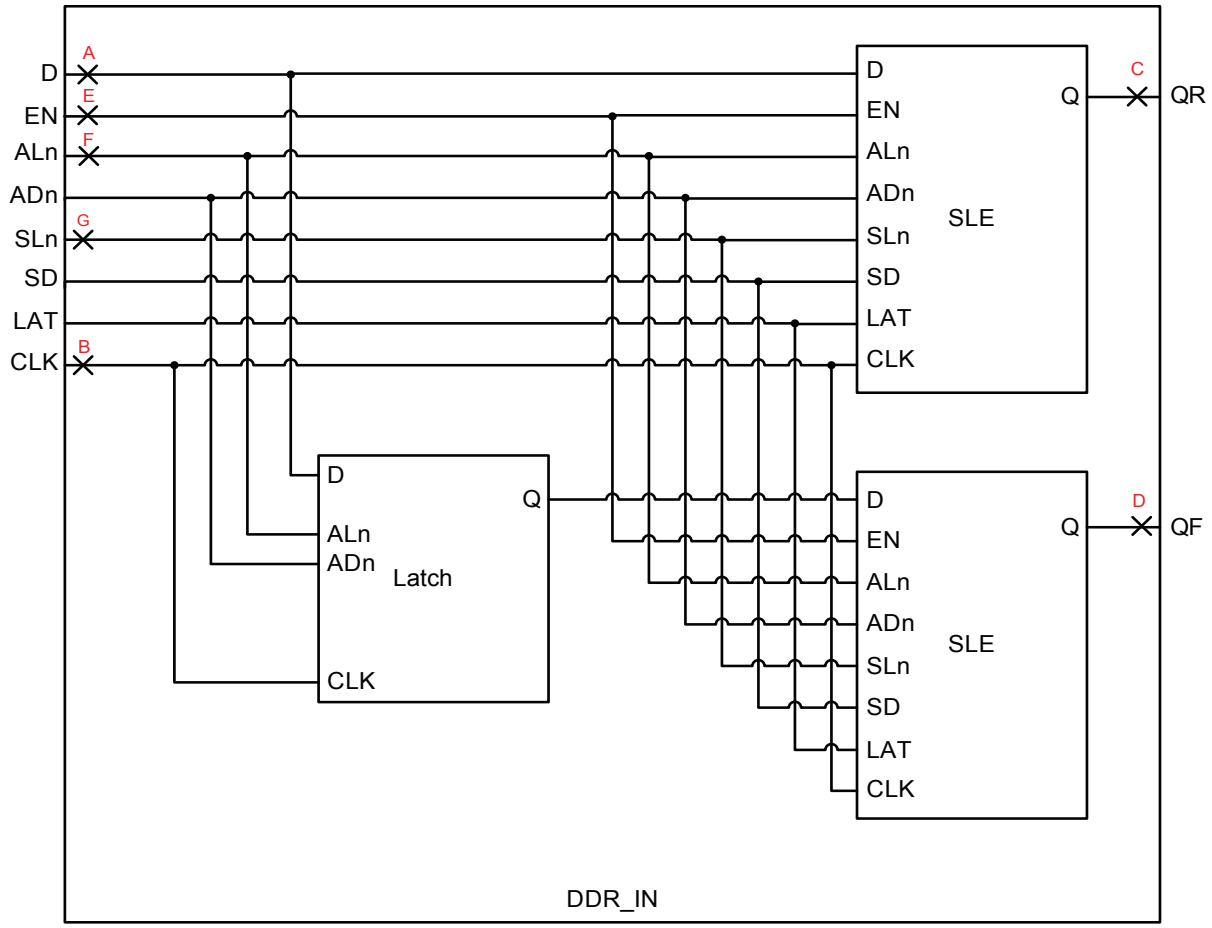


***Figure 3* • Input DDR Module**

Input DDR Timing Diagram

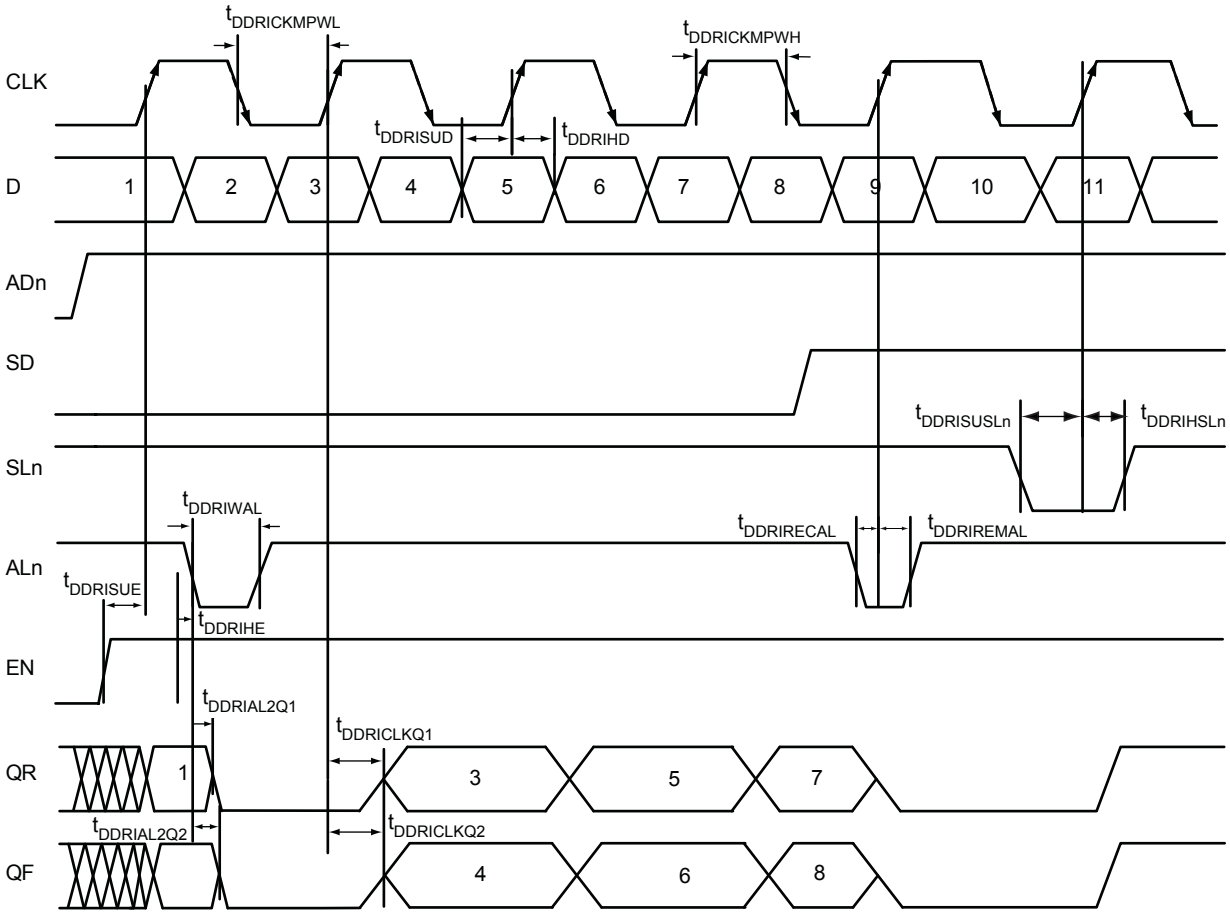


***Figure 4* • Input DDR Timing Diagram**

Timing Characteristics

Table 93 • Input DDR Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	B, C	0.178	0.209	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	B, D	0.175	0.205	ns
$t_{DDRISUD}$	Data Setup for Input DDR	A, B	0.464	0.546	ns
t_{DDRIHD}	Data Hold for Input DDR	A, B	0	0	ns
$t_{DDRISUE}$	Enable Setup for Input DDR	E, B	TBD	TBD	ns
t_{DDRIHE}	Enable Hold for Input DDR	E, B	0	0	ns
$t_{DDRISUSLn}$	Synchronous Load Setup for Input DDR	G, B	0.577	0.679	ns
$t_{DDRIHSLn}$	Synchronous Load Hold for Input DDR	G, B	0	0	ns
$t_{DDRIAL2Q1}$	Asynchronous Load-to-Out QR for Input DDR	F, C	0.618	0.727	ns
$t_{DDRIAL2Q2}$	Asynchronous Load-to-Out QF for Input DDR	F, D	0.569	0.67	ns
$t_{DDRIREMAL}$	Asynchronous Load Removal time for Input DDR	F, B	0	0	ns
$t_{DDRIRECAL}$	Asynchronous Load Recovery time for Input DDR	F, B	0.041	0.048	ns
$t_{DDRIWAL}$	Asynchronous Load Minimum Pulse Width for Input DDR	F, F	0.32	0.376	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	B, B	0.08	0.094	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	B, B	0.068	0.08	ns

Output DDR Module

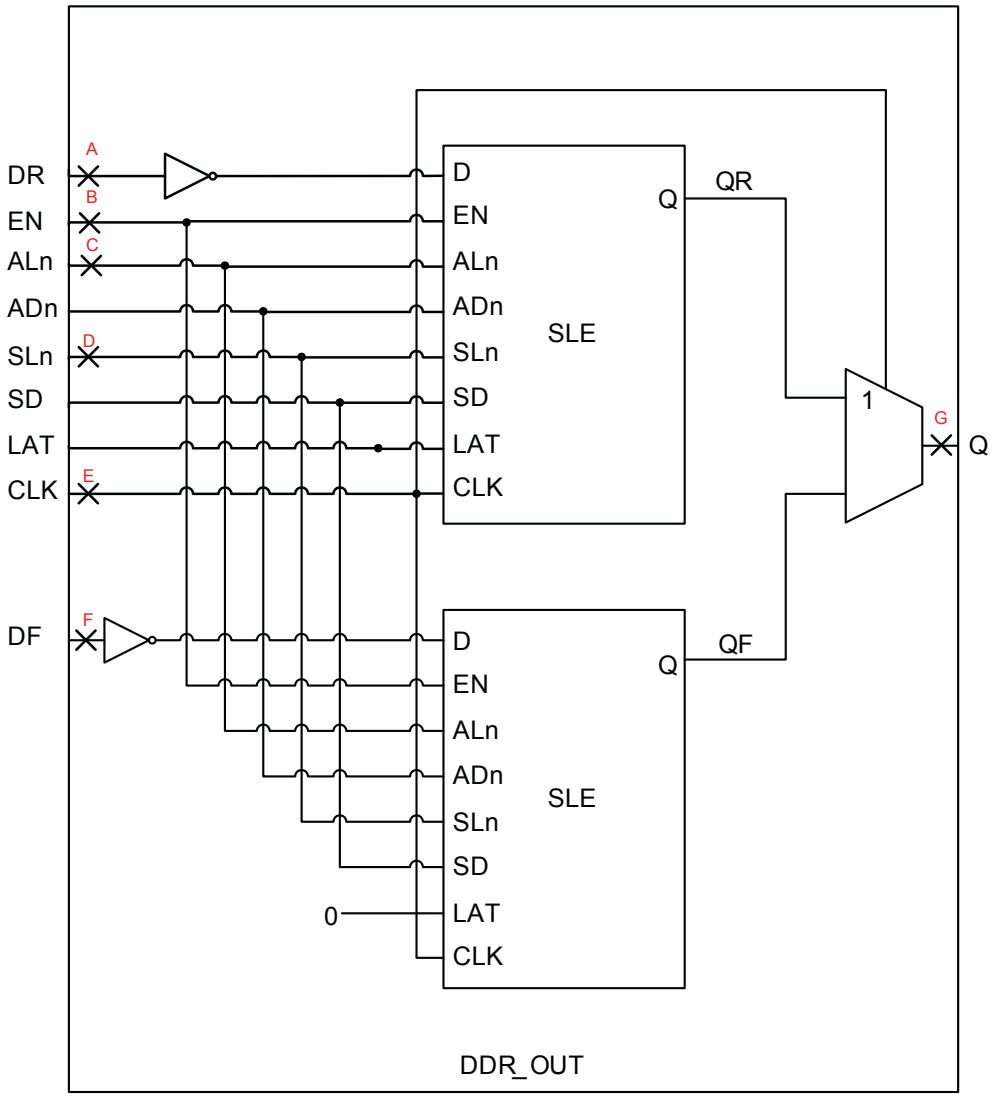


***Figure 5* • Output DDR Module**

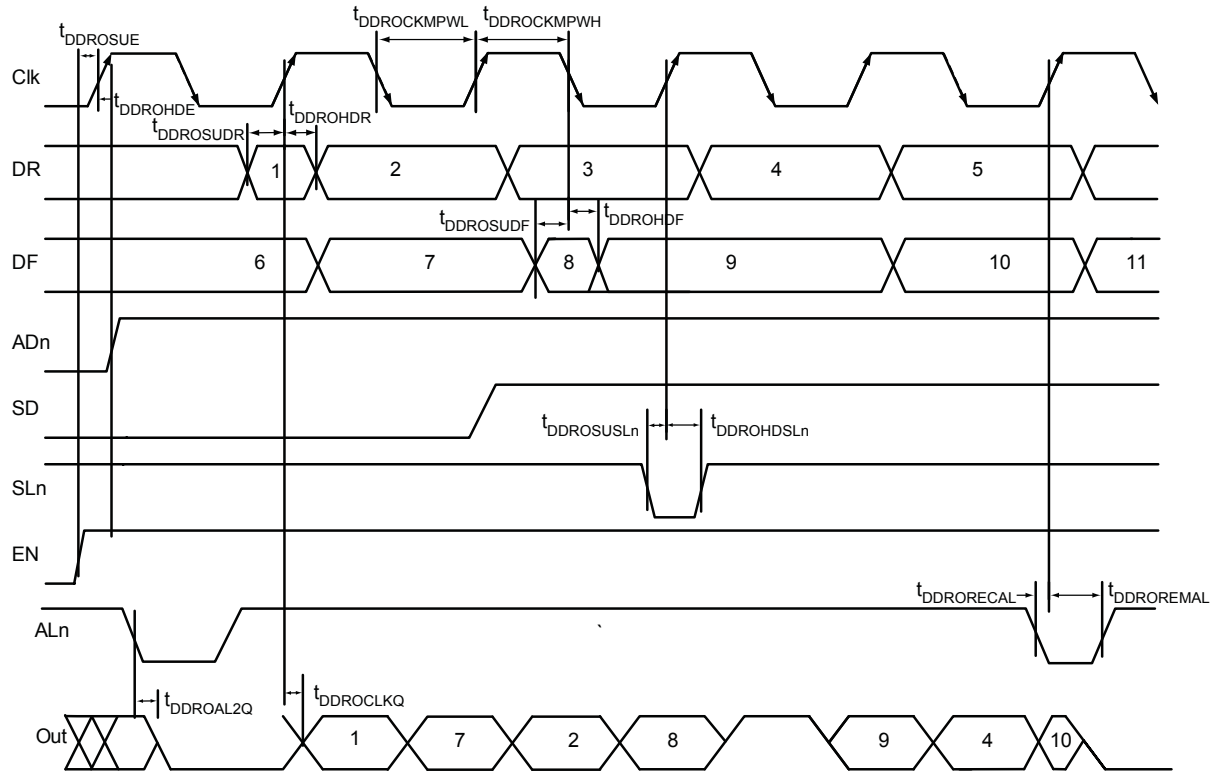


***Figure 6* • Output DDR Timing Diagram**

Timing Characteristics

Table 94 • Output DDR Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	E, G	0.288	0.339	ns
$t_{DDROSUDF}$	Data_F Data Setup for Output DDR	F, E	0.154	0.181	ns
$t_{DDROSUDR}$	Data_R Data Setup for Output DDR	A, E	TBD	TBD	ns
$t_{DDROHDF}$	Data_F Data Hold for Output DDR	F, E	0	0	ns
$t_{DDROHDR}$	Data_R Data Hold for Output DDR	A, E	0	0	ns
$t_{DDROSUE}$	Enable Setup for Input DDR	B, E	0.148	0.174	ns
t_{DDROHE}	Enable Hold for Input DDR	B, E	0	0	ns
$t_{DDROSUSLn}$	Synchronous Load Setup for Input DDR	D, E	0.79	0.93	ns
$t_{DDROHSLn}$	Synchronous Load Hold for Input DDR	D, E	0	0	ns
$t_{DDROAL2Q}$	Asynchronous Load-to-Out for Output DDR	C, G	0.575	0.677	ns
$t_{DDROREMAL}$	Asynchronous Load Removal time for Output DDR	C, E	0	0	ns
$t_{DDRORECAL}$	Asynchronous Load Recovery time for Output DDR	C, E	0.775	0.911	ns
$t_{DDROWAL}$	Asynchronous Load Minimum Pulse Width for Output DDR	C, C	0.191	0.224	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	E, E	0.101	0.119	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	E, E	0.156	0.184	ns

Logic Module Specifications

4-input LUT (LUT-4)

The SmartFusion2 offers a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library.

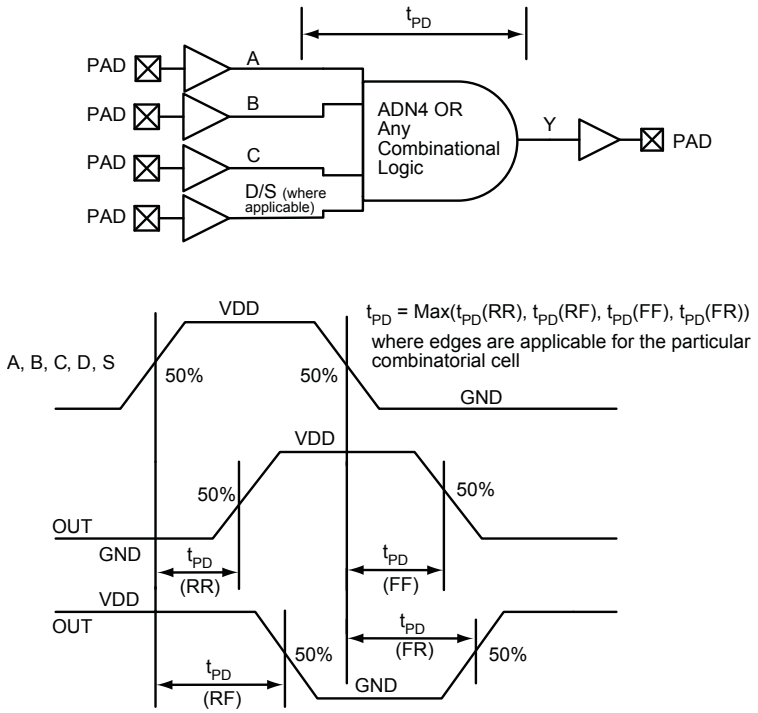


Figure 7 • **LUT-4**

Timing Characteristics

Table 95 • **Combinatorial Cell Propagation Delays**

Combinatorial Cell	Equation	Parameter	–1	Std.	Units	Notes
INV	Y = !A	tPD	0.108	0.127	ns	
AND2	Y = A · B	tPD	0.172	0.203	ns	
NAND2	Y = !(A · B)	tPD	0.16	0.188	ns	
OR2	Y = A + B	tPD	0.172	0.203	ns	
NOR2	Y = !(A + B)	tPD	0.16	0.188	ns	
XOR2	Y = A ⊕ B	tPD	0.172	0.203	ns	
XOR3	Y = A ⊕ B ⊕ C	tPD	0.24	0.283	ns	
AND3	Y = A · B · C	tPD	0.22	0.259	ns	
AND4	Y = A · B · C · D	tPD	0.493	0.58	ns	

Sequential Module

SmartFusion2 offers a separate flip flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

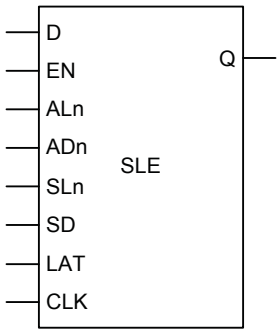


Figure 8 • **Sequential Module**

Figure 9 shows a configuration with SD = 1 (synchronous preset) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

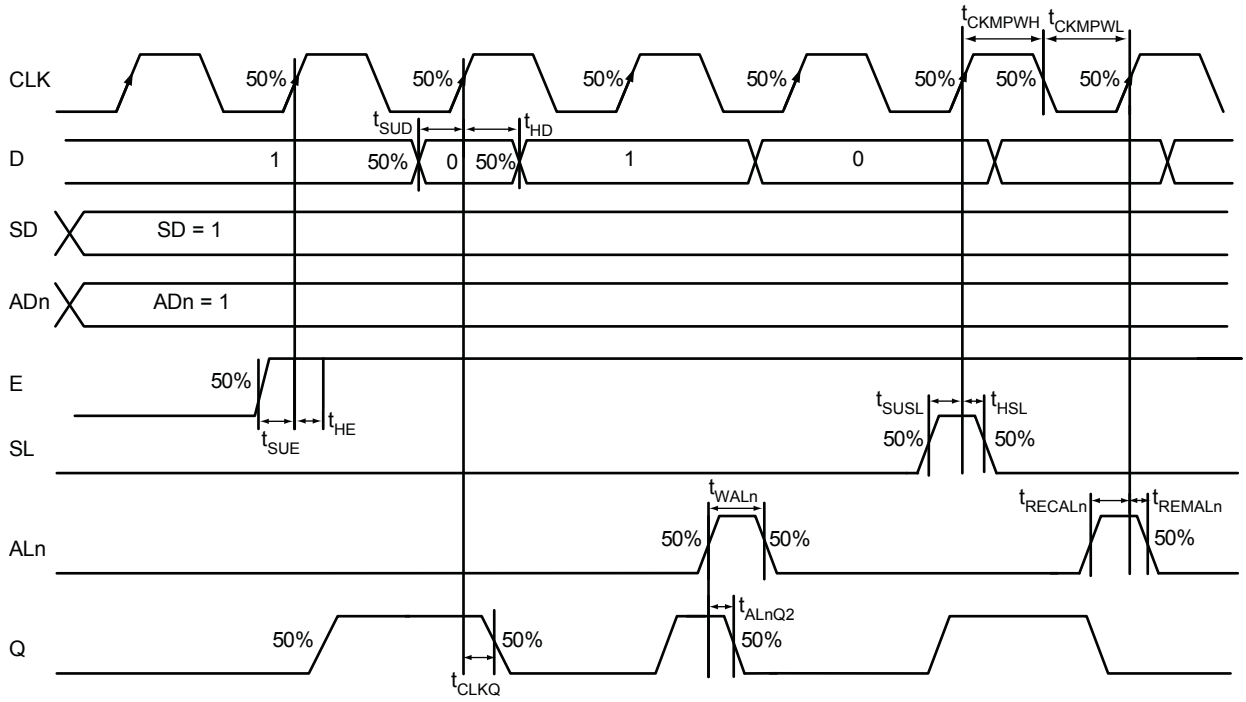


Figure 9 • **Timing Diagram**

Timing Characteristics

Table 96 • Register Delays

Parameter	Description	–1	Std.	Units	Notes
t_{CLKQ}	Clock-to-Q of the Core register	0.114	0.134	ns	
t_{SUD}	Data Setup Time for the Core register	0.267	0.314	ns	
t_{HD}	Data Hold Time for the Core register	0	0	ns	
t_{SUE}	Enable Setup Time for the Core register	0.353	0.415	ns	
t_{HE}	Enable Hold Time for the Core register	0	0	ns	
t_{SUSL}	Synchronous Load Setup Time for the Core register	0.353	0.415	ns	
t_{HSL}	Synchronous Load Hold Time for the Core register	0	0	ns	
t_{ALn2Q}	Asynchronous Clear-to-Q of the Core register (ADn = 1)	0.498	0.586	ns	
	Asynchronous Preset-to-Q of the Core register (ADn = 0)	0.475	0.559	ns	
t_{REMALn}	Asynchronous Load Removal Time for the Core register	0	0	ns	
t_{RECALn}	Asynchronous Load Recovery Time for the Core register	0.371	0.437	ns	
t_{WALn}	Asynchronous Load Minimum Pulse Width for the Core register	0.32	0.376	ns	
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core register	0.079	0.093	ns	
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core register	0.168	0.197	ns	

Global Resource Characteristics

SmartFusion2 devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide* for the positions of various global routing resources.

Table 97 • **M2S050T Global Resource**

Parameter	Description	Speed Grade				Units	Notes
		–1		Std.			
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	TBD	TBD	TBD	TBD	ns	
t_{RCKH}	Input High Delay for Global Clock	TBD	TBD	TBD	TBD	ns	
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	TBD	TBD	TBD	TBD	ns	
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	TBD	TBD	TBD	TBD	ns	
t_{RCKSW}	Maximum Skew for Global Clock	TBD	TBD	TBD	TBD	ns	

FPGA Fabric SRAM

Refer to the *SmartFusion2 FPGA Fabric Architecture User's Guide* for more information.

FPGA Fabric Large SRAM (LSRAM)

Table 98 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1k × 18**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipelined register	–	0.352	–	0.414	ns
	Read access time without pipelined register	–	0.2392	–	2.815	ns
	Access time with feed-through write timing	–	1.609	–	1.893	ns
t_{ADDRSU}	Address setup time	0.457	–	0.538	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.352	–	0.414	–	ns
t_{DHD}	Data hold time	0.103	–	0.121	–	ns
t_{BLKSU}	Block select setup time (with pipelined register enabled)	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time (with pipelined register enabled)	0.13	–	0.153	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
	Block select to out enable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	TBD	–	TBD	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.465	–	0.547	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.061	–	0.072	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.586	–	1.865	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.403	–	0.474	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 99 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2k × 9**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined cock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipelined register	–	0.352	–	0.414	ns
	Read access time without pipelined register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.61	–	1.894	ns
t_{ADDRSU}	Address setup time	0.493	–	0.58	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.346	–	0.408	–	ns
t_{DHD}	Data hold time	0.071	–	0.084	–	ns
t_{BLKSU}	Block select setup time (with pipelined register enabled)	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time (with pipelined register enabled)	0.13	–	0.153	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
	Block select to out enable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	TBD	–	TBD	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN =0)	0.503	–	0.592	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN =0)	0.061	–	0.072	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.594	–	1.875	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.43	–	0.505	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 100 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4k × 4**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipelined register	–	0.34	–	0.4	ns
	Read access time without pipelined register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.591	–	1.872	ns
t_{ADDRSU}	Address setup time	0.564	–	0.664	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.345	–	0.405	–	ns
t_{DHD}	Data hold time	0.071	–	0.084	–	ns
t_{BLKSU}	Block select setup time (with pipelined register enabled)	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time (with pipelined register enabled)	0.13	–	0.153	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
	Block select to out enable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	TBD	–	TBD	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN =0)	0.536	–	0.631	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN =0)	0.061	–	0.072	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.587	–	1.866	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.475	–	0.559	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 101 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8k × 2**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width high	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipelined register	–	0.337	–	0.397	ns
	Read access time without pipelined register	–	2.392	–	2.814	ns
	Access time with feed-through write timing	–	1.591	–	1.872	ns
t_{ADDRSU}	Address setup time	0.637	–	0.749	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.34	–	0.4	–	ns
t_{DHD}	Data hold time	0.071	–	0.084	–	ns
t_{BLKSU}	Block select setup time (with pipelined register enabled)	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time (with pipelined register enabled)	0.13	–	0.153	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
	Block select to out enable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	TBD	–	TBD	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN =0)	0.55	–	0.647	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN =0)	0.061	–	0.072	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.608	–	1.892	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.507	–	0.596	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 102 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16k × 1**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipelined register	–	0.337	–	0.397	ns
	Read access time without pipelined register	–	2.388	–	2.809	ns
	Access time with feed-through write timing	–	1.59	–	1.87	ns
t_{ADDRSU}	Address setup time	0.652	–	0.767	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.332	–	0.39	–	ns
t_{DHD}	Data hold time	0.071	–	0.084	–	ns
t_{BLKSU}	Block select setup time (with pipelined register enabled)	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time (with pipelined register enabled)	0.13	–	0.153	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
	Block select to Out Enable Time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block Select minimum pulse width	TBD	–	TBD	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN =0)	0.551	–	0.648	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN =0)	0.061	–	0.072	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.628	–	1.916	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.471	–	0.554	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

Table 103 • **RAM1K18 – Two-Port Mode for Depth × Width C0nfiguration 512 × 36**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	1.981	–	2.33	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	0.823	–	0.968	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	0.318	–	0.374	–	ns
t_{PLCY}	Pipelined clock period	2.096	–	2.465	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	0.826	–	0.972	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	0.315	–	0.371	–	ns
t_{CLK2Q}	Read access time with pipelined register	–	0.351	–	0.413	ns
	Read access time without pipelined register	–	2.392	–	2.815	ns
t_{ADDRSU}	Address setup time	0.207	–	0.244	–	ns
t_{ADDRHD}	Address hold time	0.077	–	0.09	–	ns
t_{DSU}	Data setup time	0.348	–	0.409	–	ns
t_{DHD}	Data hold time	0.103	–	0.121	–	ns
t_{BLKSU}	Block select setup time (with pipelined register enabled)	0.211	–	0.249	–	ns
t_{BLKHD}	Block select hold time (with pipelined register enabled)	0.027	–	0.032	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
	Block select to out enable time (when pipelined register is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Block select minimum pulse width	TBD	–	TBD	–	ns
t_{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.465	–	0.547	–	ns
t_{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.065	–	0.077	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.703	–	0.827	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	–0.053	–	–0.062	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.586	–	1.865	ns
t_{RSTREM}	Asynchronous reset removal time	0.532	–	0.626	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.005	–	0.006	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.317	–	0.373	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	–0.293	–	–0.345	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.344	–	0.405	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.297	–	0.35	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.231	–	0.271	–	ns
t_{SRSTHD}	Synchronous reset hold time	–0.054	–	–0.063	–	ns
t_{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.403	–	0.474	–	ns
t_{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.053	–	0.063	–	ns

FPGA Fabric Micro SRAM (uSRAM)

Table 104 • **uSRAM (RAM1024x1) in 1024x1 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipelined clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipelined clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipelined clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipelined clock low phase in order to prevent glitches with pipelined register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipelined register	–	0.37	–	0.435	ns
	Read access time with pipelined register in latch mode	–	TBD	–	TBD	ns
	Read access time without pipelined register	–	1.984	–	2.335	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.88	–	2.212	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.131	–	0.154	–	ns
	Read address hold time in asynchronous mode	0.092	–	0.108	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipelined register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.299	–	2.705	ns
	Read block select to out enable time (when pipelined registered is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	TBD	–	TBD	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	TBD	–	TBD	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to output propagation delay (with pipeline register enabled)	–	1.041	–	1.225	ns
	Read asynchronous reset to output propagation delay (with pipeline register disabled)	–	0.824	–	0.97	ns
t_{SRSTSU}	Read synchronous reset setup time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read synchronous reset hold time	0.074	–	0.087	–	ns
t_{CCY}	Write clock period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write clock minimum pulse width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write clock minimum pulse width Low	0.297	–	0.349	–	ns

Table 104 • **uSRAM (RAM1024x1) in 1024x1 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{BLKCSU}	Write block setup time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write block hold time	–0.009	–	–0.011	–	ns
t_{DINCSU}	Write input data setup time	–0.089	–	–0.104	–	ns
t_{DINCHD}	Write input data hold time	0.002	–	0.003	–	ns
$t_{ADDRCSU}$	Write address setup time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write address hold time	0.098	–	0.115	–	ns
t_{WECSU}	Write enable setup time	0.32	–	0.377	–	ns
t_{WECHD}	Write enable hold time	–0.03	–	–0.035	–	ns

Table 105 • **uSRAM (RAM512x2) in 512x2 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read clock period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read clock minimum pulse width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read clock minimum pulse width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read pipelined clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read pipelined clock minimum pulse width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read pipelined clock minimum pulse width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipelined clock low phase in order to prevent glitches with pipelined register in latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read access time with pipelined register	–	0.37	–	0.435	ns
	Read access time with pipelined register in latch mode	–	TBD	–	TBD	ns
	Read access time without pipelined register	–	1.954	–	2.299	ns
t_{ADDRSU}	Read address setup time in synchronous mode	0.294	–	0.345	–	ns
	Read address setup time in asynchronous mode	1.849	–	2.175	–	ns
t_{ADDRHD}	Read address hold time in synchronous mode	0.131	–	0.154	–	ns
	Read address hold time in asynchronous mode	0.092	–	0.108	–	ns
t_{RDENSU}	Read enable setup time	0.245	–	0.289	–	ns
t_{RDENHD}	Read enable hold time	0.074	–	0.087	–	ns
t_{BLKSU}	Read block select setup time (with pipelined register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read block select hold time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)	–	2.272	–	2.673	ns
	Read block select to out enable time (when pipelined registered is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Read block select minimum pulse width	TBD	–	TBD	–	ns
t_{RSTREM}	Read asynchronous reset removal time (pipelined clock)	TBD	–	TBD	–	ns
	Read asynchronous reset removal time (non-pipelined clock)	TBD	–	TBD	–	ns
t_{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.546	–	0.642	–	ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read asynchronous reset to Output Propagation Delay (with pipeline register enabled)	–	1.041	–	1.225	ns
	Read Asynchronous Reset to Output Propagation Delay (with pipeline register disabled)	–	0.937	–	1.102	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.074	–	0.087	–	ns
t_{CCY}	Write Clock Period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write Block Setup Time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write Block Hold Time	–0.009	–	–0.011	–	ns

Table 105 • **uSRAM (RAM512x2) in 512x2 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{DINCSU}	Write Input Data setup Time	–0.025	–	–0.03	–	ns
t_{DINCHD}	Write Input Data hold Time	0.002	–	0.003	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.098	–	0.115	–	ns
t_{WECSU}	Write Enable Setup Time	0.32	–	0.377	–	ns
t_{WECHD}	Write Enable Hold Time	–0.03	–	–0.035	–	ns

Table 106 • **uSRAM (RAM256x4) in 256x4 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read Clock Period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read Pipelined clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read Pipelined clock Minimum Pulse Width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read Pipelined clock Minimum Pulse Width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipelined clock low phase in order to prevent glitches with Pipelined Register in Latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read Access Time with Pipelined register	–	0.37	–	0.435	ns
	Read Access Time with Pipelined register in Latch mode	–	TBD	–	TBD	ns
	Read Access Time without Pipelined register	–	1.933	–	2.275	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous mode	0.294	–	0.345	–	ns
	Read Address Setup Time in Asynchronous mode	1.812	–	2.131	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous mode	0.101	–	0.119	–	ns
	Read Address Hold Time in Asynchronous mode	0.082	–	0.096	–	ns
t_{RDENSU}	Read Enable Setup Time	0.245	–	0.289	–	ns
t_{RDENHD}	Read Enable Hold Time	0.074	–	0.087	–	ns
t_{BLKSU}	Read Block Select Setup Time (with pipelined register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read Block Select Hold Time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when pipelined register is disabled)	–	2.249	–	2.646	ns
	Read Block Select to Out Enable Time (when pipelined registered is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Read Block Select Minimum Pulse Width	TBD	–	TBD	–	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (pipelined clock)	TBD	–	TBD	–	ns
	Read Asynchronous Reset Removal Time (non-pipelined clock)	TBD	–	TBD	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (pipelined clock)	0.546	–	0.642	–	ns
	Read Asynchronous Reset Recovery Time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (with pipeline register enabled)	–	1.042	–	1.226	ns
	Read Asynchronous Reset to Output Propagation Delay (with pipeline register disabled)	–	0.94	–	1.106	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.074	–	0.087	–	ns
t_{CCY}	Write Clock Period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write Block Setup Time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write Block Hold Time	–0.009	–	–0.011	–	ns

Table 106 • **uSRAM (RAM256x4) in 256x4 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{DINCSU}	Write Input Data setup Time	–0.025	–	–0.03	–	ns
t_{DINCHD}	Write Input Data hold Time	0.002	–	0.003	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.088	–	0.103	–	ns
t_{WECSU}	Write Enable Setup Time	0.32	–	0.377	–	ns
t_{WECHD}	Write Enable Hold Time	–0.03	–	–0.035	–	ns

Table 107 • **uSRAM (RAM128x8) in 128x8 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read Clock Period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read Pipelined clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read Pipelined clock Minimum Pulse Width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read Pipelined clock Minimum Pulse Width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipelined clock low phase in order to prevent glitches with Pipelined Register in Latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read Access Time with Pipelined register	–	0.37	–	0.435	ns
	Read Access Time with Pipelined register in Latch mode	–	TBD	–	TBD	ns
	Read Access Time without Pipelined register	–	1.898	–	2.233	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous mode	0.294	–	0.345	–	ns
	Read Address Setup Time in Asynchronous mode	1.791	–	2.107	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous mode	0.101	–	0.119	–	ns
	Read Address Hold Time in Asynchronous mode	0.082	–	0.096	–	ns
t_{RDENSU}	Read Enable Setup Time	0.245	–	0.289	–	ns
t_{RDENHD}	Read Enable Hold Time	0.074	–	0.087	–	ns
t_{BLKSU}	Read Block Select Setup Time (with pipelined register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read Block Select Hold Time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when pipelined register is disabled)	–	2.211	–	2.601	ns
	Read Block Select to Out Enable Time (when pipelined registered is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Read Block Select Minimum Pulse Width	TBD	–	TBD	–	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (pipelined clock)	TBD	–	TBD	–	ns
	Read Asynchronous Reset Removal Time (non-pipelined clock)	TBD	–	TBD	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (pipelined clock)	0.546	–	0.642	–	ns
	Read Asynchronous Reset Recovery Time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (with pipeline register enabled)	–	1.042	–	1.226	ns
	Read Asynchronous Reset to Output Propagation Delay (with pipeline register disabled)	–	0.94	–	1.106	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.074	–	0.087	–	ns
t_{CCY}	Write Clock Period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write Block Setup Time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write Block Hold Time	–0.009	–	–0.011	–	ns

Table 107 • **uSRAM (RAM128x8) in 128x8 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{DINCSU}	Write Input Data setup Time	–0.025	–	–0.03	–	ns
t_{DINCHD}	Write Input Data hold Time	0.002	–	0.003	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.071	–	0.084	–	ns
t_{WECSU}	Write Enable Setup Time	0.32	–	0.377	–	ns
t_{WECHD}	Write Enable Hold Time	–0.03	–	–0.035	–	ns

Table 108 • **uSRAM (RAM128x9) in 128x9 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read Clock Period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read Pipelined clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read Pipelined clock Minimum Pulse Width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read Pipelined clock Minimum Pulse Width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipelined clock low phase in order to prevent glitches with Pipelined Register in Latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read Access Time with Pipelined register	–	0.37	–	0.435	ns
	Read Access Time with Pipelined register in Latch mode	–	TBD	–	TBD	ns
	Read Access Time without Pipelined register	–	1.898	–	2.233	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous mode	0.294	–	0.345	–	ns
	Read Address Setup Time in Asynchronous mode	1.791	–	2.107	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous mode	0.101	–	0.119	–	ns
	Read Address Hold Time in Asynchronous mode	0.082	–	0.096	–	ns
t_{RDENSU}	Read Enable Setup Time	0.245	–	0.289	–	ns
t_{RDENHD}	Read Enable Hold Time	0.074	–	0.087	–	ns
t_{BLKSU}	Read Block Select Setup Time (with pipelined register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read Block Select Hold Time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when pipelined register is disabled)	–	2.211	–	2.601	ns
	Read Block Select to Out Enable Time (when pipelined registered is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Read Block Select Minimum Pulse Width	TBD	–	TBD	–	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (pipelined clock)	TBD	–	TBD	–	ns
	Read Asynchronous Reset Removal Time (non-pipelined clock)	TBD	–	TBD	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (pipelined clock)	0.546	–	0.642	–	ns
	Read Asynchronous Reset Recovery Time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (with pipeline register enabled)	–	1.042	-	1.226	ns
	Read Asynchronous Reset to Output Propagation Delay (with pipeline register disabled)	–	0.94	-	1.106	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.074	–	0.087	–	ns
t_{CCY}	Write Clock Period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write Block Setup Time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write Block Hold Time	–0.009	–	–0.011	–	ns

Table 108 • **uSRAM (RAM128x9) in 128x9 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{DINCSU}	Write Input Data setup Time	–0.025	–	–0.03	–	ns
t_{DINCHD}	Write Input Data hold Time	0.002	–	0.003	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.071	–	0.084	–	ns
t_{WECSU}	Write Enable Setup Time	0.32	–	0.377	–	ns
t_{WECHD}	Write Enable Hold Time	–0.03	–	–0.035	–	ns

Table 109 • **uSRAM (RAM64x16) in 64x16 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read Clock Period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read Pipelined clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read Pipelined clock Minimum Pulse Width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read Pipelined clock Minimum Pulse Width Low	0296	–	0.348	–	ns
t_{CLPL1}	Minimum pipelined clock low phase in order to prevent glitches with Pipelined Register in Latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read Access Time with Pipelined register	–	0.37	–	0.435	ns
	Read Access Time with Pipelined register in Latch mode	–	TBD	–	TBD	ns
	Read Access Time without Pipelined register	–	1.858	–	2.185	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous mode	0.294	–	0.345	–	ns
	Read Address Setup Time in Asynchronous mode	1.755	–	2.064	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous mode	0.055	–	0.064	–	ns
	Read Address Hold Time in Asynchronous mode	0.035	–	0.041	–	ns
t_{RDENSU}	Read Enable Setup Time	0.245	–	0.289	–	ns
t_{RDENHD}	Read Enable Hold Time	0.074	–	0.087	–	ns
t_{BLKSU}	Read Block Select Setup Time (with pipelined register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read Block Select Hold Time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when pipelined register is disabled)	–	2.173	–	2.556	ns
	Read Block Select to Out Enable Time (when pipelined registered is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Read Block Select Minimum Pulse Width	TBD	–	TBD	–	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (pipelined clock)	TBD	–	TBD	–	ns
	Read Asynchronous Reset Removal Time (non-pipelined clock)	TBD	–	TBD	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (pipelined clock)	0.546	–	0.642	–	ns
	Read Asynchronous Reset Recovery Time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (with pipeline register enabled)	–	1.044	–	1.228	ns
	Read Asynchronous Reset to Output Propagation Delay (with pipeline register disabled)	–	0.94	–	1.106	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.074	–	0.087	–	ns
t_{CCY}	Write Clock Period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write Block Setup Time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write Block Hold Time	–0.009	–	–0.011	–	ns

Table 109 • **uSRAM (RAM64x16) in 64x16 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{DINCSU}	Write Input Data setup Time	0.017	–	0.02	–	ns
t_{DINCHD}	Write Input Data hold Time	0.002	–	0.003	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	–0.043	–	–0.05	–	ns
t_{WECSU}	Write Enable Setup Time	0.32	–	0.377	–	ns
t_{WECHD}	Write Enable Hold Time	–0.03	–	–0.035	–	ns

Table 110 • **uSRAM (RAM64x18) in 64x18 Mode**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Read Clock Period	0.836	–	0.984	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	0.296	–	0.348	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	0.324	–	0.382	–	ns
t_{PLCY}	Read Pipelined clock period	1.989	–	2.34	–	ns
$t_{PLCLKMPWH}$	Read Pipelined clock Minimum Pulse Width High	0.259	–	0.305	–	ns
$t_{PLCLKMPWL}$	Read Pipelined clock Minimum Pulse Width Low	0.296	–	0.348	–	ns
t_{CLPL1}	Minimum pipelined clock low phase in order to prevent glitches with Pipelined Register in Latch mode	TBD	–	TBD	–	ns
t_{CLK2Q}	Read Access Time with Pipelined register	–	0.37	–	0.435	ns
	Read Access Time with Pipelined register in Latch mode	–	TBD	–	TBD	ns
	Read Access Time without Pipelined register	–	1.858	–	2.185	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous mode	0.294	–	0.345	–	ns
	Read Address Setup Time in Asynchronous mode	1.755	–	2.064	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous mode	0.055	–	0.064	–	ns
	Read Address Hold Time in Asynchronous mode	0.035	–	0.041	–	ns
t_{RDENSU}	Read Enable Setup Time	0.245	–	0.289	–	ns
t_{RDENHD}	Read Enable Hold Time	0.074	–	0.087	–	ns
t_{BLKSU}	Read Block Select Setup Time (with pipelined register enabled)	1.901	–	2.237	–	ns
t_{BLKHD}	Read Block Select Hold Time (with pipelined register enabled)	0.001	–	0.001	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when pipelined register is disabled)	–	2.173	–	2.556	ns
	Read Block Select to Out Enable Time (when pipelined registered is disabled)	–	TBD	–	TBD	ns
t_{BLKMPW}	Read Block Select Minimum Pulse Width	TBD	–	TBD	–	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (pipelined clock)	TBD	–	TBD	–	ns
	Read Asynchronous Reset Removal Time (non-pipelined clock)	TBD	–	TBD	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (pipelined clock)	0.546	–	0.642	–	ns
	Read Asynchronous Reset Recovery Time (non-pipelined clock)	0.085	–	0.099	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (with pipeline register enabled)	–	1.05	–	1.236	ns
	Read Asynchronous Reset to Output Propagation Delay (with pipeline register disabled)	–	0.944	–	1.11	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.25	–	0.294	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.074	–	0.087	–	ns
t_{CCY}	Write Clock Period	1.49	–	1.752	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.506	–	0.596	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.297	–	0.349	–	ns
t_{BLKCSU}	Write Block Setup Time	0.332	–	0.39	–	ns
t_{BLKCHD}	Write Block Hold Time	–0.009	–	–0.011	–	ns

Table 110 • **uSRAM (RAM64x18) in 64x18 Mode (continued)**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{DINCSU}	Write Input Data setup Time	0.017	–	0.02	–	ns
t_{DINCHD}	Write Input Data hold Time	0.002	–	0.003	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.012	–	0.015	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	–0.043	–	–0.05	–	ns
t_{WECSU}	Write Enable Setup Time	0.32	–	0.377	–	ns
t_{WECHD}	Write Enable Hold Time	–0.03	–	–0.035	–	ns

On-Chip Oscillators

Table 111 through Table 113 on page 107 describe the electrical characteristics of the available on-chip oscillators in SmartFusion2 devices.

Table 111 • **Electrical Characteristics of the Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
FXTAL	Operating frequency		–	32	–	kHz	
ACCXTAL	Accuracy	Temperature: 0°C to 85°C	TBD	TBD	TBD	%	
CYCXTAL	Output duty cycle		TBD	TBD	TBD	%	
JITXTAL	Output jitter	Period jitter	TBD	TBD	TBD	ps RMS	
		Cycle-to-cycle jitter	TBD	TBD	TBD	ps	
IDYNXTAL	Operating current		TBD	TBD	TBD	mA	
ISTBXTAL	Standby current of crystal oscillator		TBD	TBD	TBD	µA	
PSRRXTAL	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
ENXTAL	Enable Time		TBD	TBD	TBD	µs	
VIHXTAL	Input logic level High		TBD	TBD	TBD	V	
VILXTAL	Input logic level Low		TBD	TBD	TBD	V	
SUXTAL	Startup time	Test load used:	TBD	TBD	TBD	µs	

Table 112 • **Electrical Characteristics of the 25/50 MHz RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F25_50RC	Operating frequency		–	25/50	–	MHz	
ACC25_50RC	Accuracy	Temperature: 0°C to 85°C	TBD	TBD	TBD	%	
CYC25_50RC	Output duty cycle		TBD	TBD	TBD	%	
JIT25_50RC	Output jitter	Period jitter	TBD	TBD	TBD	ps RMS	
		Cycle-to-cycle jitter	TBD	TBD	TBD	ps	
IDYN25_50RC	Operating current		TBD	TBD	TBD	mA	
ISTB25_50RC	Standby current of crystal oscillator		TBD	TBD	TBD	µA	
PSRR25_50RC	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
VIH25_50RC	Input logic level High		TBD	TBD	TBD	V	
VIL25_50RC	Input logic level Low		TBD	TBD	TBD	V	
SU25_50RC	Startup time	Test load used:	TBD	TBD	TBD	µs	

Table 113 • **Electrical Characteristics of the 1 MHz RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F1RC	Operating frequency		–	1	–	MHz	
ACC1RC	Accuracy	Temperature: 0°C to 85°C	TBD	TBD	TBD	%	
CYC1RC	Output duty cycle		TBD	TBD	TBD	%	
JIT1RC	Output jitter	Period jitter	TBD	TBD	TBD	ps RMS	
		Cycle-to-cycle jitter	TBD	TBD	TBD	ps	
IDYN1RC	Operating current		TBD	TBD	TBD	mA	
ISTB1RC	Standby current of crystal oscillator		TBD	TBD	TBD	µA	
PSRR1RC	Power supply noise tolerance		TBD	TBD	TBD	Vp-p	
EN1RC	Enable Time		TBD	TBD	TBD	µs	
VIH1RC	Input logic level High		TBD	TBD	TBD	V	
VIL1RC	Input logic level Low		TBD	TBD	TBD	V	
SU1RC	Startup time	Test load used:	TBD	TBD	TBD	µs	

Clock Conditioning Circuits (CCC)

Table 114 • **SmartFusion2 CCC/PLL Specification**

Parameter			**Minimum**	**Typical**	**Maximum**	**Units**	**Notes**
Clock conditioning circuitry input frequency f_{IN_CCC}			1		200	MHz	
Clock conditioning circuitry output frequency f_{OUT_CCC}			20		400	MHz	
Delay increments in programmable delay blocks				100		ps	
Number of programmable values in each programmable delay block					64		
Acquisition time					500	µs	
Tracking jitter				TBD		ns	
Output duty cycle			48		52	%	
Feedback delay					8	ns	
CCC output peak-to-peak period jitter FCCC_OUT	Maximum peak-to-peak period jitter						
	SSO = 0	0 < SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16		
	FG896	FG896	FG896	FG896	FG896		
20 MHz to 100 MHz	1	TBD	TBD	TBD	TBD	% f_{OUT_CCC}	
100 MHz to 200 MHz	1	TBD	TBD	TBD	TBD	% f_{OUT_CCC}	
200 MHz to 400 MHz	1	TBD	TBD	TBD	TBD	% f_{OUT_CCC}	
Spread Spectrum Characteristics							
Modulation frequency range			25	35	50	kHz	
Modulation depth range			0		1.5	%	
Modulation depth control				0.5		%	

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 10 on page 110.

Table 115 • **SPI Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	M2S050T	Unit
sp1	SPI_x_CLK minimum period		
	SPI_x_CLK = PCLK/2	–	ns
	SPI_x_CLK = PCLK/4	TBD	ns
	SPI_x_CLK = PCLK/8	TBD	ns
	SPI_x_CLK = PCLK/16	TBD	µs
	SPI_x_CLK = PCLK/32	TBD	µs
	SPI_x_CLK = PCLK/64	TBD	µs
	SPI_x_CLK = PCLK/128	TBD	µs
	SPI_x_CLK = PCLK/256	TBD	µs
sp2	SPI_x_CLK minimum pulse width High		
	SPI_x_CLK = PCLK/2	–	ns
	SPI_x_CLK = PCLK/4	TBD	ns
	SPI_x_CLK = PCLK/8	TBD	ns
	SPI_x_CLK = PCLK/16	TBD	µs
	SPI_x_CLK = PCLK/32	TBD	µs
	SPI_x_CLK = PCLK/64	TBD	µs
	SPI_x_CLK = PCLK/128	TBD	µs
	SPI_x_CLK = PCLK/256	TBD	us
sp3	SPI_x_CLK minimum pulse width Low		
	SPI_x_CLK = PCLK/2	–	ns
	SPI_x_CLK = PCLK/4	TBD	ns
	SPI_x_CLK = PCLK/8	TBD	ns
	SPI_x_CLK = PCLK/16	TBD	µs
	SPI_x_CLK = PCLK/32	TBD	µs
	SPI_x_CLK = PCLK/64	TBD	µs
	SPI_x_CLK = PCLK/128	TBD	µs
	SPI_x_CLK = PCLK/256	TBD	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%)	TBD	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%)	TBD	ns
sp6	Data from master (SPI_x_DO) setup time	TBD	pclk cycles
sp7	Data from master (SPI_x_DO) hold time	TBD	pclk cycles
sp8	SPI_x_DI setup time	TBD	pclk cycles
sp9	SPI_x_DI hold time	TBD	pclk cycles

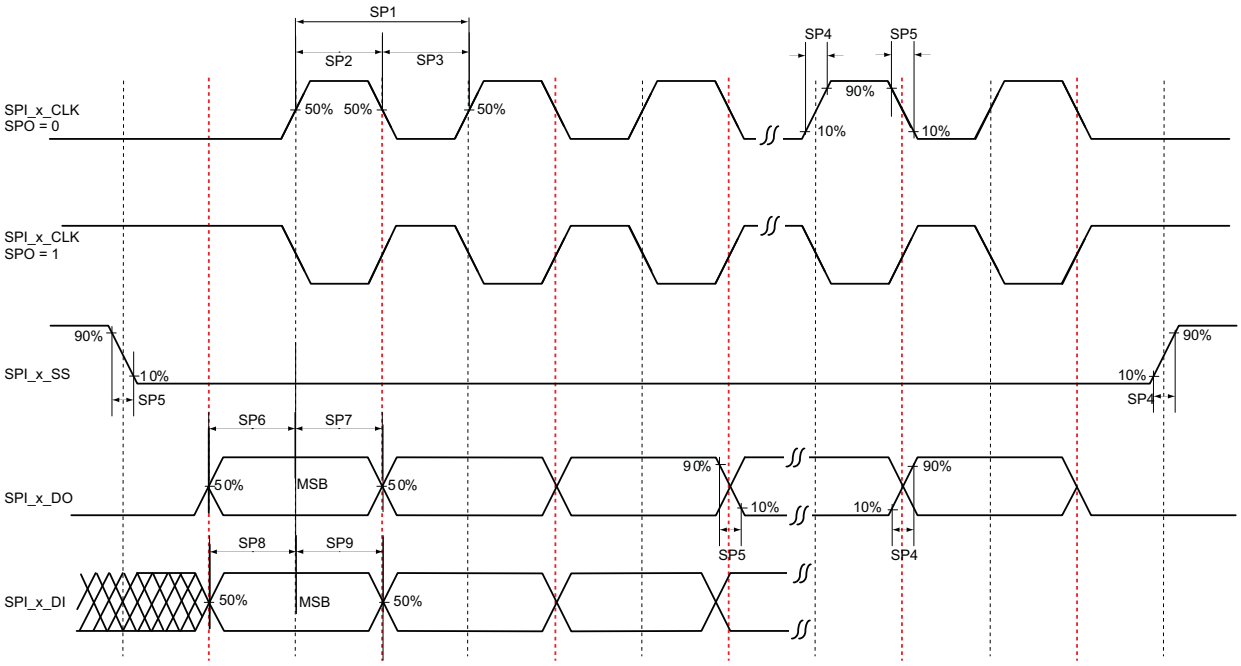


***Figure 10* • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 11 on page 112.

Table 116 • **I^2C Characteristics**
Commercial Case Conditions: T_J = 85ºC, VDD = 1.14 V, –1 Speed Grade

Parameter	Definition	Condition	Value	Unit
VIL	Minimum input low voltage	–	See Table 19 on page 29	–
	Maximum input low voltage	–	See Table 19	–
VIH	Minimum input high voltage	–	See Table 19	–
	Maximum input high voltage	–	See Table 19	–
VOL	Maximum output voltage low	IOL = TBD	See Table 19	–
IIL	Input current High	–	See Table 19	–
IIH	Input current Low	–	See Table 19	–
Vhyst	Hysteresis of Schmitt trigger inputs	–	See Table 18 on page 28	V
T_{FALL}	Fall time	VIHmin to VILMax, Cload = 400 pF	TBD	ns
		VIHmin to VILMax, Cload = 100 pF	TBD	ns
T_{RISE}	Rise time	VILMax to VIHmin, Cload = 400 pF	TBD	ns
		VILMax to VIHmin, Cload = 100 pF	TBD	ns
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	TBD	pF
$R_{pull-up}$	Output buffer maximum pull-down resistance	–	TBD	Ω
$R_{pull-down}$	Output buffer maximum pull-up resistance	–	TBD	Ω
D_{max}	Maximum data rate	Fast mode	TBD	Kbps
t_{LOW}	Low period of I2C_x_SCL	–	TBD	pclk cycles
t_{HIGH}	High period of I2C_x_SCL	–	TBD	pclk cycles
$t_{HD;STA}$	START hold time	–	TBD	pclk cycles
$t_{SU;STA}$	START setup time	–	TBD	pclk cycles
$t_{HD;DAT}$	DATA hold time	–	TBD	pclk cycles
$t_{SU;DAT}$	DATA setup time	–	TBD	pclk cycles
$t_{SU;STO}$	STOP setup time	–	TBD	pclk cycles
t_{FILT}	Maximum spike width filtered	–	TBD	ns

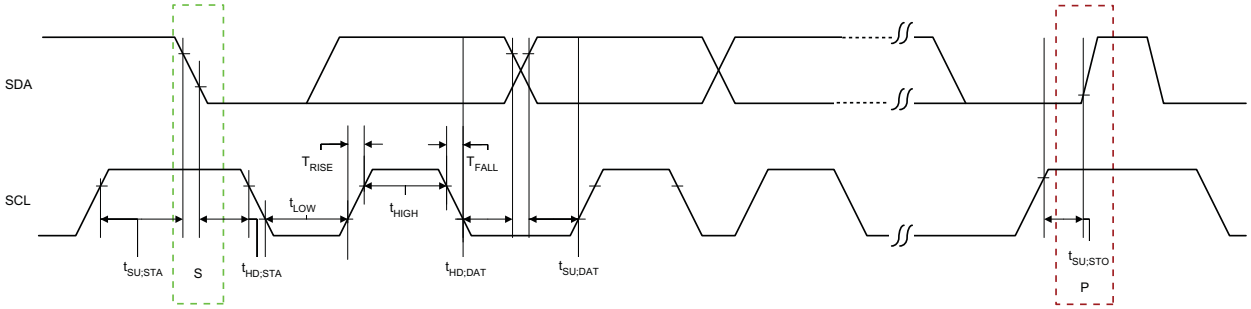


***Figure 11* • I2C Timing Parameter Definition**

Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the datasheet.

Revision	Changes	Page
Revision 3 (February 2013)	SmartFusion2 product brief and pin information has been removed from the datasheet and published in separate documents: *SmartFusion2 Product Brief* and *SmartFusion2 Pin Descriptions* (SAR 45184).	N/A
Revision 2 (February 2013)	Table 1 • Absolute Maximum Ratings and Table 2 • Recommended Operating Conditions were updated with the new pin names and latest values (SAR 45081).	7, 8
	The storage temperature minimum value was added to Table 1 • Absolute Maximum Ratings, including a note with references to additional tables (SAR 44887).	7
	In EQ 1 , $T_J - \theta_A$ was corrected to $T_J - T_A$ (SAR 44109).	10
	Timing tables were updated with respect to slew and configuration. AC and DC specifications were placed in separate tables. Values were added to replace TBD in a number of tables in the "User I/O Characteristics" section (SAR 44471).	24
	The termination scheme for the differential I/O test setup in the "Output Buffer and AC Loading" section was corrected (SAR 43591).	25
	The worst commercial-case conditions for Table 27 • LVCMOS 2.5 V Receiver Characteristics were changed from VDDI = 3.0 V to VDDI = 2.375 V (SAR 44471).	32
	The following tables were revised to remove typical and minimum Fmax values and change maximum Fmax values (SAR 44471): Table 68 • LVDS DC Voltage Specification Table 80 • Mini-LVDS DC Voltage Specification Table 84 • RSDS DC Voltage Specification	 63 69 71
	Table 99 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2k × 9 through Table 102 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16k × 1 are new (SAR 44471).	87 to 90
	Table 104 • uSRAM (RAM1024x1) in 1024x1 Mode through Table 109 • uSRAM (RAM64x16) in 64x16 Mode are new (SAR 44471).	92 to 102
Revision 1 (January 2013)	Table 1 • Absolute Maximum Ratings is new. In Table 2 • Recommended Operating Conditions, the expression "VDDI0" in the values for VREFx was corrected to "VDDIx." VCCENVM was corrected to VPPNVM (SAR 42461). VDDIx was defined differently for different types of I/O banks (SAR 43850).	7, 8
	The "Power Supply Sequencing and Power-On Reset (Commercial and Industrial)" section was revised to correct the available ramp rate options from "50 µs, 100 µs, 1 ms, and 100 ms" to "50 µs, 1 ms, 10 ms, and 100 ms." Each selection represents the maximum ramp rate to apply to VDD and VPP. The user can set the ramp rate setting using Libero SOC (SARs 41970, 42401).	9
	The units for input leakage current (IIL/IIH) were corrected from mA to µA in the DC voltage tables (SAR 43848).	29 to 41
	A note to reference IBIS models for a detailed I/V curve was added to transmitter drive strength tables for LVTTL/LVCMOS 3.3 V through LVCMOS 1.2 V (SAR 42171). For more information, refer to the *IBIS Models: Background and Usage* application note.	30 to 41

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in Table 1 on page 1 is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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