SY89847U

1.5 GHz Precision LVDS 1:5 Fanout with 2:1 MUX and Fail Safe Input with Internal Termination

Features

- Selects Between Two Sources and Provides 5 Precision LVDS Copies
- Fail Safe Input Prevents Outputs from Oscillating when Input is Invalid
- Guaranteed AC Performance over Temperature and Supply Voltage:
  - DC-to >1.5 GHz Throughput
  - <1000 ps Propagation Delay (IN-to-Q)
  - <210 ps Rise/Fall Times
- Ultra-Low Jitter Design:
  - <1 ps_{RMS} Random Jitter
  - <1 ps_{RMS} Cycle-to-Cycle Jitter
  - <10 ps_{PP} Total Jitter (Clock)
  - <0.7 ps_{RMS} MUX Crosstalk Induced Jitter
- Unique, Patented MUX Input Isolation Design Minimizes Adjacent Channel Crosstalk
- Unique, Patented Internal Termination and V_T Pin Accepts DC- and AC-Coupled Inputs (CML, PECL, LVDS)
- Wide Input Voltage Range V_{CC} to GND
- 2.5V ±5% Supply Voltage
- –40°C to +85°C Industrial Temperature Range
- Available in 32-Pin (5 mm x 5 mm) QFN Package

Applications

- Fail Safe Clock Protection
- Ultra-Low Jitter LVDS Clock Distribution
- Rack-Based Telecom/Datacom

Markets

- LAN/WAN
- Enterprise Servers
- ATE
- Test and Measurement

General Description

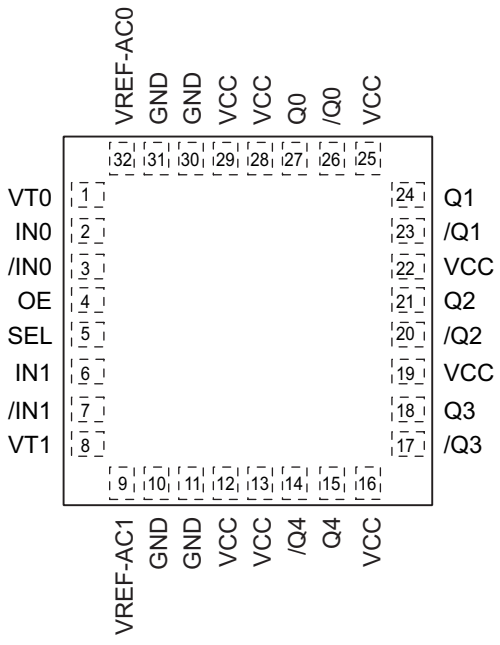
The SY89847U is a 2.5V, 1:5 LVDS fanout buffer with a 2:1 differential input multiplexer (MUX). A unique fail safe input (FSI) protection prevents metastable output conditions when the selected input clock fails to a DC voltage (voltage between the pins of the differential input drops significantly below 100 mV).

The differential input includes Microchip's unique, 3-pin internal termination architecture that can interface to any differential signal (AC- or DC-coupled) as small as 100 mV (200 mV_{PP}) without any level shifting or termination resistor networks in the signal path. The outputs are LVDS compatible with very fast rise/fall times guaranteed to be less than 210 ps.

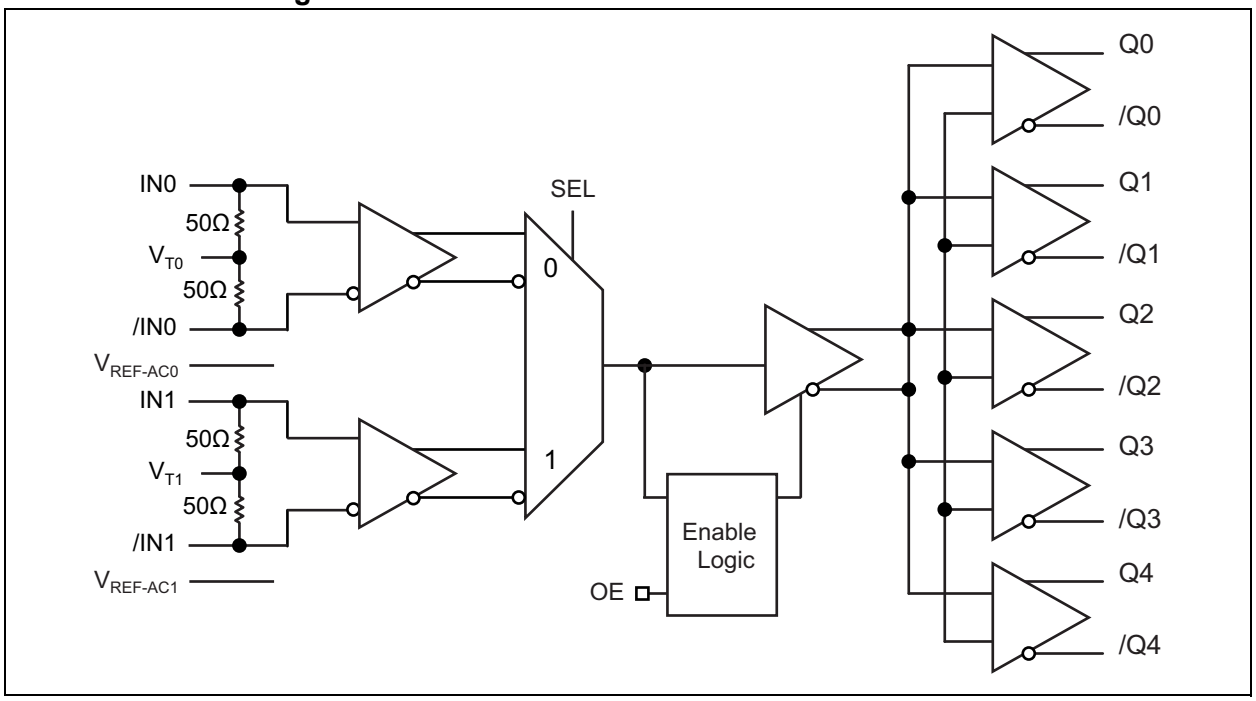
The SY89847U operates from a 2.5V ±5% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89847U is part of Microchip's high-speed, Precision Edge® product line.

Package Type

SY89847U
5 mm x 5 mm QFN-32 (M)
(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
    Continuous ..... 50 mA
    Surge ..... 100 mA
Current (V_T)
    Source or Sink on V_T Pin ..... ±100 mA
Input Current
    Source or Sink Current on IN, /IN ..... ±50 mA
Current (V_{REF})
    Source or Sink Current on V_{REF-AC} (Note 1) ..... ±0.5 mA

Operating Ratings ††

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: T_A = –40°C to +85°C, unless otherwise stated.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply	V_{CC}	2.375	2.5	2.625	V	—
Power Supply Current	I_{CC}	—	90	130	mA	No load, max. V_{CC}
Input Resistance (IN-to-V_T)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN-to-/IN)	R_{DIFF_IN}	90	100	110	Ω	—
Input High Voltage (IN, /IN)	V_{IH}	0.1	—	V_{CC}	V	—
Input Low Voltage (IN, /IN)	V_{IL}	0	—	V_{IH} – 0.1	V	—
Input Voltage Swing (IN, /IN)	V_{IN}	0.1	—	1.0	V	Note 2, See Figure 5-6
Different Input Voltage Swing |IN, /IN|	V_{DIFF_IN}	0.2	—	2.0	V	See Figure 5-7
Input Voltage Threshold that Triggers FSI	V_{IN_FSI}	—	30	100	mV	—
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V	$I_{VREF-AC}$ = ±0.5 mA
Voltage from Input to V_T	V_{T_IN}	—	—	1.28	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: $V_{IN(MAX)}$ is specified when V_T is floating.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: V_{CC} = +2.5V ±5%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output Voltage Swing (Q, /Q)	V_{OUT}	250	325	—	mV	See Figure 5-6
Differential Output Voltage Swing |Q, /Q|	V_{DIFF_OUT}	500	650	—	mV	See Figure 5-7
Output Common Mode Voltage (Q, /Q)	V_{OCM}	1.125	1.20	1.275	V	See Figure 7-1
Change in Common Mode Voltage (Q, /Q)	ΔV_{OCM}	–50	—	50	mV	See Figure 7-2

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input High Current	I_{IH}	–125	—	30	µA	—
Input Low Current	I_{IL}	–300	—	—	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: V_{CC} = 2.5V ±5%, R_L = 100Ω across the outputs, Input t_r/t_f ≤300 ps; T_A = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Maximum Operating Frequency	f_{MAX}	1.5	2.0	—	GHz	V_{OUT} ≥ 200 mV, V_{IN} ≥ 200 mV
		1.0	1.5	—		V_{OUT} ≥ 200 mV, V_{IN} ≥ 100 mV
Differential Propagation Delay IN-to-Q	t_{pd}	600	820	1100	ps	Note 2, 100 mV < V_{IN} ≤ 200 mV
Differential Propagation Delay IN-to-Q		500	720	1000		Note 2, IN-to-Q, 200 mV < V_{IN} ≤ 800 mV
Differential Propagation Delay SEL-to-Q		400	600	800		V_{TH} = V_{CC}/2
Set-Up Time OE-to-IN	t_S	300	—	—	ps	Note 3
Hold Time IN-to-OE	t_H	800	—	—	ps	Note 3
Differential Propagation Delay Temperature Coefficient	t_{pd} tempco	—	256	—	fs/°C	—
Output-to-Output Skew	t_{SKEW}	—	5	20	ps	Note 4
Input-to-Input Skew		—	5	15		Note 5
Part-to-Part Skew		—	—	300		Note 6
Clock Random Jitter	t_{JITTER}	—	—	1	ps_{RMS}	Note 7
Cycle-to-Cycle Jitter		—	—	1	ps_{RMS}	Note 8
Total Jitter		—	—	10	ps_{PP}	Note 9
Crosstalk-Induced Jitter		—	—	0.7	ps_{RMS}	Note 10

AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Note 1)

Electrical Characteristics: V_{CC} = 2.5V ±5%, R_L = 100Ω across the outputs, Input t_r/t_f ≤300 ps; T_A = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output Rise/Fall Time (20% - 80%)	t_r/t_f	70	120	210	ps	At full output swing.
Duty Cycle	—	47	—	53	%	V_{IN} >200 mV
		45	—	55		100 mV ≤ V_{IN} ≤ 200 mV

Note 1: High-frequency AC parameters are guaranteed by design and characterization.

2: Propagation delay is measured with input t_r, t_f ≤300 ps (20% to 80%). The propagation delay is a function of the rise and fall times at IN. See Typical Performance Curves for details. t_{pd} varies with input t_r/t_f.

3: Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.

4: Output-to-Output skew is measured between two different outputs under identical transitions.

5: Input-to-Input skew is the time difference between the two inputs to one output, under identical input transitions.

6: Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

7: Random Jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.

8: Cycle-to-Cycle Jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.

9: Total Jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

10: Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	–40	—	+85	°C	—
Maximum Operating Junction Temperature	T_J	—	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, 5x5 QFN-32Ld	θ_{JA}	—	50	—	°C/W	Still-air
	Ψ_{JB}	—	31	—	°C/W	Junction-to-board

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 2.5V, GND = 0V, t_r/t_f ≤300 ps, V_{IN} = 100 mV, R_L = 100Ω across the outputs, T_A = +25°C, unless otherwise stated.

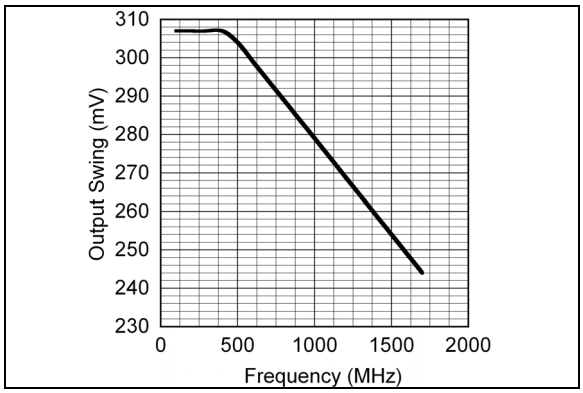


FIGURE 2-1: *Frequency Response.*

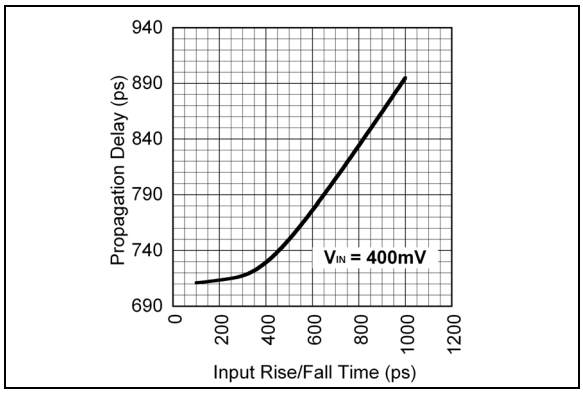


FIGURE 2-4: *Propagation Delay vs. Input Rise/Fall Time.*

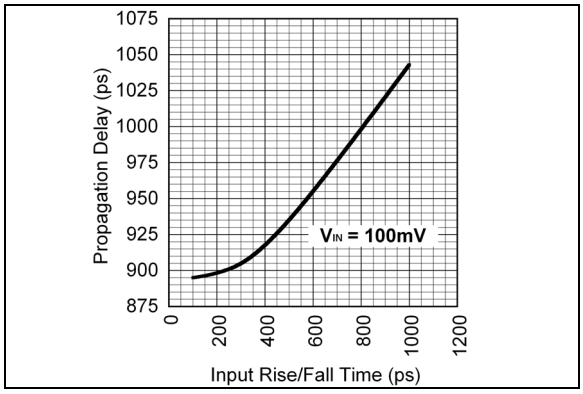


FIGURE 2-2: *Propagation Delay vs. Input Rise/Fall Time.*

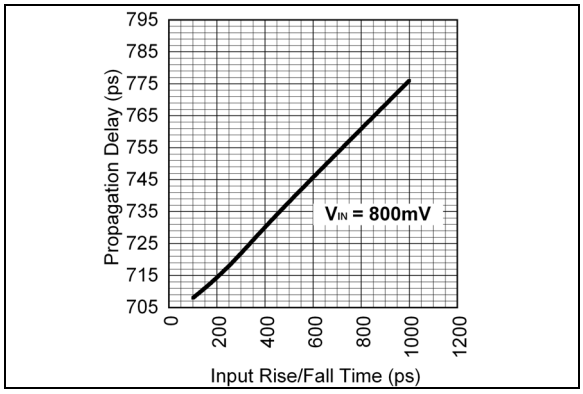


FIGURE 2-5: *Propagation Delay vs. Input Rise/Fall Time.*

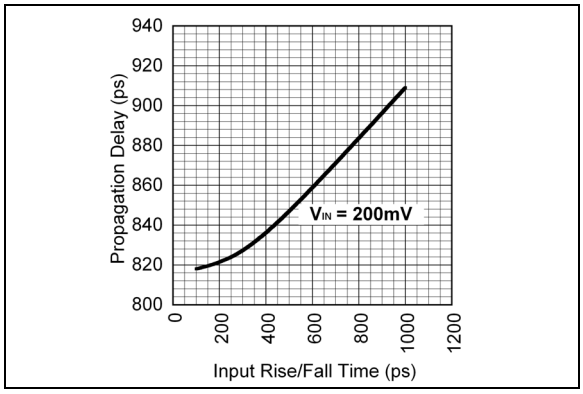


FIGURE 2-3: *Propagation Delay vs. Input Rise/Fall Time.*

V_{CC} = 2.5V, GND = 0V, V_{IN} = 250 mV, R_L = 100Ω across the outputs, T_A = +25°C, unless otherwise stated.

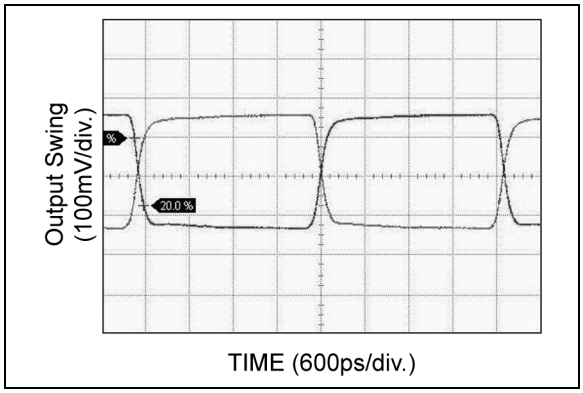


FIGURE 2-6: *200 MHz Clock.*

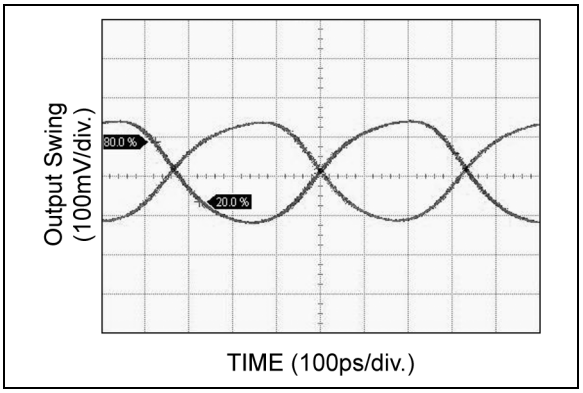


FIGURE 2-9: *1.5 GHz Clock.*

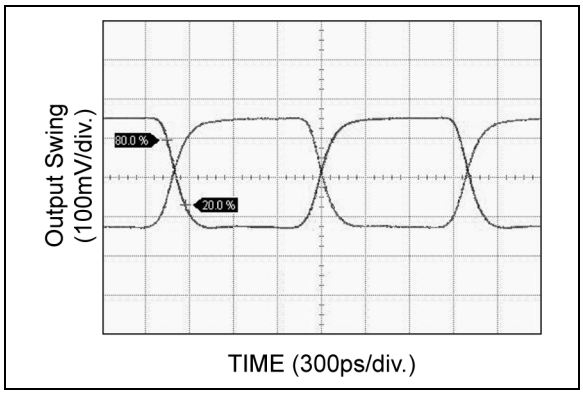


FIGURE 2-7: *500 MHz Clock.*

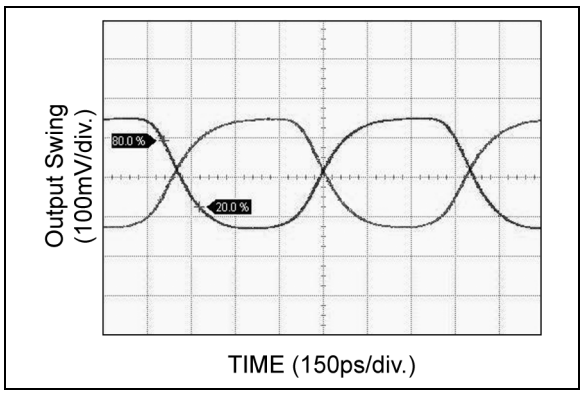


FIGURE 2-8: *1 GHz Clock.*

3.0 ADDITIVE PHASE NOISE PLOT

Additive jitter is defined as the RMS Jitter of the device added to the input signal and is calculated in Equation 3-1.

EQUATION 3-1:

$$DeviceAdditiveJitter = \sqrt{OutputRMSJitter^2 - InputRMSJitter^2}$$

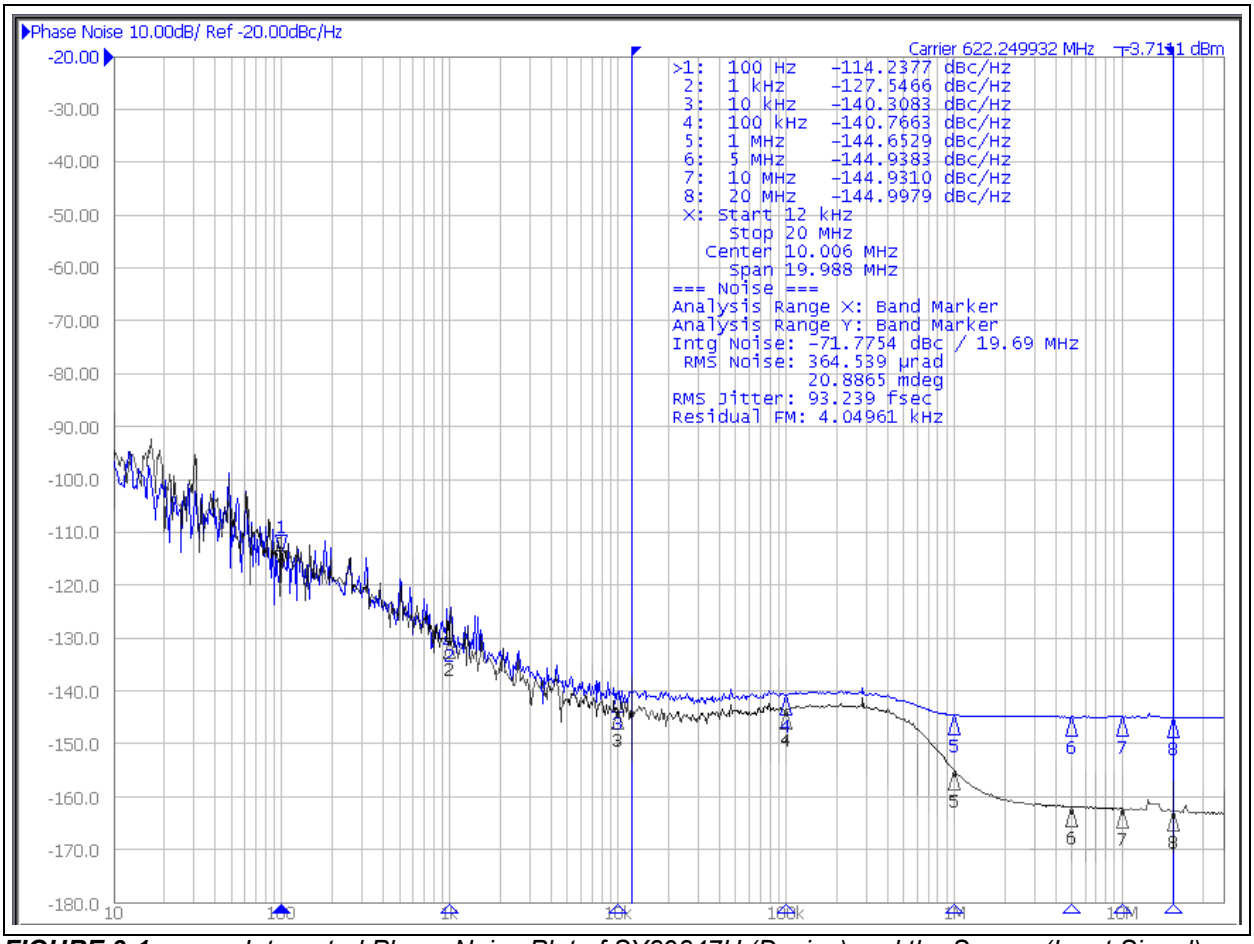


FIGURE 3-1: *Integrated Phase Noise Plot of SY89847U (Device) and the Source (Input Signal).*

From the plot shown in Figure 3-1, the device additive jitter can be calculated as follows.

EQUATION 3-2:

$$CalculatedAdditiveJitter = \sqrt{93.23^2 - 22.84^2} = 90.39fs$$

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1, 8	VT0, VT1	Input Termination Center-Tap: Each side of a differential input pair terminates to the VT pin. The VT pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See the Input Interface Applications section.
2, 3 6, 7	IN0, /IN0 IN1, /IN1	Differential Inputs: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100 mV. The input pairs internally terminate to a VT pin through 50Ω. Each input has level shifting resistors of 3.72 kΩ to VCC. This allows a wide input voltage range from VCC to GND. See Figure 5-8, Simplified Differential Input Stage for details. Note that these inputs will default to a valid (either high or low) state if left open. See the Input Interface Applications section.
10, 11, 30, 31	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
4	OE	Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q4 outputs. It is internally connected to a 25 kΩ pull-up resistor and will default to a logic high state if left open. When disabled, Q goes low and /Q goes high. OE being synchronous, outputs will be enabled/disabled following a rising and a falling edge of the input clock. $V_{TH} = V_{CC}/2$.
5	SEL	Single-Ended Input: This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic high state if left open. $V_{TH} = V_{CC}/2$.
9, 32	VREF-AC1 VREF-AC0	Reference Voltage: These outputs bias to V_{CC} – 1.2V. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01 µF low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is ±0.5 mA. See the Input Interface Applications section.
12, 13, 16, 19, 22, 25, 28, 29	VCC	Positive Power Supply: Bypass with 0.1 µF||0.01 µF low ESR capacitors as close to the VCC pins as possible.
27, 26 24, 23 21, 20 18, 17 15, 14	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3 Q4, /Q4	LVDS Differential Output Pairs: Differential copies of the selected input signal. The output swing is typically 325 mV. Used and unused outputs must be terminated with 100Ω across the pair (Q, /Q). These differential LVDS outputs are a logic function of the IN0, IN1, and SEL inputs. See Table 4-2.

TABLE 4-2: TRUTH TABLE

Inputs					Outputs	
IN0	**/IN0**	**IN1**	**/IN1**	**SEL**	**Q**	**/Q**
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

5.0 FUNCTIONAL DESCRIPTION

5.1 Clock Select (SEL)

SEL is an asynchronous TTL/CMOS compatible input that selects one of the two input signals. Internal 25 kΩ pull-up resistor defaults the input to logic high if left open. Input switching threshold is $V_{CC}/2$. Refer to Figure 5-1.

5.2 Output Enable (OE)

OE is a synchronous TTL/CMOS compatible input that enables/disables the outputs based on the input to this pin. The enable function is synchronous so that the clock outputs will be enabled or disabled following a rising and a falling edge of the input clock. Refer to Figure 5-2. Internal 25 kΩ pull-up resistor defaults the input to logic high if left open. Input switching threshold is $V_{CC}/2$.

5.3 Fail-Safe Input (FSI)

The input includes a special fail-safe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below 100 mV_{PK} (200 mV_{PP}), typically 30 mV_{PK}. Refer to Figure 5-4.

5.4 Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing such that the voltage swing across the input pair is significantly less than 100 mV, FSI function will eliminate a metastable condition and latch the outputs to the last valid state. No ringing and no undetermined state will occur at the output under these conditions. The output recovers to normal operation once the input signal returns to a valid state with a typical swing greater than 30 mV.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to the Typical Performance Curves for detailed information.

Timing Diagrams

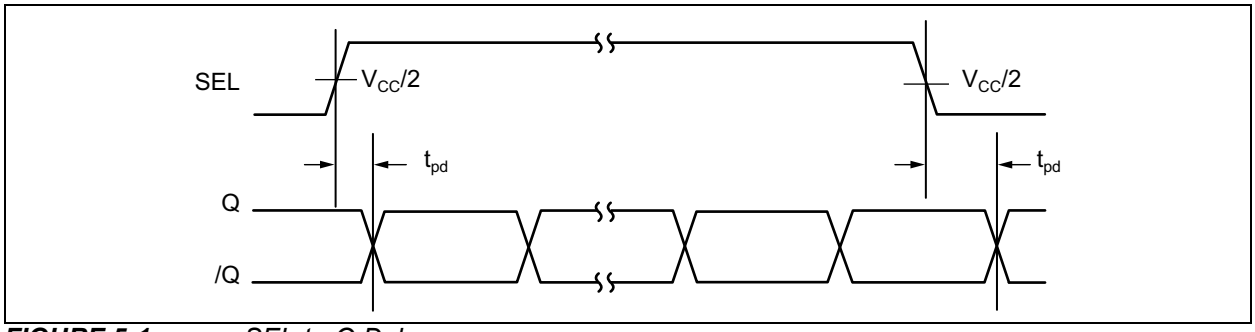


FIGURE 5-1: *SEL-to-Q Delay.*

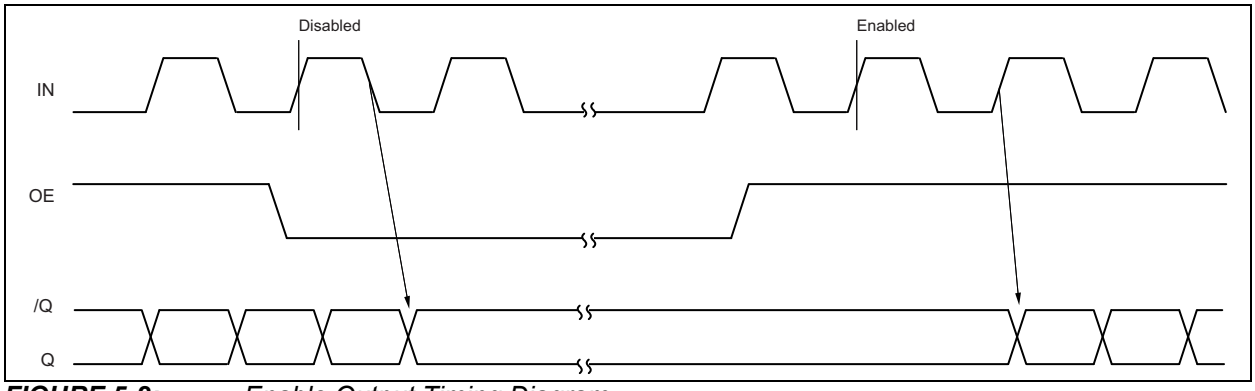


FIGURE 5-2: *Enable Output Timing Diagram.*

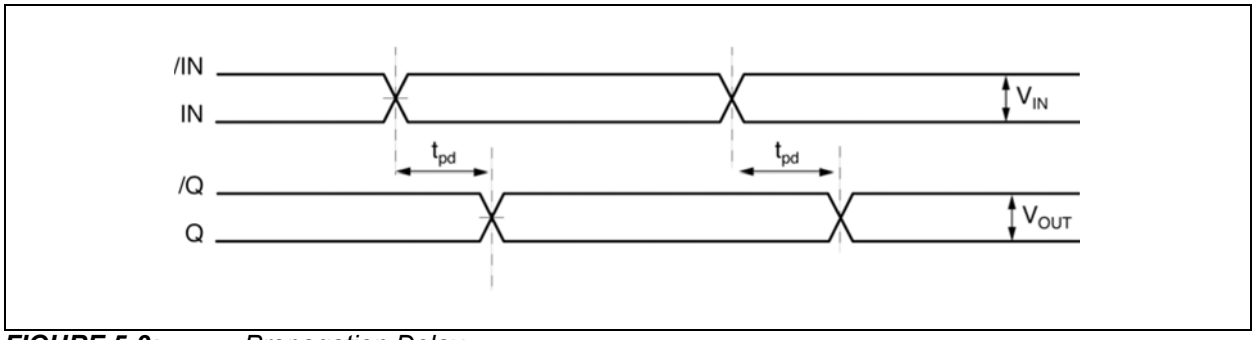


FIGURE 5-3: *Propagation Delay.*

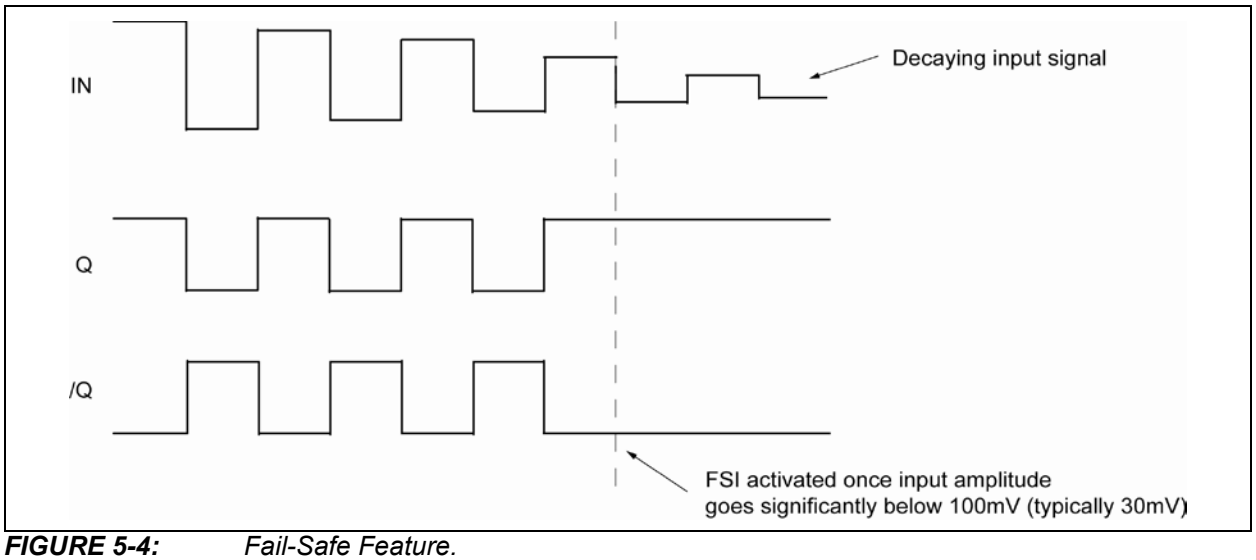


FIGURE 5-4: *Fail-Safe Feature.*

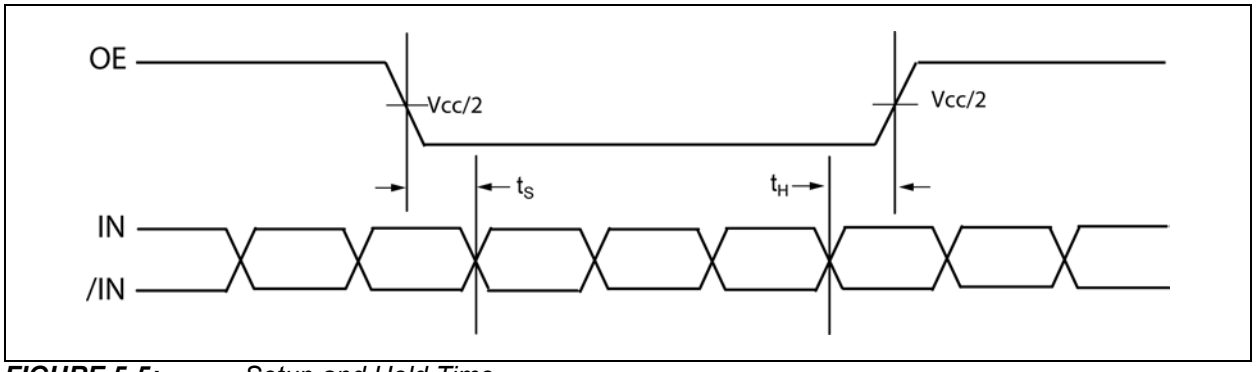


FIGURE 5-5: *Setup and Hold Time.*

Single-Ended and Differential Swings

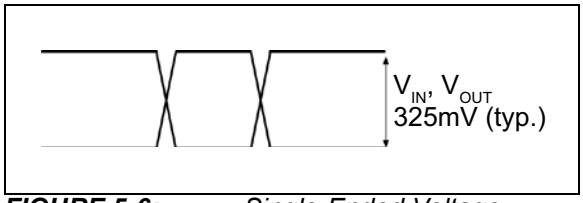


FIGURE 5-6: *Single-Ended Voltage Swing.*

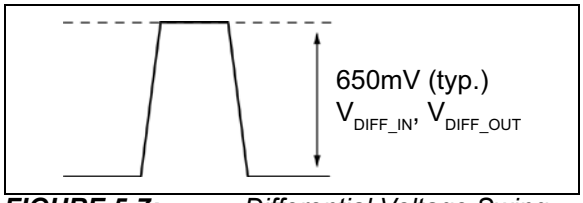


FIGURE 5-7: *Differential Voltage Swing.*

Input Stage

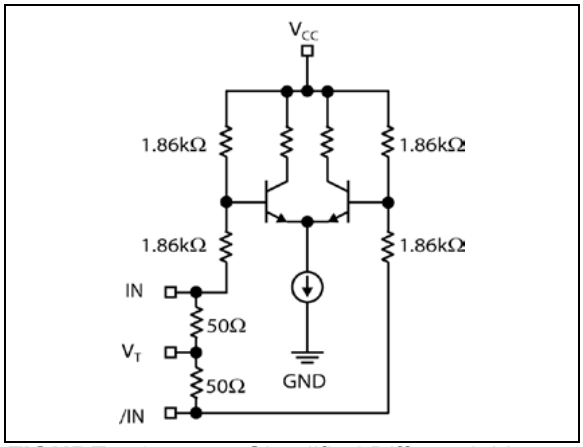


FIGURE 5-8: *Simplified Differential Input Stage.*

6.0 INPUT INTERFACE APPLICATIONS

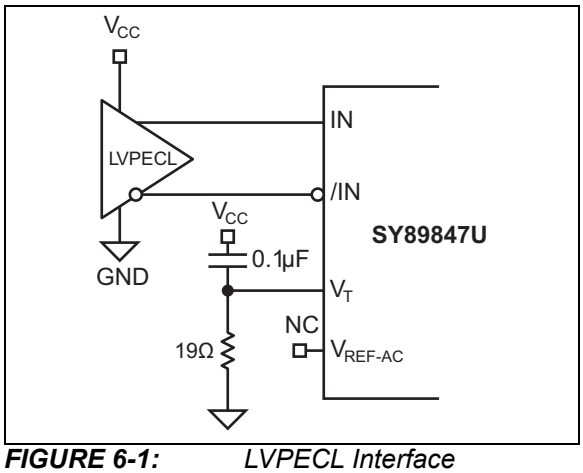


FIGURE 6-1: *LVPECL Interface (DC-Coupled).*

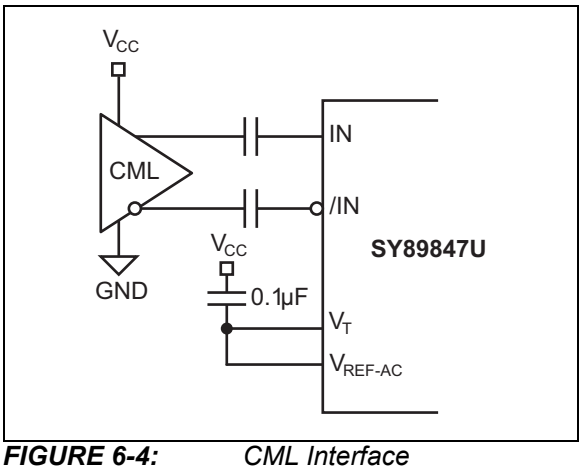


FIGURE 6-4: *CML Interface (AC-Coupled).*

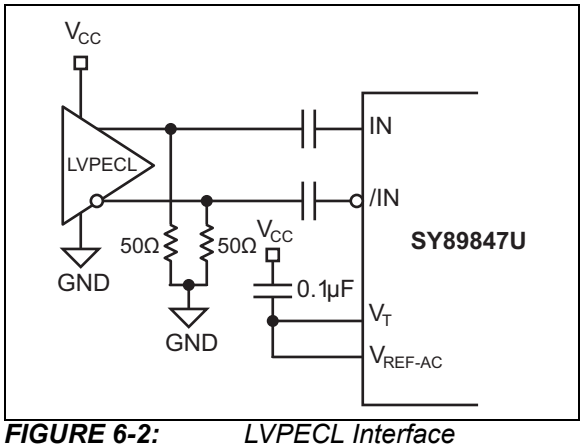


FIGURE 6-2: *LVPECL Interface (AC-Coupled).*

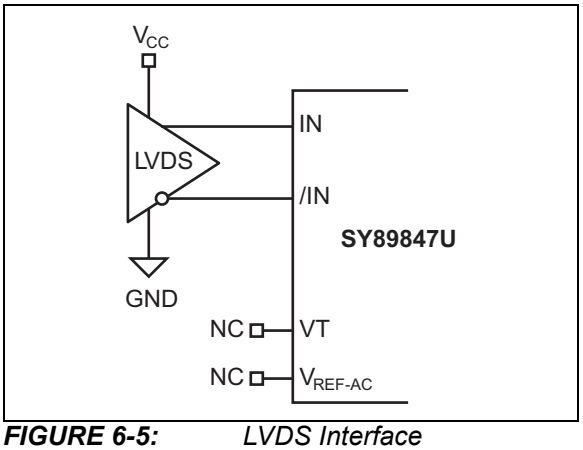


FIGURE 6-5: *LVDS Interface (DC-Coupled).*

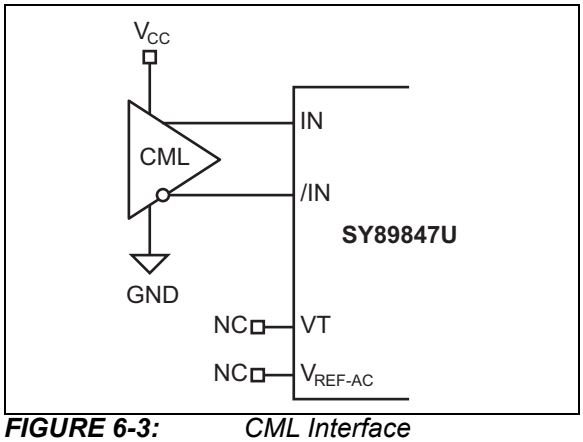


FIGURE 6-3: *CML Interface (DC-Coupled).*

7.0 LVDS OUTPUT INTERFACE APPLICATIONS

LVDS specifies a small swing of 325 mV, typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in the ground between and LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

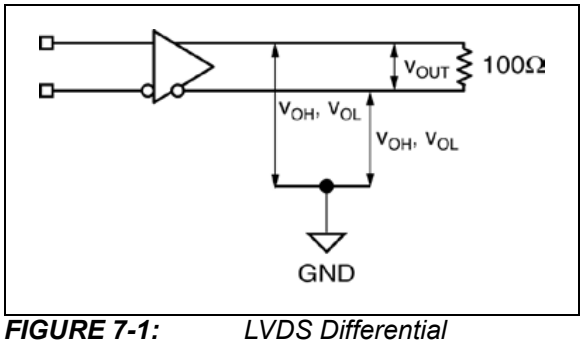


FIGURE 7-1: *LVDS Differential Measurement.*

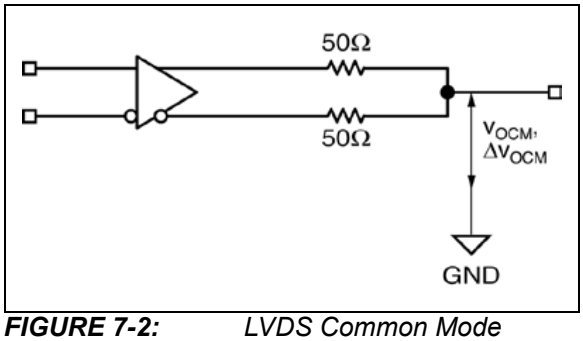
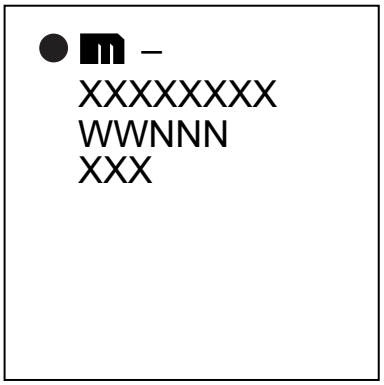


FIGURE 7-2: *LVDS Common Mode Measurement.*

8.0 PACKAGING INFORMATION

8.1 Package Marking Information

32-Pin QFN*



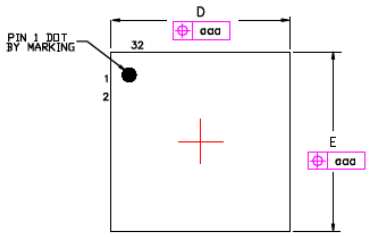
Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

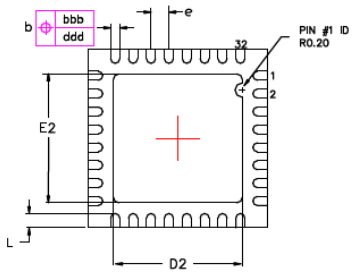
32-Lead 5 mm x 5 mm QFN Package Outline and Recommended Land Pattern

TITLE
32 LEAD QFN 5x5mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN55-32LD-PL-5	UNIT	MM
LEAD FRAME	NiPdAu	LEAD FINISH	NiPdAu

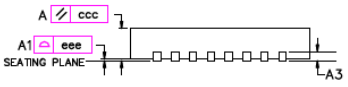


TOP VIEW



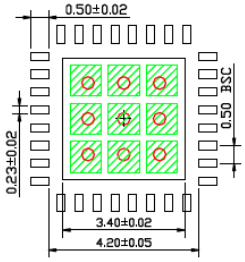
BOTTOM VIEW

	DIMENSION IN mm		
SYMBOL	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
A3		0.20 (REF)	
D		5.00 BSC	
D2	3.00	3.10	3.20
E		5.00 BSC	
E2	3.00	3.10	3.20
L	0.35	0.40	0.45



SIDE VIEW

	b (mm)			e (mm)		
N	MIN	NOM	MAX	MIN	NOM	MAX
32	0.18	0.25	0.30	0.50 BSC		



RECOMMENDED LAND PATTERN

TOLERANCE OF FORM AND POSITION	
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08

NOTE:
1. REFER TO JEDEC STANDARD MO-220 VHHD-2.
2. DIMENSION "b" APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm TO 0.30mm FROM THE TERMINAL TIP.
3. "aaa" THE BILATERAL PROFILE TOLERANCE THAT CONTROLS THE POSITION OF THE PLASTIC BODY SIDES. THE CENTERS OF THE PROFILE ZONES ARE DEFINED BY THE BASIC DIMENSIONS "D" AND "E".
4. "bbb" THE TOLERANCE THAT CONTROLS THE POSITION OF THE ENTIRE TERMINAL PATTERN WITH RESPECT TO DATUM'S A AND B. THE CENTER OF THE TOLERANCE ZONE OF EACH TERMINAL IS DEFINED BY THE BASIC DIMENSION "e" AS RELATED TO DATUM A AND B.
5. "ccc" THE TOLERANCE LOCATED PARALLEL TO THE SEATING PLANE IN WHICH THE TOP SURFACE OF THE PACKAGE MUST BE LOCATED.
6. "ddd" THE TOLERANCE THAT CONTROLS THE POSITION OF THE TERMINALS TO EACH OTHER. THE CENTERS OF THE PROFILE ZONES ARE DEFINED BY BASIC DIMENSION "e".
7. "eee" THE UNILATERAL TOLERANCE LOCATED ABOVE THE SEATING PLANE WHEREIN THE BOTTOM SURFACE OF THE TERMINALS MUST BE LOCATED.
8. THE TOLERANCE THAT CONTROLS THE POSITION OF THE EXPOSED METAL HEAT FEATURE. THE CENTER OF THE TOLERANCE ZONE WILL BE THE DATUM'S DEFINED BY THE CENTERLINES OF THE PACKAGE BODY.
9. MAX PACKAGE WARPAGE IS 0.05 MM.
10. PIN #1 IS ON TOP WILL BE LASER MARKED.
11. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
12. GREEN RECTANGLES (SHADED AREA) inolcate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.87x0.87 MM IN SIZE, 1.07 MM PITCH.
13. THIS DOCUMENT IS FOR AUTOMOTIVE PRODUCT USE ONLY.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document SY89847U to Microchip data sheet template DS20006101A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Input Voltage	Package	Temperature Range	Tape and Reel

Device:	SY89847:		1.5 GHz Precision, LVDS 1:5 Fanout Buffer with 2:1 MUX and Fail-Safe Input with Internal Termination
Input Voltage:	U	=	2.5V/3.3V
Package:	M	=	5 mm x 5 mm QFN-32
Temperature Range:	G	=	–40°C to 85°C (NiPdAu Lead-Free)
Special Processing:	<blank>	=	60/Tube
	TR	=	1,000/Reel

Examples:

a) SY89847UMG: SY89847, 2.5V/3.3V Input Voltage, 5 mm x 5 mm 32-Lead QFN, –40°C to +85°C Temperature Range, 60/Tube

b) SY89847UMG-TR: SY89847, 2.5V/3.3V Input Voltage, 5 mm x 5 mm 32-Lead QFN, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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