SY88343BL

3.3V, 3.2 Gbps CML Limiting Post Amplifier with High Gain TTL Loss-of-Signal

Features

- Single 3.3V Power Supply
- DC to 3.2 Gbps Operation
- Low-Noise CML Data Outputs
- High Gain LOS
- Chatter-Free Open-Collector TTL Loss-of-Signal (LOS) Output with Internal 4.75 kΩ Pull-Up Resistor
- TTL /EN Input
- Programmable LOS Level Set (LOS_{LVL})
- Ideal for Multi-Rate Applications
- Available in a 16-Lead VQFN Package

Applications

- APON, BPON, EPON, and GPON
- Gigabit Ethernet
- Fibre Channel
- OC-3 and OC-12/24 SONET/SDH
- High-Gain Line Driver and Line Receiver

Markets

- FTTP
- Optical Transceivers
- Datacom/Telecom
- Low-Gain TIA Interface
- Long-Reach FOM

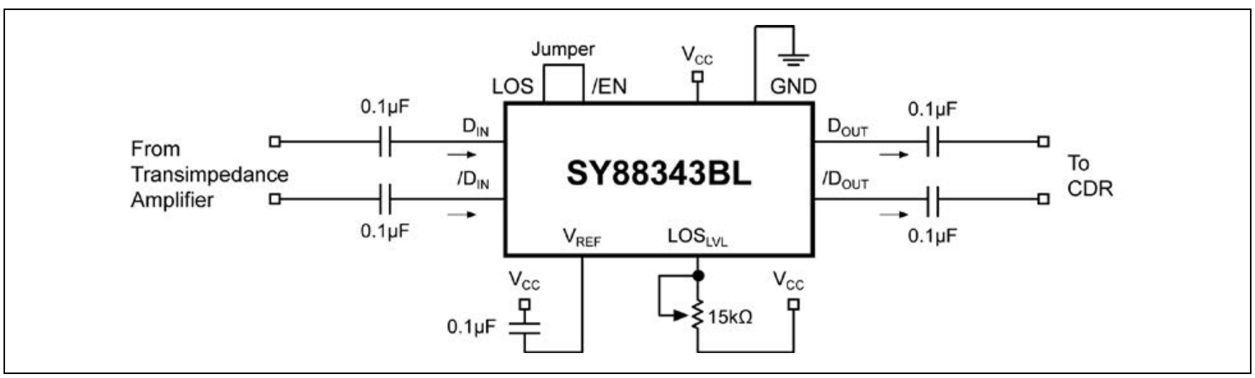
General Description

The SY88343BL low-power limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs) that are AC-coupled. The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88343BL quantizes these signals and outputs CML-level waveforms.

The SY88343BL operates from a single +3.3V power supply, over temperatures ranging from –40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 3.2 Gbps and as small as 5 mV_{PP} can be amplified to drive devices with CML inputs or AC-coupled CML/PECL inputs.

The SY88343BL generates a high-gain loss-of-signal (LOS) open-collector TTL output. The LOS function has a high gain input stage for increased sensitivity. A programmable loss-of-signal level set pin (LOS_{LVL}) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold set by LOS_{LVL} and de-asserts low otherwise. The enable bar input (/EN) de-asserts the true output signal without removing the input signal. The LOS output can be fed back to the /EN input to maintain output stability under a loss-of-signal condition. Typically, 3.5 dB LOS hysteresis is provided to prevent chattering.

Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) .... 0V to +7.0V
input Voltage (DIN, /DIN) .... 0V to V_{CC}
Output Current (I_{OUT})
Continuous .... ±50 mA
Surge .... ±100 mA
/EN Voltage .... 0V to V_{CC}
V_{REF} Current .... –800 µA to +500 µA
LOL_{LVL} Voltage .... V_{REF} to V_{CC}

Operating Ratings ‡

Supply Voltage (V_{CC}) .... +3.0V to +3.6V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.0V to 3.6V; R_L = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = 3.3V, T_A = +25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{CC}	—	45	62	mA	No output load
LOS_{LVL} Voltage	V_{LOSLVL}	V_{REF}	—	V_{CC}	V	—
CML Output HIGH Voltage	V_{OH}	V_{CC} – 0.020	V_{CC} – 0.005	V_{CC}	V	—
CML Output LOW Voltage	V_{OL}	V_{CC} – 0.475	V_{CC} – 0.4	V_{CC} – 0.350	V	—
Differential Output Offset	V_{OFFSET}	—	—	±80	mV	—
Reference Voltage	V_{REF}	V_{CC} – 1.48	V_{CC} – 1.32	V_{CC} – 1.16	V	—
Input Common Mode Range	V_{IHCMR}	GND + 2.0	—	V_{CC}	V	—
Single-Ended Output Impedance	Z_O	40	50	60	Ω	—
Single-Ended Input Impedance	Z_I	40	50	60	Ω	—

TTL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.0V to 3.6V; T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
/EN Input HIGH Voltage	V_{IH}	2.0	—	—	V	—
/EN Input LOW Voltage	V_{IL}	—	—	0.8	V	—
/EN Input HIGH Current	I_{IH}	—	—	20	µA	V_{IN} = 2.7V
		—	—	100	µA	V_{IN} = V_{CC}
/EN Input LOW Current	I_{IL}	–0.3	—	—	mA	V_{IN} = 0.5V
LOS Output HIGH Level	V_{OH}	2.4	—	—	V	V_{CC} ≥ 3.3V, I_{OH-MAX} < 160 µA
		2.0	—	—	V	V_{CC} < 3.3V, I_{OH-MAX} < 160 µA
LOS Output LOW Level	V_{OL}	—	—	0.5	V	I_{OL} = +2 mA

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.0V to 3.6V; T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Rise/Fall Time (20% to 80%)	t_r/t_f	—	60	120	ps	Note 1
Deterministic Jitter	t_{JITTER}	—	15	—	ps_{PP}	Note 2
Random Jitter		—	5	—	ps_{RMS}	Note 3
Differential Input Voltage Swing	V_{ID}	5	—	1800	mV_{PP}	Figure 4-2
Differential Output Voltage Swing	V_{OD}	700	800	950	mV_{PP}	$V_{ID} \geq 12\ mV_{PP}$, Figure 4-2
LOS Release Time	t_{OFF}	—	2	10	µs	—
LOS Assert Time	t_{ON}	—	2	10	µs	—
Low LOS De-assert Level	LOS_{DL}	—	4.8	—	mV_{PP}	R_{LOSLVL} = 15 kΩ, Note 5
Low LOS Assert Level	LOS_{AL}	—	3.1	—	mV_{PP}	R_{LOSLVL} = 15 kΩ, Note 5
Low LOS Hysteresis	HYS_L	—	3.8	—	dB	R_{LOSLVL} = 15 kΩ, Note 4
Medium LOS De-assert Level	LOS_{DM}	—	7.5	11	mV_{PP}	R_{LOSLVL} = 5 kΩ, Note 5
Medium LOS Assert Level	LOS_{AM}	3	5.2	—	mV_{PP}	R_{LOSLVL} = 5 kΩ, Note 5
LOS Hysteresis	HYS_M	2	3.2	4.5	dB	R_{LOSLVL} = 5 kΩ, Note 4
High LOS De-assert Level	LOS_{DH}	—	18	23	mV_{PP}	R_{LOSLVL} = 100Ω, Note 5
High LOS Assert Level	LOS_{AH}	8	12	—	mV_{PP}	R_{LOSLVL} = 100Ω, Note 5
High LOS Hysteresis	HYS_H	2	3.5	4.5	dB	R_{LOSLVL} = 100Ω, Note 4
3 dB Bandwidth	B_{-3dB}	—	2	—	GHz	—
Differential Voltage Gain	$A_{V(DIFF)}$	32	38	—	dB	—
Single-Ended Small-Signal Gain	S_{21}	26	32	—	dB	—

Note 1: Amplifier in limiting mode. Input is a 200 MHz square wave.

2: Deterministic jitter measured using 3.2 Gbps K28.5 pattern, V_{ID} = 10 mV_{PP}.

3: Random jitter measured using 3.2 Gbps K28.7 pattern, V_{ID} = 10 mV_{PP}.

4: This specification defines electrical hysteresis as 20log (LOS De-assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2, depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2 dB to 4.5 dB, shown in the AC characteristics table, will be 1 dB to 3 dB Optical Hysteresis.

5: See Figure 2-1 for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
Thermal Resistance, VQFN 16-Ld, Note 2	θ_{JA}	—	61	—	°C/W	—
	Ψ_{JB}	—	38	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact the device reliability.

2: Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

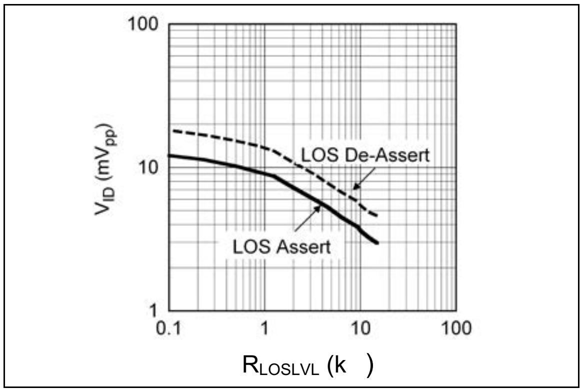


FIGURE 2-1: *V_{ID} to Assert/De-Assert LOS vs. R_{LOSLVL}.*

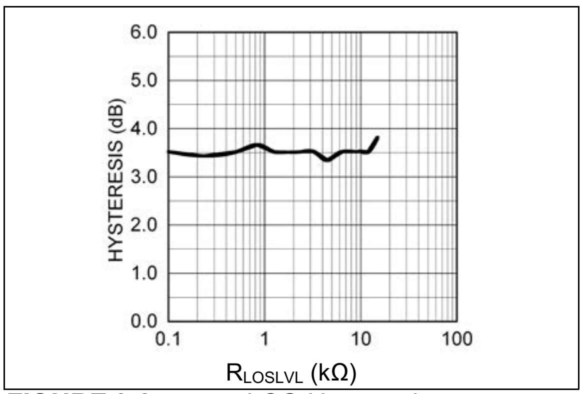
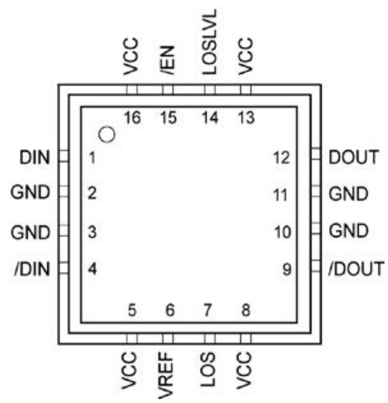


FIGURE 2-2: *LOS Hysteresis vs. R_{LOSLVL}.*

3.0 PIN DESCRIPTIONS

Package Type



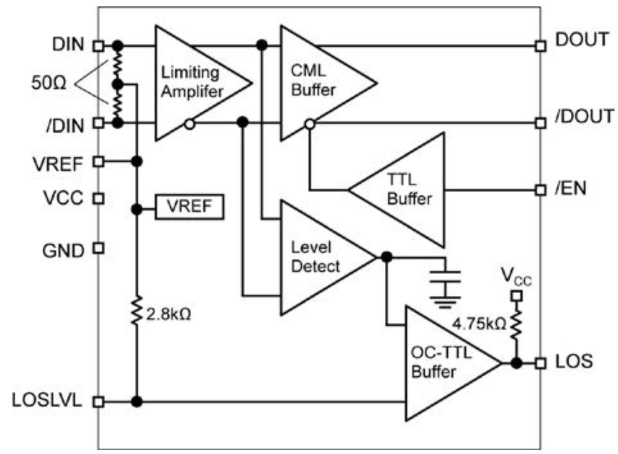
The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Type	Description
15	/EN	TTL Input: Default is high	/Enable: This input enables the outputs when it is LOW. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic HIGH state if left open.
1	DIN	Data Input	True data input.
4	/DIN	Data Input	Complementary data input.
6	VREF	—	Reference Voltage: Bypass with 0.01 µF low ESR capacitor from VREF to VCC to stabilize LOS_{LVL} and V_{REF}.
14	LOSLVL	Input	Loss-of-Signal Level Set: A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which the LOS output will be asserted.
2, 3, 10, 11	GND, Exposed Pad	Ground	Device ground. Exposed pad must be connected to PCB ground plane.
7	LOS	Open Collector TTL Output with internal 4.75 kΩ pull-down resistor	Loss-of-Signal: Asserts high when the data input amplitude falls below the threshold set by LOS_{LVL}.
9	/DOUT	CML Output	Complementary data output.
12	DOUT	CML Output	True data output.
5, 8, 13, 16	VCC	Power Supply	Positive power supply.

4.0 FUNCTIONAL DESCRIPTION

Functional Block Diagram



The SY88343BL low-power limiting post amplifier operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 3.2 Gbps and as small as 5 mV_{PP} can be amplified. Figure 4-1 shows the allowed input voltage swing. The SY88343BL generates a LOS output allowing feedback to /EN for output stability. LOS_{LVL} sets the sensitivity of the input amplitude detection.

4.1 Input Amplifier Buffer

Figure 4-2 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as 5 mV_{PP} to be detected and amplified. The input amplifier also allows input signals as large as 1800 mV_{PP}. Input signals are linearly amplified with a typical 38 dB differential voltage gain. Because it is a limiting amplifier, this device outputs typically 800 mV_{PP} voltage-limited waveforms for input signals greater than 12 mV_{PP}. Applications that require the SY88343BL to operate with high gain should have the upstream TIA placed as close as possible to the device's input pins. This ensures the best performance of the device.

4.2 Output Buffer

The SY88343BL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} for each output pin provides this. Figure 4-4 shows a simplified schematic of the output stage.

4.3 Loss-of-Signal

The SY88343BL generates a chatter-free LOS open-collector TTL output with an internal 4.75 kΩ pull-up resistor, as shown in Figure 4-3. LOS is used to determine that the input amplitude is large enough to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold sets by LOS_{LVL} and de-asserts low otherwise. LOS can be fed back to the enable bar (/EN) input to maintain output stability under a loss-of-signal condition. /EN de-asserts the true output signal without removing the input signals. Typical, 3.5 dB LOS hysteresis is provided to prevent chattering.

4.4 Loss-of-Signal Level Set

Programmable LOS level-set pin (LOS_{LVL}) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOS_{LVL} sets the voltage at LOS_{LVL}. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and V_{REF}, as shown in Figure 4-5.

4.5 Hysteresis

The SY88343BL provides typically 3.5 dB LOS electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V_{IN}^2/R for an electrical signal. Hence, the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and therefore, the ratios change linearly. Thus, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. Because the SY88343BL is an electrical device, this data sheet refers to hysteresis in electrical terms. With 3.5 dB LOS hysteresis, a voltage factor of 1.5 is required to assert or de-assert LOS.

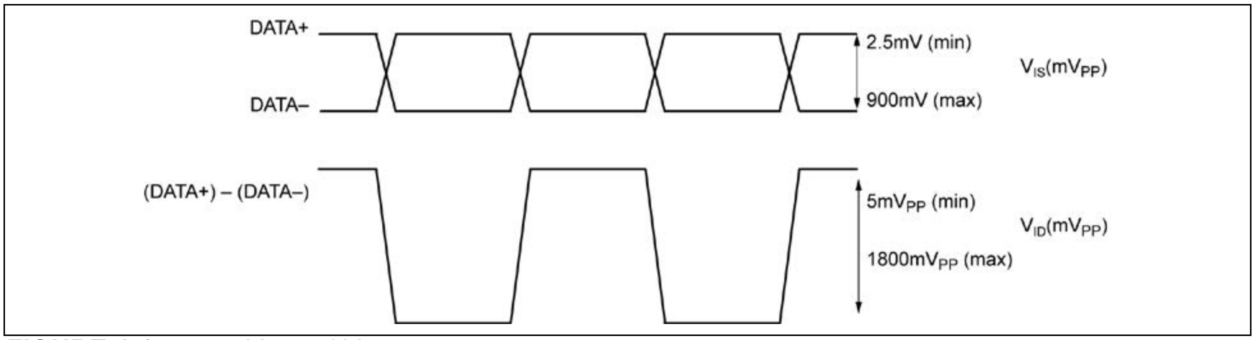


FIGURE 4-1: *V_{IS} and V_{ID}.*

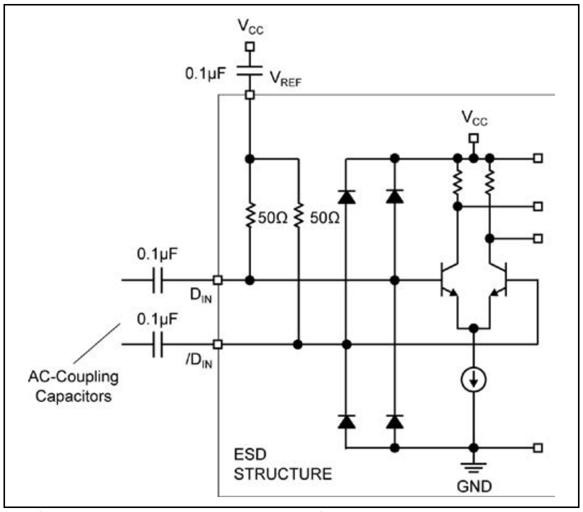


FIGURE 4-2: *Input Structure.*

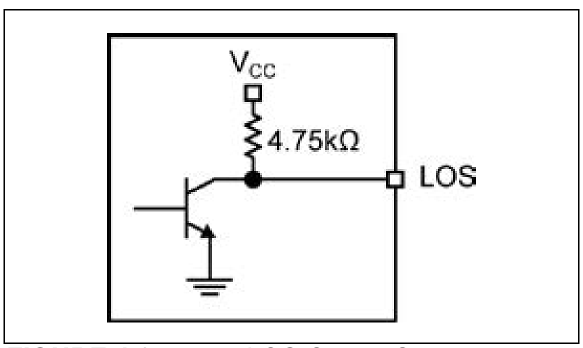


FIGURE 4-3: *LOS Output Structure.*

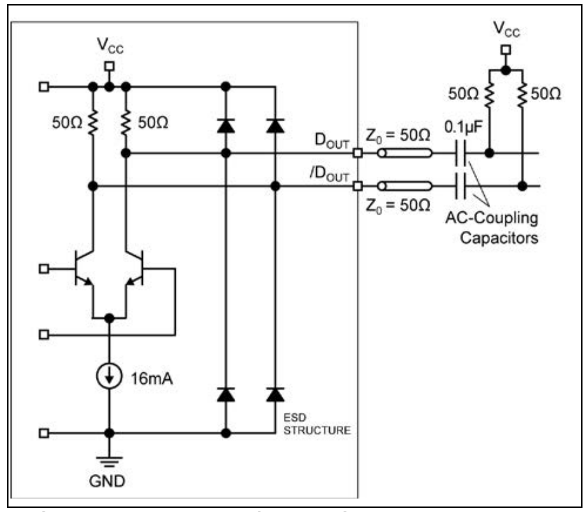


FIGURE 4-4: *Output Structure.*

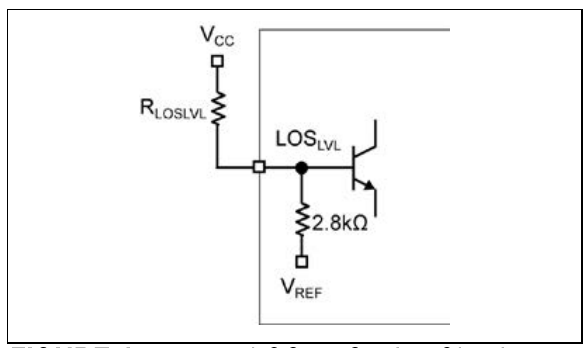
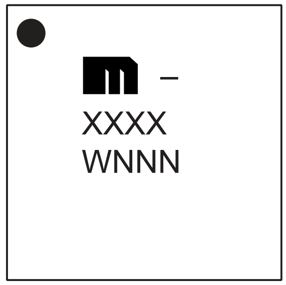


FIGURE 4-5: *LOS_{LVL} Setting Circuit.*

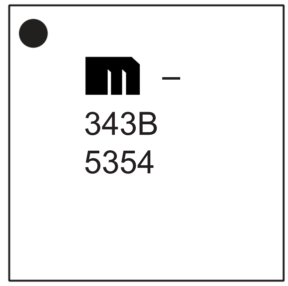
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

16-Lead VQFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

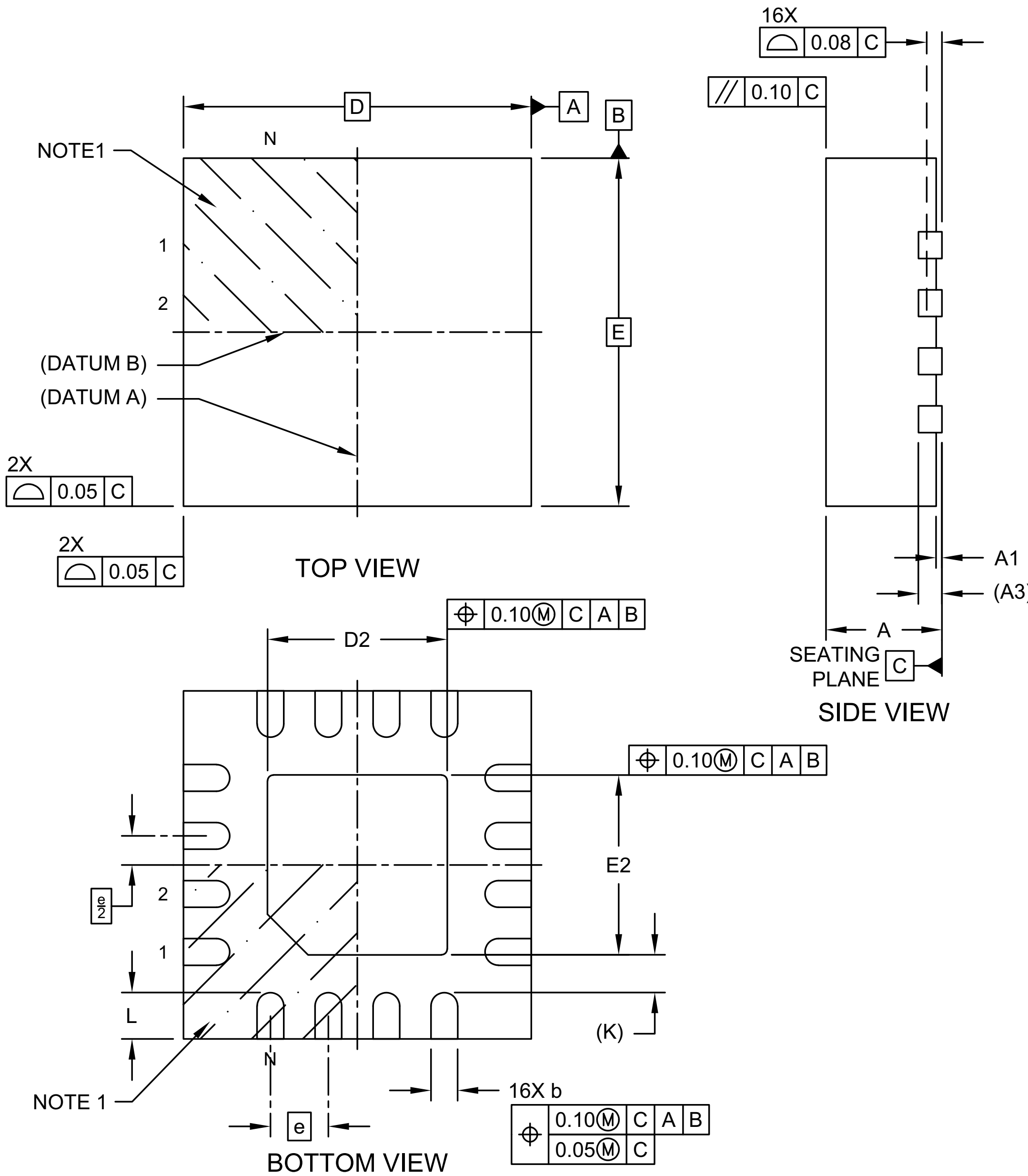
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

16-Lead VQFN Package Outline and Recommended Land Pattern

16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev B Sheet 1 of 2

16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad

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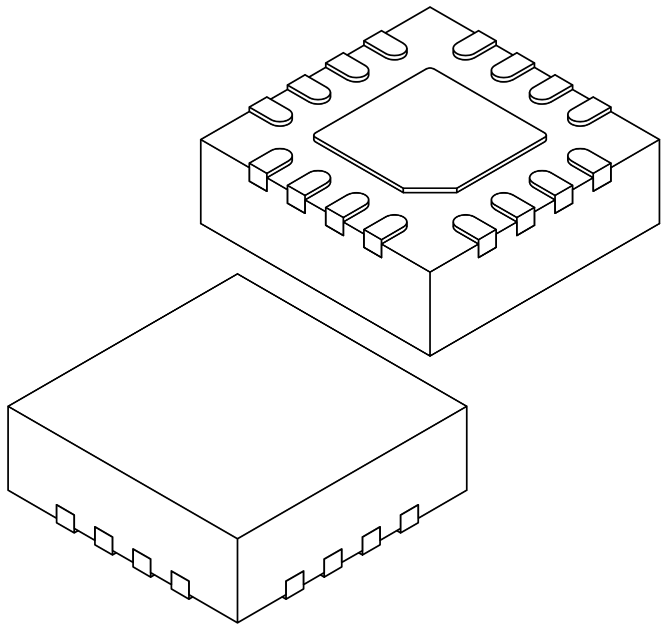


	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

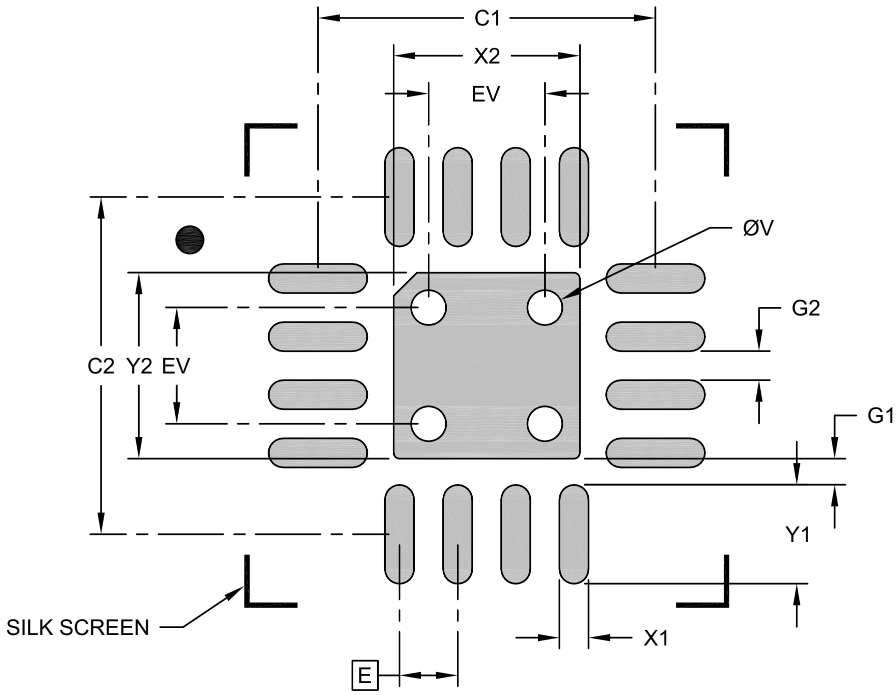
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev B Sheet 2 of 2

16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.90	
Contact Pad Spacing	C2		2.90	
Contact Pad Width (Xnn)	X1			0.25
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.23		
Contact Pad to Contact Pad (Xnn)	G2	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3103-NCA Rev B

APPENDIX A: REVISION HISTORY

Revision A (November 2021)

- Converted Micrel document SY88343BL to Microchip data sheet DS20006622A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	X	X	X	-XX
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY88343B:	3.2 Gbps CML Limiting Post Amplifier with High Gain TTL Loss-of-Signal
Supply Voltage:	L =	3.3V
Package:	M =	16-Lead 3 mm x 3 mm VQFN
Temperature Range:	G =	–40°C to +85°C
Media Type:	(blank)= TR =	100/Tube 1,000/Reel

Examples:

a) SY88343BLMG: SY88343B, 3.3V Supply Voltage, 16-Lead 3x3 VQFN, –40°C to +85°C Temp. Range, 100/Tube

b) SY88343BLMG-TR: SY88343B, 3.3V Supply Voltage, 16-Lead 3x3 VQFN, –40°C to +85°C Temp. Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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