SY75608/612

8 or 12 Output Ultra-Low Additive Jitter PCIe 1/2/3/4/5/6 Clock Buffer

Features

- Eight (SY75608) and Twelve (SY75612) PCIe 1.0, 2.0, 3.0, 4.0, 5.0, and 6.0 Compliant Outputs
- Ultra-Low Additive Jitter: 10 fs (PCIe Gen5)
- Supports Frequencies of Up to 250 MHz
- Transparent for Spread Spectrum
- Supports 1.8V ±10%, 2.5V ±10%, and 3.3V ±10% Power Supplies
- Outputs Low Power HCSL with Embedded Termination Resistors
- Selectable Pin or I^2C Bus Control
- Individual Glitch Free Output Enable (OExb) Control Pins
- Accepts DC-Coupled HCSL Input Signal and AC-Coupled PECL, LVDS, and CML Input Signals
- Extended Temperature Range: –40°C to +105°C
- 6 mm x 6 mm VQFN (SY75608) and 8 mm x 8 mm VQFN (SY75612) package

Applications

- Cloud and High-Performance Computing
- PCIe-Based SSD Drives
- PCIe Switches
- Servers

General Description

The SY75608 and SY75612 are industry-leading PCIe clock buffers with ultra-low additive jitter:

- 6 fs (PCIe 6.0)
- 10 fs (PCIe 5.0)
- 20 fs (PCIe 3.0/4.0)
- 52 fs in the 12 kHz to 20 MHz band

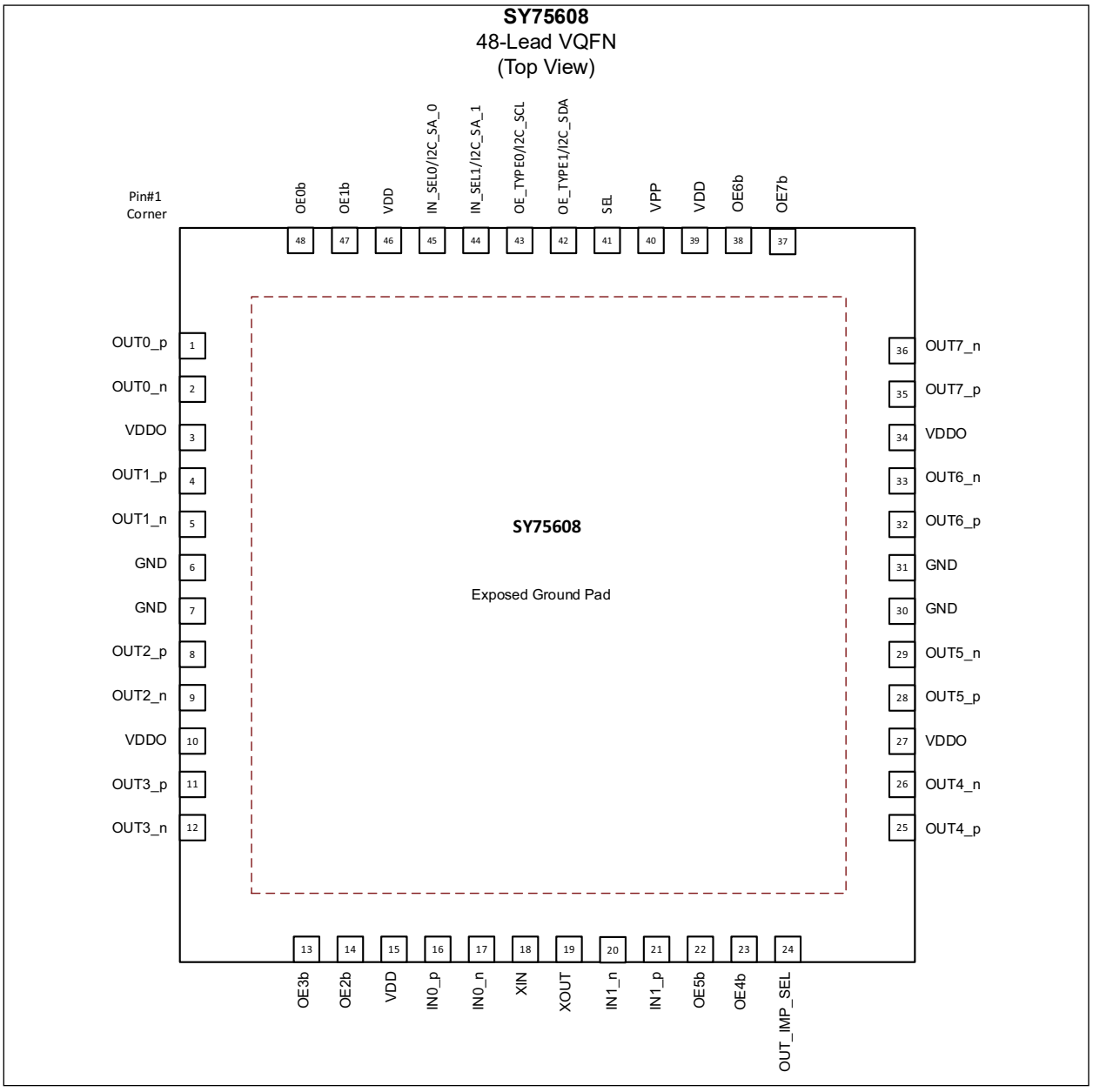
They can be used in all PCIe 1/2/3/4/5/6 common clock and SRIS applications.

SY75608 and SY75612 are, respectively, eight and twelve output PCIe clock buffers with glitch free per-output enable/disable control hardware pins. Devices are packaged in 6 mm x 6 mm VQFN (SY75608) and 8 mm x 8 mm VQFN (SY75612).

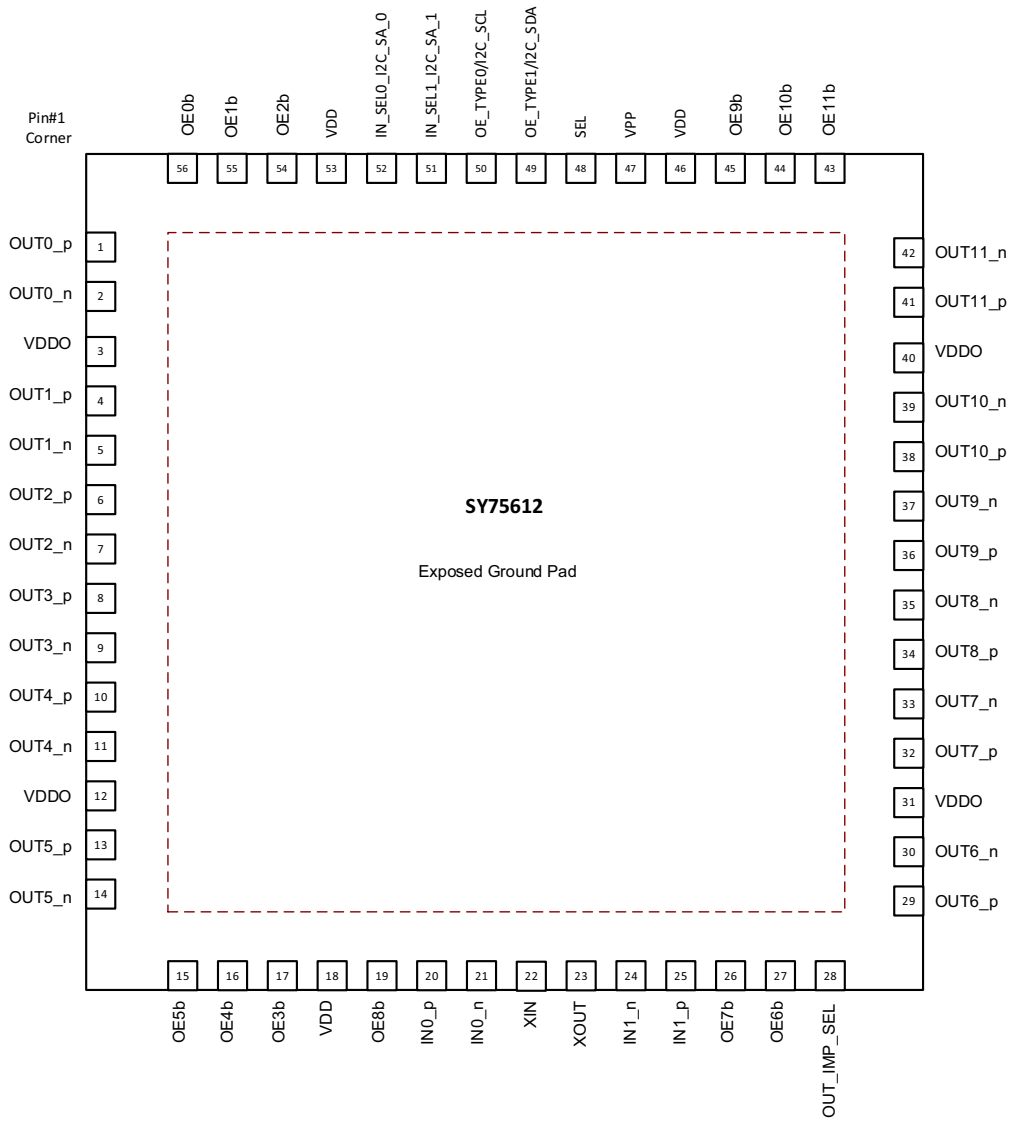
The SY75608/612 each have an embedded low-dropout regulator (LDO) for superior power noise supply rejection. They support 1.8V, 2.5V, and 3.3V supplies with a tolerance of ±10%, which exceeds the ±9% required by the PCIe Card Electro Mechanical Specification.

Both parts are available in the extended temperature range of –40°C to +105°C. Both parts are also available with customized configurations to meet the customer's needs. Please visit the ClockWorks Configurator to design your particular specifications.

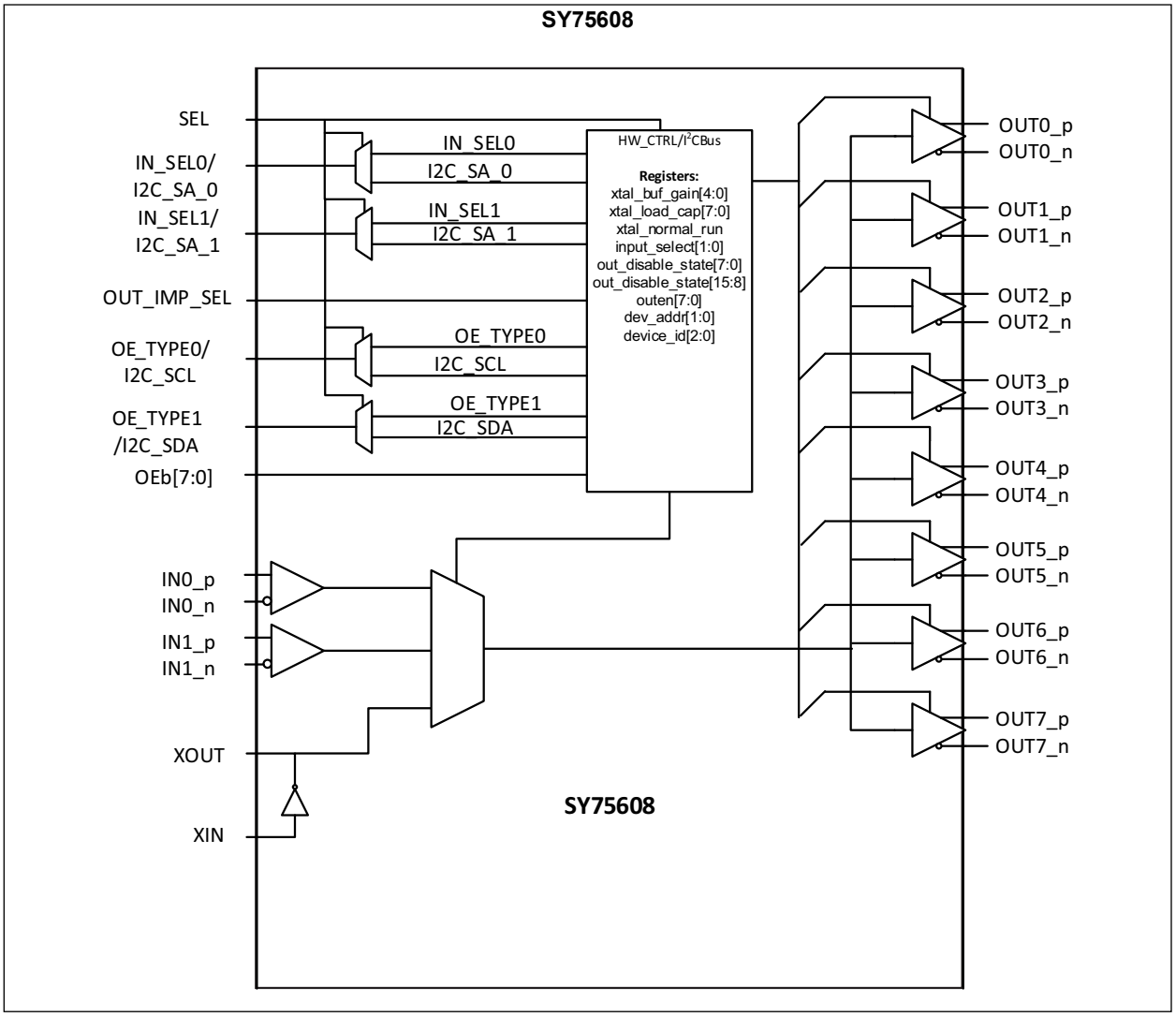
Package Types

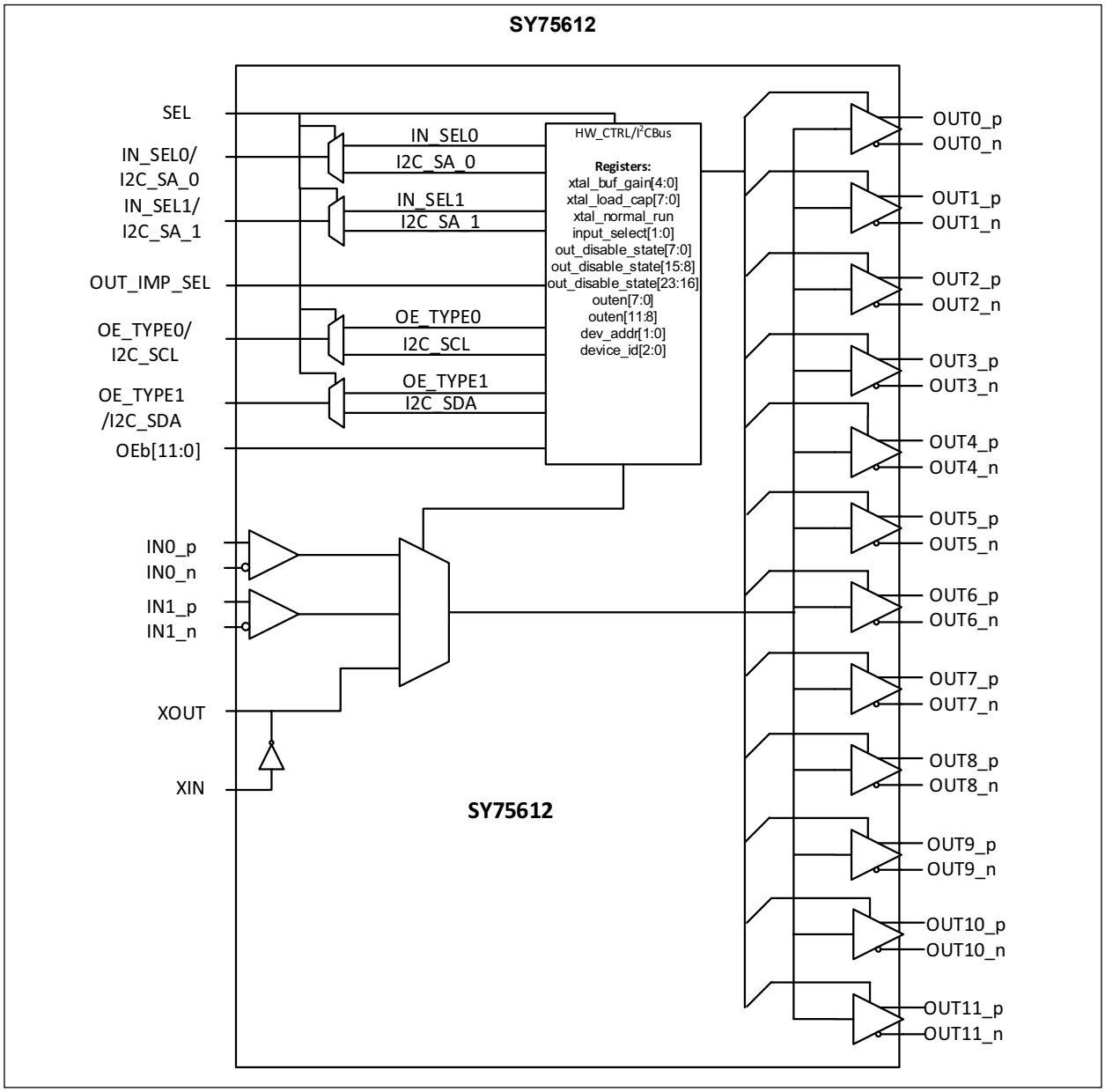


SY75612
56-Lead VQFN
(Top View)



Block Diagrams





1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}) ..... –0.5V to +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{DD} + 0.5V
Input ESD Protection (HBM) ..... 2 kV

Operating Ratings ‡

1.8V Operating Voltage (V_{DD}) ..... +1.62V to +1.98V
2.5V Operating Voltage (V_{DD}) ..... +2.25V to +2.75V
3.3V Operating Voltage (V_{DD}) ..... +2.97V to +3.63V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions may affect device reliability.

‡ Notice: The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V ±10%, T_A = –40°C to +105°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Current Consumption						
Core Device Current	I_{DD}	—	13	15	mA	All outputs and XTAL disabled. Both reference inputs fed with 100 MHz differential clock.
Core Device Current	I_{DD_XTAL}	—	13	15	mA	All outputs disabled; XTAL circuit enabled with 25 MHz Crystal connected between XIN and XOUT
Current Dissipation per LPHCSL Output (100Ω)	$I_{DD\_HCSL\_100\Omega}$	—	3.5	3.9	mA	Note 1
Current Dissipation per LPHCSL Output (85Ω)	$I_{DD\_HCSL\_85\Omega}$	—	4.0	4.4	mA	Note 1
Power Supply Noise Rejection Ratio						
Power Supply Noise Rejection Ratio	$PSNRR_{HCSL}$	—	70	—	dB	100 mV_{PP}, 100 kHz noise injected to V_{DD}. Clock Frequency 100 MHz, V_{DD} = 3.3V
Input						
Input Slew Rate	SR_{IN}	0.6	—	—	V/ns	—
Differential Input High Voltage	V_{IH}	0.15	—	—	V	—
Differential Input Low Voltage	V_{IL}	—	—	–0.15	V	—
Input Voltage Swing	V_{ASWING}	0.15	—	—	V	—
Absolute Crossing Point Voltage	V_{CROSS}	0.25	—	0.55	V	—
Variation of V_{CROSS} Over All Edges	$V_{CROSSDELTA}$	—	—	0.14	V	—
Voltage High for Control Inputs	V_{IH_OE}	$0.7*V_{DD}$	—	—	V	—
Voltage Low for Control Inputs	V_{IL_OE}	—	—	$0.3*V_{DD}$	V	—

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V ±10%, T_A = –40°C to +105°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Leakage Current	I_{IL_IN}	–5	—	5	µA	$V_{IN} = V_{DD}$, V_{IN} = GND
Input Capacitance	C_{IN}	—	—	5	pF	—
Input Leakage Current for OE Inputs	I_{IL_OE}	–5	—	70	µA	$V_{IN} = V_{INMAX}$, V_{IN} = GND; includes current due to pull down resistors
Single-Ended Input Common Mode Voltage (IN_p)	V_{SIC}	0.25	—	0.55	V	HCSL common mode
Single-Ended Input Voltage Swing for IN_p	V_{SID}	0.3	—	1.45		—
Maximum Input Voltage	$V_{IN(MAX)}$	—	—	1.15	V	—
Minimum Input Voltage	$V_{IN(MIN)}$	–0.3	—	—	V	—
Differential Input Frequency	f_{IN}	0	—	250	MHz	Note 2
Single-Ended Input Frequency	f_{IN_SE}	0	—	250	MHz	Note 2
Input Duty Cycle	DC	35	—	65	%	—
Input Multiplexer Isolation IN0_p/n to IN1_p/n and Vice Versa	I_{SO}	—	–84	—	dBc	f_{IN} = 100 MHz, Note 2, Power on both inputs 0 dBm, f_{OFFSET} >50 kHz
		—	–82	—		f_{IN} = 250 MHz, Note 2, Power on both inputs 0 dBm, f_{OFFSET} >50 kHz

Note 1: Tested with 100 MHz clock with outputs driving 4” long trace terminated with 2 pF Capacitors to ground.

2: Output Enable control (pin or register) is synchronous with the input clock and it takes four rising edges before output gets enabled or disabled. Hence the minimum input frequency is greater than 0 Hz. Once the outputs are enabled the input clock frequency can be reduced to 0 Hz.

CRYSTAL OSCILLATOR CHARACTERISTICS

Electrical Characteristics: V_{DD}/V_{DDO} = 3.3V ±10%, V_{DD}/V_{DDO} = 2.5V ±10%, V_{DD}/V_{DDO} = 1.8V ±10%, T_A = –40°C to +105°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Mode of Oscillation	—	—	—	—	—	Fundamental
Frequency	f	8	—	160	MHz	High frequency crystal needs lower motion resistance. For example, the motion resistance for 156.25 MHz needs to be lower than 25Ω
On-Chip Load Capacitance in I^2C Bus Controlled Mode	C_L	0	—	21.75	pF	The values are programmable. On the top of this, there are intrinsic pin capacitances and the capacitance of PCB trace connecting to the crystal.
On-Chip Load Capacitance in Pin Controlled Mode	—	—	4	—	pF	Fixed
On-Chip Series Resistor in Pin Controlled Mode	—	—	150	—	Ω	Fixed
On-Chip Shunt Resistor	R	—	500	—	kΩ	—

CRYSTAL OSCILLATOR CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD}/V_{DDO} = 3.3V ±10%, V_{DD}/V_{DDO} = 2.5V ±10%, V_{DD}/V_{DDO} = 1.8V ±10%, T_A = –40°C to +105°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency in Overdrive Mode (Note 1)	f_{OV}	8	—	160	MHz	Functional, but may not meet AC parameters. Minimum depends on AC coupling Capacitor (0.1 µF assumed)
Frequency in Bypass Mode (Note 2)	f_{BP}	0	—	250	MHz	Functional, but may not meet AC parameters

Note 1: Maximum input level is 2V.

2: Maximum output level is V_{DD}.

OUTPUT ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V ±10%, T_A = –40°C to +105°C, unless noted. C_{LOAD} = 2 pF.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Rising Edge Rate	—	1	2.5	4	V/ns	Note 1, Note 2
Falling Edge Rate	—	1	2.5	4	V/ns	Note 1, Note 2
Differential Output High Voltage	V_{OH}	0.6	—	0.9	V	Note 1
Differential Output Low Voltage	V_{OL}	–0.9	—	–0.6	V	Note 1
Absolute Crossing Voltage	V_{CROSS}	0.25	—	0.55	V	Note 3, Note 4, Note 5
Variation of V_{CROSS} Over All Rising Clock Edges	V_{CROSS_DELTA}	—	—	0.14	V	Note 3, Note 4, Note 6
Ring Back Voltage Margin	V_{RB}	–0.1	—	0.1	V	Note 1, Note 7
Time before V_{RB} is Allowed	t_{STABLE}	500	—	—	ps	Note 1, Note 7
Cycle-to-Cycle Additive Jitter	$t_{OCJITTER}$	—	6.5	8.1	ps_{PP}	Note 1
Absolute Maximum Output Voltage	V_{MAX}	—	—	1.15	V	Note 3, Note 8
Absolute Minimum Output Voltage	V_{MIN}	–0.3	—	—	V	Note 3, Note 9
Output Duty Cycle	ODC	48	50	52	%	When input has 50% duty cycle and V_{IN} ≥ 200 mV, Note 1
Rising-to-Falling Edge Matching	—	—	—	15	%	Note 3, Note 10
Clock Source DC Impedance (OUTx_p)	$Z_{C\text{-}DC\_OUT\_p}$	—	50/42.5	—	Ω	OUT_IMP_SEL = low/high, Note 3, Note 11
Clock Source DC Impedance (OUTx_n)	$Z_{C\text{-}DC\_OUT\_n}$	—	50/42.5	—	Ω	OUT_IMP_SEL = low/high, Note 3, Note 11
Output Frequency	f_{MAX}	0	—	250	MHz	—
Output-to-Output Skew	t_{OOSK}	—	14	30	ps	—

OUTPUT ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 3.3V ±10%, V_{DD} = 2.5V ±10%, V_{DD} = 1.8V ±10%, T_A = –40°C to +105°C, unless noted. C_{LOAD} = 2 pF.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Device-to-Device Output Skew	t_{DOOSK}	—	—	0.6	ps	—
Input-to-Output Delay	t_{IOD}	1	1.4	2	ns	—
Output Enable Time	t_{EN}	—	—	5	cycles	Note 12
Output Disable Time	t_{DIS}	—	—	6	cycles	Note 12

Note 1: Measurement taken from differential waveform.

2: Measured from –150 mV to +150 mV on the differential waveform (derived from OUTx_p to OUTx_n). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 1-5.

3: Measurement taken from single ended waveform.

4: Measured at crossing point where the instantaneous voltage value of the rising edge of OUTx_p equals the falling edge of OUTx_n. See Figure 1-1.

5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 1-1.

6: Defined as the total variation of all crossing voltages of Rising OUTx_p and Falling OUTx_n. This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 1-2.

7: t_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See Figure 1-6.

8: Defined as the maximum instantaneous voltage including overshoot. See Figure 1-1.

9: Defined as the minimum instantaneous voltage including undershoot. See Figure 1-1.

10: Matching applies to rising edge rate for OUTx_p and falling edge rate for OUTx_n. It is measured using a ±75 mV window centered on the median cross point where OUTx_p rising meets OUTx_n falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of OUTx_p should be compared to the Fall Edge Rate of OUTx_n; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 1-3.

11: System board compliance measurements must use the test load card described in Figure 1-7. OUTx_p and OUTx_n are to be measured at the load capacitors C_{LOAD}. Single-ended probes must be used for measurements requiring single-ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements. Test load C_{LOAD} = 2 pF.

12: Output Enable control (pin or register) is synchronous with the input clock and it takes four rising edges before output gets enabled or disabled. Hence the minimum input frequency is greater than 0 Hz. Once the outputs are enabled the input clock frequency can be reduced to 0 Hz.

JITTER AND PHASE NOISE

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Peak-to-Peak Additive Jitter	A_{JRMS_PP}	—	4	5.1	ps	Note 1, Note 2
Additive Jitter per PCIe 1.0 (1.5 MHz to 22 MHz)	$t_{jPCIe\_1.0}$	—	0.7	0.9	ps_{RMS}	Note 1, Note 2
Additive Jitter per PCIe 2.0 High Band (1.5 MHz to 50 MHz)	$t_{jPCIe\_2.0\_high}$	—	79	100	fs_{RMS}	Note 1, Note 2
Additive Jitter per PCIe 2.0 Low Band (10 kHz to 1.5 MHz)	$t_{jPCIe\_2.0\_low}$	—	16	21	fs_{RMS}	Note 1, Note 2
Additive Jitter per PCIe 2.0 Mid Band (5 MHz to 16 MHz)	$t_{jPCIe\_2.0\_mid}$	—	62	79	fs_{RMS}	Note 1, Note 2

JITTER AND PHASE NOISE (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Additive Jitter per PCIe 3.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_3.0}$	—	20	25	fs_{RMS}	Note 1, Note 2
Additive Jitter per PCIe 4.0 (PLL_BW = 2 MHz to 5 MHz, CDR = 10 MHz)	$t_{jPCIe\_4.0}$	—	20	25	fs_{RMS}	Note 1, Note 2
Additive Jitter per PCIe 5.0 (PLL_BW = 0.5 MHz to 1.8 MHz, CDR for 32 GT/s CC)	$t_{jPCIe\_5.0}$	—	8.2	10	fs_{RMS}	Note 2, Note 3
Additive Jitter per PCIe 6.0 (PLL_BW = 0.5 MHz to 1.0 MHz, CDR for 64 GT/s CC)	$t_{jPCIe\_6.0}$	—	5.2	6.2	fs_{RMS}	Note 2, Note 3
Additive jitter per Intel QPI 9.6 Gbps	t_{jQPI}	—	35	45	fs_{RMS}	Note 1, Note 2
Additive RMS Jitter in 1 MHz to 20 MHz Band	$t_{j\_1M\_20M}$	—	53	67	fs_{RMS}	Note 1, Note 2, 100 MHz Clock
		—	41	56	fs_{RMS}	Note 1, Note 2, 133 MHz Clock
Additive RMS Jitter in 12 kHz to 20 MHz Band	$t_{j\_12k\_20M}$	—	51	64	fs_{RMS}	Note 1, Note 2, 100 MHz Clock
		—	39	54	fs_{RMS}	Note 1, Note 2, 133 MHz Clock
Noise Floor	N_F	—	–165	–163	dBc/Hz	Note 1, Note 2, 100 MHz Clock
		—	–165	–162	dBc/Hz	Note 1, Note 2, 133 MHz Clock

Note 1: Measured into AC test load as per Figure 1-7.

2: Measured from differential crossing point to differential crossing point.

3: Measured with 50Ω termination in instrument without a test load.

I^2C BUS ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Nominal Bus Voltage	V_{DD_I2C}	1.62	—	5.5	V	Note 1
Input Low Voltage	V_{IL}	—	—	0.6	V	—
Input High Voltage	V_{IH}	1.5	—	V_{DD_I2C}	V	—
Output Low Voltage	V_{OL}	—	—	0.4	V	At $I_{PULLUP,MAX}$
Input Leakage Current	I_{LEAK}	—	—	±10	µA	—
Current Sinking at $V_{OL,MAX}$	I_{PULLUP}	4	—	—	mA	—
Pin Capacitive Load	C_L	—	—	1	pF	—
Signal Noise Immunity from 10 MHz to 100 MHz	V_{NOISE}	300	—	—	mV_{PP}	—
Noise Spike Suppression Time	t_{SPIKE}	0	—	50	ns	Note 3
I^2C Bus Operating Frequency	f_{I2C}	0	—	400	kHz	—
Bus Free Time Between Stop and Start Condition	t_{BUF}	1.3	—	—	µs	—
Hold Time After (Repeated) Start Condition	$t_{HD:STA}$	0.6	—	—	µs	After this period, the first clock is generated.

I²C BUS ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Repeated Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	µs	—
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—	—	µs	—
Data Hold Time	$t_{HD:DAT}$	0	—	0.9	µs	Note 4
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	—
Clock Low Period	t_{LOW}	1.3	—	—	µs	—
Clock High Period	t_{HIGH}	0.6	—	—	µs	—
Clock/Data Fall Time	t_F	20 + 0.1*Cb	—	250	ns	Note 2
Clock/Data Rise Time	t_R	20 + 0.1*Cb	—	250	ns	Note 2

Note 1: 3V to 5V ±10%.

2: Rise and fall time is defined as follows: $t_R = (V_{IL,MAX} – 0.15)$ to $(V_{IH,MIN} + 0.15)$; $t_F = (V_{IH,MIN} – 0.15)$ to $(V_{IL,MAX} + 0.15)$

3: Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

4: The maximum hold time has to be less than the maximum data valid or data valid acknowledge time as per Table 10, note [4] of I²C bus Rev. 6 specification.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Operating Temperature Range	T_A	–40	—	+105	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Junction to Ambient Thermal Resistance 6x6 VQFN-48Ld	Θ_{JA}	—	29	—	°C/W	Still-Air
		—	24	—	°C/W	1 m/s airflow
		—	22	—	°C/W	2.5 m/s airflow
Junction to Board Thermal Resistance 6x6 VQFN-48Ld	Θ_{JB}	—	8	—	°C/W	—
Junction to Case Thermal Resistance 6x6 VQFN-48Ld	Θ_{JC}	—	18	—	°C/W	—
Thermal Characterization, Junction to Top of Package 6x6 VQFN-48Ld	Ψ_{JB}	—	1	—	°C/W	Still-Air
Junction to Ambient Thermal Resistance 8x8 VQFN-56Ld	Θ_{JA}	—	28	—	°C/W	Still-Air
		—	23	—	°C/W	1 m/s airflow
		—	22	—	°C/W	2.5 m/s airflow
Junction to Board Thermal Resistance 8x8 VQFN-56Ld	Θ_{JB}	—	8	—	°C/W	—
Junction to Case Thermal Resistance 8x8 VQFN-56Ld	Θ_{JC}	—	14	—	°C/W	—
Thermal Characterization, Junction to Top of Package 8x8 VQFN-56Ld	Ψ_{JB}	—	1	—	°C/W	Still-Air

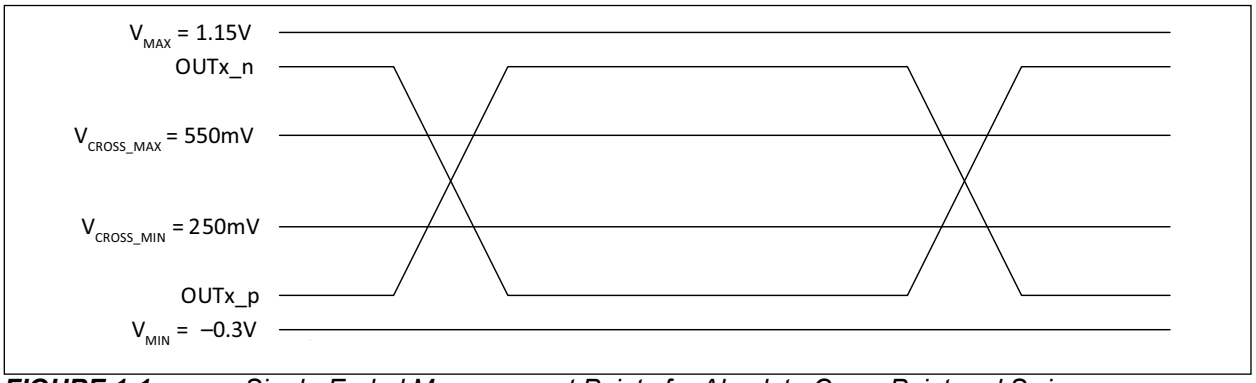


FIGURE 1-1: *Single-Ended Measurement Points for Absolute Cross Point and Swing.*

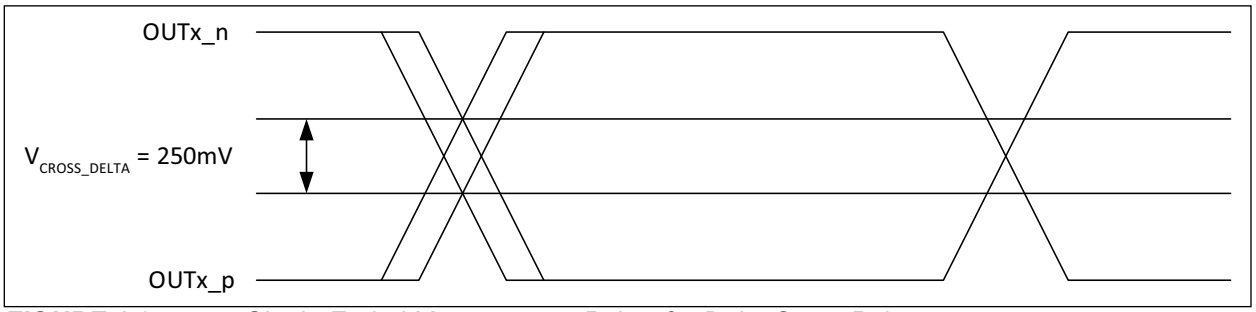


FIGURE 1-2: *Single-Ended Measurement Points for Delta Cross Point.*

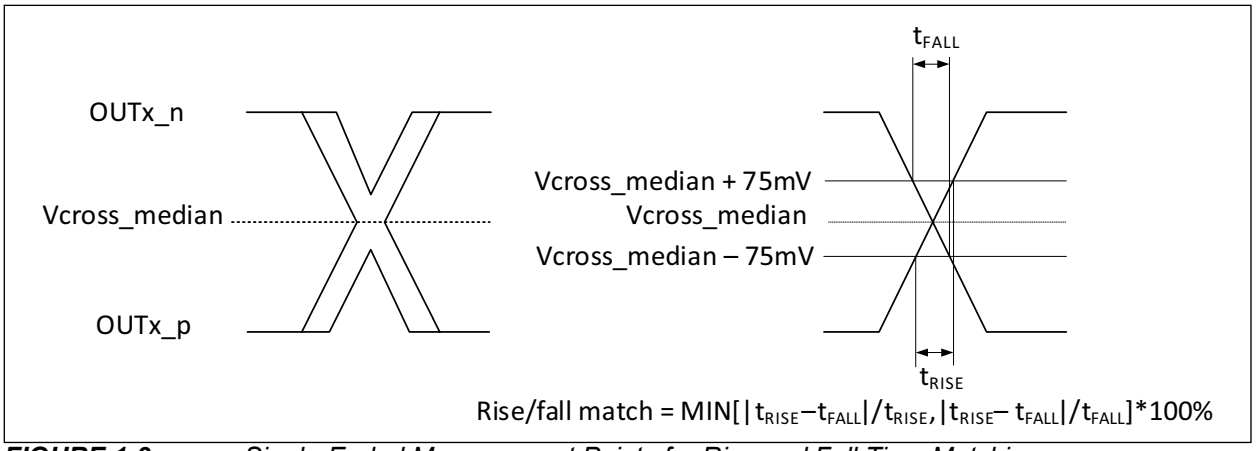


FIGURE 1-3: *Single-Ended Measurement Points for Rise and Fall Time Matching.*

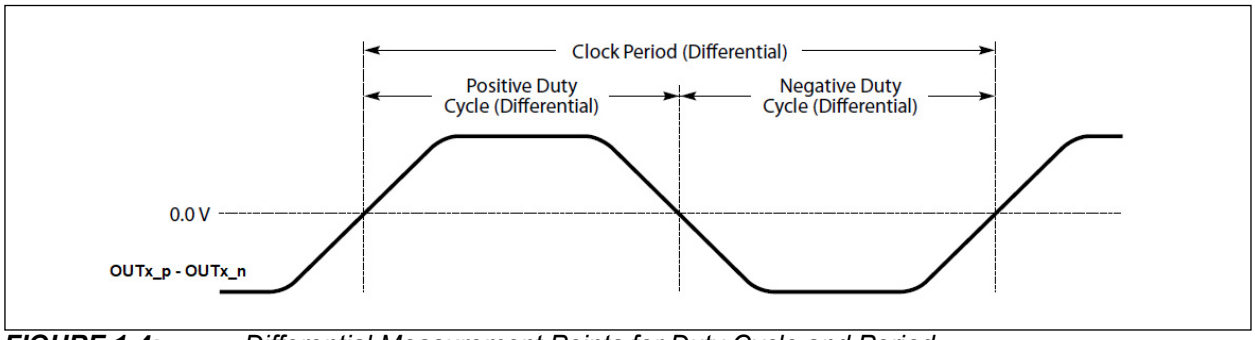


FIGURE 1-4: *Differential Measurement Points for Duty Cycle and Period.*

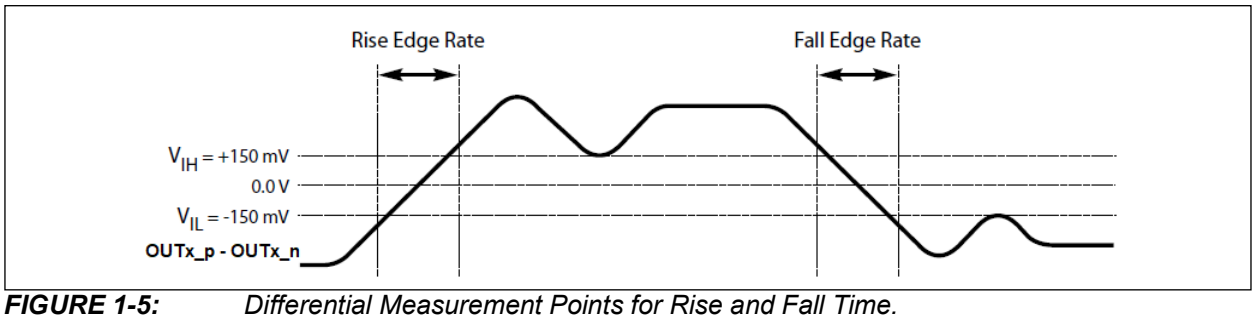


FIGURE 1-5: *Differential Measurement Points for Rise and Fall Time.*

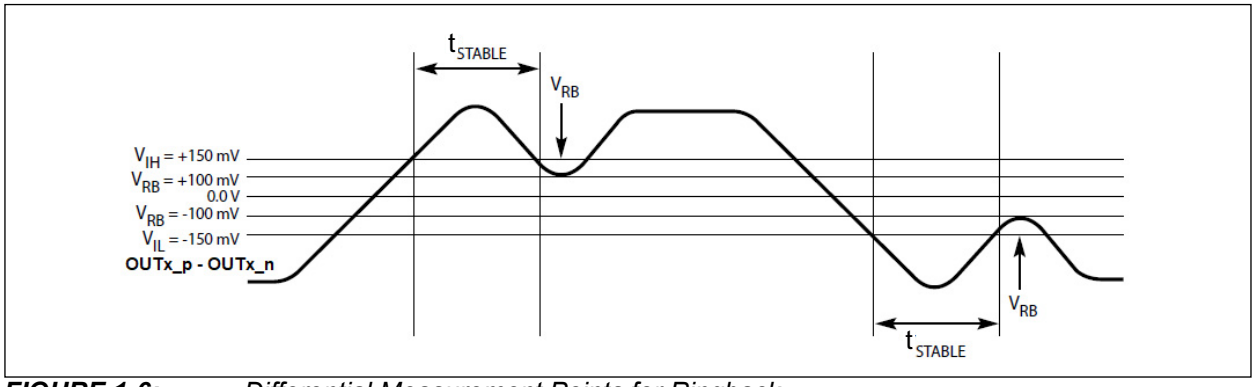


FIGURE 1-6: *Differential Measurement Points for Ringback.*

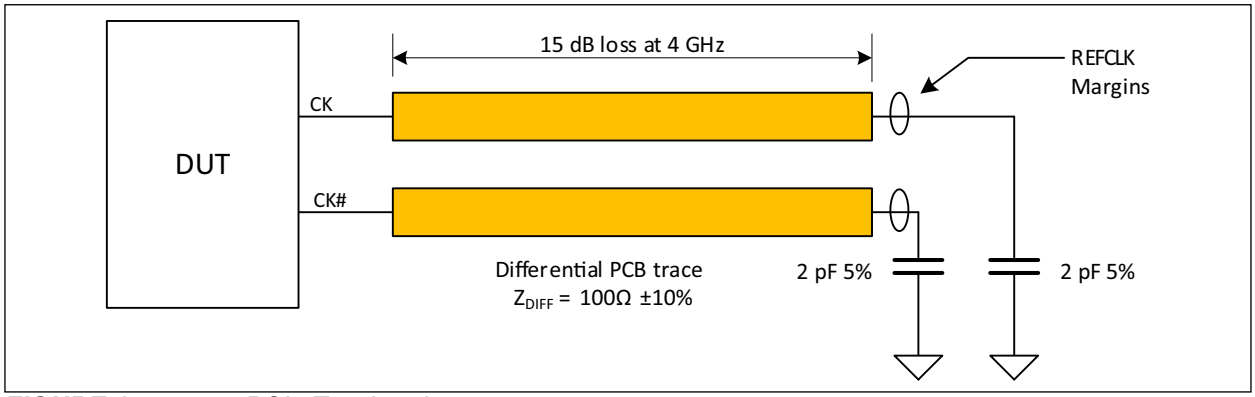


FIGURE 1-7: *PCIe Test Load.*

2.0 TYPICAL OPERATING CHARACTERISTICS

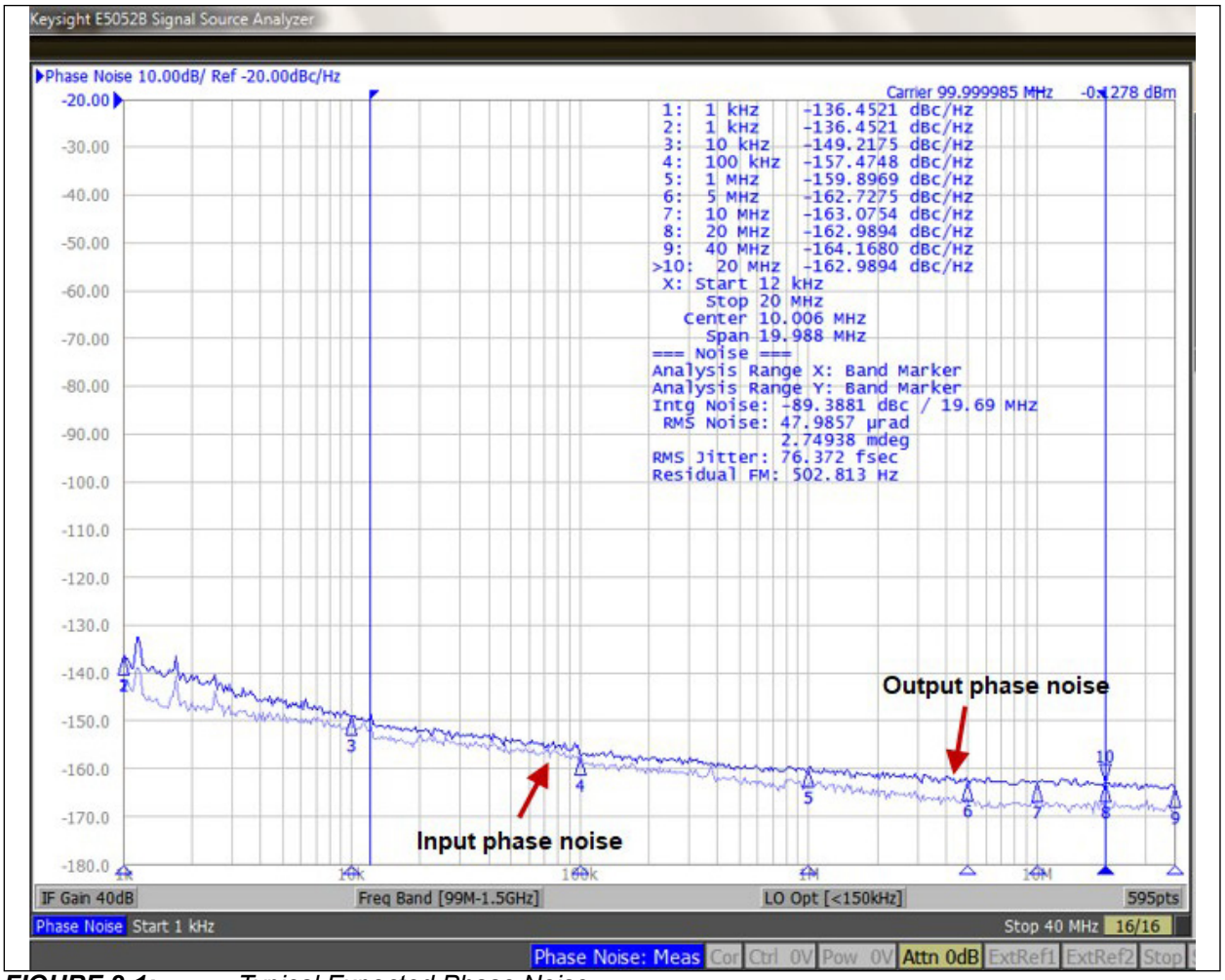


FIGURE 2-1: *Typical Expected Phase Noise.*

3.0 PIN DESCRIPTIONS

All device inputs and outputs are LPHCSL unless described otherwise. The Type column uses the following symbols:

- I: Input
- IPU: Input with 100 kΩ internal pull-up resistor
- IPD: Input with 100 kΩ internal pull-down resistor
- O: Output
- I/OOD: Input/Open-Drain Output
- NC: No Connect
- P: Power Supply

The descriptions of the pins are listed in Table 3-1 and Table 3-2.

TABLE 3-1: SY75608 PIN FUNCTION TABLE

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>16</td><td>IN0_p</td><td rowspan="4">I</td><td rowspan="4">Differential/Single Ended References 0 and 1

Input frequency range >0 Hz to 250 MHz

Note: >0 Hz means frequency higher than DC. Output Enable control pins (OEnb) need four clock cycles before the corresponding output get enabled/disable. This feature ensures glitch free transition of the outputs.</td></tr>
<tr><td>17</td><td>IN0_n</td></tr>
<tr><td>21</td><td>IN1_p</td></tr>
<tr><td>20</td><td>IN1_n</td></tr>
<tr><td>1</td><td>OUT0_p</td><td rowspan="16">O</td><td rowspan="16">Ultra-Low Additive Jitter Differential LPHCSL Outputs 0 to 7

Output frequency range >0 Hz to 250 MHz

In I²C bus controlled mode (SEL pin pulled high) output enable is controlled via internal registers

In Hardware control mode (SEL pin pulled low) output enable is controlled by OE_n pins.</td></tr>
<tr><td>2</td><td>OUT0_n</td></tr>
<tr><td>4</td><td>OUT1_p</td></tr>
<tr><td>5</td><td>OUT1_n</td></tr>
<tr><td>8</td><td>OUT2_p</td></tr>
<tr><td>9</td><td>OUT2_n</td></tr>
<tr><td>11</td><td>OUT3_p</td></tr>
<tr><td>12</td><td>OUT3_n</td></tr>
<tr><td>25</td><td>OUT4_p</td></tr>
<tr><td>26</td><td>OUT4_n</td></tr>
<tr><td>28</td><td>OUT5_p</td></tr>
<tr><td>29</td><td>OUT5_n</td></tr>
<tr><td>32</td><td>OUT6_p</td></tr>
<tr><td>33</td><td>OUT6_n</td></tr>
<tr><td>35</td><td>OUT7_p</td></tr>
<tr><td>36</td><td>OUT7_n</td></tr>
<tr><td rowspan="5">45</td><td rowspan="5">IN_SEL0
/I2C_SA_0</td><td rowspan="5">IPD</td><td>Input Select 0 or I²C Address
When SEL pin is low, this pin is Input Select 0 hardware control input. When SEL pin is high, this pin together with pin 44 provides address for I²C Bus. This pin is pulled down with 100 kΩ resistor.</td></tr>
<tr><td>
<table>
<tr><th>IN_SEL1</th><th>IN_SEL0</th><th>OUTN</th></tr>
<tr><td>0</td><td>0</td><td>Input 0 (IN0)</td></tr>
<tr><td>0</td><td>1</td><td>Input 1 (IN1)</td></tr>
<tr><td>1</td><td>0</td><td>Crystal Oscillator or Overdrive</td></tr>
<tr><td>1</td><td>1</td><td>Crystal Bypass</td></tr>
</table>
</td></tr>
<tr><td rowspan="3"></td></tr>
<tr></tr>
<tr></tr>
<tr><td>44</td><td>IN_SEL1
/I2C_SA_1</td><td>IPD</td><td>Input Select 1 or Serial Interface Input
When SEL pin is low, this pin is Input Select 1 hardware control pin. When SEL pin is high, this pin together with pin 45 provides address for I²C Bus. This pin is pulled down with 100 kΩ resistor.</td></tr>
</table>

TABLE 3-1: SY75608 PIN FUNCTION TABLE (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td rowspan="7">43</td><td rowspan="7">OE_TYPE0
/I2C_SCL</td><td rowspan="7">IPD/O</td><td>Output Signal Type or I²C Bus Clock
When SEL pin is low this pin and pin 42 selects output type.</td></tr>
<tr><td>
<table>
<tr><th>OE_TYPE1</th><th>OE_TYPE0</th><th>Output [7:0] state when OE_n is high</th></tr>
<tr><td>0</td><td>0</td><td>Both p and n are pulled low via internal output termination resistors per standard HCSL (PCIe)</td></tr>
<tr><td>0</td><td>1</td><td>Drive Differential Low: p is pulled low and n is pulled high via output termination resistors</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>High-Z (disabled)</td></tr>
</table>
</td></tr>
<tr><td>When SEL pin is high this pin is I²C Bus Clock. This pin is pulled down with 100 kΩ resistor when SEL is low.</td></tr>
<tr><td>42</td><td>OE_TYPE1/
I2C_SDA</td><td>IPD/OOD</td><td>Output Signal Type or I²C Bus I/O Data
When SEL pin is low, this pin and pin 43 selects output type.
When SEL pin is high, this pin is an I/O pin (Input/Open-Drain) for I²C Bus.
This pin is pulled down with 100 kΩ resistor when SEL is low.</td></tr>
<tr><td>48</td><td>OE0b</td><td rowspan="8">IPD</td><td rowspan="8">Output Enable Control
When the SEL pin is low and OEnb is low, the output n where n = {0,..,7} is active.
When the SEL pin is low and OEnb is high, the output is dependent on OE_TYPE0/1 pins
OEnb is synchronous and it need four clock cycles before the corresponding output gets enabled/disabled.

OEnb pins are pulled-down with 100 kΩ resistor.</td></tr>
<tr><td>47</td><td>OE1b</td></tr>
<tr><td>14</td><td>OE2b</td></tr>
<tr><td>13</td><td>OE3b</td></tr>
<tr><td>23</td><td>OE4b</td></tr>
<tr><td>22</td><td>OE5b</td></tr>
<tr><td>38</td><td>OE6b</td></tr>
<tr><td>37</td><td>OE7b</td></tr>
<tr><td>18</td><td>XIN</td><td>I</td><td>Crystal Oscillator Input or Crystal Bypass Mode or Crystal Overdrive Mode
If crystal circuit is not used, pull-down this pin or connect it to ground.</td></tr>
<tr><td>19</td><td>XOUT</td><td>O</td><td>Crystal Oscillator Output</td></tr>
<tr><td>41</td><td>SEL</td><td>IPD</td><td>Select Control
When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE_TYPE0/1.
When this pin is high, the device is controlled via I²C Bus port.

Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly.
This pin is pulled down with 100 kΩ resistor.</td></tr>
<tr><td>24</td><td>OUT_IMP_SEL</td><td>IPD</td><td>Output Impedance Select
When this pin is low, the output differential impedance is 100Ω
When this pin is high, the output differential impedance is 85Ω
This pin is pulled down with 100 kΩ resistor.</td></tr>
<tr><td>15</td><td rowspan="3">VDD</td><td rowspan="3">P</td><td rowspan="3">Positive Supply Voltage
Connect to 3.3V, 2.5V, or 1.8V supply.</td></tr>
<tr><td>39</td></tr>
<tr><td>46</td></tr>
</table>

TABLE 3-1: SY75608 PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Pin Type	Description
3	VDDO	P	**Positive Supply Voltage for Differential Outputs** Connect to 3.3V, 2.5V or 1.8V supply. These pins power up differential outputs OUT[7:0]_p/n.
10			
27			
34			
40	VPP	P	**Positive Supply Voltage for Programming OTP Memory** This pin is used for generating custom configurations on ATE. Connect to ground for normal operation.
6	GND	P	**Ground** Connect to ground.
7			
30			
31			
ePAD			

TABLE 3-2: SY75612 PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
20	IN0_p	I	**Differential/Single-Ended References 0 and 1** Input frequency range >0 Hz to 250 MHz Note: >0 Hz means frequency higher than DC. Output Enable control pins (OEnb) need four clock cycles before the corresponding output get enabled/disable. This feature ensures glitch free transition of the outputs.
21	IN0_n		
25	IN1_p		
24	IN1_n		
1	OUT0_p	O	**Ultra-Low Additive Jitter Differential LPHCSL Outputs 0 to 11** Output frequency range >0 Hz to 250 MHz In I^2C bus controlled mode (SEL pin pulled high) output enable is controlled via internal registers In Hardware control mode (SEL pin pulled low) output enable is controlled by OE_n pins.
2	OUT0_n		
4	OUT1_p		
5	OUT1_n		
6	OUT2_p		
7	OUT2_n		
8	OUT3_p		
9	OUT3_n		
10	OUT4_p		
11	OUT4_n		
13	OUT5_p		
14	OUT5_n		
29	OUT6_p		
30	OUT6_n		
32	OUT7_p		
33	OUT7_n		
34	OUT8_p		
35	OUT8_n		
36	OUT9_p		
37	OUT9_n		
38	OUT10_p		
39	OUT10_n		
41	OUT11_p		
42	OUT11_n		

TABLE 3-2: SY75612 PIN FUNCTION TABLE (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td rowspan="6">52</td><td rowspan="6">IN_SEL0
/I2C_SA_0</td><td rowspan="6">IPD</td><td>Input Select 0 or I²C Address
When SEL pin is low, this pin is Input Select 0 hardware control input.
When SEL pin is high, this pin together with pin 51 provides address for I²C Bus. This pin is pulled down with 100 kΩ resistor when SEL is low.</td></tr>
<tr><td><table>
<tr><th>IN_SEL1</th><th>IN_SEL0</th><th>OUTN</th></tr>
<tr><td>0</td><td>0</td><td>Input 0 (IN0)</td></tr>
<tr><td>0</td><td>1</td><td>Input 1 (IN1)</td></tr>
<tr><td>1</td><td>0</td><td>Crystal Oscillator or Overdrive</td></tr>
<tr><td>1</td><td>1</td><td>Crystal Bypass</td></tr>
</table></td></tr>
<tr><td>51</td><td>IN_SEL1
/I2C_SA_1</td><td>IPD</td><td>Input Select 1 or Serial Interface Input
When SEL pin is low, this pin is Input Select 1 hardware control pin.
When SEL pin is high, this pin together with pin 52 provides address for I²C Bus.
This pin is pulled-down with 100 kΩ resistor when SEL is low.</td></tr>
<tr><td rowspan="2">50</td><td rowspan="2">OE_TYPE0
/I2C_SCL</td><td rowspan="2">IPD/O</td><td>Output Signal Type or I²C Bus Clock
When SEL pin is low this pin and pin 49 selects output type.</td></tr>
<tr><td><table>
<tr><th>OE_TYPE1</th><th>OE_TYPE0</th><th>Output [11:0] state when OE_n is high</th></tr>
<tr><td>0</td><td>0</td><td>Both p and n are pulled low via internal output termination resistors per standard HCSL (PCIe)</td></tr>
<tr><td>0</td><td>1</td><td>Drive Differential Low: p is pulled low and n is pulled high via output termination resistors</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>High-Z (Disabled)</td></tr>
</table>When SEL pin is high this pin is I²C Bus Clock.
This pin is pulled-down with 100 kΩ resistor.</td></tr>
<tr><td>49</td><td>OE_TYPE1
/I2C_SDA</td><td>IPD/OOD</td><td>Output Signal Type or I²C Bus I/O Data
When SEL pin is low, this pin and pin 50 selects output type.
When SEL pin is high, this pin is an I/O pin (Input/Open-Drain) for I²C Bus.
This pin is pulled down with 100 kΩ resistor.</td></tr>
<tr><td>56</td><td>OE0b</td><td rowspan="12">IPD</td><td rowspan="12">Output Enable Control
When the SEL pin is low and OEnb is low the output n where n = {0,..,11} is active
When the SEL pin is low and OEnb is high the output is dependent on OE_TYPE0/1 pins

OEnb is synchronous and it need four clock cycles before the corresponding output gets enabled/disabled.

OEnb pins are pulled-down with 100 kΩ resistor.</td></tr>
<tr><td>55</td><td>OE1b</td></tr>
<tr><td>54</td><td>OE2b</td></tr>
<tr><td>17</td><td>OE3b</td></tr>
<tr><td>16</td><td>OE4b</td></tr>
<tr><td>15</td><td>OE5b</td></tr>
<tr><td>27</td><td>OE6b</td></tr>
<tr><td>26</td><td>OE7b</td></tr>
<tr><td>19</td><td>OE8b</td></tr>
<tr><td>45</td><td>OE9b</td></tr>
<tr><td>44</td><td>OE10b</td></tr>
<tr><td>43</td><td>OE11b</td></tr>
<tr><td>22</td><td>XIN</td><td>I</td><td>Crystal Oscillator Input or Crystal Bypass Mode or Crystal Overdrive Mode
If crystal circuit is not used pull-down this pin or connect it to the ground.</td></tr>
<tr><td>23</td><td>XOUT</td><td>O</td><td>Crystal Oscillator Output</td></tr>
</table>

TABLE 3-2: SY75612 PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Pin Type	Description
48	SEL	IPD	**Select control** When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE_TYPE0/1. When this pin is high, the device is controlled via I^2C Bus port. Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly. This pin is pulled down with 100 kΩ resistor.
28	OUT_IMP_SEL	IPD	**Output Impedance Select** When this pin is low, the output differential impedance is 100Ω When this pin is high, the output differential impedance is 85Ω This pin is pulled down with 100 kΩ resistor.
18	VDD	P	**Positive Supply Voltage** Connect to 3.3V, 2.5V, or 1.8V supply.
46			
53			
3	VDDO	P	**Positive Supply Voltage for Differential Outputs** Connect to 3.3V, 2.5V, or 1.8V power supply. These pins power up differential outputs OUT[11:0]_p/n.
12			
31			
40			
47	VPP	P	**Positive Supply Voltage for Programming OTP Memory** This pin is used for generating custom configurations on ATE. Connect to ground for normal operation.
ePAD	GND	P	**Ground** Connect to ground

4.0 FUNCTIONAL DESCRIPTION

The SY75608 and SY75612, respectively, are 2-to-8 and 2-to-12 PCIe clock buffers with ultra-low additive jitter. They can be used in all PCIe 1/2/3/4/5/6 common clock and SRIS applications.

Each output can be enabled/disabled glitch-free via dedicated OE pins or via I^2C bus.

The SY75608/612 each have an embedded low-dropout regulator (LDO) for superior power noise supply rejection. They support 1.8V, 2.5V, and 3.3V supplies with tolerance of ±10%, which exceeds the ±9% required by PCIe Card Electro Mechanical Specification.

Besides operating as fanout buffers, these devices can work as fixed frequency clock generators with external crystal. Supported crystal frequencies are 8 MHz to 160 MHz.

4.1 Clock Input

The following figures show how to terminate input of the device in most common cases: Low Power HCSL (LPHCSL), HCSL, and single-ended LVCMOS.

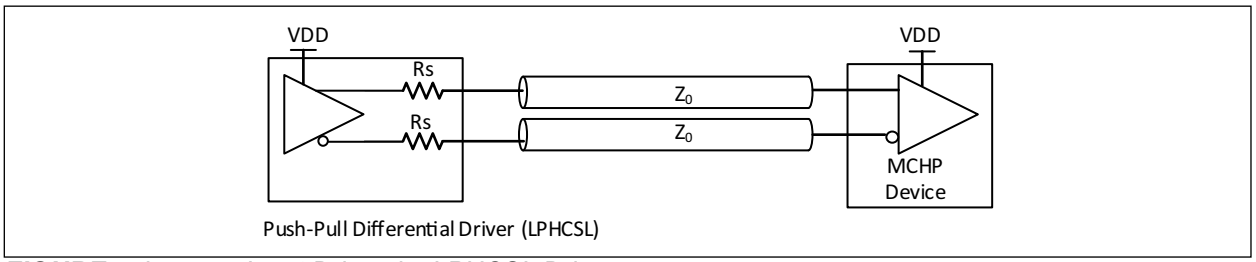


FIGURE 4-1: *Input Driven by LPHCSL Driver.*

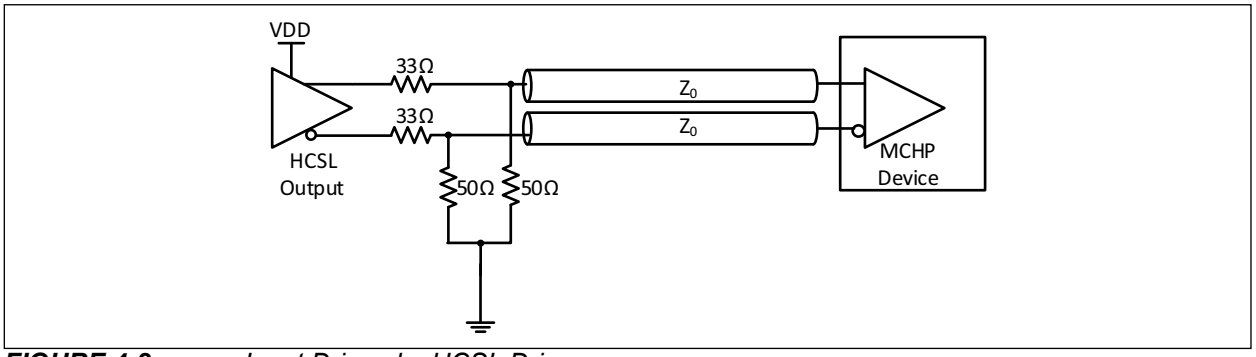
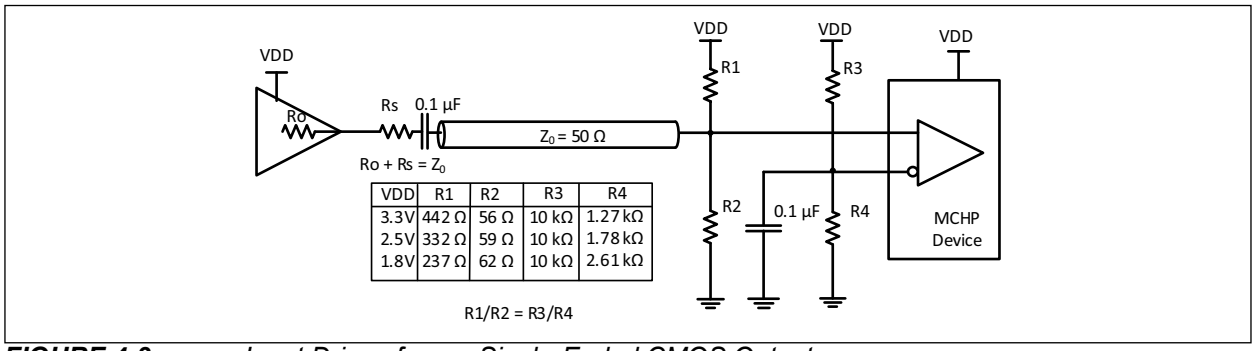


FIGURE 4-2: *Input Driven by HCSL Driver.*

Figure 4-3 shows how to terminate a single-ended output, such as LVCMOS. This example assumes 50Ω transmission line, which is the most common for single-ended CMOS signaling. Ideally, resistors R1 and R2 should be 100Ω each and $R_O + R_S$ should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input, but this should be fine as long as the input voltage swing requirement is not violated (Figure 1-3). The source resistors of R_S = 270Ω could be used for a standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) * (1/(270Ω + 50Ω)) = 5.16 mA.

For optimum performance both differential input pins (_p and _n) need to be DC-biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.



VDD	R1	R2	R3	R4
3.3V	442 Ω	56 Ω	10 kΩ	1.27 kΩ
2.5V	332 Ω	59 Ω	10 kΩ	1.78 kΩ
1.8V	237 Ω	62 Ω	10 kΩ	2.61 kΩ

FIGURE 4-3: *Input Driven from a Single-Ended CMOS Output.*

4.2 Clock Outputs

Differential outputs have embedded termination resistors as shown in Figure 4-4. This provides significant saving relative to traditional current-based HCSL outputs that require four resistors per differential output.

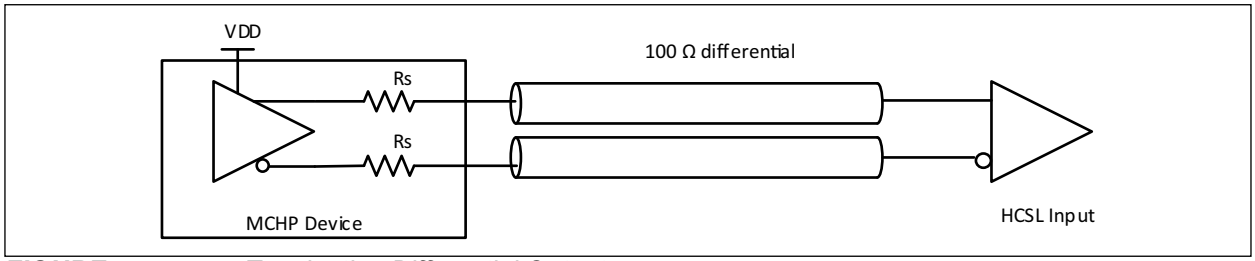


FIGURE 4-4: *Terminating Differential Outputs.*

Embedded termination resistors in SY75608/612 are matched for 85Ω or 100Ω differential transmission lines.

4.3 Crystal Oscillator Circuit

The crystal oscillator circuit can work with crystal resonators from 8 MHz to 160 MHz. As can be seen in Figure 4-5, only a crystal resonator is required and all the other components are built into the device. To be able support crystal resonators with different characteristics all internal components are programmable in I^2C Controlled mode.

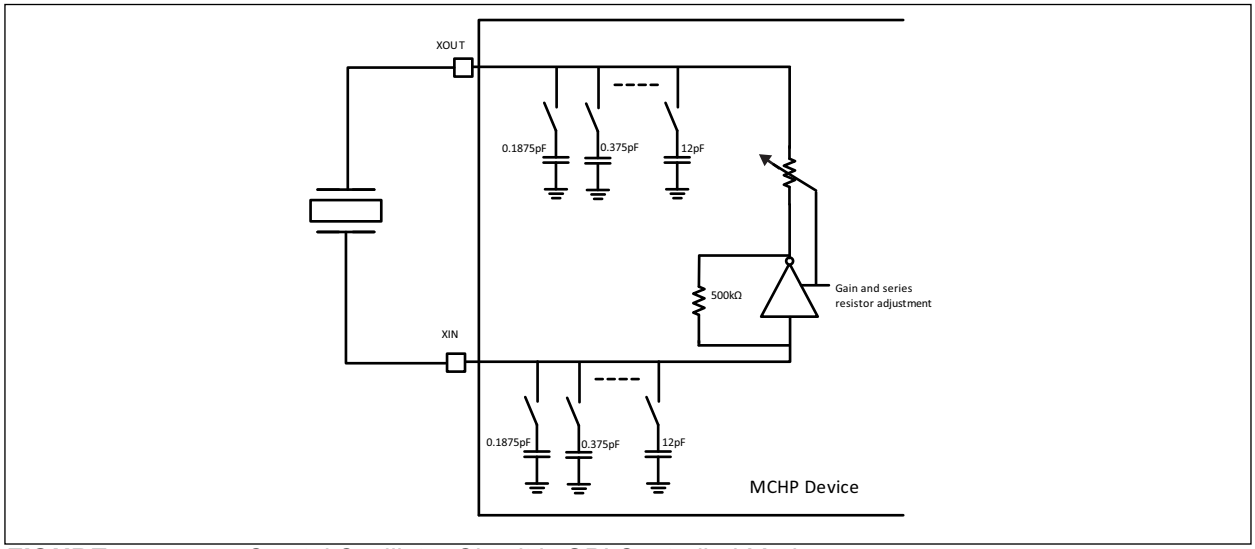


FIGURE 4-5: *Crystal Oscillator Circuit in SPI Controlled Mode.*

Load capacitors can be programmed from 0 pF to 23.8 pF with a resolution of 0.1875 pF that not only meets load requirement for most crystal resonator, but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted by selecting one of seven gain values. The series resistor is adjusted based on the selected gain. Shunt resistor has fixed value of 500 kΩ.

In Hardware Controlled mode, the capacitive load is set at 8 pF and cannot be changed. For crystals that require higher load, additional capacitance can be added externally as shown in Figure 4-6.

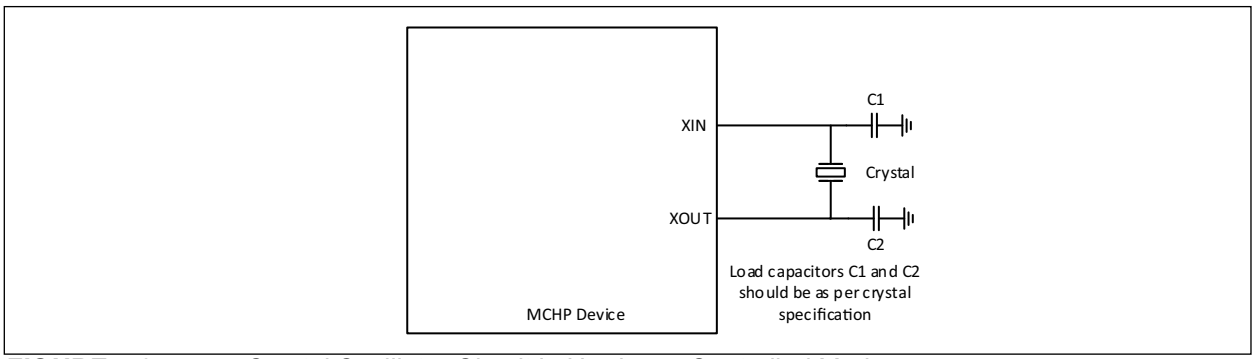


FIGURE 4-6: *Crystal Oscillator Circuit in Hardware Controlled Mode.*

5.0 HOST INTERFACE

SY75608 and SY75612 can be controlled via hardware pins (SEL pin tied low) or via I^2C Bus (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on the fly.

5.1 Hardware Controlled Mode

In this mode, SY75608/612 is controlled via Input Select pins (IN_SEL[1:0]) that select which one of three inputs is fed to outputs (as shown in Table 5-1), output enable pins (OE_b) for each output (as shown in Figure 5-1), and Output Impedance Select pin.

TABLE 5-1: INPUT CLOCK SELECTION

IN_SEL1	IN_SEL0	Selected Input
0	0	IN0_p, IN0_n
0	1	IN1_p, IN1_n
1	X	XIN (crystal input pin)

Any outputs can be disabled by pulling the corresponding OExb pin high. The OExb is sampled on the falling edge of the differential input clock (or falling edge of INx_p). It takes 4.5 clock cycles before the output goes from the active state to the state defined by OE_TYPE0/1 pins (SEL = 0) or defined by DRVSTATE0/1/2 register (SEL = 1) as shown in Figure 5-1.

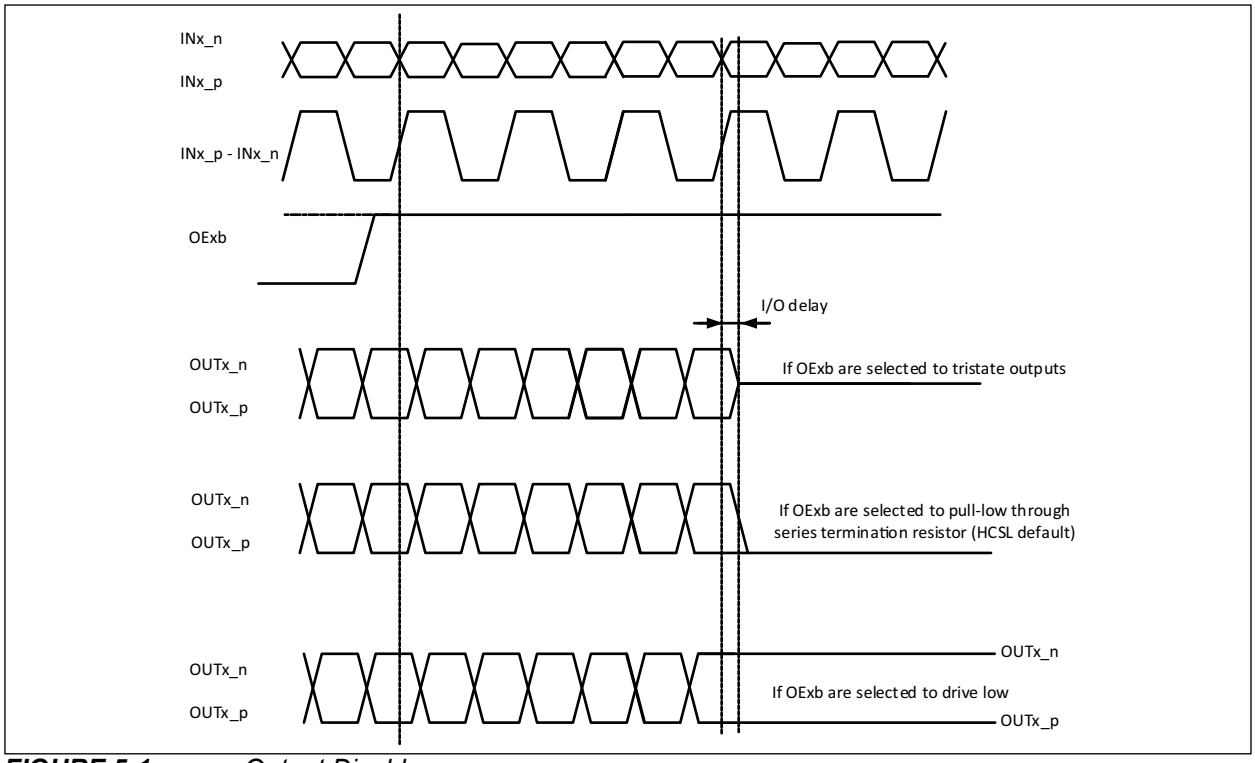


FIGURE 5-1: *Output Disable.*

Any outputs can be enabled by pulling the corresponding OExb pin low. The OExb is sampled on the falling edge of the differential input (or falling edge of Inx_p signal). It takes 3.5 clock cycles of the input clock before the output goes from the state defined by OE_TYPE0/1 pins (SEL pin pulled low) or defined by DRVSTATE0/1/2 registers (SEL pin pulled high) to the active state as shown in Figure 5-2.

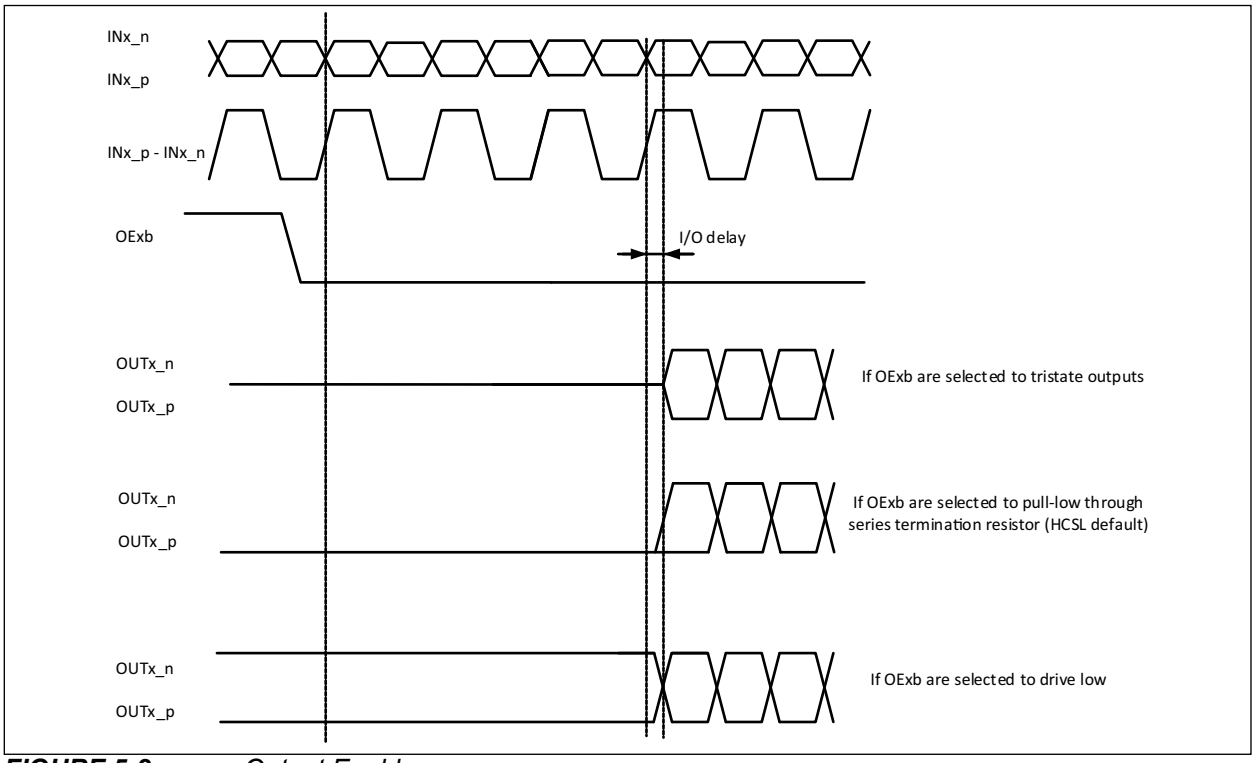


FIGURE 5-2: *Output Enable.*

The Output Impedance Select pin is an asynchronous control input that selects between 100Ω (OUT_IMP_SEL tied low) and 85Ω (OUT_IMP_SEL tied high).

5.2 I²C Bus Control Mode

The SY75608 and SY75612 are controlled via four pin I²C Bus client interface as shown in Figure 5-3.

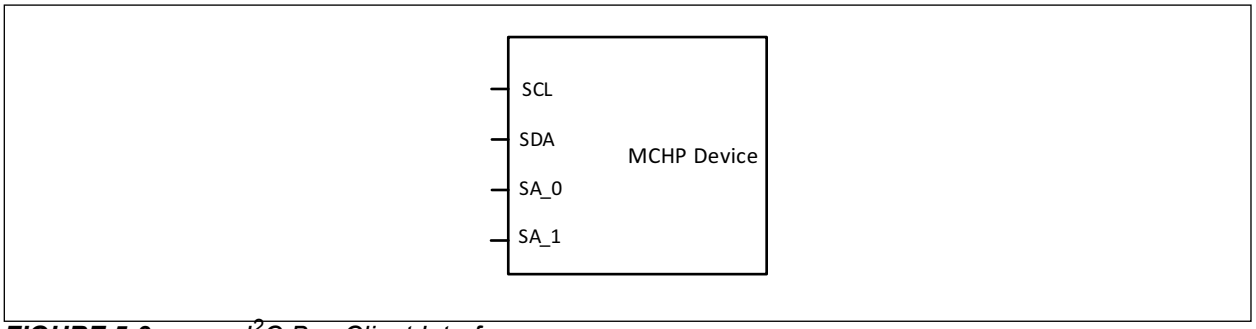


FIGURE 5-3: *I²C Bus Client Interface.*

The address selection is done via SA_0 and SA_1 hardware pins that select the appropriate address for the device.

TABLE 5-2: I²C BUS ADDRESS

SA_1	SA_0	I²C Bus Address
0	0	0x34
0	1	0x35
1	0	0x36
1	1	0x37

5.2.1 I²C BUS READ/WRITE

Reading or writing a register or registers in a I²C Bus client device is MSB first and LBS last in one-byte blocks.

The access from I²C server starts with the start condition followed by the client address and the write indicator bit. This is then followed by the command byte which in bits [6:0] contains the address of the register to be accessed for byte mode or the first register to be accessed in the burst mode. The most significant bit in the command byte must be set to 1.

Byte Read. The standard byte read is as shown in Figure 5-4. The command byte is followed the client address and read indication bit. The device (client) will respond by sending the requested byte.

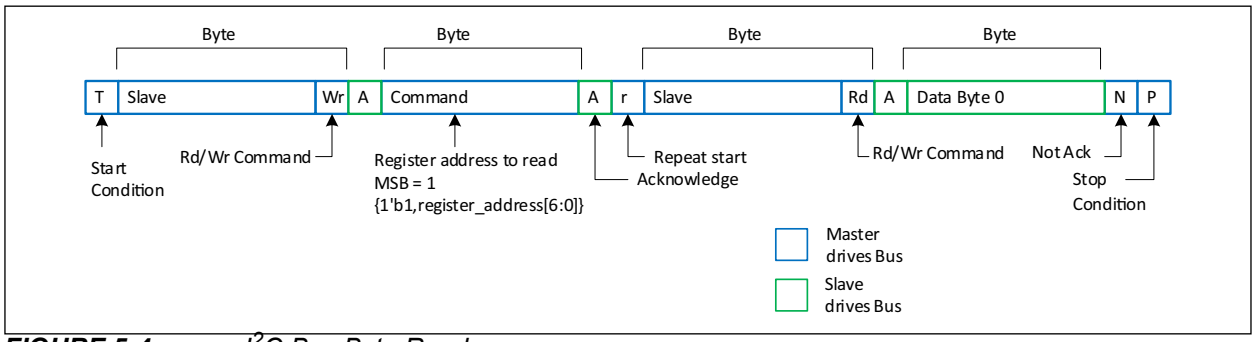


FIGURE 5-4: *I²C Bus Byte Read.*

Write. Figure 5-5 illustrates the standard byte write. After the written byte has been acknowledged by the device, the server will assert the stop signal.

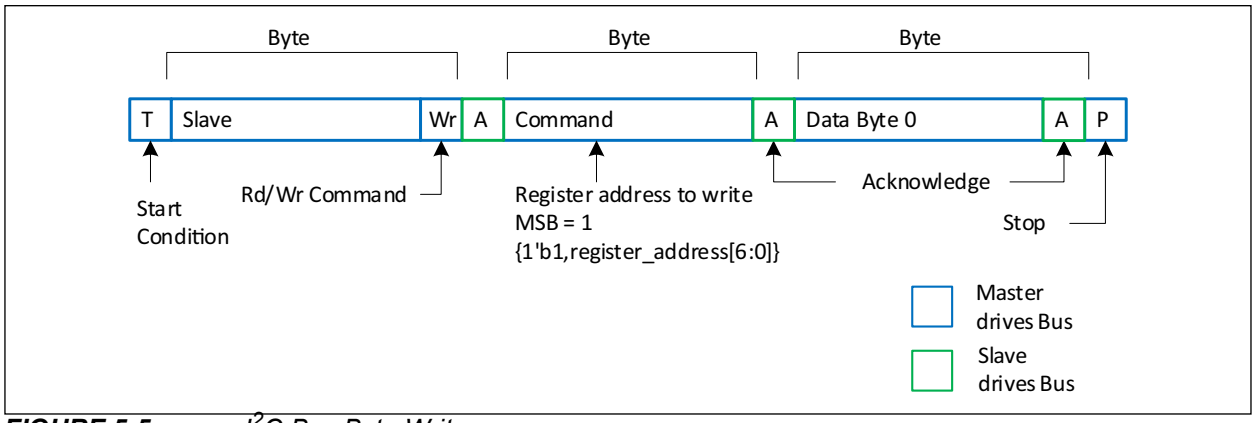


FIGURE 5-5: *I²C Bus Byte Write.*

5.2.2 I²C BURST READ/WRITE

Burst Read and Write are very similar to Byte Read and Write.

Burst Read. Figure 5-6 illustrates the Burst Read. The I²C server acknowledges after each received byte and finally sends a Not Acknowledge (NACK) followed with Stop Condition.

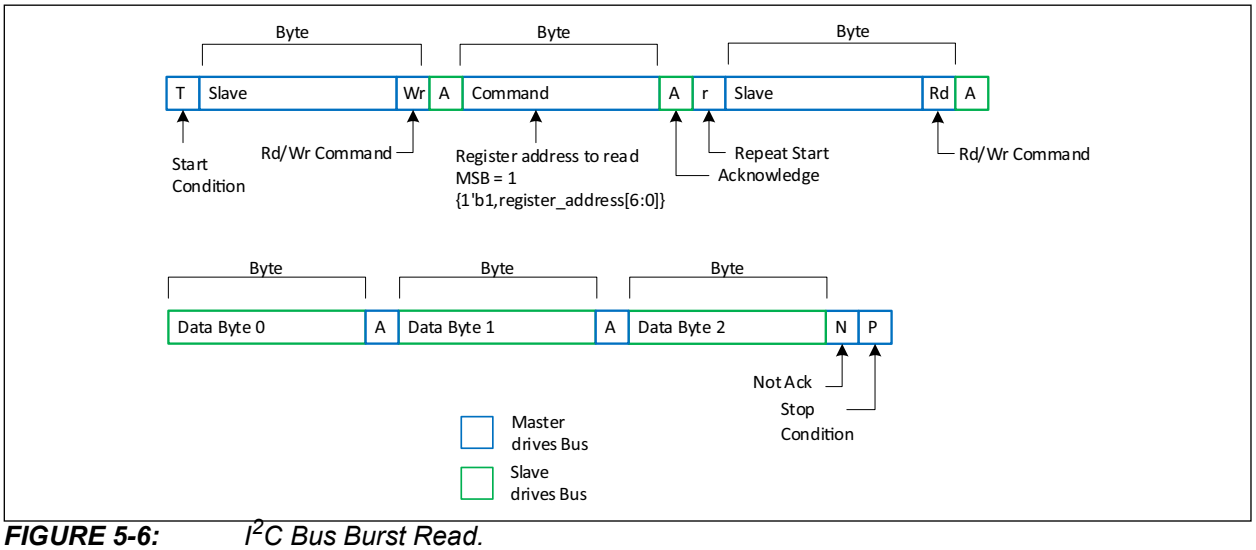


FIGURE 5-6: *I²C Bus Burst Read.*

Burst Write. Figure 5-7 illustrates Burst Write operation. The I²C server will send the Stop Condition after the last data byte.

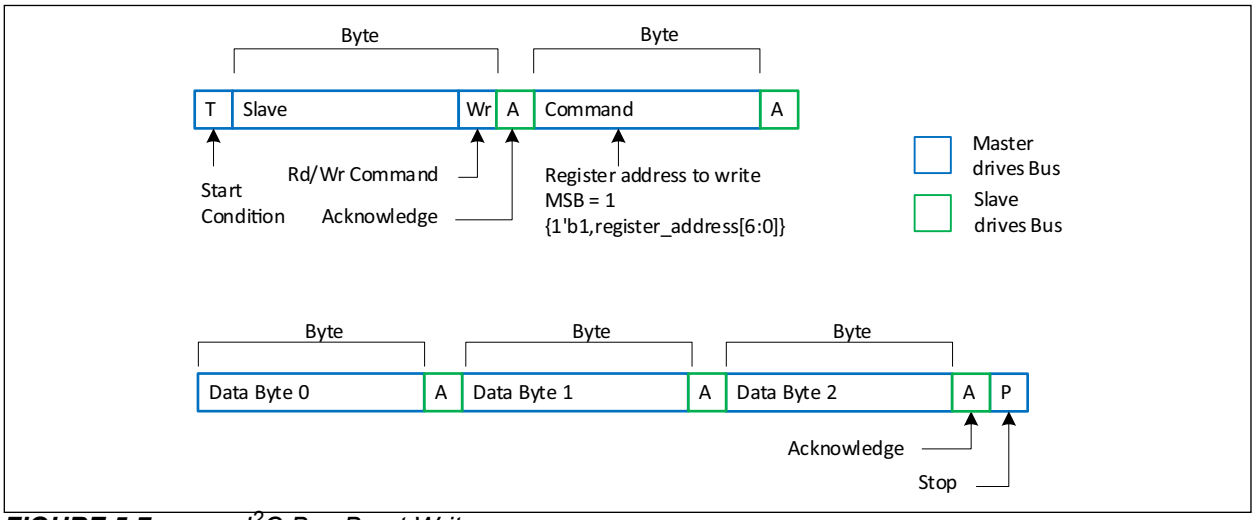


FIGURE 5-7: *I²C Bus Burst Write.*

6.0 REGISTER MAP

The device is controlled by accessing registers through the serial interface. The following table provides a summary of the registers available for the configuration of the device. The default settings can be modified via factory programmable OTP memory (64 bit in total).

TABLE 6-1: REGISTER MAP

Address I^2C A[6:0] Hex (0x)	Name	Data D[7:0]
00	XTALBG	xtal_buf_gain[4:0]
01	Reserved	Leave as default
02	XTALLC	xtal_load_cap[7:0]
03	XTALNR	xtal_normal_run
04	INSEL	input_select[1:0]
05	OUTDSTATE0	out_disable_state[7:0] (differential output OUT3, OUT2, OUT1, OUT0)
06	OUTDSTATE1	out_disable_state[15:8] (differential output OUT7, OUT6, OUT5, OUT4)
07	OUTDSTATE2	out_disable_state[23:16] (differential output OUT11, OUT10, OUT9, OUT8), SY75612 Only
08	OUTEN0	outen[7:0]
09	OUTEN1	outen[15:8], SY75612 Only
0A	DEVADDR	dev_addr[2:0]
0B	DEVICEID	Device Identification
0D	IN1_BUFF_CTRL	Differential Input 1 Control

TABLE 6-2: DETAILED REGISTER MAP

<table>
<tr><th>Bit</th><th>Name</th><th colspan="3">Description</th><th>Type</th><th>Reset</th></tr>
<tr><td colspan="7">XTAL Buffer Gain - XTALBG (0x00)</td></tr>
<tr><td>7:5</td><td>Unused</td><td colspan="3">Leave as default</td><td>R/W</td><td>000</td></tr>
<tr><td rowspan="12">4:0</td><td rowspan="12">xtal_buf_gain[4:0]</td><td colspan="3">Programs crystal buffer (inverting amplifier) gain by selecting number of parallel gain elements:
Each gain value has associated series resistor as shown below:</td><td rowspan="12">R/W</td><td rowspan="12">00100
Note 1</td></tr>
<tr><td>xtal_buf_gain[4:0]</td><td>Number of Parallel XO Amplifiers</td><td>Series Resistance</td></tr>
<tr><td>0</td><td>0</td><td>Open circuit</td></tr>
<tr><td>1</td><td>1</td><td>550Ω</td></tr>
<tr><td>2</td><td>2</td><td>550Ω</td></tr>
<tr><td>3</td><td>3</td><td>550Ω</td></tr>
<tr><td>4</td><td>4</td><td>150Ω</td></tr>
<tr><td>8</td><td>4</td><td>0Ω</td></tr>
<tr><td>16</td><td>8</td><td>0Ω</td></tr>
<tr><td>24</td><td>12</td><td>0Ω</td></tr>
<tr><td colspan="3">Only values 0, 1, 2, 3, 4, 8, 16 and 24 are allowed values to be written to xtal_buf_gain[4:0].
All the other values are reserved.</td></tr>
</table>

TABLE 6-2: DETAILED REGISTER MAP (CONTINUED)

Bit	Name	Description	Type	Reset
XTAL Load Capacitance - XTALLC (0x02)				
7:0	xtal_load_cap[7:0]	Internal load capacitance of crystal circuit (0 pF to 23.8 pF with the resolution of 0.1875 pF). XIN and XOUT have each capacitor connected to GND. Multiple bit combinations available between 7 capacitors. 8'b0000_0000 = Disable all xtal load capacitors 8'b0000_0001 = Enable capacitor 0.1875 pF 8'b0000_0010 = Enable capacitor 0.375 pF 8'b0000_0100 = Enable capacitor 0.75 pF 8'b0000_1000 = Enable capacitor 1.5 pF 8'b0001_0000 = Enable capacitor 3 pF 8'b0010_0000 = Enable capacitor 6 pF 8'b0100_0000 = Enable capacitor 12 pF 8'b1000_0000 = Reserved	R/W	40 Note 1
XTAL Normal Run - XTALNR (0x03)				
7:1	Unused	Unused	R	0000000
0	xtal_normal_run	When this bit is set high crystal oscillator circuit is running only if input_select[1:0] register at address 0x05 selects crystal mode (2'b10). This value is recommended because it provides best jitter performance—XO circuit is running only when it is needed. When this bit is set low the crystal oscillator will keep running even if crystal oscillator is not selected in input_select[1:0] register at address 0x05. This mode should only be used when fast switching between input references and crystal oscillator is required.	R/W	1 Note 1
Input Select - INSEL (0x04)				
7:2	Unused	Unused	R	000000
1:0	input_select[1:0]	Input reference clock selection. Proper external coupling and termination are required. 2'b00 = Differential input from IN0_p and IN0_n 2'b01 = Differential input from IN1_p and IN1_n 2'b10 = Fundamental XTAL mode with XIN and XOUT (Use internal crystal oscillator circuits) or XTAL overdrive mode (single-ended clock signal fed to XIN) 2'b11 = XTAL bypass mode (single-ended clock signal with XIN and disabled internal crystal buffer circuit in the analog block)	R/W	00 Note 1
State of Outputs when Disabled (Outputs 0 to 3) - OUTDSTATE0 (0x05)				
7:6	out_disable_state[7:6]	State of OUT3 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
5:4	out_disable_state[5:4]	State of OUT2 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00

TABLE 6-2: DETAILED REGISTER MAP (CONTINUED)

Bit	Name	Description	Type	Reset
3:2	out_disable_state[3:2]	State of OUT1 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
1:0	out_disable_state[1:0]	State of OUT0 driver when the corresponding bit in OUTEN register is set low. These bits should be set first before the corresponding bit in OUTEN register is toggled. 2'b00 = Both low (p output low, n output low) 2'b01 = Drive Low (p output low, n output high) 2'b10 = Outputs High-Z 2'b11 = Outputs High-Z	R/W	00
State of Outputs when Disabled (Outputs 4 to 7) - OUTDSTATE1 (0x06)				
7:6	out_disable_state[15:14]	State of OUT7 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
5:4	out_disable_state[13:12]	State of OUT6 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
3:2	out_disable_state[11:10]	State of OUT5 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
1:0	out_disable_state[9:8]	State of OUT4 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
State of Outputs when Disabled (Outputs 8 to 11) - OUTDSTATE2 (0x07) (Applies only to SY75612)				
7:6	out_disable_state[23:22]	State of OUT11 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
5:4	out_disable_state[21:20]	State of OUT10 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
3:2	out_disable_state[19:18]	State of OUT9 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
1:0	out_disable_state[17:16]	State of OUT8 driver when the corresponding bit in OUTEN register is set low. The same bit configuration with OUT0.	R/W	00
Output Enable (Outputs 0 to 7) - OUTEN0 (0x08)				
7	outen7	Enable/Disable output 7. The same bit configuration with OUT0.	RW	0
6	outen6	Enable/Disable output 6. The same bit configuration with OUT0.	RW	0
5	outen5	Enable/Disable output 5. The same bit configuration with OUT0.	RW	0
4	outen4	Enable/Disable output 4. The same bit configuration with OUT0.	RW	0
3	outen3	Enable/Disable output 3. The same bit configuration with OUT0.	RW	0
2	outen2	Enable/Disable output 2. The same bit configuration with OUT0.	RW	0

TABLE 6-2: DETAILED REGISTER MAP (CONTINUED)

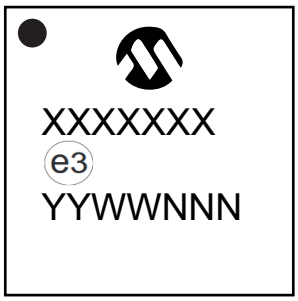
Bit	Name	Description	Type	Reset
1	outen1	Enable/Disable output 1. The same bit configuration with OUT0.	RW	0
0	outen0	Enable/Disable output 0. When this bit is set low the OUT 0 is disabled. The type of the disable mode is specified in the corresponding bit of the OUTDSTATE register. When this bit is set high the OUT0 is in LPHCSL active mode.	RW	0
Output Enable (Outputs 11 to 8) - OUTEN1 (0x09) (Applies only to SY75612)				
7:4	Reserved	Leave as default	RW	0000
3	outen11	Enable/Disable output 11. The same bit configuration with OUT0.	RW	0
2	outen10	Enable/Disable output 10. The same bit configuration with OUT0.	RW	0
1	outen9	Enable/Disable output 9. The same bit configuration with OUT0.	RW	0
0	outen8	Enable/Disable output 8. The same bit configuration with OUT0.	RW	0
I^2C Bus Client Device Address - DEVADDR (0x0A)				
7:2	Unused	Unused	R	000000
1:0	dev_addr[1:0]	These three bits contributes as the following to the 7 bits of the I^2C Bus client address {2'b011, dev_addr[1:0],SA1,SA0}, where SA0 and SA1 are from pins IN_SEL0_I2C_SA_0 and IN_SEL0_I2C_SA_0 respectively	RW	01 Note 1
Device Identification - DEVID (0x0B)				
7	Unused	Unused	R	0
6:3	Revision Number	Silicon Revision Number	RO	0010
2:0	dev_id[2:0]	Device ID 3'b001 = SY75608 3'b002 = SY75612	RO	001(Note 1) or 010(Note 1)
Differential Input 1 Control - IN1_BUFF_CTRL (0x0D)				
7:6	Unused	Unused	R	0
5:2	in1_buff_ctrl	Bias current control from low (4'b0000) to high (4'b1111)	RW	1010 Note 1
1	in1_buff_powdwn	1'b0 = Input buffer is enabled 1'b1 = Input buffer is powered down	RW	0
0	in1_buff_ac_coupl	This bit selects either internal DC or AC coupling of the differential input 1 signal. 1'b0 = Input is DC-coupled 1'b1 = Input is AC-coupled	RW	0

Note 1: The default value is OTP programmable.

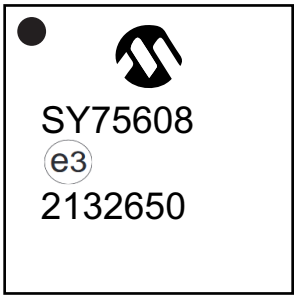
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

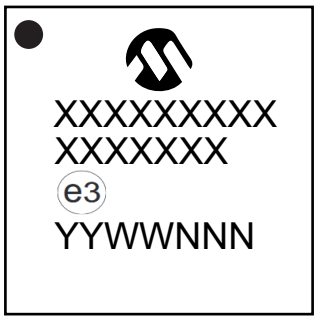
48-Lead VQFN*



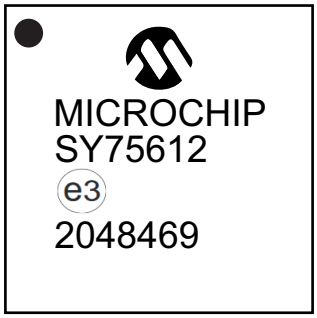
Example



56-Lead VQFN*



Example



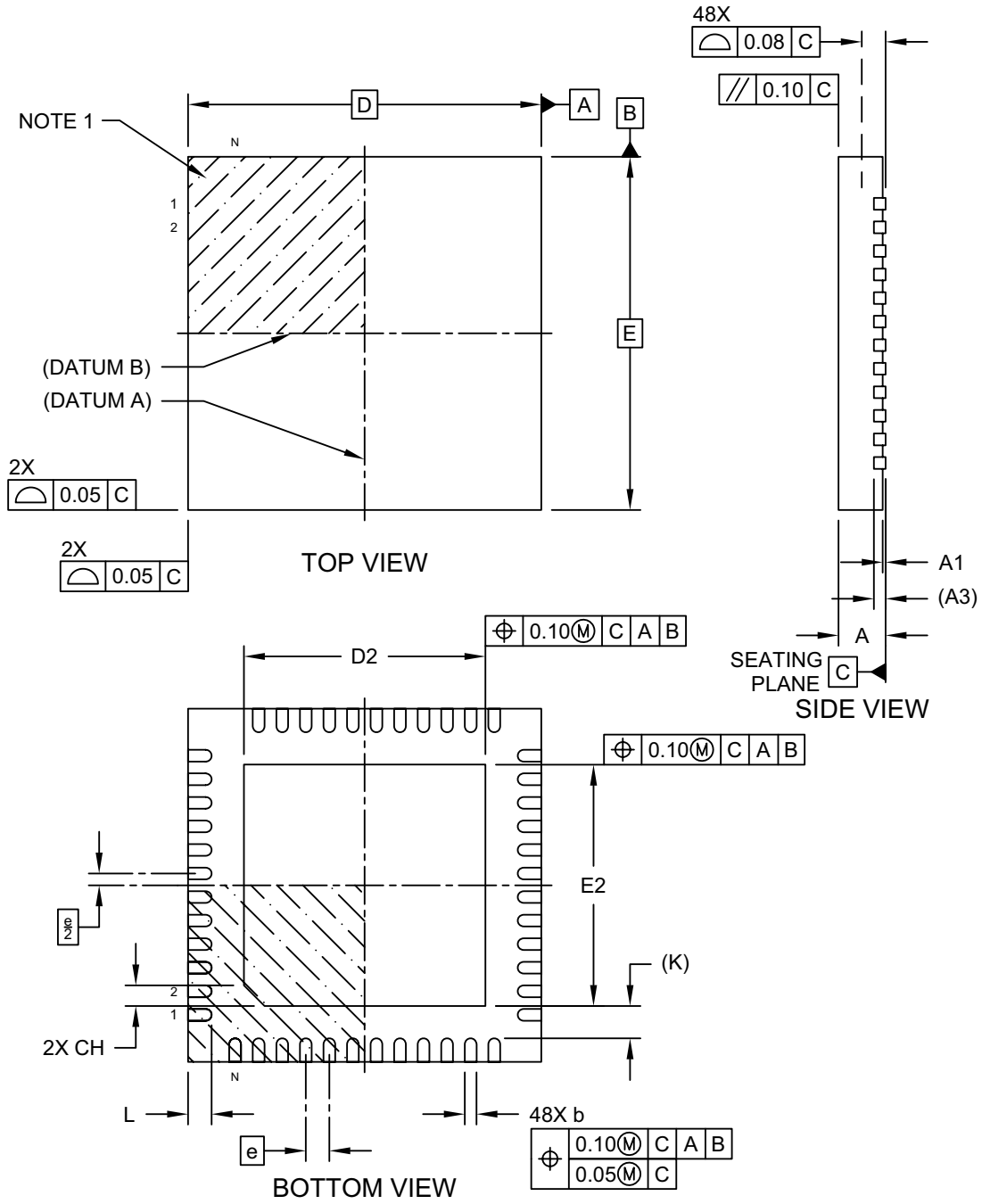
Note: For customers ordering these parts with a customized configuration, the characters “GXXX” will appear on the marking to the right of the JEDEC designator in which “XXX” represents a numerical code. Please visit the ClockWorks Configurator to design your particular specifications.

Legend:	XX...X	Product code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3) *	Pb-free JEDEC® designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

48-Lead VQFN 6 mm x 6 mm Package Outline and Recommended Land Pattern

48-Lead Very Thin Plastic Quad Flat, No Lead Package (6LX) - 6x6 mm Body [VQFN] With 4.1x4.1 mm Exposed Pad

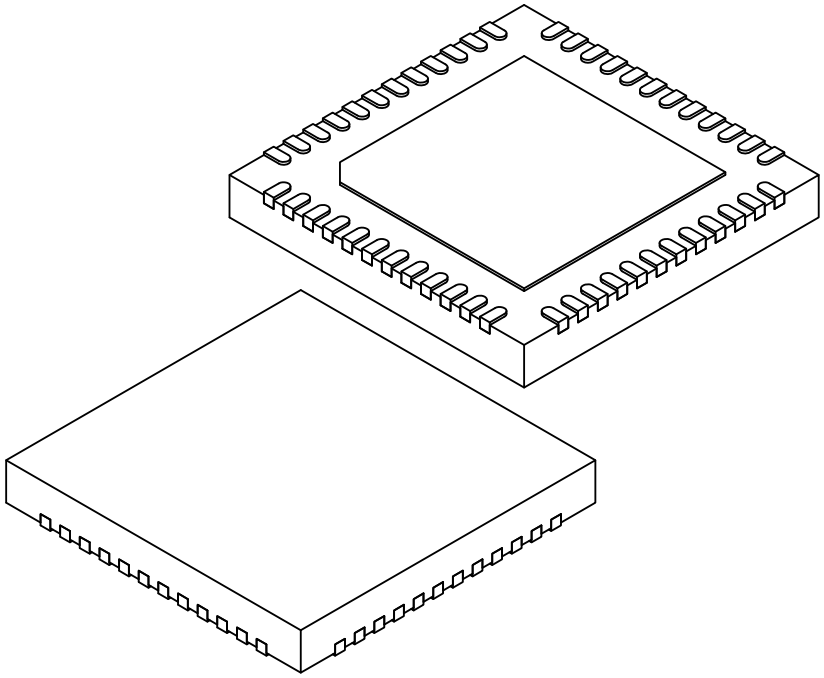
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-494 Rev A Sheet 1 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (6LX) - 6x6 mm Body [VQFN] With 4.1x4.1 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.00	4.10	4.20
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.00	4.10	4.20
Exposed Pad Corner Chamfer	CH		0.35 REF	
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.55 REF	

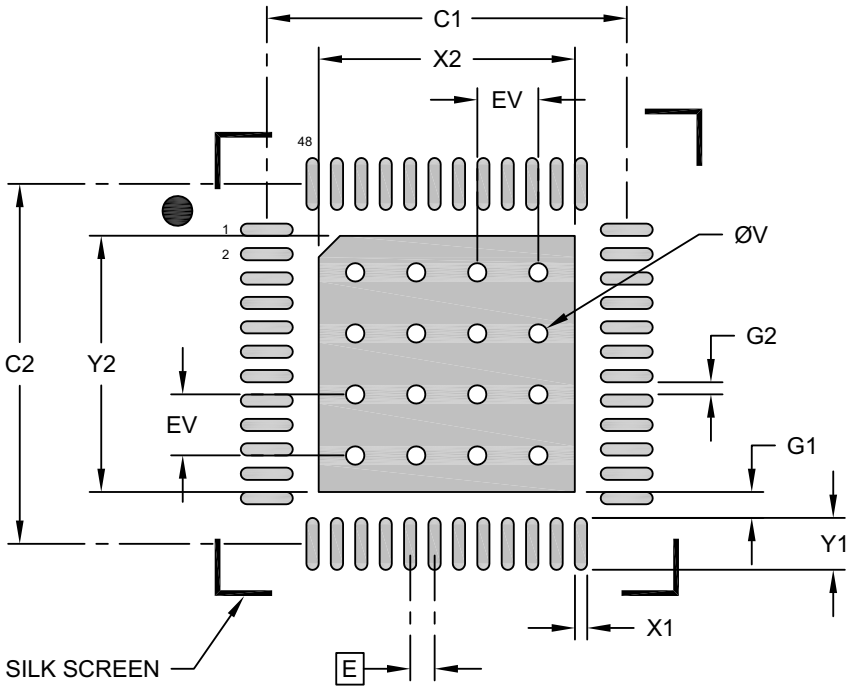
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-494 Rev A Sheet 1 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead (6LX) - 6x6 mm Body [VQFN] With 4.1x4.1 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			4.20
Optional Center Pad Length	Y2			4.20
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (X48)	X1			0.20
Contact Pad Length (X48)	Y1			0.85
Contact Pad to Center Pad (X48)	G1	0.20		
Contact Pad to Contact Pad (X44)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

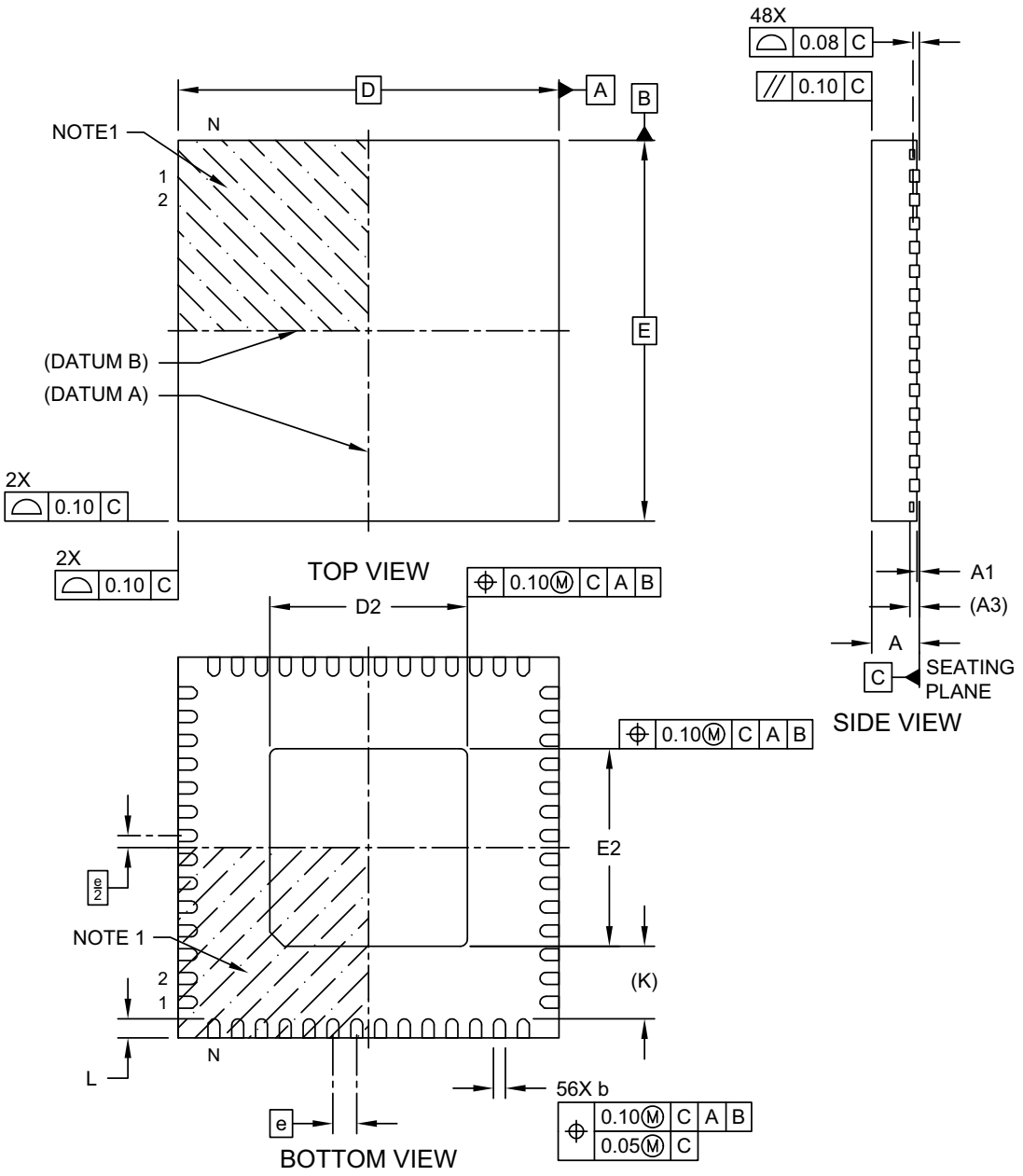
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2494 Rev A

56-Lead VQFN 8 mm x 8 mm Package Outline and Recommended Land Pattern

56-Lead Very Thin Plastic Quad Flat, No Lead Package (K3C) - 8x8x1.0 mm Body [VQFN] With 4.15 mm Exposed Pad

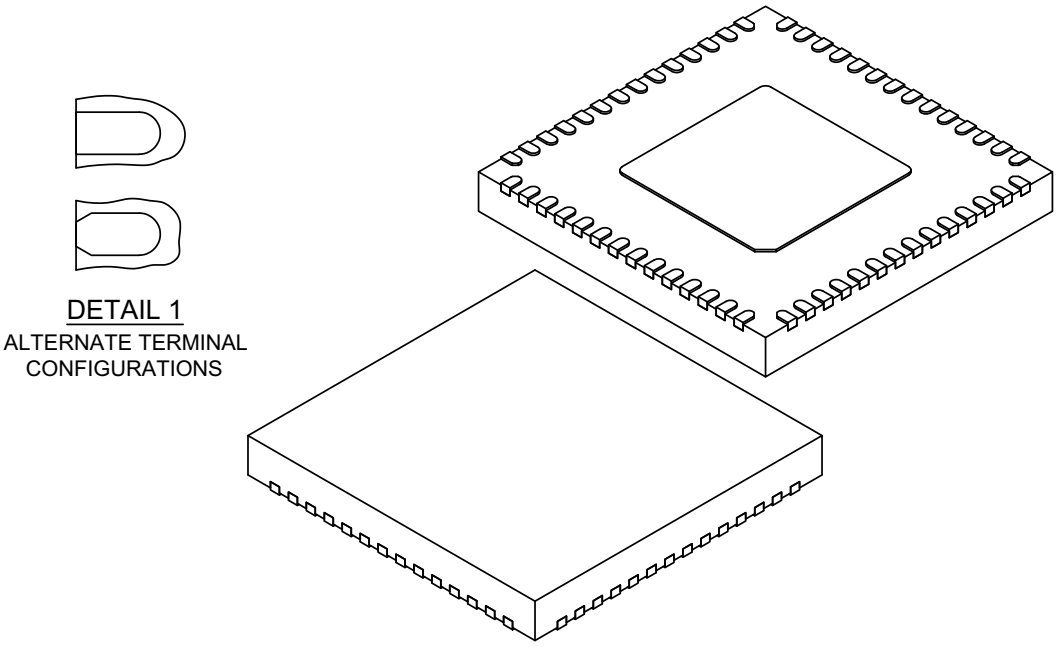
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25665 Rev A Sheet 1 of 2

56-Lead Very Thin Plastic Quad Flat, No Lead Package (K3C) - 8x8x1.0 mm Body [VQFN] With 4.15 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		56	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	4.05	4.15	4.25
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	4.05	4.15	4.25
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		1.53 REF	

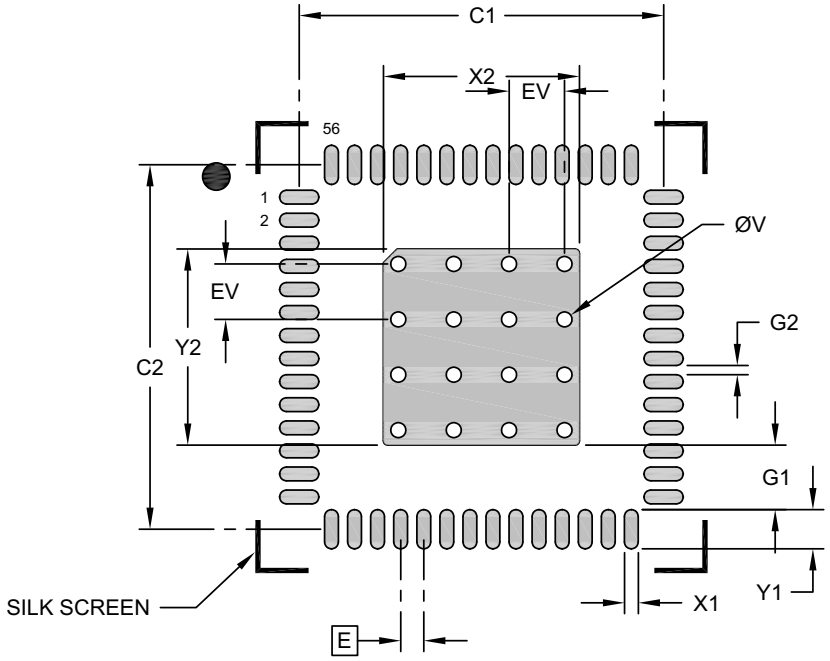
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25665 Rev A Sheet 2 of 2

56-Lead Very Thin Plastic Quad Flat, No Lead Package (K3C) - 8x8x1.0 mm Body [VQFN] With 4.15 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			4.25
Optional Center Pad Length	Y2			4.25
Contact Pad Spacing	C1		7.90	
Contact Pad Spacing	C2		7.90	
Contact Pad Width (X56)	X1			0.30
Contact Pad Length (X56)	Y1			0.85
Contact Pad to Center Pad (X56)	G1	0.85		
Contact Pad to Contact Pad (X52)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27665 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2021)

- Initial release of SY75608/612 as Microchip data sheet DS20006363A.

Revision B (August 2022)

- Replaced 48-lead VQFN (6MX) package outline drawing with 48-lead VQFN (6LX) package outline drawing.
- Replaced 56-lead VQFN (MEC) package outline drawing with 56-lead VQFN (K3C) package outline drawing.
- Updated the Product Identification System section to remove Wettable Flank from both package options.
- Updated the Package Marking Information drawing.
- Updated values for Output Enable and Disable Time in the Output Electrical Characteristics table.
- Updated max value for Input Leakage Current for OE Inputs in the Electrical Characteristics table.

Revision C (January 2023)

- Update values in the Electrical Characteristics, Crystal Oscillator Characteristics, Output Electrical Characteristics, and Jitter and Phase Noise tables.
- Added I2C Bus Electrical Characteristics table.
- Removed Preliminary from the footer.
- Added content relevant to PCIe Gen 6.0 throughout document.

Revision D (October 2023)

- Updated Silicon Revision Number in Table 6-2 to “0010”.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	XXX	[-XX]
Device	Package	Media Type

Device:	SY75608:	8 Output Ultra-Low Additive Jitter PCIe Gen1/2/3/4/5/6 Clock Buffer
	SY75612:	12 Output Ultra-Low Additive Jitter PCIe Gen1/2/3/4/5/6 Clock Buffer
Package:	TWL =	48-Lead 6 mm x 6 mm VQFN
	TWL =	56-Lead 8 mm x 8 mm VQFN
Media Type:	<blank>=	490/Tray (SY75608 Only)
	<blank>=	260/Tray (SY75612 Only)
	TR =	3,000/Reel (SY75612 Only)
	TR =	3,300/Reel (SY75608 Only)

Examples:

a) SY75608TWL: 8 Output Ultra-Low Additive Jitter PCIe Gen1/2/3/4/5/6 Clock Buffer, 48-Lead 6 mm x 6 mm VQFN, 490/Tray

b) SY75608TWL-TR: 8 Output Ultra-Low Additive Jitter PCIe Gen1/2/3/4/5/6 Clock Buffer, 48-Lead 6 mm x 6 mm VQFN, 3,300/Reel

c) SY75612TWL: 12 Output Ultra-Low Additive Jitter PCIe Gen1/2/3/4/5/6 Clock Buffer, 56-Lead 8 mm x 8 mm VQFN, 260/Tray

d) SY75612TWL-TR: 12 Output Ultra-Low Additive Jitter PCIe Gen1/2/3/4/5/6 Clock Buffer, 56-Lead 8 mm x 8 mm VQFN, 3,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note: For customers ordering a customized configuration from the ClockWorks Configurator, the part number examples shown above will be appended by “GXXX” in which the “XXX” represents a numerical code assigned by Microchip (e.g., SY75608TWL-TRG0001).

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Trademarks

ISBN: 978-1-6683-3254-2

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

SY75608TWL SY75612TWL SY75612TWL-TR SY75608TWL-TR