SY58032U

Ultra-Precision 1:8 Fanout Buffer with LVPECL Outputs and Internal Termination (Precision Edge®)

Features

- Precision 1:8, LVPECL Fanout Buffer
- Guaranteed AC Performance Over Temperature and Voltage:
  - Clock Frequency Range: DC to 4 GHz
  - <110 ps t_r / t_f Times
  - <330 ps t_{pd}
  - <20 ps Skew
- Low-jitter Performance:
  - 76 fs_{RMS} Phase Jitter (typ)
- 100k LVPECL Compatible Outputs
- Fully Differential Inputs/Outputs
- Accepts an Input Signal as Low as 100 mV
- Unique Input Termination and VT Pin Accepts DC-coupled and AC-coupled Differential Inputs: (LVPECL, LVDS, and CML)
- Power Supply 2.5V ±5% or 3.3V ±10%
- Industrial Temperature Range: –40°C to +85°C
- Available in 32-lead (5 mm x 5 mm) VQFN Package

Applications

- All SONET and All GigE Clock Distribution
- All Fibre Channel Clock and Data Distribution
- Network Routing Engine Timing Distribution
- High-end, Low-skew Multiprocessor Synchronous Clock Distribution

Related Microchip Products

- SY58031U
- SY58033U

General Description

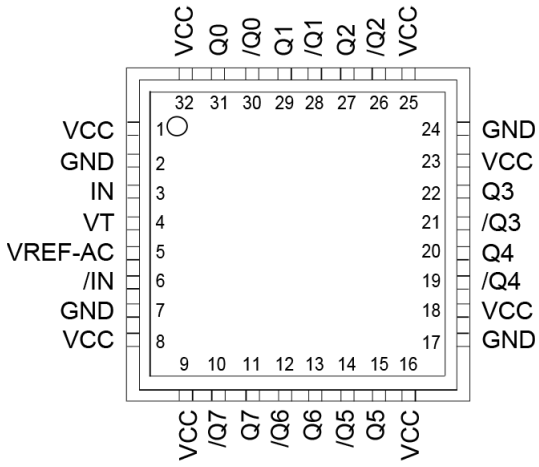
The SY58032U is a 2.5V/3.3V precision, high-speed, fully differential LVPECL 1:8 fanout buffer. The SY58032U is optimized to provide eight identical output copies with less than 20 ps of skew and only 76 fs_{RMS} phase jitter. It can process clock signals as fast as 4 GHz.

The differential input includes Microchip's unique 3-pin input termination architecture that allows the SY58032U to directly interface to LVPECL, CML, and LVDS differential signals (AC- or DC-coupled) without any level-shifting or termination resistor networks in the signal path. The result is a clean, stub-free, low-jitter interface solution. The LVPECL (100k temperature compensated) outputs feature 800 mV typical swing into 50Ω loads, and provide an extremely fast rise/fall time guaranteed to be less than 110 ps.

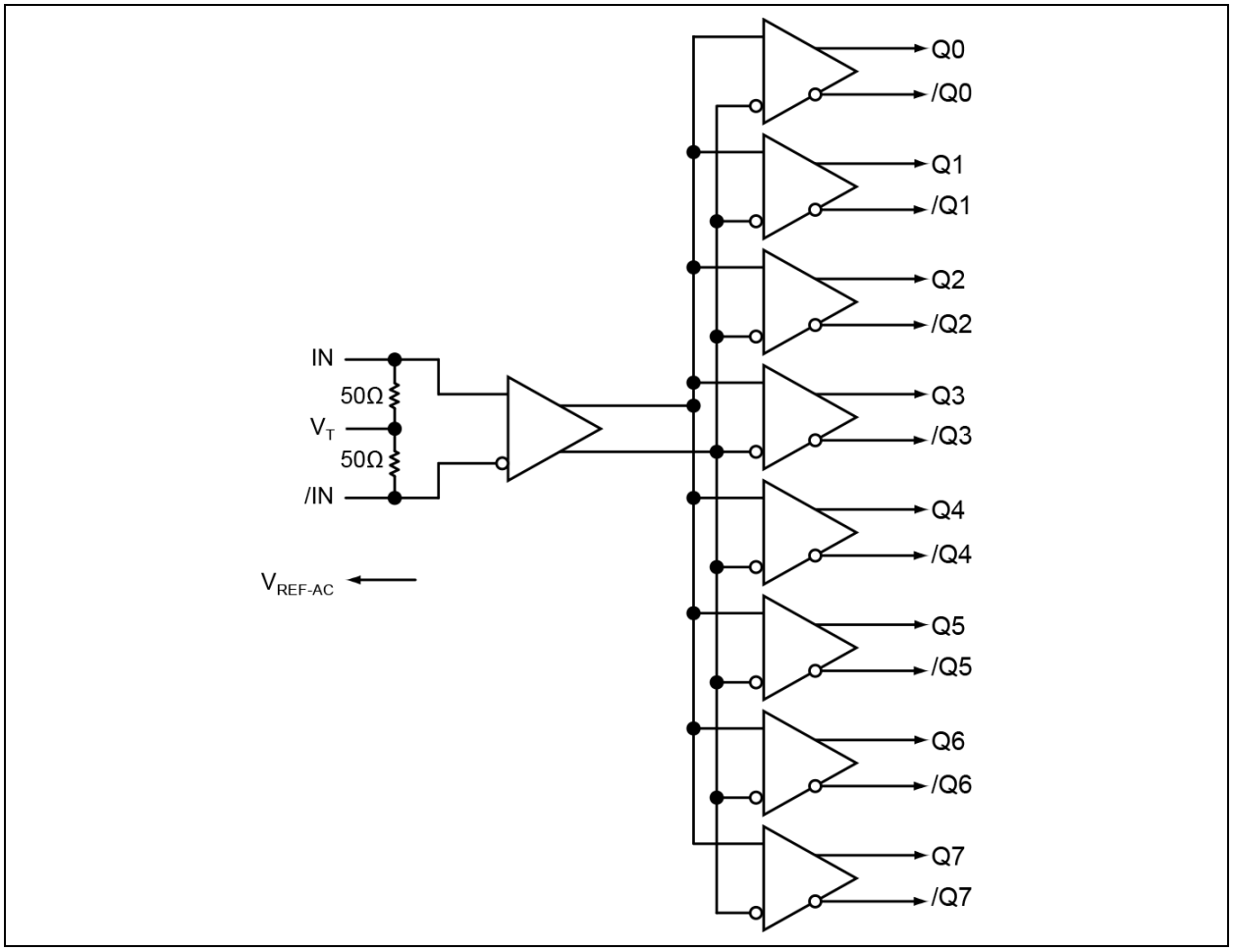
The SY58032U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require a higher high-speed 1:8 fanout buffer, consider the SY58031U or SY58033U. The SY58032U is part of Microchip's high-speed, Precision Edge® product line.

Package Type

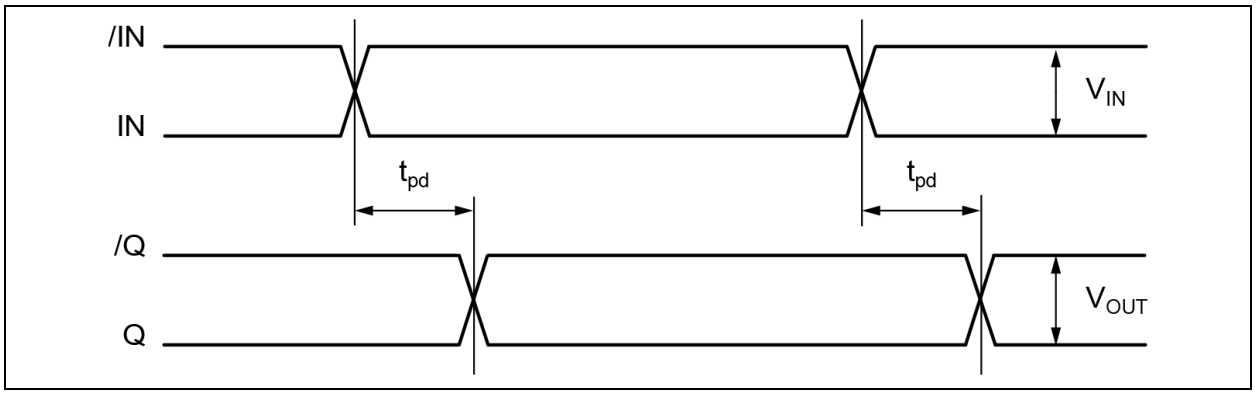
SY58032U
32-Lead VQFN



Functional Block Diagram



Timing Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
Current (V_T), Source or sink current on VT pin ..... ±100 mA
Input Current (V_T), Source or sink current on IN, /IN ..... ±50 mA
Current (V_{REF}), Source or sink current on V_{REF-AC} (Note 1) ..... ±1.5 mA

Operating Ratings††

Power Supply Voltage (V_{CC}) ..... +2.375V to +3.60V
Ambient Temperature Range (T_A) ..... –40°C to +85°C

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

All values applicable for when T_A = –40°C to +85°C unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply Voltage	V_{CC}	2.375	2.5	2.625	V	2.5V nominal
		3.0	3.3	3.6		3.3V nominal
Power Supply Current	I_{CC}	—	190	250	mA	V_{CC} = max. No load. Includes current through 50Ω pull-ups.
Input HIGH Voltage	V_{IH}	V_{CC} – 1.6	—	V_{CC}	V	IN, /IN, see Note 2.
Input LOW Voltage	V_{IL}	0	—	V_{IH} – 0.1	V	IN, /IN
Input Voltage Swing	V_{IN}	0.1	—	1.7	V	IN, /IN, see Figure 6-1.
Differential Input Voltage Swing |IN0, /IN0|, |IN1, /IN1|	V_{DIFF_IN}	0.2	—	—	V	IN, /IN, see Figure 6-2.
In-to-V_T Resistance	R_{IN}	40	50	60	Ω	—
Max. In-to-V_T (IN, /IN)	V_{T_IN}	—	—	1.28	V	—
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V	—

Note 1: The circuit is designed to meet the DC specifications shown in this table after thermal equilibrium has been established.

2: V_{IH} (min) not lower than 1.2V.

TABLE 1-2: LVPECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to +85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output HIGH Voltage	V_{OH}	V_{CC} – 1.145	—	V_{CC} – 0.895	V	—
Output LOW Voltage	V_{OL}	V_{CC} – 1.945	—	V_{CC} – 1.695	V	—
Output Voltage Swing	V_{OUT}	500	800	—	mV	See Figure 6-1
Differential Voltage Swing	V_{DIFF_OUT}	1000	1600	2000	mV	See Figure 6-2

Note 1: The circuit is designed to meet the DC specifications shown in this table after thermal equilibrium has been established.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to + 85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Frequency (Clock)	f_{MAX}	4	—	—	GHz	V_{OUT} ≥ 400 mV
Propagation Delay (IN-to-Q)	t_{pd}	180	260	330	ps	—
Differential Propagation Delay Temperature Coefficient	t_{pd_tempco}	—	35	—	fs/°C	—
Output-to-Output Skew (Within Device)	t_{SKEW}	—	7	20	ps	See Note 2.
Part-to-Part Skew		—	—	100	ps	See Note 3.
RMS Phase Jitter	t_{JITTER}	—	76	—	fs	Output = 622 MHz, Integration Range 12 kHz–20 MHz.
Output Rise/Fall Times (20% to 80%)	t_r, t_f	35	75	110	ps	At full output swing

Note 1: High-frequency AC parameters are guaranteed by design and characterization. All outputs loaded with 50Ω to V_{CC} – 2V, V_{IN} ≥ 100 mV.

2: Output-to-output skew is measured between outputs under identical transitions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Part-to-part skew includes variation in t_{pd}.

TABLE 1-4: TEMPERATURE SPECIFICATIONS

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Range						
Operating Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance (Note 1)						
32-Lead VQFN, Still Air	θ_{JA}	—	+35	—	°C/W	—
32-Lead VQFN, Junction-to-Board	Ψ_{JB}	—	+20	—	°C/W	—

Note 1: Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. The Ψ_{JB} and θ_{JA} values are determined for a 4-layer board at the still-air package thermal resistance, unless otherwise stated.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
3, 6	IN, /IN	Differential Signal Input: Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See “Input Interface Applications” section.
4	VT	Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See “Input Interface Applications” section.
2, 7, 17, 24	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
1, 8, 9, 16, 18, 23, 25, 32	VCC	Positive Power Supply: Bypass with 0.1µF||0.01µF low ESR capacitors as close to the pins as possible.
31, 30, 29, 28, 27, 26, 22, 21, 20, 19, 15, 14, 13, 12, 11, 10	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3, Q4, /Q4, Q5, /Q5, Q6, /Q6, Q7, /Q7	100k LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The LVPECL output swing is typically 800mV into 50Ω. Unused output pairs may be left floating with no impact on jitter. See “LVPECL Output” section.
5	VREF-AC	Bias Reference Voltage: Equal to VCC–1.2V (typical), and used for AC-coupled applications. See “Input Interface Applications” section. When using VREF-AC, bypass with 0.01µF capacitor to VCC. Maximum sink/source current is 0.5mA.

3.0 TYPICAL PHASE NOISE

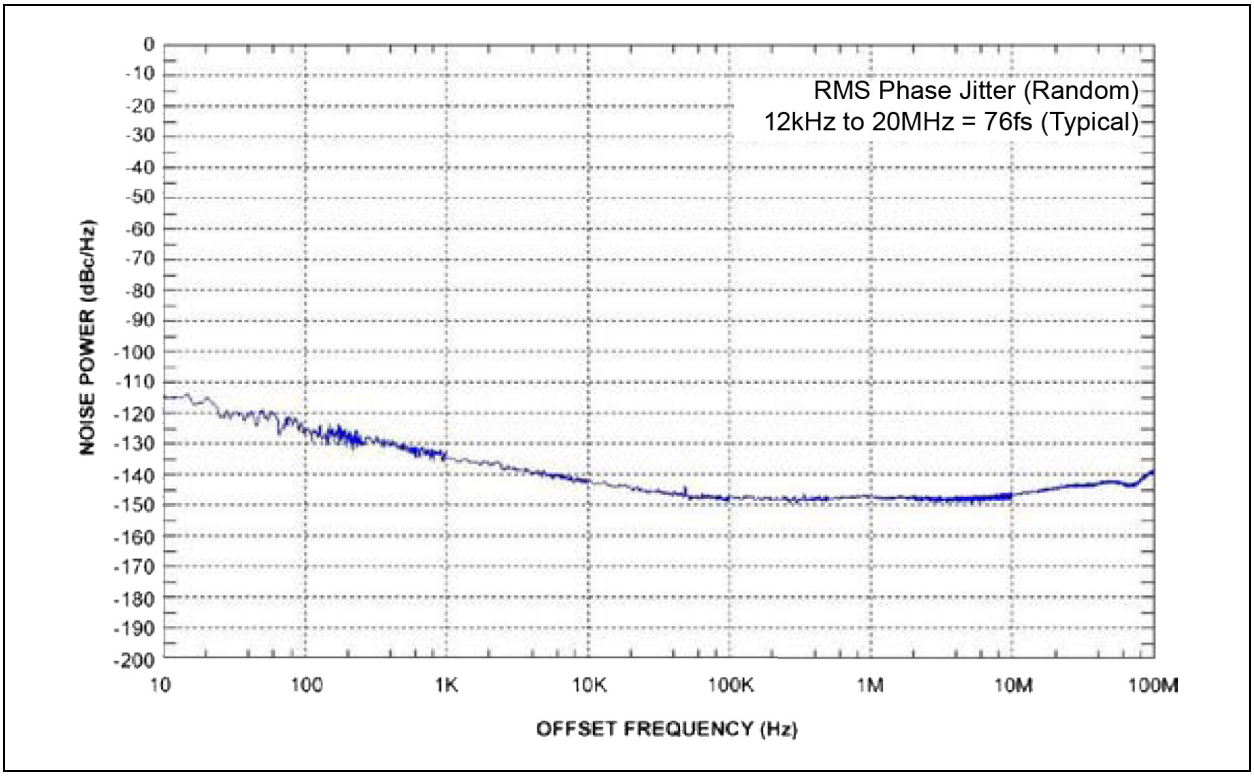


FIGURE 3-1: SY58032U PHASE NOISE PLOT: 622 MHZ @ 3.3V.

4.0 TYPICAL CHARACTERISTICS

V_{CC} = 2.5V; GND = 0V; V_{IN} = 100 mV, T_A = 25°C, unless otherwise noted.

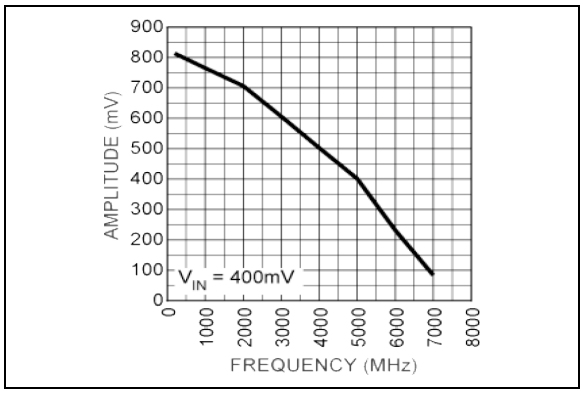


FIGURE 4-1: AMPLITUDE VS. FREQUENCY.

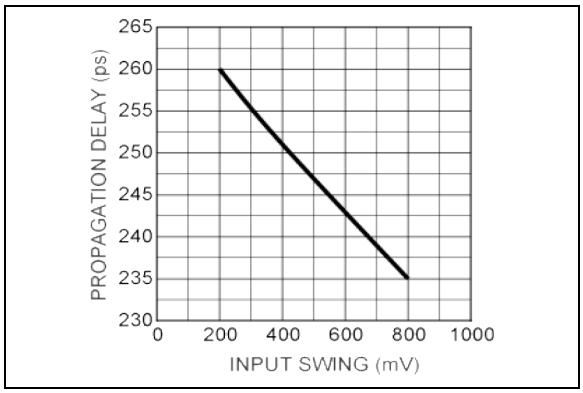


FIGURE 4-3: PROPAGATION DELAY VS. INPUT SWING.

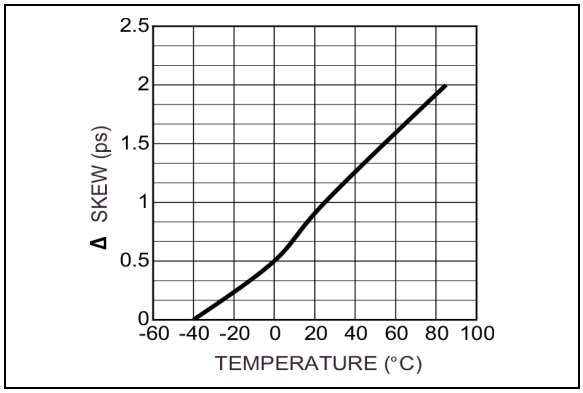


FIGURE 4-2: Δ OUTPUT-TO-OUTPUT SKEW VS. TEMPERATURE.

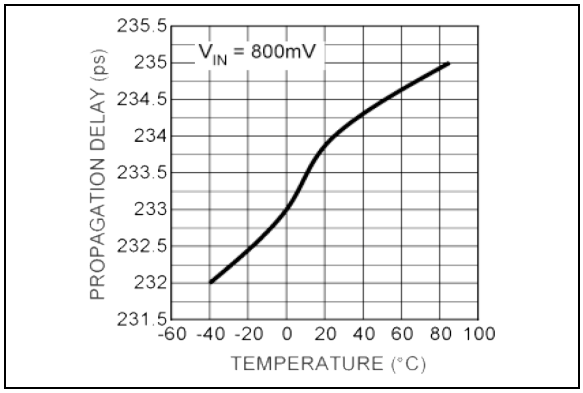


FIGURE 4-4: PROPAGATION DELAY VS. TEMPERATURE.

5.0 TYPICAL OUTPUT WAVEFORMS

V_{CC} = 2.5V; GND = 0V; V_{IN} = 100 mV, T_A = 25°C, unless otherwise noted.

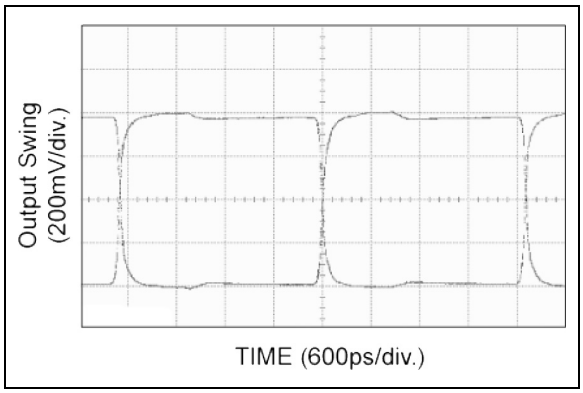


FIGURE 5-1: 200 MHZ OUTPUT.

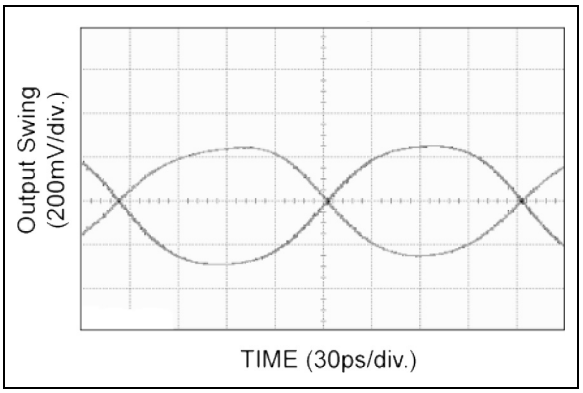


FIGURE 5-3: 4 GHZ OUTPUT.

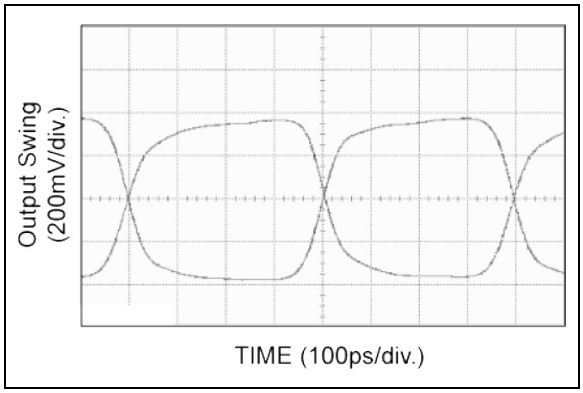


FIGURE 5-2: 1.25 GHZ OUTPUT.

6.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

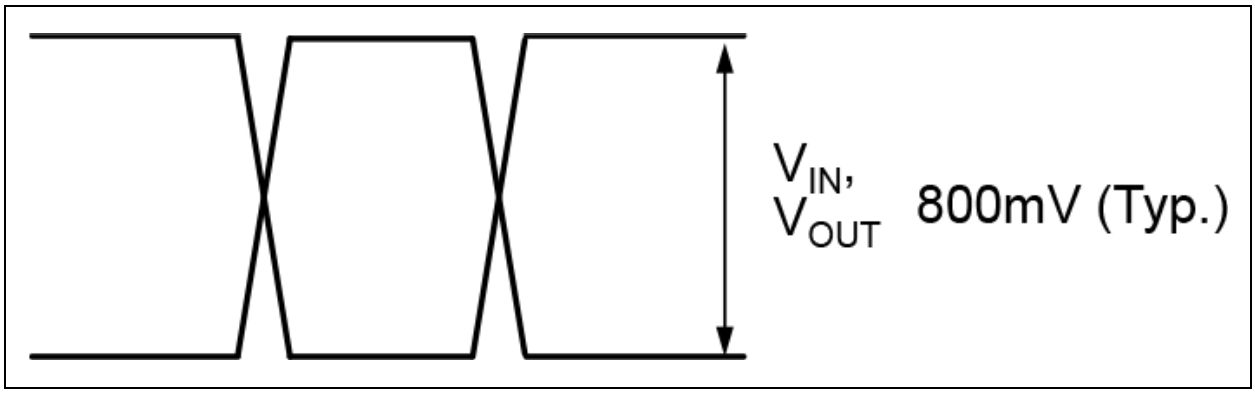


FIGURE 6-1: SINGLE-ENDED VOLTAGE SWING.

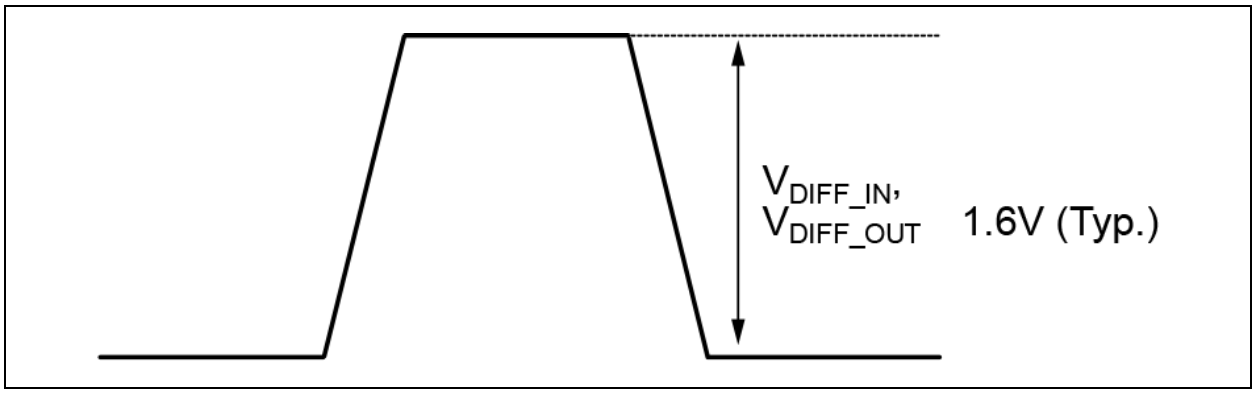


FIGURE 6-2: DIFFERENTIAL VOLTAGE SWING.

7.0 INPUT BUFFER

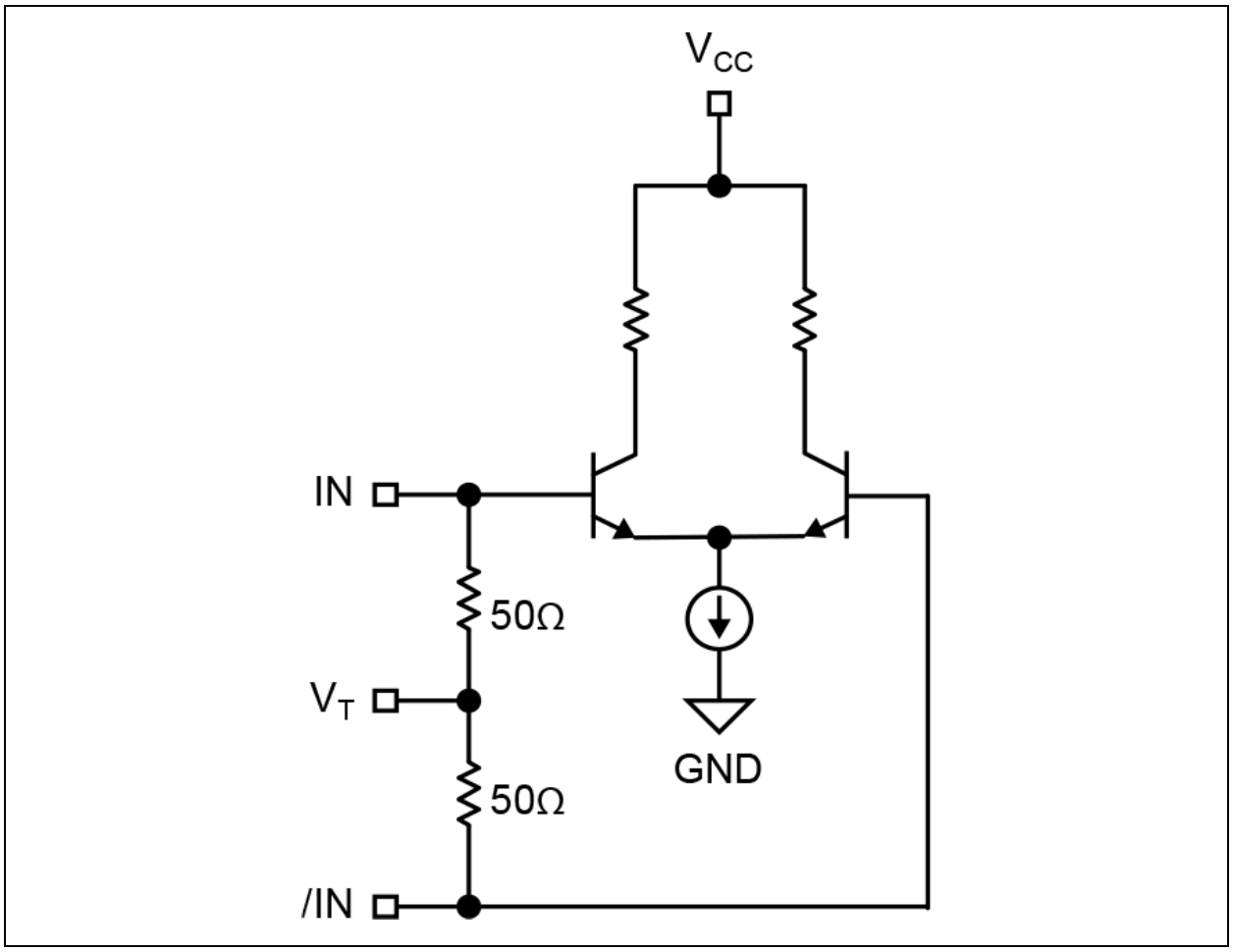


FIGURE 7-1: SIMPLIFIED DIFFERENTIAL INPUT BUFFER.

8.0 INPUT INTERFACE APPLICATIONS

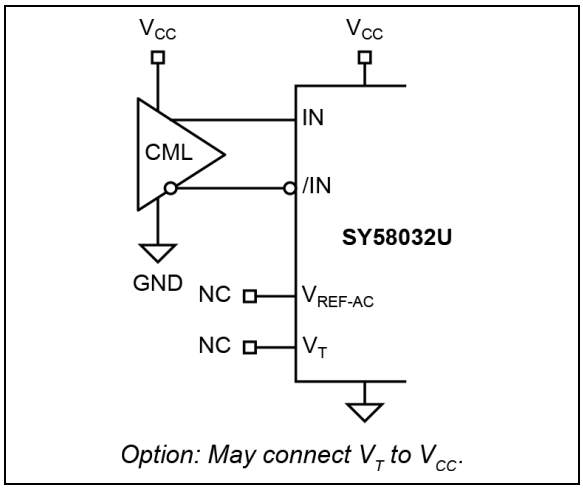


FIGURE 8-1: DC-COUPLED CML INPUT INTERFACE.

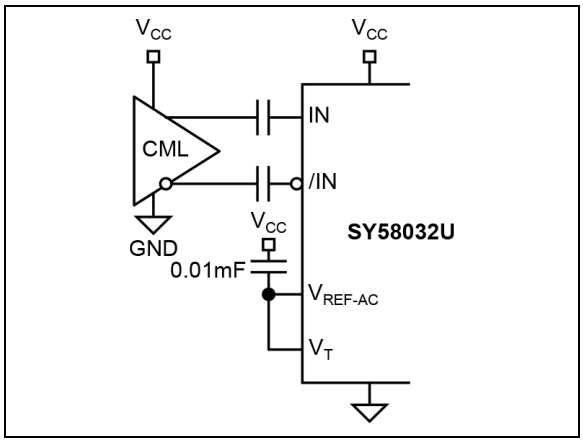


FIGURE 8-2: AC-COUPLED CML INPUT INTERFACE.

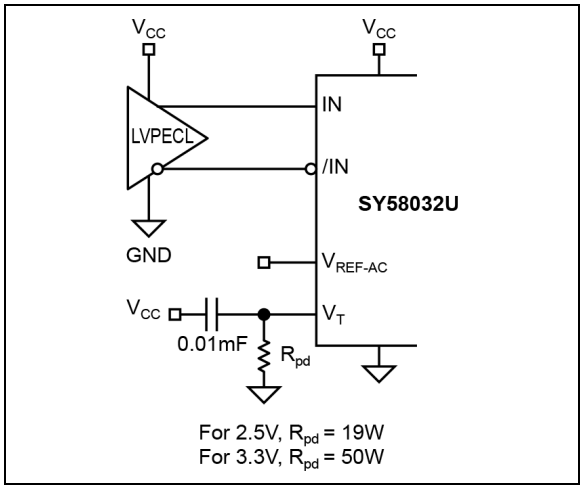


FIGURE 8-3: LVPECL INPUT INTERFACE.

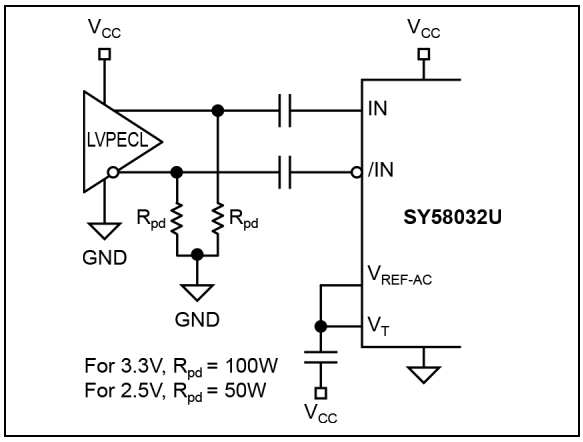


FIGURE 8-4: AC-COUPLED LVPECL INPUT INTERFACE.

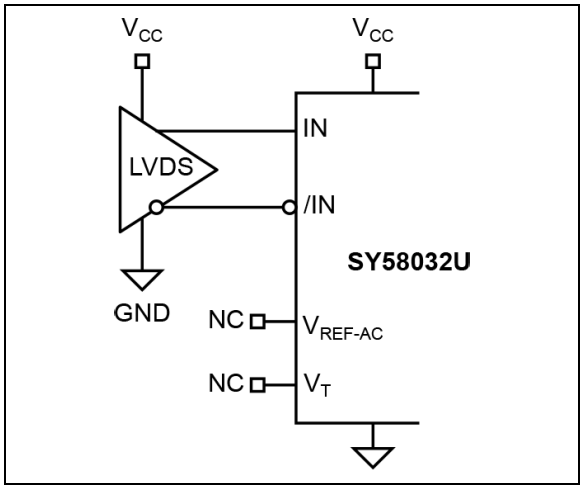


FIGURE 8-5: LVDS INPUT INTERFACE.

9.0 OUTPUT TERMINATION RECOMMENDATIONS

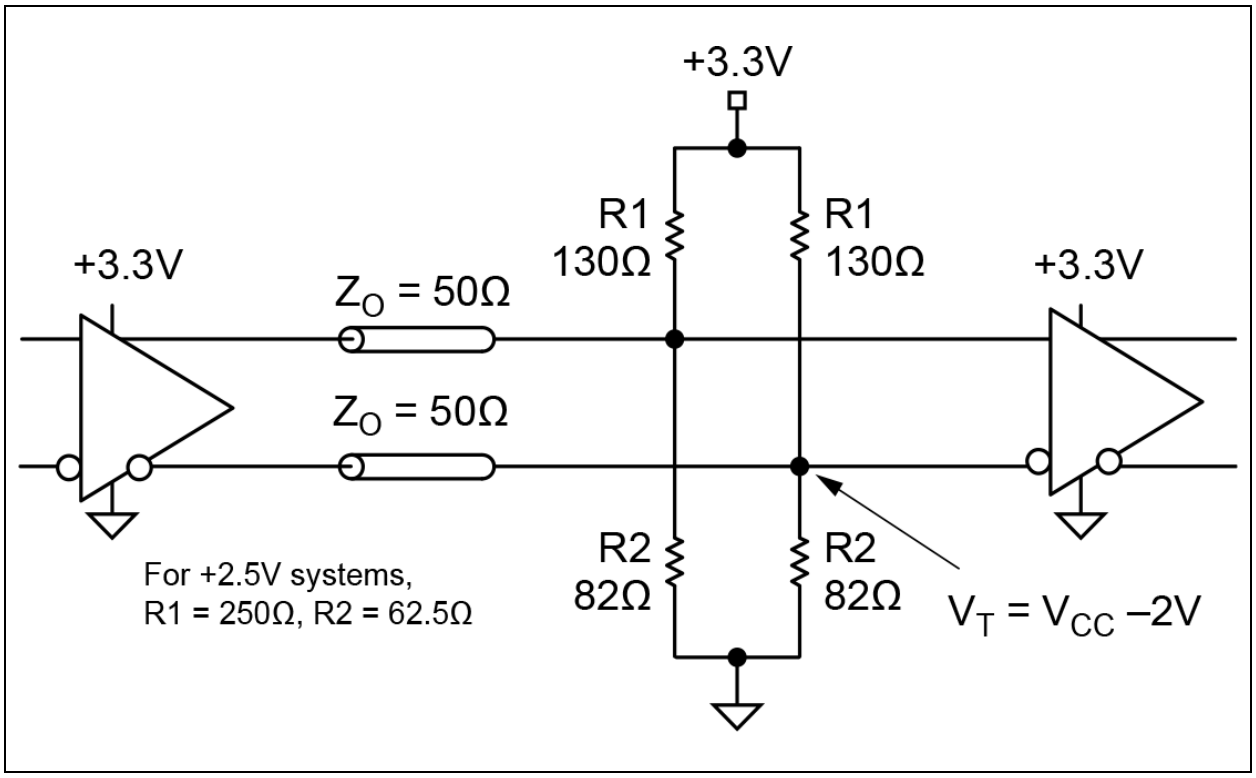


FIGURE 9-1: PARALLEL TERMINATION – THEVENIN EQUIVALENT.

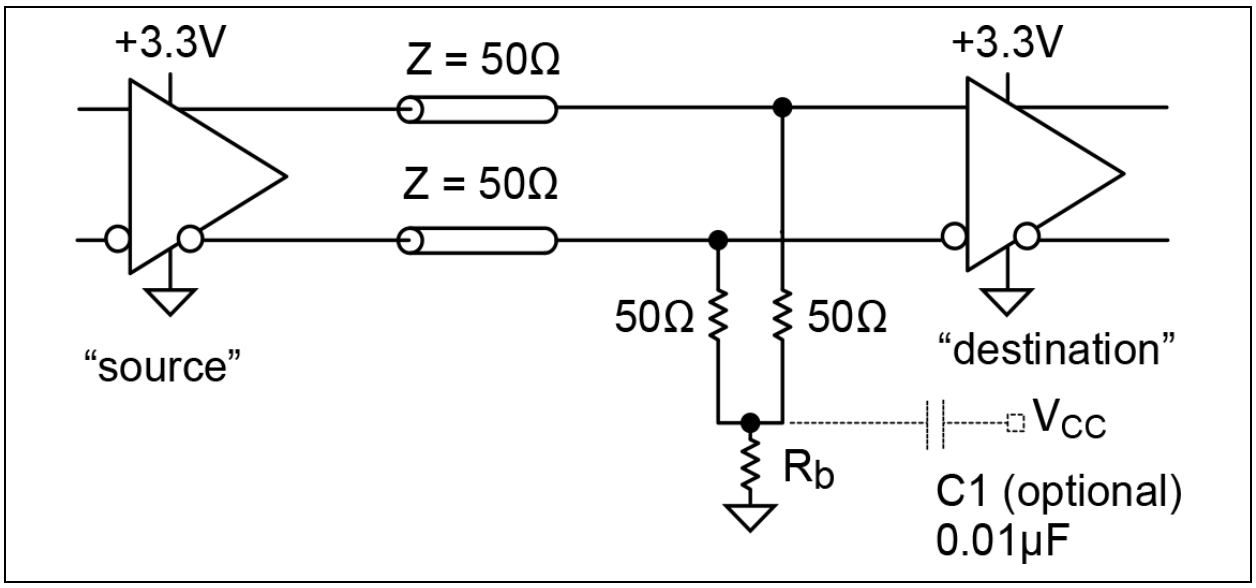


FIGURE 9-2: PARALLEL TERMINATION (3-RESISTOR).

Note 1: Power-saving alternative to Thevenin termination.

2: Place termination resistors as close to destination inputs as possible.

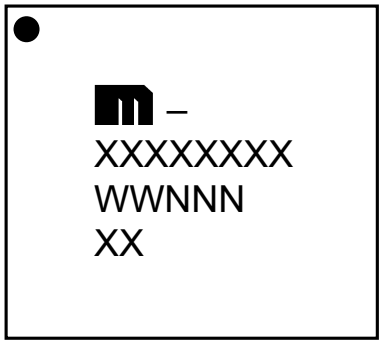
3: R_b resistor sets the DC bias voltage, equal to VT.

4: For 2.5V systems, R_b = 19Ω. For 3.3V systems, R_b = 50Ω

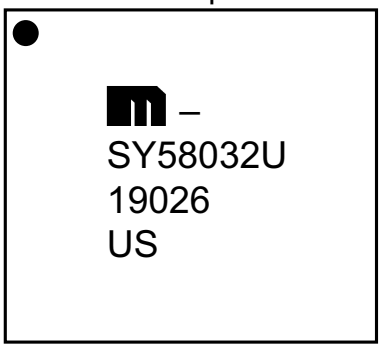
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

32-Lead VQFN*



Example*



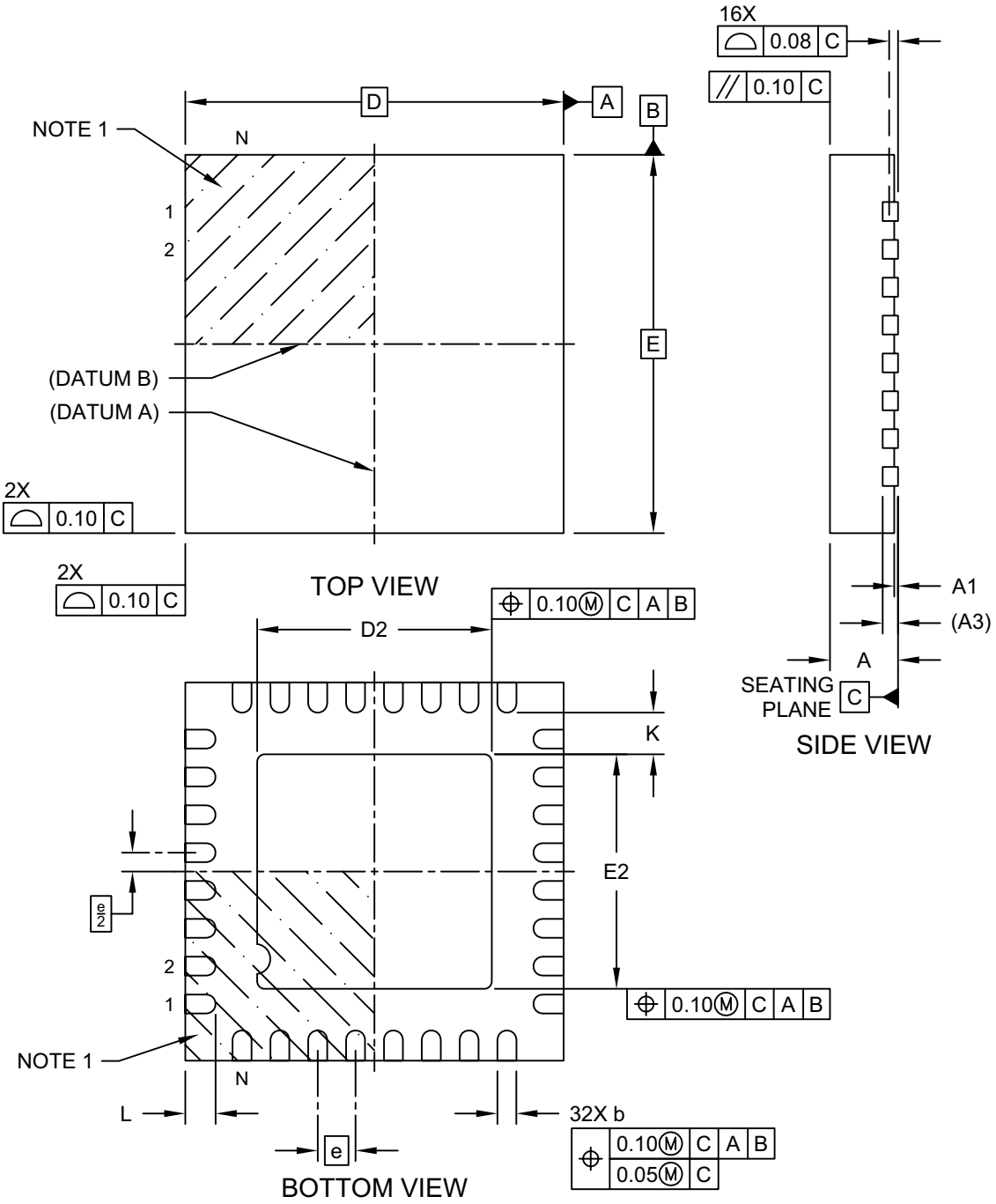
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

32-Lead 5 mm × 5 mm VQFN [PEA] Package Outline and Recommended Land Pattern

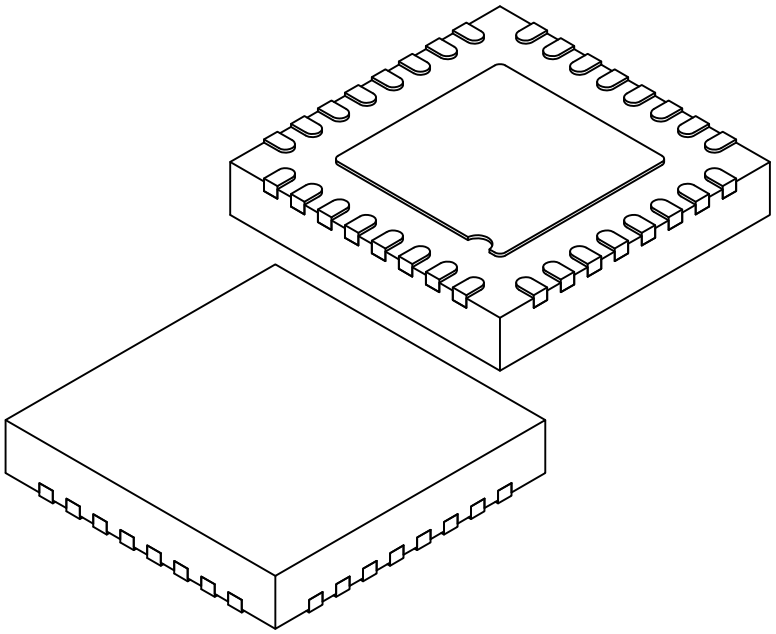
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1118-PEA Rev A Sheet 1 of 2

32-Lead 5 mm × 5 mm VQFN [PEA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.05	3.10	3.15
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.05	3.10	3.15
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

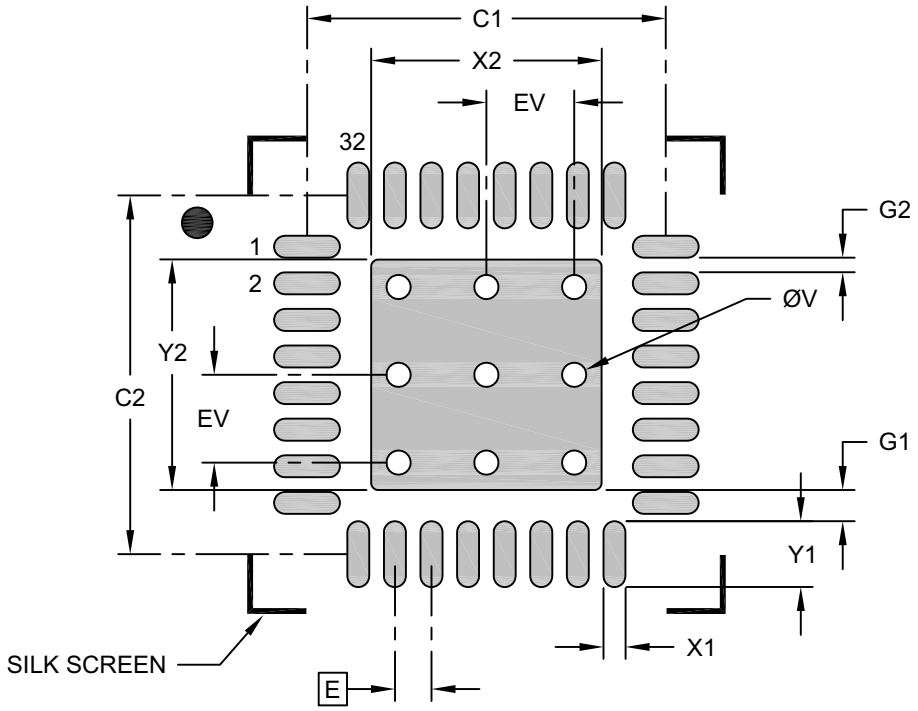
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1118-PEA Rev A Sheet 2 of 2

32-Lead 5 mm × 5 mm VQFN [PEA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.15
Optional Center Pad Length	Y2			3.15
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.90
Contact Pad to Center Pad (Xnn)	G1	0.43		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3118-PEA Rev A

APPENDIX A: REVISION HISTORY

Revision A (May 2024)

- Converted Micrel data sheet for SY58032U to Microchip format as DS20006845A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY58032	=	Ultra-Precision 1:8 Fanout Buffer with LVPECL Outputs and Internal Termination (Precision Edge®)
Voltage Option:	U	=	2.5V/3.3V
Package:	M	=	32-Lead VQFN
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	60/Tube
	TR	=	1,000/Reel

Examples:

a) **SY58032UMG**

2.5V/3.3V, 32-Lead VQFN, –40°C to 85°C, 60/Tube

b) **SY58032UMG-TR**

2.5V/3.3V, 32-Lead VQFN, –40°C to 85°C, 1,000/Reel

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
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