MICROCHIP

SY55857L

3.3V, 2.5 Gbps Any Input-to-LVPECL Dual Translator

Features

- Input Accepts Virtually All Logic Standards:
  - Single-Ended: SSTL, TTL, CMOS
  - Differential: LVDS, HSTL, CML
- Ensured AC Parameters over Temperature:
  - f_{MAX} > 2.5 Gbps (2.5 GHz Toggle)
  - t_r/t_f < 200 ps
  - Within-Device Skew < 50 ps
  - Propagation Delay < 400 ps
- Low Power: 46 mV/Channel (Typ.)
- 3.0V to 3.6V Power Supply
- 100K LVPECL Outputs
- Flow-Through Pinout and Fully Differential Design
- Two Channels in a 10-Lead (3 mm x 3 mm) MSOP Package

Applications

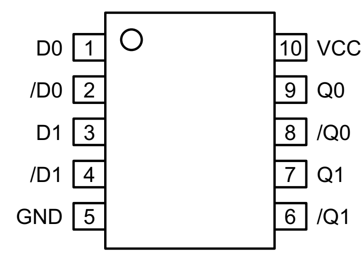
- High-Speed Logic
- Data Communication Systems
- Wireless Communication Systems
- Telecom Systems

General Description

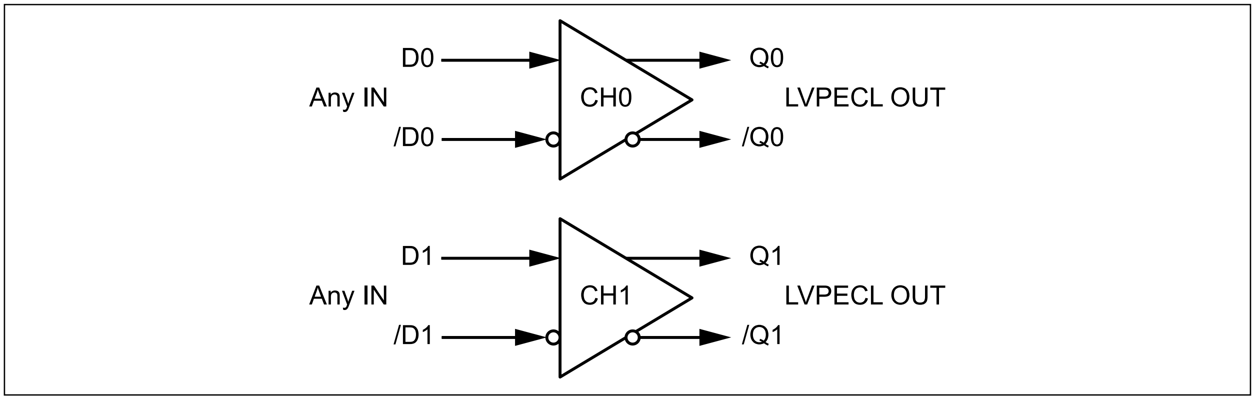
The SY55857L is a fully differential, high-speed dual translator optimized to accept any logic standard from single-ended TTL/CMOS to differential LVDS, HSTL, or CML and translate it to LVPECL. Translation is ensured for speeds up to 2.5 Gbps (2.5 GHz toggle frequency). The SY55857L does not internally terminate its inputs, as different interfacing standards have different termination requirements.

Package Type

SY55857L
10-Lead MSOP (K)
(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage (V_{CC}) .... –0.5V to +6.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC} + 0.5V
Continuous Output Current (I_{OUT}) .... 50 mA
Surge Output Current (I_{OUT}) .... 100 mA

Operating Ratings ‡

Power Supply Voltage (V_{CC}) .... +3.0V to +3.6V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	—
Power Supply Current	I_{CC}	—	28	45	mA	Inputs/outputs open

Note 1: The specifications shown are valid after thermal equilibrium has been established.

INPUT ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V to +3.6V; GND = 0V; T_A = –40°C to +85°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Voltage Swing	V_{ID}	100	—	—	mV	See Figure 1-1, V_{IN} < 2.4V
		200	—	—	mV	V_{IN} < V_{CC} + 0.3V
Input High Voltage	V_{IH}	—	—	V_{CC} + 0.3V	V	—
Input Low Voltage	V_{IL}	–0.3	—	—	V	—

Note 1: The specifications shown are valid after thermal equilibrium has been established.

100K LVPECL OUTPUT CHARACTERISTICS

V_{CC} = +3.0V to +3.6V; GND = 0V; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC} – 2V, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Low Voltage Q, /Q	V_{OL}	V_{CC} – 1.945	V_{CC} – 1.820	V_{CC} – 1.695	V	—
Output High Voltage Q, /Q	V_{OH}	V_{CC} – 1.145	V_{CC} – 1.020	V_{CC} – 0.895	V	—
Output Voltage Swing Q, /Q	V_{OUT}	550	800	—	mV	See Figure 1-1
Differential Output Voltage Swing Q, /Q	V_{DIFF_OUT}	1100	1600	—	mV_{PP}	See Figure 1-2

Note 1: 100K circuits are designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

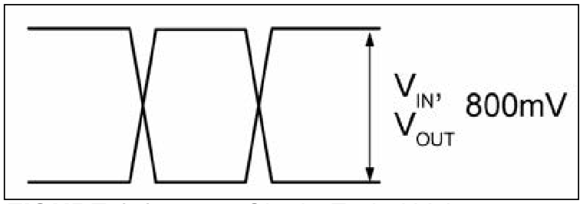


FIGURE 1-1: Single-Ended Voltage Swing.

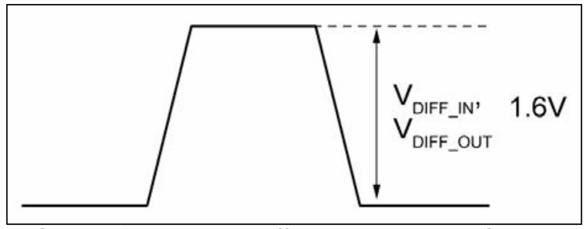


FIGURE 1-2: Differential Voltage Swing.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency (Note 1)	f_{MAX}	2.5	—	—	Gbps	V_{IN} < 2.4V, NRZ Data
		2.5	—	—	GHz	V_{IN} < 2.4V, Clock
		1.25	—	—	Gbps	V_{IN} < V_{CC} + 0.3V, NRZ Data
		1.25	—	—	GHz	V_{IN} < V_{CC} + 0.3V, Clock
Propagation Delay (D-to-Q)	t_{PD}	—	—	400	ps	—
Within-Device Skew (Diff.)	t_{SKEW}	—	—	50	ps	Note 2
Part-to-Part Skew (Diff.)		—	—	200	ps	Note 3
Random Jitter (RJ)	t_{JITTER}	—	—	1	ps_{RMS}	Note 4
Deterministic Jitter (DJ)		—	—	10	ps_{PP}	Note 5
Total Jitter (TJ)		—	1	10	ps_{PP}	Note 6
Output Rise/Fall Time, 20% to 80%	t_r/t_f	—	—	200	ps	At full output swing.

Note 1: Clock frequency is defined as the maximum toggle frequency, and ensured for functionality only. Measured with a 750 mV signal, 50% duty cycle and V_{OUT} swing ≥ 400 mV. High-frequency AC parameters are ensured by design and characterization.

2: Within-device skew is measured between two different outputs under identical transitions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

4: Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5 Gbps.

5: Deterministic jitter is measured at 2.5 Gbps with both K28.5 and 2^{23}–1 PRBS pattern.

6: Total jitter definition: with an ideal differential clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, MSOP 10-Ld	θ_{JA}	—	113	—	°C/W	Still-Air
	θ_{JA}	—	96	—	°C/W	500 lpfm
	θ_{JC}	—	42	—	°C/W	Junction-to-case

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. θ_{JC} uses 4-layer θ_{JA} in a still air environment, unless otherwise stated.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2	D0, /D0	Channel 0 Differential Inputs (clock or data). See Figure 3-1 for input structure. See the Input Interface section for typical interface recommendations.
3, 4	D1, /D1	Channel 1 Differential Inputs (clock or data). See Figure 3-1 for input structure. See the Input Interface section for typical interface recommendations.
9, 8	Q0, /Q0	Channel 0 Differential 100K-compatible LVPECL Outputs. Terminate to V_{CC} – 2V. See the LVPECL Output Termination section. Outputs are low impedance, emitter-followers. For AC-coupled applications, a pull-down resistor is required on Q and /Q to ensure a DC current path to GND.
7, 6	Q1, /Q1	Channel 1 Differential 100K-compatible LVPECL Outputs. Terminate to V_{CC} – 2V. See the LVPECL Output Termination section. Outputs are low impedance, emitter-followers. For AC-coupled applications, a pull-down resistor is required on Q and /Q to ensure a DC current path to GND.
5	GND	Device Ground. Typically connected to Logic ground.
10	VCC	Supply Voltage. Typically connect to +3.3V ±10% supply. Bypass with 0.01 µF||0.1 µF low ESR capacitors.

3.0 FUNCTIONAL DESCRIPTION

3.1 Establishing Static Logic Inputs

Do not leave unused inputs floating. Tie either the true or complement inputs to ground, but not both. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a 2.5 kΩ resistor between the complement input and ground. See the Input Interface section.

3.2 Input Levels

LVDS, CML, and HSTL differential signals may be connected directly to the D inputs. Depending on the actual worst case voltage seen, performance of SY55857L varies as per the following table:

TABLE 3-1: INPUT VOLTAGE SWINGS

Input Voltage Range	Minimum Voltage Swing	Maximum Translation Speed
0V to 2.4V	100 mV	2.5 Gbps
0V to V_{CC} + 0.3V	200 mV	1.25 Gbps

For LVDS applications, only point-to-point interfaces are supported. Due to the current required by the input structure shown in Figure 3-1, multi-drop and multi-point architectures are not supported.

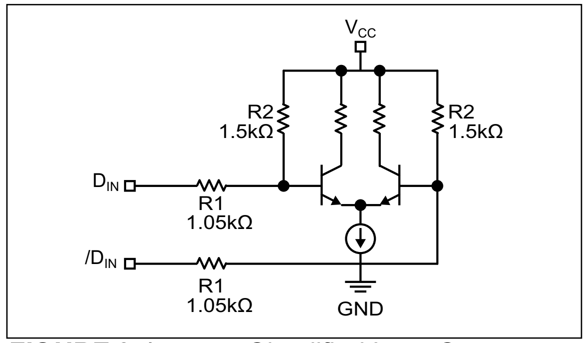


FIGURE 3-1: *Simplified Input Structure.*

4.0 INPUT INTERFACE

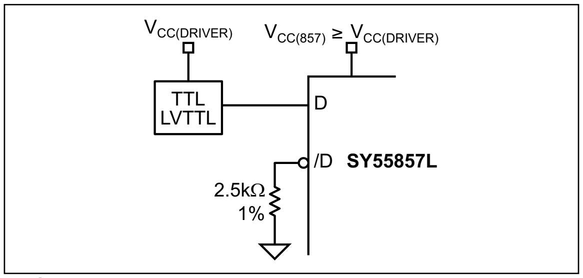


FIGURE 4-1: *3.3V TTL.*

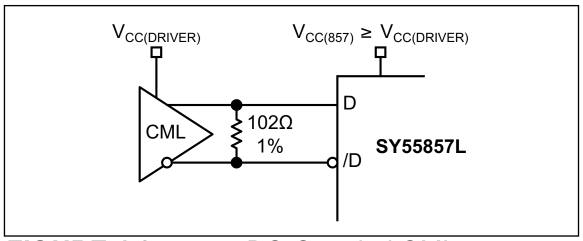


FIGURE 4-2: *DC-Coupled CML.*

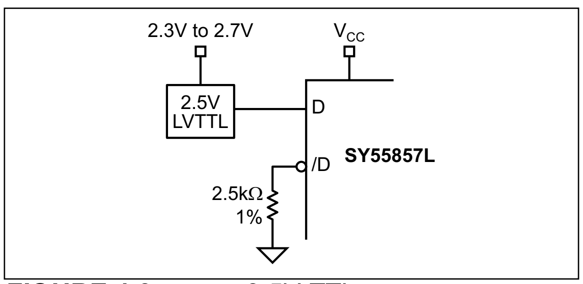


FIGURE 4-3: *2.5V TTL.*

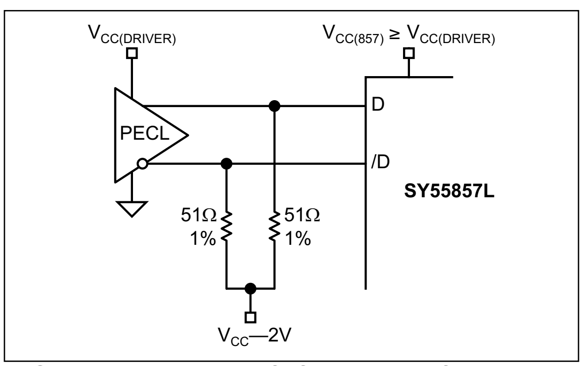


FIGURE 4-4: *DC-Coupled PECL.*

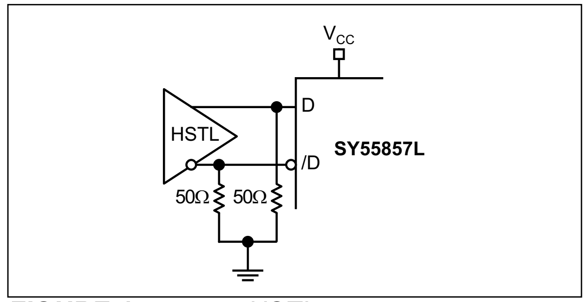


FIGURE 4-5: *HSTL.*

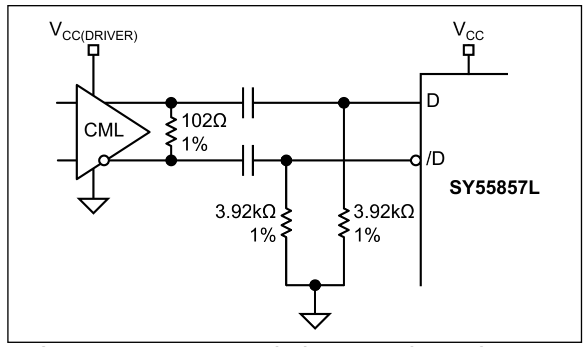


FIGURE 4-6: *AC-Coupled CML, Short Lines.*

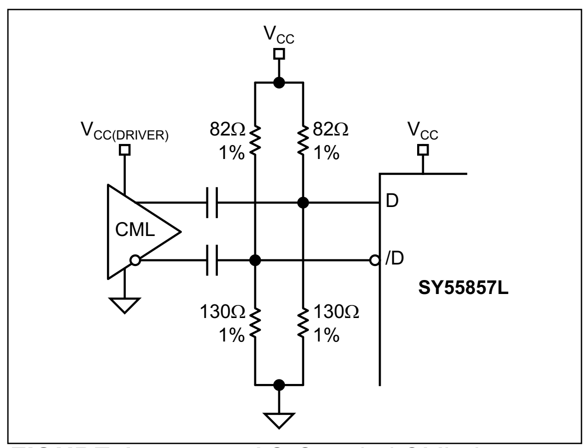


FIGURE 4-7: *AC-Coupled CML, Long Lines.*

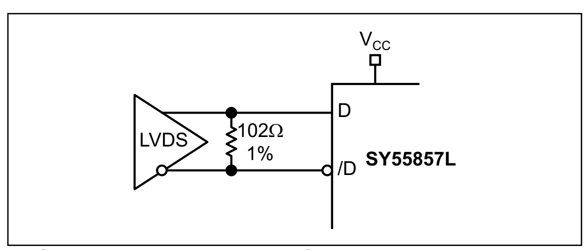


FIGURE 4-8: *LVDS.*

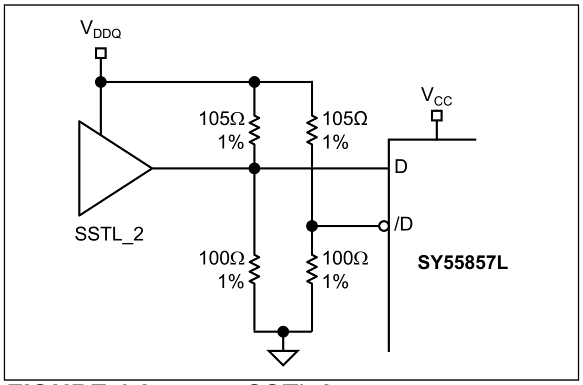


FIGURE 4-9: *SSTL 2.*

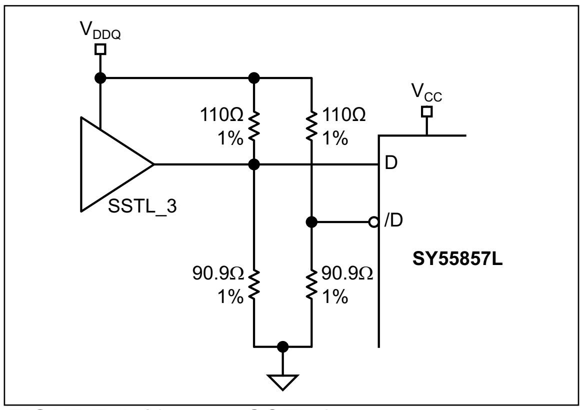
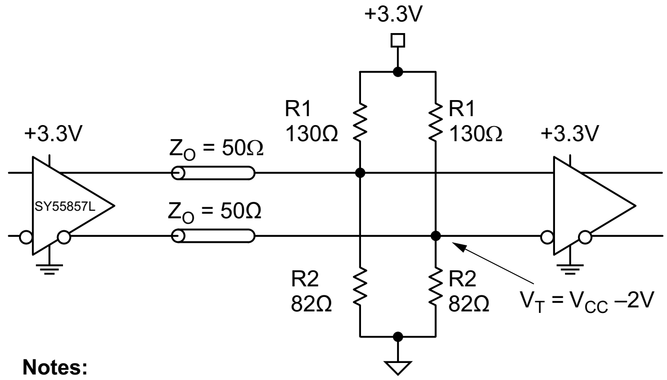


FIGURE 4-10: *SSTL 3.*

5.0 LVPECL OUTPUT TERMINATION

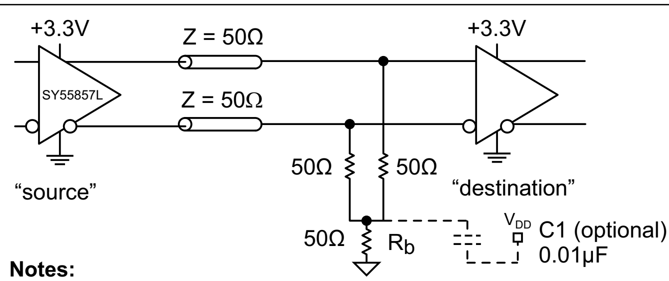
LVPECL outputs have very low output impedance (open emitter) and small signal swing that results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω-controlled impedance transmission lines. There are several techniques in terminating the LVPECL output, as shown in Figure 5-1 through Figure 5-3.



Notes:

1. For +3.3V systems: R1 = 130Ω, R2 = 82Ω.

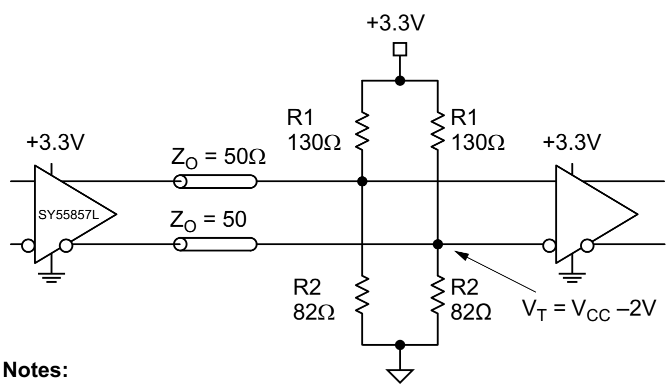
FIGURE 5-1: *Parallel Termination: Thevenin Equivalent.*



Notes:

1. Power-saving alternatives to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. Rb resistor sets the DC bias voltage, equal to V_T.
   For +3.3V systems: R_b = 46Ω to 50Ω.
4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

FIGURE 5-2: *Parallel Termination: Three-Resistor "Y-Termination".*



Notes:

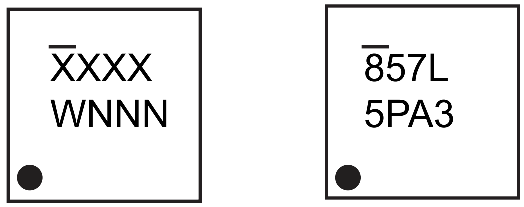
1. Unused output (/Q) must be terminated to balance the output.
2. For +3.3V systems: R1 = 130Ω, R2 = 82Ω, R3 = 1kΩ, R4 = 1.6kΩ.
3. Unused output pairs (Q and /Q) may be left floating.

FIGURE 5-3: *Terminating Unused I/O.*

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

10-Lead MSOP* Example

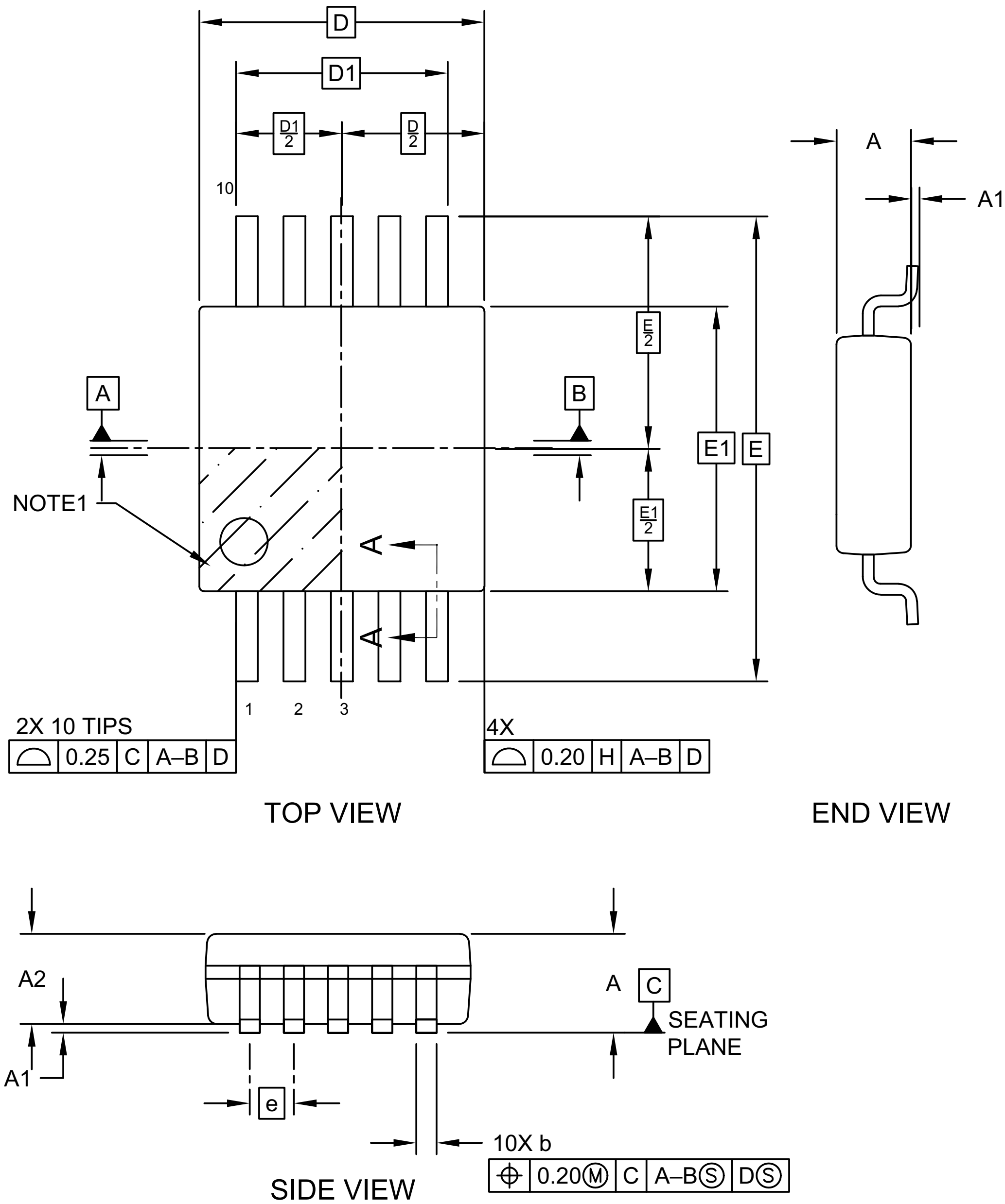


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

10-Lead Plastic Micro Small Outline Package (DQA)- 3x3x1.0 mm Body [MSOP]

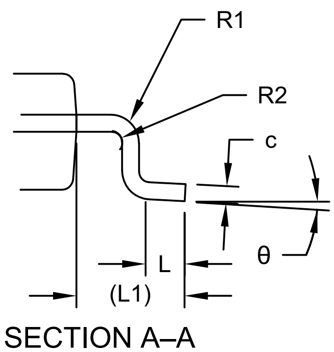
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

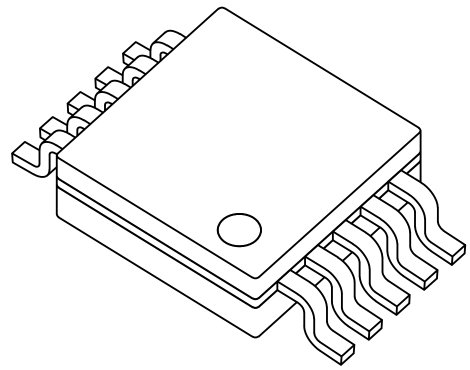


Microchip Technology Drawing C04-01081 Rev A Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (DQA)- 3x3x1.0 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.94	1.02	1.10
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.91	0.92	0.95
Overall Length	D		3.00 BSC	
Molded Package Length	D1		2.23 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.16	0.23	0.30
Terminal Thickness	c	0.13	0.15	0.23
Footprint	L	0.40	0.55	0.70
Terminal Length	L1		0.95 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	θ	0°	3°	6°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

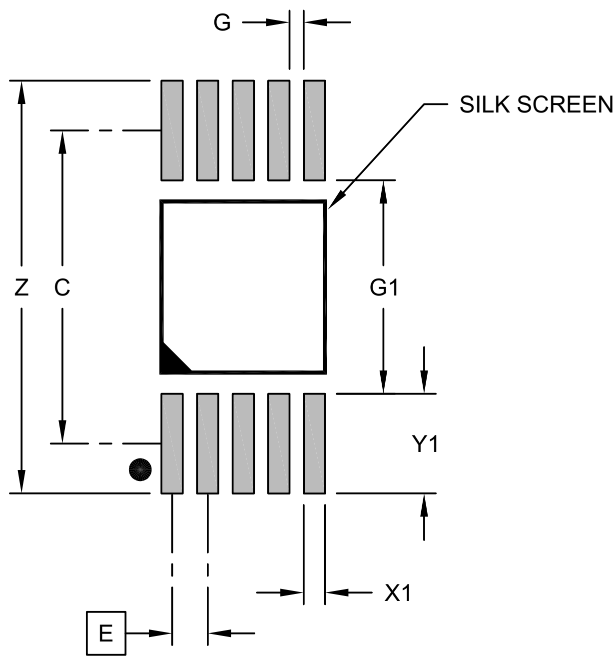
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-01081 Rev A Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (DQA)- 3x3x1.0 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			6.06
Contact Pad Width (X10)	X1	0.28	0.30	0.32
Contact Pad Length (X10)	Y1	1.24	1.26	1.28
Distance Between Pads (X5)	G1	3.00		
Distance Between Pads (X8)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-03081 Rev A

APPENDIX A: REVISION HISTORY

Revision A (February 2024)

- Converted Micrel document SY55857L to Microchip data sheet template DS20006853A.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	[-XX]
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY55857:	3.3V, 2.5 Gbps Any Input-to-LVPECL Dual Translator	
Supply Voltage:	L	=	3.3V
Package:	K	=	10-Lead 3 mm x 3 mm MSOP
Temperature Range:	G	=	–40°C to +85°C
Media Type:	<blank> TR	= =	100/Tube 1,000/Reel

Examples:

a) SY55857LKG:
SY55857, 3.3V Supply Voltage, 10-Lead MSOP, –40°C to +85°C Temperature Range, 100/Tube

b) SY55857LKG-TR:
SY55857, 3.3V Supply Voltage, 10-Lead MSOP, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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