

3.3V LVTTTL-to-Differential LVPECL and Differential LVPECL-to-LVTTTL Translator

Features

- 3.3V $\pm 10\%$ Power Supply
- Guaranteed AC Parameters over Temperature:
 $f_{MAX} > 275$ MHz (LVTTTL)
- < 2.5 ns LVPECL-to-LVTTTL Propagation Delay
- < 600 ps LVTTTL-to-LVPECL Propagation Delay
- Industrial Temperature Range: -40°C to $+85^{\circ}\text{C}$
- Available in 8-Lead MSOP and SOIC packages

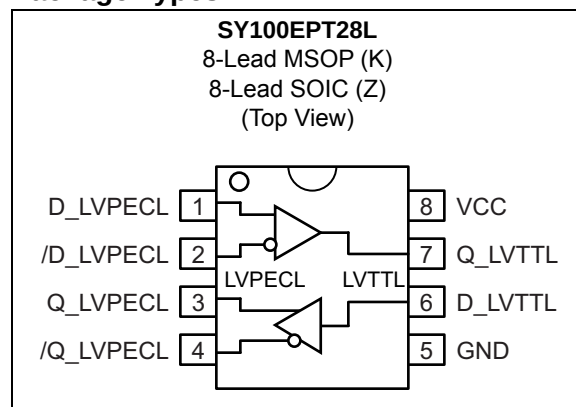
General Description

The SY100EPT28L is a differential LVPECL-to-LVTTTL translator and an LVTTTL-to-differential LVPECL translator in a single package. Because LVPECL (Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-pin package and the dual translation design of the EPT28L makes it ideal for applications that are sending and receiving signals across a backplane.

Under open input conditions, the $/D_LVPECL$ input will be biased at $V_{CC}/2$ and the D_LVPECL input will be pulled to GND. This condition will force the Q_LVTTTL to a low, ensuring stability.

The 100k series includes temperature compensation. Thus, logic levels are constant over temperature.

Package Types



SY100EPT28L

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage (V_{CC})	–0.5V to +3.8V
Input Voltage (V_{IN})	0V to V_{CC}
LVPECL Output Current (Continuous)	50 mA
LVPECL Output Current (Surge)	100 mA
Lead Temperature (Soldering, 5 sec.)	+260°C
Storage Temperature (T_S)	–65°C to +150°C

Operating Ratings ††

Supply Voltage Range (V_{CC})	+3.0V to +3.6V
Operating Temperature Range (T_A)	–40°C to +85°C
Package Thermal Resistance	
SOIC 8-Ld, Still-Air (θ_{JA})	160°C/W
SOIC 8-Ld, 500 lfpm (θ_{JA})	109°C/W
SOIC 8-Ld (θ_{JC})	39°C/W
MSOP 8-Ld, Still-Air (θ_{JA})	206°C/W
MSOP 8-Ld, 500 lfpm (θ_{JA})	155°C/W
MSOP 8-Ld (θ_{JC})	39°C/W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The device is not guaranteed to function outside its operating ratings.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{CC}	—	20	40	mA	$T_A = -40^{\circ}\text{C}$
		—	22	40		$T_A = +25^{\circ}\text{C}$
		—	25	40		$T_A = +85^{\circ}\text{C}$

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a PCB and transverse airflow greater than 500 lfpm is maintained.

TABLE 1-2: LVPECL DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{CC} = 3.0\text{V}$ to 3.6V ; $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	$V_{CC} - 1.145$	$V_{CC} - 1.020$	$V_{CC} - 0.895$	V	50Ω to $V_{CC} - 2.0\text{V}$
Output Low Voltage	V_{OL}	$V_{CC} - 1.945$	$V_{CC} - 1.820$	$V_{CC} - 1.695$	V	50Ω to $V_{CC} - 2.0\text{V}$
Input High Voltage (Single-Ended)	V_{IH}	$V_{CC} - 1.225$	—	$V_{CC} - 0.880$	V	—
Input Low Voltage (Single-Ended)	V_{IL}	$V_{CC} - 1.945$	—	$V_{CC} - 1.625$	V	—
Common Mode Range	V_{IHCMR}	1.2	—	V_{CC}	μA	Note 2
Input High Current	I_{IH}	—	—	150	μA	D, /D
Input Low Current	C_{IN}	0.5	—	—	μA	D, $V_{IN} = V_{IL(MIN)}$
		-150	—	—		/D

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a PCB and transverse airflow greater than 500 lfpm is maintained.

2: The CMR range is referenced to the most positive side of the differential input voltage.

TABLE 1-3: LVTTTL DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{CC} = 3.0\text{V}$ to 3.6V ; $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	2.0	—	—	V	$I_{OH} = -3\text{ mA}$
Output Low Voltage	V_{OL}	—	—	0.5	V	$I_{OL} = 24\text{ mA}$
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input Clamp Voltage	V_{IK}	-1.2	—	—	V	$I_{IK} = -18\text{ mA}$
Input High Current	I_{IH}	—	—	20	μA	$V_{IN} = 2.7\text{V}$
		—	—	100		$V_{IN} = V_{CC}$
Input Low Current	I_{IL}	-0.2	—	—	μA	$V_{IN} = 0.5\text{V}$
LVTTTL Output Short Circuit Current	I_{OUT}	-275	—	-80	mA	$V_{OUT} = 0\text{V}$
Input Capacitance	C_{IN}	—	0.75	—	pF	SOIC, $T_A = +25^{\circ}\text{C}$
		—	1.1	—		MSOP, $T_A = +25^{\circ}\text{C}$

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a PCB and transverse airflow greater than 500 lfpm is maintained.

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TABLE 1-4: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.0V$ to $3.6V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$ unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	f_{MAX}	700	—	—	MHz	LVPECL, Output Toggle Freq.
		275	350	—		LVTTL, Output Toggle Freq.
Propagation Delay D_LVPECL to Q_LVTTL	t_{PLH}, t_{PHL}	1.5	—	2.5	ns	$C_L = 20$ pF
Propagation Delay Q_LVTTL to D_LVPECL		100	400	600	ps	50Ω to $V_{CC} - 2.0V$
LVPECL Input Voltage Swing (Single-Ended)	V_{PP}	100	—	—	mV	Note 1
LVPECL Output Rise/Fall Times (20% to 80%)	t_r/t_f	200	—	500	ns	50Ω to $V_{CC} - 2.0V$
LVTTL Output Rise/Fall Times (20% to 80%)		0.5	—	1.0		$C_L = 20$ pF
Duty Cycle	t_{DC}	45	50	55	%	—
Cycle-to-Cycle Jitter (RMS)	t_{JITTER}	—	0.2	<1	ps _{RMS}	—

Note 1: $V_{PP(MIN)}$ is the minimum input swing for which AC parameters are guaranteed.

Termination Recommendations

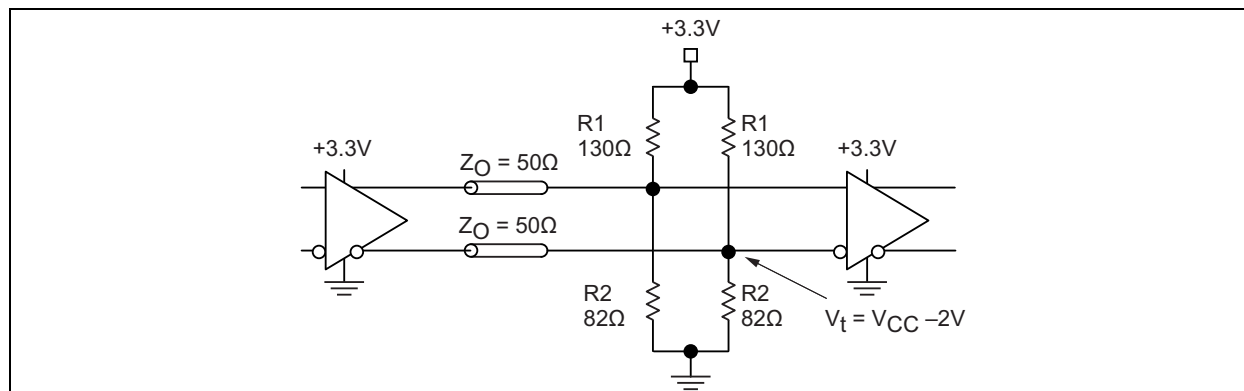


FIGURE 1-1: LVPECL Parallel Termination – Thevenin Equivalent.

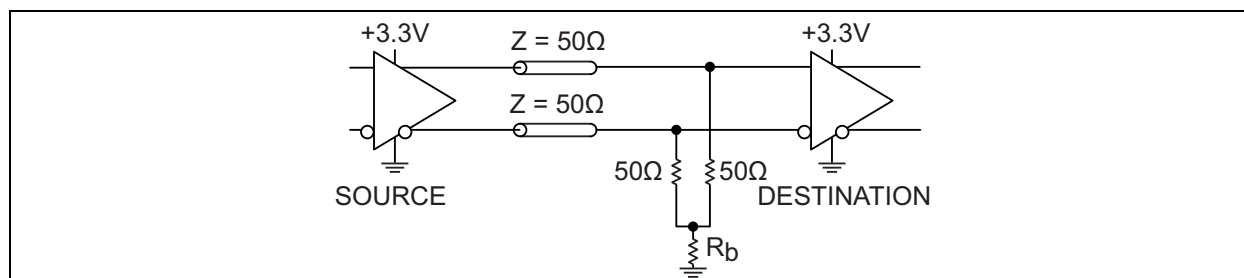


FIGURE 1-2: LVPECL Three-Resistor “Y Termination”.

Figure 1-2 is a power-saving alternative to four-resistor, Thevenin termination. Place termination resistors as close to the destination inputs as possible. The R_b resistor sets the DC voltage, equal to V_t . For 3.3V supply, R_b is between 46Ω and 50Ω .

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2	D_LVPECL, /D_LVPECL	Low Voltage Differential PECL Inputs. D_LVPECL with 75 k Ω internal pull-down, /D_LVPECL with 75 k Ω internal pull-down and pull-up.
3, 4	Q_LVPECL, /Q_LVPECL	Low Voltage Differential PECL Outputs.
5	GND	Ground.
6	D_LVTTL	Low Voltage TTL Input.
7	Q_LVTTL	Low Voltage TTL Output.
8	V _{CC}	3.3V positive supply.

3.0 PACKAGING INFORMATION

3.1 Package Marking Information

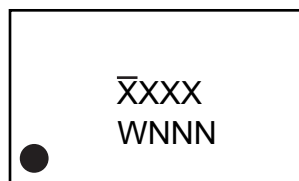
8-Lead SOIC*



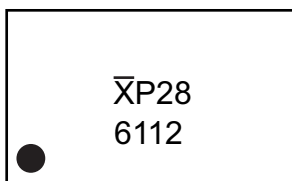
Example



8-Lead MSOP*



Example

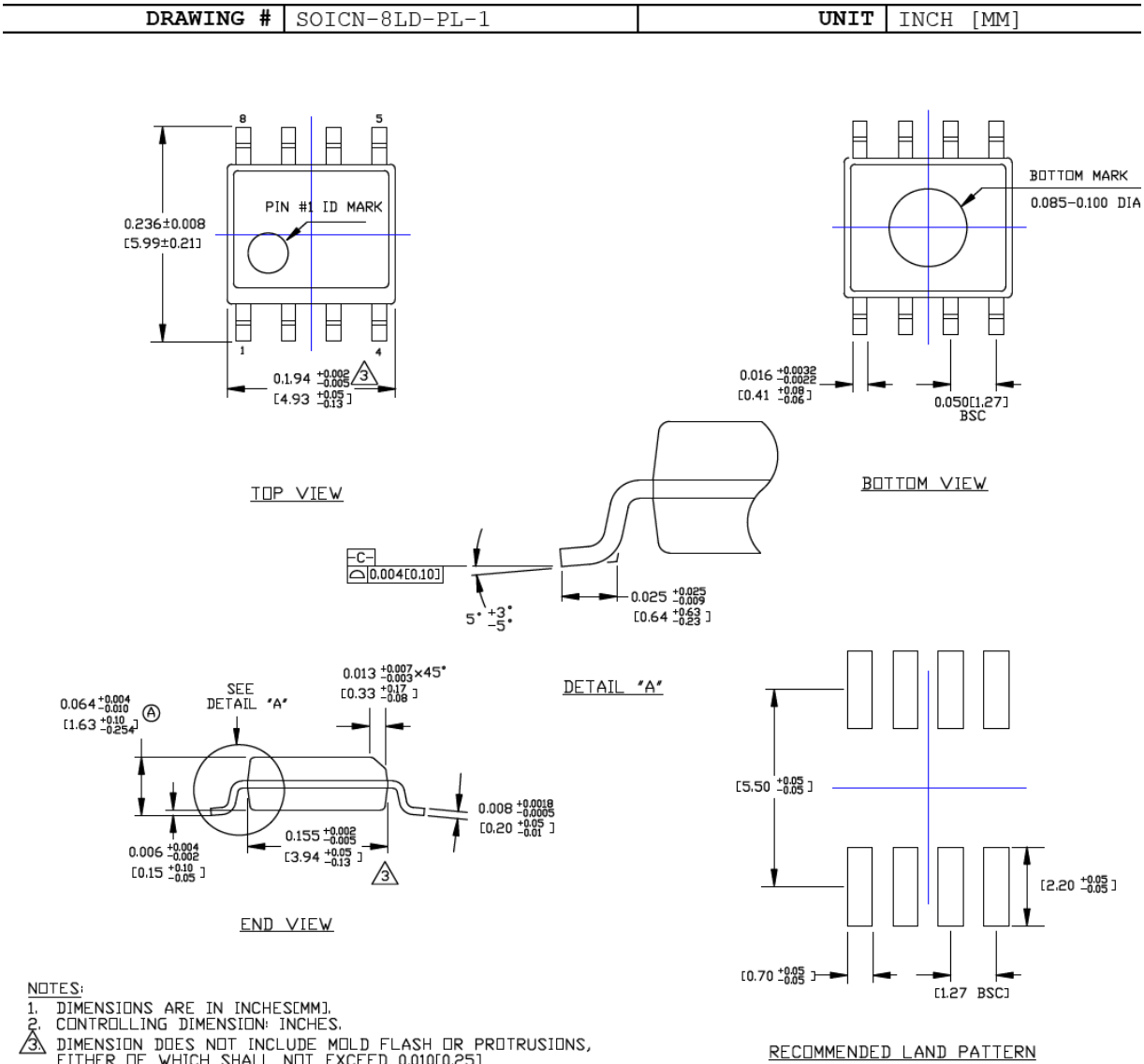


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (¯) and/or Overbar (¯) symbol may not be to scale.	

8-Lead SOIC Package Outline and Recommended Land Pattern

TITLE

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN



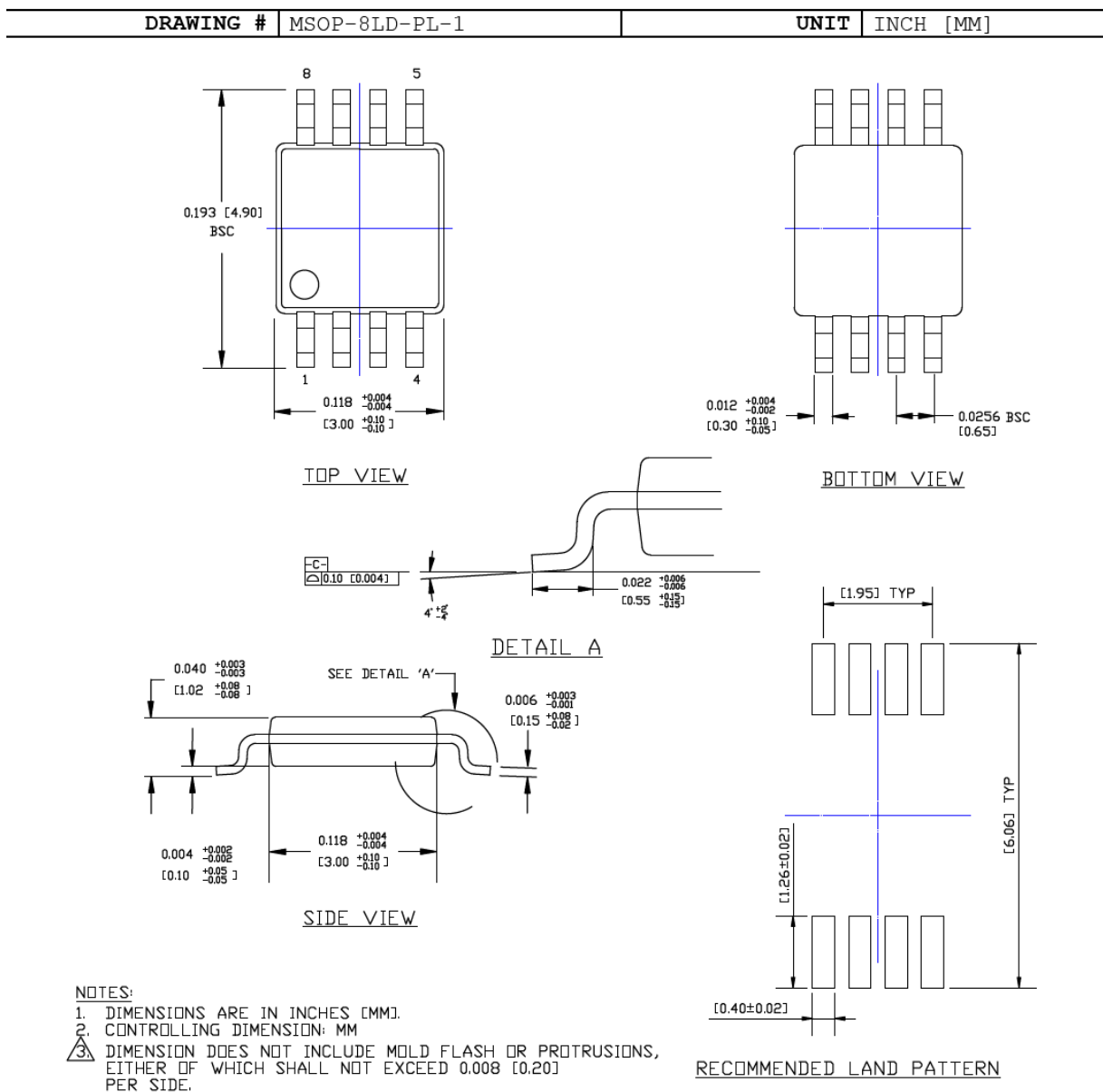
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

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8-Lead MSOP Package Outline and Recommended Land Pattern

TITLE

8 LEAD MSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN



Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (September 2018)

- Converted Micrel document SY100EPT28L to Microchip data sheet DS20006067A.
- Minor text changes throughout.
- Removed all reference to the EOL SY100EPT28L version.

SY100EPT28L

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.		X	X	-XX
Device		Package	Temperature Range	Special Processing
Device:		SY100EPT28L: 3V LVTTL-to-Differential LVPECL and Differential LVPECL-to-LVTTL Translator		
Package:	Z	=	8-Lead SOIC	
	K	=	8-Lead MSOP	
Temperature Range:	G	=	-40°C to +85°C (Pb-Free NiPdAu)	
Special Processing:	<blank>	=	95/Tube (SOIC package)	
	<blank>	=	100/Tube (MSOP package)	
	TR	=	1,000/Reel	

Examples:

a) SY100EPT28LZG: SY100EPT28L, 8-Lead SOIC, -40°C to +85°C (Pb-Free NiPdAu), 95/Tube

b) SY100EPT28LZG-TR: SY100EPT28L, 8-Lead SOIC, -40°C to +85°C (Pb-Free NiPdAu), 1,000/Reel

c) SY100EPT28LKG: SY100EPT28L, 8-Lead MSOP, -40°C to +85°C (Pb-Free NiPdAu), 100/Tube

d) SY100EPT28LKG-TR: SY100EPT28L, 8-Lead MSOP, -40°C to +85°C (Pb-Free NiPdAu), 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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