MICROCHIP

SST26LF064RT

64-Mbit Serial Quad I/O™ (SQI™) Radiation Tolerant Flash Memory

Features

- Single Voltage Read and Write Operations:
  - 3.0V-3.6V
- Radiation Tolerance Data:
  - Total dose:
    - Unbiased: 50 krad (Si) (Read) / 50 krad (Si) (Write)
    - Biased: 50 krad (Si) (Read) / 30 krad (Si) (Write)
- Heavy Ion Single-Event Effects (SEE):
  - Single Event Upset (SEU) Rate < 3.33e-14 upsets/bit/day
  - Latch-up immunity > 62.5 MeV.cm^2/mg (+125°C)
- Serial Interface Architecture:
  - Nibble-wide multiplexed I/O's with SPI-like serial command structure:
    - Mode 0 and Mode 3
  - x1/x2/x4 Serial Peripheral Interface (SPI) Protocol
- High-Speed Clock Frequency:
  - 80 MHz maximum
- Burst Modes:
  - Continuous linear burst
  - 8/16/32/64-byte linear burst with wrap-around
- Superior Reliability:
  - Endurance: 10,000 cycles (minimum)
  - Greater than 20 years data retention
- Fast Erase Time:
  - Sector/Block erase: 18 ms (typical), 25 ms (maximum)
  - Chip Erase: 35 ms (typical), 50 ms (maximum)
- Page Program:
  - 256 bytes per page in x1 or x4 mode
- End-of-Write Detection:
  - Software polling the BUSY bit in STATUS register
- Flexible Erase Capability:
  - Uniform 4-Kbyte sectors
  - Four 8-Kbyte top and bottom parameter overlay blocks
  - One 32-Kbyte top and bottom overlay blocks
  - Uniform 64-Kbyte overlay blocks
- Write Suspend:
  - Suspend Program or Erase operation to access another block/sector
- Software Reset (RST) Mode
- Software Protection:
  - Individual Block Write Protection with permanent lock-down capability:
    - 64-Kbyte blocks, two 32-Kbyte blocks and eight 8-Kbyte parameter blocks
  - Read Protection on top and bottom 8-Kbyte parameter blocks
- Security ID:
  - One-Time-Programmable (OTP) 2-Kbyte, Secure ID:
    - 64-bit unique, factory preprogrammed identifier
    - User-programmable area
- Temperature Range:
  - Military: -55°C to +125°C
- All devices are RoHS compliant

Packages

- 8-Lead SOIJ (5.28 mm) - 0.136g
- 8-Lead Ceramic Dual Flat Package (CDFP) - 0.723g

Product Description

The Serial Quad I/O™ (SQI™) Flash memory device features a six-wire, 4-bit I/O interface that allows for high-performance operation in a low pin count package.

SST26LF064RT is a radiation-tolerant device manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

SST26LF064RT significantly improves performance and reliability while lowering power consumption. This device writes (Program or Erase) with a single power supply of 3.0V-3.6V. The total energy consumed is a function of the applied voltage, current and time of application. For any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time. Therefore, the total energy consumed during any erase or program operation is less than alternative Flash memory technologies. See Figure 2-1 for pin assignments and Table 2-1 for pin descriptions.

Space Quality Grade

The hermetic SST26LF064RT is manufactured in compliance with the following MIL Class Q or Class V requirements: screening testing, qualification testing and TCI/QCI specifications. The plastic SST26LF064RT is compliant with AEC-Q100 automotive requirements with specific additional tests necessary for space applications. Screening and qualification flows are described in Aerospace and Defense AEQA0242/DS60001546 specification available on the Microchip website.

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To determine if an errata sheet exists for a particular device, please check with one of the following:

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When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

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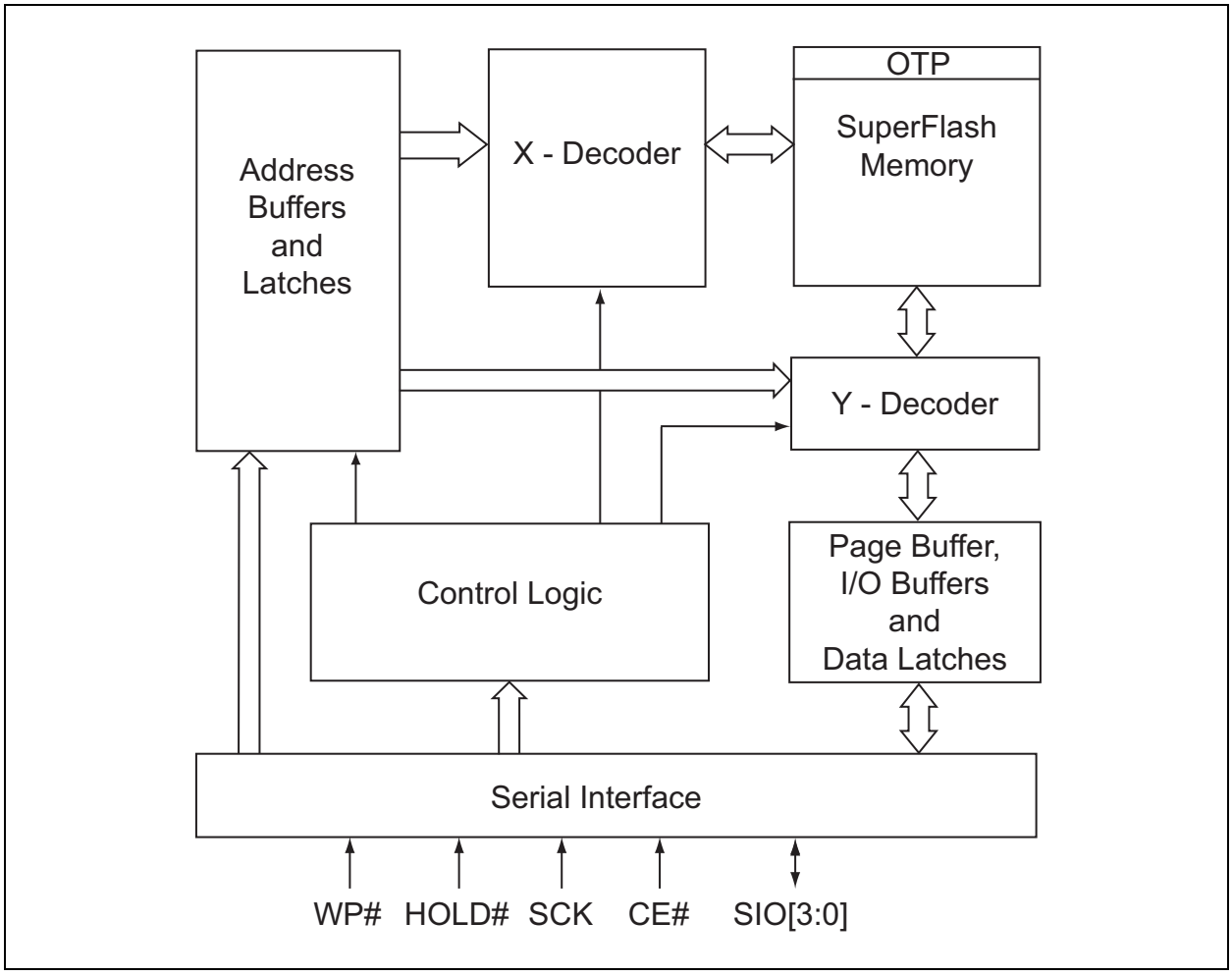
1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN DESCRIPTION FOR 8-LEAD SOIJ AND 8-LEAD CERAMIC

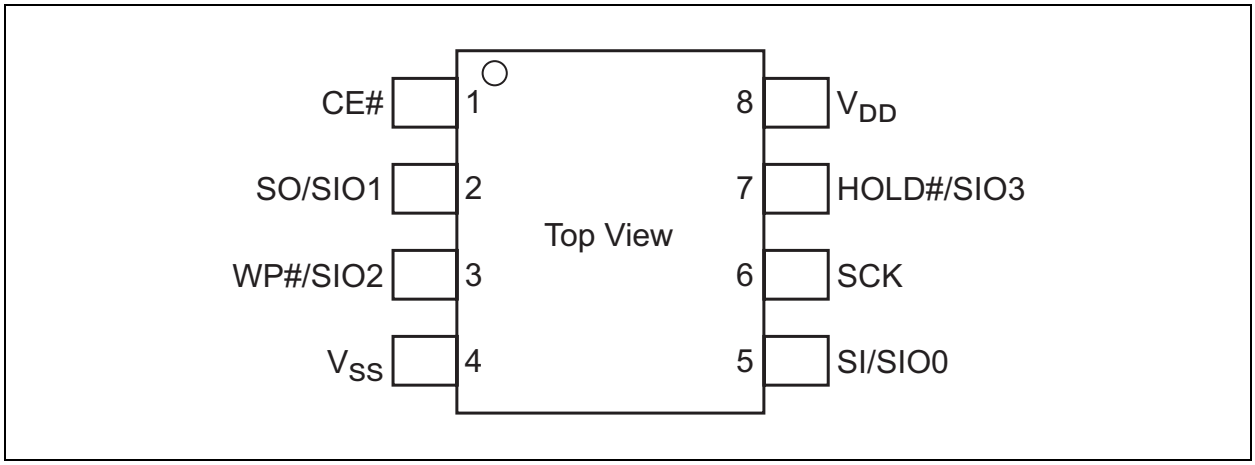


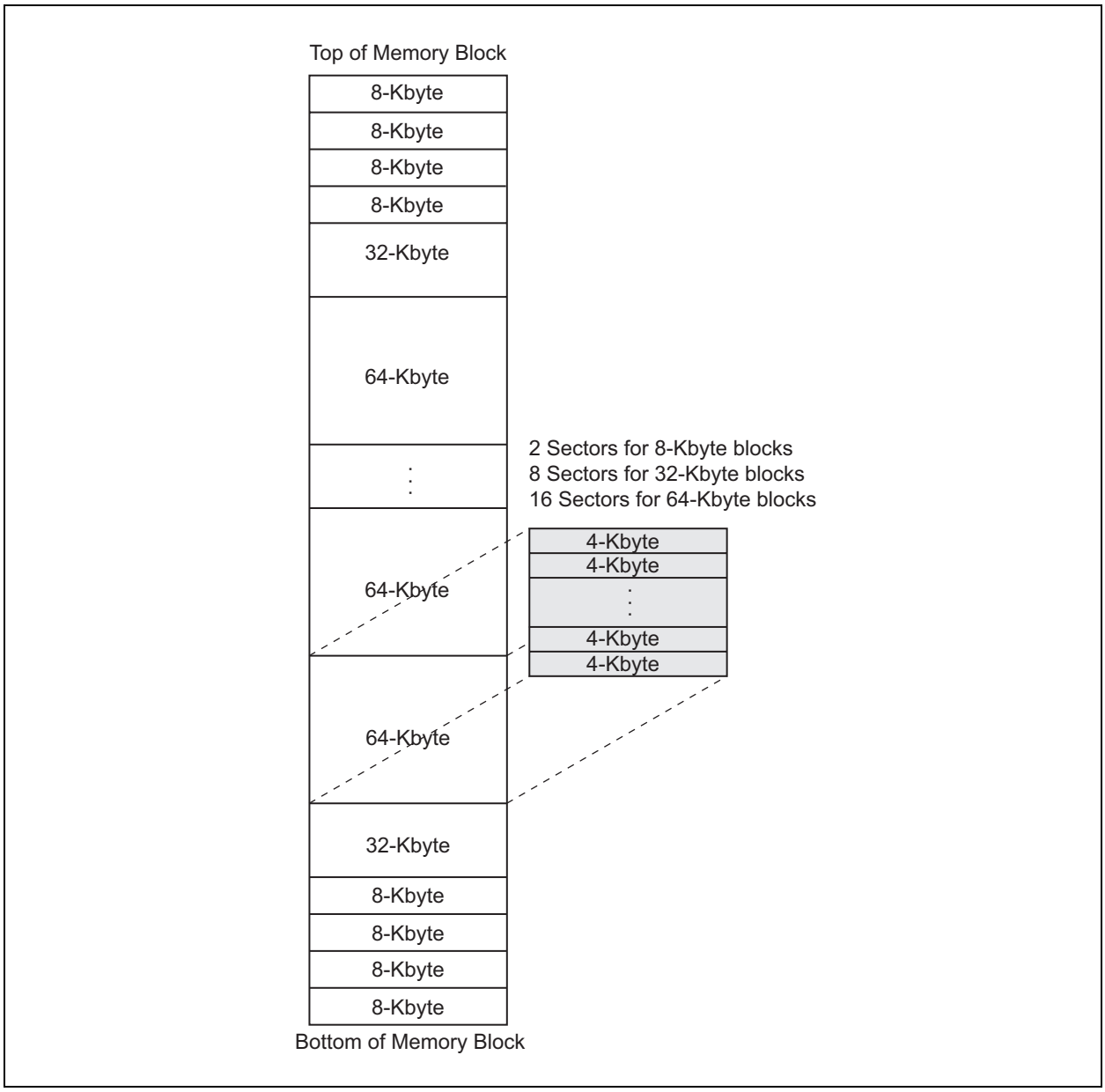
TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
CE#	Chip Enable	The device is enabled by a high-to-low transition on CE#. CE# must remain low for the duration of any command sequence; or in the case of write operations, for the command/data input sequence.
SO	Serial Data Output for SPI Mode	Transfer data serially out of the device. Data are shifted out on the falling edge of the serial clock. SO is the default state after a Power-on Reset.
SIO[3:0]	Serial Data Input/Output	Transfer commands, addresses or data serially into the device or data out of the device. Inputs are latched on the rising edge of the serial clock. Data are shifted out on the falling edge of the serial clock. The Enable Quad I/O (EQIO) command instruction configures these pins for Quad I/O mode.
WP#	Write-Protect	The WP# is used in conjunction with the WPEN and IOC bits in the Configuration register to prohibit write operations to the Block Protection register. This pin only works in SPI, single-bit and dual-bit Read mode.
VSS	Ground	
SI	Serial Data Input for SPI Mode	Transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock. SI is the default state after a Power-on Reset.
SCK	Serial Clock	Provide the timing of the serial interface. Commands, addresses or input data are latched on the rising edge of the clock input, while output data are shifted out on the falling edge of the clock input.
HOLD#	Hold	Temporarily stops serial communication with the SPI Flash memory while the device is selected. This pin only works in SPI, single-bit and dual-bit Read mode and must be tied high when not in use.
VDD	Power Supply	Provide power supply voltage.

3.0 MEMORY ORGANIZATION

The SST26LF064RT SQI memory array is organized in uniform, 4-Kbyte erasable sectors with the following erasable blocks: eight 8-Kbyte parameter, two 32-Kbyte overlay and 126 64-Kbyte overlay blocks (see Figure 3-1).

FIGURE 3-1: MEMORY MAP



4.0 DEVICE OPERATION

SST26LF064RT supports both Serial Peripheral Interface (SPI) bus protocol and a 4-bit multiplexed SQI bus protocol. To provide backward compatibility to traditional SPI Serial Flash devices, the device's initial state after a Power-on Reset is SPI mode, which supports multi-I/O (x1/x2/x4) Read/Write commands. A command instruction configures the device to SQI mode. The data flow in the SQI mode is similar to the SPI mode, except it uses four multiplexed I/O signals for command, address and data sequence.

SQI Flash Memory supports both Mode 0 (0,0) and Mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus host is in Standby mode and no data are being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data I/O (SIO[3:0]) are sampled at the rising edge of the SCK clock signal for input and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals, as shown in Figure 4-1. The SQI protocol uses four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 4-2. This means the SQI protocol quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package.

FIGURE 4-1: SPI PROTOCOL (TRADITIONAL 25 SERIES SPI DEVICE)

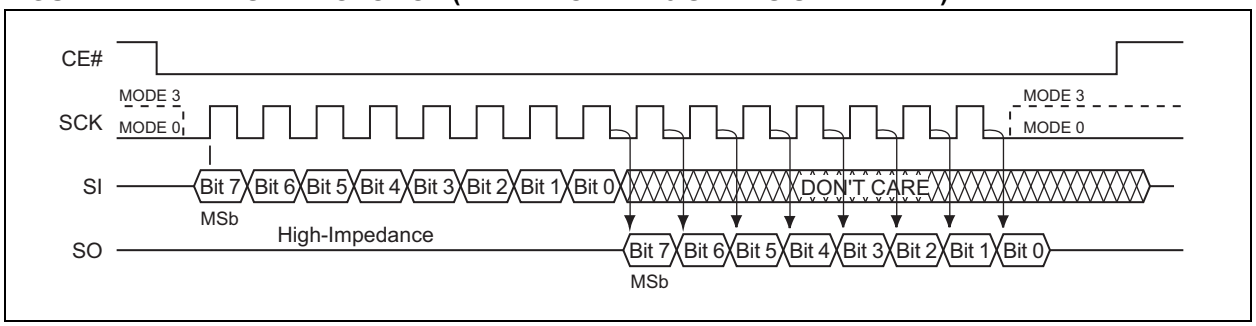
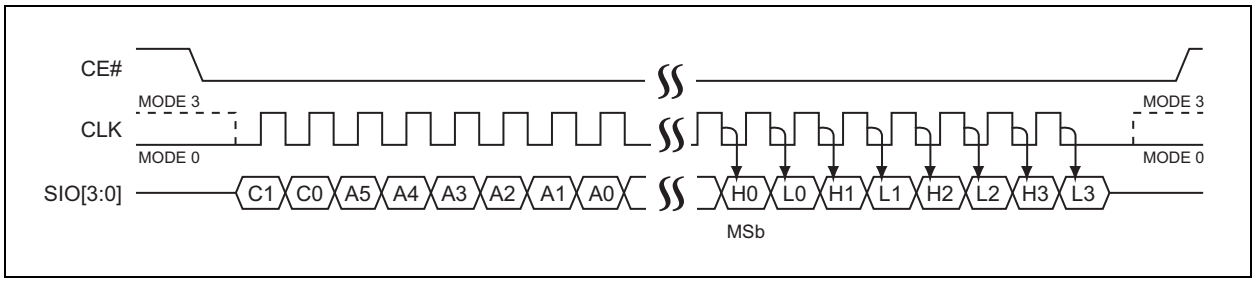


FIGURE 4-2: SQI SERIAL QUAD I/O PROTOCOL



4.1 Device Protection

SST26LF064RT offers a flexible memory protection scheme that allows the protection state of each individual block to be controlled separately. In addition, the Write Protection Lock-Down register prevents any change of the lock status during device operation. To avoid inadvertent writes during power-up, the device is write-protected by default after a Power-on Reset cycle. A Global Block Protection Unlock command offers a single command cycle that unlocks the entire memory array for faster manufacturing throughput.

For extra protection, there is an additional nonvolatile register that can permanently write-protect the Block Protection register bits for each individual block.

Each of the corresponding lock-down bits are One-Time-Programmable (OTP); once written, they cannot be erased. Data that had been previously programmed into these blocks cannot be altered by programming or erase and are not reversible.

4.1.1 INDIVIDUAL BLOCK PROTECTION

SST26LF064RT has a Block Protection register which provides a software mechanism to write lock the individual memory blocks and write lock and/or read lock the individual parameter blocks. The Block Protection register is 144-bit wide: two bits each for the eight 8-Kbyte parameter blocks (write lock and read lock) and one bit each for the remaining 32-Kbyte and 64-Kbyte overlay blocks (write lock). See Table 5-6 for address range protected per register bit.

Each bit in the Block Protection register (BPR) can be written to a '1' (protected) or '0' (unprotected). For the parameter blocks, the Most Significant bit is for read lock and the Least Significant bit is for write lock. Read locking the parameter blocks provides additional security for sensitive data after retrieval (e.g., after initial boot). If a block is read-locked, all reads to the block return data 00H.

The Write Block Protection Register command is a two-cycle command, which requires that Write Enable (WREN) is executed prior to the Write Block Protection Register command. The Global Block Protection Unlock command clears all write protection bits in the Block Protection register.

4.1.2 WRITE PROTECTION LOCK-DOWN (VOLATILE)

To prevent changes to the Block Protection register, use the Lockdown Block Protection Register (LBPR) command to enable Write Protection Lock-Down. Once Write Protection Lock-Down is enabled, the Block Protection register cannot be changed. To avoid inadvertent lock-down, the WREN command must be executed prior to the LBPR command.

To reset Write Protection Lock-Down, performing a power cycle on the device is required. The Write Protection Lock-Down status may be read from the STATUS register.

4.1.3 WRITE LOCK LOCK-DOWN (NONVOLATILE)

The nonvolatile Write Lock Lock-Down register is an alternate register that permanently prevents changes to the block-protect bits. The nonvolatile Write Lock Lock-Down register (nVWLDR) is 136-bit wide per device: one bit each for the eight 8-Kbyte parameter blocks and one bit each for the remaining 32-Kbyte and 64-Kbyte overlay blocks. See Table 5-6 for address range protected per register bit.

Writing '1' to any or all of the nVWLDR bits disables the change mechanism for the corresponding Write Lock bit in the BPR and permanently sets this bit to a '1' (protected) state. After this change, both bits will be set to '1', regardless of the data entered in subsequent writes to either the nVWLDR or the BPR. Subsequent writes to the nVWLDR can only alter available locations that have not been previously written to a '1'. This method provides write protection for the corresponding memory array block by protecting it from future program or erase operations.

Writing a '0' in any location in the nVWLDR has no effect on either the nVWLDR or the corresponding Write Lock bit in the BPR.

Note that if the Block Protection register had been previously locked down, the device must be power cycled before using the nVWLDR (see **Section 4.1.2 "Write Protection Lock-Down (Volatile)"**). If the Block Protection register is locked down and the Write nVWLDR command is accessed, the command will be ignored.

4.2 Hardware Write Protection

The hardware Write Protection pin (WP#) is used in conjunction with the WPEN and IOC bits in the Configuration register to prohibit write operations to the Block Protection and Configuration registers. The WP# pin function only works in SPI single-bit and dual-bit Read mode when the IOC bit in the Configuration register is set to '0'.

The WP# pin function is disabled when the WPEN bit in the Configuration register is '0'. This allows installation of the SST26LF064RT in a system with a grounded WP# pin while still enabling write to the Block Protection register. The Lock Down function of the Block Protection register supersedes the WP# pin (see Table 4-1 for Write Protection Lock-Down states).

The factory default setting at power-up of the WPEN bit is '0', disabling the Write Protect function of the WP# after power-up. WPEN is a nonvolatile bit; once the bit is set to '1', the Write-Protect function of the WP# pin continues to be enabled after power-up. The WP# pin only protects the Block Protection register and Configuration register from changes. Therefore, if the WP# pin is set to low before or after a program or erase command or while an internal write is in progress, it will have no effect on the write command.

The IOC bit takes priority over the WPEN bit in the Configuration register. When the IOC bit is '1', the function of the WP# pin is disabled and the WPEN bit serves no function. When the IOC bit is '0' and WPEN is '1', setting the WP# pin active-low prohibits write operations to the Block Protection register.

TABLE 4-1: WRITE PROTECTION LOCK-DOWN STATES

WP#	IOC	WPEN	WPLD	Execute WBPR Instruction	Configuration Register
L	0	1	1	Not Allowed	Protected
L	0	0	1	Not Allowed	Writable
L	0	1	0	Not Allowed	Protected
L	0(1)	0(2)	0	Allowed	Writable
H	0	X	1	Not Allowed	Writable
H	0	X	0	Allowed	Writable
X	1	X	1	Not Allowed	Writable
X	1	0(2)	0	Allowed	Writable

Note 1: Default at power-up register settings for SST26LF064RT

2: Factory default setting is '0'. This is a nonvolatile bit; default at power-up is the value set prior to power-down.

4.3 Security ID

SST26LF064RT offers a 2-Kbyte Security ID (Sec ID) feature. The Security ID space is divided into two parts:

- One factory-programmed, 64-bit segment
- One user-programmable segment

The factory-programmed segment is programmed during manufacturing with a unique number and cannot be changed. The user-programmable segment is left unprogrammed for the customer to program as desired.

Use the Program Security ID (PSID) command to program the Security ID using the address shown in Table 5-5. The Security ID can be locked using the Lockout Security ID (LSID) command. This prevents any future write operations to the Security ID.

The factory-programmed portion of the Security ID cannot be programmed by the user and neither the factory-programmed nor user-programmable areas can be erased.

4.4 Hold Operation

The HOLD# pin pauses active serial sequences without resetting the clocking sequence. Please note: this pin is active after every power-up and only operates during SPI single-bit and dual-bit modes. The SST26LF064RT is shipped with the IOC bit set to '0' and the HOLD# pin function enabled.

The HOLD# pin is always disabled in SQI mode and only works in SPI single-bit and dual-bit Read mode.

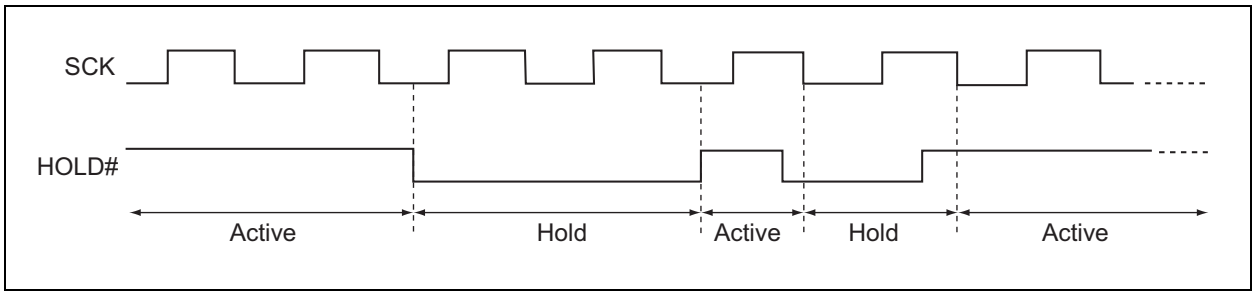
To activate Hold mode, CE# must be in active-low state. Hold mode begins when the SCK active-low state coincides with the falling edge of the HOLD# signal. Hold mode ends when the HOLD# signal's rising edge coincides with the SCK active-low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active-low state, then the device enters Hold mode when the SCK next reaches the active-low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active-low state, then the device exits Hold mode when the SCK next reaches the active-low state (see Figure 4-3).

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active-high during a Hold condition, it resets the internal logic of the device. As long as the HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active-high and CE# must be driven active-low.

FIGURE 4-3: HOLD CONDITION WAVEFORM



4.5 STATUS Register

The STATUS register is a read-only register that provides the following status information: whether the Flash memory array is available for any read or write operation, if the device is write enabled, whether an erase or program operation is suspended and if the Block Protection register and/or Security ID are locked down. During an internal erase or program operation, the STATUS register can be read to determine the completion of an operation in progress. Table 4-2 describes the function of each bit in the STATUS register.

TABLE 4-2: STATUS REGISTER

Bit	Name	Function	Default at Power-Up	Read/Write (R/W)
0	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	Write Enable Latch status 1 = Device is write enabled 0 = Device is not write enabled	0	R
2	WSE	Write Suspend Erase status 1 = Erase suspended 0 = Erase is not suspended	0	R
3	WSP	Write Suspend Program status 1 = Program suspended 0 = Program is not suspended	0	R
4	WPLD	Write Protection Lock-Down status 1 = Write Protection Lock-Down enabled 0 = Write Protection Lock-Down disabled	0	R
5	SEC(1)	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0	R
6	RES	Reserved for future use	0	R
7	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R

Note 1: The Security ID status will always be '1' at power-up after a successful execution of the Lockout Security ID instruction, otherwise default at power-up is '0'.

4.5.1 WRITE ENABLE LATCH (WEL)

The Write Enable Latch (WEL) bit indicates the status of the internal memory's Write Enable Latch. If the WEL bit is set to '1', the device is write enabled. If the bit is set to '0' (Reset), the device is not write enabled and does not accept any memory Program or Erase, Protection Register Write or Lock-Down commands. The Write Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Reset
- Write Disable (WRDI) Instruction
- Page Program Instruction Completion
- Sector Erase Instruction Completion
- Block Erase Instruction Completion
- Chip Erase Instruction Completion
- Write Block Protection Register Instruction
- Lock Down Block Protection Register Instruction
- Program Security ID Instruction Completion
- Lockout Security ID Instruction Completion
- Write Suspend Instruction
- SPI Quad Page Program Instruction Completion
- Write STATUS Register

4.5.2 WRITE SUSPEND ERASE STATUS (WSE)

The Write Suspend Erase status (WSE) bit indicates when an erase operation has been suspended. The WSE bit is '1' after the host issues a suspend command during an erase operation. Once the suspended Erase resumes, the WSE bit is reset to '0'.

4.5.3 WRITE SUSPEND PROGRAM STATUS (WSP)

The Write Suspend Program status (WSP) bit indicates when a program operation has been suspended. The WSP is '1' after the host issues a suspend command during the Program operation. Once the suspended Program resumes, the WSP bit is reset to '0'.

4.5.4 WRITE PROTECTION LOCK-DOWN STATUS (WPLD)

The Write Protection Lock-Down status (WPLD) bit indicates when the Block Protection register is locked down to prevent changes to the protection settings. The WPLD is '1' after the host issues a Lock Down Block Protection command. After a power cycle, the WPLD bit is reset to '0'.

4.5.5 SECURITY ID STATUS (SEC)

The Security ID Status (SEC) bit indicates when the Security ID space is locked to prevent a write command. The SEC is '1' after the host issues a Lockout SID command. Once the host issues a Lockout SID command, the SEC bit can never be reset to '0.'

4.5.6 BUSY

The Busy bit determines whether there is an internal erase or program operation in progress. If the BUSY bit is '1', the device is busy with an internal erase or program operation. If the bit is '0', no erase or program operation is in progress.

4.5.7 CONFIGURATION REGISTER

The Configuration register is a Read/Write register that stores a variety of configuration information. See Table 4-3 for the function of each bit in the register.

TABLE 4-3: CONFIGURATION REGISTER

Bit	Name	Function	Default at Power-Up	Read/Write (R/W)
0	RES	Reserved	0	R
1	IOC	I/O Configuration for SPI mode 1 = WP# and HOLD# pins disabled 0 = WP# and HOLD# pins enabled	0(1)	R/W
2	RES	Reserved	0	R
3	BPNV	Block Protection Volatility State 1 = No memory block has been permanently locked 0 = Any block has been permanently locked	1	R
4	RES	Reserved	0	R
5	RES	Reserved	0	R
6	RES	Reserved	0	R

Note 1: SST26LF064RT default at Power-up is '0'.

2: Factory default setting. This is a nonvolatile bit; default at power-up will be the setting prior to power-down.

TABLE 4-3: CONFIGURATION REGISTER

Bit	Name	Function	Default at Power-Up	Read/Write (R/W)
7	WPEN	Write Protection Pin (WP#) Enable 1 = WP# enabled 0 = WP# disabled	0(2)	R/W

Note 1: SST26LF064RT default at Power-up is '0'.

2: Factory default setting. This is a nonvolatile bit; default at power-up will be the setting prior to power-down.

4.5.8 I/O CONFIGURATION (IOC)

The I/O Configuration (IOC) bit reconfigures the I/O pins. The IOC bit is set by writing a '1' to Bit 1 of the Configuration register. When the IOC bit is '0', the WP# pin and HOLD# pin are enabled (SPI or Dual Configuration setup). When the IOC bit is set to '1', the SIO2 pin and SIO3 pin are enabled (SPI Quad I/O Configuration setup). The IOC bit must be set to '1' before issuing the following SPI commands: SQOR (6BH), SQIOR (EBH), RBSPI (ECH) and SPI Quad page program (32H). Without setting the IOC bit to '1', those SPI commands are not valid. The I/O configuration bit does not apply when in SQI mode. The default at power-up for SST26LF064RT is '0'.

4.5.9 BLOCK PROTECTION VOLATILITY STATE (BPNV)

The Block Protection Volatility State bit indicates whether any block has been permanently locked with the nVWLDR. When no bits in the nVWLDR have been set, the BPNV is '1'; this is the default state from the factory. When one or more bits in the nVWLDR are set to '1', the BPNV bit will also be '0' from that point forward, even after power-up.

4.5.10 WRITE-PROTECT ENABLE (WPEN)

The Write-Protect Enable (WPEN) bit is a nonvolatile bit that enables the WP# pin.

The Write-Protect (WP#) pin and the Write-Protect Enable (WPEN) bit control the programmable hardware write-protect feature. Setting the WP# pin to low and the WPEN bit to '1' enables hardware write protection. To disable hardware write protection, set either the WP# pin to high or the WPEN bit to '0'. There is latency associated with writing to the WPEN bit. Poll the BUSY bit in the STATUS register or wait TWPEN for the completion of the internal, self-timed write operation. When the chip is hardware write-protected, only write operations to Block Protection and Configuration registers are disabled. See **Section 4.2 "Hardware Write Protection"** and Table 4-1 for more information about the functionality of the WPEN bit.

5.0 INSTRUCTIONS

Instructions are used to read, write (erase and program) and configure the SST26LF064RT. The complete list of the instructions is provided in Table 5-1.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26LF064RT

Instruction	Description	Command Cycle(1)	Mode		Address Cycle(s)(2,3)	Dummy Cycle(s)(3)	Data Cycle(s)(3)	Max Freq(4)
			SPI	SQI				
Configuration								
NOP	No Operation	00H	X	X	0	0	0	80 MHz
RSTEN	Reset Enable	66H	X	X	0	0	0	
RST(5)	Reset Memory	99H	X	X	0	0	0	
EQIO	Enable Quad I/O	38H	X		0	0	0	
RSTQIO(6)	Reset Quad I/O	FFH	X	X	0	0	0	
RDSR	Read STATUS Register	05H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
WRSR	Write STATUS Register	01H	X	X	0	0	2	
RDCR	Read Configuration Register	35H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
Read								
Read	Read Memory	03H	X		3	0	1 to ∞	40 MHz
High-Speed Read	Read Memory at Higher Speed	0BH		X	3	3	1 to ∞	80 MHz
			X		3	1	1 to ∞	
SQOR(7)	SPI Quad Output Read	6BH	X		3	1	1 to ∞	
SQIOR(8)	SPI Quad I/O Read	EBH	X		3	3	1 to ∞	
SDOR(9)	SPI Dual Output Read	3BH	X		3	1	1 to ∞	
SDIOR(10)	SPI Dual I/O Read	BBH	X		3	1	1 to ∞	
SB	Set Burst Length	C0H	X	X	0	0	1	
RBSQI	SQI Read Burst with Wrap	0CH		X	3	3	n to ∞	
RBSPI(8)	SPI Read Burst with Wrap	ECH	X		3	3	n to ∞	

Note 1: Command cycle is two-clock periods in SQI mode and eight-clock periods in SPI mode.

2: Address bits above the Most Significant bit of each density can be VIL or VIH.

3: Address, Dummy/Mode bits and Data cycles are two-clock periods in SQI and eight-clock periods in SPI mode.

4: The maximum frequency for all instructions is up to 80 MHz unless otherwise noted.

5: RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.

6: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.

7: Data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

8: Address, Dummy/Mode bits and data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

9: Data cycles are four-clock periods.

10: Address, Dummy/Mode bits and Data cycles are four-clock periods.

11: Sector Addresses: Use AMS-A12, remaining address are don't care, but must be set to VIL or VIH.

12: Blocks are 64-Kbyte, 32-Kbyte or 8-Kbyte, depending on location. Block Erase Address: AMS-A16 for 64-Kbyte; AMS-A15 for 32-Kbyte; AMS-A13 for 8-Kbyte. Remaining addresses are don't care but must be set to VIL or VIH.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26LF064RT (CONTINUED)

Instruction	Description	Command Cycle(1)	Mode		Address Cycle(s)(2,3)	Dummy Cycle(s)(3)	Data Cycle(s)(3)	Max Freq(4)
			SPI	SQI				
Identification								
JEDEC-ID	JEDEC-ID Read	9FH	X		0	0	3 to ∞	80 MHz
Quad J-ID	Quad I/O J-ID Read	AFH		X	0	1	3 to ∞	
Write								
WREN	Write Enable	06H	X	X	0	0	0	80 MHz
WRDI	Write Disable	04H	X	X	0	0	0	
SE(11)	Erase 4 Kbytes of Memory Array	20H	X	X	3	0	0	
BE(12)	Erase 64, 32 or 8 KBytes of Memory Array	D8H	X	X	3	0	0	
CE	Erase Full Array	C7H	X	X	0	0	0	
PP	Page Program	02H	X	X	3	0	1 to 256	
SPI Quad PP(7)	SQI Quad Page Program	32H	X		3	0	1 to 256	
WRSU	Suspends Program/Erase	B0H	X	X	0	0	0	
WRRE	Resumes Program/Erase	30H	X	X	0	0	0	

Note 1: Command cycle is two-clock periods in SQI mode and eight-clock periods in SPI mode.

2: Address bits above the Most Significant bit of each density can be VIL or VIH.

3: Address, Dummy/Mode bits and Data cycles are two-clock periods in SQI and eight-clock periods in SPI mode.

4: The maximum frequency for all instructions is up to 80 MHz unless otherwise noted.

5: RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.

6: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.

7: Data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

8: Address, Dummy/Mode bits and data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

9: Data cycles are four-clock periods.

10: Address, Dummy/Mode bits and Data cycles are four-clock periods.

11: Sector Addresses: Use AMS-A12, remaining address are don't care, but must be set to VIL or VIH.

12: Blocks are 64-Kbyte, 32-Kbyte or 8-Kbyte, depending on location. Block Erase Address: AMS-A16 for 64-Kbyte; AMS-A15 for 32-Kbyte; AMS-A13 for 8-Kbyte. Remaining addresses are don't care but must be set to VIL or VIH.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26LF064RT (CONTINUED)

Instruction	Description	Command Cycle(1)	Mode		Address Cycle(s)(2,3)	Dummy Cycle(s)(3)	Data Cycle(s)(3)	Max Freq(4)
			SPI	SQI				
Protection								
RBPR	Read Block Protection Register	72H	X		0	0	1 to 18	80 MHz
				X	0	1	1 to 18	
WBPR	Write Block Protection Register	42H	X	X	0	0	1 to 18	
LBPR	Lock Down Block Protection Register	8DH	X	X	0	0	0	
nVWLDR	Nonvolatile Write Lock-Down Register	E8H	X	X	0	0	1 to 18	
ULBPR	Global Block Protection Unlock	98H	X	X	0	0	0	
RSID	Read Security ID	88H	X		2	1	1 to 2048	
				X	2	3	1 to 2048	
PSID	Program User Security ID Area	A5H	X	X	2	0	1 to 256	
LSID	Lockout Security ID Programming	85H	X	X	0	0	0	

Note 1: Command cycle is two-clock periods in SQI mode and eight-clock periods in SPI mode.

2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.

3: Address, Dummy/Mode bits and Data cycles are two-clock periods in SQI and eight-clock periods in SPI mode.

4: The maximum frequency for all instructions is up to 80 MHz unless otherwise noted.

5: RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.

6: Device accepts eight-clock command in SPI mode or two-clock command in SQI mode.

7: Data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

8: Address, Dummy/Mode bits and data cycles are two-clock periods. IOC bit must be set to '1' before issuing the command.

9: Data cycles are four-clock periods.

10: Address, Dummy/Mode bits and Data cycles are four-clock periods.

11: Sector Addresses: Use AMS-A12, remaining address are don't care, but must be set to V_{IL} or V_{IH}.

12: Blocks are 64-Kbyte, 32-Kbyte or 8-Kbyte, depending on location. Block Erase Address: AMS-A16 for 64-Kbyte; AMS-A15 for 32-Kbyte; AMS-A13 for 8-Kbyte. Remaining addresses are don't care but must be set to V_{IL} or V_{IH}.

5.1 No Operation (NOP)

The No Operation command only cancels a Reset Enable command. NOP has no impact on any other command.

5.2 Reset Enable (RSTEN) and Reset (RST)

The Reset operation is used as a system (software) Reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset Enable (RSTEN) followed by Reset (RST).

To reset the SST26LF064RT, the host drives CE# low, sends the Reset Enable command (66H) and drives CE# high. Next, the host drives CE# low again, sends the Reset command (99H) and drives CE# high (see Figure 5-1).

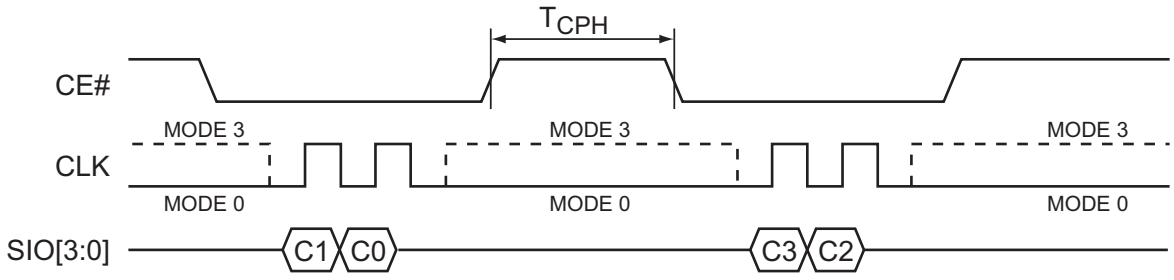
The Reset operation requires the Reset Enable command followed by the Reset command. Any command other than the Reset command after the Reset Enable command will disable the Reset Enable.

Once the Reset Enable and Reset commands are successfully executed, the device returns to normal operation Read mode and then does the following:

- Resets the protocol to SPI mode
- Resets the burst length to 8 bytes
- Clears all the bits, except for bit 4 (WPLD) and bit 5 (SEC), in the STATUS register to their default states
- Clears bit 1 (IOC) in the Configuration register to its default state

A device Reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the Reset timing may vary. Recovery from a write operation requires more latency time than recovery from other operations. See Table 8-2 for Rest timing parameters.

FIGURE 5-1: RESET SEQUENCE



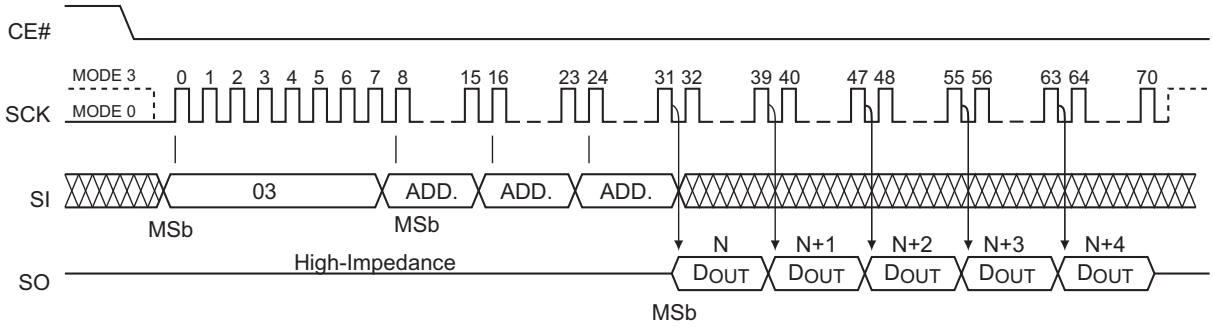
Note: C[1:0] = 66H; C[3:2] = 99H

5.3 Read (40 MHz)

The Read instruction, 03H, is supported in SPI bus protocol only with clock frequencies up to 40 MHz. This command is not supported in SQI bus protocol. The device outputs the data starting from the specified address location then continuously streams the data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically return to the beginning (wrap-around) of the address space.

Initiate the Read instruction by executing an 8-bit command, 03H, followed by address bits A[23:0]. CE# must remain active-low for the duration of the Read cycle. See Figure 5-2 for Read Sequence.

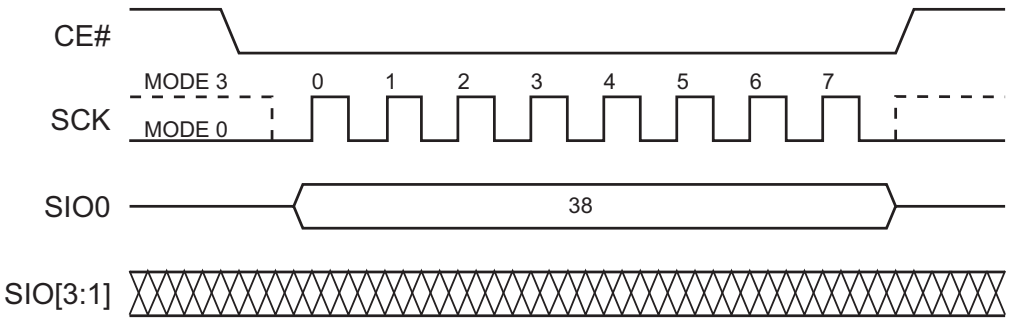
FIGURE 5-2: READ SEQUENCE (SPI)



5.4 Enable Quad I/O (EQIO)

The Enable Quad I/O (EQIO) instruction, 38H, enables the Flash device for SQI bus operation. Upon completion of the instruction, all instructions thereafter are expected to be 4-bit multiplexed input/output (SQI mode) until a power cycle or a “Reset Quad I/O instruction” is executed (see Figure 5-3).

FIGURE 5-3: ENABLE QUAD I/O SEQUENCE



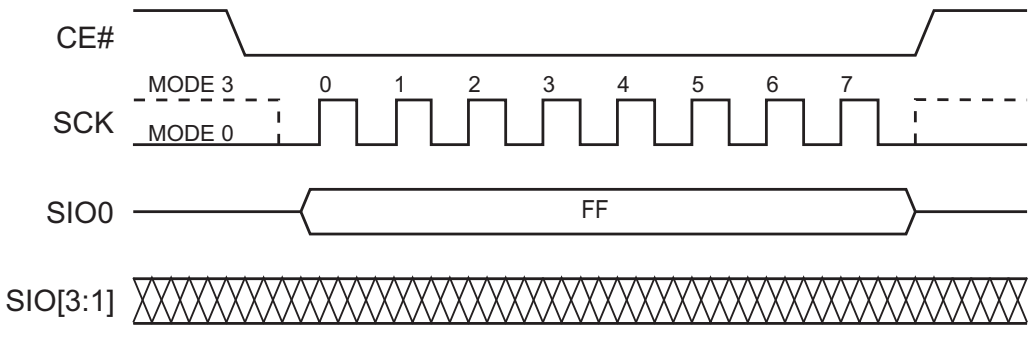
Note: SIO[3:1] must be driven VIH.

5.5 Reset Quad I/O (RSTQIO)

The Reset Quad I/O instruction, FFH, resets the device to 1-bit SPI protocol operation or exits the Set Mode configuration during a read sequence. This command allows the Flash device to return to the default I/O state (SPI) without a power cycle and executes in either 1-bit or 4-bit mode. If the device is in the Set Mode configuration, while in SQI High-Speed Read mode, the RSTQIO command will only return the device to a state where it can accept new command instruction. An additional RSTQIO is required to reset the device to SPI mode.

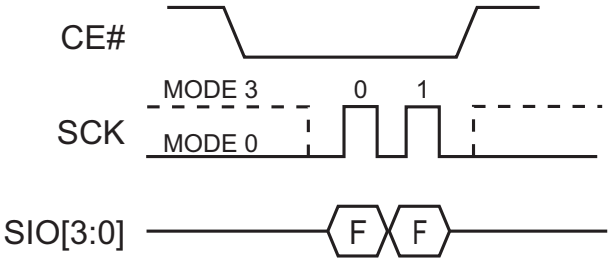
To execute a Reset Quad I/O operation, the host drives CE# low, sends the Reset Quad I/O command cycle (FFH) and then drives CE# high. Execute the instruction in either SPI (8 clocks) or SQI (2 clocks) command cycles. For SPI, SIO[3:1] are don’t care for this command, but should be driven to VIH or VIL (see Figure 5-4 and Figure 5-5).

FIGURE 5-4: RESET QUAD I/O SEQUENCE (SPI)



Note: SIO[3:1] must be driven VIH.

FIGURE 5-5: RESET QUAD I/O SEQUENCE (SQI)

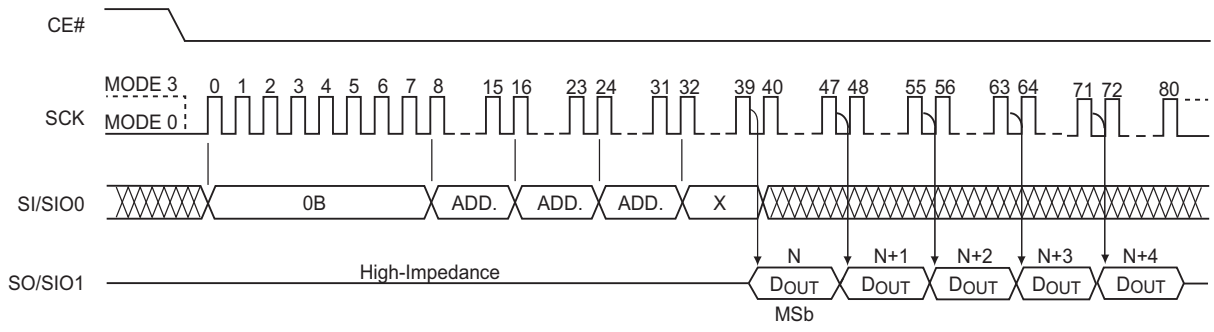


5.6 High-Speed Read

The High-Speed Read instruction, 0BH, is supported in both SPI bus protocol and SQI protocol. This instruction supports frequencies of up to 80 MHz. On power-up, the device is set to use SPI.

Initiate High-Speed Read by executing an 8-bit command, 0BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 5-6 for the High-Speed Read sequence for SPI bus protocol.

FIGURE 5-6: HIGH-SPEED READ SEQUENCE (SPI) (C[1:0] = 0BH)



In SQI protocol, the host drives CE# low and then sends the Read command cycle command, 0BH, followed by three address cycles, a Set Mode Configuration cycle and two dummy cycles. Each cycle is two nibbles (clocks) long, the most significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#.

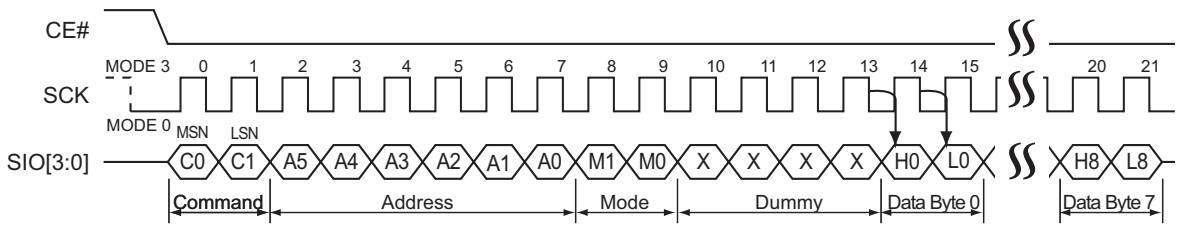
The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to address location 000000H. During this operation, blocks that are Read-locked will output data 00H.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SQI High-Speed Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another Read command, 0BH, and does not require the op-code to be entered again. The host may initiate the next Read cycle by driving CE# low, then sending the four-bits input for address A[23:0], followed by the Set Mode configuration bits M[7:0] and two dummy cycles.

After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command FFH. While in the Set Mode configuration, the RSTQIO command will only return the device to a state where it can accept new command instruction. An additional RSTQIO is required to reset the device to SPI mode. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

FIGURE 5-7: HIGH-SPEED READ SEQUENCE (SQI)



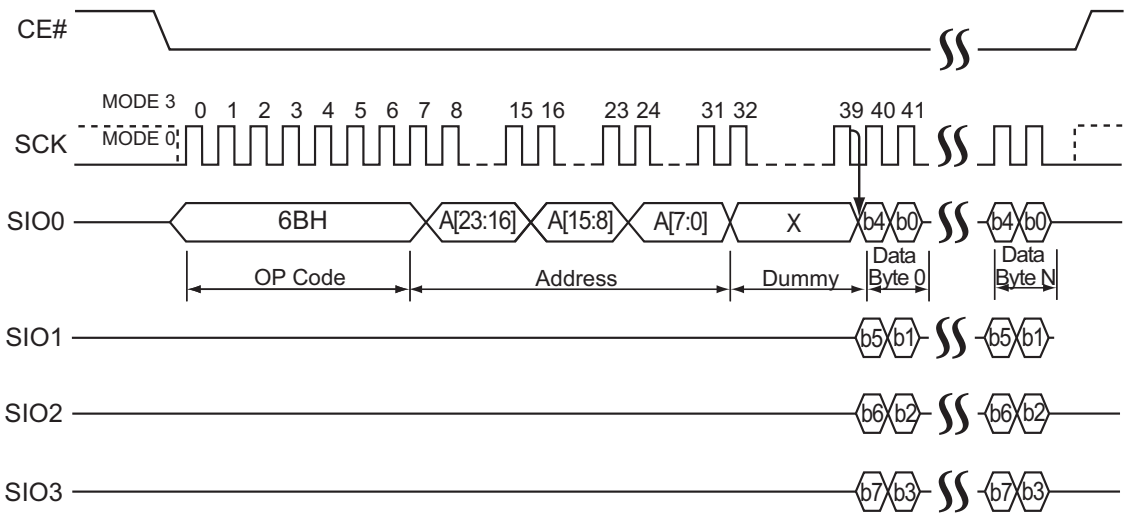
Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
Hx = High Data Nibble, Lx = Low Data Nibble C[1:0] = 0BH

5.7 SPI Quad Output Read

The SPI Quad Output Read instruction supports frequencies of up to 80 MHz. SST26LF064RT requires the IOC bit in the Configuration register to be set to '1' prior to executing the command. Initiate SPI Quad Output Read by executing an 8-bit command, 6BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active-low for the duration of the SPI Quad Mode Read. See Figure 5-8 for the SPI Quad Output Read sequence.

Following the dummy byte, the device outputs data from SIO[3:0], starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

FIGURE 5-8: SPI QUAD OUTPUT READ



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble

5.8 SPI Quad I/O Read

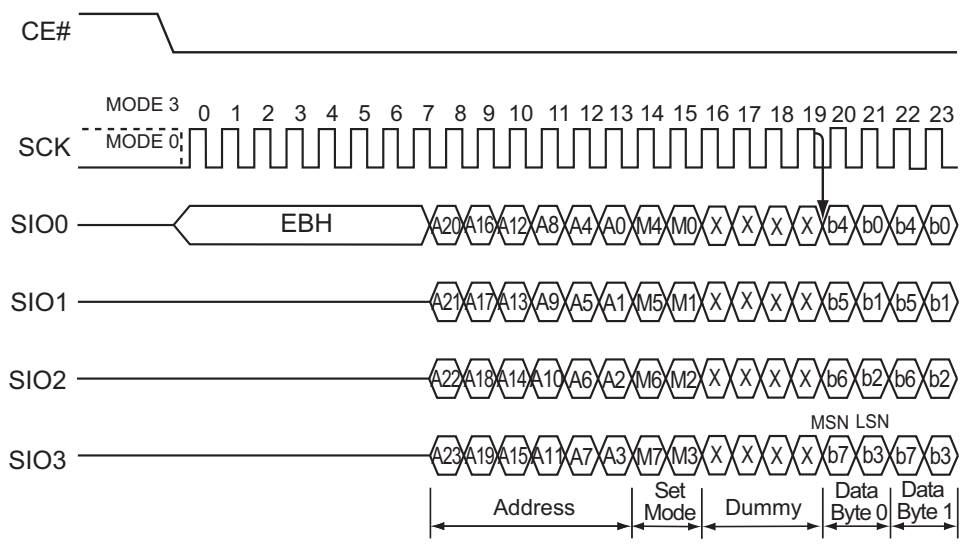
The SPI Quad I/O Read (SQIOR) instruction supports frequencies of up to 80 MHz. SST26LF064RT requires the IOC bit in the Configuration register to be set to '1' prior to executing the command. Initiate SQIOR by executing 8-bit command EBH. The device then switches to 4-bit I/O mode for address bits A[23-0], followed by the Set Mode configuration bits M[7:0] and two dummy bytes. CE# must remain active-low for the duration of the SPI Quad I/O Read. See Figure 5-9 for the SPI Quad I/O Read sequence.

Following the dummy bytes, the device outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Quad I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another Read command, EBH, and does not require the op-code to be entered again. The host may set the next SQIOR cycle by driving CE# low, then sending the four-bit wide input for address A[23:0], followed by the Set Mode configuration bits M[7:0] and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

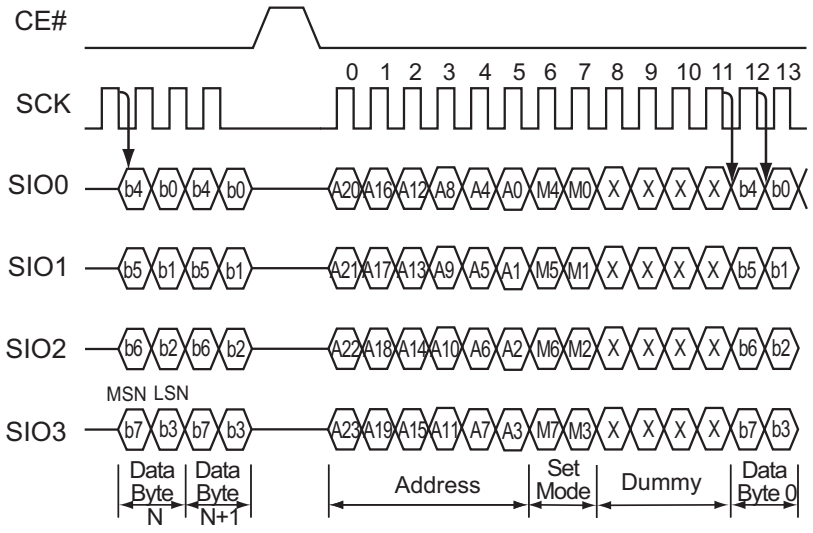
When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command FFH. See Figure 5-10 for the SPI Quad I/O mode Read sequence when M[7:0] = AXH.

FIGURE 5-9: SPI QUAD I/O READ SEQUENCE



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble

FIGURE 5-10: BACK-TO-BACK SPI QUAD I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble

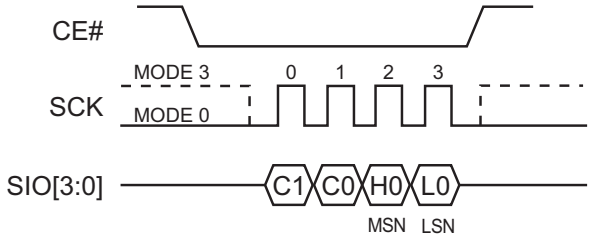
5.9 Set Burst

The Set Burst command specifies the number of bytes to be output during a Read Burst command before the device wraps around. It supports both SPI and SQI protocols. To set the burst length, the host drives CE# low, sends the Set Burst command cycle (C0H) and one data cycle and then drives CE# high. After power-up or Reset, the burst length is set to eight bytes (00H). See Table 5-2 for burst length data and Figures 5-11 and 5-12 for the sequences.

TABLE 5-2: BURST LENGTH DATA

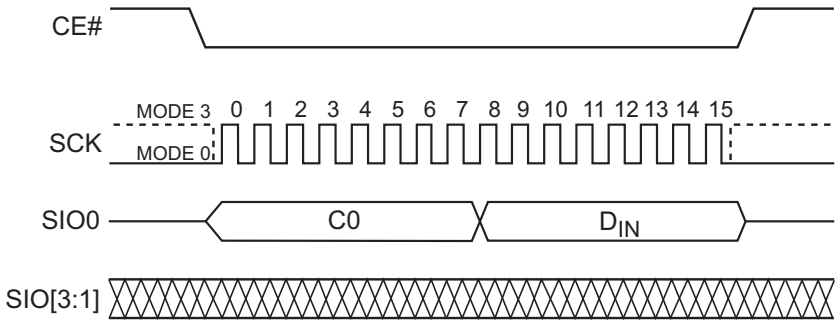
Burst Length	High Nibble (H0)	Low Nibble (L0)
8 Bytes	0h	0h
16 Bytes	0h	1h
32 Bytes	0h	2h
64 Bytes	0h	3h

FIGURE 5-11: SET BURST LENGTH SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0]=C0H

FIGURE 5-12: SET BURST LENGTH SEQUENCE (SPI)



Note: SIO[3:1] must be driven VIH.

5.10 SQI Read Burst with Wrap (RBSQI)

SQI Read Burst with wrap is similar to High-Speed Read in SQI mode, except data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SQI Read Burst operation, drive CE# low and send the Read Burst command cycle (0CH), followed by three address cycles and then three dummy cycles. Each cycle is two nibbles (clocks) long, the most significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During RBSQI, the internal Address Pointer automatically increments until the last byte of the burst is reached and then it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length (see Table 5-3). For example, if the burst length is eight bytes and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are read-locked will output data 00H.

5.11 SPI Read Burst with Wrap (RBSPI)

SPI Read Burst with Wrap (RBSPI) is similar to SPI Quad I/O Read, except the data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SPI Read Burst with Wrap operation, drive CE# low and then send the Read Burst command cycle (ECH), followed by three address cycles and then three dummy cycles.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During RBSPI, the internal Address Pointer automatically increments until the last byte of the burst is reached and then it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length (see Table 5-3). For example, if the burst length is eight bytes and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are read-locked will output data 00H.

TABLE 5-3: BURST ADDRESS RANGES

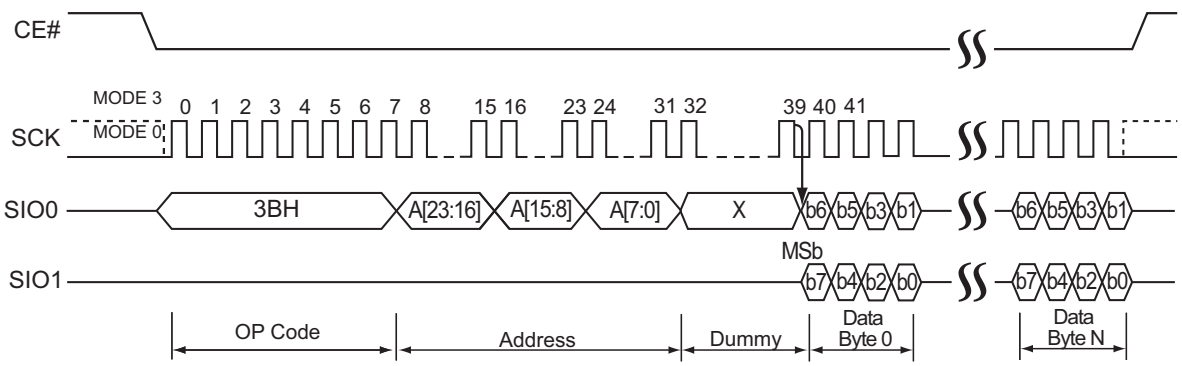
Burst Length	Burst Address Ranges
8 Bytes	00-07H, 08-0FH, 10-17H, 18-1FH...
16 Bytes	00-0FH, 10-1FH, 20-2FH, 30-3FH...
32 Bytes	00-1FH, 20-3FH, 40-5FH, 60-7FH...
64 Bytes	00-3FH, 40-7FH, 80-BFH, C0-FFH

5.12 SPI Dual Output Read

The SPI Dual Output Read instruction supports frequencies of up to 80 MHz. Initiate SPI Dual Output Read by executing an 8-bit command, 3BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active-low for the duration of the SPI Dual-Output Read operation. See Figure 5-13 for the SPI Quad Output Read sequence.

Following the dummy byte, the SST26LF064RT outputs data from SIO[1:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

FIGURE 5-13: FAST READ, DUAL OUTPUT SEQUENCE



Note: MSb = Most Significant bit

5.13 SPI Dual I/O Read

The SPI Dual I/O Read (SDIOR) instruction supports up to 80 MHz frequency. Initiate SDIOR by executing 8-bit command BBH. The device then switches to 2-bit I/O mode for address bits A[23-0], followed by the Set Mode configuration bits M[7:0]. CE# must remain active-low for the duration of the SPI Dual I/O Read. See Figure 5-14 for the SPI Dual I/O Read sequence.

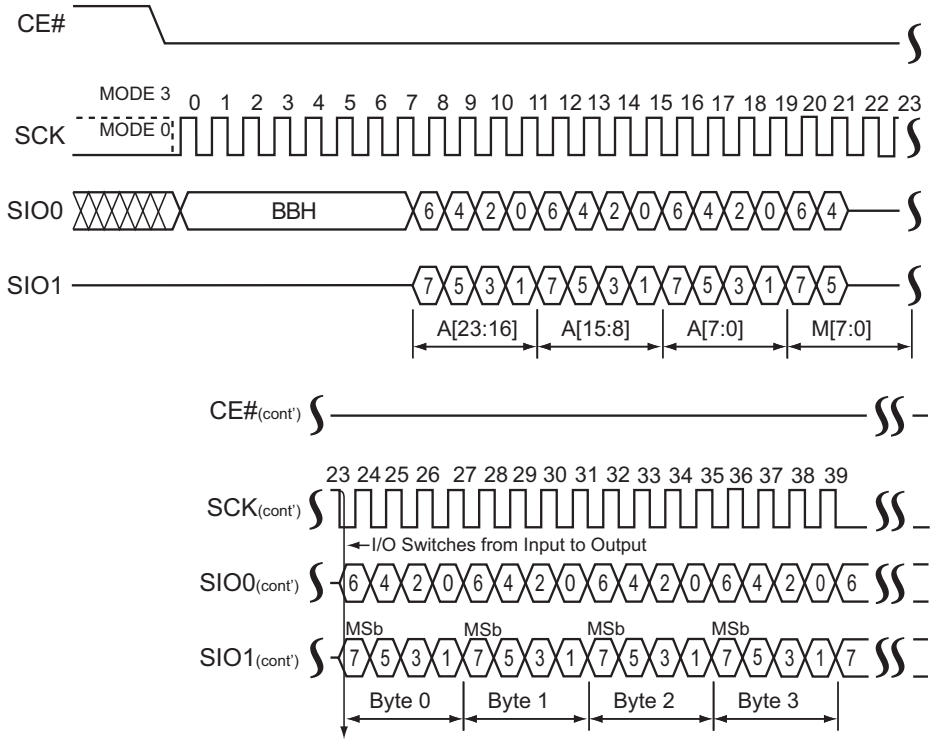
Following the Set Mode configuration bits, the SST26LF064RT outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached, at which point the Address Pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Dual I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another SDIOR command, BBH, and does not require the op-code to be entered again.

The host may set the next SDIOR cycle by driving CE# low, then sending the two-bit wide input for address A[23:0], followed by the Set Mode configuration bits M[7:0]. After the Set Mode configuration bits, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

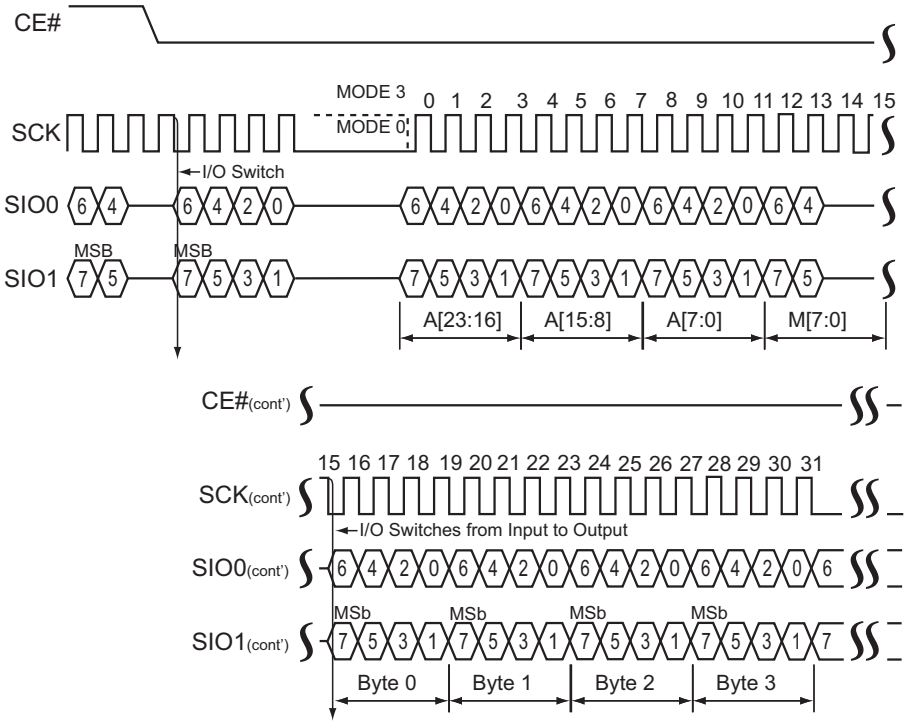
When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command FFH. See Figure 5-15 for the SPI Dual I/O Read sequence when M[7:0] = AXH.

FIGURE 5-14: SPI DUAL I/O READ SEQUENCE



Note: MSb = Most Significant bit, LSb = Least Significant bit

FIGURE 5-15: BACK-TO-BACK SPI DUAL I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSb = Most Significant bit, LSb = Least Significant bit

5.14 JEDEC-ID Read (SPI Protocol)

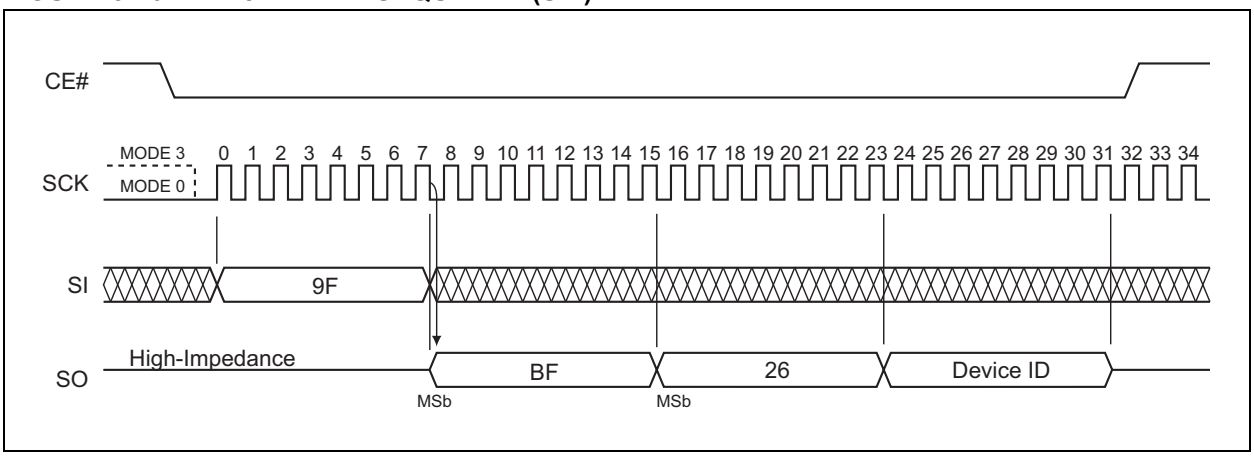
Using traditional SPI protocol, the JEDEC-ID Read instruction identifies the device as SST26LF064RT and the manufacturer as Microchip. To execute a JECEC-ID operation, the host drives CE# low and then sends the JEDEC-ID command cycle (9FH).

Immediately following the command cycle, SST26LF064RT output data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition on CE#. The device outputs three bytes of data: manufacturer, device type and device ID (see Table 5-4). For instruction sequence, see Figure 5-16.

TABLE 5-4: DEVICE ID DATA OUTPUT

Product	Manufacturer ID (Byte 1)	Device ID	
		Device Type (Byte 2)	Device ID (Byte 3)
SST26LF064RT	BFH	26H	43H

FIGURE 5-16: JEDEC-ID SEQUENCE (SPI)

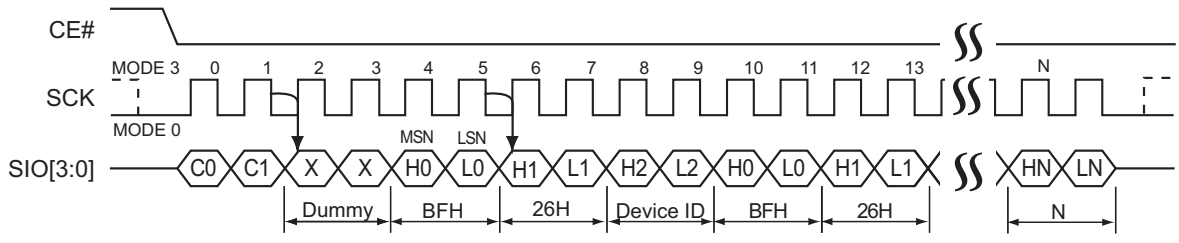


5.15 Read Quad J-ID Read (SQI Protocol)

The Read Quad J-ID Read instruction identifies the device as SST26LF064RT and manufacturer as Microchip. To execute a Quad J-ID operation, the host drives CE# low and then sends the Quad J-ID command cycle (AFH). Each cycle is two nibbles (clocks) long, the most significant nibble first.

Immediately following the command cycle and one dummy cycle, SST26LF064RT outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition of CE#. The device outputs three bytes of data: manufacturer, device type and device ID (see Table 5-4). For instruction sequence, see Figure 5-17.

FIGURE 5-17: QUAD J-ID READ SEQUENCE



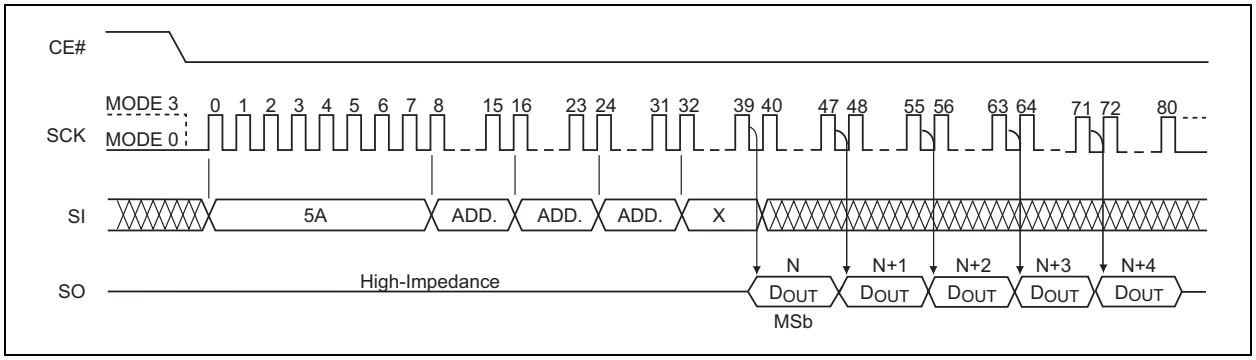
Note: MSN = Most significant Nibble, LSN= Least Significant Nibble, C{1:0] = AFH

5.16 Serial Flash Discoverable Parameters (SFDP)

The Serial Flash Discoverable Parameters (SFDP) contain information describing the characteristics of the device. This allows device-independent, JEDEC ID-independent and forward/backward compatible software support for all future Serial Flash device families.

Initiate SFDP by executing an 8-bit command, 5AH, followed by address bits A[23-0] and a dummy byte. CE# must remain active-low for the duration of the SFDP cycle. For the SFDP sequence, see Figure 5-18.

FIGURE 5-18: SERIAL FLASH DISCOVERABLE PARAMETERS SEQUENCE



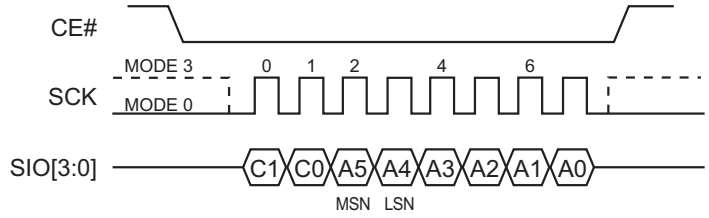
5.17 Sector Erase

The Sector Erase instruction clears all bits in the selected 4 Kbyte sector to '1,' but it does not change a protected memory area. Prior to any write operation, the Write Enable (WREN) instruction must be executed.

To execute a Sector Erase operation, the host drives CE# low, sends the Sector Erase command cycle (20H) and three address cycles and then drives CE# high.

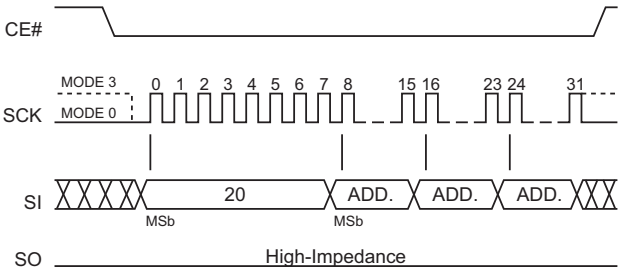
Address bits [AMS:A12] (AMS = Most Significant Address) determine the sector address (SAX); the remaining address bits can be VIL or VIH. To identify the completion of the internal, self-timed, Write operation poll the BUSY bit in the STATUS register or wait TSE. See Figure 5-19 and Figure 5-20 for the Sector Erase sequence.

FIGURE 5-19: 4-KBYTE SECTOR ERASE SEQUENCE – SQI MODE



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = 20H

FIGURE 5-20: 4-KBYTE SECTOR ERASE SEQUENCE (SPI)

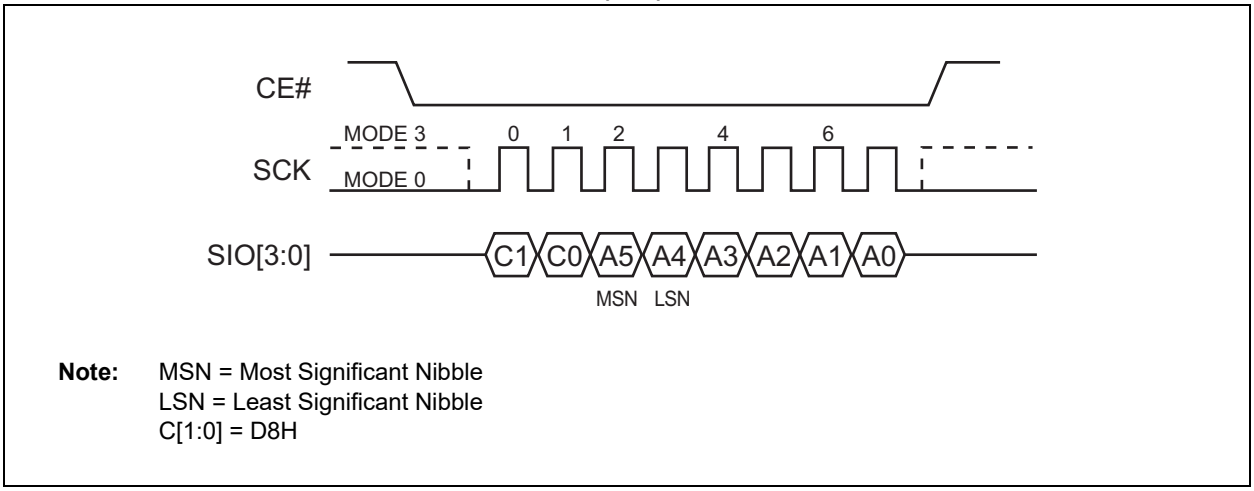


5.18 Block Erase

The Block Erase instruction clears all bits in the selected block to '1'. Block sizes can be 8 Kbytes, 32 Kbytes or 64 Kbytes depending on the address (see Figure 3-1 for details). A Block Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, execute the WREN instruction. Keep CE# active-low for the duration of any command sequence.

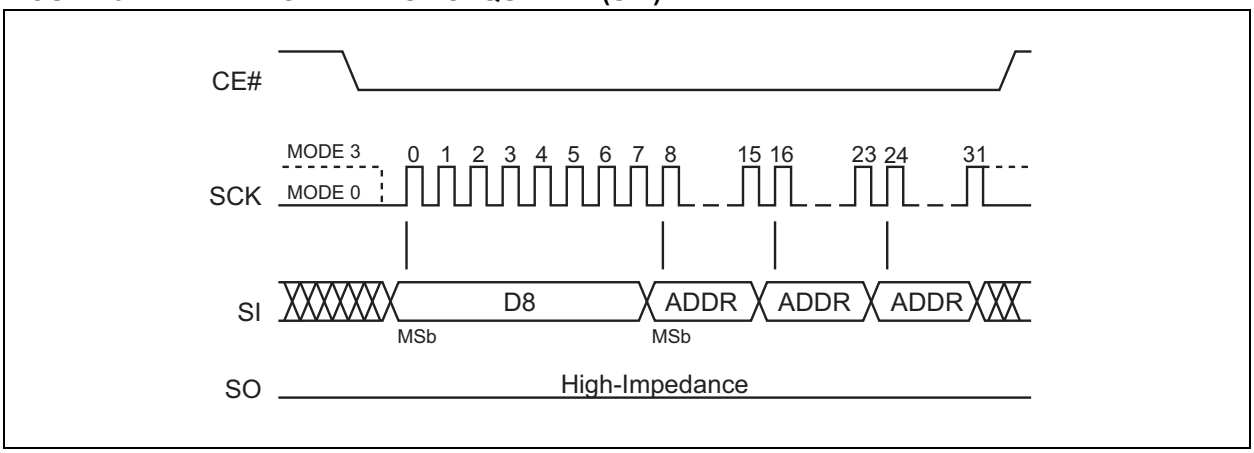
To execute a Block Erase operation, the host drives CE# low, sends the Block Erase command cycle (D8H) and three address cycles and then drives CE# high. Address bits, AMS-A13, determine the block address (BAX); the remaining address bits can be VIL or VIH. For 32-Kbyte blocks, A14:A13 can be VIL or VIH; for 64-Kbyte blocks, A15:A13 can be VIL or VIH. Poll the BUSY bit in the STATUS register or wait TBE for the completion of the internal, self-timed Block Erase operation. See Figure 5-21 and Figure 5-22 for the Block Erase sequence.

FIGURE 5-21: BLOCK ERASE SEQUENCE (SQI)



Note: MSN = Most Significant Nibble
LSN = Least Significant Nibble
C[1:0] = D8H

FIGURE 5-22: BLOCK ERASE SEQUENCE (SPI)

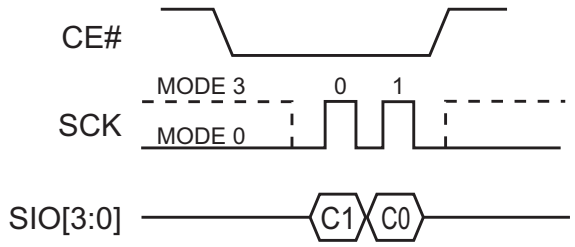


5.19 Chip Erase

The Chip Erase instruction clears all bits in the device to '1.' The Chip Erase instruction is ignored if any of the memory area is protected. Prior to any write operation, execute the WREN instruction.

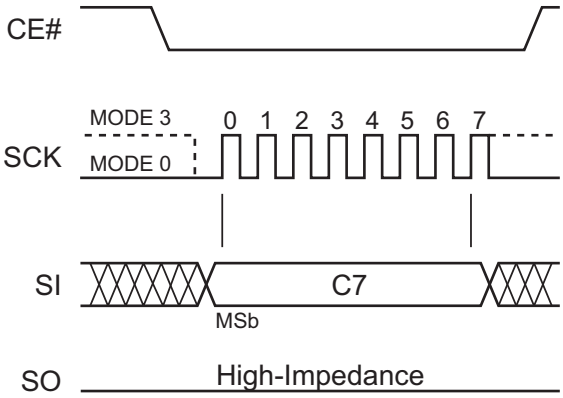
To execute a Chip Erase operation, the host drives CE# low, sends the Chip Erase command cycle (C7H) and then drives CE# high. Poll the BUSY bit in the STATUS register or wait TSCE for the completion of the internal, self-timed Write operation. See Figure 5-23 and Figure 5-24 for the Chip Erase sequence.

FIGURE 5-23: CHIP ERASE SEQUENCE (SQI)



Note: C[1:0] = C7H

FIGURE 5-24: CHIP ERASE SEQUENCE (SPI)



5.20 Page Program

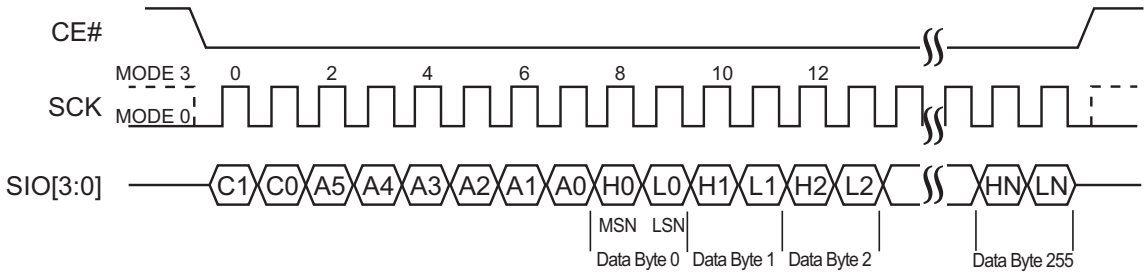
The Page Program instruction programs up to 256 bytes of data in the memory and supports both SPI and SQI protocols. The data for the selected page address must be in the erased state (FFH) before initiating the Page Program operation. A Page Program applied to a protected memory area will be ignored. Prior to the program operation, execute the WREN instruction.

To execute a Page Program operation, the host drives CE# low, sends the Page Program command cycle (02H) three address cycles, followed by the data to be programmed and then drives CE# high. The programmed data must be between 1 to 256 bytes and in whole byte increments; sending less than a full byte will cause the partial byte to be ignored.

Poll the BUSY bit in the STATUS register or wait TPP for the completion of the internal, self-timed Write operation. See Figure 5-25 and Figure 5-26 for the Page Program sequence.

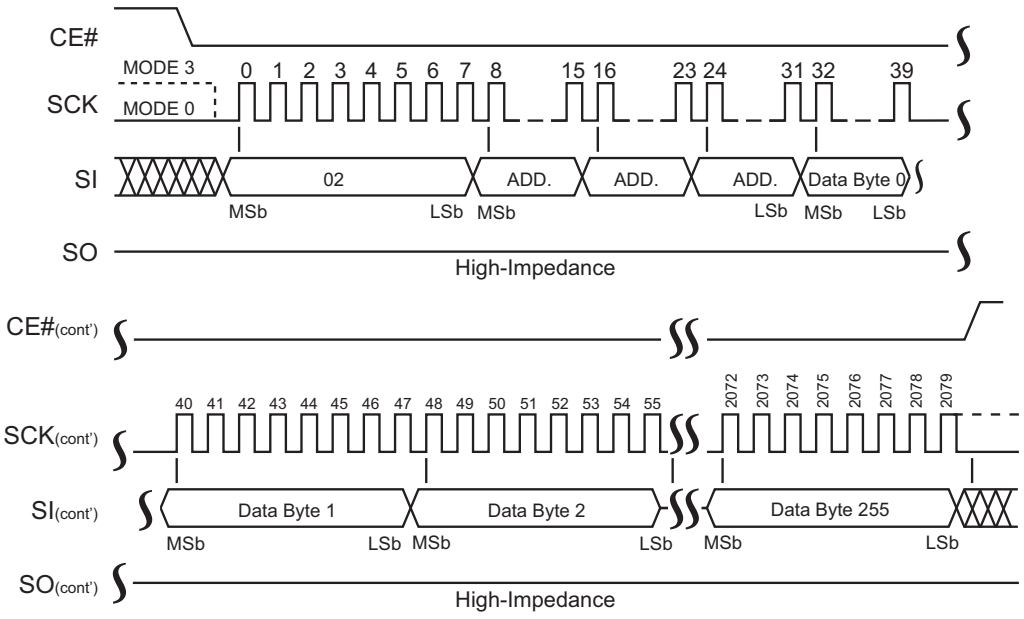
When executing Page Program, the memory range for the SST26LF064RT is divided into 256-byte page boundaries. The device handles shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the Page Program instruction is not the beginning of the page boundary (A[7:0] are not all zero) and the number of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

FIGURE 5-25: PAGE PROGRAM SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
C[1:0] = 02H

FIGURE 5-26: PAGE PROGRAM SEQUENCE (SPI)



5.21 SPI Quad Page Program

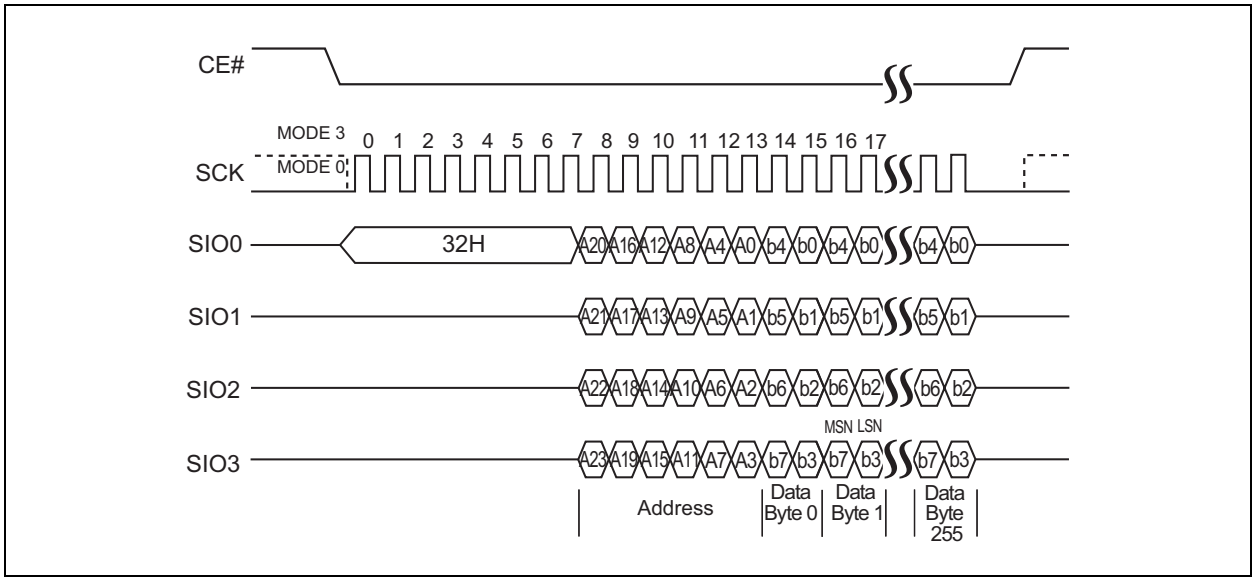
The SPI Quad Page Program instruction programs up to 256 bytes of data in the memory. The data for the selected page address must be in the erased state (FFH) before initiating the SPI Quad Page Program operation. A SPI Quad Page Program applied to a protected memory area will be ignored. SST26LF064RT requires the ICO bit in the Configuration register to be set to '1' prior to executing the command. Prior to the program operation, execute the WREN instruction.

To execute a SPI Quad Page Program operation, the host drives CE# low, sends the SPI Quad Page Program command cycle (32H) three address cycles, followed by the data to be programmed and then drives CE# high. The programmed data must be between 1 to 256 bytes and in whole byte increments.

The command cycle is eight clocks long while the address and data cycles are each two clocks long, Most Significant bit first. Poll the BUSY bit in the STATUS register or wait TPP for the completion of the internal, self-timed Write operation (see Figure 5-27).

When executing SPI Quad Page Program, the memory range for the SST26LF064RT is divided into 256-byte page boundaries. The device handles shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the SPI Quad Page Program instruction is not the beginning of the page boundary (A[7:0] are not all zero) and the of bytes of data input exceed or overlap the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

FIGURE 5-27: SPI QUAD PAGE PROGRAM SEQUENCE



5.22 Write Suspend and Write Resume

Write Suspend allows the interruption of Sector Erase, Block Erase, SPI Quad Page Program or Page Program operations in order to erase, program or read data in another portion of memory. The original operation can be continued with the Write Resume command. This operation is supported in both SQI and SPI protocols.

Only one write operation can be suspended at a time; if an operation is already suspended, the device will ignore the Write Suspend command. Write Suspend during Chip Erase is ignored; Chip Erase is not a valid command while a write is suspended. The Write Resume command is ignored until any write operation (Program or Erase) initiated during the Write Suspend is complete. The device requires a minimum of 500 µs between each Write Suspend command.

5.23 Write Suspend During Sector Erase or Block Erase

Issuing a Write Suspend instruction during Sector Erase or Block Erase allows the host to program or read any sector that was not being erased. The device will ignore any programming commands pointing to the suspended sector(s). Any attempt to read from the suspended sector(s) will output unknown data because the Sector or Block Erase will be incomplete.

To execute a Write Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H) and then drives CE# high. The STATUS register indicates that the erase has been suspended by changing the WSE bit from '0' to '1,' but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the STATUS register or wait TWS.

5.24 Write Suspend During Page Programming or SPI Quad Page Programming

Issuing a Write Suspend instruction during Page Programming allows the host to erase or read any sector that is not being programmed. Erase commands pointing to the suspended sector(s) will be ignored. Any attempt to read from the suspended page will output unknown data because the program will be incomplete.

To execute a Write Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H) and then drives CE# high. The STATUS register indicates that the programming has been suspended by changing the WSP bit from '0' to '1,' but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the STATUS register or wait TWS.

5.25 Write Resume

Write Resume restarts a Write command that was suspended and changes the suspend status bit in the STATUS register (WSE or WSP) back to '0'.

To execute a Write Resume operation, the host drives CE# low, sends the Write Resume command cycle (30H) and then drives CE# high. To determine if the internal, self-timed Write operation is completed, poll the BUSY bit in the STATUS register or wait the specified time TSE, TBE or TPP for Sector Erase, Block Erase or Page Programming, respectively. The total write time before suspend and after resume will not exceed the uninterrupted write times TSE, TBE or TPP.

5.26 Read Security ID

The Read Security ID operation is supported in both SPI and SQI modes. To execute a Read Security ID (SID) operation in SPI mode, the host drives CE# low and then sends the Read Security ID command cycle (88H), two address cycles and one dummy cycle.

To execute a Read Security ID operation in SQI mode, the host drives CE# low and then sends the Read Security ID command, two address cycles and three dummy cycles.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal, starting from the specified address location. The data output stream is continuous through all SID addresses until terminated by a low-to-high transition on CE#. See Table 5-5 for the Security ID address range.

5.27 Program Security ID

The Program Security ID instruction programs one to 2040 bytes of data in the user-programmable, Security ID space. This Security ID space is One-Time-Programmable (OTP). The device ignores a Program Security ID instruction pointing to an invalid or protected address (see Table 5-5). Prior to the program operation, execute WREN.

To execute a Program SID operation, the host drives CE# low, sends the Program Security ID command cycle (A5H), two address cycles, the data to be programmed and then drives CE# high. The programmed data must be between 1 to 256 bytes and in whole byte increments.

The device handles shifting of more than 256 bytes of data by maintaining the last 256 bytes of data as the correct data to be programmed. If the target address for the Program Security ID instruction is not the beginning of the page boundary and the number of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

The Program Security ID operation is supported in both SPI and SQI mode. To determine the completion of the internal, self-timed Program SID operation, poll the BUSY bit in the software STATUS register or wait TPSID for the completion of the internal self-timed Program Security ID operation.

TABLE 5-5: PROGRAM SECURITY ID

Program Security ID	Address Range
Unique ID Pre-Programmed at Factory	0000–0007H
User Programmable	0008H–07FFH

5.28 Lockout Security ID

The Lockout Security ID instruction prevents any future changes to the Security ID and is supported in both SPI and SQI modes. Prior to the operation, execute WREN.

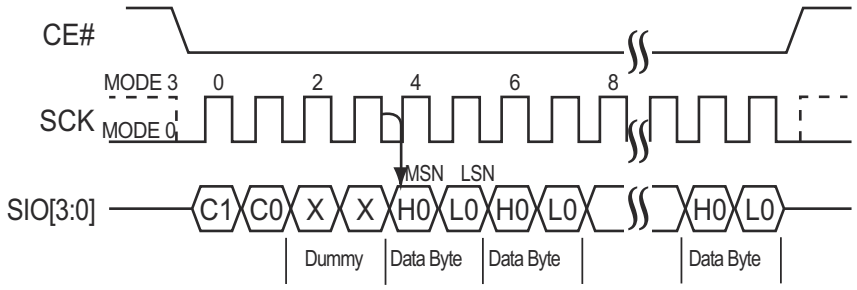
To execute a Lockout SID, the host drives CE# low, sends the Lockout Security ID command cycle (85H) and then drives CE# high. Poll the BUSY bit in the software STATUS register or wait TPSID for the completion of the Lockout Security ID operation.

5.29 Read STATUS Register (RDSR) and Read Configuration Register (RDCR)

The Read STATUS Register (RDSR) and Read Configuration Register (RDCR) commands output the contents of the STATUS and Configuration registers. These commands function in both SPI and SQI modes. The STATUS register can be read at any time, even during a write operation. When a write is in progress, poll the BUSY bit before sending any new commands to assure that the new commands are properly received by the device.

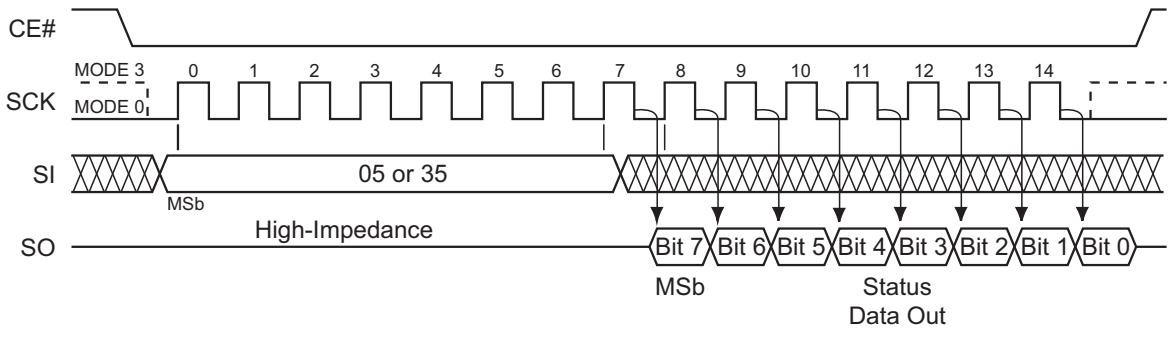
To read the STATUS or Configuration registers, the host drives CE# low and then sends the Read STATUS Register command cycle (05H) or the Read Configuration Register command (35H). A dummy cycle is required in SQI mode. Immediately after the command cycle, the device outputs data on the falling edge of the SCK signal. The data output stream continues until terminated by a low-to-high transition on CE#. See Figure 5-28 and Figure 5-29 for the instruction sequence.

FIGURE 5-28: READ STATUS REGISTER AND READ CONFIGURATION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0]=05H or 35H

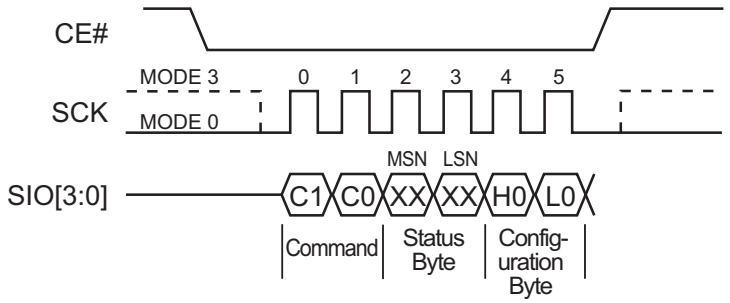
FIGURE 5-29: READ STATUS REGISTER AND READ CONFIGURATION REGISTER SEQUENCE (SPI)



5.30 Write STATUS Register (WRSR)

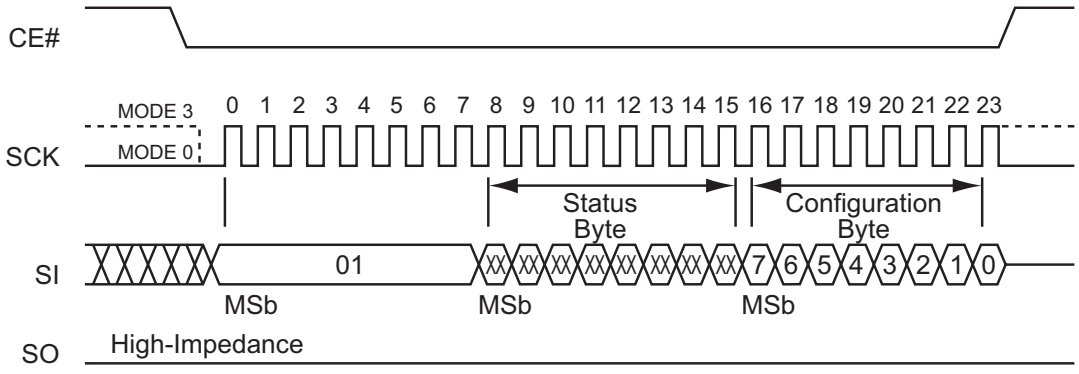
The Write STATUS Register (WRSR) command writes new values to the Configuration register. To execute a Write STATUS Register operation, the host drives CE# low, sends the Write STATUS Register command cycle (01H) and two cycles of data and then drives CE# high. Values in the second data cycle will be accepted by the device (see Figure 5-30 and Figure 5-31).

FIGURE 5-30: WRITE STATUS REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, XX = Don't Care, C[1:0]=01H

FIGURE 5-31: WRITE STATUS REGISTER SEQUENCE (SPI)



Note: XX = Don't Care

5.31 Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch bit in the STATUS register to '1,' allowing write operations to occur. The WREN instruction must be executed prior to any of the following operations: Sector Erase, Block Erase, Chip Erase, Page Program, Program Security ID, Lockout Security ID, Write Block Protection Register, Lock Down Block Protection Register, Nonvolatile Write Lock Lock-Down Register, SPI Quad Page program and Write STATUS Register. To execute a write enable, the host drives CE# low, sends the Write Enable command cycle (06H) and then drives CE# high. See Figure 5-32 and Figure 5-33 for the WREN instruction sequence.

FIGURE 5-32: WRITE ENABLE SEQUENCE (SQI)

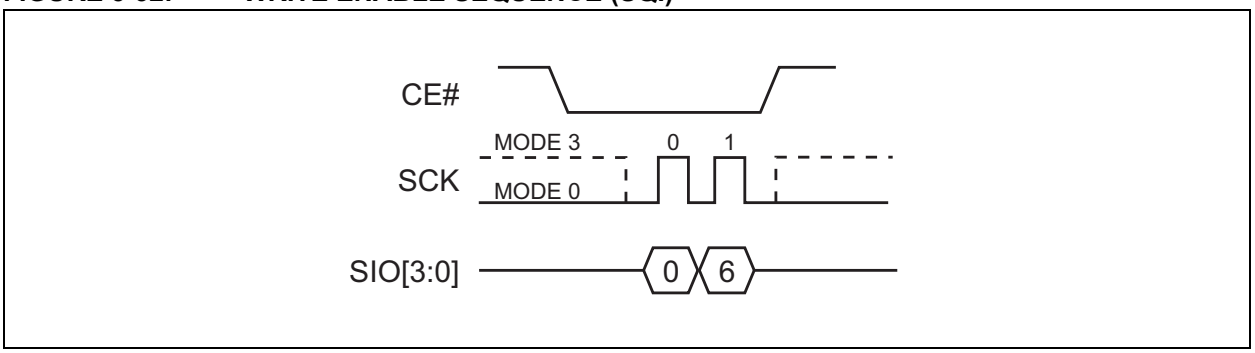
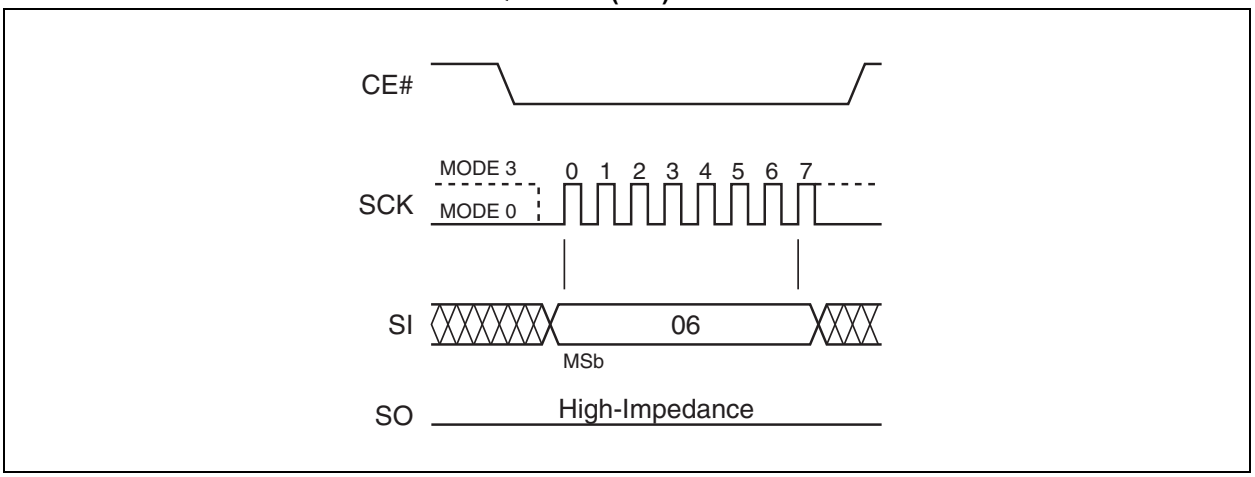


FIGURE 5-33: WRITE ENABLE SEQUENCE (SPI)



5.32 Write Disable (WRDI)

The Write Disable (WRDI) instruction sets the Write Enable Latch bit in the STATUS register to '0', preventing write operations. The WRDI instruction is ignored during any internal write operations. Any write operation started before executing WRDI will complete. Drive CE# high before executing WRDI.

To execute a Write Disable, the host drives CE# low, sends the Write Disable command cycle (04H) and then drives CE# high (see Figure 5-34 and Figure 5-35).

FIGURE 5-34: WRITE DISABLE (WRDI) SEQUENCE (SQI)

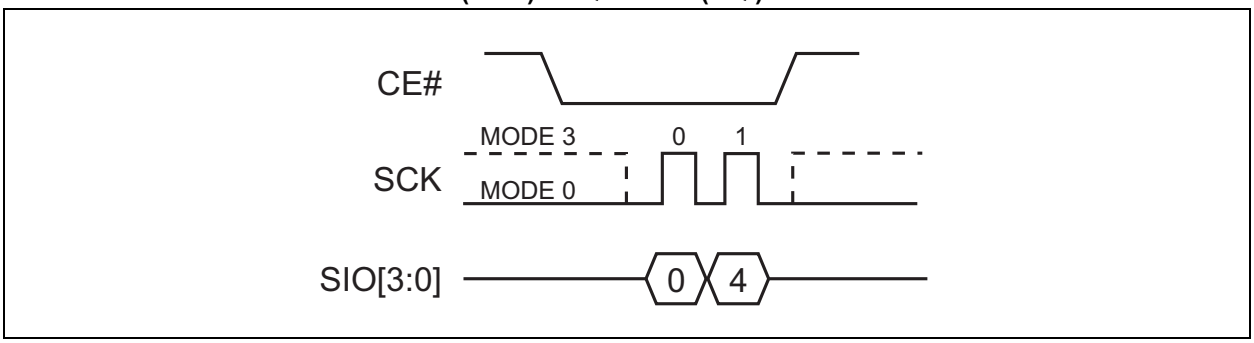
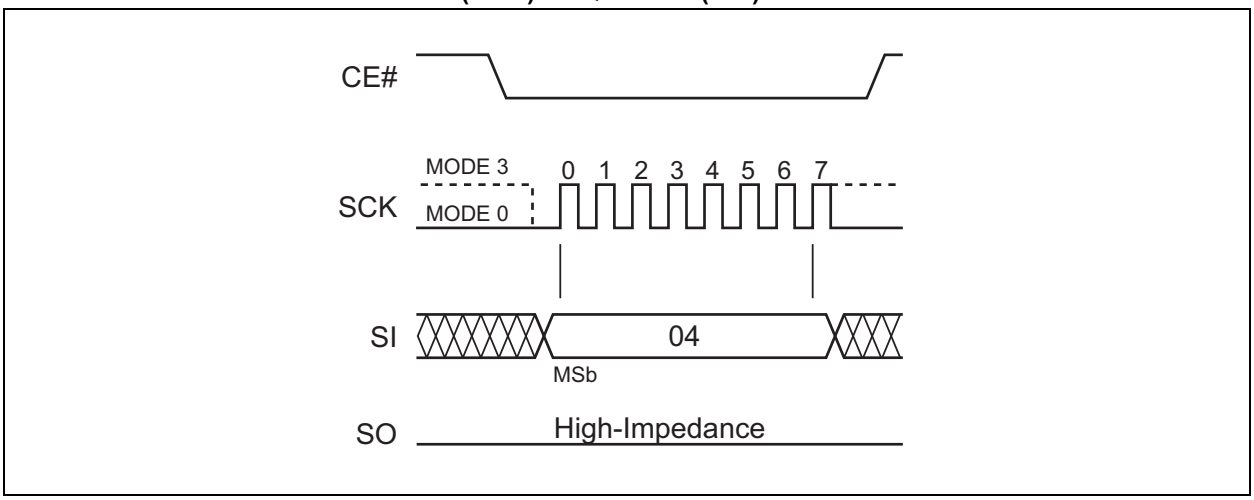


FIGURE 5-35: WRITE DISABLE (WRDI) SEQUENCE (SPI)

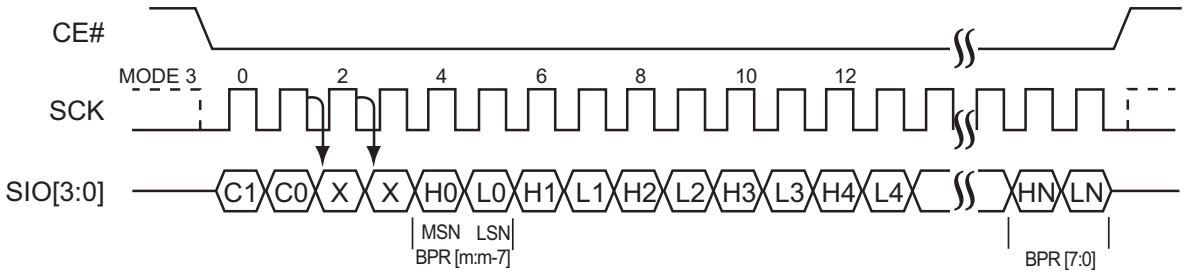


5.33 Read Block Protection Register (RBPR)

The Read Block Protection Register instruction outputs the Block Protection register data that determine the protection status. To execute a Read Block Protection Register operation, the host drives CE# low and then sends the Read Block Protection Register command cycle (72H). A dummy cycle is required in SQI mode.

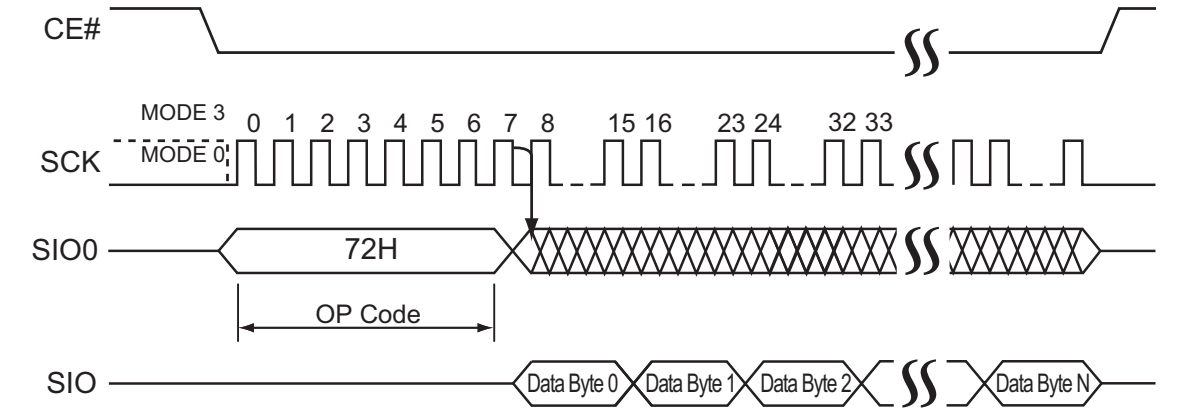
After the command cycle, the device outputs data on the falling edge of the SCK signal starting with the Most Significant bit(s). See Table 5-6 for definitions of each bit in the Block Protection register. The RBPR command does not wrap around. After all data have been output, the device will output 0H until terminated by a low-to-high transition on CE# (see Figure 5-36 and Figure 5-37).

FIGURE 5-36: READ BLOCK PROTECTION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, Block Protection Register (BPR), m = 143 for SST26LF064RT, C[1:0]=72H

FIGURE 5-37: READ BLOCK PROTECTION REGISTER SEQUENCE (SPI)

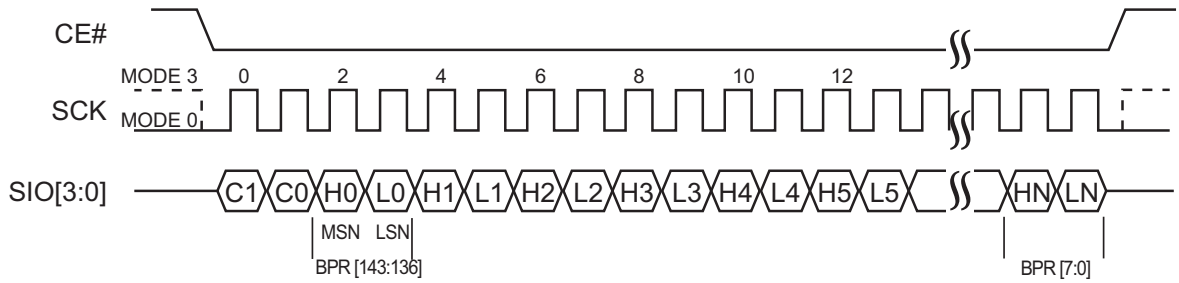


5.34 Write Block Protection Register (WBPR)

The Write Block Protection Register (WBPR) command changes the Block Protection register data to indicate the protection status. Execute WREN before executing WBPR.

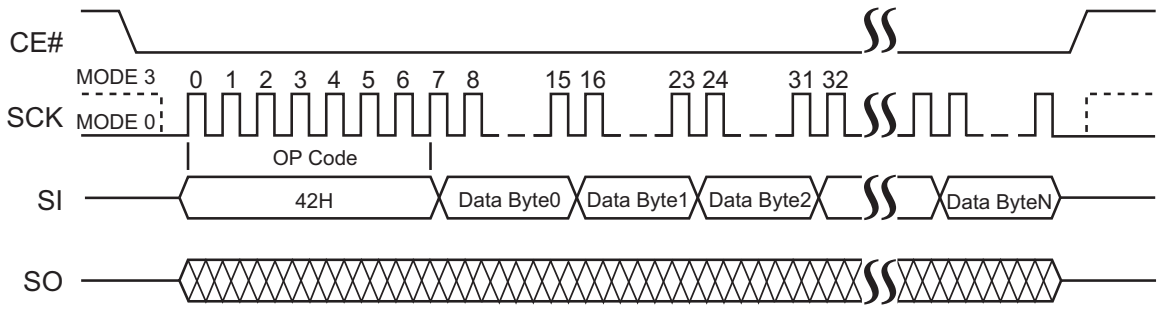
To execute a Write Block Protection Register operation, the host drives CE# low, sends the Write Block Protection Register command cycle (42H), sends 18 cycles of data and finally drives CE# high. Data input must be Most Significant bit(s) first. See Table 5-6 for definitions of each bit in the Block Protection register and also refer to Figures 5-38 and 5-39.

FIGURE 5-38: WRITE BLOCK PROTECTION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, Block Protection Register (BPR), C[1:0]=42H

FIGURE 5-39: WRITE BLOCK PROTECTION REGISTER SEQUENCE (SPI)



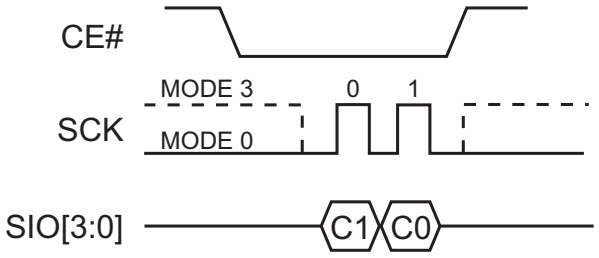
Note: C[1:0]=42H

5.35 Lock Down Block Protection Register (LBPR)

The Lock Down Block Protection Register instruction prevents changes to the Block Protection register during device operation. Lock Down resets after power cycling; this allows the Block Protection register to be changed. Execute WREN before initiating the Lock Down Block Protection Register instruction.

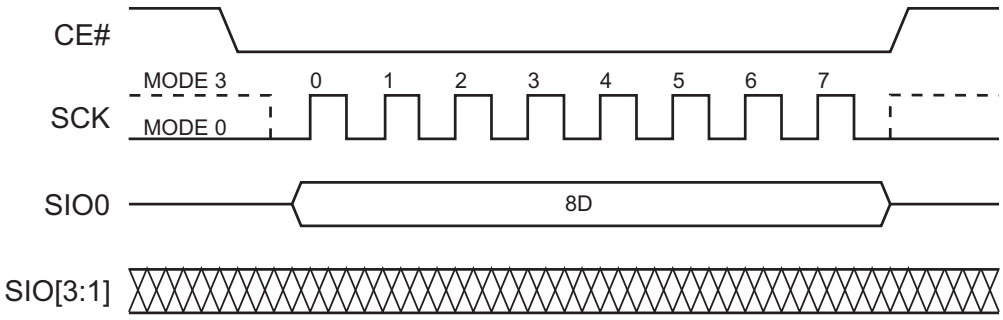
To execute a Lock Down Block Protection Register, the host drives CE# low, sends the Lock Down Block Protection Register command cycle (8DH) and then drives CE# high.

FIGURE 5-40: LOCK DOWN BLOCK PROTECTION REGISTER (SQI)



Note: C[1:0]=8DH

FIGURE 5-41: LOCK DOWN BLOCK PROTECTION REGISTER (SPI)



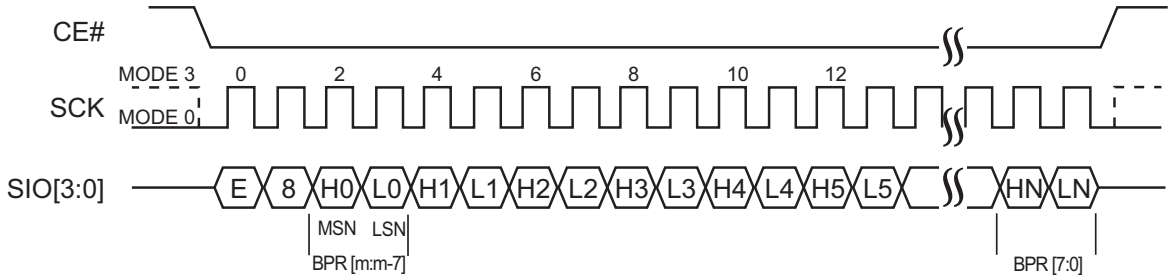
5.36 Nonvolatile Write Lock Lock-Down Register (nVWLDR)

The Nonvolatile Write Lock Lock-Down Register (nVWLDR) instruction controls the ability to change the Write Lock bits in the Block Protection register. Execute WREN before initiating the nVWLDR instruction.

To execute nVWLDR, the host drives CE# low, sends the nVWLDR command cycle (E8H), followed by 18 cycles of data and then drives CE# high.

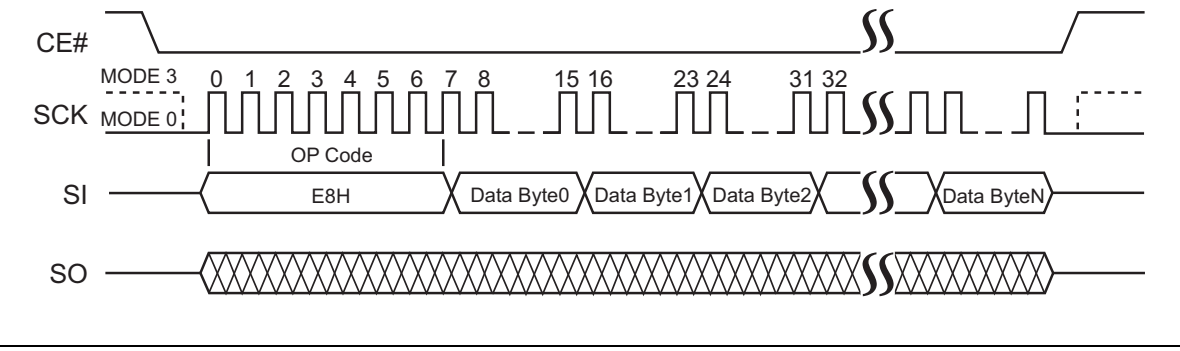
After CE# goes high, the nonvolatile bits are programmed and the programming time-out must complete before any additional commands (other than Read STATUS Register) can be entered. Poll the BUSY bit in the STATUS register or wait TPP for the completion of the internal, self-timed Write operation. Data inputs must be Most Significant bit(s) first.

FIGURE 5-42: WRITE LOCK LOCK-DOWN REGISTER SEQUENCE (SQI)



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble, Write-Lock Lock-Down Register (nVWLDR) m = 143

FIGURE 5-43: WRITE LOCK LOCK-DOWN REGISTER SEQUENCE (SPI)

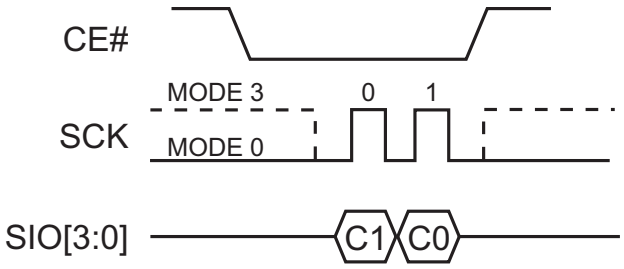


5.37 Global Block Protection Unlock (ULBPR)

The Global Block Protection Unlock (ULBPR) instruction clears all write protection bits in the Block Protection register, except for those bits that have been locked down with the nVWLDR command. Execute WREN before initiating the ULBPR instruction.

To execute a ULBPR instruction, the host drives CE# low, sends the ULBPR command cycle (98H) and then drives CE# high.

FIGURE 5-44: GLOBAL BLOCK PROTECTION UNLOCK (SQI)



Note: C[1:0]=98H

FIGURE 5-45: GLOBAL BLOCK PROTECTION UNLOCK (SPI)

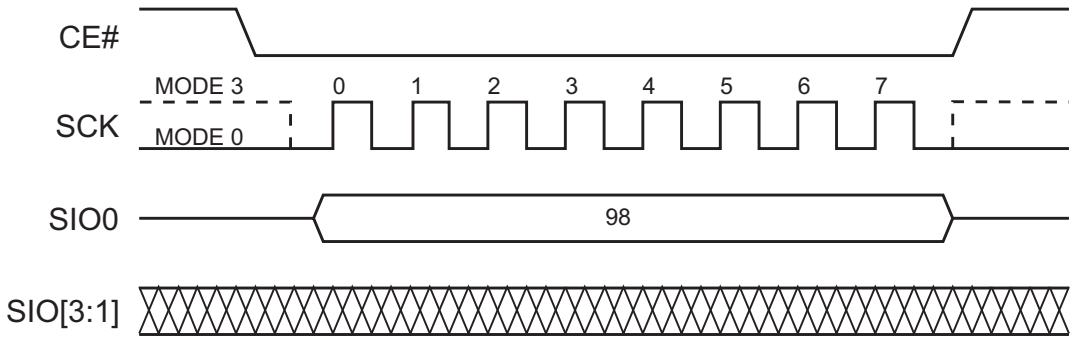


TABLE 5-6: BLOCK PROTECTION REGISTER FOR SST26LF064RT (1 OF 4)[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock/nVWLDR[2]		
143	142	7FE000H-7FFFFFH	8 Kbytes
141	140	7FC000H-7FDFFFH	8 Kbytes
139	138	7FA000H-7FBFFFH	8 Kbytes
137	136	7F8000H-7F9FFFH	8 Kbytes
135	134	006000H-007FFFH	8 Kbytes
133	132	004000H-005FFFH	8 Kbytes
131	130	002000H-003FFFH	8 Kbytes
129	128	000000H-001FFFH	8 Kbytes
	127	7F0000H-7F7FFFH	32 Kbytes
	126	008000H-00FFFFH	32 Kbytes
	125	7E0000H-7EFFFFH	64 Kbytes
	124	7D0000H-7DFFFFH	64 Kbytes
	123	7C0000H-7CFFFFH	64 Kbytes
	122	7B0000H-7BFFFFH	64 Kbytes
	121	7A0000H-7AFFFFH	64 Kbytes
	120	790000H-79FFFFH	64 Kbytes
	119	780000H-78FFFFH	64 Kbytes
	118	770000H-77FFFFH	64 Kbytes
	117	760000H-76FFFFH	64 Kbytes
	116	750000H-75FFFFH	64 Kbytes
	115	740000H-74FFFFH	64 Kbytes
	114	730000H-73FFFFH	64 Kbytes
	113	720000H-72FFFFH	64 Kbytes
	112	710000H-71FFFFH	64 Kbytes
	111	700000H-70FFFFH	64 Kbytes
	110	6F0000H-6FFFFFH	64 Kbytes
	109	6E0000H-6EFFFFH	64 Kbytes
	108	6D0000H-6DFFFFH	64 Kbytes
	107	6C0000H-6CFFFFH	64 Kbytes
	106	6B0000H-6BFFFFH	64 Kbytes
	105	6A0000H-6AFFFFH	64 Kbytes
	104	690000H-69FFFFH	64 Kbytes
	103	680000H-68FFFFH	64 Kbytes
	102	670000H-67FFFFH	64 Kbytes
	101	660000H-66FFFFH	64 Kbytes
	100	650000H-65FFFFH	64 Kbytes
	99	640000H-64FFFFH	64 Kbytes
	98	630000H-63FFFFH	64 Kbytes
	97	620000H-62FFFFH	64 Kbytes
	96	610000H-61FFFFH	64 Kbytes

Note 1: The default state after a power-on Reset is write-protected BPR[143:0] = 5555 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF.

2: nVWLDR bits are One-Time-Programmable. Once a nVWLDR bit is set, the protection state of that particular block is permanently write-locked.

TABLE 5-6: BLOCK PROTECTION REGISTER FOR SST26LF064RT (CONTINUED) (2 OF 4)[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock/nVWLDR[2]		
	95	600000H-60FFFFH	64 Kbytes
	94	5F0000H-5FFFFFH	64 Kbytes
	93	5E0000H-5EFFFFH	64 Kbytes
	92	5D0000H-5DFFFFH	64 Kbytes
	91	5C0000H-5CFFFFH	64 Kbytes
	90	5B0000H-5BFFFFH	64 Kbytes
	89	5A0000H-5AFFFFH	64 Kbytes
	88	590000H-59FFFFH	64 Kbytes
	87	580000H-58FFFFH	64 Kbytes
	86	570000H-57FFFFH	64 Kbytes
	85	560000H-56FFFFH	64 Kbytes
	84	550000H-55FFFFH	64 Kbytes
	83	540000H-54FFFFH	64 Kbytes
	82	530000H-53FFFFH	64 Kbytes
	81	520000H-52FFFFH	64 Kbytes
	80	510000H-51FFFFH	64 Kbytes
	79	500000H-50FFFFH	64 Kbytes
	78	4F0000H-4FFFFFH	64 Kbytes
	77	4E0000H-4EFFFFH	64 Kbytes
	76	4D0000H-4DFFFFH	64 Kbytes
	75	4C0000H-4CFFFFH	64 Kbytes
	74	4B0000H-4BFFFFH	64 Kbytes
	73	4A0000H-4AFFFFH	64 Kbytes
	72	490000H-49FFFFH	64 Kbytes
	71	480000H-48FFFFH	64 Kbytes
	70	470000H-47FFFFH	64 Kbytes
	69	460000H-46FFFFH	64 Kbytes
	68	450000H-45FFFFH	64 Kbytes
	67	440000H-44FFFFH	64 Kbytes
	66	430000H-43FFFFH	64 Kbytes
	65	420000H-42FFFFH	64 Kbytes
	64	410000H-41FFFFH	64 Kbytes
	63	400000H-40FFFFH	64 Kbytes
	62	3F0000H-3FFFFFH	64 Kbytes
	61	3E0000H-3EFFFFH	64 Kbytes
	60	3D0000H-3DFFFFH	64 Kbytes
	59	3C0000H-3CFFFFH	64 Kbytes
	58	3B0000H-3BFFFFH	64 Kbytes
	57	3A0000H-3AFFFFH	64 Kbytes
	56	390000H-39FFFFH	64 Kbytes

Note 1: The default state after a power-on Reset is write-protected BPR[143:0] = 5555 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF.

2: nVWLDR bits are One-Time-Programmable. Once a nVWLDR bit is set, the protection state of that particular block is permanently write-locked.

TABLE 5-6: BLOCK PROTECTION REGISTER FOR SST26LF064RT (CONTINUED) (3 OF 4)[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock/nVWLDR[2]		
	55	380000H-38FFFFH	64 Kbytes
	54	370000H-37FFFFH	64 Kbytes
	53	360000H-36FFFFH	64 Kbytes
	52	350000H-35FFFFH	64 Kbytes
	51	340000H-34FFFFH	64 Kbytes
	50	330000H-33FFFFH	64 Kbytes
	49	320000H-32FFFFH	64 Kbytes
	48	310000H-31FFFFH	64 Kbytes
	47	300000H-30FFFFH	64 Kbytes
	46	2F0000H-2FFFFFH	64 Kbytes
	45	2E0000H-2EFFFFH	64 Kbytes
	44	2D0000H-2DFFFFH	64 Kbytes
	43	2C0000H-2CFFFFH	64 Kbytes
	42	2B0000H-2BFFFFH	64 Kbytes
	41	2A0000H-2AFFFFH	64 Kbytes
	40	290000H-29FFFFH	64 Kbytes
	39	280000H-28FFFFH	64 Kbytes
	38	270000H-27FFFFH	64 Kbytes
	37	260000H-26FFFFH	64 Kbytes
	36	250000H-25FFFFH	64 Kbytes
	35	240000H-24FFFFH	64 Kbytes
	34	230000H-23FFFFH	64 Kbytes
	33	220000H-22FFFFH	64 Kbytes
	32	210000H-21FFFFH	64 Kbytes
	31	200000H-20FFFFH	64 Kbytes
	30	1F0000H-1FFFFFH	64 Kbytes
	29	1E0000H-1EFFFFH	64 Kbytes
	28	1D0000H-1DFFFFH	64 Kbytes
	27	1C0000H-1CFFFFH	64 Kbytes
	26	1B0000H-1BFFFFH	64 Kbytes
	25	1A0000H-1AFFFFH	64 Kbytes
	24	190000H-19FFFFH	64 Kbytes
	23	180000H-18FFFFH	64 Kbytes
	22	170000H-17FFFFH	64 Kbytes
	21	160000H-16FFFFH	64 Kbytes
	20	150000H-15FFFFH	64 Kbytes
	19	140000H-14FFFFH	64 Kbytes
	18	130000H-13FFFFH	64 Kbytes
	17	120000H-12FFFFH	64 Kbytes
	16	110000H-11FFFFH	64 Kbytes

Note 1: The default state after a power-on Reset is write-protected BPR[143:0] = 5555 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF.

2: nVWLDR bits are One-Time-Programmable. Once a nVWLDR bit is set, the protection state of that particular block is permanently write-locked.

TABLE 5-6: BLOCK PROTECTION REGISTER FOR SST26LF064RT (CONTINUED) (4 OF 4)[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock/nVWLDR[2]		
	15	100000H-10FFFFH	64 Kbytes
	14	0F0000H-0FFFFFH	64 Kbytes
	13	0E0000H-0EFFFFH	64 Kbytes
	12	0D0000H-0DFFFFH	64 Kbytes
	11	0C0000H-0CFFFFH	64 Kbytes
	10	0B0000H-0BFFFFH	64 Kbytes
	9	0A0000H-0AFFFFH	64 Kbytes
	8	090000H-09FFFFH	64 Kbytes
	7	080000H-08FFFFH	64 Kbytes
	6	070000H-07FFFFH	64 Kbytes
	5	060000H-06FFFFH	64 Kbytes
	4	050000H-05FFFFH	64 Kbytes
	3	040000H-04FFFFH	64 Kbytes
	2	030000H-03FFFFH	64 Kbytes
	1	020000H-02FFFFH	64 Kbytes
	0	010000H-01FFFFH	64 Kbytes

Note 1: The default state after a power-on Reset is write-protected BPR[143:0] = 5555 FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF.

2: nVWLDR bits are One-Time-Programmable. Once a nVWLDR bit is set, the protection state of that particular block is permanently write-locked.

6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to V_{DD}+0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... -2.0V to V_{DD}+2.0V

Surface mount solder reflow temperature ..... +260°C for 10 seconds

Output short circuit current[1] ..... 50 mA

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Military	-55°C to +125°C	3V-3.6V

TABLE 6-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
3 ns	C_L = 30 pF

Note 1: See Figure 8-5.

TABLE 6-3: RECOMMENDED THERMAL OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
T_A	Ambient Temperature	-55	—	125	°C	
R_{JC}[1]	Junction-to-Case Thermal Resistance	—	—	9.0	°C/W	CDFP
R_{JC}[1]	Junction-to-Case Thermal Resistance	—	—	39.5	°C/W	SOIJ
P_D	Power Dissipation	—	—	0.11	W	V_{CC} = 3.6V, I_{CC} = 30 mA (program/read maximum)

Note 1: Simulated in vacuum environment.

6.1 Power-Up Specifications

All functionalities and DC specifications are specified for a VDD ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See Table 6-4 and Figure 6-1 for more information.

When VDD drops from the operating voltage to below the minimum VDD threshold at power-down, all operations are disabled and the device does not respond to commands. Data corruption may result if a power-down occurs while a Write Registers, program or erase operation is in progress (see Figure 6-2).

TABLE 6-4: RECOMMENDED SYSTEM POWER-UP/DOWN TIMINGS

Symbol	Parameter	Minimum	Maximum	Units	Condition
$T_{PU-READ}$(1)	VDD Min to Read operation	100	-	µs	
$T_{PU-WRITE}$(1)	VDD Min to Write operation	100	-	µs	
T_{PD}(1)	Power-down duration	100	-	ms	
V_{OFF}	VDD off time	-	0.3	V	0V recommended

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 6-1: POWER-UP TIMING DIAGRAM

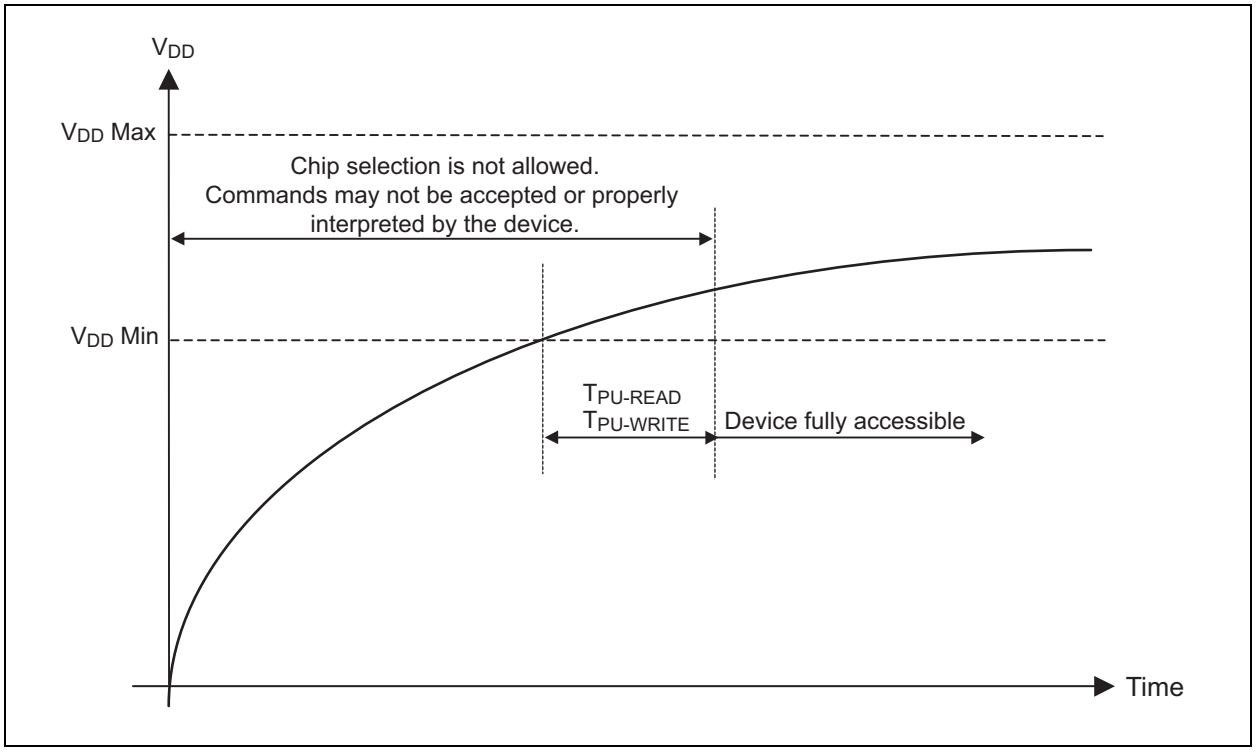
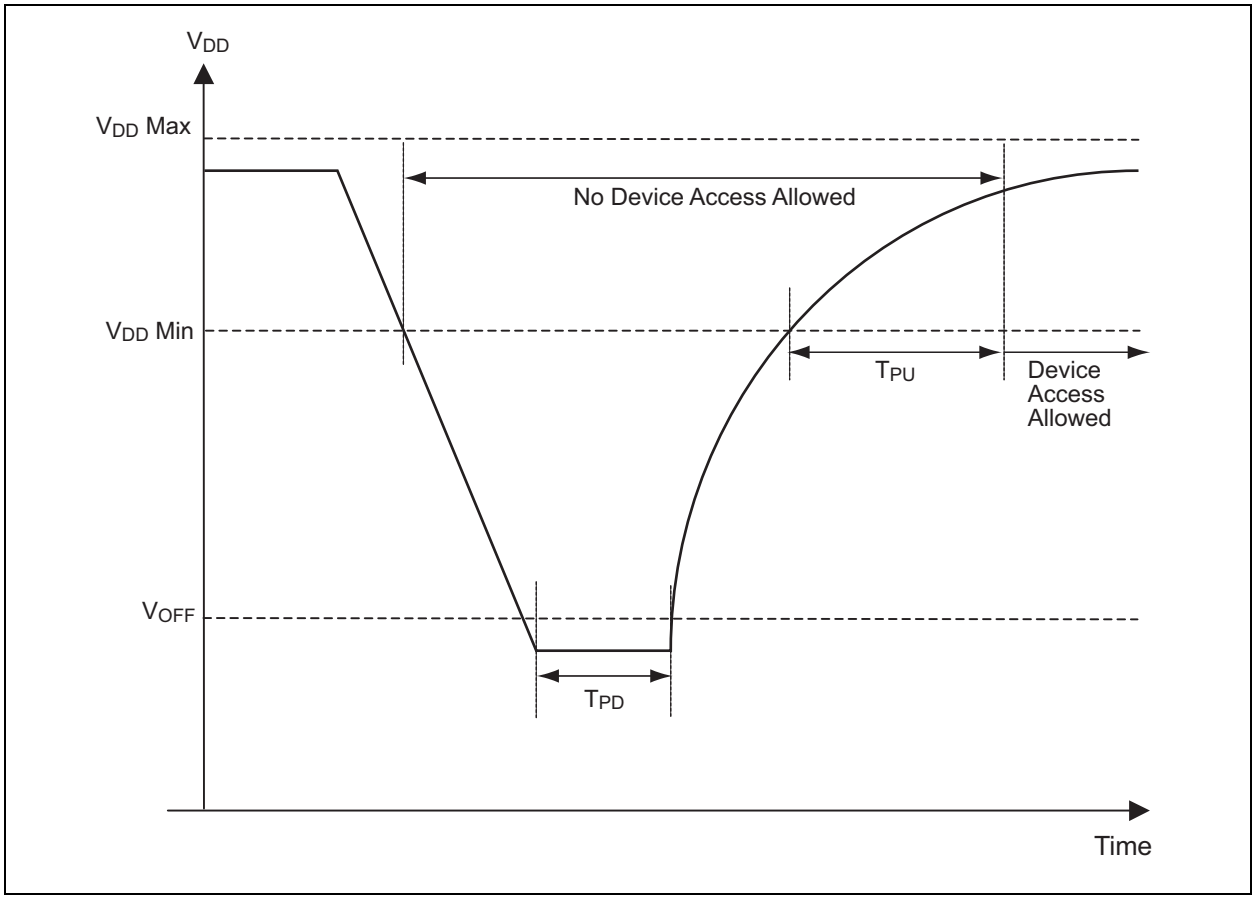


FIGURE 6-2: POWER-DOWN AND VOLTAGE DROP DIAGRAM



7.0 DC CHARACTERISTICS

TABLE 7-1: DC OPERATING CHARACTERISTICS (V_{DD} = 3V-3.6V)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typical	Max.	Units	
I_{DDR1}	Read Current	—	—	15	mA	V_{DD} = V_{DD} Max, CE# = 0.1 V_{DD}/0.9 V_{DD}@40 MHz, SO = open
I_{DDR2}	Read Current	—	—	20	mA	V_{DD} = V_{DD} Max, CE# = 0.1 V_{DD}/0.9 V_{DD}@80 MHz, SO = open
I_{DDW}	Program and Erase Current	—	—	30	mA	V_{DD} Max
I_{SB}	Standby Current	—	—	1	mA	CE# = V_{DD}, V_{IN} = V_{DD} or V_{SS}
I_{LI}	Input Leakage Current	—	—	2	µA	V_{IN} = GND to V_{DD}, V_{DD} = V_{DD} Max
I_{LO}	Output Leakage Current	—	—	2	µA	V_{OUT} = GND to V_{DD}, V_{DD} = V_{DD} Max
V_{IL}	Input Low-Voltage	—	—	0.8	V	V_{DD} = V_{DD} Min
V_{IH}	Input High-Voltage	0.7 V_{DD}	—	—	V	V_{DD} = V_{DD} Max
V_{OL}	Output Low-Voltage	—	—	0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min
V_{OH}	Output High-Voltage	V_{DD}-0.2	—	—	V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min

TABLE 7-2: CAPACITANCE (T_A = +25°C, F = 1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
C_{OUT}(1)	Output Pin Capacitance	V_{OUT} = 0V	8 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7-3: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	10,000(3)	Cycles	JEDEC Standard A117
T_{DR}(1,2)	Data Retention	20	Years	JEDEC Standard A103
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

2: Data retention performed after 1K cycles endurance.

3: The industrial version of the product is warranted 100,000 cycles over the temperature range from -40°C to +105°C.

TABLE 7-4: WRITE TIMING PARAMETERS (V_{DD} = 3V-3.6V)

Symbol	Parameter	Minimum	Maximum	Units
T_{SE}	Sector Erase	—	25	ms
T_{BE}	Block Erase	—	25	ms
T_{SCE}	Chip Erase	—	50	ms
T_{PP}(1)	Page Program	—	1.5	ms
T_{PSID}	Program Security ID	—	1.5	ms

Note 1: Estimate for typical conditions less than 256 bytes: Programming Time (µs) = 55 + (3.75 x # of bytes)

TABLE 7-4: WRITE TIMING PARAMETERS (V_{DD} = 3V-3.6V)

Symbol	Parameter	Minimum	Maximum	Units
T_{WS}	Write Suspend Latency	—	25	µs
T_{WPEN}	Write Protection Enable Bit Latency	—	25	ms

Note 1: Estimate for typical conditions less than 256 bytes: Programming Time (µs) = 55 + (3.75 x # of bytes)

8.0 AC CHARACTERISTICS

TABLE 8-1: AC OPERATING CHARACTERISTICS (V_{DD} = 3V-3.6V)

Symbol	Parameter	Limits – 40 MHz		Limits – 80 MHz		Units
		Min.	Max.	Min.	Max.	
F_{CLK}	Serial Clock Frequency	—	40	—	80	MHz
T_{CLK}	Serial Clock Period	—	25	—	12.5	ns
T_{SCKH}	Serial Clock High Time	11	—	5.5	—	ns
T_{SCKL}	Serial Clock Low Time	11	—	5.5	—	ns
T_{SCKR}(1)	Serial Clock Rise Time (slew rate)	0.1	—	0.1	—	V/ns
T_{SCKF}(1)	Serial Clock Fall Time (slew rate)	0.1	—	0.1	—	V/ns
T_{CES}(2)	CE# Active Setup Time	8	—	5	—	ns
T_{CEH}(2)	CE# Active Hold Time	8	—	5	—	ns
T_{CHS}(2)	CE# Not Active Setup Time	8	—	5	—	ns
T_{CHH}(2)	CE# Not Active Hold Time	8	—	5	—	ns
T_{CPH}	CE# High Time	25	—	12.5	—	ns
T_{CHZ}	CE# High to High-Z Output	—	19	—	12.5	ns
T_{CLZ}	SCK Low to Low-Z Output	0	—	0	—	ns
T_{HLS}	HOLD# Low Setup Time	8	—	5	—	ns
T_{HHS}	HOLD# High Setup Time	8	—	5	—	ns
T_{HLH}	HOLD# Low Hold Time	8	—	5	—	ns
T_{HHH}	HOLD# High Hold Time	8	—	5	—	ns
T_{HZ}	HOLD# Low-to-High-Z Output	—	8	—	8	ns
T_{LZ}	HOLD# High-to-Low-Z Output	—	8	—	8	ns
T_{DS}	Data In Setup Time	3	—	3	—	ns
T_{DH}	Data In Hold Time	4	—	4	—	ns
T_{OH}	Output Hold from SCK Change	0	—	0	—	ns
T_V	Output Valid from SCK	—	8/5(3)	—	8/5(3)	ns

Note 1: Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements.

2: Relative to SCK.

3: 30 pF/10 pF

FIGURE 8-1: HOLD TIMING DIAGRAM

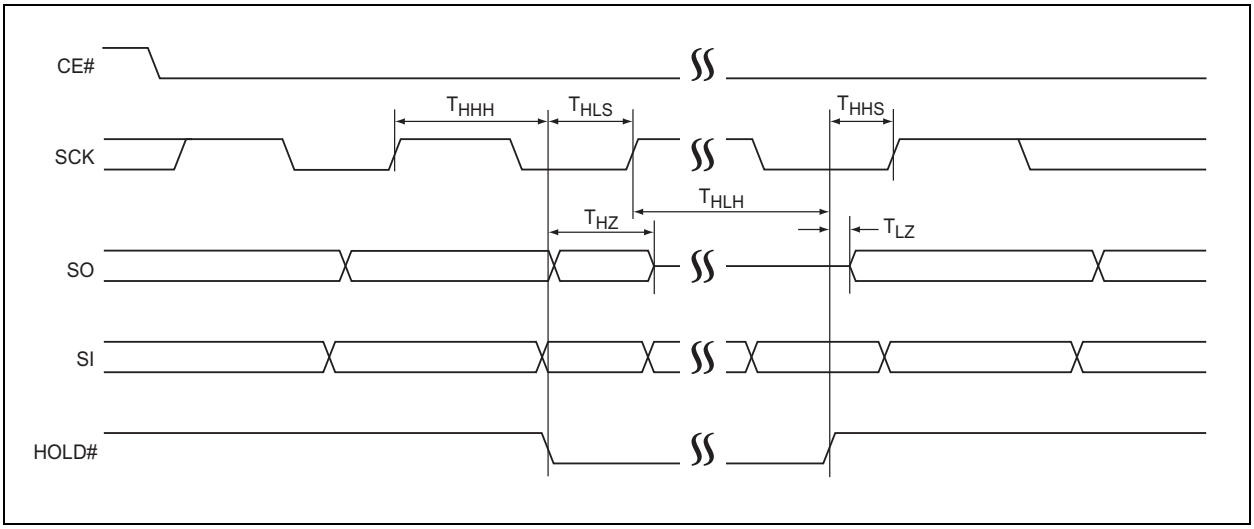


FIGURE 8-2: SERIAL INPUT TIMING DIAGRAM

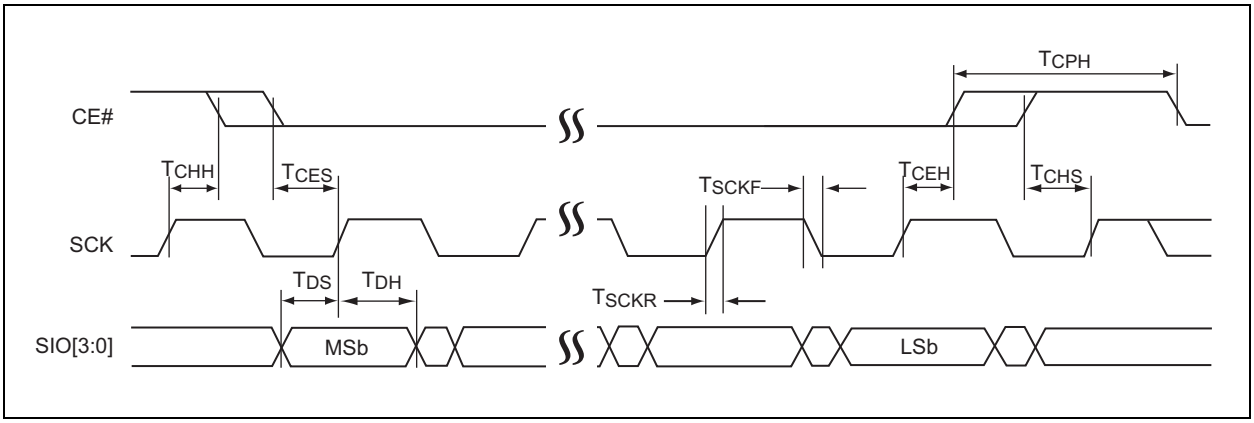


FIGURE 8-3: SERIAL OUTPUT TIMING DIAGRAM

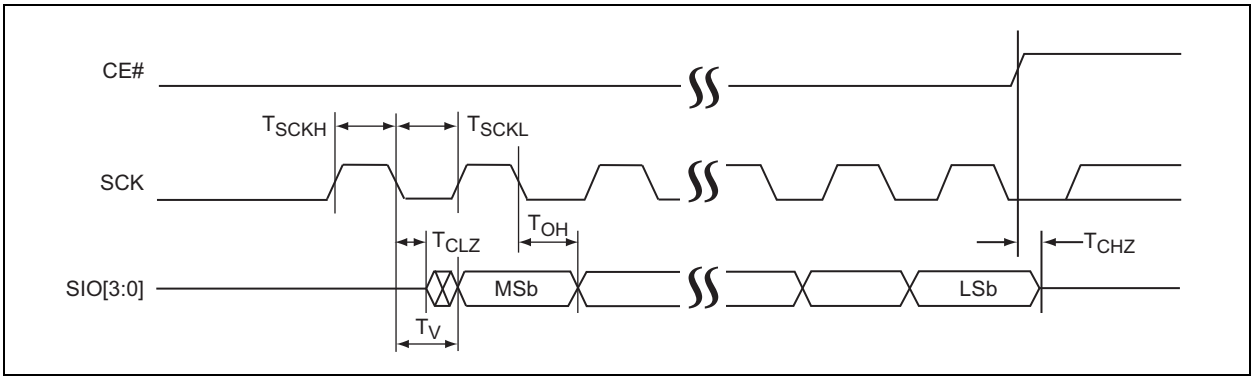
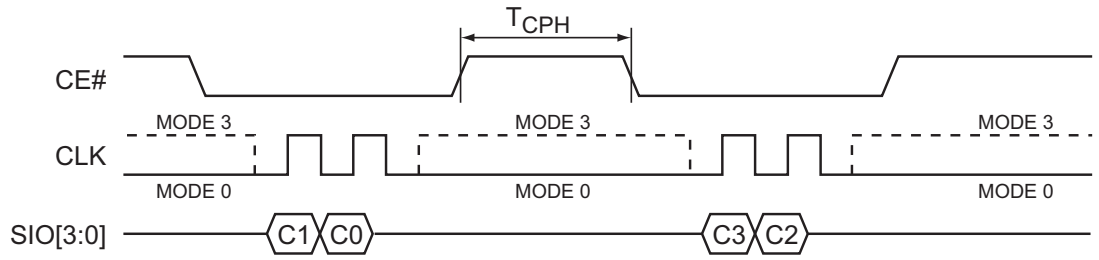


TABLE 8-2: RESET TIMING PARAMETERS

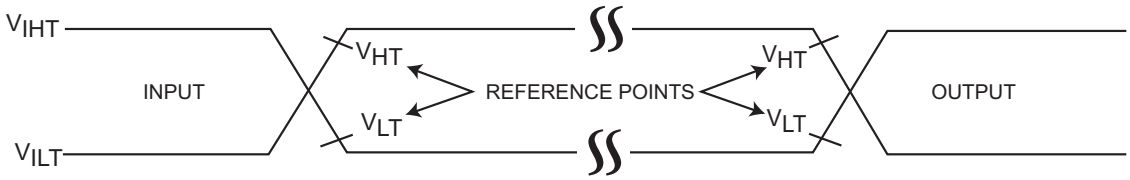
TR(I)	Parameter	Minimum	Maximum	Units
TR(O)	Reset to Read (non-data operation)	—	20	ns
TR(P)	Reset Recovery from Program or Suspend	—	100	µs
TR(E)	Reset Recovery from Erase	—	1	ms

FIGURE 8-4: RESET TIMING DIAGRAM



Note: C[1:0] = 66H; C[3:2] = 99H

FIGURE 8-5: AC INPUT/OUTPUT REFERENCE WAVEFORMS



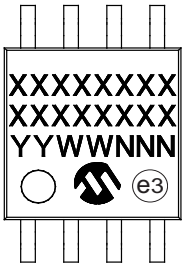
Note 1: AC test inputs are driven at VIHT (0.9VDD) for a logic '1' and VILT (0.1VDD) for a logic '0'. Measurement reference points for inputs and outputs are VHT (0.6VDD) and VLT (0.4VDD). Input rise and fall times (10% ↔ 90%) are <3 ns.

2: V_{HT} – VHIGH Test
VLT – VLOW Test
VIHT – VINPUT HIGH Test
VILT – VINPUT LOW Test

9.0 PACKAGING INFORMATION

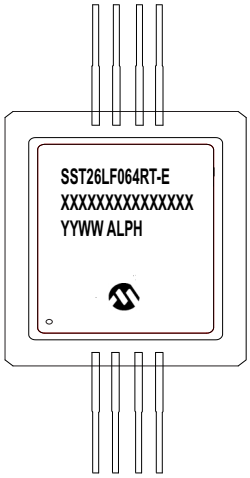
9.1 Package Marking

8-Lead SOIJ (5.28 mm)

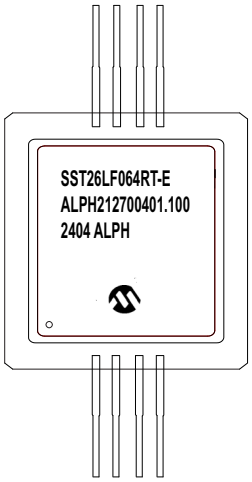


Example

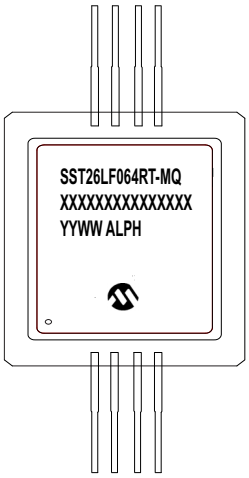
8-Lead CDFP



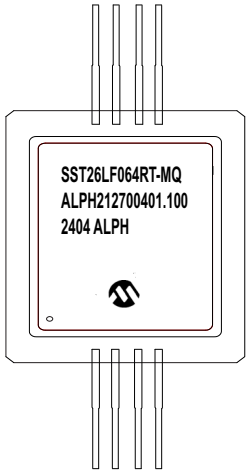
Example



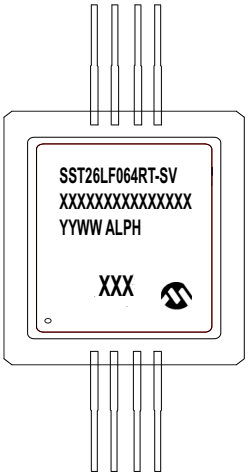
8-Lead CDFP



Example



8-Lead CDFP



Example

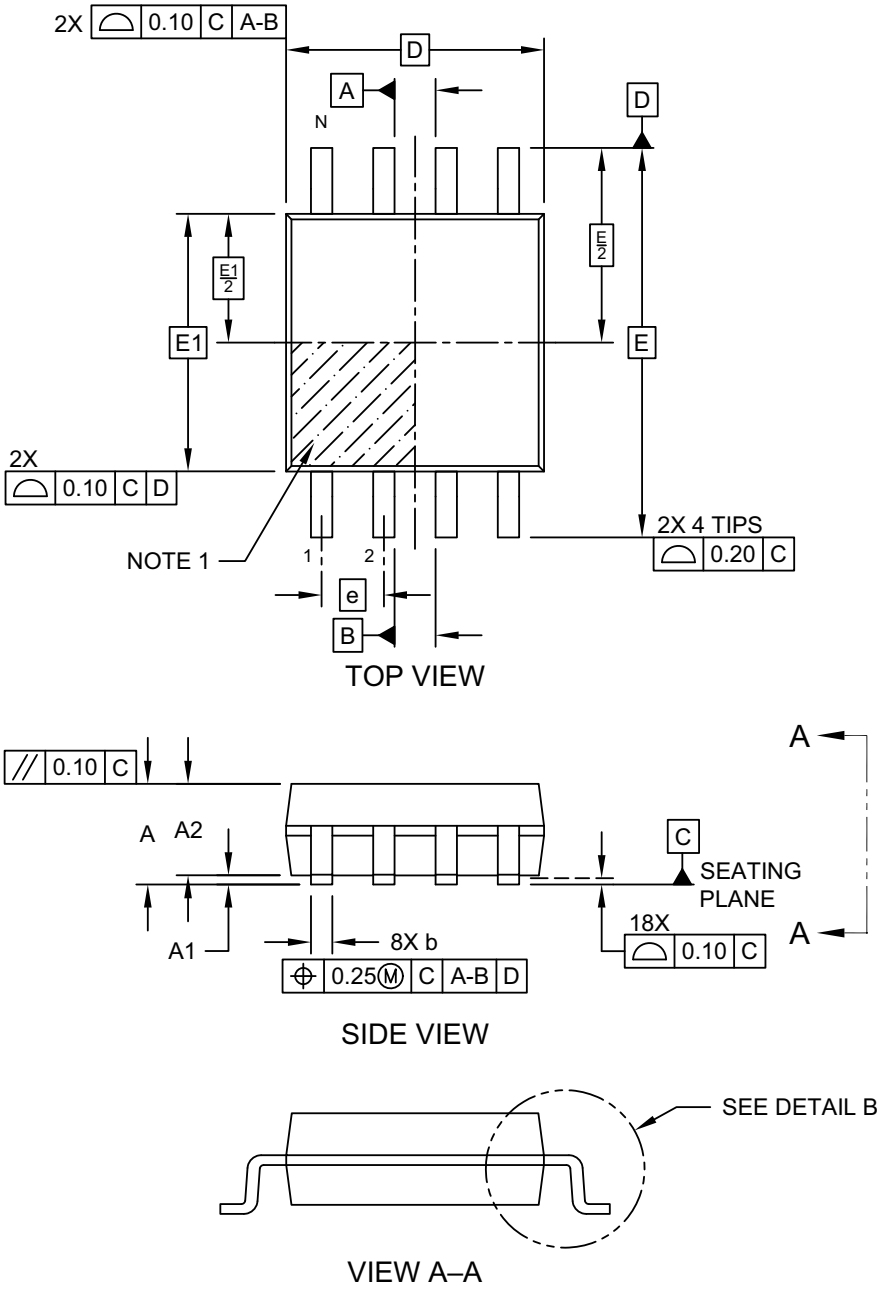
Legend:	XX...X	Part number or part number code for SOIJ08
	XX...X	Lot reference number for CDFP package type
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	ALPH	Location code
	XXX	Serialization
	(e3)	JEDEC® designator for Matte Tin (Sn)

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

9.2 Package Diagrams

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

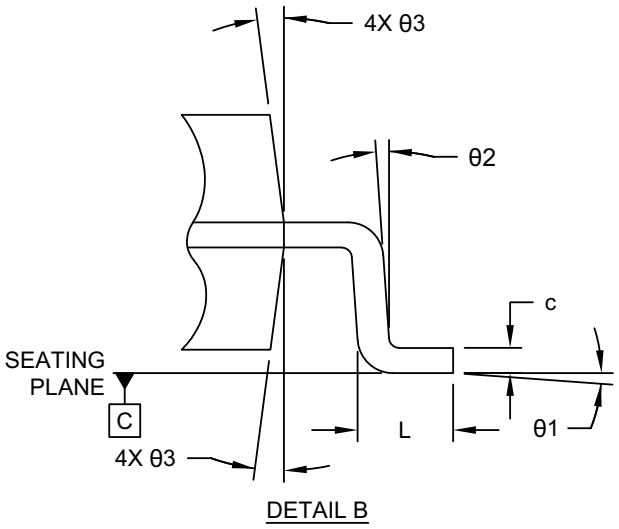
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

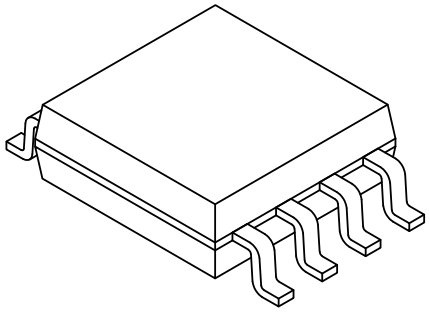


Microchip Technology Drawing C04-056 Rev E Sheet 1 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.77	–	2.03
Standoff §	A1	0.05	–	0.25
Molded Package Thickness	A2	1.75	–	1.98
Overall Length	D		5.26 BSC	
Overall Width	E		7.94 BSC	
Molded Package Width	E1		5.25 BSC	
Terminal Width	b	0.36	–	0.51
Terminal Thickness	c	0.15	–	0.25
Terminal Length	L	0.51	–	0.76
Foot Angle	θ1	0°	–	8°
Lead Angle	θ2	0°	–	–
Mold Draft Angle	θ3	–	–	15°

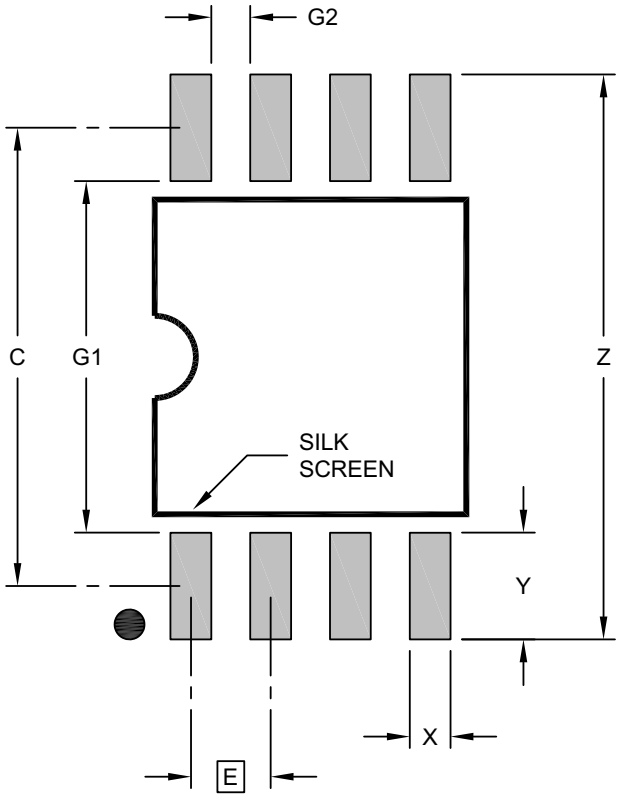
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. SOIJ – JEITA/EIAJ Standard, Formerly called SOIC
3. § – Significant Characteristic
4. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
5. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-056 Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Overall Width	Z			9.00
Contact Pad Spacing	C		7.30	
Contact Pad Width (X8)	X			0.65
Contact Pad Length (X8)	Y			1.70
Contact Pad to Contact Pad (X4)	G1	5.60		
Contact Pad to Contact Pad (X6)	G2	0.62		

Notes:

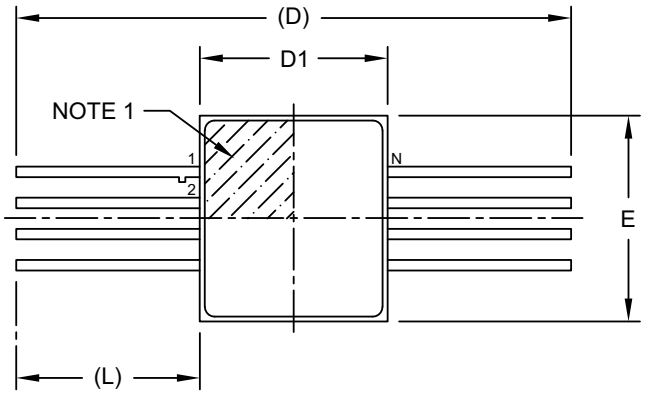
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

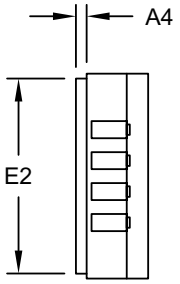
Microchip Technology Drawing C04-2056 Rev E

8-Lead Ceramic Dual Flat Package (HHB) - 7.68x8.41 Body [CDFP]

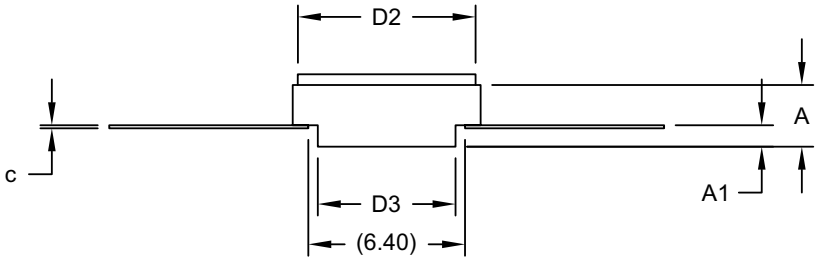
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



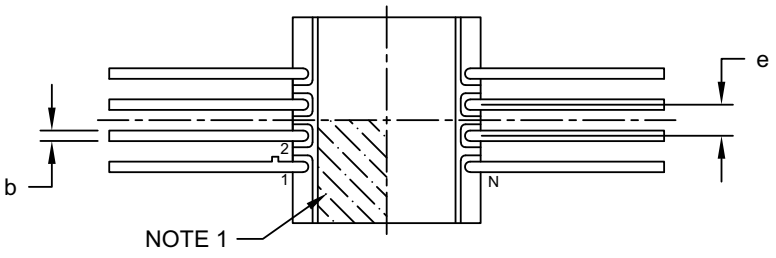
TOP VIEW



END VIEW



SIDE VIEW

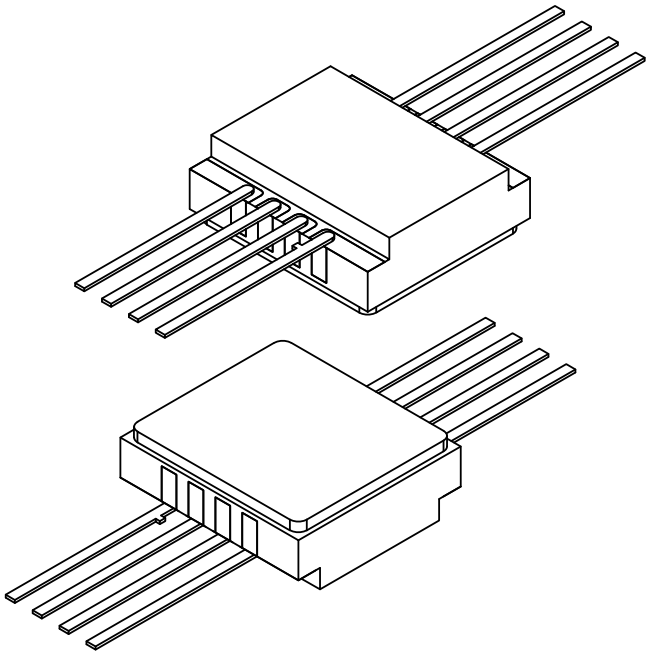


BOTTOM VIEW

Microchip Technology Drawing C04-21533 Rev B Sheet 1 of 2

8-Lead Ceramic Dual Flat Package (HHB) - 7.68x8.41 Body [CDFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units	MILLIMETERS		
Dimension Limits	MIN	NOM	MAX
N		8	
e	1.22	1.27	1.32
A	2.27	2.52	2.77
A1	0.79	0.88	0.97
A4	0.41	0.44	0.47
D		22.67 REF	
D1	7.54	7.67	7.80
D2	7.18	7.26	7.34
D3	5.50	5.63	5.76
E	8.28	8.41	8.54
E2	7.92	8.00	8.08
b	0.38	0.43	0.48
c	0.102	0.127	0.177
L		7.50 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21533 Rev B Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision F (February 2024)

Updated Latch-up immunity value to > 62.5 MeV.cm^2/mg (+125°C)

Revision E (October 2023)

Removed Low Power information and typical values in electrical table; Changed standby current in the electrical table.

Revision D (October 2022)

Added Note to Product Identification System section.

Revision C (September 2022)

Removed “Preliminary” status from the footer; Updated SOIJ package drawing.

Revision B (March 2022)

Updated Features section; Added note to Product Identification System section.

Revision A (September 2021)

Initial release of this document.

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	-XX	/XX	-XX
Device	Operating Frequency	Radiation Tolerant	Package	Type

Device:	SST26LF064 = 64-Mbit 3.0V, SQI Flash Memory WP#/Hold# pin Enable at power-up	
Operating Frequency:	80	= 80 MHz
Radiation Tolerant:	RT	
Package:	SM	= 8-Lead Plastic Small Outline – Medium, 5.28 mm Body (SOIJ)
	HHB	= 8-Lead Ceramic CDFP
Type:	HP	= HiRel Plastic
	MQ	= QML-Q Equivalent
	SV	= QML-V Equivalent
	E	= Engineering Ceramic +25°C
	HC	= HiRel Ceramic

Examples:

a) SST26LF064-80-RT/SM-HP: SQI Flash Memory, SOIJ Package.

b) SST26LF064-80-RT/HHB-MQ: SQI Flash Memory, 8-Lead Ceramic, QML-Q Type Package.

c) SST26LF064-80-RT/HHB-SV: SQI Flash Memory, 8-Lead Ceramic, QML-V Type Package.

d) SST26LF064-80-RT/HHB-E: SQI Flash Memory, 8-Lead Engineering Ceramic Package.

e) SST26LF064-80-RT/HHB-HC(1): SQI Flash Memory, 8-Lead Ceramic CDFP.

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