SST25WF040B

4-Mbit 1.8V SPI Serial Flash

Features

- Single Voltage Read and Write Operations:
  - 1.65V-1.95V
- Serial Interface Architecture:
  - SPI Compatible: Mode 0 and Mode 3
- High-Speed Clock Frequency:
  - 40 MHz
- Dual Input/Output Support:
  - Fast Read Dual Output Instruction (3BH)
  - Fast Read Dual I/O Instruction (BBH)
- Superior Reliability:
  - Endurance: 100,000 cycles
  - Greater than 20 years data retention
- Ultra-Low Power Consumption:
  - Active Read current: 4 mA (typical)
  - Standby current: 7 µA (typical)
  - Power-Down mode Standby current: 2 µA (typical)
- Flexible Erase Capability:
  - Uniform 4-Kbyte sectors
  - Uniform 64-Kbyte overlay blocks
- Page Program Mode:
  - 256 bytes/page
- Fast Erase and Page Program:
  - Chip Erase time: 400 ms (typical)
  - Sector Erase time: 40 ms (typical)
  - Block Erase time: 80 ms (typical)
  - Page Program time: 0.8 ms/256 bytes (typical)
- End-of-Write Detection:
  - Software polling the BUSY bit in STATUS register
- Hold Pin (HOLD#):
  - Suspend a serial sequence without deselecting the device
- Write Protection (WP#):
  - Enables/Disables the Lock-Down function of the STATUS register
- Software Write Protection:
  - Write protection through Block Protection bits in STATUS register
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- All devices are RoHS compliant

Packages

- 8-Lead SOIC (150 mils) and 8-Contact USON (2 mm x 3 mm)

Product Description

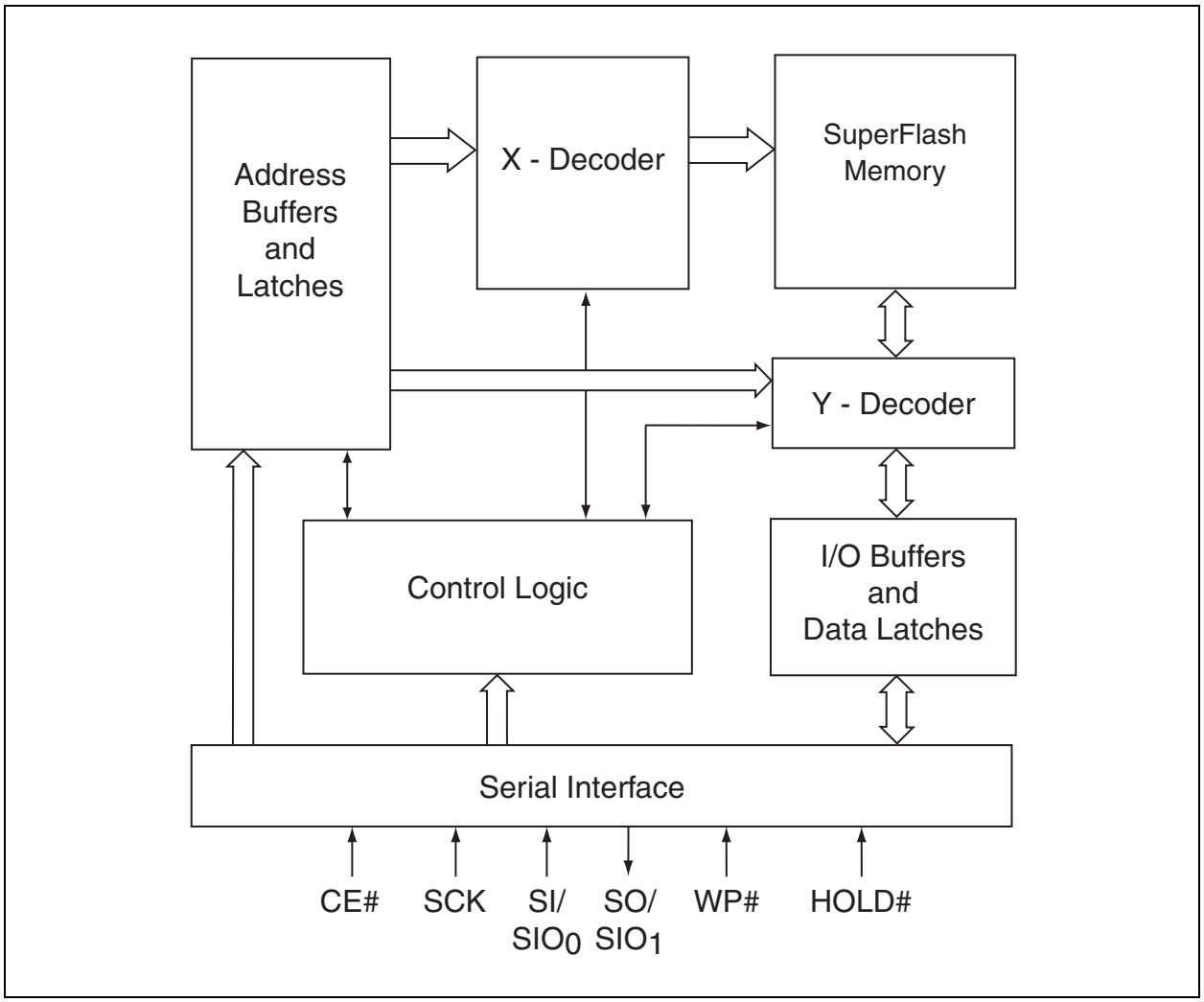
SST25WF040B is a member of the Serial Flash 25 Series family and features a four-wire, SPI-compatible interface that allows for a low pin count package which occupies less board space and ultimately lowers total system costs. SPI Serial Flash memory is manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

This Serial Flash significantly improves performance and reliability, while lowering power consumption. The device writes (Program or Erase) with a single power supply of 1.65V-1.95V. The total energy consumed is a function of the applied voltage, current and time of application. For any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time. As a result, the total energy consumed during any Erase or Program operation is less than alternative Flash memory technologies.

See Figure 2-1 for the pin assignments.

1.0 FUNCTIONAL BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN ASSIGNMENTS

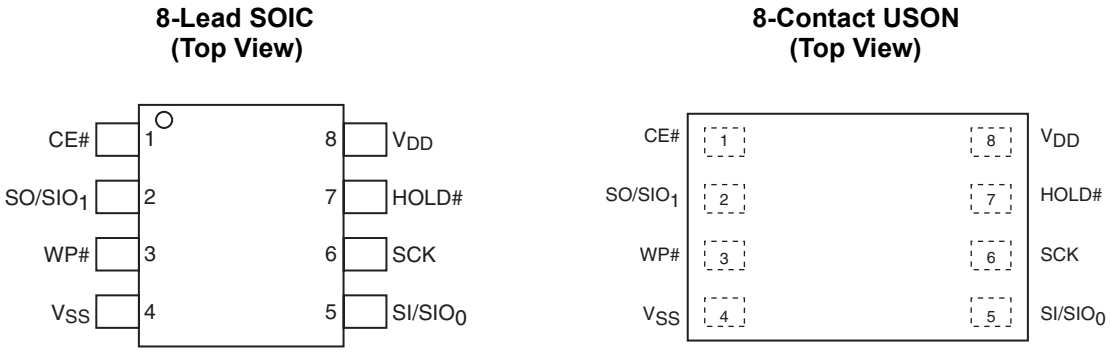


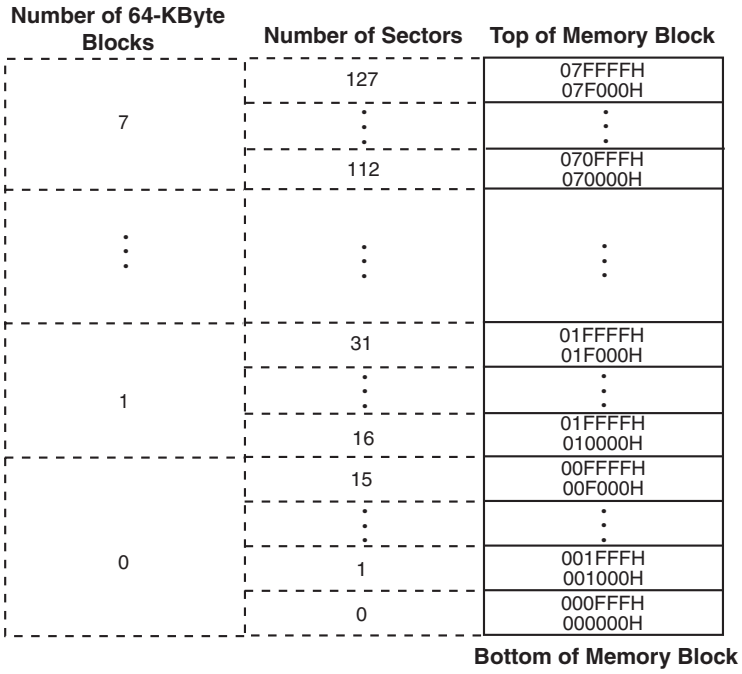
TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the input/output timing of the serial interface. Commands, addresses or input data are latched on the rising edge of the clock input, while output data are shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data are shifted out on the falling edge of the serial clock.
SIO[0:1]	Serial Data Input/Output for Dual I/O Mode	To transfer commands, addresses or data serially into or out of the device. Inputs are latched on the rising edge of the serial clock. Data are shifted out on the falling edge of the serial clock. These pins are used in Dual I/O mode.
CE#	Chip Enable	The device is enabled by a high-to-low transition on CE#. CE# must remain low for the duration of any command sequence. The device is deselected and placed in Standby mode when CE# is high.
WP#	Write-Protect	To enable/disable BPL bit in the STATUS register.
HOLD#	Hold	To temporarily stop serial communication with SPI Flash memory while device is selected.
V_{DD}	Power Supply	To provide power supply voltage: 1.65V-1.95V for SST25WF040B
V_{SS}	Ground	

3.0 MEMORY ORGANIZATION

The SST25WF040B SuperFlash memory arrays are organized in 128 uniform 4-Kbyte sectors, with eight 64-Kbyte overlay erasable blocks.

FIGURE 3-1: MEMORY MAP

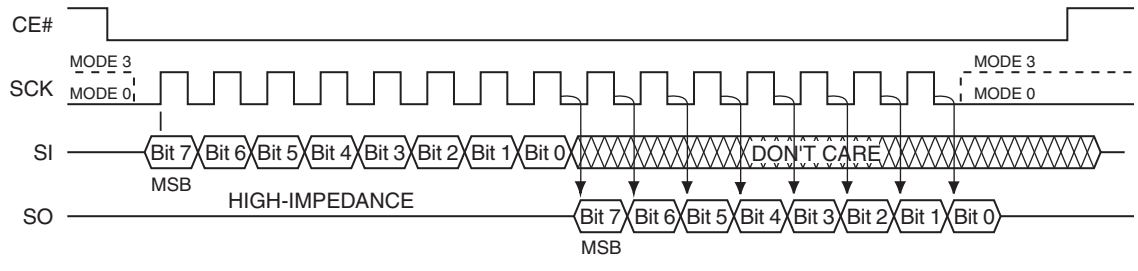


4.0 DEVICE OPERATION

SST25WF040B is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consists of four control lines; Chip Enable (CE#) is used to select the device and data are accessed through the Serial Data Input (SI), Serial Data Output (SO) and Serial Clock (SCK).

The SST25WF040B supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 4-1, is the state of the SCK signal when the bus host is in Standby mode and no data are being transferred. The SCK signal is low for Mode 0 and high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

FIGURE 4-1: SPI PROTOCOL



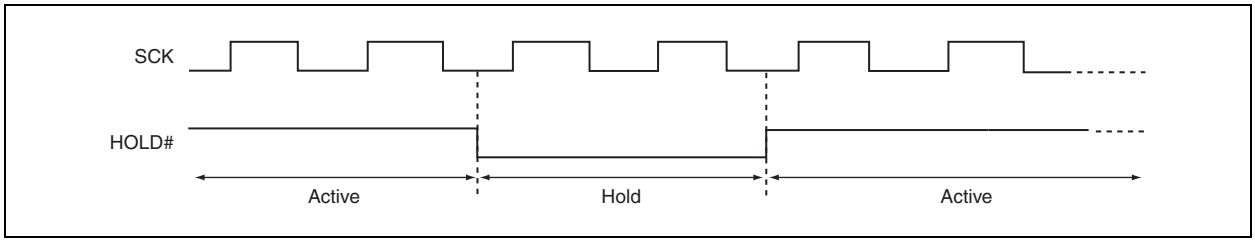
4.0.1 HOLD

In Hold mode, serial sequences underway with the SPI Flash memory are paused without resetting the clocking sequence. To activate HOLD# mode, CE# must be in active-low state. HOLD# mode begins when the SCK active-low state coincides with the falling edge of the HOLD# signal. Hold mode ends when the rising edge of the HOLD# signal coincides with the SCK active-low state. HOLD# must not rise or fall when SCK logic level is high. See Figure 4-2 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active-high during a Hold condition, the device returns to Standby mode. The device can then be re-initiated with the command sequences listed in Table 5-1. As long as the HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active-high and CE# must be driven active-low. See Figure 4-2 for Hold timing.

FIGURE 4-2: HOLD CONDITION WAVEFORM



4.1 Write Protection

SST25WF040B provides software Write protection. The Write-Protect pin (WP#) enables or disables the lock-down function of the STATUS register. The Block Protection bits (BP0, BP1, BP2, TB and BPL) in the STATUS register provide Write protection to the memory array and the STATUS register. See Table 4-3 for the Block Protection description.

4.1.1 WRITE-PROTECT PIN (WP#)

The Write-Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the STATUS register. When WP# is driven low, the execution of the Write Status Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4-1). When WP# is high, the lock-down function of the BPL bit is disabled.

TABLE 4-1: CONDITIONS TO EXECUTE WRITE STATUS REGISTER (WRSR) INSTRUCTION

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

4.2 STATUS Register

The software STATUS register provides information on the availability of the Flash memory array for any Read or Write operation, whether the device is write enabled, and the state of the memory write protected. During an internal Erase or Program operation, the STATUS register may be read only to determine the completion of an operation in progress. Table 4-2 describes the function of each bit in the software STATUS register.

TABLE 4-2: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory write enabled 0 = Device is not memory write enabled	0	R
2	BP0(1)	Indicate current level of block write protection (see Table 4-3)	0 or 1	R/W
3	BP1(1)	Indicate current level of block write protection (see Table 4-3)	0 or 1	R/W
4	BP2(1)	Indicate current level of block write protection (see Table 4-3)	0 or 1	R/W
5	TB(1)	1 = 1/8, 1/4, or 1/2 Bottom Memory Blocks are protected (see Table 4-3) 0 = 1/8, 1/4, or 1/2 Top Memory Blocks are protected	0 or 1	R/W
6	RES	Reserved for future use	0	N/A
7	BPL(1)	1 = BP0, BP1, BP2, TB, and BPL are read-only bits 0 = BP0, BP1, BP2, TB, and BPL are read/writable	0 or 1	R/W

Note 1: BP0, BP1, BP2, TB and BPL bits are nonvolatile memory bits.

4.2.1 BUSY (BIT 0)

The Busy bit determines whether there is an internal Erase or Program operation in progress. A '1' for the Busy bit indicates the device is busy with an operation in progress. A '0' indicates the device is ready for the next valid operation.

4.2.2 WRITE ENABLE LATCH (WEL BIT 1)

The Write Enable Latch bit indicates the status of the internal Write Enable Latch memory. If the WEL bit is set to '1', it indicates the device is write enabled. If the bit is set to '0' (Reset), it indicates the device is not write enabled and does not accept any write (Program/Erase) commands. The Write Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Program instruction completion
- Sector Erase instruction completion
- 64-Kbyte Block Erase instruction completion
- Chip Erase instruction completion
- Write Status Register instruction completion

4.2.3 BLOCK PROTECTION (BP0, BP1, BP2 AND TB BITS 2, 3, 4 AND 5)

The Block Protection (BP0, BP1, BP2 and TB) bits define the size of the memory area to be software protected against any memory write (Program or Erase) operation (see Table 4-3). The Write Status Register (WRSR) instruction is used to program the BP0, BP1, BP2 and TB bits as long as WP# is high or the Block Protect Lock (BPL) bit is '0'. Chip Erase can only be executed if Block Protection bits are all '0'. BP0, BP1 and BP2 select the protected area and TB allocates the protected area to the higher-order address area (Top Blocks) or lower-order address area (Bottom Blocks).

4.2.4 BLOCK PROTECTION LOCK-DOWN (BPL–BIT 7)

When the WP# pin is driven low (V_{IL}), it enables the Block Protection Lock-Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BP0, BP1, BP2, TB and BPL bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is "don't care".

TABLE 4-3: SOFTWARE STATUS REGISTER BLOCK PROTECTION

Protection Level	STATUS Register Bit				Protected Memory Address
	TB	BP2	BP1	BP0	
0 (Full Memory Array unprotected)	X	0	0	0	None
T1 (1/8 Top Memory Block protected)	0	0	0	1	070000H-07FFFFH
T2 (1/4 Top Memory Block protected)	0	0	1	0	060000H-07FFFFH
T3 (1/2 Top Memory Block protected)	0	0	1	1	040000H-07FFFFH
B1 (1/8 Bottom Memory Block protected)	1	0	0	1	000000H-00FFFFH
B2 (1/4 Bottom Memory Block protected)	1	0	1	0	000000H-01FFFFH
B3 (1/2 Bottom Memory Block protected)	1	0	1	1	000000H-03FFFFH
4 (Full Memory Block protected)	X	1	X	X	000000H-0FFFFFH

5.0 INSTRUCTIONS

Instructions are used to read, write (Erase and Program) and configure the SST25WF040B devices. The instruction bus cycles are 8 bits each for commands (Op Code), data and addresses. The Write Enable (WREN) instruction must be executed prior to Sector Erase, Block Erase, Page Program, Write Status Register or Chip Erase instructions. The complete instructions are provided in Table 5-1. All instructions are synchronized off a high-to-low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the Most Significant bit (MSb).

CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (with the exception of Read, Read-ID and Read Status Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to Standby mode. Instruction commands (Op Code), addresses and data are all input from the Most Significant bit first.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Op Code Cycle(1)	Address Cycle(s)(2)	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞	30 MHz
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞	40 MHz
Fast-Read Dual Output	Read Memory with Dual Output	0011 1011b (3BH)	3	1(3)	1 to ∞(3)	
Fast-Read Dual I/O	Read Memory with Dual Address Input and Data Output	1011 1011b (BBH)	3(3)	1(3)	1 to ∞(3)	
4-Kbyte Sector Erase(4)	Erase 4 Kbytes of Memory Array	0010 0000b (20H) 1101 0111b (D7H)	3	0	0	
64-Kbyte Block Erase(5)	Erase 64-Kbyte Block of Memory Array	1101 1000b (D8H)	3	0	0	
Chip Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	
Page Program	To program up to 256 bytes	0000 0010b (02H)	3	0	1 to 256	
RDSR(6)	Read Status Register	0000 0101b (05H)	0	0	1 to ∞	
WRSR	Write Status Register	0000 0001b (01H)	0	0	1	
WREN	Write Enable	0000 0110b (06H)	0	0	0	
WRDI	Write Disable	0000 0100b (04H)	0	0	0	
RDID(7,8)	Read ID	1010 1011b (ABH)	3	0	1 to ∞	
JEDEC-ID	JEDEC ID Read	1001 1111b (9FH)	0	0	4 to ∞	
DPD	Deep Power-Down Mode	1011 1001b (B9H)	0	0	0	
RDPD(8)	Release from Deep Power-Down or Read ID	1010 1011b (ABH)	0	0	0	

Note 1: One bus cycle is eight-clock periods.

2: Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.

3: One bus cycle is four-clock periods in Dual Operation.

4: 4-Kbyte Sector Erase addresses: use A_{MS}-A_{12}, remaining addresses are “don’t care” but must be set either at V_{IL} or V_{IH}.

5: 64-Kbyte Block Erase addresses: use A_{MS}-A_{16}, remaining addresses are “don’t care” but must be set either at V_{IL} or V_{IH}.

6: The Read Status Register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.

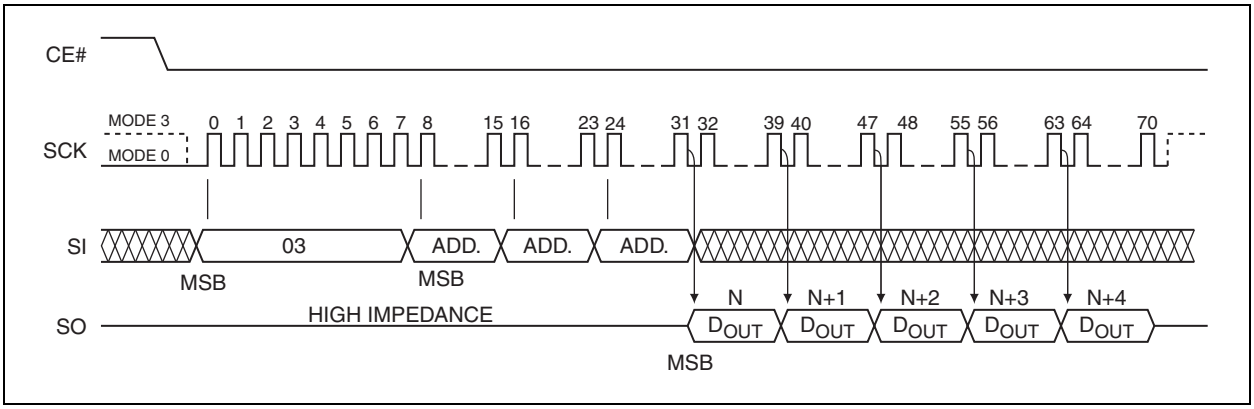
7: Device ID is read after three dummy address bytes. The Device ID output stream is continuous until terminated by a low-to-high transition on CE#.

8: The instructions Release from Deep Power-Down and Read ID are similar instructions (ABH). Executing Read-ID requires the ABH instruction, followed by 24 dummy address bits to retrieve the Device ID. Release from Deep Power-Down only requires the instruction ABH.

5.1 Read (30 MHz)

The Read instruction, 03H, supports up to 30 MHz Read. The device outputs a data stream starting from the specified address location. The data stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer automatically increments until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer automatically increments to the beginning (wrap-around) of the address space. For example, for 4-Mbit density, once the data from the address location 7FFFFH are read, the next output is from address location 000000H. The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits A_{23}-A_0. CE# must remain active-low for the duration of the Read cycle. See Figure 5-1 for the Read sequence.

FIGURE 5-1: READ SEQUENCE



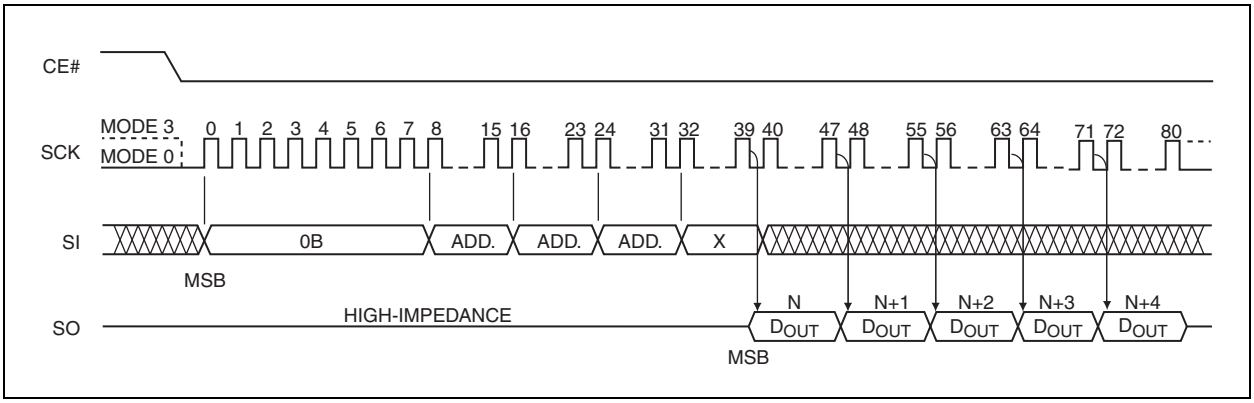
5.2 High-Speed Read (40 MHz)

The High-Speed Read instruction supporting up to 40 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits [A_{23}-A_0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 5-2 for the High-Speed Read sequence.

Following a dummy cycle, the High-Speed Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically increment to the beginning (wrap-around) of the address space. For example, for 4-Mbit density, once the data from address location 7FFFFH are read, the next output will be from address location 000000H.

FIGURE 5-2: HIGH-SPEED READ SEQUENCE

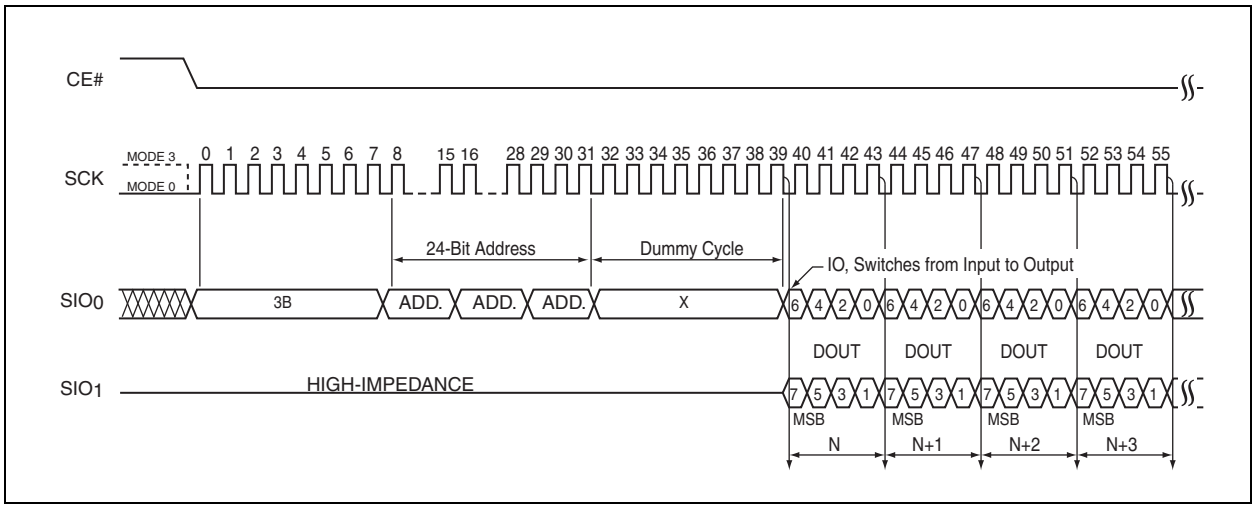


5.3 Fast-Read Dual Output (40 MHz)

The Fast-Read Dual Output (3BH) instruction outputs data up to 40 MHz from the SIO_0 and SIO_1 pins. To initiate the instruction, execute an 8-bit command (3BH) followed by address bits A23-A0 and a dummy byte on SI/SIO_0. Following a dummy cycle, the Fast-Read Dual Output instruction outputs the data starting from the specified address location on the SIO_1 and SIO_0 lines. SIO_1 outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO_0 outputs even data bits D6, D4, D2, and D0. CE# must remain active-low for the duration of the Fast-Read Dual Output instruction cycle. See Figure 5-3 for the Fast-Read Dual Output sequence.

The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer automatically increments to the beginning (wrap-around) of the address space. For 4-Mbit density, once the data from address location 7FFFFH have been read, the next output will be from address location 000000H.

FIGURE 5-3: FAST-READ DUAL OUTPUT SEQUENCE



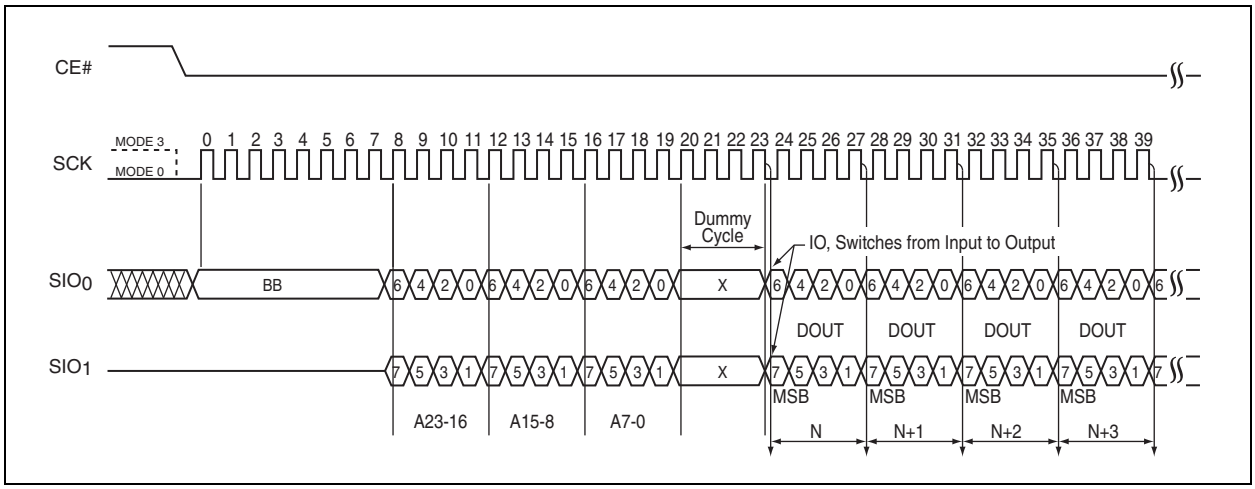
5.4 Fast-Read Dual I/O (40 MHz)

The Fast-Read Dual I/O (BBH) instruction reduces the total number of input clock cycles, which results in faster data access. The device is first selected by driving Chip Enable CE# low. Fast-Read Dual I/O is initiated by executing an 8-bit command (BBH) on SI/SIO_0, thereafter, the device accepts address bits A23-A0 and a dummy byte on SI/SIO_0 and SO/SIO_1. It offers the capability to input address bits A23-A0 at a rate of two bits per clock. Odd address bits A23 through A1 are input on SIO_1 and even address bits A22 through A0 are input on SIO_0, alternately. For example, the Most Significant bit is input first followed by A23/22, A21/A20, and so on. Each bit is latched at the same rising edge of the Serial Clock (SCK). The input data during the dummy clocks is “don’t care”. However, the SIO_0 and SIO_1 pin must be in high-impedance prior to the falling edge of the first data output clock.

Following a dummy cycle, the Fast-Read Dual I/O instruction outputs the data starting from the specified address location on the SIO_1 and SIO_0 lines. SIO_1 outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO_0 outputs even data bits D6, D4, D2, and D0 per clock edge. CE# must remain active-low for the duration of the Fast-Read Dual I/O instruction cycle. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer automatically increments to the beginning (wrap-around) of the address space. For example, once the data from address location 7FFFFH is read, the next output is from address location 000000H. See Figure 5-4 for the Fast-Read Dual I/O sequence.

FIGURE 5-4: FAST-READ DUAL I/O SEQUENCE



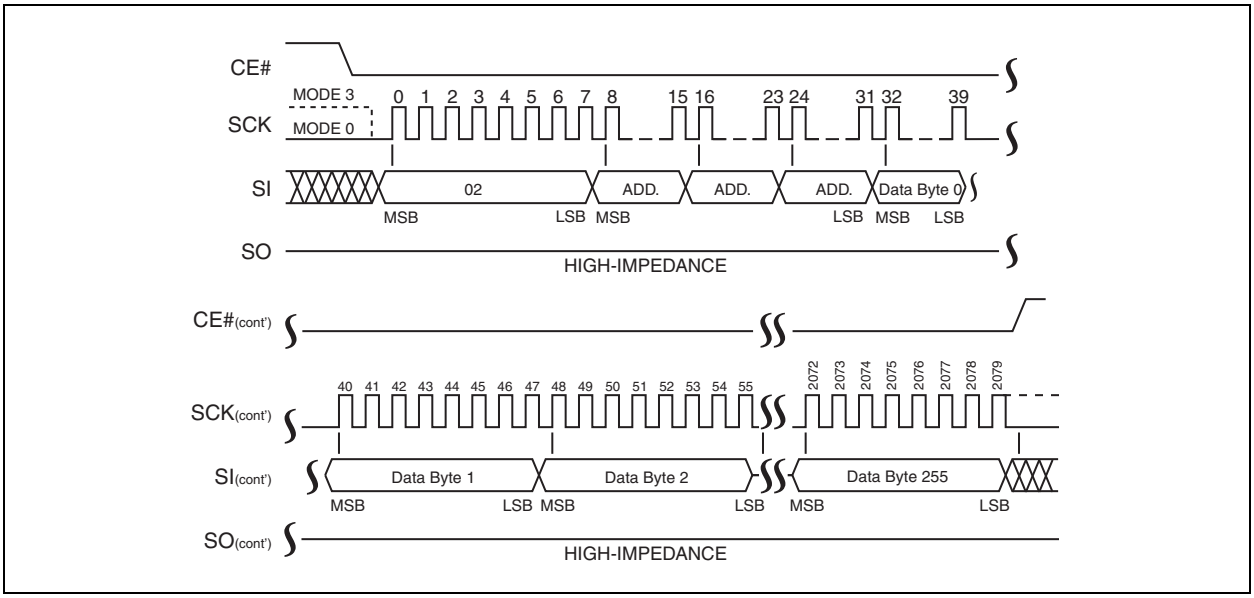
5.5 Page Program

The Page Program instruction programs up to 256 bytes of data in the memory. The data for the selected page address must be in the erased state (FFH) before initiating the Page Program operation. A Page Program applied to a protected memory area will be ignored. Prior to the program operation, execute the WREN instruction.

To execute a Page Program operation, the host drives CE# low, then sends the Page Program command cycle (02H), three address cycles, followed by the data to be programmed, and then drives CE# high. The programmed data must be between 1 and 256 bytes and in whole byte increments. Sending less than a full byte will cause the partial byte to be ignored. Poll the BUSY bit in the STATUS register, or wait T_{PP}, for the completion of the internal, self-timed, Page Program operation. See Figure 5-5 for the Page Program sequence and Figure 6-8 for the flow chart.

When executing Page Program, the memory range for the SST25WF040B is divided into 256-byte page boundaries. The device handles the shifting of more than 256 bytes of data by maintaining the last 256 bytes as the correct data to be programmed. If the target address for the Page Program instruction is not the beginning of the page boundary (A[7:0] are not all zero) and the number of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

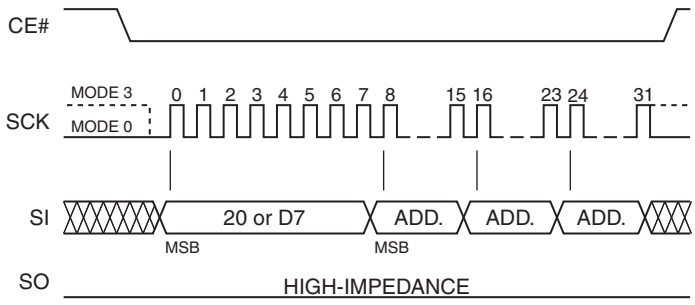
FIGURE 5-5: PAGE PROGRAM SEQUENCE



5.6 Sector Erase

The Sector Erase instruction clears all bits in the selected 4-Kbyte sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H or D7H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{12}] (A_{MS} = Most Significant address) are used to determine the sector address (SA_X). Remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. Poll the BUSY bit in the Software Status register, or wait T_{SE}, for the completion of the internal self-timed Sector Erase cycle. See Figure 5-6 for the Sector Erase sequence and Figure 6-9 for the flow chart.

FIGURE 5-6: SECTOR ERASE SEQUENCE

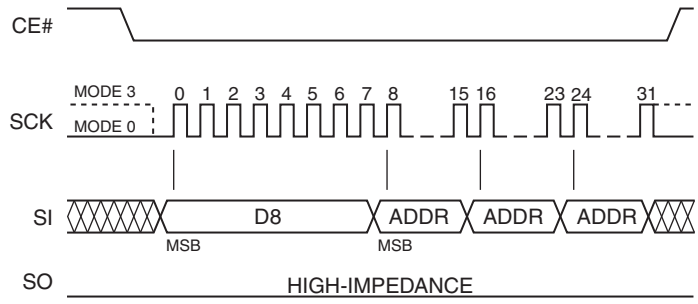


5.7 64-Kbyte Block Erase

The 64-Kbyte Block Erase instruction clears all bits in the selected 64-Kbyte block to FFH. Applying this instruction to a protected memory area results in the instruction being ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of any command sequence.

Initiate the 64-Byte Block Erase instruction by executing an 8-bit command, D8H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{16}] (A_{MS} = Most Significant Address) determine the block address (BA_X). Remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before executing the instruction. Poll the Busy bit in the software status register, or wait T_{BE}, for the completion of the internal self-timed Block Erase cycle. See Figure 5-7 for the 64-Kbyte Block Erase sequences and Figure 6-9 for the flow chart.

FIGURE 5-7: 64-KBYTE BLOCK ERASE SEQUENCE

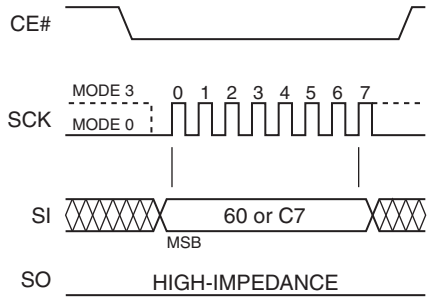


5.8 Chip Erase

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction is ignored if any of the memory area is protected. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Chip Erase instruction sequence. Initiate the Chip Erase instruction by executing an 8-bit command, 60H or C7H.

CE# must be driven high before the instruction is executed. Poll the BUSY bit in the Software Status register, or wait T_{SCE}, for the completion of the internal self-timed Chip Erase cycle. See Figure 5-8 for the Chip Erase sequence and Figure 6-10 for the flow chart.

FIGURE 5-8: CHIP ERASE SEQUENCE

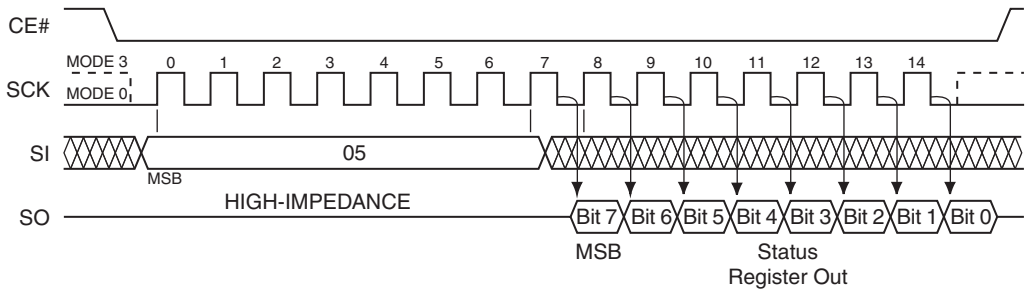


5.9 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction, 05H, allows reading of the STATUS register. The STATUS register may be read at any time, even during a write (Program/Erase) operation. When a write operation is in progress, the BUSY bit may be checked before sending any new commands to assure that the new commands are properly received by the device.

CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read Status Register is continuous with ongoing clock cycles until it is terminated by a low-to-high transition of the CE#. See Figure 5-9 for the RDSR instruction sequence.

FIGURE 5-9: READ STATUS REGISTER (RDSR) SEQUENCE

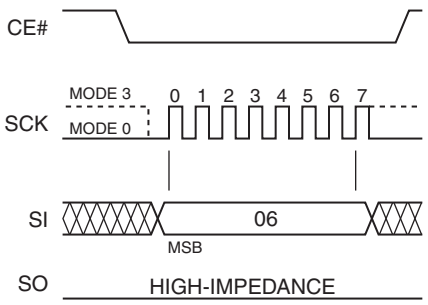


5.10 Write Enable (WREN)

The Write Enable (WREN) instruction, 06H, sets the Write Enable Latch bit in the STATUS Register to '1', allowing Write operations to occur. The WREN instruction must be executed prior to any write (Program/Erase) operation. The WREN instruction may also be used to allow execution of the Write Status Register (WRSR) instruction; however, the Write Enable Latch bit in the STATUS Register will be cleared upon the rising edge CE# of the WRSR instruction.

CE# must be driven low before entering the WREN instruction, and CE# must be driven high before executing the WREN instruction. See Figure 5-10 for the WREN instruction sequence.

FIGURE 5-10: WRITE ENABLE (WREN) SEQUENCE

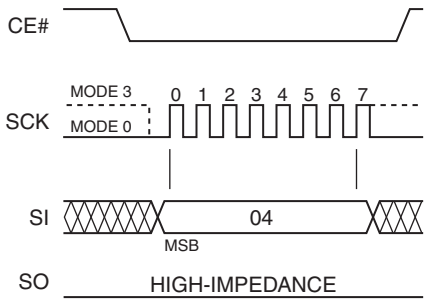


5.11 Write Disable (WRDI)

The Write Disable (WRDI) instruction, 04H, resets the Write Enable Latch bit to '0', thus preventing any new write operations.

CE# must be driven low before entering the WRDI instruction, and CE# must be driven high before executing the WRDI instruction. See Figure 5-11 for the WRDI instruction sequence.

FIGURE 5-11: WRITE DISABLE (WRDI) SEQUENCE

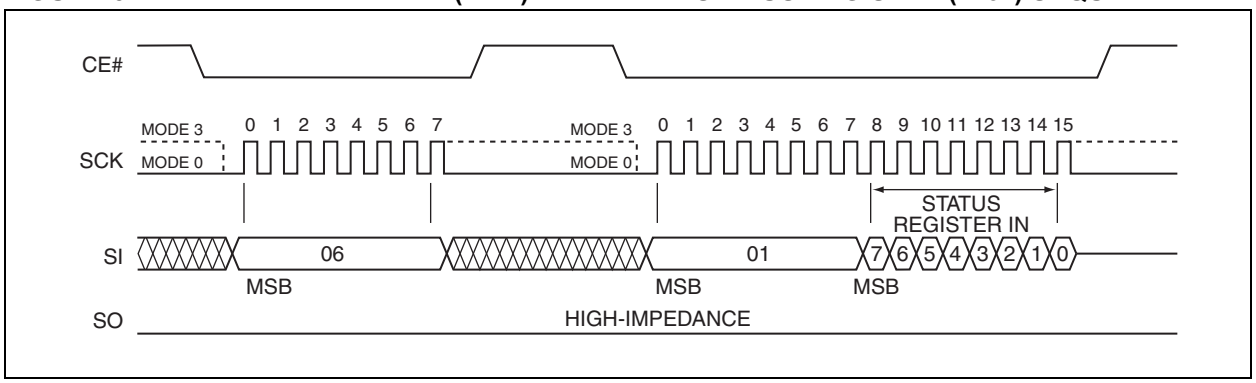


5.12 Write Status Register (WRSR)

The Write Status Register instruction writes new values to the BP0, BP1, BP2, TB and BPL bits of the STATUS register. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. Poll the BUSY bit in the Software Status register, or wait T_{WRSR}, for the completion of the internal self-timed Write Status Register cycle. See Figure 5-12 for WREN and WRSR instruction sequences and Figure 6-11 for the WRSR flow chart.

Executing the Write Status Register instruction will be ignored when WP# is low and BPL bit is set to '1'. When the WP# is low, the BPL bit can only be set from '0' to '1' to lock down the STATUS register, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, BP1, BP2 and TB bits in the STATUS register can all be changed. As long as the BPL bit is set to '0' or the WP# pin is driven high (V_{IH}) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the STATUS register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the STATUS register as well as alter the BP0, BP1, BP2 and TB bits at the same time. See Table 4-1 for a summary description of WP# and BPL functions.

FIGURE 5-12: WRITE ENABLE (WREN) AND WRITE STATUS REGISTER (WRSR) SEQUENCE



5.13 Power-Down

The Deep Power-Down (DPD) instruction puts the device in the lowest power consumption mode – Deep Power-Down mode. This instruction is ignored if the device is busy with an internal write operation. While the device is in DPD mode, all instructions are ignored except for the Release Deep Power-Down instruction or Read ID.

To initiate deep power-down, input the Deep Power-Down instruction (B9H) while driving CE# low. CE# must be driven high before executing the DPD instruction. After driving CE# high, it requires a delay of T_{DPD} before the standby current I_{SB} is reduced to the deep power-down current I_{DPD}. See Figure 5-13 for the DPD instruction sequence.

Exit the power-down state using the Release from Deep Power-Down or Read ID instruction. CE# must be driven low before sending the Release from Deep Power-Down command cycle (ABH) and then driving CE# high. The device will return to Standby mode and be ready for the next instruction after T_{SBR}. See Figure 5-14. for the Release from Deep Power-Down sequence.

FIGURE 5-13: DEEP POWER-DOWN SEQUENCE

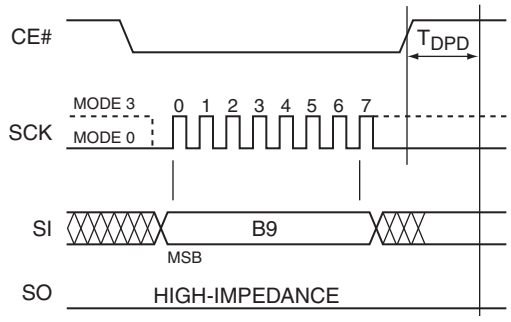
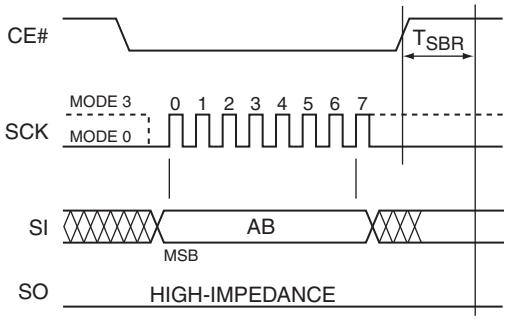


FIGURE 5-14: RELEASE FROM DEEP POWER-DOWN SEQUENCE



5.14 Read ID

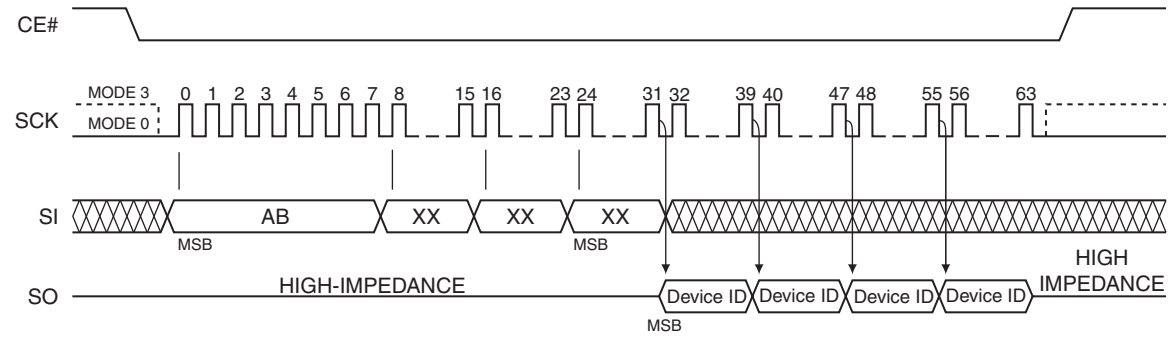
The Read ID instruction identifies the device as SST25WF040B. Use the Read ID instruction to identify SST25WF040B when using multiple manufacturers in the same socket. See Table 5-2.

The device ID information is read by executing an 8-bit command, ABH, followed by 24 dummy address bits. Following the Read ID instruction and 24 address dummy bits, the device ID continues to output with continuous clock input until terminated by a low-to-high transition on CE#.

TABLE 5-2: PRODUCT IDENTIFICATION

	Address	Data
SST25WF040B ID	XXXXXXH	3EH

FIGURE 5-15: READ ID SEQUENCE



Note: The Device ID output stream is continuous until terminated by a low-to-high transition on CE#.

5.15 JEDEC Read ID

The JEDEC Read ID instruction identifies the device ID information of SST25WF040B. The device information can be read by executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, 32-bit device ID information is output from the device. The Device ID information is assigned by the manufacturer and contains the Device ID 1 in the first byte, the type of memory in the second byte, the memory capacity of the device in the third byte and a reserved code in the fourth byte. The 4-byte code outputs repeatedly with continuous clock input until a low-to-high transition on CE#. See Figure 5-16 for the instruction sequence. The JEDEC Read ID instruction is terminated by a low-to-high transition on CE# at any time during data output.

FIGURE 5-16: JEDEC READ ID SEQUENCE

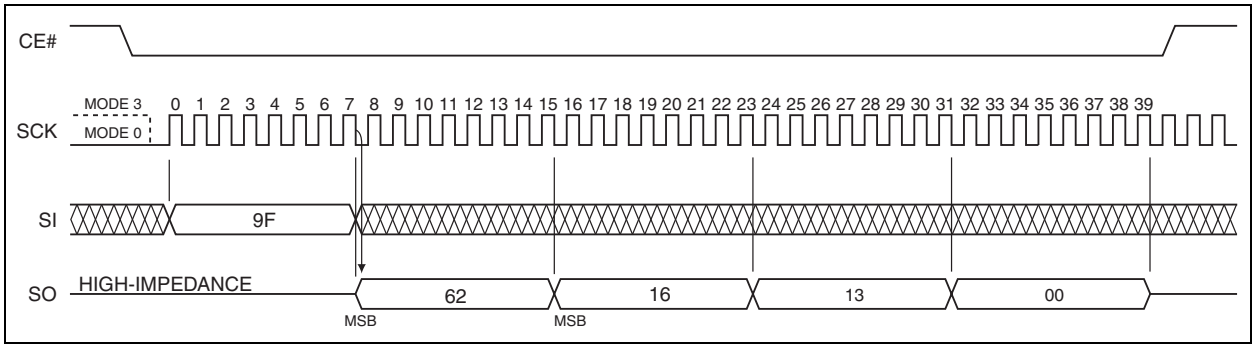


TABLE 5-3: JEDEC READ ID DATA-OUT

Product	Device ID			
	Device ID 1 (Byte 1)	Memory Type (Byte 2)	Memory Capacity (Byte 3)	Reserved Code (Byte 4)
SST25WF040B	62H	16H	13H	00H

6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -55°C to +150°C

DC voltage on any pin to ground potential ..... -0.5V to V_{DD}+0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... -2.0V to V_{DD}+2.0V

Package power dissipation capability (T_A = +25°C) 1.0W

Surface mount solder reflow temperature ..... +260°C for 10 seconds

Output short circuit current[1] ..... 50 mA

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temp.	V_{DD}
Industrial	-40°C to +85°C	1.65V-1.95V
Extended	-40°C to +125°C	1.65V-1.95V

TABLE 6-2: AC CONDITIONS OF TEST

Input Rise/Fall Time	Output Load
5 ns	C_L = 30 pF

6.1 Power-Up Specifications

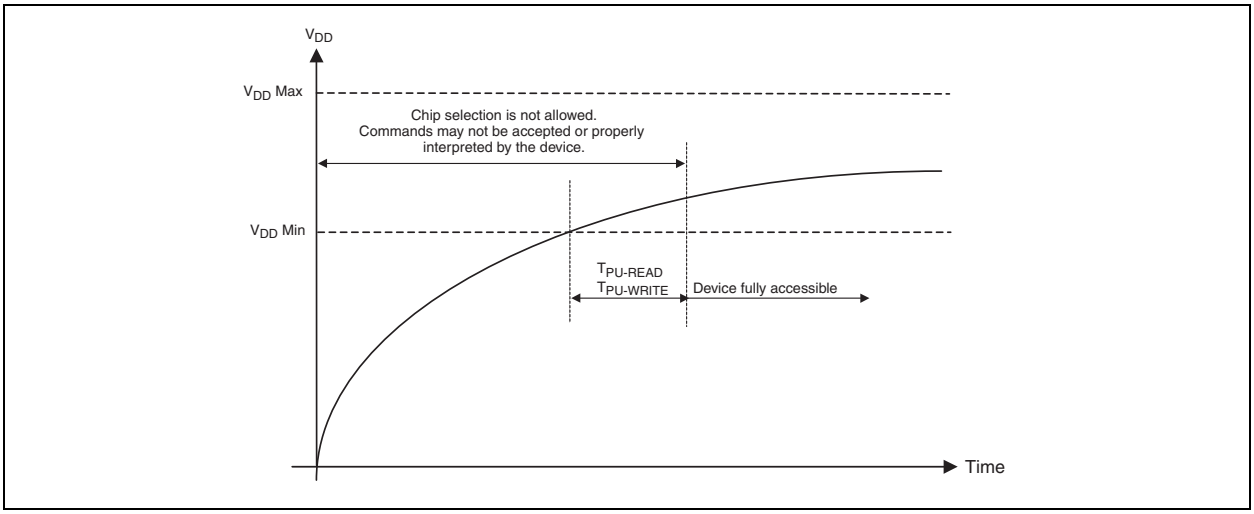
All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 1.8V in less than 180 ms). See Table 6-3 and Figure 6-2 for more information.

TABLE 6-3: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	500	µs
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	500	µs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 6-1: POWER-UP TIMING DIAGRAM



6.2 Hardware Data Protection

SST25WF040B provides a power-up reset function. To ensure that the power reset circuit will operate correctly, the device must meet the conditions shown in Figure 6-2 and Table 6-4.

Microchip does not guarantee the data in the event of an instantaneous power failure that occurs during a write operation.

FIGURE 6-2: POWER-DOWN TIMING DIAGRAM

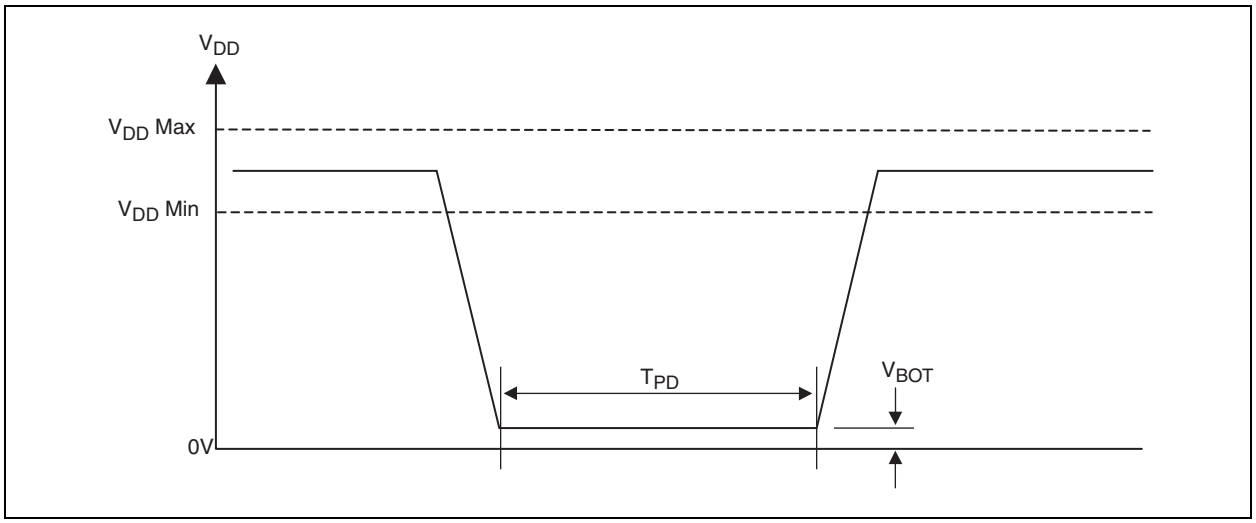


TABLE 6-4: RECOMMENDED SYSTEM POWER-DOWN TIMINGS

Symbol	Parameter	Minimum	Maximum	Units
T_{PD}	Power-down time	10		ms
V_{BOT}	Power-down voltage		0.2	V

6.3 Software Data Protection

SST25WF040B prevents unintentional operations by not recognizing commands under the following conditions:

- After inputting a write command, if the rising CE# edge timing is not in a bus cycle (8 CLK units of SCK)
- When the Page Program data is not in one byte increments
- If the Write Status Register instruction is input for two bus cycles or more

6.4 Decoupling Capacitor

A 0.1 µF ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} to ensure that the device will operate correctly.

6.5 DC Characteristics

TABLE 6-5: DC OPERATING CHARACTERISTICS

Symbol	Parameter		Limits				Test Conditions
			Min	Typ[1]	Max	Units	
I_{DDR}	Read Current				6	mA	CE#=0.1 V_{DD}/0.9 V_{DD}@30 MHz, SO=open; Single I/O
I_{DDR2}	Read Current				8	mA	CE#=0.1 V_{DD}/0.9V_{DD}@40 MHz, SO=open
I_{DDR3}	Read Current				10	mA	CE#=0.1 V_{DD}/0.9V_{DD}@40 MHz, SO=open; Dual I/O
I_{DDW}	Program and Erase Current				15	mA	CE#=V_{DD}
I_{SB}	Standby Current	Industrial		7	50	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
		Extended		7	70	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{DPD}	Deep Power-Down	Industrial		2	10	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
		Extended		2	50	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{LI}	Input Leakage Current				2	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current				2	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		-0.3		0.3	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage		0.7 V_{DD}		V_{DD}+0.3	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage				0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage		V_{DD}-0.2			V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

Note 1: Value characterized, not fully tested in production.

TABLE 6-6: CAPACITANCE (T_A = +25°C, F=1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
C_{OUT}(1)	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-7: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	100,000	Cycles	JEDEC Standard A117
	Status Register Write Cycle	100,000	Cycles	JEDEC Standard A117
T_{DR}(1)	Data Retention	20	Years	JEDEC Standard A103
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

6.6 AC Characteristics

TABLE 6-8: AC OPERATING CHARACTERISTICS

Symbol	Parameter		Limits - 30 MHz			Limits - 40 MHz			Units
			Min		Max	Min		Max	
F_{CLK}[1]	Serial Clock Frequency				30			40	MHz
T_{SCKH}	Serial Clock High Time		14			11.5			ns
T_{SCKL}	Serial Clock Low Time		14			11.5			ns
T_{SCKR}	Serial Clock Rise Time				5			5	ns
T_{SCKF}	Serial Clock Fall Time				5			5	ns
T_{CES}[2]	CE# Active Setup Time		10			10			ns
T_{CEH}[2]	CE# Active Hold Time		10			10			ns
T_{CHS}[2]	CE# Not Active Setup Time		10			10			ns
T_{CHH}[2]	CE# Not Active Hold Time		10			10			ns
T_{CPH}	CE# High Time		25			25			ns
T_{CHZ}	CE# High to High-Z Output				15			15	ns
T_{CLZ}	SCK Low to Low-Z Output		0			0			ns
T_{DS}	Data In Setup Time		5			5			ns
T_{DH}	Data In Hold Time		5			5			ns
T_{HLS}	HOLD# Low Setup Time		5			5			ns
T_{HHS}	HOLD# High Setup Time		5			5			ns
T_{HLH}	HOLD# Low Hold Time		5			5			ns
T_{HHH}	HOLD# High Hold Time		5			5			ns
T_{HZ}	HOLD# Low to High-Z Output				9			9	ns
T_{LZ}	HOLD# High to Low-Z Output				12			12	ns
T_{OH}	Output Hold from SCK Change		1			1			ns
T_V	Output Valid from SCK				11			11	ns
T_{WPS}	WP# Setup Time		20			20			ns
T_{WPH}	WP# Hold Time		20			20			ns
T_{WRSR}	Status Register Write Time				10			10	ms
T_{DPD}	CE# High to Deep Power-Down				5			5	µs
T_{SBR}	Deep Power-Down (CE# High) to Standby Mode				500			500	µs
T_{SE}	Sector Erase			40	150		40	150	ms
T_{BE}	Block Erase			80	250		80	250	ms
T_{SCE}	Chip Erase			0.4	4		0.4	4	s
T_{PP}	Page Program (256 Byte)	Industrial		0.8	1		0.8	1	ms
		Extended		0.8	1.3		0.8	1.3	ms
	n Byte	Industrial		0.15 + n*0.65/256	0.20 + n*0.8/256		0.15 + n*0.65/256	0.20 + n*0.8/256	ms
		Extended		0.15 + n*0.65/256	0.50 + n*0.8/256		0.15 + n*0.65/256	0.20 + n*0.8/256	ms

Note 1: Maximum clock frequency for Read instruction, 03H, is 30 MHz.

2: Relative to SCK.

FIGURE 6-3: SERIAL OUTPUT TIMING DIAGRAM

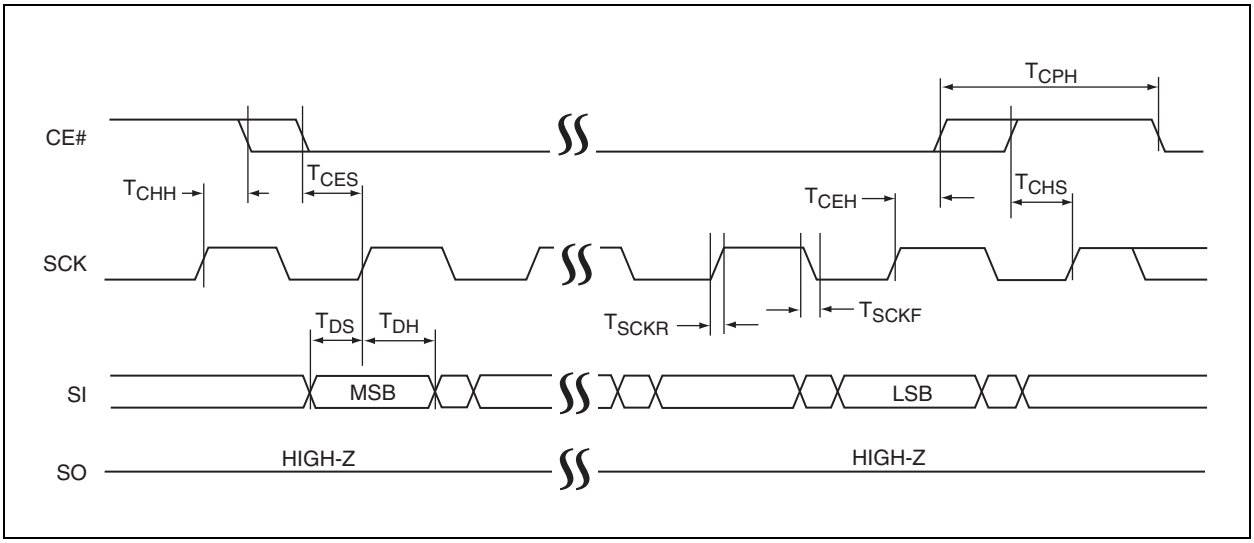


FIGURE 6-4: SERIAL INPUT TIMING DIAGRAM

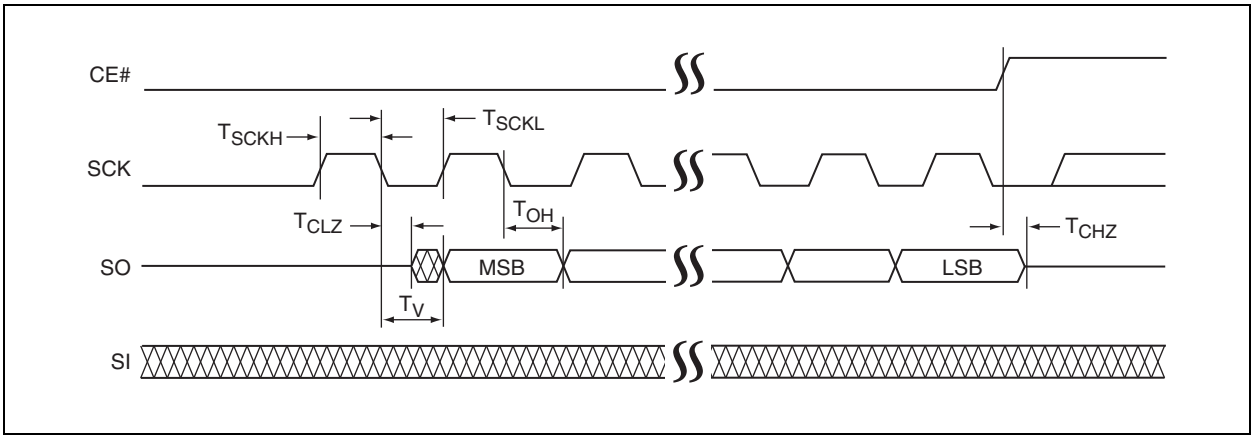


FIGURE 6-5: HOLD TIMING DIAGRAM

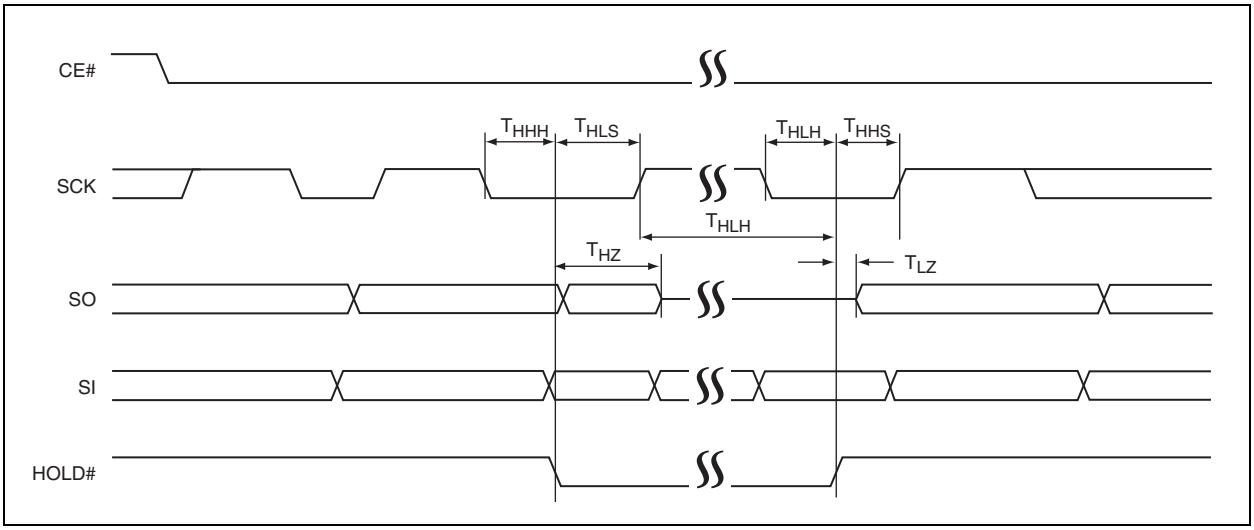


FIGURE 6-6: STATUS REGISTER WRITE TIMING

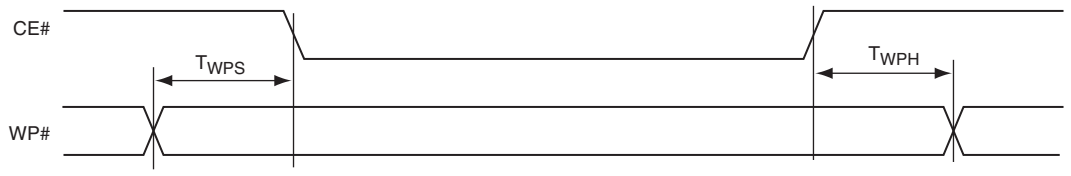
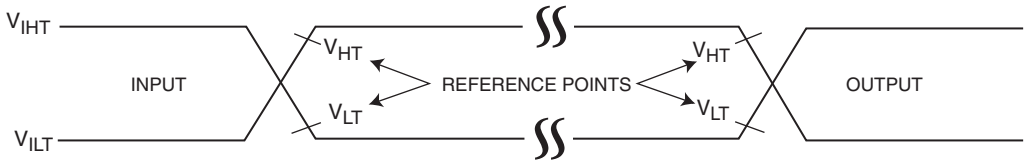


FIGURE 6-7: AC INPUT/OUTPUT REFERENCE WAVEFORMS



AC test inputs are driven at V_{IHT} ($0.8V_{DD}$) for a logic '1' and V_{ILT} ($0.2V_{DD}$) for a logic '0'. Measurement reference points for inputs and outputs are V_{HT} ($0.5V_{DD}$) and V_{LT} ($0.5V_{DD}$). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 6-8: PAGE PROGRAM FLOW CHART

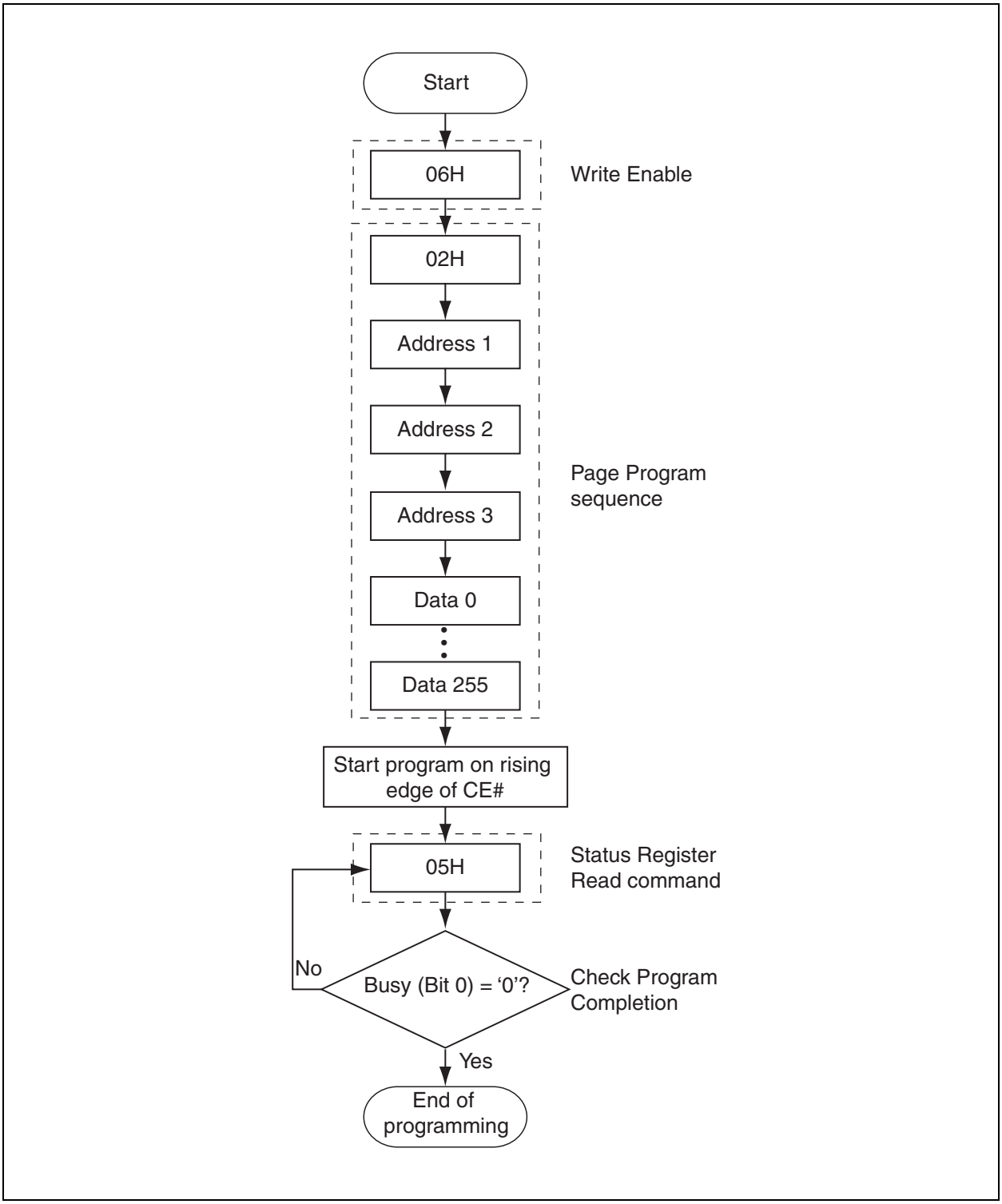


FIGURE 6-9: SECTOR ERASE OR 64-KBYTE BLOCK ERASE FLOW CHART

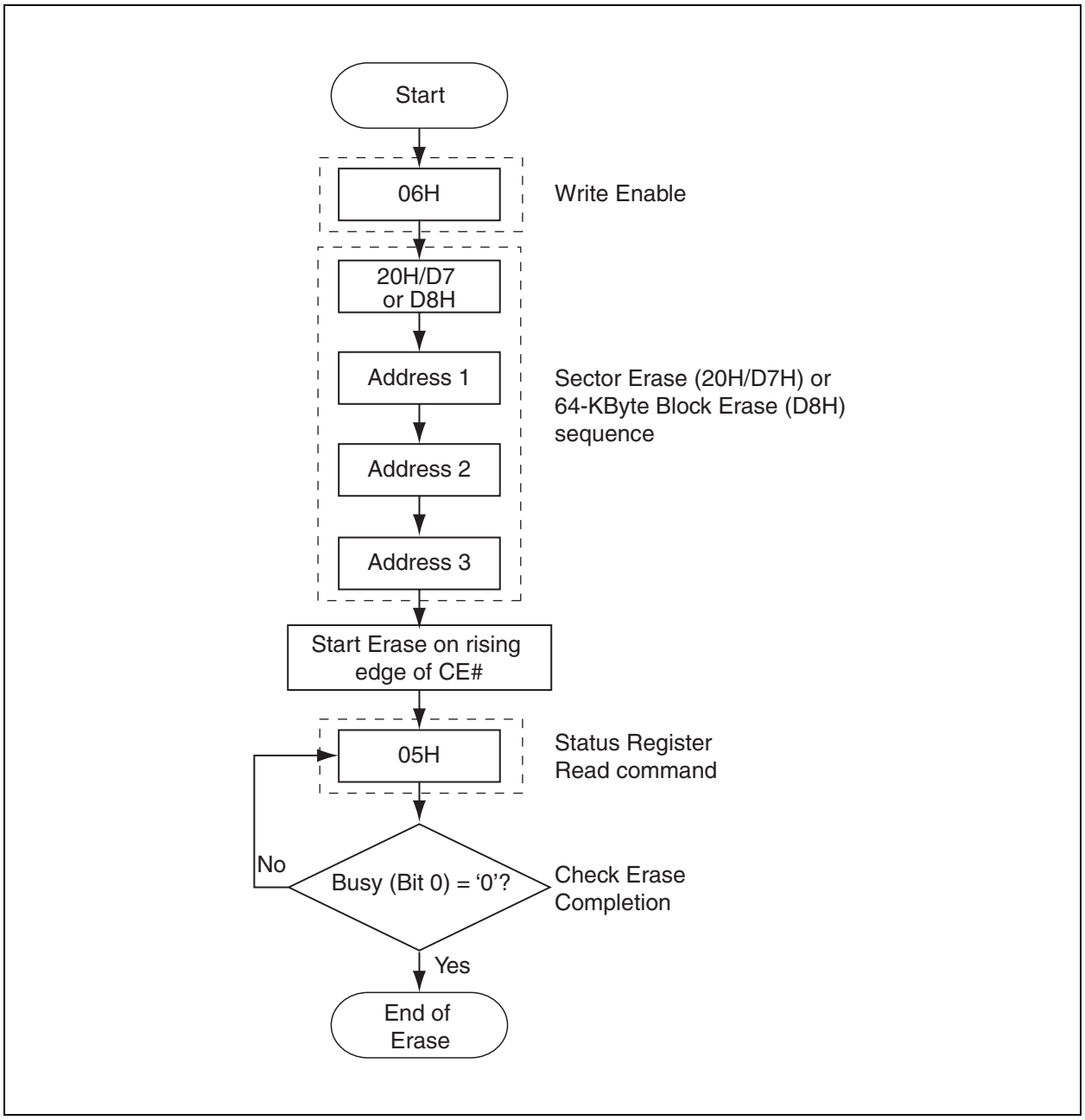


FIGURE 6-10: CHIP ERASE FLOW CHART

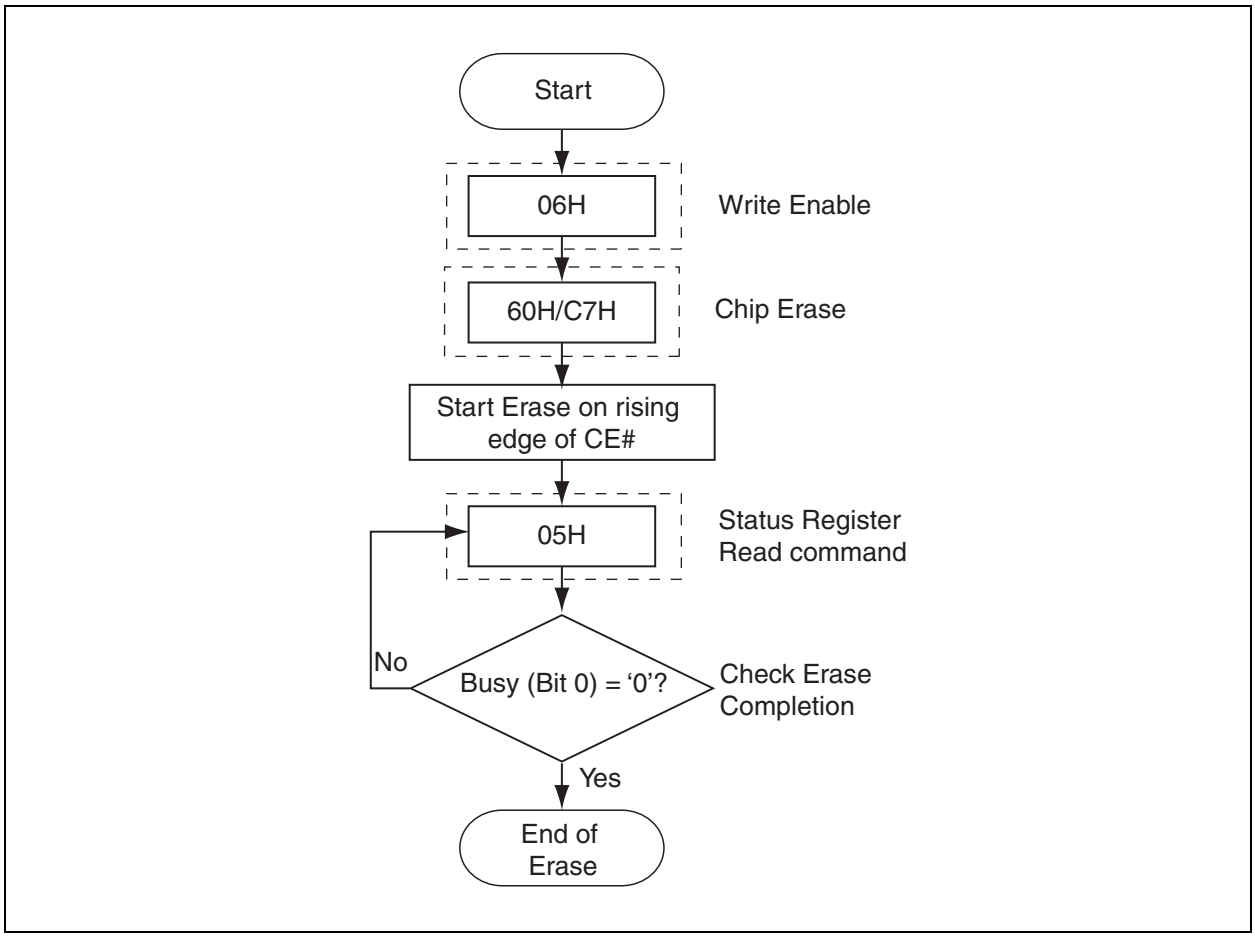
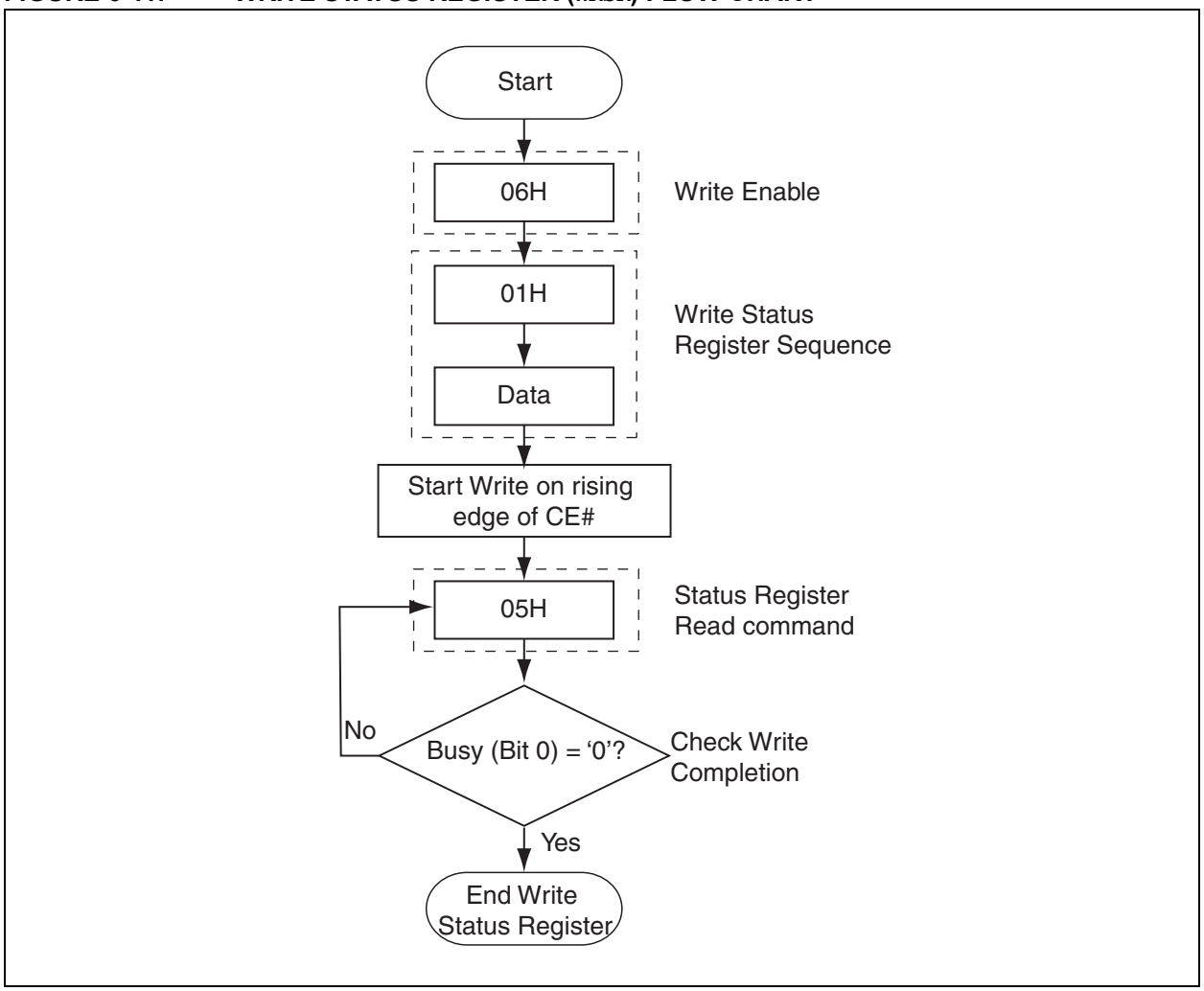


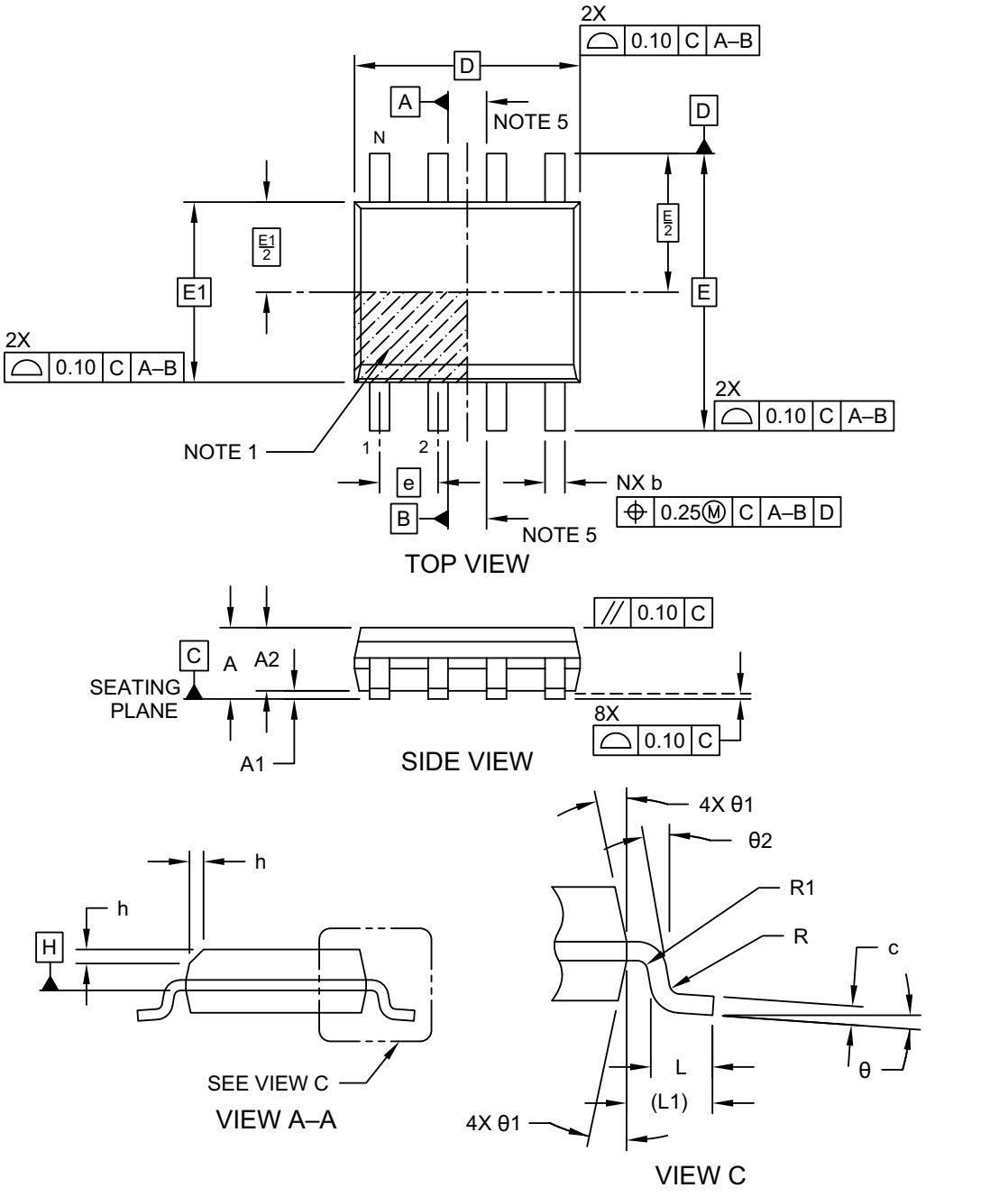
FIGURE 6-11: WRITE STATUS REGISTER (WRSR) FLOW CHART



7.0 PACKAGING DIAGRAMS

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

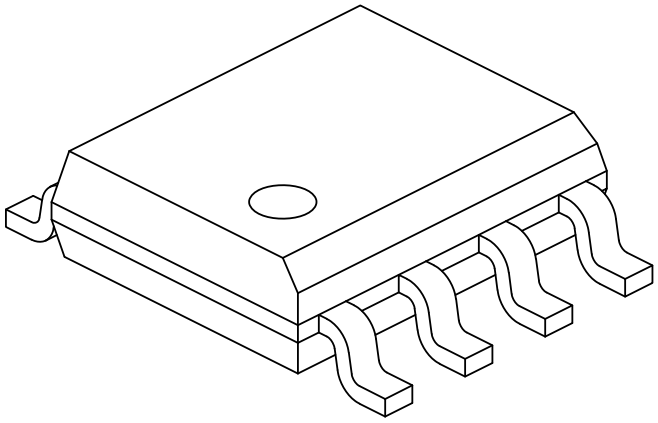
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

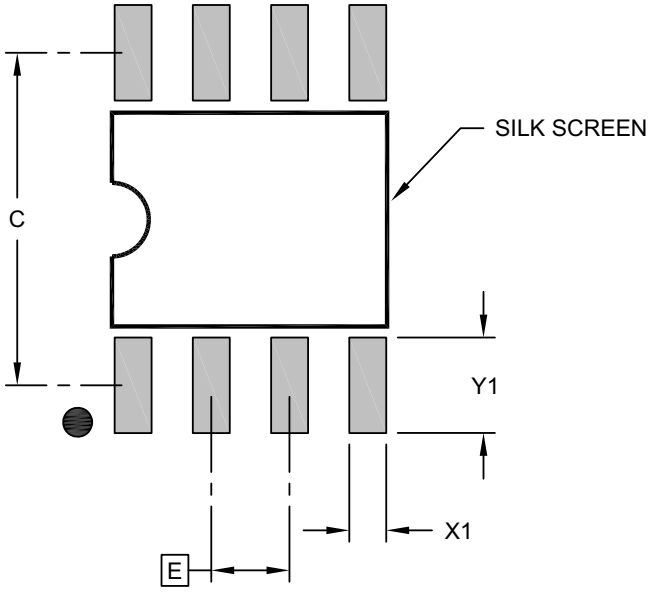
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

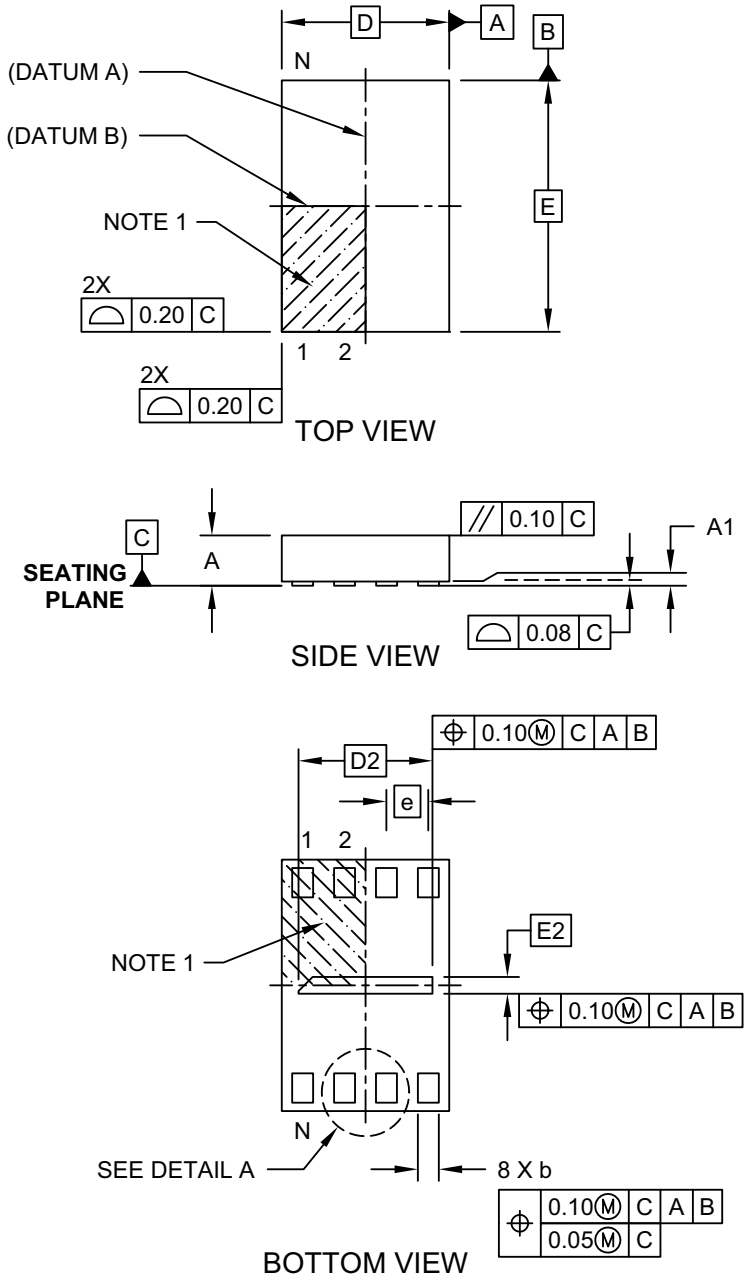
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev K

8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

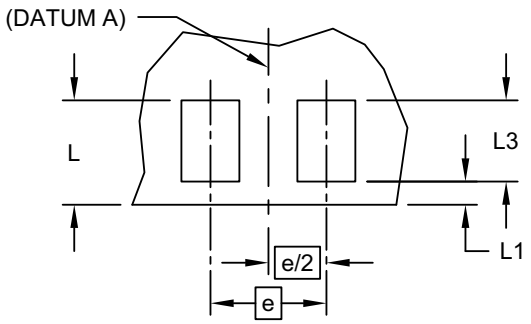
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



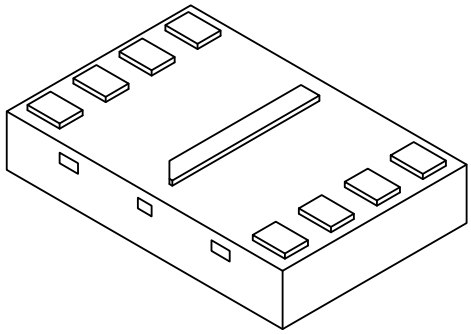
Microchip Technology Drawing C04-203C [PRX] Sheet 1 of 2

8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.45	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Overall Width	D		2.00 BSC	
Exposed Pad Width	D2	1.50	1.60	1.70
Overall Length	E		3.00 BSC	
Exposed Pad Length	E2	0.10	0.20	0.30
Terminal Width	b	0.20	0.25	0.30
Package Edge to Terminal Edge	L	0.40	0.45	0.50
Package Edge to Terminal Edge	L1	—	0.10	—
Terminal Length	L3	0.30	0.35	0.40

Notes:

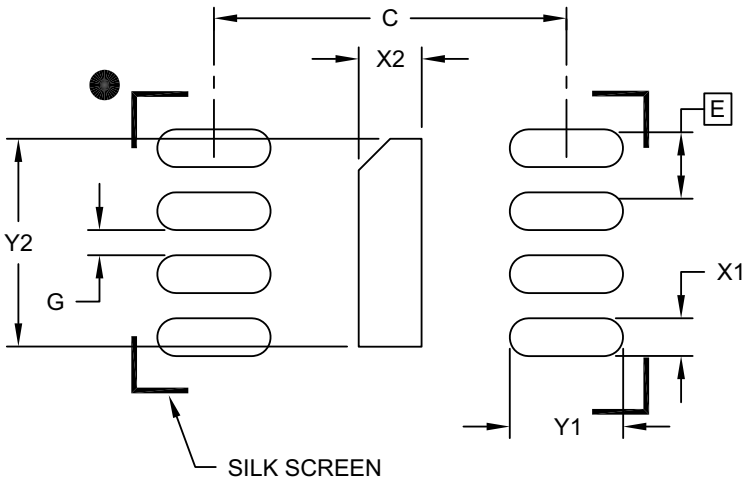
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-203C [PRX] Sheet 2 of 2

8-Lead Plastic Ultra Thin Small Outline No Lead Package (PRX) - 2x3 mm Body [USON] [Also called UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Terminal Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			0.30
Optional Center Pad Length	Y2			1.70
Terminal Pad Spacing	C		2.80	
Terminal Pad Width (X8)	X1			0.30
Terminal Pad Length (X8)	Y1			0.90
Mininum Between Terminal Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2203B [PRX]

8.0 REVISION HISTORY

Revision G (August 2023)

Corrected Figure 3-1 and Power-up ramp time requirement.

Revision F (March 2023)

Updated Product Identification System section; Minor edits to improve document readability.

Revision E (December 2018)

Added Extended temperature content.

Revision D (November 2017)

Updated package drawings.

Revision C (January 2014)

Removed “Preliminary” status from the footer.

Revision B (August 2013)

Updated Product Identification System section; Changed all occurrences of TCE and TSCE; Updated Figure 6-7 and Table 6-8.

Revision A (April 2013)

Initial release of the document.

NOTES:

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PART NO.	X [1]	XXX	-XX	XX
Device	Tape/Reel Indicator	Operating Frequency	Temperature	Package

Device:	SST25WF040B	= 4-Mbit,1.65V-1.95V, Serial Flash Memory
Tape and Reel Indicator:	T	= Tape and Reel[1]
Operating Frequency:	40	= 40 MHz
Temperature:	I	= -40°C to +85°C
	E	= -40°C to +125°C
Package:	NP	= USON (2mm x 3mm Body), 8-contact
	SN	= SOIC (150 mil Body), 8-lead

Valid Combinations:

SST25WF040BT-40I/NP
SST25WF040B-40I/SN
SST25WF040BT-40I/SN
SST25WF040B-40E/SN
SST25WF040BT-40E/SN
SST25WF040BT-40E/NP

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