2-Mbit SPI Serial Flash
SST25LF020A

Not Recommended for New Designs

Microchip Technology's serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin count package occupying less board space and ultimately lowering total system costs. SST25LF020A SPI serial Flash memory is manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

Features

- **Single 3.0V-3.6V Read and Write Operations**

- **Serial Interface Architecture:**
    - SPI Compatible: Mode 0 and Mode 3

- **33 MHz Maximum Clock Frequency**

- **Superior Reliability:**
    - Endurance: 100,000 cycles (typical)
    - Greater than 100 years data retention

- **Low-Power Consumption:**
    - Active Read current: 7 mA (typical)
    - Standby current: 8 µA (typical)

- **Flexible Erase Capability:**
    - Uniform 4-Kbyte sectors
    - Uniform 32-Kbyte overlay blocks

- **Fast Erase and Byte Program:**
    - Chip Erase Time: 70 ms (typical)
    - Sector or Block Erase Time: 18 ms (typical)
    - Byte Program Time: 14 µs (typical)

- **Auto Address Increment (AAI) Programming:**
    - Decrease total chip programming time over Byte Program operations

- **End-of-Write Detection:**
    - Software status

- **Hold Pin (HOLD#):**
    - Suspends a serial sequence to the memory without deselecting the device

- **Write Protection (WP#):**
    - Enables/Disables the Lock-Down function of the STATUS register

- **Software Write Protection:**
    - Write protection through Block Protection bits in STATUS register

- **Temperature Range:**
    - Commercial: 0°C to +70°C
    - Industrial: -40°C to +85°C

- **Packages Available**
    - 8-Lead SOIC 150 mil body width
    - 8-Contact WSON (5 mm x 6 mm)

- **All devices are RoHS compliant**

Not Recommended for New Designs

Product Description

Microchip Technology's serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin count package occupying less board space and ultimately lowering total system costs. SST25LF020A SPI serial Flash memory is manufactured with proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST25LF020A devices significantly improve performance, while lowering power consumption. The total energy consumed is a function of the applied voltage, current and time of application. For any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time. As a result, the total energy consumed during any Erase or Program operation is less than alternative Flash memory technologies. The SST25LF020A devices operate with a single 3.0V-3.6V power supply.

The SST25LF020A devices are offered in an 8-lead SOIC 150 mil body width (SA) package and in an 8-contact WSON package. See Figure 2 for the pin assignments.

Block Diagram

Figure 1: Functional Block Diagram
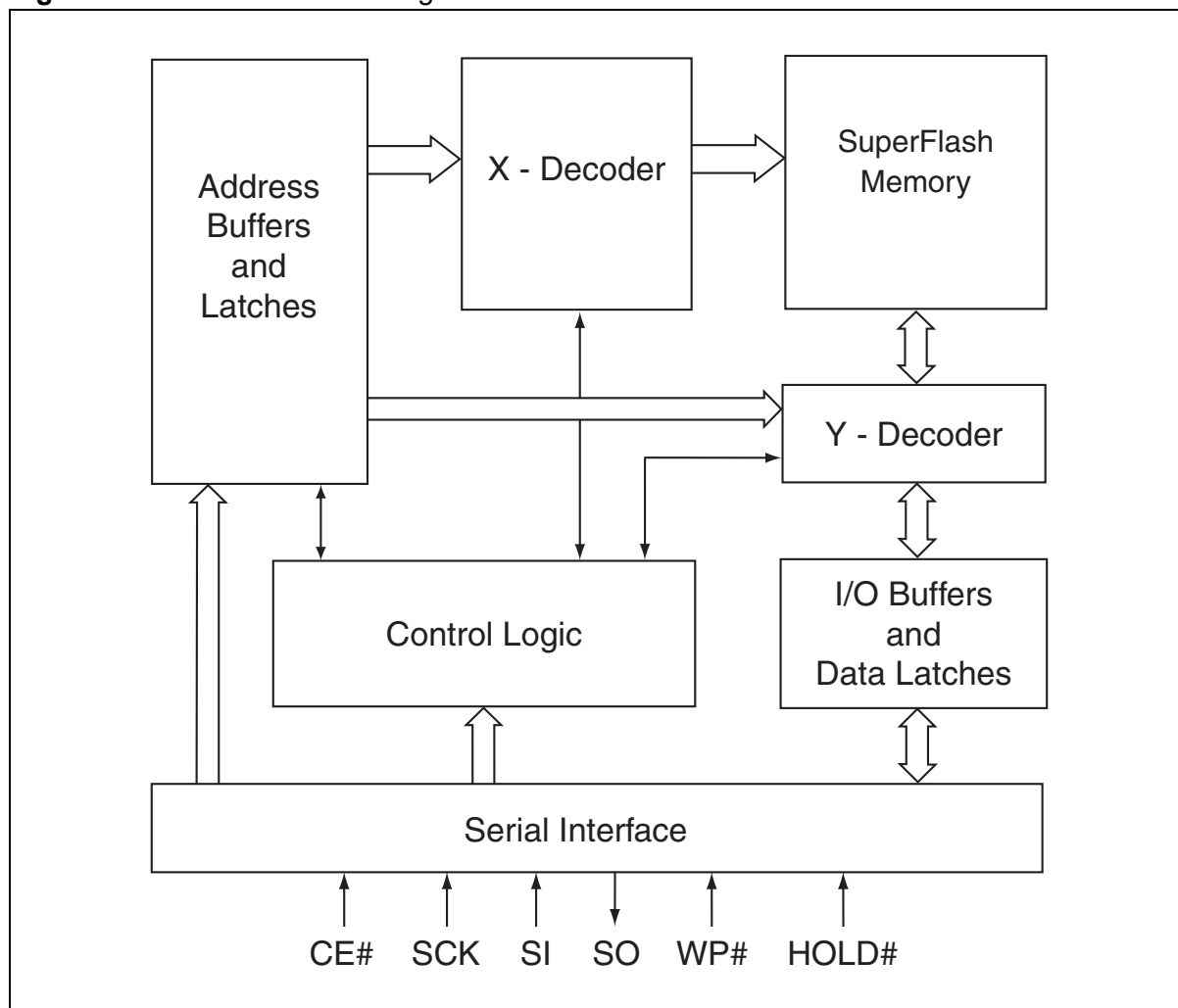
Pin Description
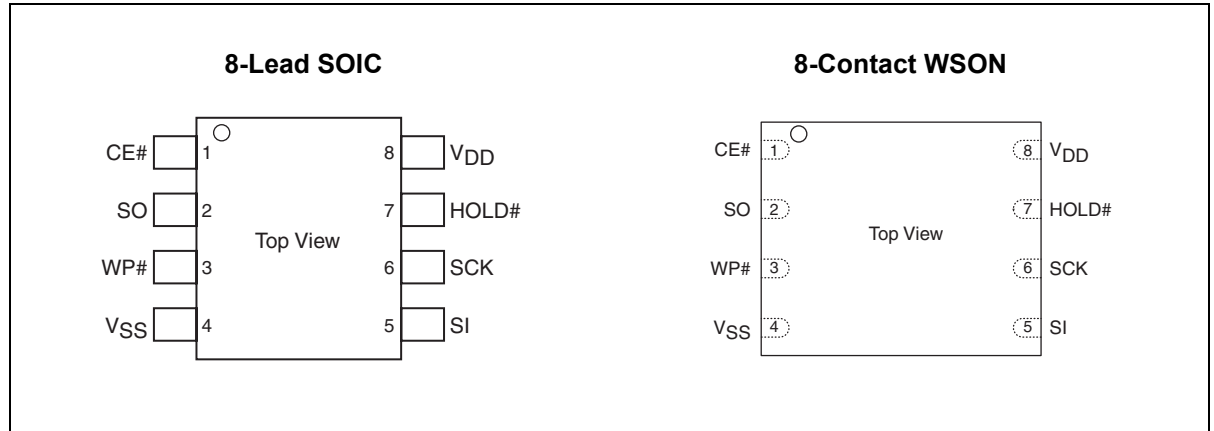
Figure 2: Pin Assignments

Table 1: Pin Description

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses or input data are latched on the rising edge of the clock input, while output data are shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data are shifted out on the falling edge of the serial clock.
CE#	Chip Enable	The device is enabled by a high-to-low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	To enable/disable BPL bit in the STATUS register.
HOLD#	Hold	To temporarily stop serial communication with SPI Flash memory without resetting the device.
V_{DD}	Power Supply	To provide power supply (3.0V-3.6V).
V_{SS}	Ground	

Not Recommended for New Designs

Memory Organization

The SST25LF020A SuperFlash memory array is organized in 4-Kbyte sectors with 32-Kbyte overlay blocks.

Device Operation

The SST25LF020A is accessed through the Serial Peripheral Interface (SPI) bus compatible protocol. The SPI bus consists of four control lines: Chip Enable (CE#) is used to select the device, while data are accessed through the Serial Data Input (SI), Serial Data Output (SO) and Serial Clock (SCK).

The SST25LF020A supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 3, is the state of the SCK signal when the bus host is in Standby mode and no data are being transferred. The SCK signal is low for Mode 0 and high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

Figure 3: SPI Protocol
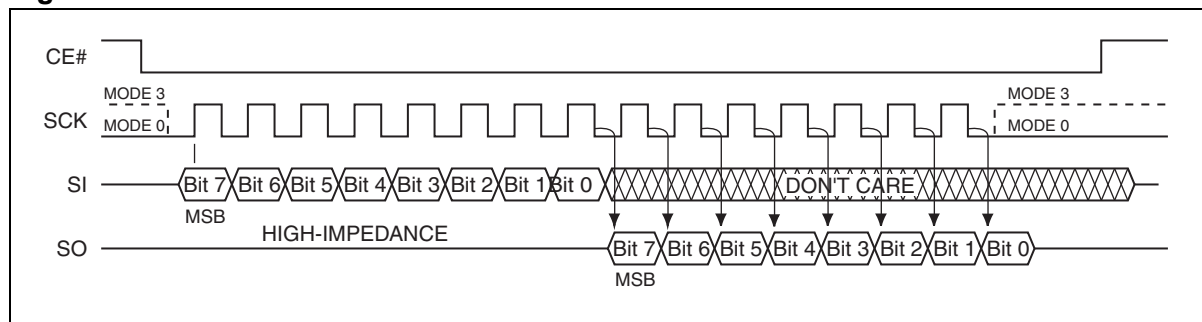
Hold Operation

The HOLD# pin is used to pause a serial sequence underway with the SPI Flash memory without resetting the clocking sequence. To activate HOLD# mode, CE# must be in active-low state. HOLD# mode begins when the SCK active-low state coincides with the falling edge of the HOLD# signal. HOLD# mode ends when the HOLD# signal's rising edge coincides with the SCK active-low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active-low state, then the device enters HOLD# mode when the SCK next reaches the active-low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active-low state, then the device exits in HOLD# mode when the SCK next reaches the active-low state. See Figure 4 for Hold Condition waveform.

Once the device enters HOLD# mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active-high during a Hold condition, it resets the internal logic of the device. As long as the HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active-high, and CE# must be driven active-low. See Figure 19 for Hold timing.

Figure 4: Hold Condition Waveform
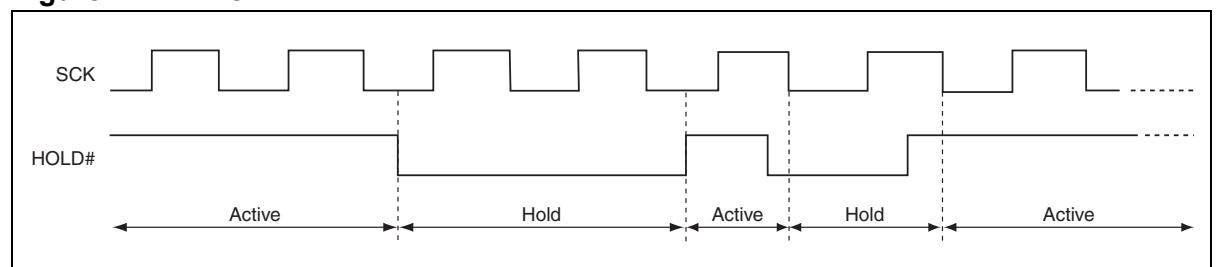
Write Protection

SST25LF020A provides software Write protection. The Write Protect pin (WP#) enables or disables the lock-down function of the STATUS register. The Block Protection bits (BP1, BP0 and BPL) in the STATUS register provide Write protection to the memory array and the STATUS register. See Table 4 for Block Protection description.

Write Protect Pin (WP#)

The Write Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the STATUS register. When WP# is driven low, the execution of the Write Status Register (WRSR) instruction is determined by the value of the BPL bit (see Table 2). When WP# is high, the lock-down function of the BPL bit is disabled.

Table 2: Conditions to execute Write Status Register (WRSR) Instruction

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

STATUS Register

The software STATUS register provides status on whether the Flash memory array is available for any Read or Write operation, whether the device is Write enabled and the state of the memory Write protection. During an internal Erase or Program operation, the STATUS register may be read only to determine the completion of an operation in progress. Table 3 describes the function of each bit in the software STATUS register.

Table 3: Software STATUS Register

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (see Table 4)	1	R/W
3	BP1	Indicate current level of block write protection (see Table 4)	1	R/W
4:5	RES	Reserved for future use	0	N/A
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte Program mode	0	R
7	BPL	1 = BP1, BP0 are read-only bits 0 = BP1, BP0 are read/writable	0	R/W

Busy

The BUSY bit determines whether there is an internal Erase or Program operation in progress. A '1' for the BUSY bit indicates the device is busy with an operation in progress. A '0' indicates the device is ready for the next valid operation.

Write Enable Latch (WEL)

The Write Enable Latch bit indicates the status of the internal memory Write Enable Latch. If the Write Enable Latch bit is set to '1', it indicates the device is write enabled. If the bit is set to '0' (Reset), it indicates the device is not write enabled and does not accept any memory write (Program/Erase) commands. The Write Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Byte Program instruction completion
- Auto Address Increment (AAI) programming reached its highest memory address
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion

Block Protection (BP1, BP0)

The Block Protection (BP1, BP0) bits define the size of the memory area, as defined in Table 4, to be software protected against any memory write (Program or Erase) operations. The Write Status Register (WRSR) instruction is used to program the BP1 and BP0 bits as long as WP# is high or the Block Protect Lock (BPL) bit is '0'. Chip Erase can only be executed if Block Protection bits are both '0'. After power-up, BP1 and BP0 are set to '1'.

Block Protection Lock-Down (BPL)

WP# pin driven low (V_{IL}) enables the Block Protection Lock-Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BPL, BP1 and BP0 bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is "don't care". After power-up, the BPL bit is reset to '0'.

Table 4: Software STATUS Register Block Protection[1]

Protection Level	STATUS Register Bit		Protected Memory Area
	BP1	BP0	2 Mbit
0	0	0	None
1 (1/4 Memory Array)	0	1	030000H-03FFFFH
2 (1/2 Memory Array)	1	0	020000H-03FFFFH
3 (Full Memory Array)	1	1	000000H-03FFFFH

T4.

1. Default at power-up for BP1 and BP0 is '11'.

Auto Address Increment (AAI)

The Auto Address Increment Programming Status bit provides status on whether the device is in AAI programming mode or Byte Program mode. The default at power up is Byte Program mode.

Instructions

Instructions are used to read, write (Erase and Program) and configure the SST25LF020A. The instruction bus cycles are 8 bits each for commands (Op Code), data and addresses. Prior to executing any Byte Program, Auto Address Increment (AAI) programming, Sector Erase, Block Erase or Chip Erase instructions, the Write Enable (WREN) instruction must be executed first. The complete list of the instructions is provided in Table 5. All instructions are synchronized off a high-to-low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the Most Significant bit (MSb). CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID and Read Status Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to Standby mode. Instruction commands (Op Code), addresses and data are all input from the Most Significant bit first.

Table 5: Device Operation Instructions[1]

Cycle Type/ Operation[2,3]	Max Freq MHz	Bus Cycle[4]											
		1		2		3		4		5		6	
		S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}
Read	20	03H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	X	D_{OUT}	—	—
High-Speed Read	33	0BH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	X	X	X	D_{OUT}
Sector Erase[5,6]		20H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	—	—	—	—
Block Erase[5,7]		52H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	—	—	—	—
Chip Erase[6]		60H	Hi-Z	—	—	—	—	—	—	—	—	—	—
Byte Program[6]		02H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	D_{IN}	Hi-Z	—	—
Auto Address Increment (AAI) Single-Byte Program[6,8]		AFH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	D_{IN}	Hi-Z	—	—
Read Status Register (RDSR)		05H	Hi-Z	X	D_{OUT}	—	Note 9	—	Note 9	—	Note[9]	—	—
Enable Write Status Register (EWSR)[10]		50H	Hi-Z	—	—	—	—	—	—	—	—	—	—
Write Status Register (WRSR)[10]		01H	Hi-Z	Data	Hi-Z	—	—	—	—	—	—	—	—
Write Enable (WREN)		06H	Hi-Z	—	—	—	—	—	—	—	—	—	—
Write Disable (WRDI)		04H	Hi-Z	—	—	—	—	—	—	—	—	—	—
Read ID		90H or ABH	Hi-Z	00H	Hi-Z	00H	Hi-Z	ID Addr 11	Hi-Z	X	D_{OUT} 12	—	—

1. A_{MS} = Most Significant Address
   A_{MS} = A_{17} for SST25LF020A
   Address bits above the most significant bit of each density can be V_{IL} or V_{IH}
2. Operation: S_{IN} = Serial In, S_{OUT} = Serial Out
3. X = Dummy Input Cycles (V_{IL} or V_{IH}); - = Non-Applicable Cycles (Cycles are not necessary)
4. One bus cycle is eight clock periods.
5. Sector addresses: use A_{MS}-A_{12}, remaining addresses can be V_{IL} or V_{IH}
6. Prior to any Byte Program, AAI Program, Sector Erase, Block Erase, or Chip Erase operation, the Write Enable (WREN) instruction must be executed.

7. Block addresses for: use A_{MS}-A_{15}, remaining addresses can be V_{IL} or V_{IH}
8. To continue programming to the next sequential address location, enter the 8-bit command, AFH, followed by the data to be programmed.
9. The Read Status Register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.
10. The Enable Write Status Register (EWSR) instruction and the Write Status Register (WRSR) instruction must work in conjunction with each other. The WRSR instruction must be executed immediately (very next bus cycle) after the EWSR instruction to make both instructions effective.
11. Manufacturer's ID is read with A_0=0, and Device ID is read with A_0=1. All other address bits are 00H. The Manufacturer and Device ID output stream is continuous until terminated by a low to high transition on CE#
12. Device ID = 43H for SST25LF020A

Read (20 MHz)

The Read instruction supports up to 20 MHz. It outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically increment to the beginning (wrap-around) of the address space, i.e., for 2 Mbit density, once the data from address location 3FFFFH had been read, the next output will be from address location 00000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A_{23}-A_0]. CE# must remain active-low for the duration of the Read cycle. See Figure 5 for the Read sequence.

Figure 5: Read Sequence
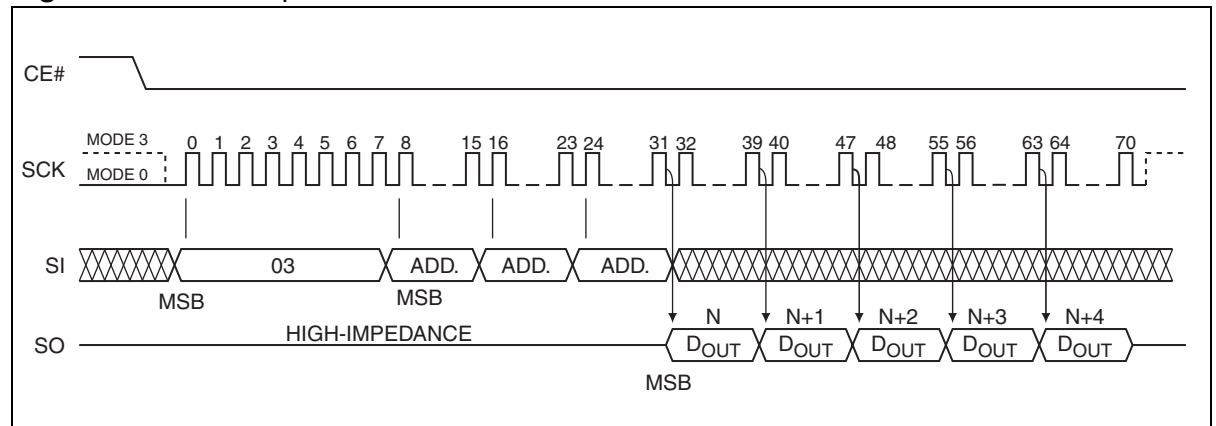
High-Speed Read (33 MHz)

The High-Speed Read instruction supporting up to 33 MHz is initiated by executing an 8-bit command, 0BH, followed by address bits [A_{23}-A_0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 6 for the High-Speed Read sequence.

Following a dummy byte (8 clocks input dummy cycle), the High-Speed Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal Address Pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the Address Pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 2 Mbit density, once the data from address location 03FFFFH has been read, the next output will be from address location 000000H.

Figure 6: High-Speed Read Sequence

Note: X = Dummy Byte: 8 Clocks Input Dummy Cycle (V_{IL} or V_{IH})
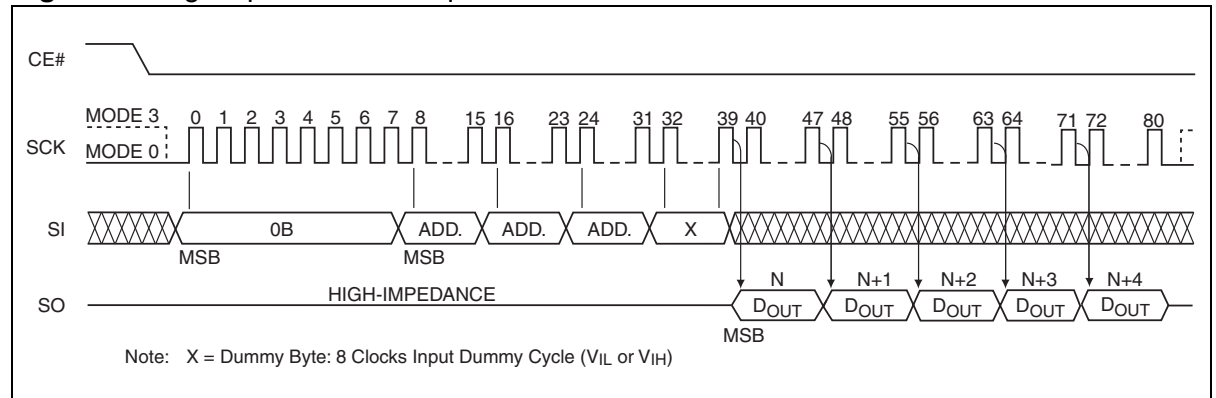
Byte Program

The Byte Program instruction programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a program operation. A Byte Program instruction applied to a protected memory area will be ignored.

Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Byte Program instruction. The Byte Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A_{23}-A_0]. Following the address, the data are input in order from MSb (bit 7) to LSb (bit 0). CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{BP} for the completion of the internal self-timed Byte Program operation. See Figure 7 for the Byte Program sequence.

Figure 7: Byte Program Sequence
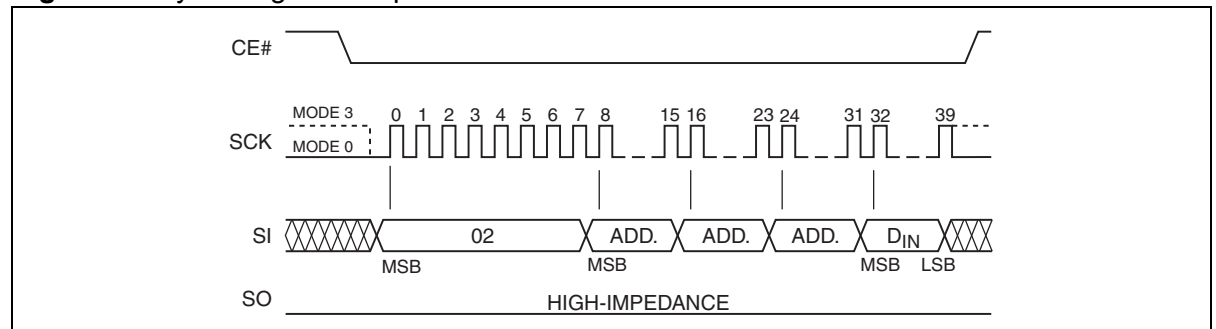
Auto Address Increment (AAI) Program

The AAI program instruction allows multiple bytes of data to be programmed without reissuing the next sequential address location. This feature decreases total programming time when the entire memory array is to be programmed. An AAI program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI program instruction.

Prior to any write operation, the Write Enable (WREN) instruction must be executed. The AAI program instruction is initiated by executing an 8-bit command, AFH, followed by address bits [A_{23}-A_0]. Following the addresses, the data are input sequentially from MSb (bit 7) to LSb (bit 0). CE# must be driven high before the AAI program instruction is executed. The user must poll the BUSY bit in the software STATUS register or wait T_{BP} for the completion of each internal self-timed Byte Program cycle. Once the device completes the programming byte, the next sequential address may be programmed by entering the 8-bit command, AFH, followed by the data to be programmed. When the last desired byte has been programmed, execute the Write Disable (WRDI) instruction, 04H, to terminate AAI. After execution of the WRDI command, the user must poll the STATUS register to ensure the device completes programming. See Figure 8 for the AAI programming sequence.

There is no wrap mode during AAI programming. Once the highest unprotected memory address is reached, the device will exit AAI operation and reset the Write Enable Latch bit (WEL = 0).

Figure 8: Auto Address Increment (AAI) Program Sequence
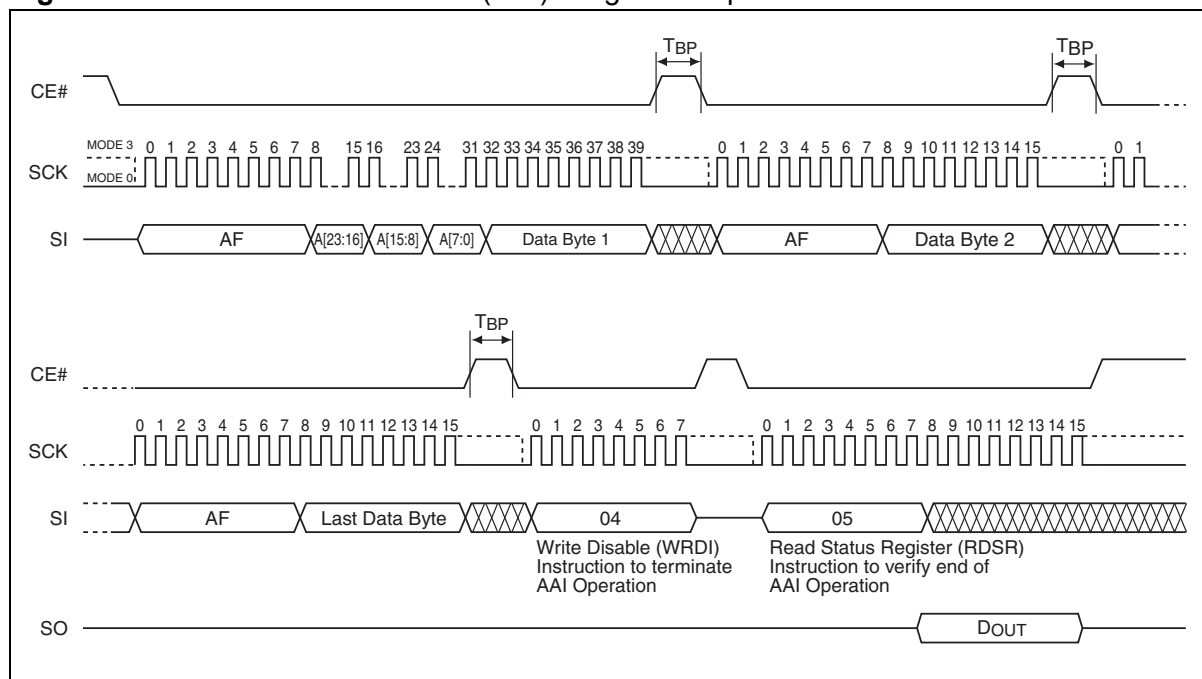
Sector Erase

The Sector Erase instruction clears all bits in the selected 4-Kbyte sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{12}] (A_{MS} = Most Significant address) are used to determine the sector address (SA$_X$), and remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{SE} for the completion of the internal self-timed Sector Erase cycle. See Figure 9 for the Sector Erase sequence.

Figure 9: Sector Erase Sequence
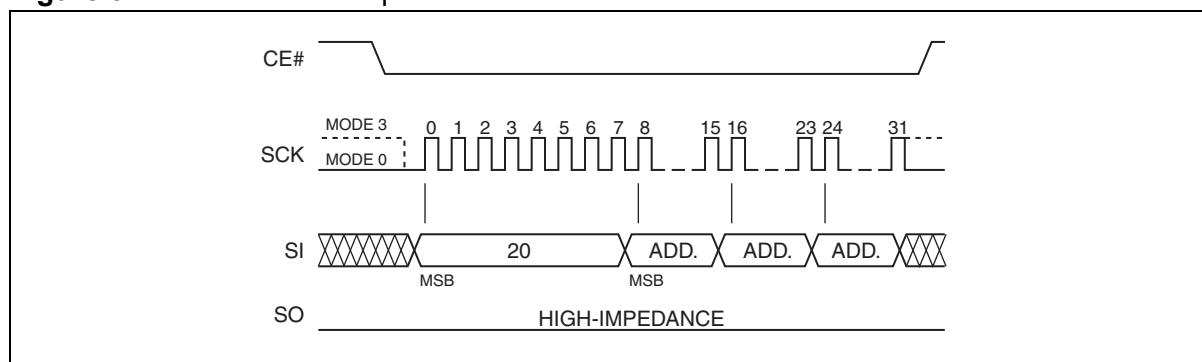
Block Erase

The Block Erase instruction clears all bits in the selected 32-Kbyte block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The Block Erase instruction is initiated by executing an 8-bit command, 52H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{15}] (A_{MS} = Most significant address) are used to determine block address (BA$_X$), and remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{BE} for the completion of the internal self-timed Block Erase cycle. See Figure 10 for the Block Erase sequence.

Figure 10: Block Erase Sequence
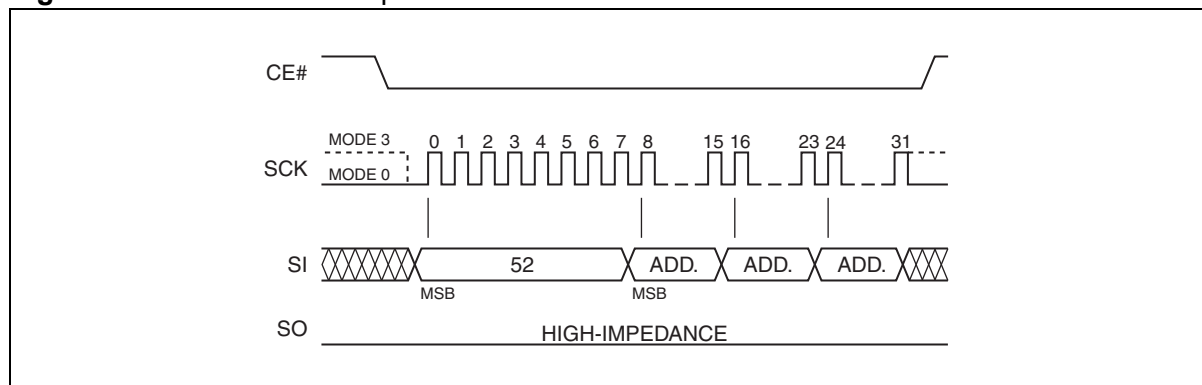
Chip Erase

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction will be ignored if any of the memory area is protected. Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Chip Erase instruction sequence. The Chip Erase instruction is initiated by executing an 8-bit command, 60H. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait T_{CE} for the completion of the internal self-timed Chip Erase cycle. See Figure 11 for the Chip Erase sequence.

Figure 11: Chip Erase Sequence
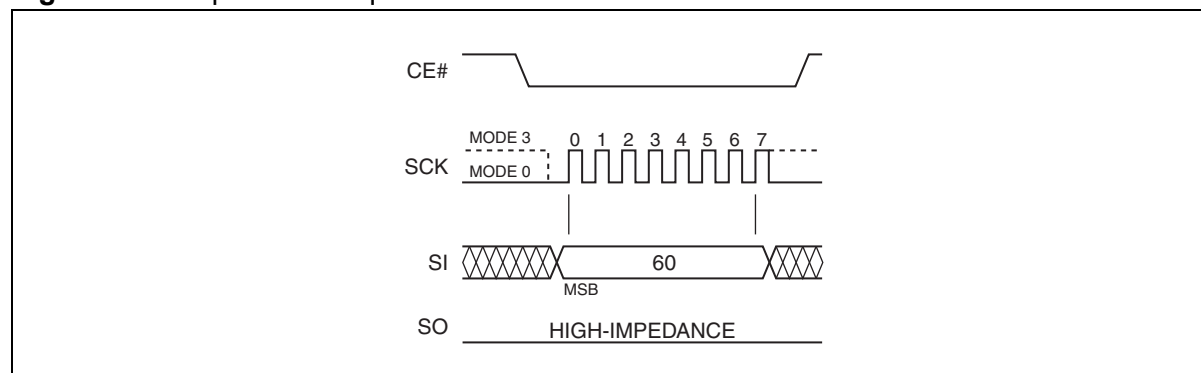
Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows reading of the STATUS register. The STATUS register may be read at any time even during a write (Program/Erase) operation. When a write operation is in progress, the BUSY bit may be checked before sending any new commands to assure that the new commands are properly received by the device. CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read Status Register is continuous with ongoing clock cycles until it is terminated by a low-to-high transition of the CE#. See Figure 12 for the RDSR instruction sequence.

Figure 12: Read Status Register (RDSR) Sequence
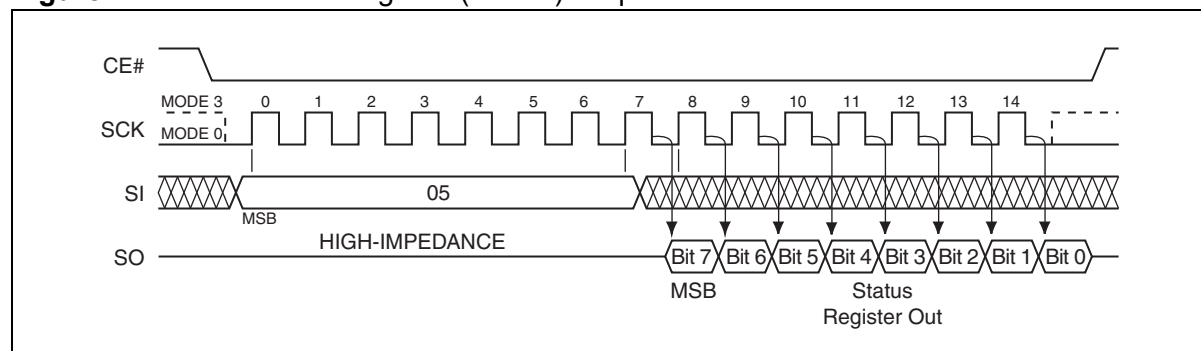
Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write Enable Latch bit to '1', allowing write operations to occur. The WREN instruction must be executed prior to any write (Program/Erase) operation. CE# must be driven high before the WREN instruction is executed.
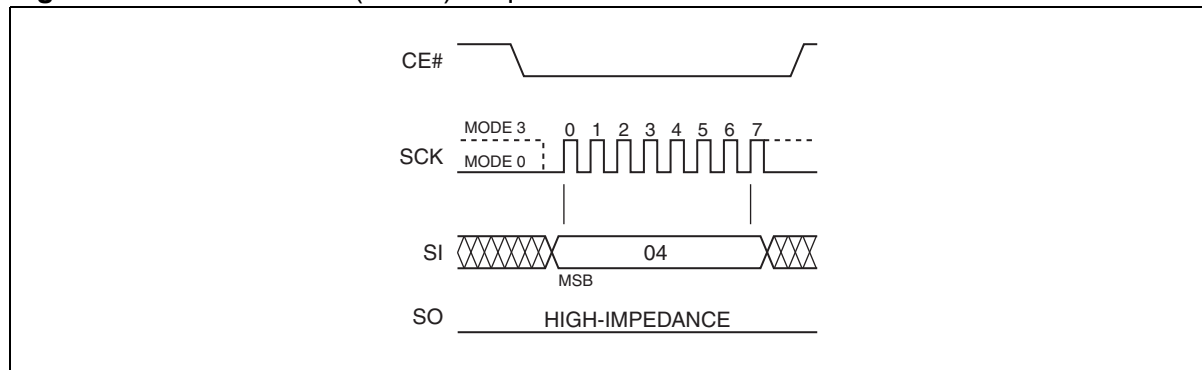
Figure 13: Write Enable (WREN) Sequence
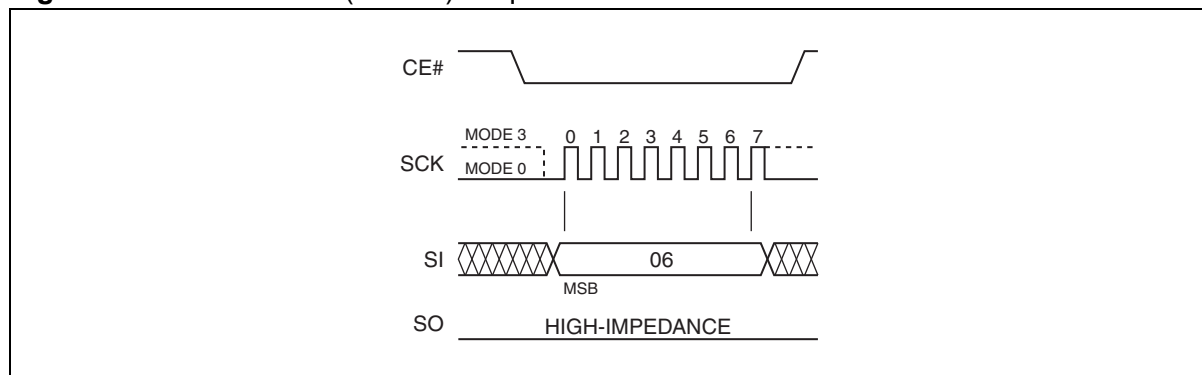
Write Disable (WRDI)

The Write Disable (WRDI) instruction resets the Write Enable Latch bit and AAI bit to '0', disabling any new write operations from occurring. CE# must be driven high before the WRDI instruction is executed.

Figure 14: Write Disable (WRDI) Sequence

Enable Write Status Register (EWSR)

The Enable Write Status Register (EWSR) instruction arms the Write Status Register (WRSR) instruction and opens the STATUS register for alteration. The Enable Write Status Register instruction does not have any effect and will be wasted if it is not followed immediately by the Write Status Register (WRSR) instruction. CE# must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

Write Status Register (WRSR)

The Write Status Register instruction works in conjunction with the Enable Write Status Register (EWSR) instruction to write new values to the BP1, BP0 and BPL bits of the STATUS register. The Write Status Register instruction must be executed immediately after the execution of the Enable Write Status Register instruction (very next instruction bus cycle). This two-step instruction sequence of the EWSR instruction followed by the WRSR instruction works like SDP (software data protection) command structure which prevents any accidental alteration of the STATUS register values. The Write Status Register instruction will be ignored when WP# is low and BPL bit is set to '1'. When the WP# is low, the BPL bit can only be set from '0' to '1' to lock-down the STATUS register, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0 and BP1 bits in the STATUS register can all be changed. As long as the BPL bit is set to '0' or the WP# pin is driven high (V_{IH}) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the BP0, BP1 and BPL bit in the STATUS register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the STATUS register as well as alter the BP0 and BP1 bit at the same time. See Table 2 for a summary description of WP# and BPL functions. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 15 for EWSR and WRSR instruction sequences.

Figure 15: Enable Write Status Register (EWSR) and Write Status Register (WRSR) Sequence
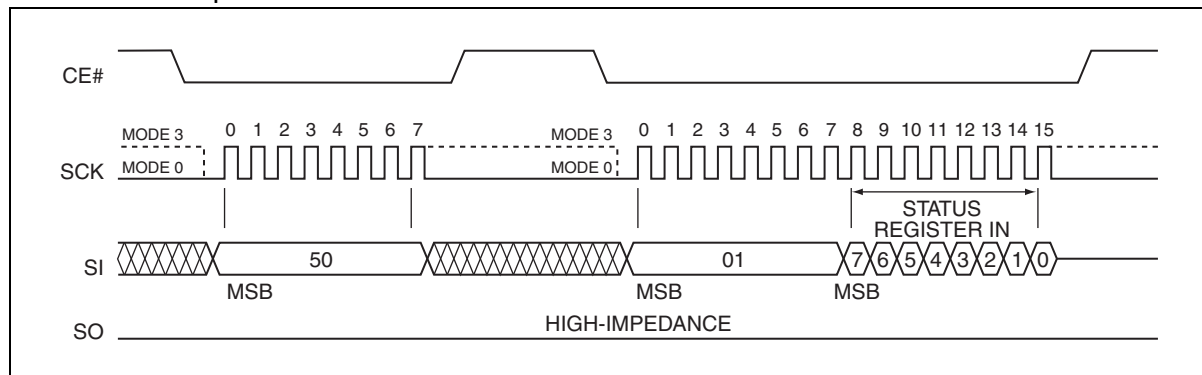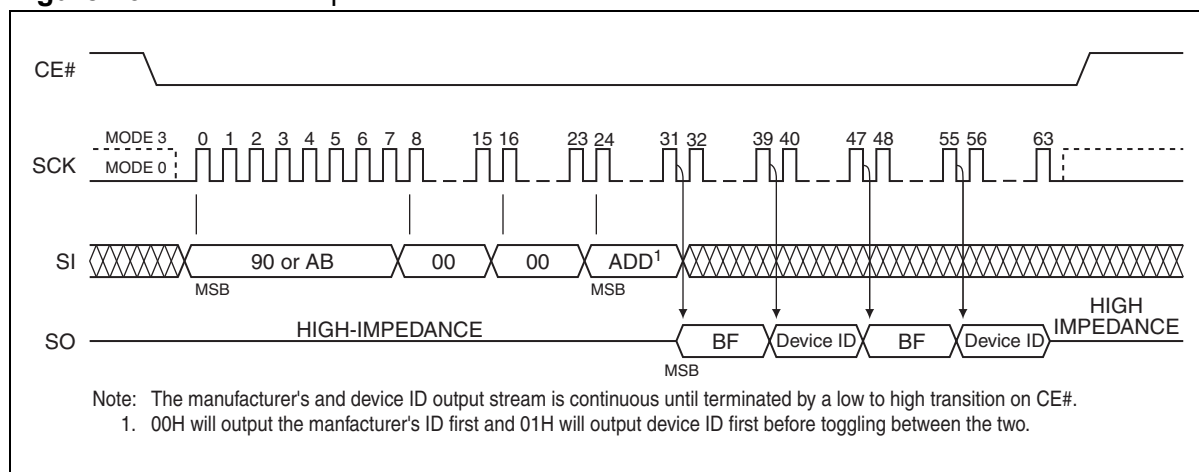
Read ID

The Read ID instruction identifies the devices as SST25LF020A and the manufacturer as Microchip. The device information can be read from executing an 8-bit command, 90H or ABH, followed by address bits [A_{23}-A_0]. Following the Read ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H. Once the device is in Read-ID mode, the manufacturer's and device ID output data toggles between address 00000H and 00001H until terminated by a low-to-high transition on CE#.

Table 6: Product Identification

	Address	Data
Manufacturer's ID	00000H	BFH
Device ID SST25LF020A	00001H	43H

T6.

Figure 16: Read ID Sequence

Note: The manufacturer's and device ID output stream is continuous until terminated by a low to high transition on CE#.
1. 00H will output the manfacturer's ID first and 01H will output device ID first before toggling between the two.

Electrical Specifications

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . -55°C to +125°C

Storage Temperature . . . . -65°C to +150°C

D. C. Voltage on Any Pin to Ground Potential . . . . -0.5V to V_{DD}+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . -2.0V to V_{DD}+2.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Surface Mount Solder Reflow Temperature . . . . 260°C for 10 seconds

Output Short Circuit Current[1] . . . . 50 mA

    1. Output shorted for no more than one second. No more than one output shorted at a time.

Table 7: Operating Range

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	3.0V-3.6V
Industrial	-40°C to +85°C	3.0V-3.6V

Table 8: AC Conditions of Test

Input Rise/Fall Time	Output Load
5ns	C_L = 30 pF

Table 9: DC Operating Characteristics V_{DD} = 3.0V-3.6V

| Symbol | Parameter | Limits | | Units | Test Conditions |
		Min	Max		
I_{DDR}	Read Current	—	10	mA	CE#=0.1 V_{DD}/0.9 V_{DD}@20 MHz, SO=open
I_{DDW}	Program and Erase Current	—	30	mA	CE#=V_{DD}
I_{SB}	Standby Current	—	15	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{LI}	Input Leakage Current	—	1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current	—	1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage	—	0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}	—	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage	—	0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2	—	V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

Table 10: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	10	μs
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	10	μs

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 11: Capacitance (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 12: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 13: AC Operating Characteristics V_{DD} = 3.0V-3.6V

Symbol	Parameter	20 MHz Min	20 MHz Max	33 MHz Min	33 MHz Max	Units
F_{CLK}	Serial Clock Frequency	—	20	—	33	MHz
T_{SCKH}	Serial Clock High Time	20	—	13	—	ns
T_{SCKL}	Serial Clock Low Time	20	—	13	—	ns
T_{CES}[1]	CE# Active Setup Time	20	—	12	—	ns
T_{CEH}[1]	CE# Active Hold Time	20	—	12	—	ns
T_{CHS}[1]	CE# Not Active Setup Time	10	—	10	—	ns
T_{CHH}[1]	CE# Not Active Hold Time	10	—	10	—	ns
T_{CPH}	CE# High Time	100	—	100	—	ns
T_{CHZ}	CE# High to High-Z Output	—	20	—	14	ns
T_{CLZ}	SCK Low to Low-Z Output	0	—	0	—	ns
T_{DS}	Data In Setup Time	5	—	3	—	ns
T_{DH}	Data In Hold Time	5	—	3	—	ns
T_{HLS}	HOLD# Low Setup Time	10	—	10	—	ns
T_{HHS}	HOLD# High Setup Time	10	—	10	—	ns
T_{HLH}	HOLD# Low Hold Time	15	—	10	—	ns
T_{HHH}	HOLD# High Hold Time	10	—	10	—	ns
T_{HZ}	HOLD# Low to High-Z Output	—	20	—	14	ns
T_{LZ}	HOLD# High to Low-Z Output	—	20	—	14	ns
T_{OH}	Output Hold from SCK Change	0	—	0	—	ns
T_V	Output Valid from SCK	—	20	—	12	ns
T_{SE}	Sector Erase	—	25	—	25	ms
T_{BE}	Block Erase	—	25	—	25	ms
T_{SCE}	Chip Erase	—	100	—	100	ms
T_{BP}	Byte Program	—	20	—	20	µs

1. Relative to SCK.

Figure 17: Serial Input Timing Diagram
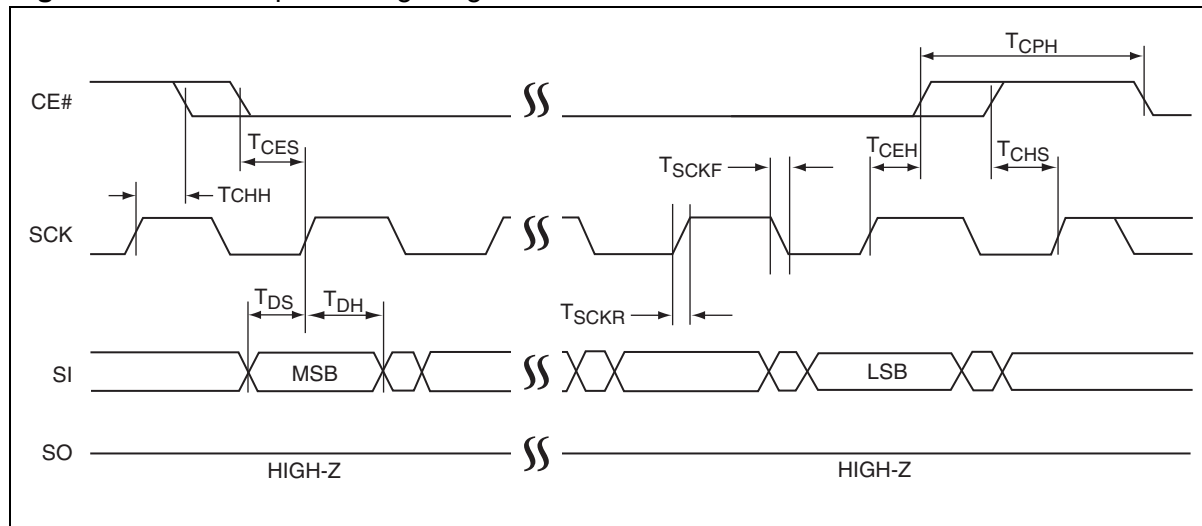
Figure 18: Serial Output Timing Diagram
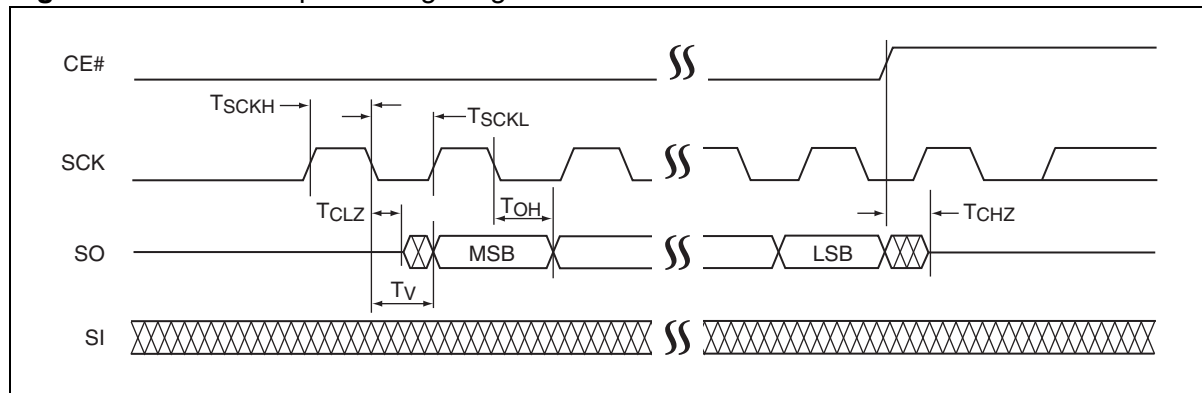
Figure 19: Hold Timing Diagram
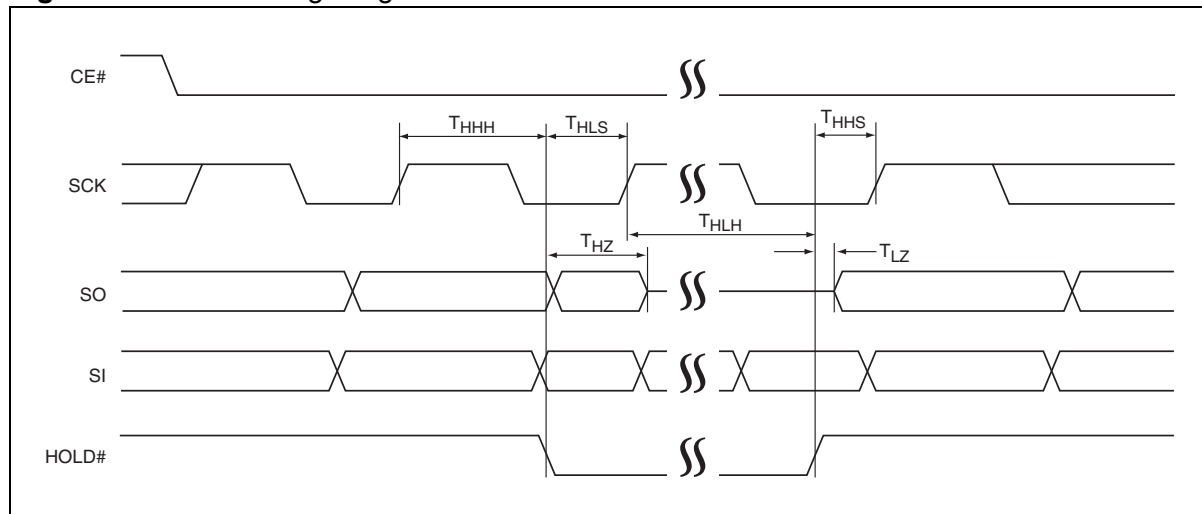
Figure 20: Power-Up Timing Diagram
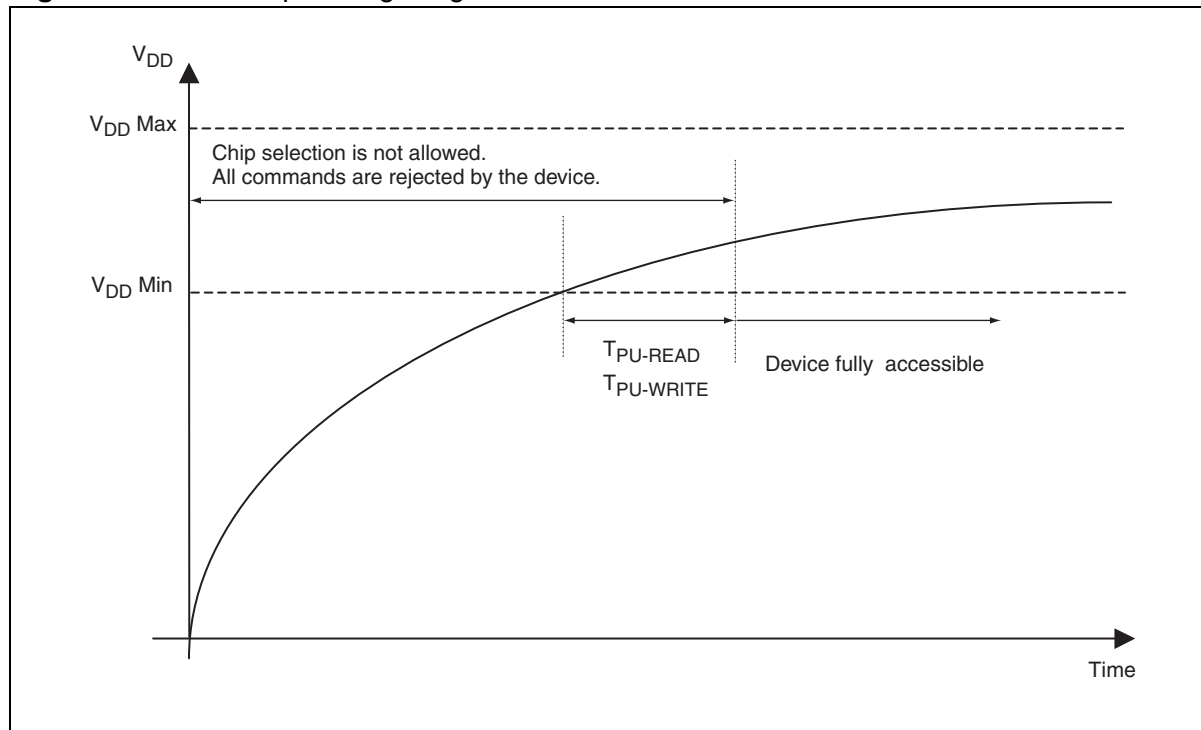
Figure 21: AC Input/Output Reference Waveforms

AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic "1" and V_{ILT} ($0.1V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are V_{HT} ($0.7V_{DD}$) and V_{LT} ($0.3V_{DD}$). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test
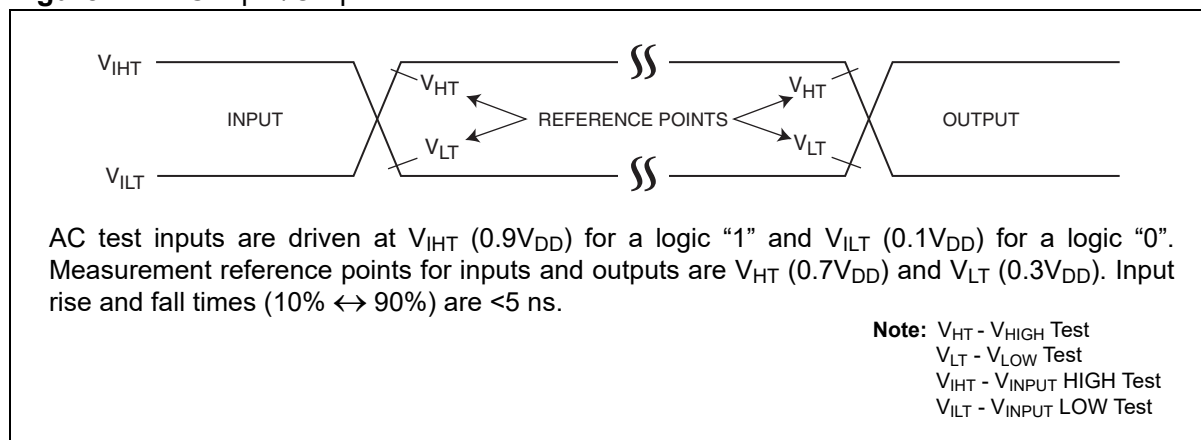
Figure 22: A Test Load Example

Not Recommended for New Designs

Product Ordering Information

SST	25	LF	020A	-	33	-	4I	-	QAE
XX	XX	XXXX	-	XX	-	XX	-	XXX

Environmental Attribute
E[1] = non-Pb

Package Modifier
A = 8 leads or contacts

Package Type
S = SOIC 150 mil body width
Q = WSON

Operation Temperature
C = Commercial = 0°C to +70°C
I = Industrial = -40°C to +85°C

Minimum Endurance
4 = 10,000 cycles

Operating Frequency
33 = 33 MHz

Device Density
020 = 2 Mbit

Voltage
L = 3.0-3.6V

Product Series
25 = Serial Peripheral Interface
flash memory

1. Environmental suffix "E" denotes non-Pb solder. Non-Pb solder devices are "RoHS Compliant".

Valid combinations for SST25LF020A

SST25LF020A-33-4C-SAE	SST25LF020A-33-4C-QAE
SST25LF020A-33-4I-SAE	SST25LF020A-33-4I-QAE
SST25LF020A-33-4C-SAE-T	SST25LF020A-33-4C-QAE-T
SST25LF020A-33-4I-SAE-T	SST25LF020A-33-4I-QAE-T

Note: Valid combinations are those products in mass production or will be in mass production. Consult your sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Packaging Diagrams

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Figure 23: 8-lead Small Outline Integrated Circuit (SOIC) 150 mil body width (4.9mm x 6mm) SST Package Code: SA
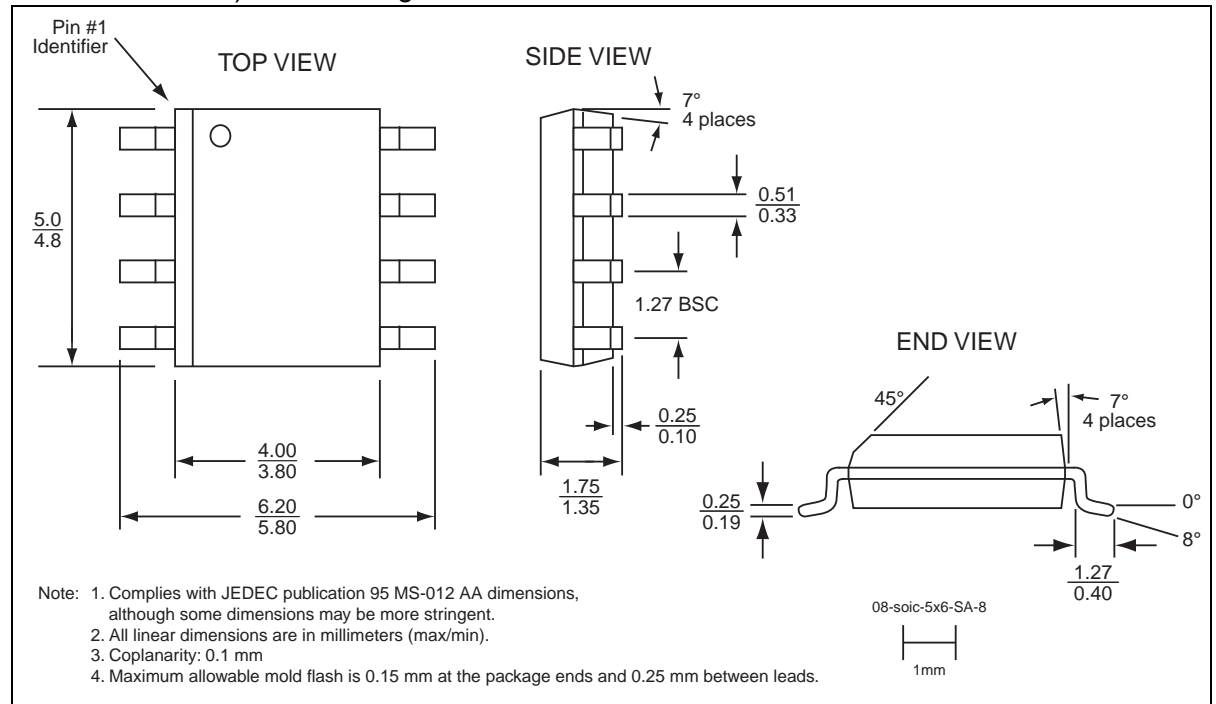
Note: 1. Complies with JEDEC publication 95 MS-012 AA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Figure 24: 8-contact Very-very-thin Small Outline No-lead (WSON) SST Package Code: QA
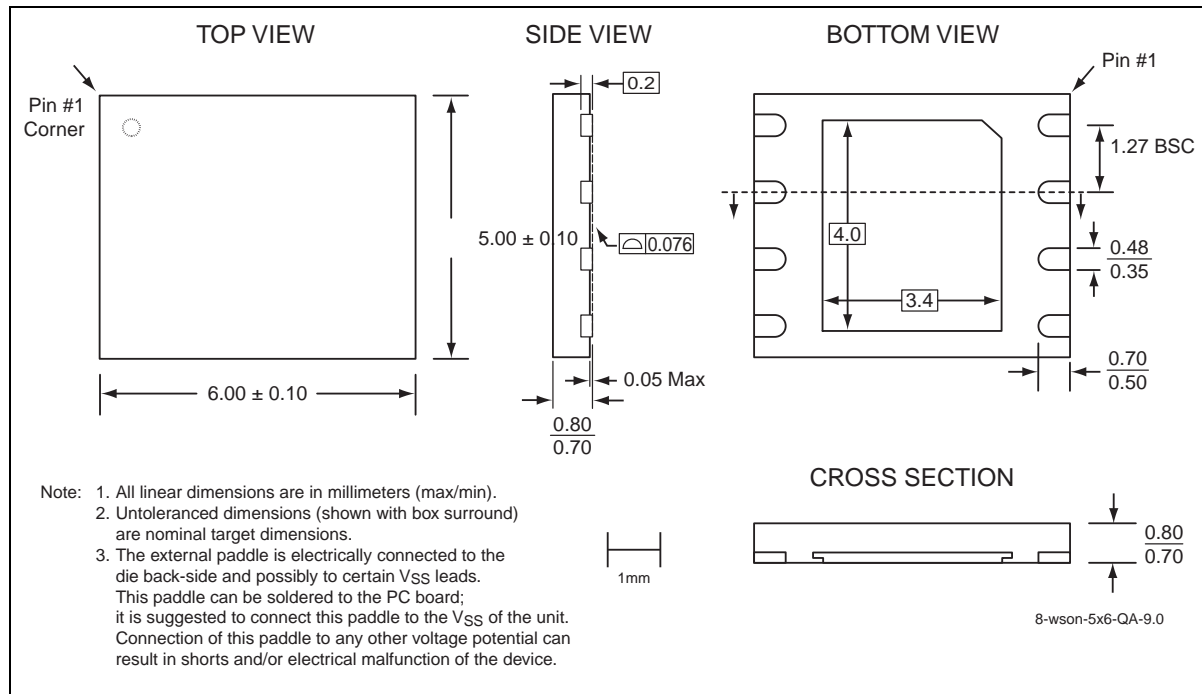
Table 14: Revision History

Revision	Description	Date
00	• Initial release of S71242	Aug 2003
01	• Added new 8-SOIC (S2A) package and associated MPNs	Oct 2003
02	• 2004 Data Book • Updated the Package Outline for S2A	Dec 2003
03	• Document status changed from "Advance Information" to "Preliminary Specifications" • Added Commercial and Extended temperatures and associated MPNs	Jun 2004
04	• Revised Absolute Max. Stress Ratings for Surface Mount Solder Reflow Temp. • Migrated document from Preliminary Specifications to Data Sheet	Nov 2005
05	• Updated QA package drawing to version 9. • Removed leaded part numbers. • Added footnote to Product Ordering Information section.	Jan 2006
06	• End of life all valid combinations of SST25LF040A. See S71242(01)	Mar 2009
07	• Removed 4Mbit information inadvertently missed in last EOL revision	Jan 2010
A	• Applied new document format • Released document under letter revision system • Updated Spec number from S71242 to DS25080	Nov 2011
B	• Deleted Extended temperature option.	May 2023

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