TMC2005-JT

ARCNET 5 Port HUB Controller

FEATURES

- ARCNET HUB Circuit for ARCNET Protocol (Data Rate From 156.25Kbps to 10Mbps)
- Able to Connect Various Transceivers Directly
- Device Includes TX/RX Timing Circuit for 5 Port Hub and Direction Control Circuit, Jitter Correct Circuit and Noise Cancel Circuit
- Easy to Design 8 or 12 Port Hub
- Can Connect with HYC9088 in Normal Mode
- Can Connect with RS485 Transceiver, HYC5000/4000/2000, Opt Module and TTL Interface in Backplane Mode
- Supports both Normal and Backplane Mode at the Same Time for Media Conversion
- + 5V Single Power

GENERAL DESCRIPTION

When configuring a network, the maximum number of nodes and the maximum cable length are limited by the electric capacity of the transceiver. In this case, the network is expanded by an equipment called a “HUB” or “repeater”. It maybe necessary to have a converter between coax, T/P and the fiber cable. It is easy to design a HUB or a repeater because the TMC2005 has various features for expanding such network.

It can connect with HYC9088, RS485 transceiver, HYC5000/4000/2000 and TTL interface for optical module. It can connect with three different transceivers at the same time and convert the media of each. (The data rate cannot be converted. It is necessary to operate all nodes in the same network at the same data rate). The Hubs can be expanded by connecting two or more TMC2005 chips. By setting one of 5 ports to open-drain output, the Hub can be expanded to either 12 or 16 ports.

ORDERING INFORMATION

Order Number(s):

TMC2005-JT for 64 pin, TQFP Lead-Free RoHS Compliant Package

DATASHEET

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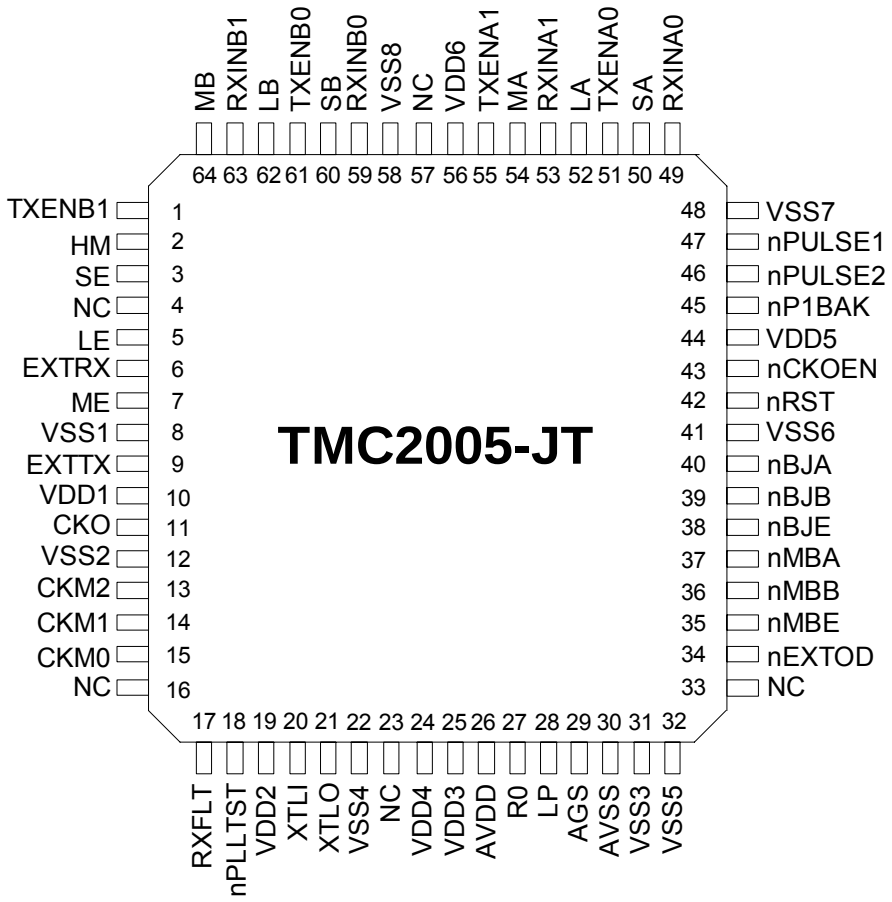
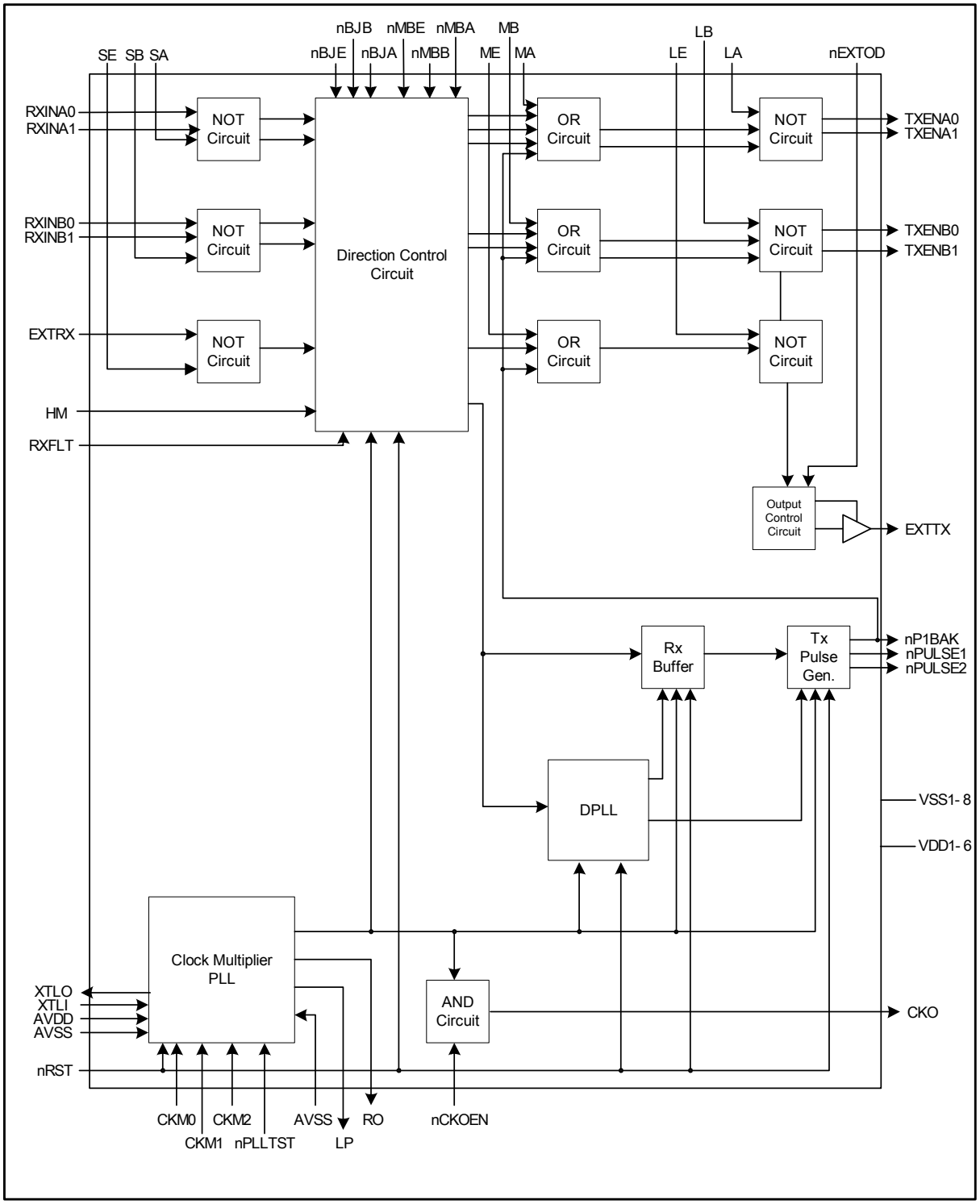
PIN CONFIGURATION



BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	INPUT/OUTPUT	DESCRIPTION	NOTE
1	TXENB1	OUTPUT	Port B-1 Tx output to media transceiver	
2	HM	INPUT	Setting for traffic release time (It should be open for normal operation.)	Pull-up
3	SE	INPUT	Port EXT. Polar assignment for EXTRX input (0:active Hi, 1:active Low)	Pull-up
4	NC		Reserved. It should be open.	
5	LE	INPUT	Port EXT. Polar assignment of EXTTX output (0:active Low, 1:active Hi)	Pull-up
6	EXTRX	INPUT	Port EXT. RX-Data input from media transceiver.	Pull-up
7	ME	INPUT	Port EXT. Output mode assignment of EXTTX (0:pulse output, 1:Tx control output)	Pull-up
8	VSS1		Ground	
9	EXTTX	OUTPUT	Port EXT. Output to media transceiver.	
10	VDD1		Power Supply	
11	CKO	OUTPUT	Clock Output	
12	VSS2		Ground	
13	CKM2	INPUT	Network speed (data rate) setting.	Pull-up
14	CKM1	INPUT		Pull-up
15	CKM0	INPUT		Pull-up
16	NC		Reserved. It should be open.	
17	RXFLT	INPUT	Test Pin. It should be open.	Pull-up
18	nPLLTST	INPUT	Test Pin for PLL.. It should connected to VDD (Set to high)	
19	VDD2		Power Supply	
20	XTLI	INPUT	X'tal input/External clock input.	
21	XTLO	OUTPUT	X'tal output	
22	VSS4		Ground	
23	NC		Reserved. It should be open.	
24	VDD4		Power Supply	
25	VDD3		Power Supply	
26	AVDD		Analog Power Supply	
27	RO	OUTPUT	VCO output for internal PLL.	
28	LP	OUTPUT	Connection pin to loop filter for internal PLL.	
29	AGS	INPUT	Analog sense pin for internal PLL.	
30	AVSS		Analog Ground	
31	VSS3		Ground	
32	VSS5		Ground	
33	NC		Reserved. It should be open.	
34	nEXTOD	INPUT	Port EXT. Open-drain mode (0:open-drain output, 1:normal output)	Pull-up
35	nMBE	INPUT	Port EXT. Noise cut (0:on, 1:off)	Pull-up
36	nMBB	INPUT	Port A0/A1 Noise cut (0:on, 1:off)	Pull-up
37	nMBA	INPUT	Port B0/B1 Noise cut (0:on, 1:off)	Pull-up
38	nBJE	INPUT	Port EXT. Jitters correct mode (0:big jitters mode, 1:normal mode)	Pull-up
39	nBJB	INPUT	Port A0/A1 Jitters correct mode (0:big jitter mode, 1:normal mode)	Pull-up
40	nBJA	INPUT	Port B0/B1 Jitter correct mode (0:big jitter mode, 1:normal mode)	Pull-up
41	VSS6		Ground	
42	nRST	INPUT	Internal reset signal (active Low)	Pull-up
43	nCKOEN	INPUT	Enable of CKO output.	Pull-up

PIN NO.	NAME	INPUT/OUTPUT	DESCRIPTION	NOTE
44	VDD5		Power Supply.	
45	nP1BAK	OUTPUT	nPULSE1 output (for backplane mode).	
46	nPULSE2	OUTPUT	nPULSE2 output (for normal mode).	
47	nPULSE1	OUTPUT	nPULSE1 output (for normal mode)	
48	VSS7		Ground	
49	RXINA0	INPUT	Port A-0 Rx-data input from media transceiver.	Pull-up
50	SA	INPUT	Port A. Polar assignment for RXINA0/A1 output (0:active Hi, 1:active Low)	Pull-up
51	TXENA0	OUTPUT	Port A-0 Tx output to media transceiver.	
52	LA	INPUT	Port A. Polar assignment for TXENA0/A1 output (0:active Low, 1:active Hi)	Pull-up
53	RXINA1	INPUT	Port A-1 Rx-data input from media transceiver.	Pull-up
54	MA	INPUT	Port A. Mode assignment for TXENA0/A1 (0:pulse output, 1:Tx control output)	Pull-up
55	TXENA1	OUTPUT	Port A-1 Tx output to media transceiver.	
56	VDD6		Power Supply	
57	NC		Reserved. It should be open.	
58	VSS8		Ground	
59	RXINB0	INPUT	Port B-0 Rx-data input from media transceiver.	Pull-up
60	SB	INPUT	Port B. Polar assignment for RXINA0/A1 input (0:active Hi, 1:Active Low)	Pull-up
61	TXENB0	OUTPUT	Port B-0 Tx output to media transceiver.	
62	LB	INPUT	Port B. Polar assignment for TXENA0/A1 output (0:active Low, 1:active Hi)	Pull-up
63	RXINB1	INPUT	Port B-1 Rx-data input from media transceiver.	Pull-up
64	MB	INPUT	Port B. Mode assignment for TXENA0/A1 (0:pulse output, 1:TX control output)	Pull-up

Note: Pull-up: Input with a pull-up resistor 70KΩ ± 30%

TX/RX Interface

	FEATURE	NAME	INPUT/OUTPUT	DESCRIPTION
RX Port		RXINA [0:1] RXINB [0:1] EXTRX	INPUT	Setup the polarity by SA, SB, SE.
RX Port	Polar Assignment	SA, SB, SE	INPUT	Setup the polarity of RXINA [0:1], RXINB [0:1], EXTTX. 0 : active H 1: active L
TX Port	TX Control	TXENA [0:1] TXENB [0:1] EXTTX	OUTPUT	TX data pulse (Mx=0) or TX enable signal (Mx=1). Setup TX mode by MA, MB, ME. Setup the polarity by LA, LB, LE
TX Port	TX Data Output	nPULSE [1:2]	OUTPUT	TX pulse data into HYC9068S-SK/9088S-SK when ARCNET chip is at normal mode. The pulse is always active Low.
TX Port		nP1BAK	OUTPUT	TX pulse data into RS485 driver or HYC2485S/2488S when ARCNET chip is at backplane

	FEATURE	NAME	INPUT/OUTPUT	DESCRIPTION
				mode. The pulse is always active Low.
TX Port	Polarity Setup	LA, LB, LE	INPUT	Setup the polarity of TXENA [0:1], TXENB [0:1], EXTTX. 0 : active L 1: active H
TX Port	Mode Setup	MA, MB, ME	INPUT	Setup the mode of TXENA [0:1], TXENB [0:1], EXTTX. 0: Output TX pulse. (It is equivalent to nTXEN "OR" nP1BAK) 1: Output TX enable

Operating Mode Setup

FEATURE	NAME	INPUT/ OUTPUT	DESCRIPTION
Data rate setup	CKM [0:2]	INPUT	Terminal to setup the data rate of TMC2005. CKM2 CKM1 CKM0 DIVISOR MULTIPLIER SPEED 0 0 0 16 x1 156.25 Kbps 0 0 1 8 x1 312.5 Kbps 0 1 0 4 x1 625 Kbps 0 1 1 2 x1 1.25 Mbps 1 0 0 1 x1 2.5 Mbps 1 0 1 1 x2 5 Mbps 1 1 0 Reserved Reserved Reserved 1 1 1 1 x4 10 Mbps External clock is 20MHz. Refer to "VARIOUS SETUP"
Noise cut mode	nMBA nMBB nMBE	INPUT	0: Cut off noise from received data 1: Don't cut off noise Setup "0" normally.
Big jitter mode	nBJA nBJB nBJE	INPUT	Setup a jitter filter feature. Select a pulse as reference phase used by DPLL. 0: 2nd pulse (big jitter mode) 1: 1st pulse (normal mode)
Open drain mode	nEXTOD	INPUT	Setup a the use of EXTTX port. 0: Set EXTTX as open drain output and use as Ext. 1: Set EXTTX as normal output and use as 5th port.

PLL

FEATURE	NAME	INPUT/ OUTPUT	DESCRIPTION
	LP	OUTPUT	Using PLL: Connect to an external condenser "C1" for loop filter. Using no PLL: must be open.
	RO	OUTPUT	VCO output Using PLL: Connect to an external resistor "R0" for loop filter. Using no PLL: must be open.
	AGS	INPUT	Analog sense input. Using PLL: Connect to loop filter. Using no PLL: Connect to ground.

FEATURE	NAME	INPUT/ OUTPUT	DESCRIPTION
	nPLLTST	INPUT	Test pin for PLL. **Must always connect to VDD.**
	AVDD		Analog power supply Using PLL: Analog power supply. There are some limits on PCB pattern. Using no PLL: Power supply (+5V) same as VDD1~6.
	AVSS		Analog ground Using PLL: Analog ground. There are some limits on PCB pattern. Using no PLL: Use a ground same as VSS1~8.

Other Signals

FEATURES	NAME	INPUT/ OUTPUT	DESCRIPTION
CRYSTAL INTERFACE	XTLI	INPUT	Connect a 20MHz crystal. When supplying an external clock, input the clock to this pin.
CRYSTAL INTERFACE	XTLO	OUTPUT	Connect a 20MHz crystal. When supplying an external clock, it must be open.
SYSTEM RESET INTERFACE	nRST	INPUT	Reset for initializing TMC2005. (active Low)
TEST PIN	CKO	OUTPUT	Output internal clock of TMC2005.
TEST PIN	nCKOEN	INPUT	Output control of CKO. 0: Output internal clock on CKO. 1: Always output Low level on CKO. Set “1” Normally.
TEST PIN	RXFLT	INPUT	It must be open
TEST PIN	NC [1:2]		It must be open
POWER SUPPLY	VDD [1:6]		Power supply (+5V)
GROUND	VSS [1:8]		Ground

OPERATIONAL DESCRIPTION

Direction Determination

All TX ports are set to disable mode in the initial state. When a signal is received from any RX ports, the circuit holds the port on receiving mode (disable TX) and changes the other ports to sending mode (disable RX). One port stays in RX and the rest change into TX after all. The circuit initializes the internal DPLL on the timing of received RX pulse, and the RX buffer circuit stores the RX data and filters its jitter. TX controlling circuit regenerates the stored RX pulse on nPULSE1, nPULSE2 and nP1BAK. The nPULSE1 and nPULSE2 are pulse output pins for transceivers (HYC9088A) of ARCNET normal mode. The nP1BAK is a pulse output pin for transceiver (HYC5000/4000/2000 and RS485 driver) of ARCNET back plane mode. When using optical transceiver, instead of these signals, TXENA [0:1], TXENB [0:1], EXTTX (MA, MB, ME = 0) must be used as TX data inputs of the optical transceiver.

Direction Release

On ARCNET protocol, each TX message starts with 6-bits of “1” ALERT and each data byte is lead by three bits (1, 1, 0) preamble. To control the HUBs direction, the circuit monitors this bit pattern and holds the state. If the end of the bit pattern comes, all TX ports return receiving mode (disable TX) again. The interval timer detects the end of the bit pattern. During data is on line, silent period is less than 4 uS* because at least one bit “1” among 10-bits is received while receiving the data. The minimum silent interval from the end of received data to the alert of the next data (the minimum time of changing the direction) is the chip turn around time (12.6 uS*) of ARCNET controller. The interval timer to detect the data end is set to 5.6uS by adding some margin to the above interval for neglecting the reflection on a cable.
[Note] Numbers marked * are at 2.5Mbps operation.

Jitter Filter

To build a network with transceivers that introduce big jitter like ones for optical fiber, the old HUB that has direction control only may cause a transmission error because jitters on each HUB are added when several HUBs were connected in serial. The TMC2005 fixes that problem with jitter filtering and wave shaping through the following three steps.

1) Input Sampling

The TMC2005 samples a data on a network by eight times clock of the network data.

2) Jitter Filtering (DPLL)

The TMC2005 filters the jitter (± 100nS at 2.5Mbps) of network data sampled by 8X clock through the internal digital PLL and stores the data into the buffer.

3) Wave Shaping Output

The TMC2005 re-synchronizes and regenerates the network data at the same clock as the data rate.

The capability of the jitter filtering is shown below.

DATA RATE	CAPABILITY OF JITTER FILTERING
10Mbps	± 25nS
5Mbps	± 50nS
2.5Mbps	± 100nS
1.25Mbps	± 200nS
625Kbps	± 400nS
312.5Kbps	± 800nS
156.25Kbps	± 1.6uS

Option Feature for Jitter Filtering

When any RX ports receive the bigger jitter than its allowance, the TMC2005 may fail to receive the data correctly and the network may be down.. However the below method to escape is effective for the case that a momentary big jitter occurs under a special condition like an optical transceiver.

1) Big jitter (BJ) mode

The reference phase of the internal DPLL is changed from the first pulse to the second pulse by setting "0" to the big jitter mode pins (nBJX). This setup is effective for the case that a big jitter occurs when rising up from DC state as same as when using an optical transceiver with ATC function (refer to complement).

Note: The delay time of the TMC2005 becomes 400nS (at 2.5Mbps) longer than the normal mode. The delay time limits the maximum cable length and maximum node number.

[Complement] The big jitter may occur in the case of using an optical transceiver, especially an optical receiver that has an ATC circuit that controls threshold level in proportion to received light strength. The first pulse especially after long time idle has the big jitter but the second pulse is stabilized.

2) Changing polar of RX port

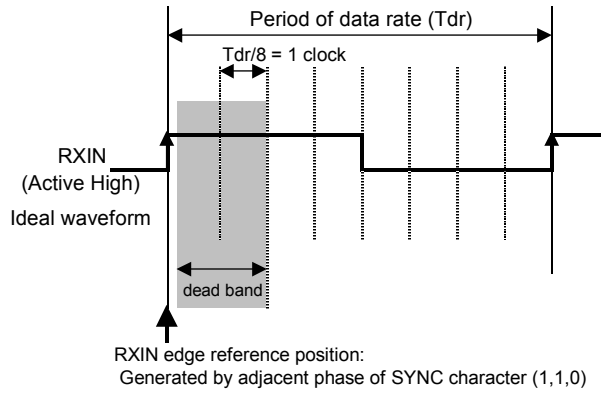
In order to filter the jitter of edge in one side, it is effective to set reverse to pin SA, SB, SE to change the polarity of RX port.

Note: Changing the polarity of RX port makes the delay time of the TMC2005 circuit a half bit (200nS) longer than original 2.5Mbps, and the delay time affects the maximum cable length and maximum node number.

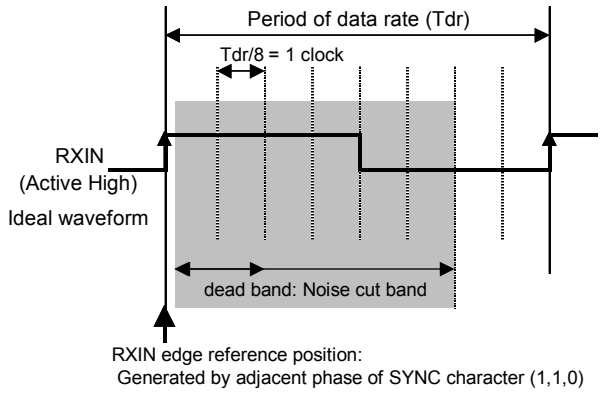
Option Feature for Noise Cut mode

The Noise cut mode is enabled by setting pin nMBx sets 0. The noise cut mode is a function to remove the ringing noise and the reflection noise generated on the leading edge side of the input pulse to receive data input RXINx. The position and the width of the "dead band" are shown in the figure below.

- Dead band at Normal mode (nMBx=1)



- Dead band at Noise cut mode (nMBx=0)



APPLICATION NOTES

Example 1: A five ports HUB with HYC4000s in backplane mode.

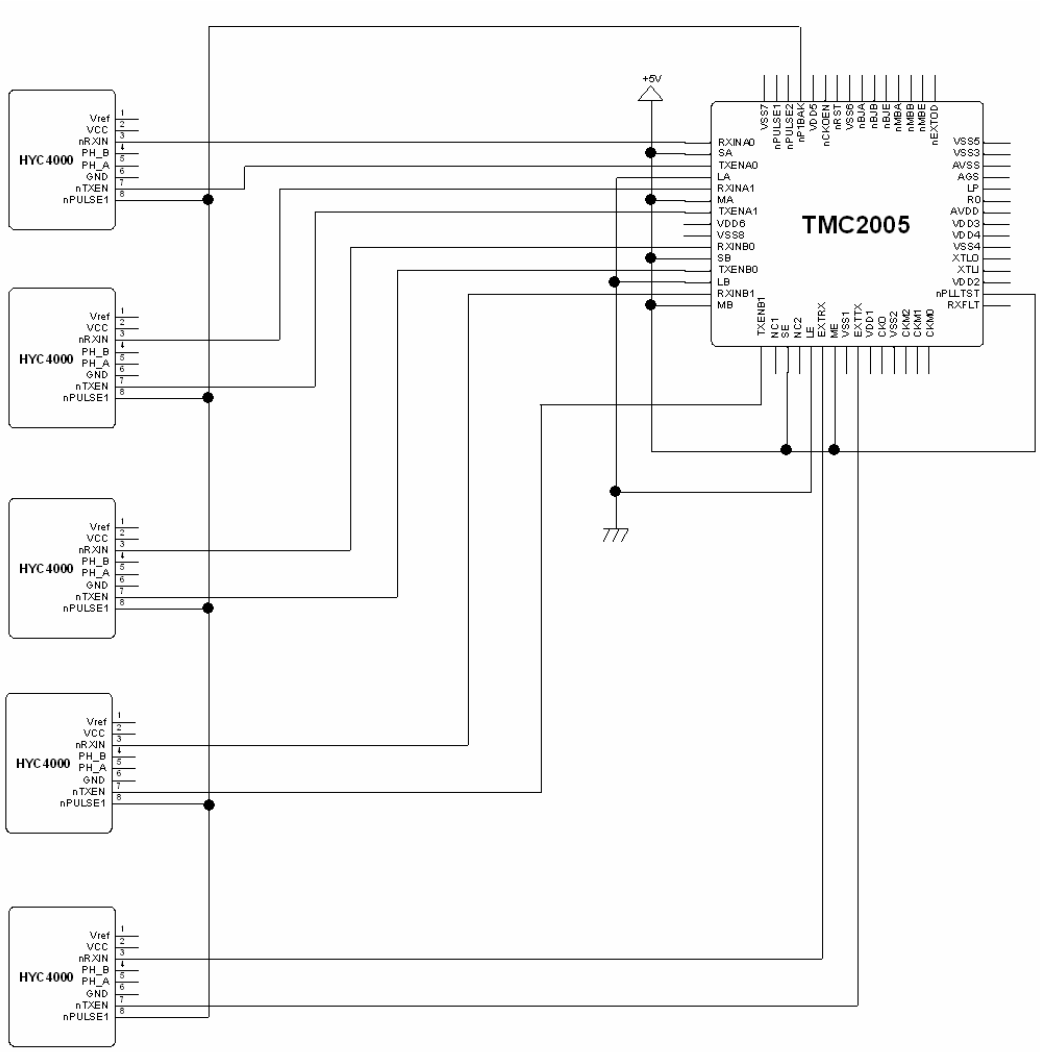


FIGURE 1 - APPLICATION EXAMPLE

Only the TMC2005 and five transceivers are indicated in the above figure. Connect the other pins adequately.

Example 2: A five ports HUB with HYC9088s and a optical transceiver(TODX270A) links the two physical layers; dipulse and fiber optics.

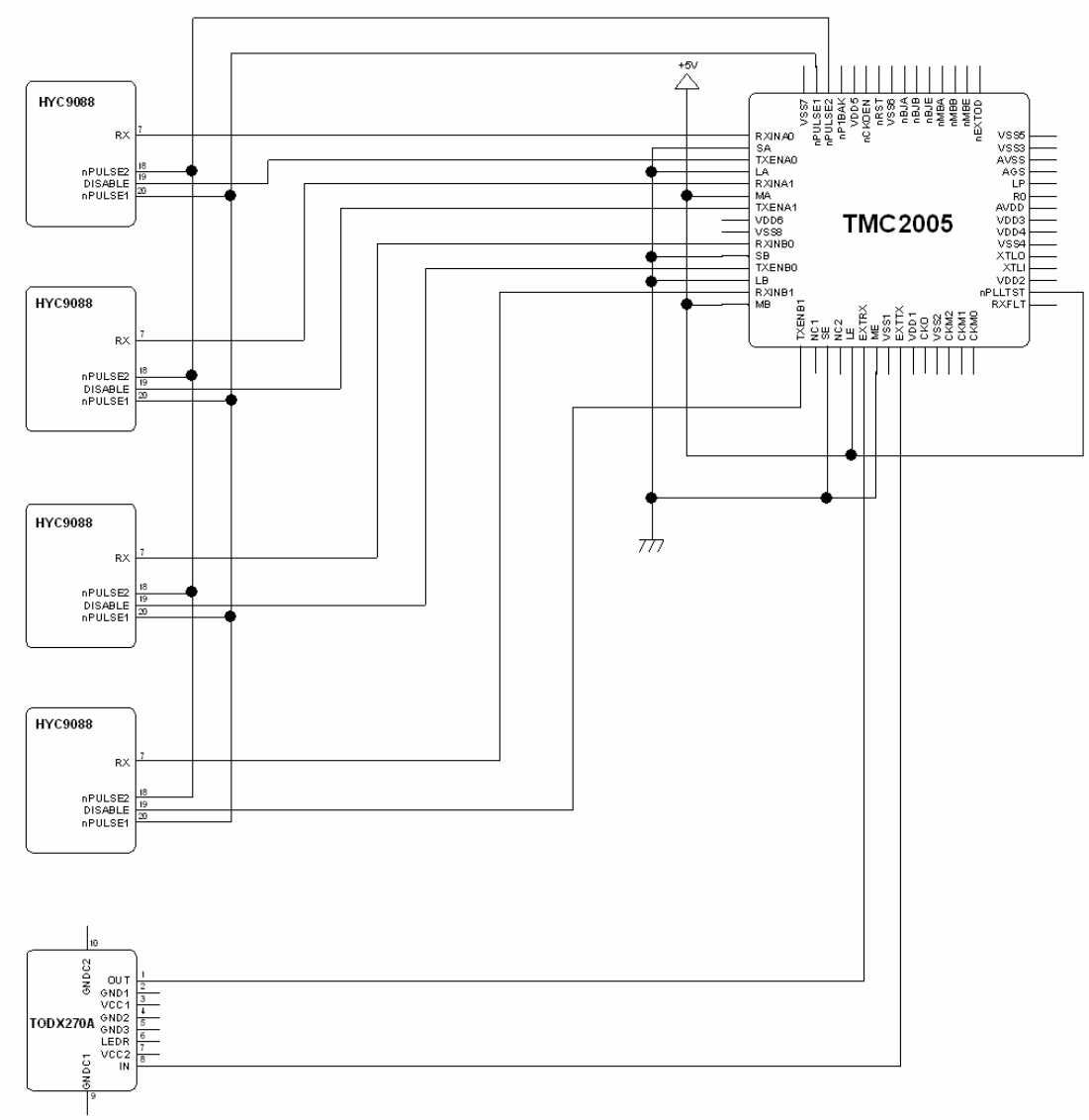


FIGURE 2 - APPLICATION EXAMPLE 2

Only the TMC2005 and five transceivers are indicated in the above figure. Connect the other pins adequately.

Example 3: A five ports HUB with two optical transceivers, two HYC9088s, and a HYC4000 links three physical layers; fiber optics, dipulse, and AC-485.

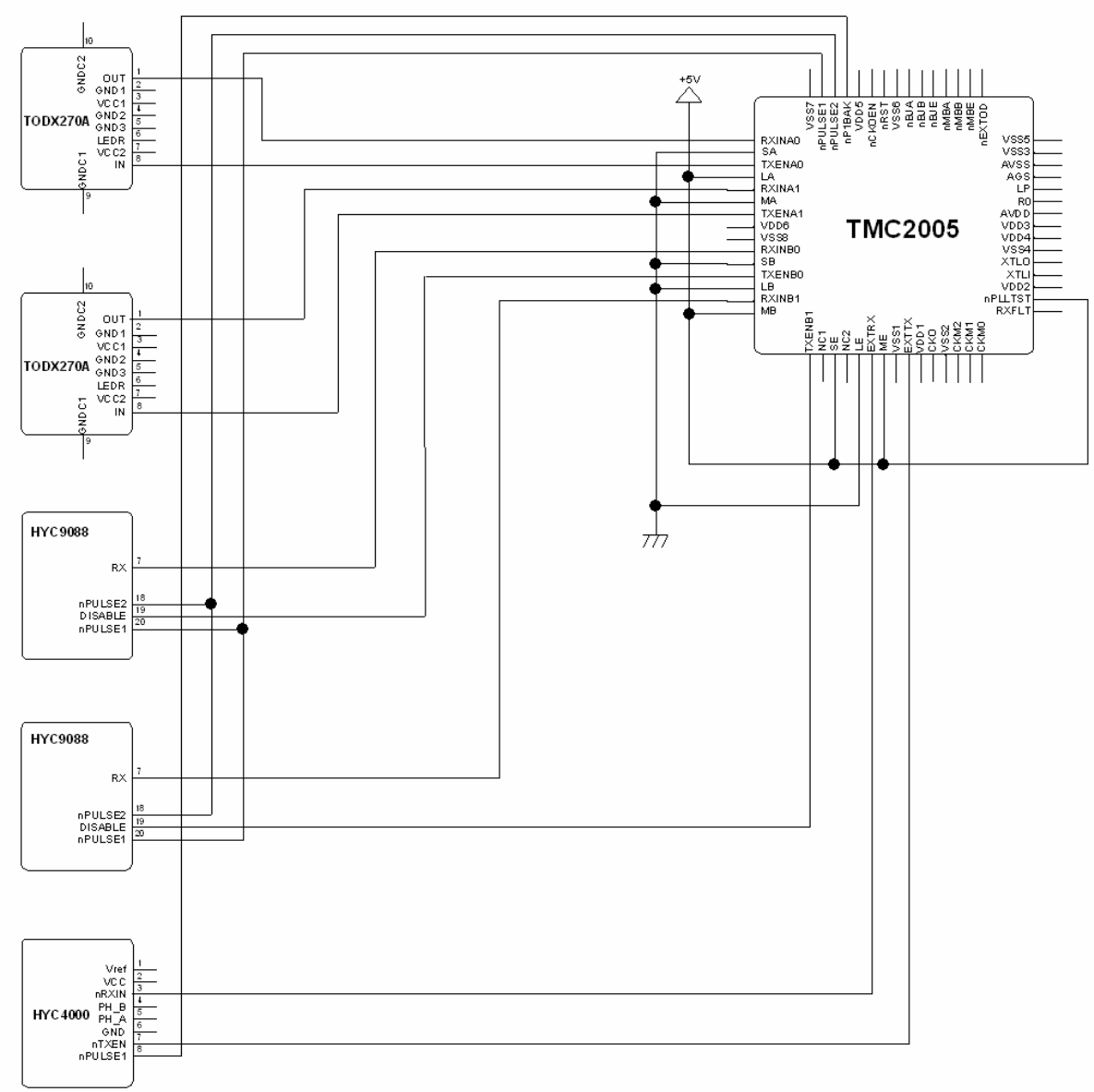


FIGURE 3 - APPLICATION EXAMPLE 3

Only the TMC2005 and five transceivers are indicated in the figure above. Connect the other pins properly.

Example 4: An on-board type HUB with a COM20020 and four optical transceivers in backplane mode.

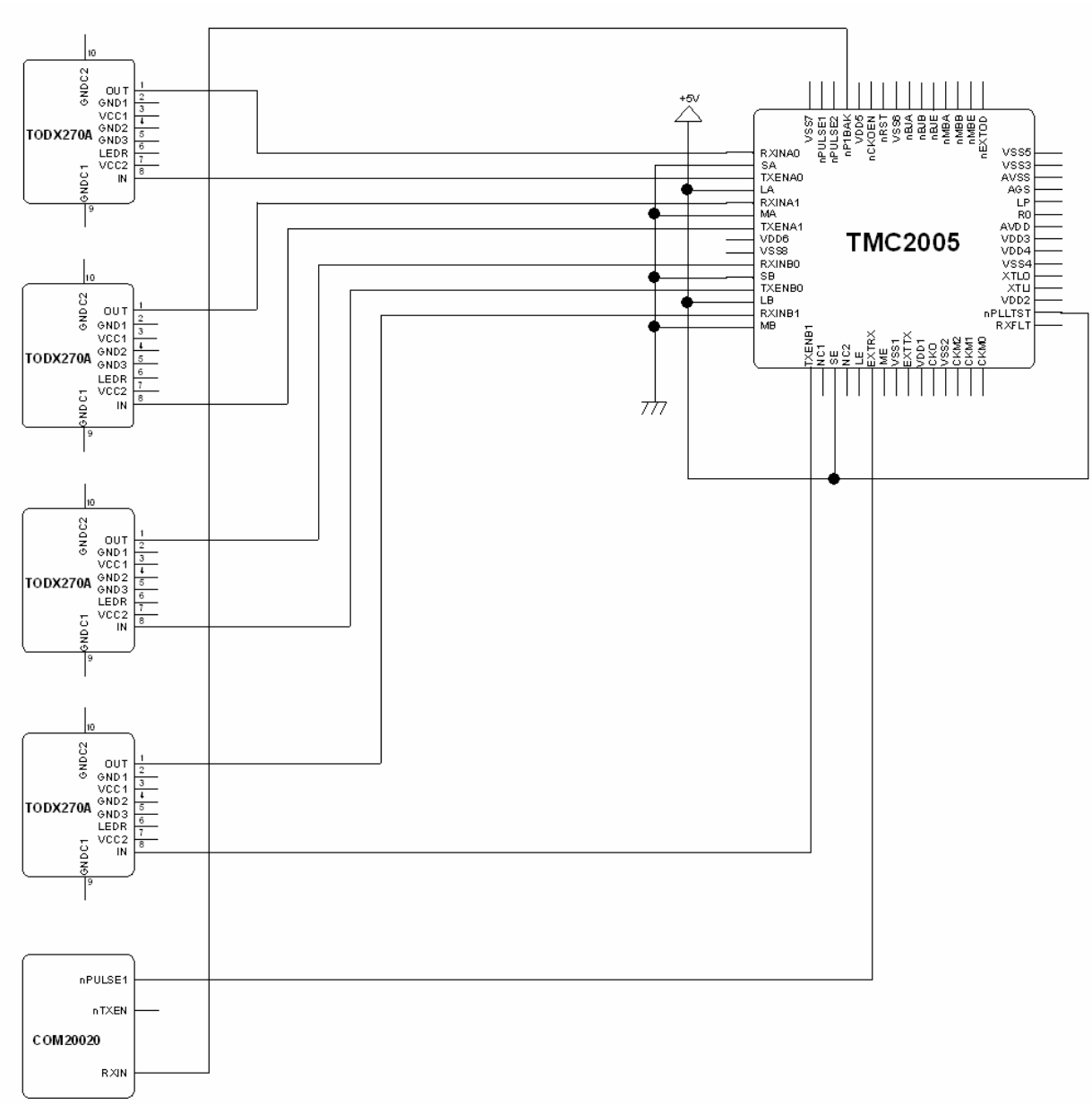


FIGURE 4 - APPLICATION EXAMPLE 4

Only the TMC2005 and four transceivers with the COM20020 are indicated in the above figure. Connect the other pins adequately.

Example 5: An on-board type HUB with a COM20020 and four RS485 transceivers.

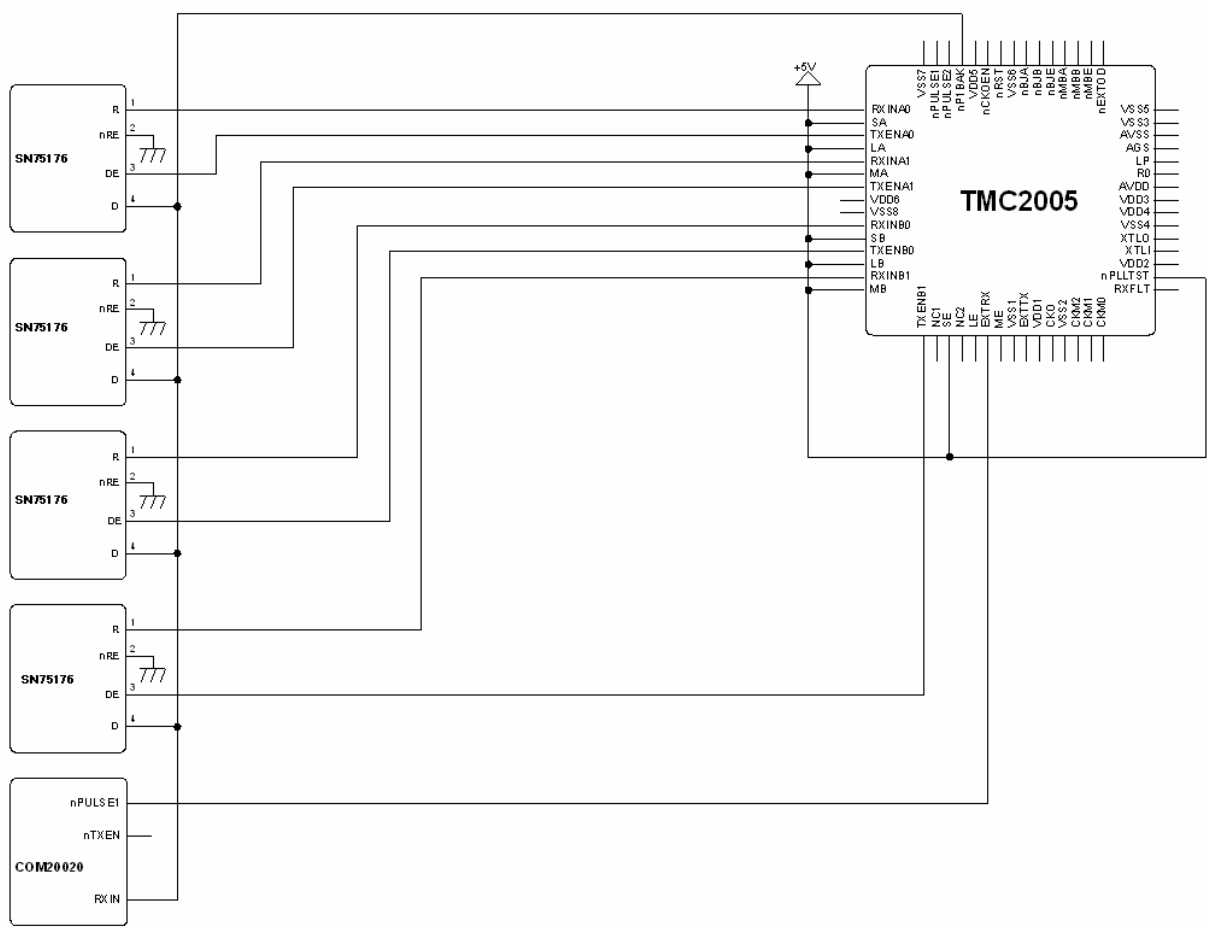


FIGURE 5 - APPLICATION EXAMPLE 5

Only the TMC2005 and four transceivers with the COM20020 are indicated in the above figure. Connect the other pins adequately.

Example 6: An on-board type HUB with a COM20020, two HYC4000s, and two HYC9088s links two different physical layers; dipulse and AC-485.

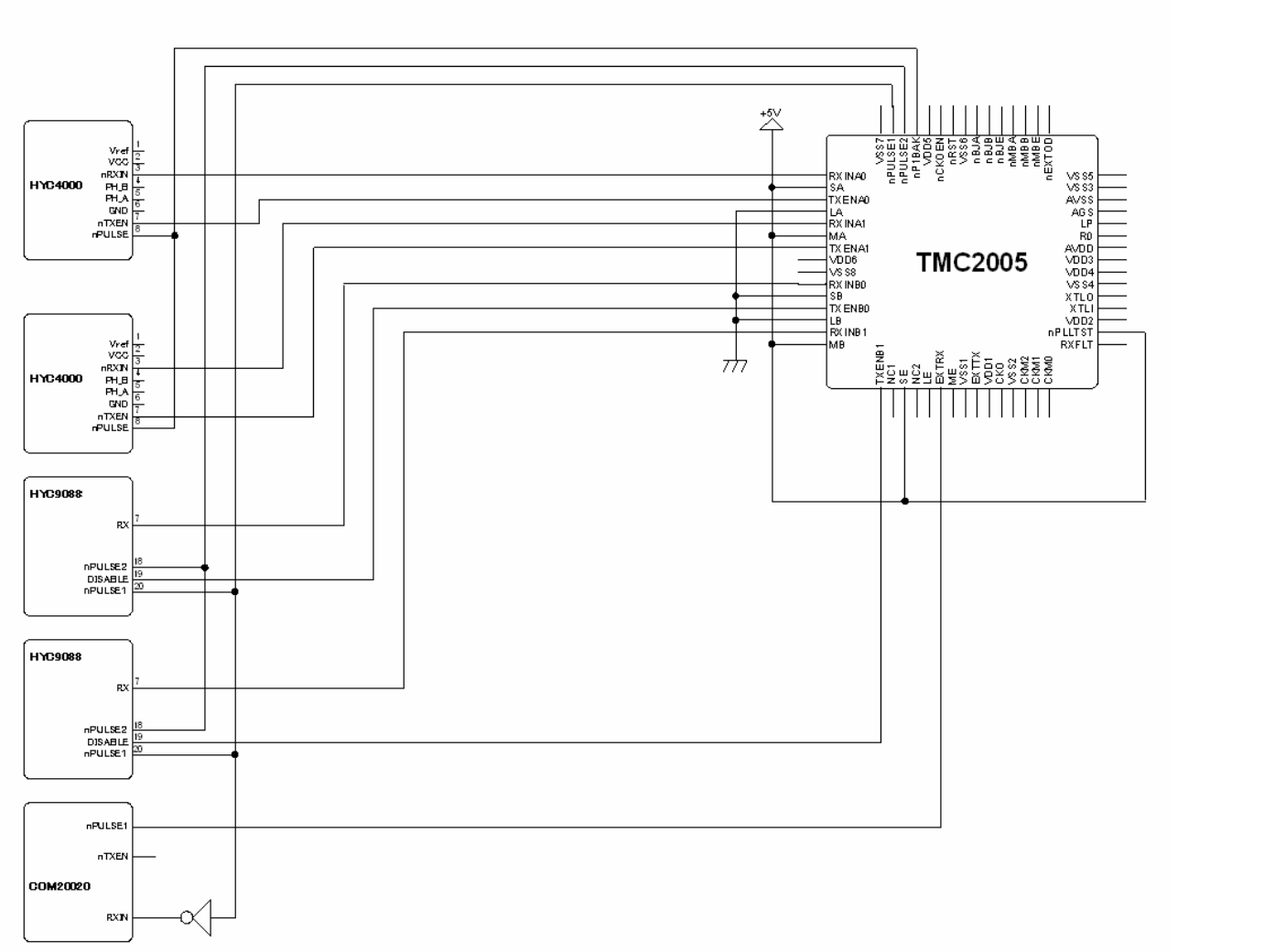


FIGURE 6 - APPLICATION EXAMPLE 6

Only the TMC2005 and four transceivers with the COM20020 are indicated in the above figure. Connect the other pins adequately.

Example 7: An eight ports HUB are composed by using two TMC2005. Two TMC2005 connects the EXTTX signal with the EXTRX signal.

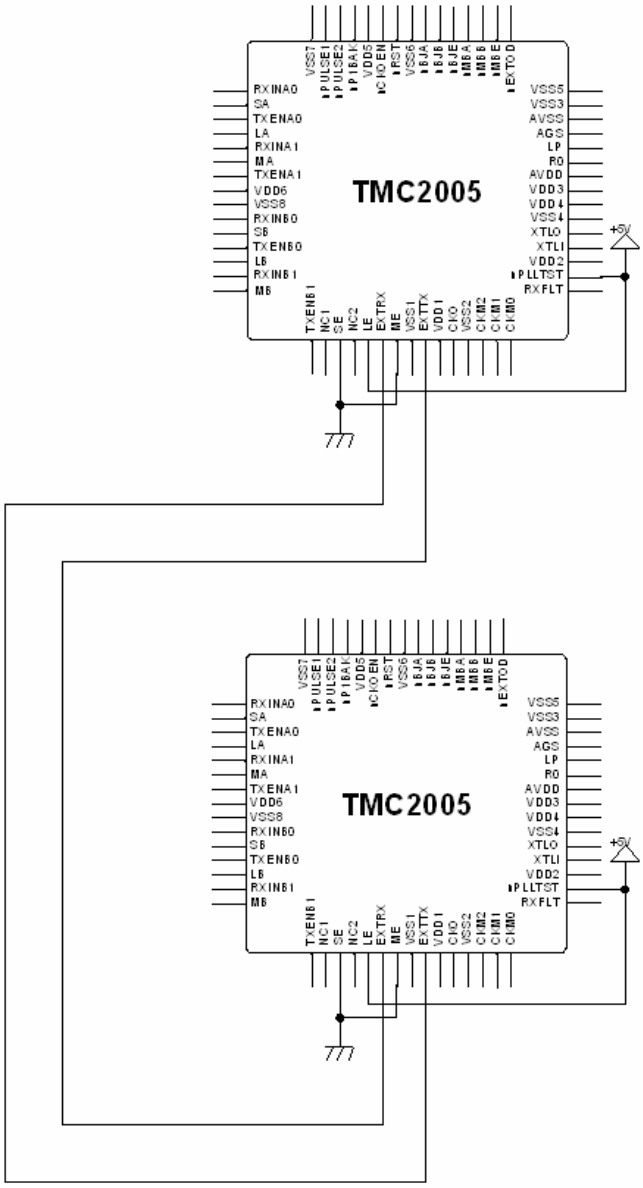


FIGURE 7 - APPLICATION EXAMPLE 7

Only the two TMC2005s are indicated in the above figure. Connect the other pins adequately.

Example 8: A sixteen ports HUB are composed by using four TMC2005. The EXT port between TMC2005 is made an open-drain mode and it connects it (left example). Or put standard logic IC such as 74LS20 outside (right example). This connected method is excellent in noised respect compared with connected method of open-drain mode.

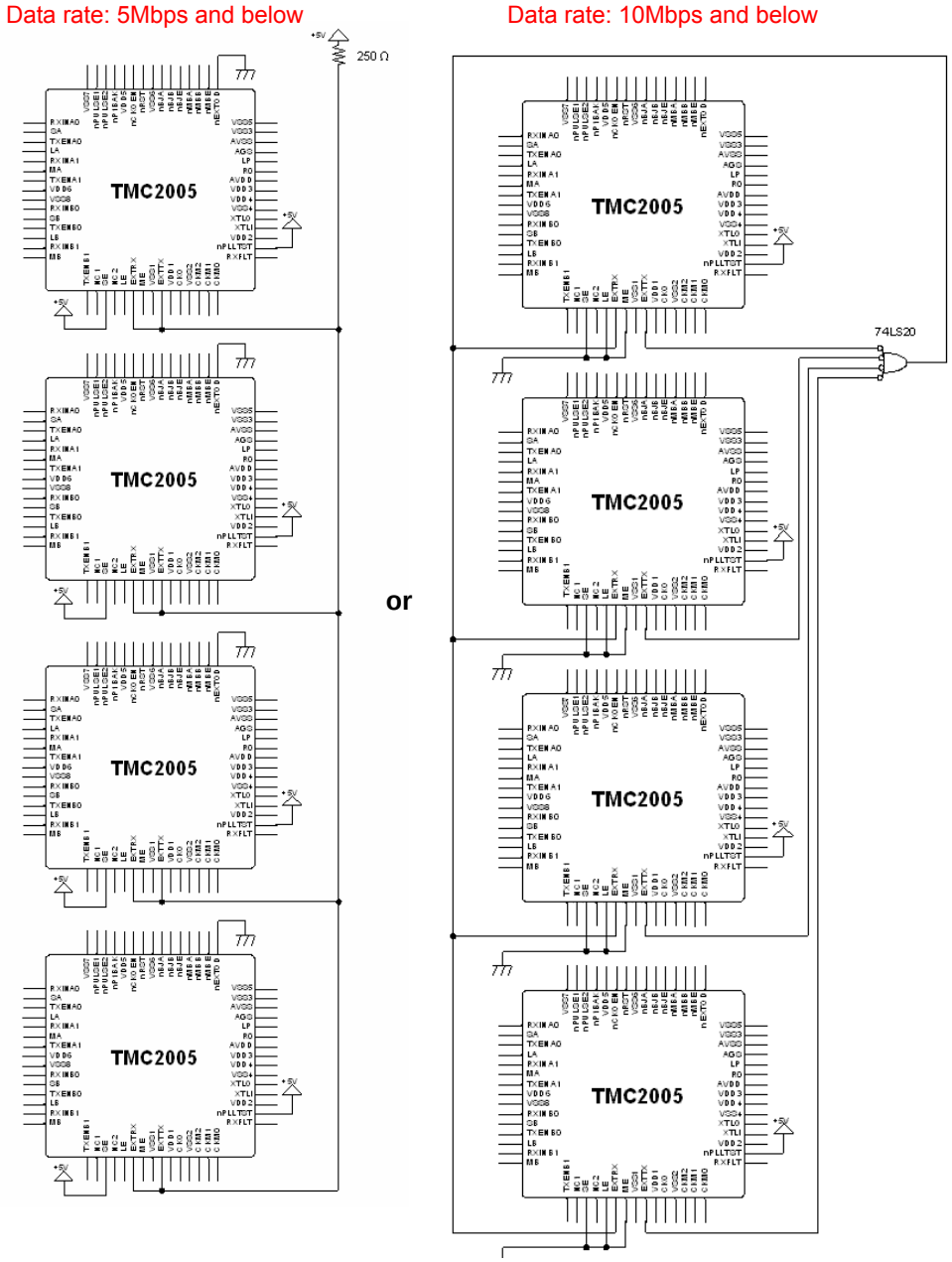


FIGURE 8 - APPLICATION EXAMPLE 8

Only the four TMC2005s are indicated in the above figure. Connect the other pins adequately.

Note: Use the wiring pattern length that connects between four TMC2005s by five inches or less in open-drain mode. Four TMC2005s is maximum in open-drain mode.

PORT GROUP

The five ports can be divided into three groups (group A: two ports, group B: two ports, extension port: one port) and each group can select TX/RX polar, noise cut mode, and big jitter mode respectively. Select pins for each group are as follows:

FUNCTION	GROUP A	GROUP B	EXTENSION
RECEIVE	RXINA0, 1	RXINB0, 1	EXTRX
TRANSMIT	TXENA0, 1	TXENB0, 1	EXTTX
RX POLARITY	SA	SB	SE
TX POLARITY	LA	LB	LE
TX CONTROL	MA	MB	ME
NOISE CUT	nMBA	nMBB	nMBE
BIG JITTER	nBJA	nBJB	nBJE
EXTENSION			nEXTOD

Various Setup

Example For Operation Mode Setup To Each Port

SA, SB, SE	LA, LB, LE	MA, MB, ME	RX POLAR	TX POLAR	TRANSCEIVER
1	0	1	Active Low	Active Low	HYC2485S/HYC2488S
0	1	0	Active High	Active High	Optical Transceiver
0	0	1	Active High	Active Low	HYC9088/HYC9068
1	1	1	Active Low	Active High	RS485 Transceiver

Note for Unused port

Unused ports can be left open because RX port (RX input), RX polar (S input), TX polar (L input), TX control (M input) pins have internal pull-up resistors. Because of internal pull-up resistors, select pins for noise cut (nMB input), big jitter (nBJ input) can be left open when used for setting “OFF”.

Example for Power-On Reset Circuit

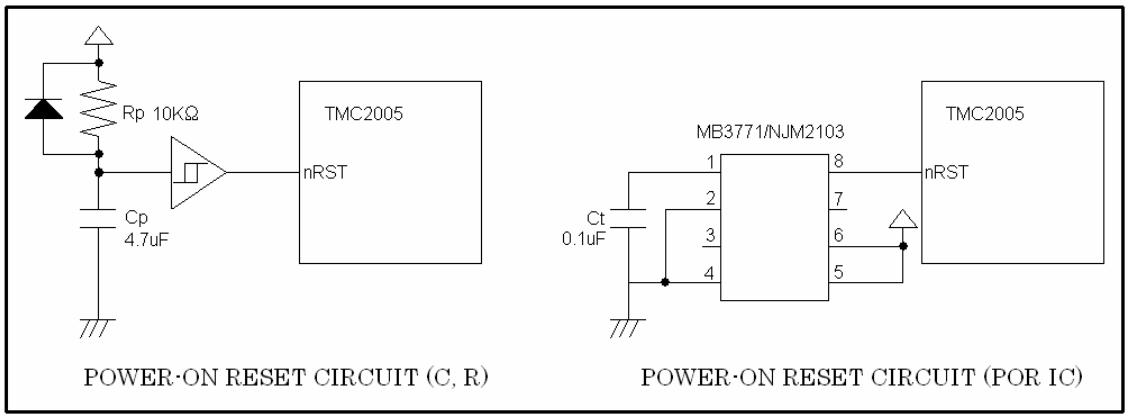


FIGURE 9 - POWER-ON RESET

CONNECTING THE TMC2005 WITH INTERNAL PLL

When using the TMC2005 at data rate 2.5Mbps or lower, it is not necessary to use internal PLL. Leave the loop filter pins (RO, LP) open and connect AGS to the Ground. The pins for the analog power supply (AVSS, AVDD) may connect to digital power supply. When using the TMC2005 at data rate 5Mbps or higher, the internal PLL has to be used as a clock multiplier. PCB layout must follow the guidelines at Figure 10, refer to Notes 1 through 5.

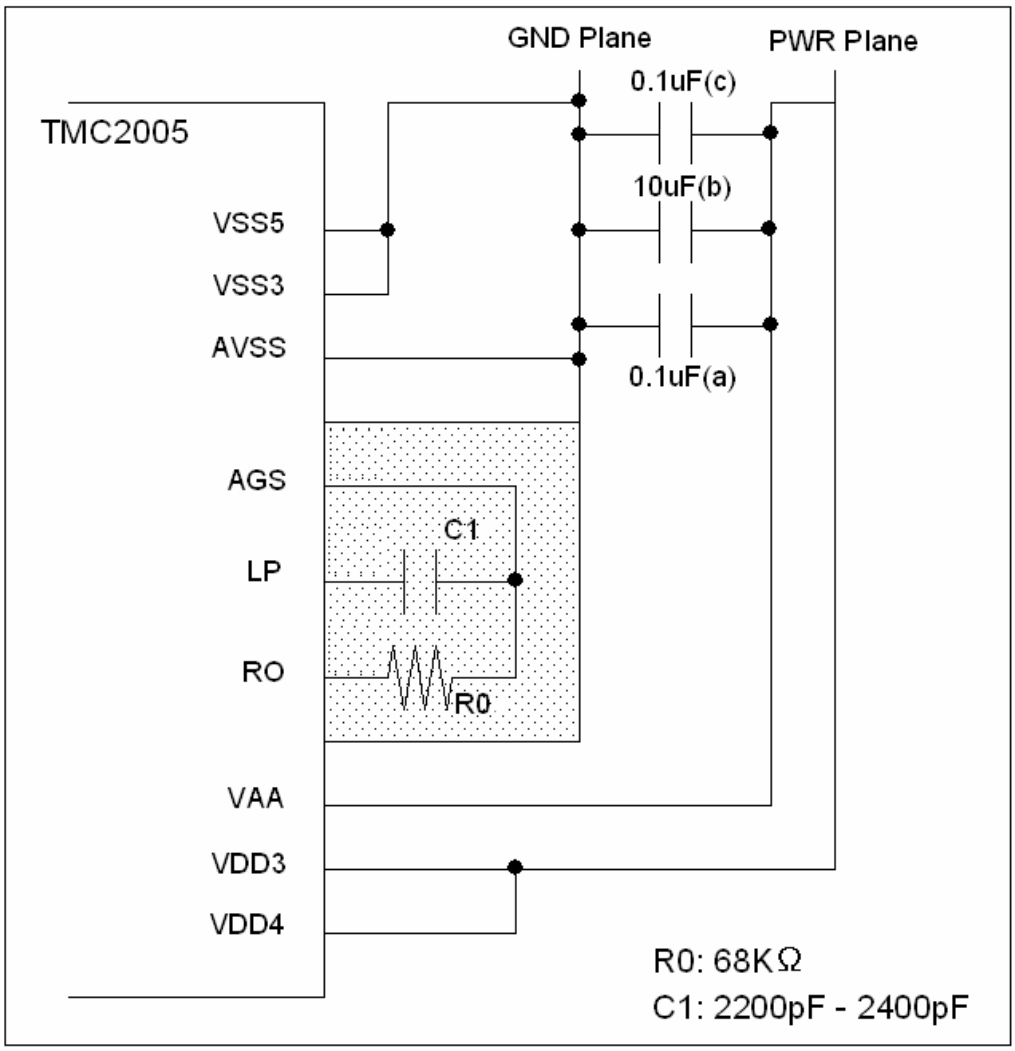


FIGURE 10 - PLL PATTERN LAYOUT

Note 1: Prohibit the patterns for LP and RO from occupying the area of digital power supply. Use the area of analog power supply between VAA and AVSS.
Note 2: Encircle the pattern between LP, RO and AGS with wide pattern of analog ground.
Note 3: Connect the analog power supply "VAA" with 0.1 uF condenser (a) with in 1/8 inch (~ 3.2mm) from VAA pin.
Note 4: In order to filter the jitter of low frequency, connect a 10 uF condenser (b) in parallel with the condenser (a).
Note 5: Place 0.1 uF bypass condenser (c) within ¼ inch (~ 6.4mm) from VDD3 and VSS3. Connect the ground side of a condenser (c) at the place (*) where AVSS returns to GND plane.

Method To Connect A Crystal Clock
Connect with external parts as follows:

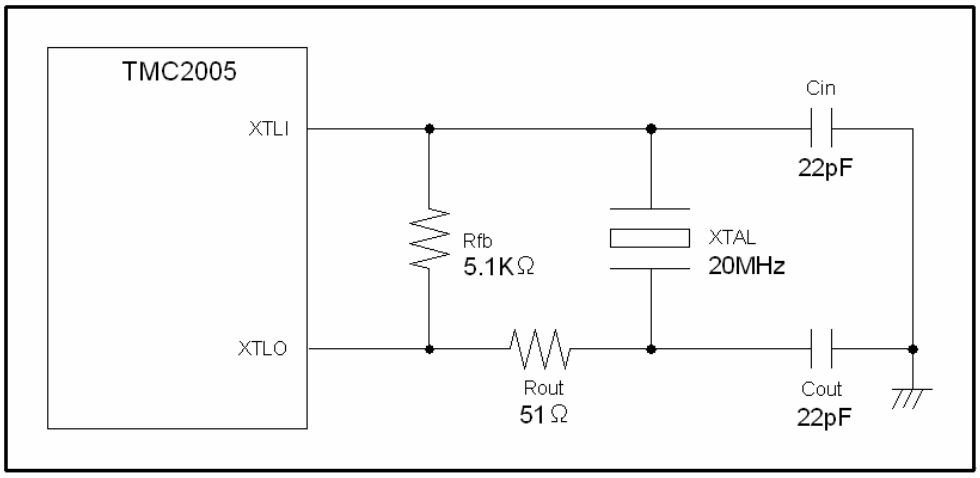


FIGURE 11 - CONNECTING THE CRYSTAL CLOCK

Note 1: When designing a printed circuit board, keep the patterns as short as possible and don't cross with other patterns.
Note 2: When using an external clock like an oscillator module, connect it to XTLI pin and leave XTLO pin open. When designing a printed circuit board, wire between XTLI pin and oscillator should be short as possible.

nPLLTST pin
nPLLTST must be connect toVDD. The rest of input pins have pull-up resistors built in, but nPLLTST pin does not have the pull-up resistor. Clock signal cannot ditributed into the TMC2005 if nPLLTST pin is connected GND or is left open.

CASCADING CONNECTION

HUBs can be connected in cascade by using the ports as Fig. 12. In the case of cascade connection, it is necessary to consider how many HUBs can exist in serial. The maximum delay between input port and output port is 650ns @2.5Mbps at the TMC2005. It is equivalent to the propagation delay when a cable length is 135m. For example, if every cable length is 10m in Figure 12, the longest distance is physically 50m but it is electrically 590m because of multiplying 10m by 5 and 135m by 4, and the total propagation delay becomes 2.8uS. For analyzing the network timing, consider the delay caused by HUBs. In the ARCNET protocol, it is defined that the longest distance between nodes is the maximum 6.4Km. For example, if 20 TMC2005s exist between nodes in the longest distance, the actual cable length is 3.7Km because of deducting 135m by 20 in converting to cable length from 6.4Km.

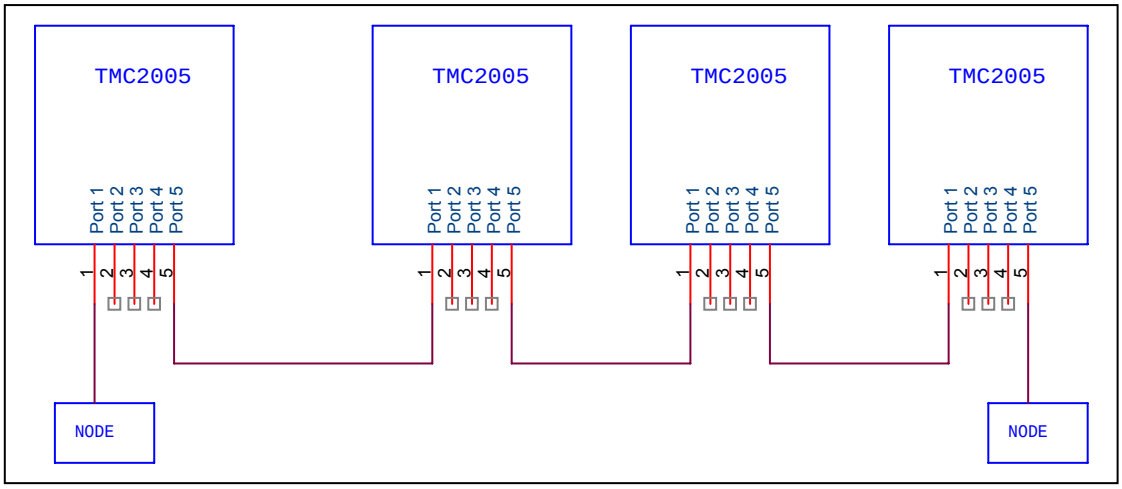


FIGURE 12 - CASCADE CONNECTION OF 4 HUBS

Two examples of eight ports HUBs using two TMC2005s are shown in Fig. 13 and 14. If connecting as in Fig. 13, eight TMC2005s exist between the nodes at both far ends. On the other hand, when assigning two ports for cascading connection to the same TMC2005, the number of TMC2005 in serial connection can be down to the number of HUBs plus two, which can reduce the propagation delay.

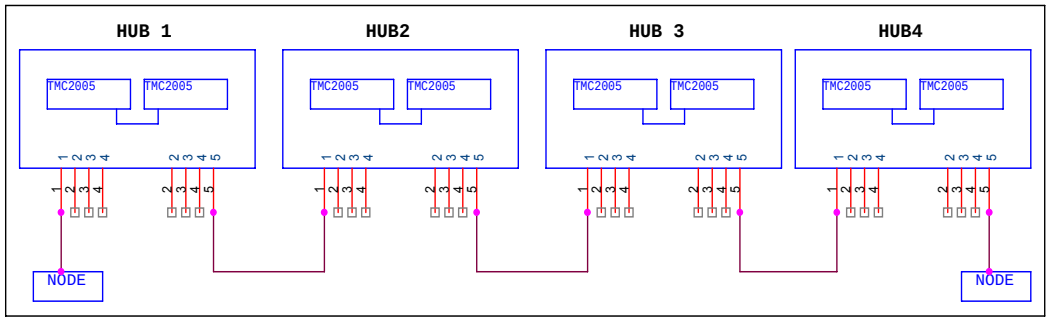


FIGURE 13 - CASCADE CONNECTION OF 8 PORT HUB

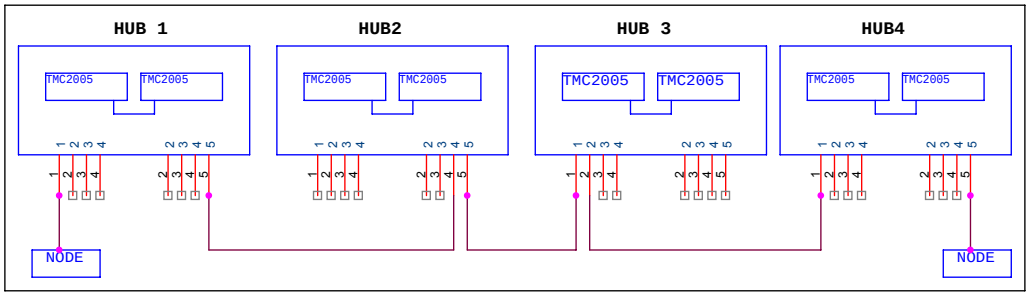


FIGURE 14 - CASCADE CONNECTION OF 8 PORT HUB

Fig.15 shows a 16 ports HUB with four TMC2005s connected by open–drain ports. When assigning two ports for cascade connection to the same TMC2005, the number of TMC2005s for serial connection can be reduced to the number of HUBs plus two.

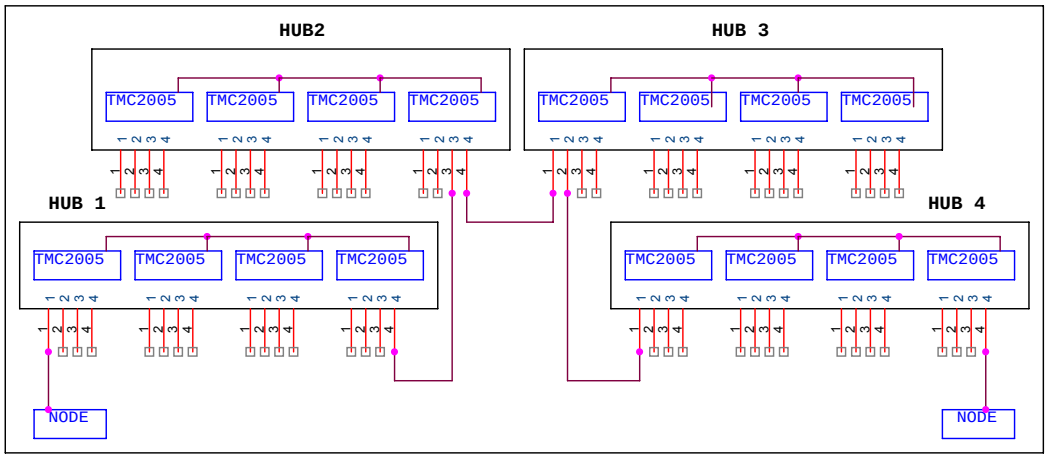


FIGURE 15 - CASCADE CONNECTION OF 16 PORT HUB

Note: When connecting TMC2005 by open-drain output on a board, connecting TMC2005s must be four or less, and the data rate must be 5Mbps or slower. The pattern of open-drain output has to be as short as possible (less than 15cm).

Ring Network With the TMC2005

The reliability of the network can be improved by connecting every node in a ring, because the communication is maintained through the reverse route even if the cable is cut at a point. However ARCNET controller alone can not support ring, because ARCNET is a half-duplex communication system. Using HUBs makes possible for ARCNET to built a ring network as in Fig.16. This configuration is available only for using fiber optics. (Refer to the application note for details.)

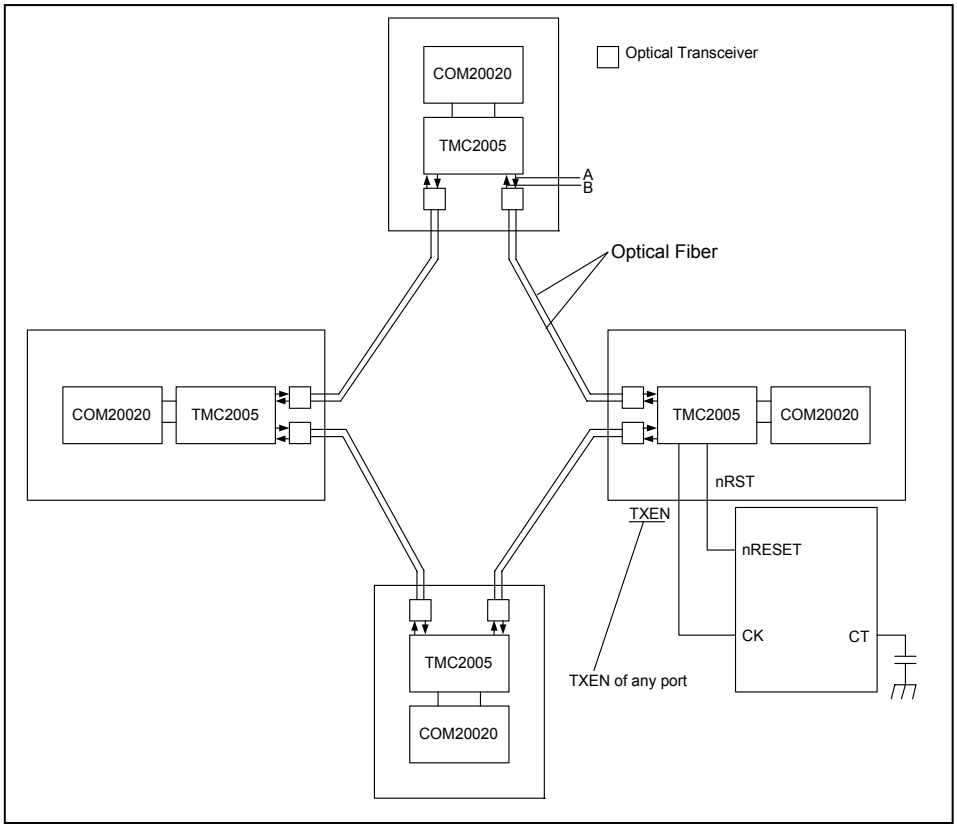


FIGURE 16 - RING CONFIGURATION

Note 1: Noise may cause an endless loop in a ring system, and the network may hang up. Therefore take care of designing the patterns between TMC2005 and transceiver or cabling of system.

Example for system hang-up

- A noise occurs only at “A” point in Figure 16.
- The noise propagates clockwise on the network.
- TMC2005 detects the noise that came back through the ring.
- The noise causes an endless loop in the ring.

Example for no hang-up

- Any noise occurs at “A” and “B” points in Figure 16 at the same time.
- The noise propagates to both directions in the network.
- An endless loop doesn’t occur because TMC2005s in the middle absorb the noise from both sides.

Note 2: Place a watch dog timer on one of the TMC2005 in at least one ring. To protect from hang-up the detecting time of the watch dog timer should be set to longer than 2.7 mS (@ 2.5Mbps) that is the burst time in the ARCNET protocol.

Note 3: Consider that a total of each segment delay time (cable delay, TMC2005 delay, driver delay and receiver delay) between HUBs in a network is less than 5.6uS (@ 2.5Mbps). The maxmimum distance between HUBs is approximiately 1000m (@ 2.5Mbps).

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

(Note) When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or “glitches” on their output when the AC power is switch on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

Vss = 0V

ITEM	SYMBOL	RATING	UNIT
POWER SUPPLY VOLTAGE	VDD	-0.3 +7.0	V
INPUT VOLTAGE	VIN	-0.3 VDD +0.3	V
OUTPUT VOLTAGE	VOUT	-0.3 VDD +0.3	V
AMBIENT TEMPERATURE	Tstg	-40 +125	°C

STANDARD OPERATING CONDITION
Vss = 0V

ITEM	SYMBOL	RATING	UNIT
POWER SUPPLY VOLTAGE	VDD	4.5 – 5.5	V
AMBIENT TEMPERATURE	Ta	0 - +85	°C

DC CHARACTERISTIC - INPUT PIN

SYMBOL	ITEM	CONDITION	MIN	MAX	UNIT
VIH	High Level Input Voltage	XTLI, nPLLTST	3.5		V
		Others	2.2		V
VIL	Low Level Input Voltage			0.8	V
IIH	High Level Input Current	VIN=VDD	-10	10	uA
IIL	Low Level Input Current	VIN=VSS	-10	10	uA
IIL	With pull-up	Vin=VSS	-200	-10	uA
IOZ	Output Leak Current	VOUT=VDD or VSS	-10	10	uA
IDD	Dissipation Current	Operating		100	mA

DC CHARACTERISTIC - OUTPUT PIN

SYMBOL	ITEM	CONDITION	MIN	MAX	UNIT	PIN
VOH	High Level Output Voltage	IOH=-4mA	2.4		V	1,9,46,51, 55,61
VOH	High Level Output Voltage	IOH=-8mA	2.4		V	11,45,47
VOL	Low Level Output Voltage	IOL=4mA		0.4	V	1,9,46,51, 55,61
VOL	Low Level Output Voltage	IOL=8mA		0.4	V	11,45,47

AC CHARACTERISTIC - CLOCK and RESET

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Generating Static Time	tx			4	mS	
Clock Cycle	tCYC		50		nS	Note 1
Clock Frequency Deflection	tCDF	-100		100	ppm	Note 1
Clock Pulse Width	tCW	20			nS	Note 1
Reset Pulse Width	ttRSW	200			nS	Note 1

Note 1: Use only F=20MHz
Note 2: VDD=4.5V

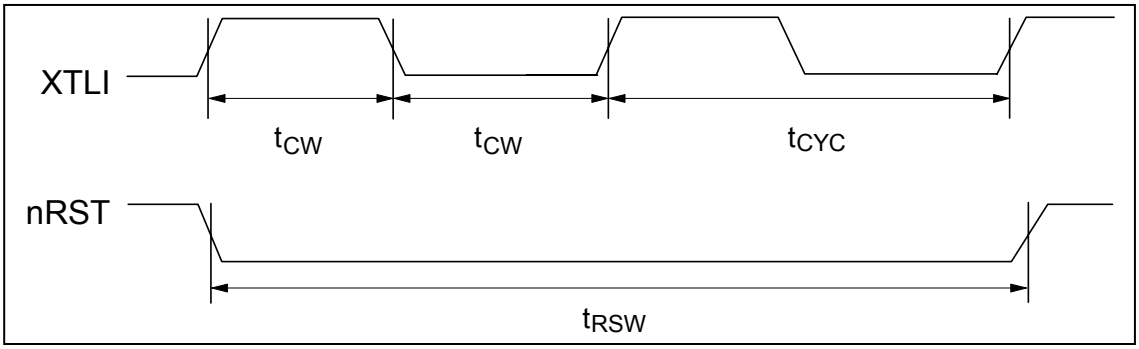


FIGURE 17 - CLOCK AND RESET

AC CHARACTERISTIC – Rx waveforms and Tx waveforms

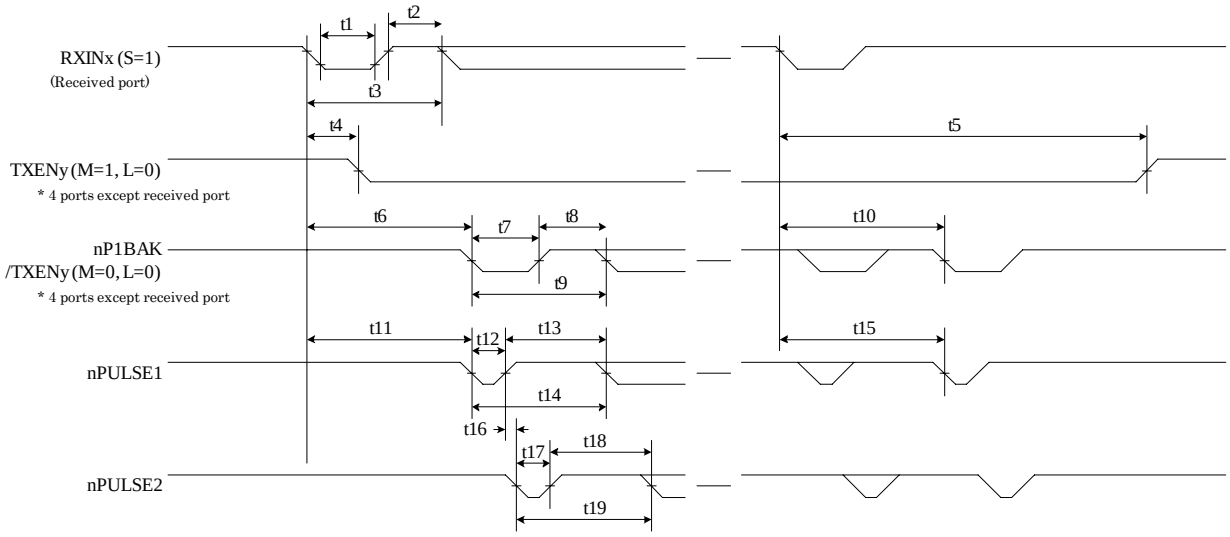


FIGURE 18 - RX WAVEFORMS AND TX WAVEFORMS

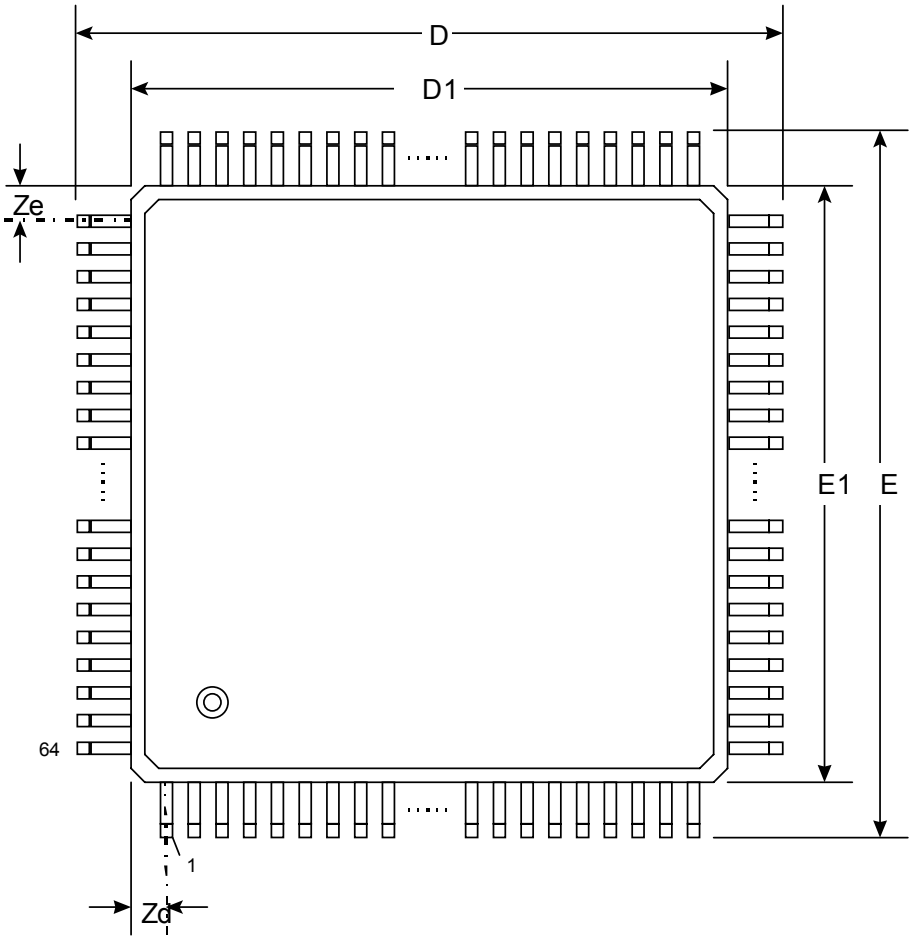
ITEMS	MARK	MIN	TYP	MAX	UNIT	REMARK
RXIN Low Pulse Width	t1	15			nS	
RXIN High Pulse Width	t2	15			nS	
RXIN Period	t3		Tdr (400)		nS	(Value at 2.5Mbps)
RXIN First Active Edge to TXEN Active	t4	2/8Tdr (100)		3/8Tdr+50 (200)	nS	Note1 (Value at 2.5Mbps)
RXIN Last Active Edge to TXEN Inactive	t5	111/8Tdr (5,550)		112/8Tdr+50 (5,650)	nS	Note1 (Value at 2.5Mbps)
RXIN First Active Edge to nP1BAK/TXEN First Active Edge	t6	9/8Tdr (450)		10/8Tdr+50 (550)	nS	Note2, Note3 (Value at 2.5Mbps)
nP1BAK/TXEN Low Pulse Width	t7		1/2Tdr (200)		nS	Note2 (Value at 2.5Mbps)
nP1BAK/TXEN High Pulse Width	t8		1/2Tdr (200)		nS	Note2 (Value at 2.5Mbps)
nP1BAK/TXEN Period	t9		Tdr (400)		nS	Note2 (Value at 2.5Mbps)
RXIN Active Edge to nP1BAK/TXEN Active Edge (Except First Edge of RXIN)	t10	5/8Tdr (250)	9/8Tdr+50 (500)	14/8Tdr+50 (750)	nS	Note2, Note3 (Value at 2.5Mbps)

ITEMS	MARK	MIN	TYP	MAX	UNIT	REMARK
RXIN First Active Edge to nPULSE1 First Active Edge	t11	9/8Tdr (450)		10/8Tdr+50 (550)	nS	Note3 (Value at 2.5Mbps)
nPULSE1 Low Pulse Width	t12		1/4Tdr (100)		nS	(Value at 2.5Mbps)
nPULSE1 High Pulse Width	t13		3/4Tdr (300)		nS	(Value at 2.5Mbps)
nPULSE1 Period	t14		Tdr (400)		nS	(Value at 2.5Mbps)
RXIN Active Edge to nPULSE1 Active Edge (Except First Edge of RXIN)	t15	5/8Tdr (250)	9/8Tdr+50 (500)	14/8Tdr+50 (750)	nS	Note3 (Value at 2.5Mbps)
nPULSE1 to nPULSE2 Overlap	t16	-10	0	+10	nS	
nPULSE2 Low Pulse Width	t17		1/4Tdr (100)		nS	(Value at 2.5Mbps)
nPULSE2 High Pulse Width	t18		3/4Tdr (300)		nS	(Value at 2.5Mbps)
nPULSE2 Period	t19		Tdr (400)		nS	(Value at 2.5Mbps)

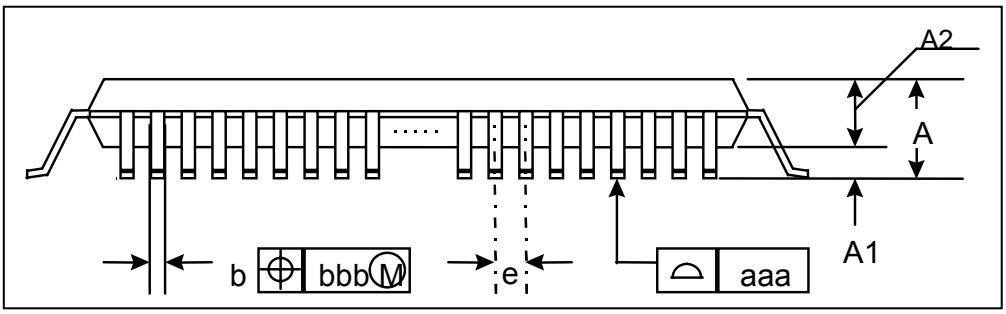
Tdr: Period of data rate, ex) Tdr=400nS at 2.5Mbps

Note1: Applied to TXENx which is set to Mx=1. (Tx Control mode)
Note2: Applied to TXENx which is set to Mx=0. (Pulse output mode)
Note3: Extra one “Tdr” time to be added at RXINx is set to nBJx=0. (Big Jitter mode)

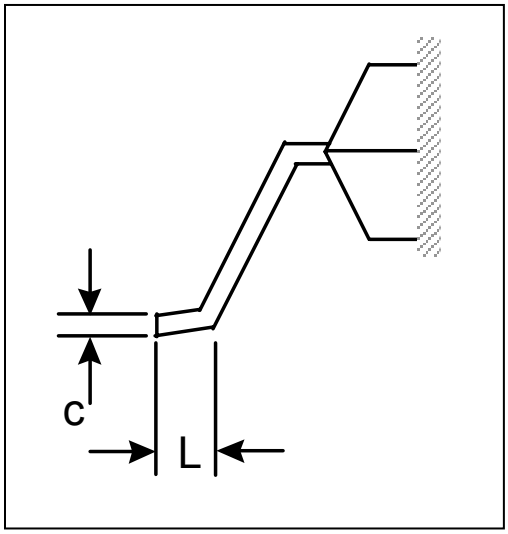
TMC2005-JT 64 PIN TQFP PACKAGE OUTLINE



SYMBOL	MIN (mm)	TYP (mm)	MAX (mm)
D	11.8	12.0	12.2
D1	9.9	10.0	10.1
E	11.8	12.0	12.2
E1	9.9	10.0	10.1
Ze	1.25 typ		
Zd	1.25 typ		



SYMBOL	MIN (mm)	TYP (mm)	MAX (mm)
A			1.6
A1	0.95	0.1	0.15
A2	1.35	1.4	1.45
B	0.17	0.22	0.27
E	0.5 BSC		
aaa	0.08		
bbb	0.08		



SYMBOL	MIN (mm)	TYP (mm)	MAX (mm)
c	0.9	0.145	0.2
L	0.45	0.6	0.75

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