SM806XXX

Ultra-Low Jitter Clock Generator

Features

- Generates up to 6 Differential or Single-Ended Outputs: Frequencies up to 875 MHz
- <65 fs Phase Jitter at 156.25 MHz (1.875 MHz to 20 MHz)
- 78 fs Phase Jitter at 156.25 MHz (12 kHz to 20 MHz)
- PCI Express Gen 1/2/3/4/5/6 Compliant
- On-Chip Power Supply Regulation for Excellent Power Supply Noise Immunity
- High Performance PLL generator to Generate Multiple Frequencies
- Independently Programmable Output Logic and Frequency:
  - Output Logic: LVPECL, LVDS, HCSL, LVCMOS
- Selectable Input:
  - Crystal: 50 MHz to 156.25 MHz (31.25 MHz to <50 MHz with Increased Phase Noise)
  - Reference Input: 50 MHz to 875 MHz
- SPI Programmable (See Flex SPI Documentation)
- No External Crystal Oscillator Capacitors Required
- 2.5V or 3.3V Operating Power Supply
- Separate Output Power Supplies:
  - Each Bank can be at a Different Power Supply Voltage Level (2 Banks of 3 Outputs Each)
- Industrial Temperature Range: –40°C to +85°C
- Green, RoHS, and PFOS Compliant VQFN Packages:
  - 48-Pin 7 mm × 7 mm (6 Differential or Single-Ended Outputs)
  - 24-Pin 4 mm × 4 mm (2 Differential or Single-Ended Outputs)

Applications

- 1/10/40/100/400/800 Gigabit Ethernet (GbE)
- SONET/SDH
- CPRI/OBSAI – Wireless Base Station
- Fibre Channel
- HDMI/HDTV-4K
- DIMM (DDR2-3-4/AMB)

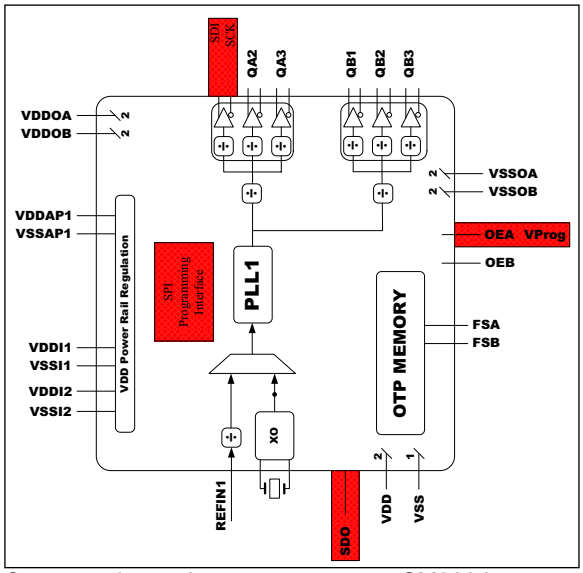
General Description

The SM806xxx is a PLL clock generator that achieves ultra-low phase jitter (78 fs_{RMS}). With six total outputs and dividers on each output, this device can generate six different frequencies up to 875 MHz, from a low-cost quartz crystal or a reference clock input.

Each of the six outputs can be independently programmed to LVPECL, LVDS, HCSL, or LVCMOS logic. For LVCMOS, only the true side of the channel is used.

The SM806xxx is packaged in a 48-pin VQFN with up to six outputs or a 24-pin VQFN with two outputs.

Functional Block Diagram



Create and sample your own custom SM806 here:

https://clockworks.microchip.com/microchip/design/inputSM806

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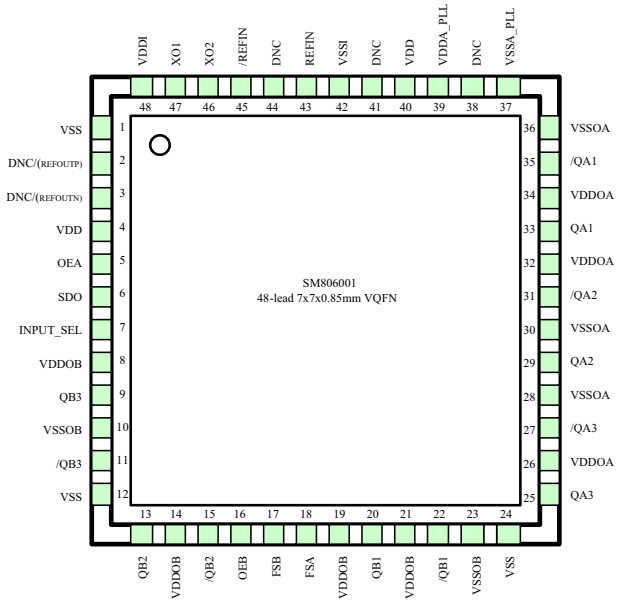
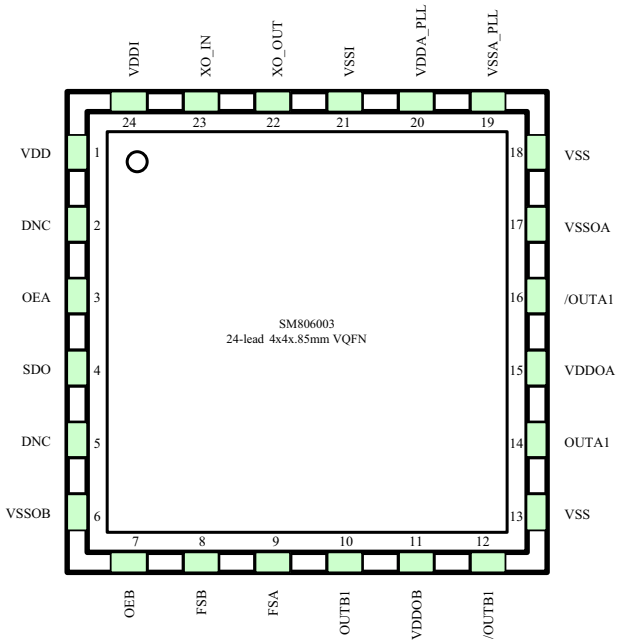
Package Types

SM806xxx (6 Outputs)
Option 1: 48-Pin 7 mm × 7 mm VQFN
(Top View)



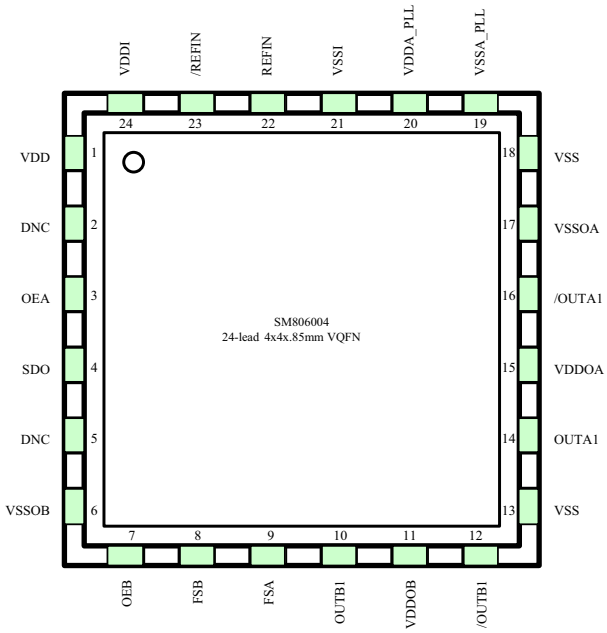
Full Feature Package

SM806xxx (2 Outputs)
Option 2: 24-Pin 4 mm × 4 mm VQFN
(Top View)



Crystal Reference

SM806xxx (2 Outputs)
Option 3: 24-Pin 4 mm × 4 mm VQFN
(Top View)



Differential Signal Reference

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}, V_{DDA}, V_{DDI}, V_{DDO}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.5V to +4.6V
ESD, Machine Model 200V
ESD, Human Body Model ..... 2 kV

Operating Ratings ††

Supply Voltage (V_{DD}, V_{DDO}) ..... +2.375V to +3.465V

† Notice: Exceeding the absolute maximum ratings may damage the device.

†† Notice: The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, typical values are valid for T_A = +25°C. The min. and max. values are valid for –40°C ≤ T_A ≤ +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}, V_{DDO}	2.375	2.5	2.625	V	2.5V Operation
		3.135	3.3	3.465		3.3V Operation
Analog & I/O Supply	V_{DDI}	2.375	—	3.465	V	—
PLL Core	V_{DDA}	2.375	—	3.465	V	—
PLL Core Current Consumption	I_{DDA}	—	—	60	mA	—
Analog & I/O Current	I_{DDI}	—	—	20	mA	—
Output Stage Current Consumption	I_{DDO}	—	—	70	mA	Per output bank, unloaded
SPI and Miscellaneous Logic	I_{DD}	—	—	8	mA	—

LVPECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCORE} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO} – 2V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{DDO} – 1.35	V_{DDO} – 1.01	V_{DDO} – 0.8	V	50Ω to V_{DDO} – 2V
Output Low Voltage	V_{OL}	V_{DDO} – 2	V_{DDO} – 1.78	V_{DDO} – 1.6	V	50Ω to V_{DDO} – 2V
Peak-to-Peak Output Voltage	V_{SWING}	0.65	0.77	0.95	V	Figure 5

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LVDS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCORE} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 100Ω between Q and /Q.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Differential Output Voltage	V_{OD}	245	350	454	mV	Figure 6-5
Common Mode Voltage	V_{CM}	1.125	1.2	1.375	V	—
Output High Voltage	V_{OH}	1.248	1.375	1.602	V	—
Output Low Voltage	V_{OL}	0.898	1.025	1.252	V	—

HCSL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCORE} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{SS}.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	660	700	850	mV	—
Output Low Voltage	V_{OL}	–150	0	27	mV	—
Crossing Point Voltage	V_{CROSS}	—	350	—	mV	—

LVCMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCORE} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO}/2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{DD} – 0.8	—	—	V	Highest Drive (Default)
Output Low Voltage	V_{OL}	—	—	0.5	V	—
Input High Voltage	V_{IH}	V_{DD} – 0.7	—	V_{DD} + 0.3	V	—
Input Low Voltage	V_{IL}	V_{SS} – 0.3	—	0.3 × V_{DD}	V	—
Input High Current	I_{IH}	—	—	5	µA	V_{DD} = V_{IN} = 3.465V
Input Low Current	I_{IL}	–150	—	—	µA	V_{DD} = 3.465V, V_{IN} = 0V

REF_IN DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Common Mode Voltage	V_{CMR}	0.3	—	V_{DD} – 0.3	V	Note 1
Input Voltage Swing	V_{SWING}	0.2	—	—	V_{PP}	Note 1

Note 1: See the Input Selection section.

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CRYSTAL CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Conditions
Mode of Oscillation	Fundamental, parallel resonant			—	—
Frequency	50	—	200	MHz	Note 1
Equivalent Series Resistance (ESR)	—	—	60	Ω	—
Load Capacitance, C_L	—	8.0	±0.5	pF	8.0 pF parallel load, typical
Shunt Capacitance, C0	—	0.3	1.5	pF	—
Correlation/Drive Level	—	10	200	µW	EIA-512

Note 1: Frequencies below 50 MHz can be used, but will have increased phase noise.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Frequency	f_{IN}	50	—	200	MHz	XO
		12.5	—	875	MHz	Reference Input
Output Frequency	f_{OUT}	12.5	—	875	MHz	LVPECL, LVDS, HCSL
		12.5	—	300	MHz	LVCMOS
Output Rise/Fall Time (Note 1)	t_r/t_f	85	135	350	ps	LVPECL output
		85	140	300		LVDS output
		175	200	400		HCSL output
		100	200	400		LVCMOS output (default drive)
Output Duty Cycle	ODC	45	50	55	%	All output frequencies
		48	50	52		<450 MHz output frequencies
Input to Output Propagation Delay	t_{PD}	–100	—	100	ps	ZDB mode
		—	4	—	ns	Generator/Bypass mode
Output-to-Output Skew (Note 2)	t_{SKEW}	—	—	50	ps	Same output bank, Note 3
PLL Lock Time	t_{LOCK}	—	5	20	ms	—
PCIe Refclk Jitter	$t_{jphPCIe6-CC}$	—	4	10	fs_{RMS}	PCIe Gen 6 (64 GT/s) in Clock Generator Mode
RMS Phase Jitter (Note 4, Note 5)	$t_{JIT(Ø)}$	—	78	100	fs	156.250 MHz, Integration range (12 kHz - 20 MHz)
		—	65	—		156.250 MHz, Integration range (1.875 MHz - 20 MHz)

Note 1: See Figure 6-5.

2: Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.

3: Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output logic type setting.

4: All phase noise measurements were taken with an Agilent 5052B phase noise system.

5: Measured using a 52.08333 MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1 MHz.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20s
Case Temperature	—	—	—	+115	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances (Note 1)						
Junction Thermal Resistance, 48-Lead 7 mm × 7 mm VQFN	θ_{JA}	—	23.4	—	°C/W	—
Junction Thermal Resistance, 24-Lead 4 mm × 4 mm VQFN	θ_{JA}	—	25	—	°C/W	Still-Air

Note 1: Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

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2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Numbers by Package Option			Pin Name	Pin Type	Pin Level	Pin Function
#1 48-pin	#2 24-pin	#3 24-pin				
33	14	14	QA1	O, (DIF/SE)	LVPECL LVDS HCSL LVCMOS (Q only)	Differential/SE Clock Output (LVCMOS)
35	16	16	/QA1			
29	—	—	QA2			
31	—	—	/QA2			
25	—	—	QA3			
27	—	—	/QA3			
20	10	10	QB1			
22	12	12	/QB1			
13	—	—	QB2			
15	—	—	/QB2			
9	—	—	QB3			
11	—	—	/QB3			
18	9	9	FSA	I, (SE)	LVCMOS	Frequency Select, on-chip 75 kΩ pull-up 1 = Primary Selection 0 = Secondary Selection
17	8	8	FSB			
4	1	1	V_{DD}	PWR	—	Power Supply
40	—	—				
26	15	15	V_{DDOA}	PWR	—	Power Supply for Outputs QA
32	—	—				
34	—	—				
8	11	11	V_{DDOB}	PWR	—	Power Supply for Outputs QB
14	—	—				
19	—	—				
21	—	—				
39	20	20	V_{DDAPLL}	PWR	—	Analog Power Supply for PLL
37	19	19	V_{SSAPLL}	PWR	—	Analog Power Supply for PLL
48	24	24	V_{DDI}	PWR	—	Power Supply for Reference Input Circuits and Crystal Oscillator
42	21	21	V_{SSI}	PWR	—	Ground for Reference Input Circuits and Crystal Oscillator
1	13	13	GND-V_{SS} (Exposed Pad)	PWR	—	Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
12	18	18				
24	—	—				
ePad	ePad	ePad				
28	17	17	V_{SSOA}	PWR	—	Ground Return Path for the Bank A Output Drivers
30	—	—				
36	—	—				
10	6	6	V_{SSOB}	PWR	—	Ground Return Path for the Bank B Output Drivers
23	—	—				

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Numbers by Package Option			Pin Name	Pin Type	Pin Level	Pin Function
#1 48-pin	#2 24-pin	#3 24-pin				
5	3	3	OEA1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QA1/2/3 disable to tri-state. 0 = Disabled 1 = Enabled, on-chip 75 kΩ pull-up
16	7	7	OEB1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QB1/2/3 disable to tri-state. 0 = Disabled 1 = Enabled, on-chip 75 kΩ pull-up
43	—	22	REFIN1	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Reference Clock Input 1
45	—	23	/REFIN1			
47	23	—	XTAL_IN	I, (SE)	Crystal	Crystal Reference Input, no external load caps needed
46	22	—	XTAL_OUT	O, (SE)	Crystal	Crystal Reference Output, no external load caps needed
38	2	2	NC	—	—	No Connect No internal connections to the ASIC are made
41	5	5				
44	—	—				
6	4	4	SDO	I/O, (SE)	LVCMOS	SPI bus pins for programming. Connect per standard data sheet for normal operation. See: Phoenix-Lite Programming Guide
33	14	14	SDI			
35	16	16	SCK			
5	3	3	V_{PROG}			

Note 1: Multi-function pins.

TABLE 2-2: TRUTH TABLE

OEA	OEB	Output
0	1	3 QA outputs tri-state
1	0	3 QB outputs tri-state

TABLE 2-3: FREQUENCY SELECT PIN

FSA	FSB	Output Frequency
0	1	QA outputs: Secondary output dividers QB outputs: Primary output dividers
1	0	QA outputs: Primary output dividers QB outputs: Secondary output dividers
1	1	QA outputs: Primary output dividers QB outputs: Primary output dividers
0	0	QA outputs: Secondary output dividers QB outputs: Secondary output dividers

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3.0 KEY PROGRAMMABLE PARAMETERS

3.1 Frequency Settings for One PLL and One Output Bank

The REF input frequency can be from a crystal or from a reference clock input. If a crystal is used, the REF input frequency range is 50 MHz to 200 MHz.

The VCO in the PLL has a range of 2875 MHz to 3540 MHz.

Counters M and P0 have a range of 4 to 259.

Counters P1, P2, and P3 have a range of 1 to 16.

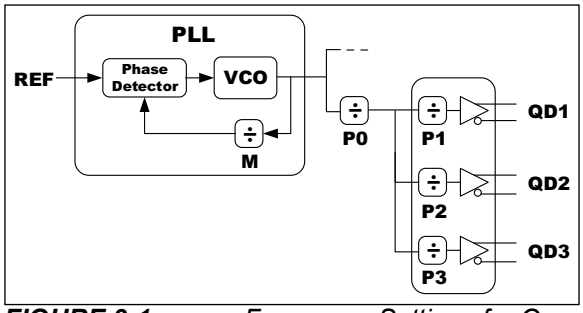

FIGURE 3-1: *Frequency Settings for One PLL and One Output Bank.*

EQUATION 3-1:

$$F_{VCO} = REF \times M$$

EQUATION 3-2:

$$QD1 = F_{VCO} \div (P0 \times P1)$$

EQUATION 3-3:

$$QD2 = F_{VCO} \div (P0 \times P2)$$

EQUATION 3-4:

$$QD3 = F_{VCO} \div (P0 \times P3)$$

3.2 Output Logic Programming

Available output logic types are LVPECL, LVDS, HCSL, and LVCMOS. Each output can be programmed individually to one of the four logic types.

All logic types are differential, except LVCMOS. For LVCMOS, only the true channel of the output pair is enabled and the complementary channel is disabled. With LVCMOS there is also an output drive setting. There is one setting for all LVCMOS outputs, so all LVCMOS outputs will have the same drive strength.

Unused outputs are disabled to high impedance.

3.3 Input Selection

The reference input for the PLLs can be programmed to be either a crystal or a reference clock.

The crystal oscillator circuit has capacitors on the IC, so external capacitors are not required.

There are two reference clock inputs, one for each PLL. Make sure they are connected to the same reference input source. The reference inputs can be differential or single-ended and require only a small amplitude. See Figure 3-2.

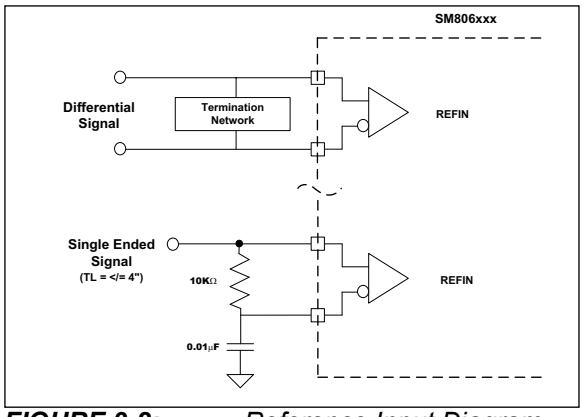

FIGURE 3-2: *Reference Input Diagram.*

The single-ended signal input can be LVCMOS, but smaller amplitudes like a >800 mV_{PP} clipped sine wave from a TCXO will also work.

3.4 Frequency Select Programming

Each of the four output banks has a frequency select pin. For each bank, two P0, P1, P2, and P3 counter values can be programmed, a primary and a secondary value. The frequency select pin toggles between the two values assigned to each counter, changing the output frequencies.

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4.0 APPLICATION INFORMATION

4.1 Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

4.2 Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the ANTC207 application note for further details.

4.3 Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin and start a 50Ω trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50Ω traces. For EMI reasons, it is better to use a balanced differential transmission line design.

LVDS can be AC-coupled or DC-coupled to its termination.

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5.0 POWER SUPPLY FILTERING RECOMMENDATIONS

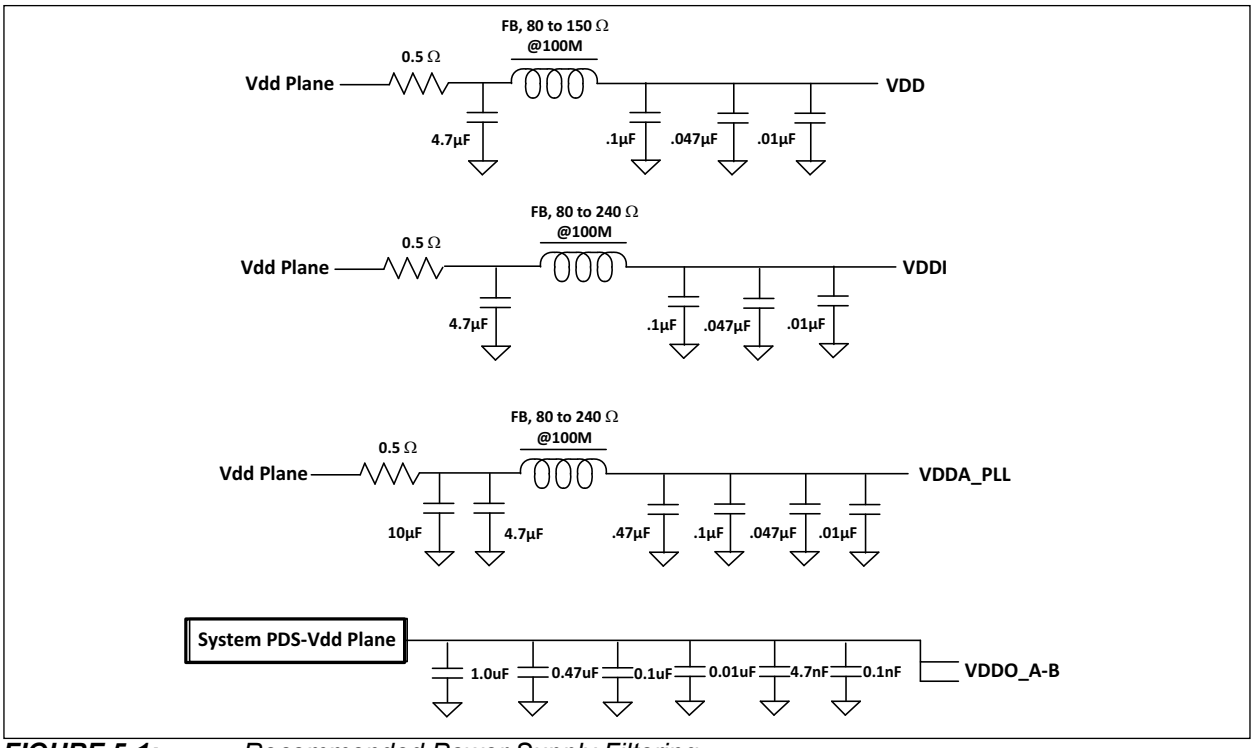

FIGURE 5-1: *Recommended Power Supply Filtering.*

- Use the power supply filtering shown in Figure 5-1 for V_{DDAP1}, V_{DDAP2}, V_{DDI1}, and V_{DDI2}.
- Connect the V_{DDO} and V_{DD} pins directly to the V_{DD} power plane.
- Connect all V_{SS} pins directly to the ground power plane.
- Recommended ferrite bead properties are 80Ω to 240Ω impedance and >250 mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, the Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in Figure 5-2 and can be used for any of the above V_{DD} sections.

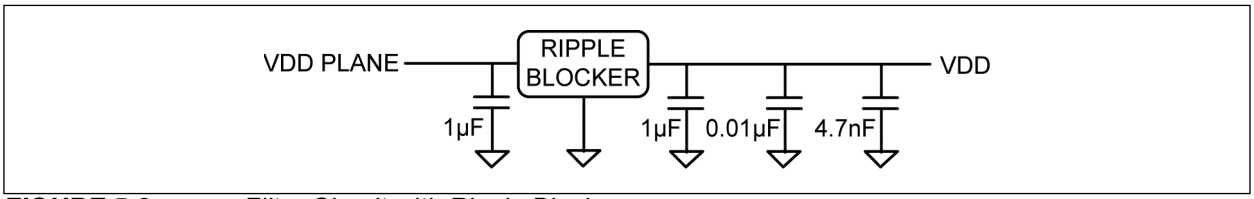

FIGURE 5-2: *Filter Circuit with Ripple Blocker.*

6.0 DIAGRAMS AND TEST CIRCUITS

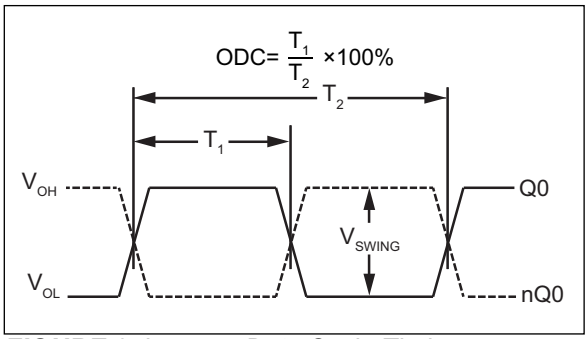

FIGURE 6-1: *Duty Cycle Timing.*

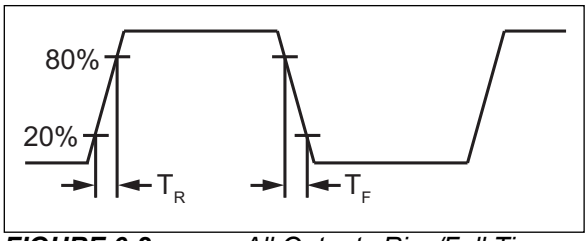

FIGURE 6-2: *All Outputs Rise/Fall Time.*

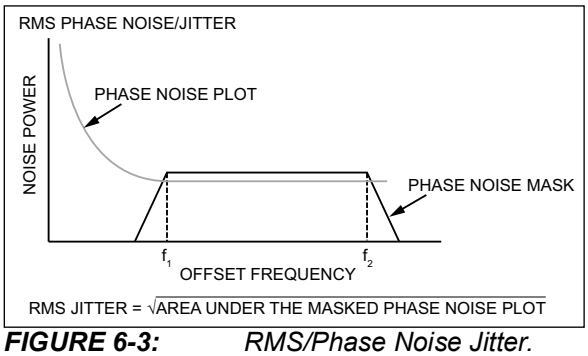

FIGURE 6-3: *RMS/Phase Noise Jitter.*

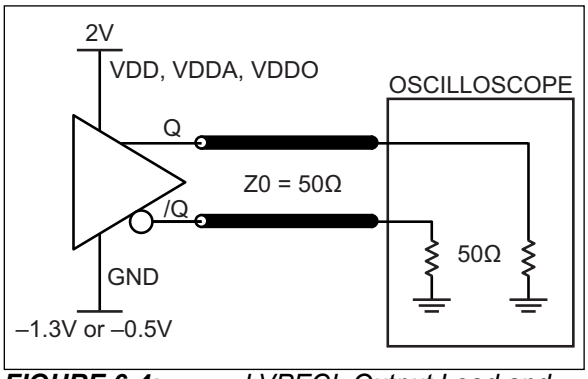

FIGURE 6-4: *LVPECL Output Load and Test Circuit.*

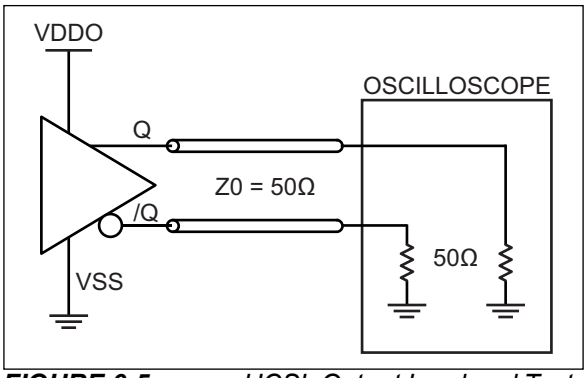

FIGURE 6-5: *HCSL Output Load and Test Circuit.*

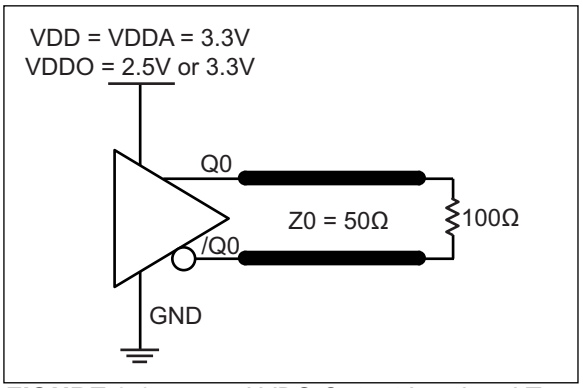

FIGURE 6-6: *LVDS Output Load and Test Circuit.*

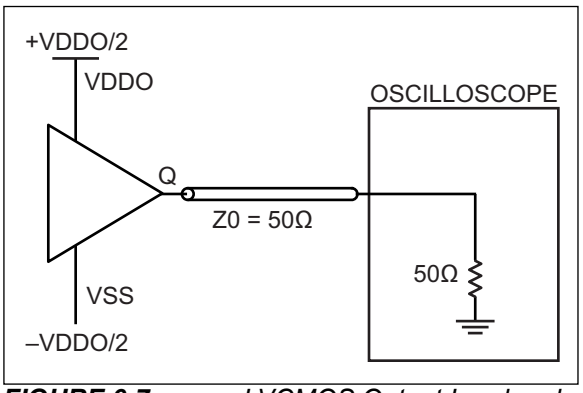

FIGURE 6-7: *LVCMOS Output Load and Test Circuit.*

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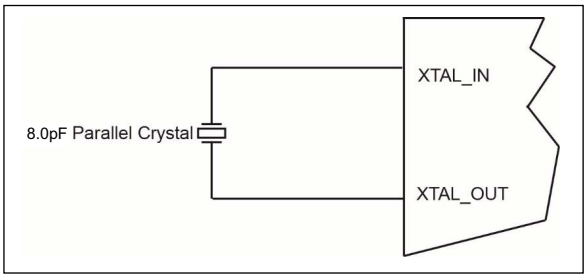

FIGURE 6-8: *SM806xxx Crystal Input Interface.*

6.1 HCSL Source Terminated per JESD8-18A

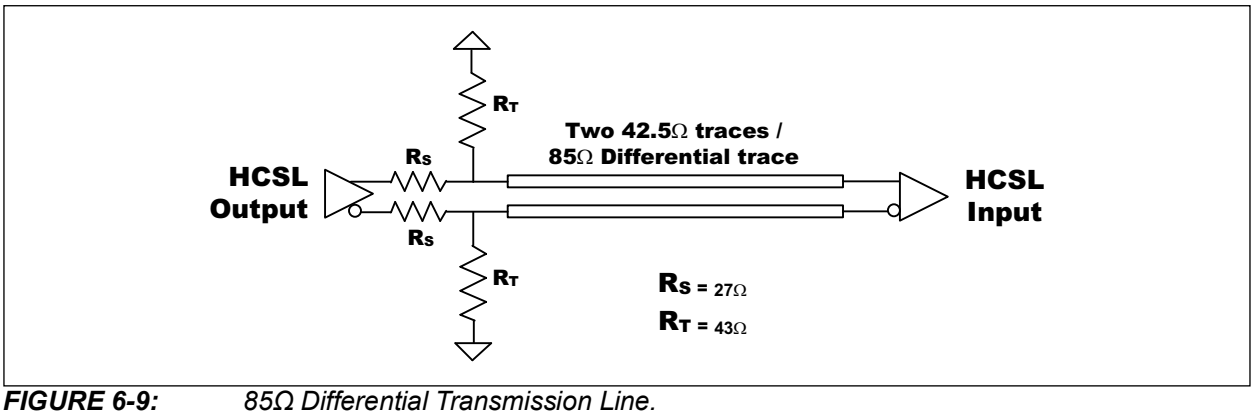

FIGURE 6-9: *85Ω Differential Transmission Line.*

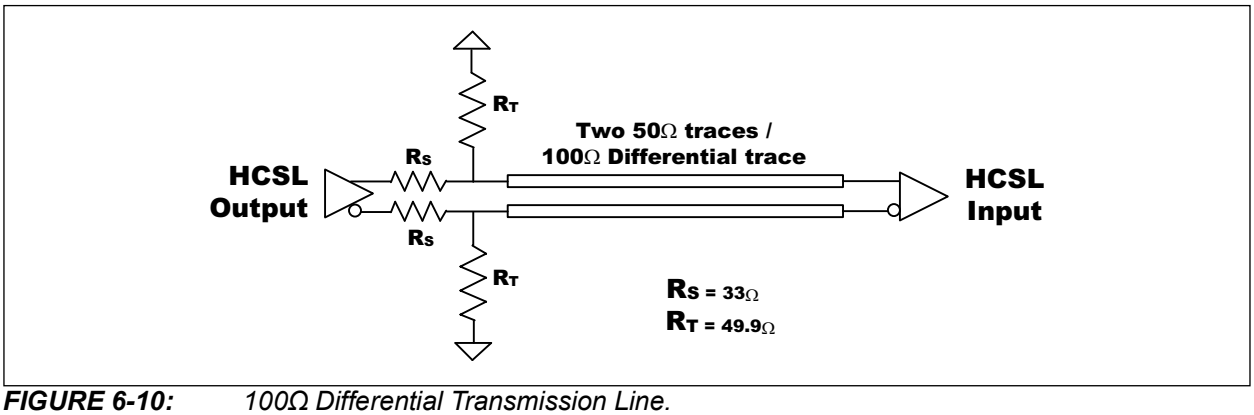

FIGURE 6-10: *100Ω Differential Transmission Line.*

7.0 PHASE NOISE PERFORMANCE

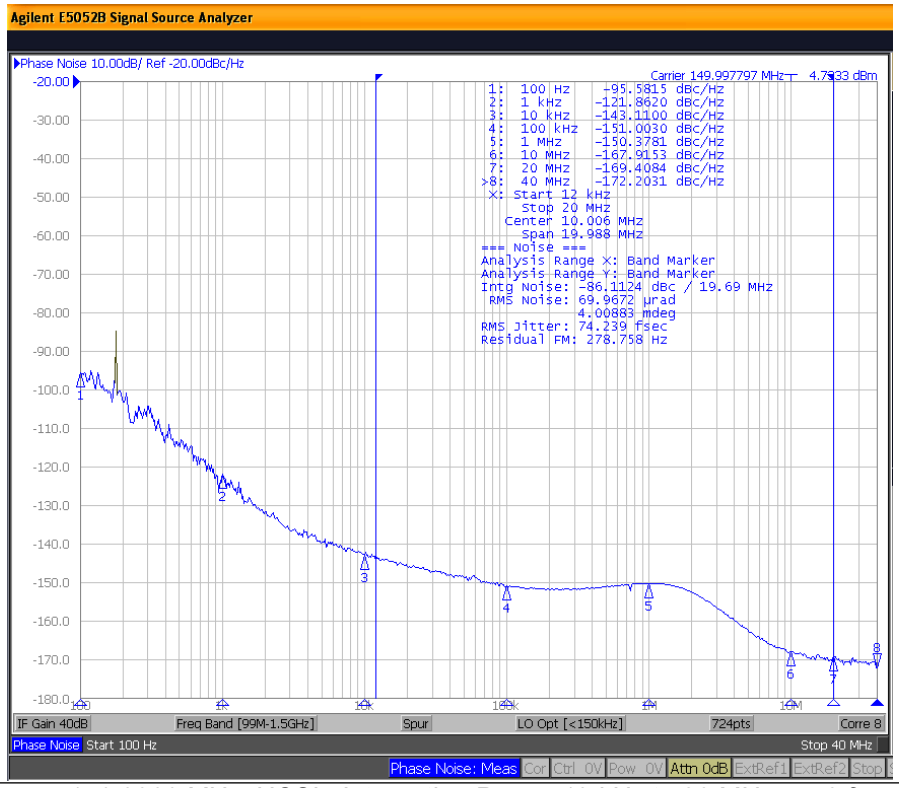

FIGURE 7-1: *150.0000 MHz, HCSL, Integration Range 12 kHz to 20 MHz: 74.2 fs_{RMS}.*

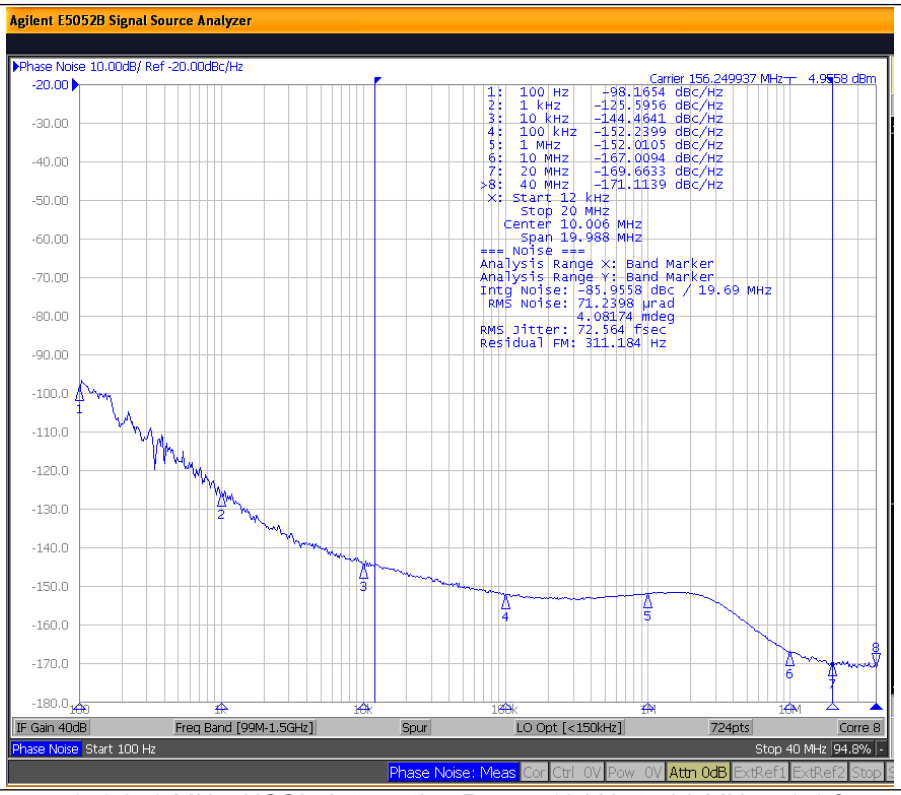

FIGURE 7-2: *156.250 MHz, HCSL, Integration Range 12 kHz to 20 MHz: 72.6 fs_{RMS}.*

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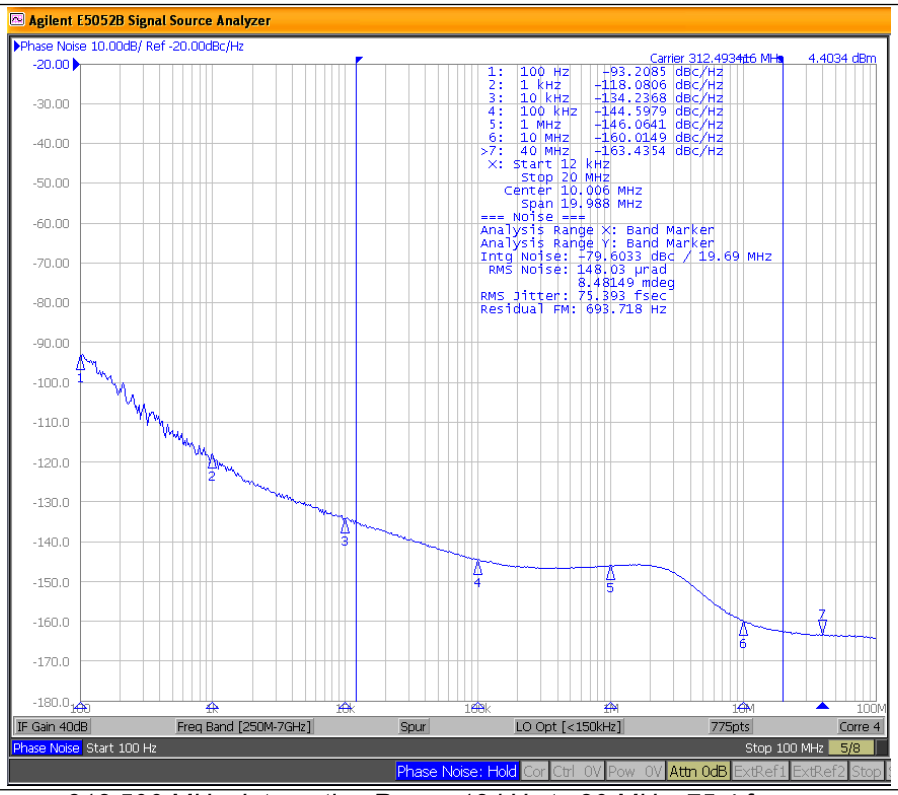


FIGURE 7-3: *312.500 MHz, Integration Range 12 kHz to 20 MHz: 75.4 fs_{RMS}.*

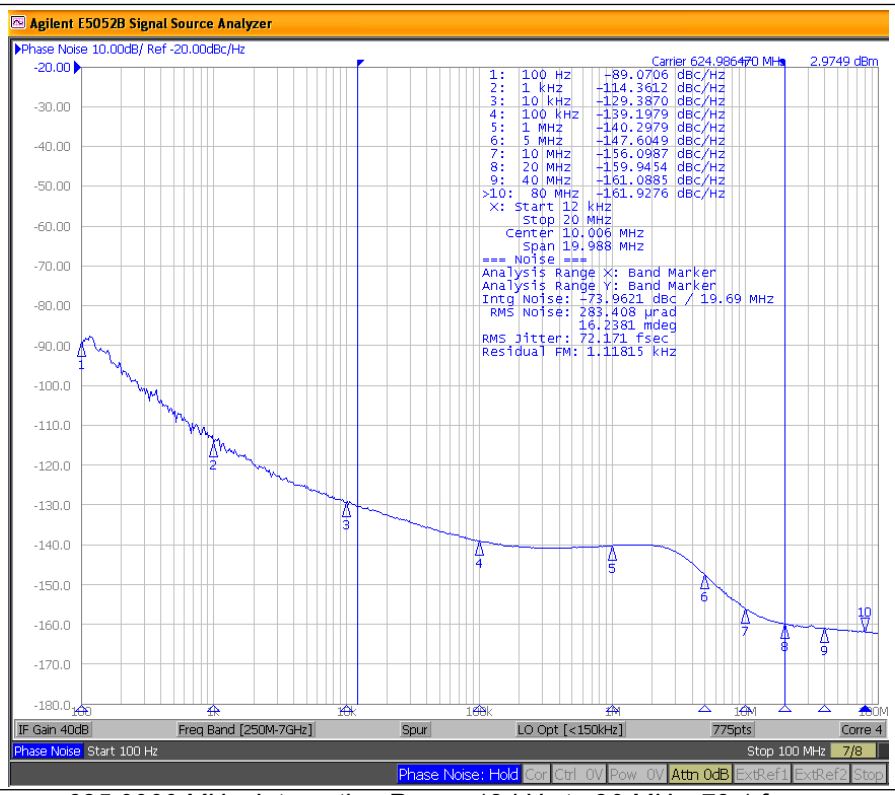
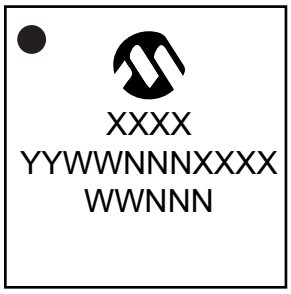


FIGURE 7-4: *625.0000 MHz, Integration Range 12 kHz to 20 MHz: 72.1 fs_{RMS}.*

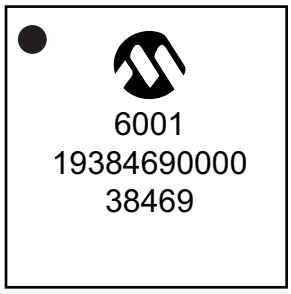
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

48-Lead VQFN*



Example



24-Lead VQFN*

Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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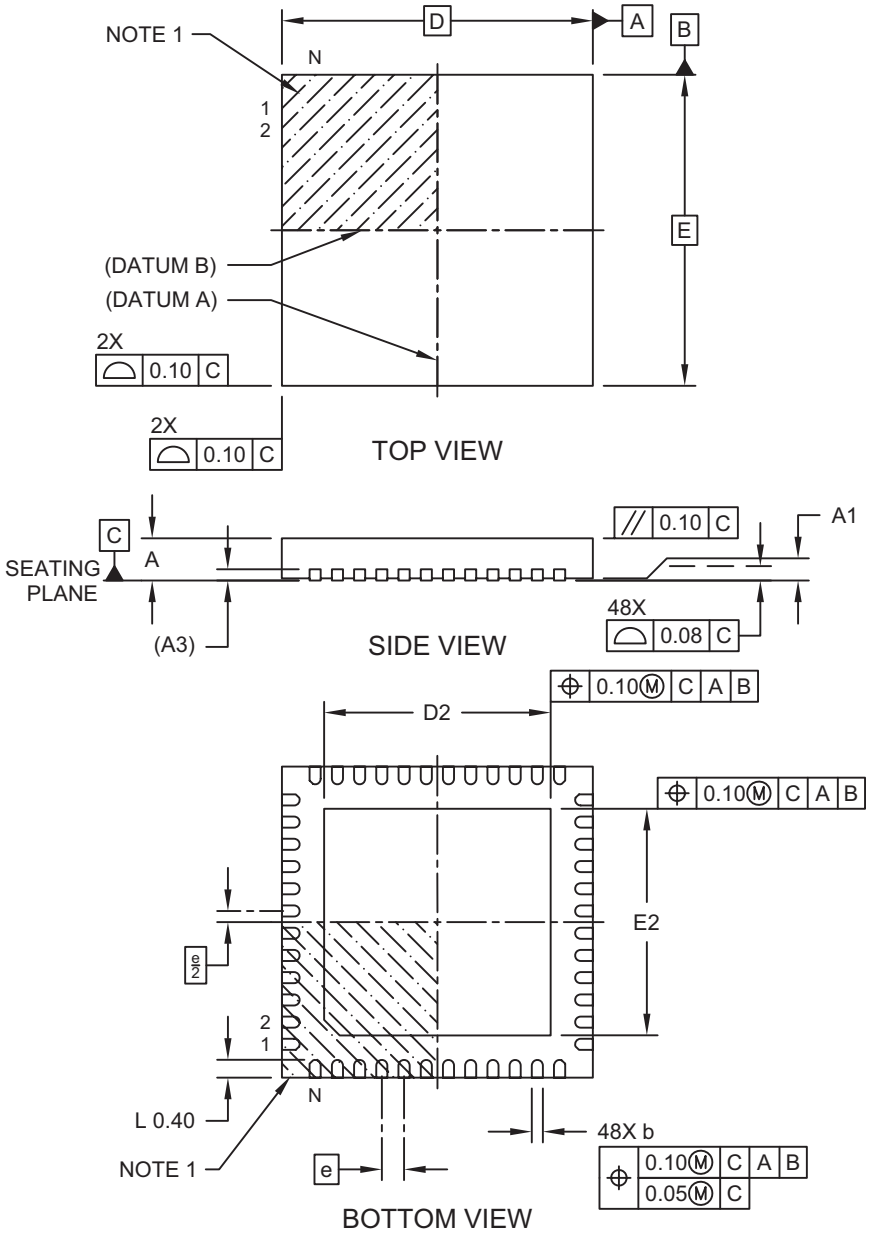
48-Lead Very Thin Plastic Quad Flat, No Lead Package (PTA) - 7x7x0.9 mm Body [VQFN] With 5.1x5.1 mm Exposed Pad; Micrel Legacy Package QFN77-48L

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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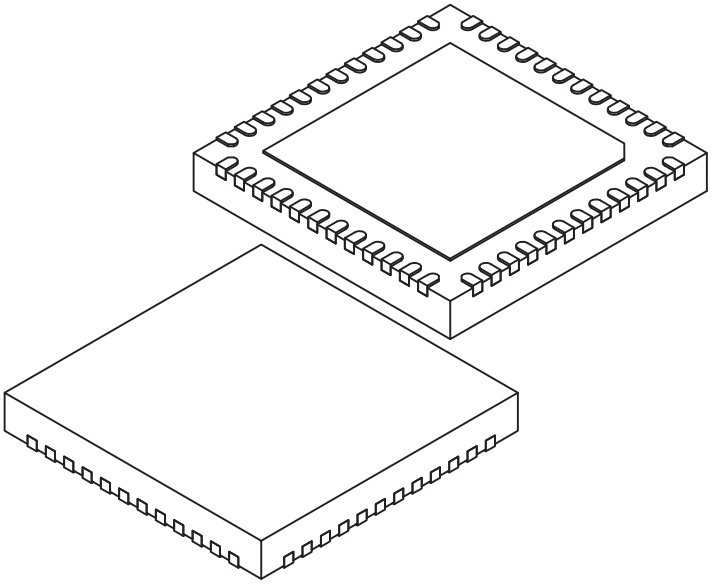
48-Lead Very Thin Plastic Quad Flat, No Lead Package (PTA) - 7x7x0.9 mm Body [VQFN] With 5.1x5.1 mm Exposed Pad; Micrel Legacy Package QFN77-48L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	48		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.253 REF		
Overall Length	D	7.00 BSC		
Exposed Pad Length	D2	5.05	5.10	5.15
Overall Width	E	7.00 BSC		
Exposed Pad Width	E2	5.05	5.10	5.15
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-01270 Rev B Sheet 2 of 2

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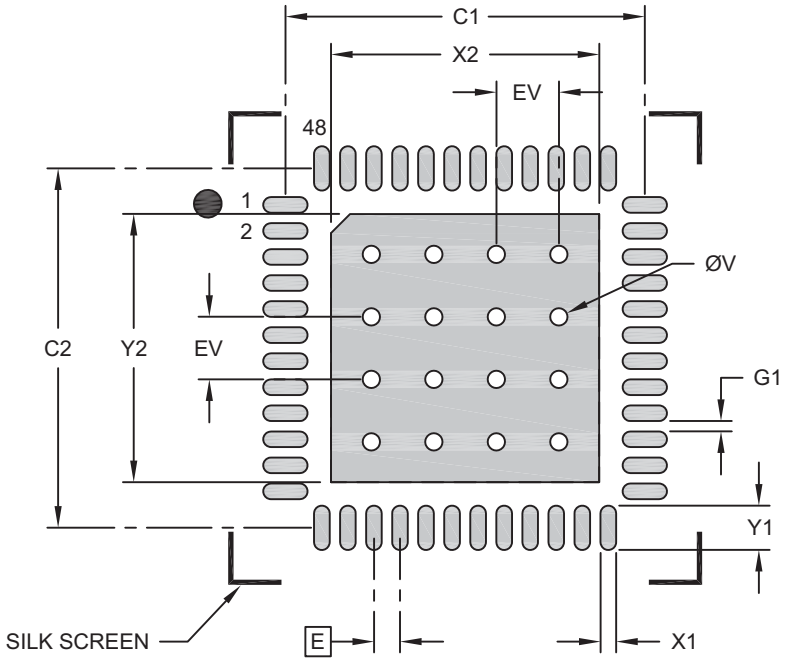
48-Lead Very Thin Plastic Quad Flat, No Lead Package (PTA) - 7x7x0.9 mm Body [VQFN] With 5.1x5.1 mm Exposed Pad; Micrel Legacy Package QFN77-48L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			5.15
Optional Center Pad Length	Y2			5.15
Contact Pad Spacing	C1		6.90	
Contact Pad Spacing	C2		6.90	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			0.85
Contact Pad to Contact Pad (X44)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

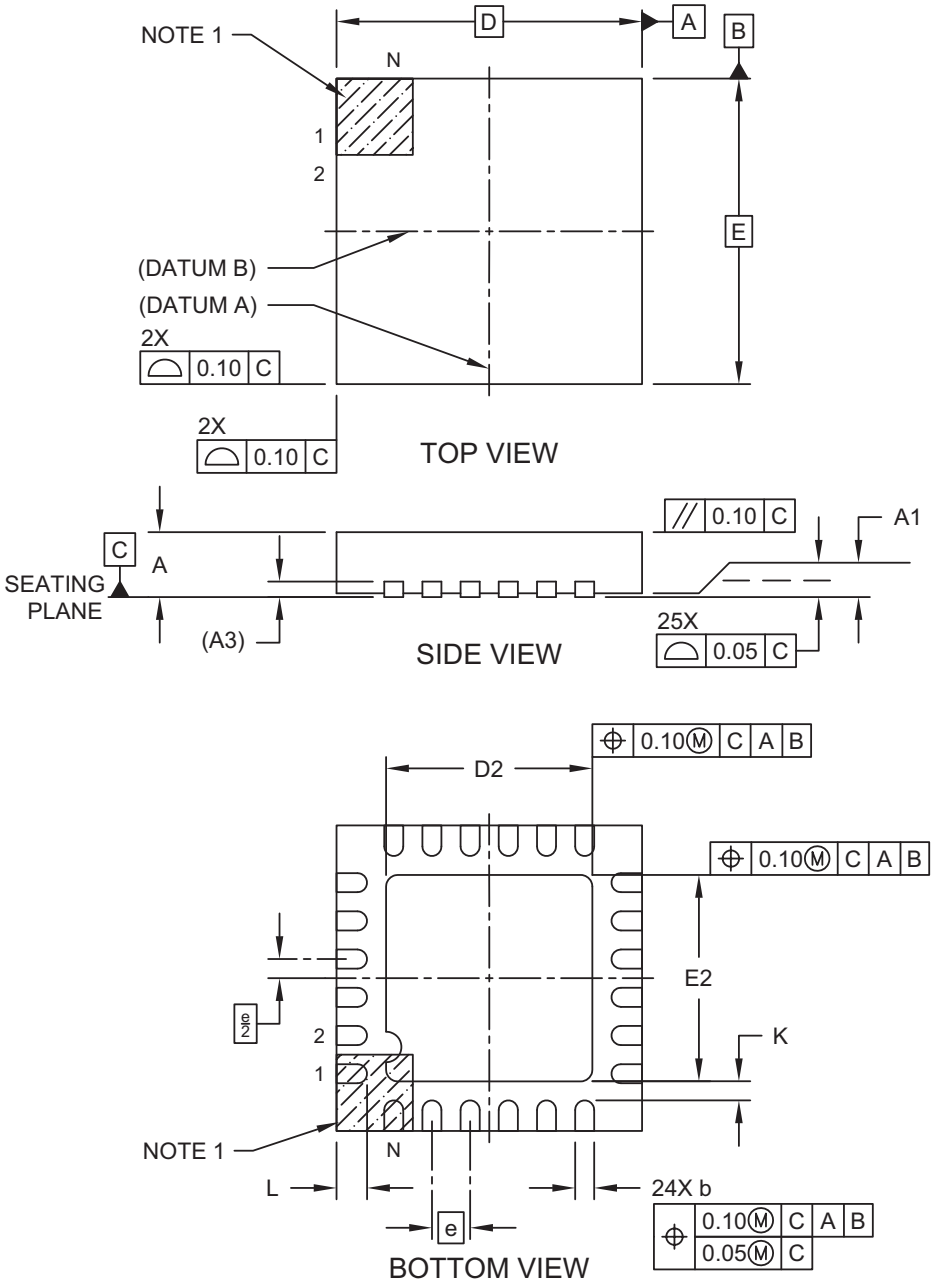
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3270 Rev B

24-Lead Very Thin Plastic Quad Flat, No Lead Package (9KX) - 4x4 mm Body [VQFN] With 2.7x2.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-428 Rev A Sheet 1 of 2

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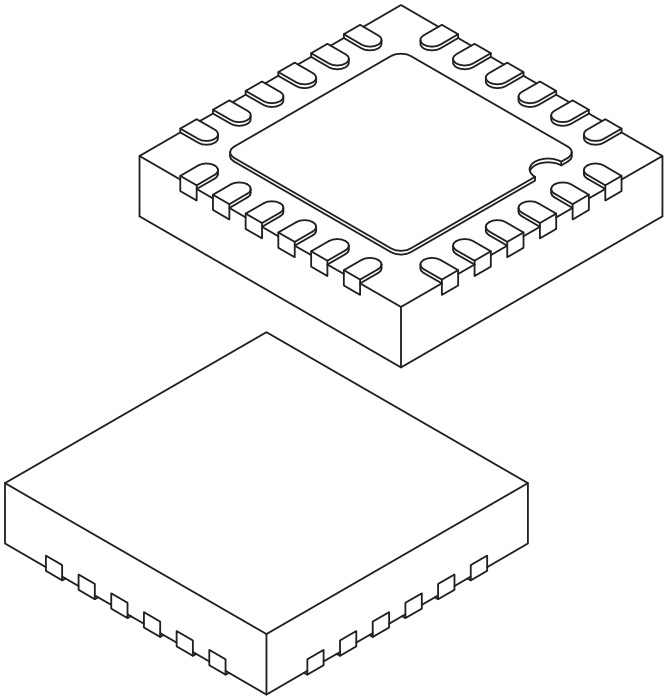
24-Lead Very Thin Plastic Quad Flat, No Lead Package (9KX) - 4x4 mm Body [VQFN] With 2.7x2.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	24		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.60	2.70	2.80
Overall Width	E	4.00 BSC		
Exposed Pad Width	E2	2.60	2.70	2.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

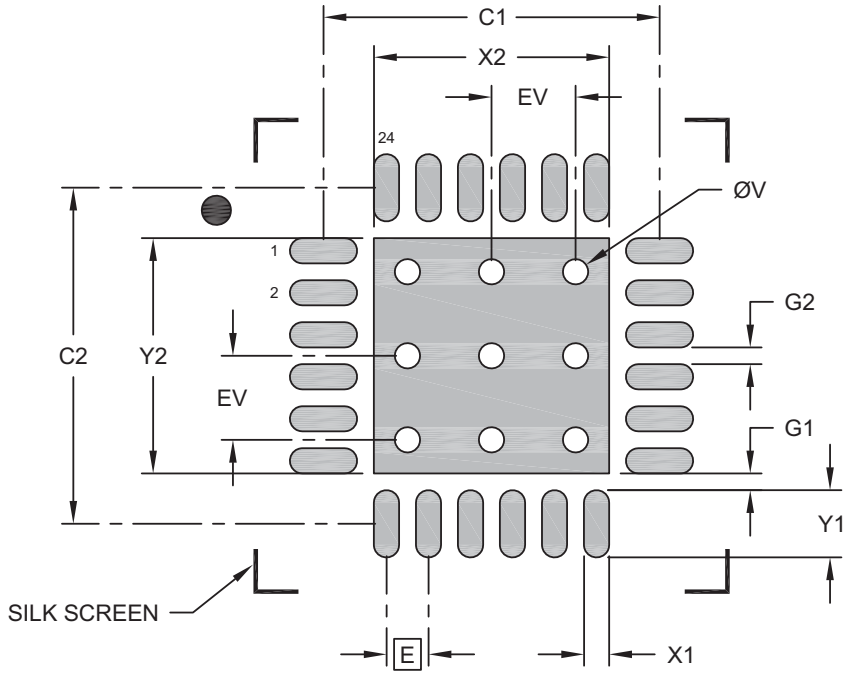
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-428 Rev A Sheet 2 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (9KX) - 4x4 mm Body [VQFN] With 2.7x2.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.80
Contact Pad to Center Pad (X24)	G1	0.20		
Contact Pad to Contact Pad (X20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2428 Rev A

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APPENDIX A: REVISION HISTORY

Revision A (August 2019)

- Initial release of SM806xxx data sheet DS20006212A.

Revision B (September 2019)

- Updated Functional Block Diagram.
- Updated Selectable Input: information in the Features section.
- Added a conditional note for the Frequency parameter of the Crystal Characteristics table.
- Added maximum value for RMS Phase Jitter and updated crystal information for Note 5 in the AC Electrical Characteristics table.

Revision C (March 2021)

- Added text below the Functional Block Diagram directing users to create their own version of the device.

Revision D (January 2023)

- Updated the Applications list to include PCIe Gen 5 and Gen 6

Revision E (October 2024)

- Updated the Applications list to include PCIe Gen 5 and Gen 6.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X
Device	Voltage Option	Package Type	Temperature	Special Processing

Device:	SM806xxx:	Flexible Ultra-Low Jitter Clock Generator	
Voltage Option:	U	=	2.5V/3.3V
Package Type:	M	=	48- or 24-VQFN; see the Package Option Table.
Temperature:	G	=	–40°C to +85°C (NiPdAu Lead Free)
	Y	=	–40°C to +85°C (Matte-Sn Lead Free)
Special Processing:	Blank	=	Tray
	R	=	Tape and Reel

Package Option Table

Package Option	Package	Outputs	OE & FSEL Control	Reference Type (Ext. or Crystal)
1	48-Lead 7x7 VQFN	6	Yes	Both
2	24-Lead 4x4 VQFN	2	Yes	Crystal
3	24-Lead 4x4 VQFN	2	Yes	External

Note: Use the web tool at http://clockworks.microchip.com/timing to determine your desired configuration.

Examples:

a) SM806xxxUMG: Flexible Ultra-Low Jitter Clock Generator, 2.5V/3.3V Voltage Option, 48- or 24-VQFN Package, –40°C to +85°C Temperature Range (NiPdAu), Tray

b) SM806xxxUMGR: Flexible Ultra-Low Jitter Clock Generator, 2.5V/3.3V Voltage Option, 48- or 24-VQFN Package, –40°C to +85°C Temperature Range (NiPdAu), Tape & Reel

c) SM806xxxUMY: Flexible Ultra-Low Jitter Clock Generator, 2.5V/3.3V Voltage Option, 48- or 24-VQFN Package, –40°C to +85°C Temperature Range (Matte-Sn), Tray

d) SM806xxxUMYR: Flexible Ultra-Low Jitter Clock Generator, 2.5V/3.3V Voltage Option, 48- or 24-VQFN Package, –40°C to +85°C Temperature Range (Matte-Sn), Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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