

Low Power, 1.62V to 3.63V, 10MHz to 40MHz, 1:4 Oscillator Fanout Buffer

FEATURES

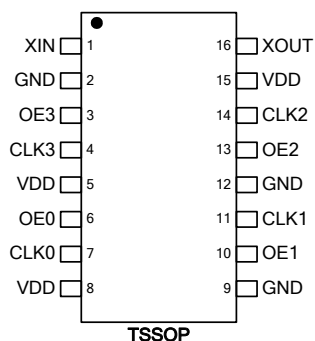
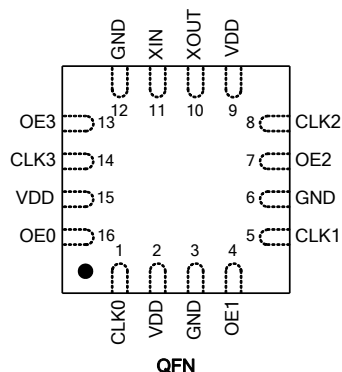
- Advanced Oscillator Design for Wide Frequency Coverage
- 4 LVCMOS Outputs with Individual OE Control
- 8mA Output Drive Strength
- Input/Output Frequency:
 - Fundamental Crystal: 10MHz to 40MHz
- Very Low Jitter and Phase Noise
- Low Current Consumption
- Single 1.62V to 3.63V Power Supply
- Available in QFN-16L and TSSOP-16L GREEN/RoHS Compliant Packages

DESCRIPTION

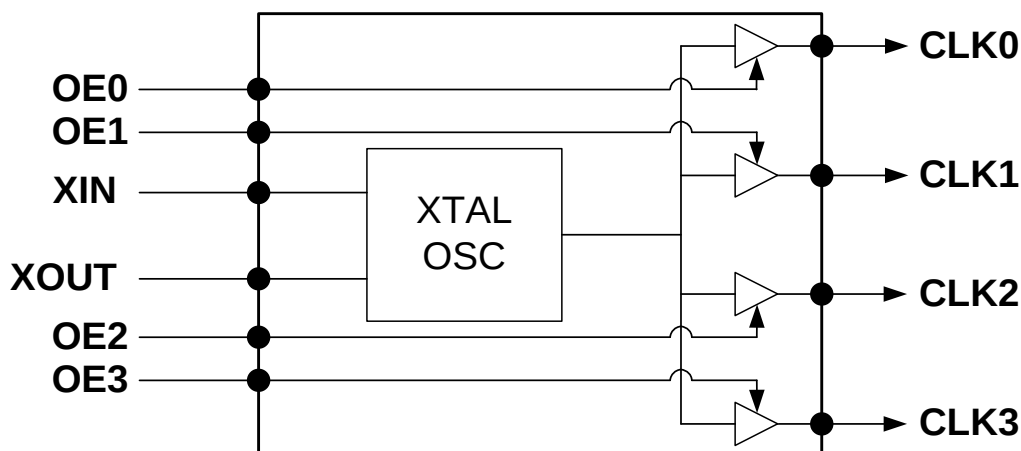
The PL135-47 is an advanced oscillator fanout buffer design for high performance, low-power, small form-factor applications. The PL135-47 accepts a fundamental input crystal of 10MHz to 40MHz and produces four outputs of the same frequency, each with its own Output Enable pin.

Offered in a small 3 x 3mm QFN or TSSOP package, the PL135-47 offers the best phase noise and jitter performance and lowest power consumption of any comparable IC.

PACKAGE PIN CONFIGURATION



BLOCK DIAGRAM



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PACKAGE PIN ASSIGNMENT

Name	Package Pin #		Type	Description
	QFN-16L	(T)SSOP-16L		
CLK0	1	7	O	Output clock
VDD	2, 9, 15	5, 8, 15	P	V _{DD} connection
GND	3, 6, 12	2, 9, 12	P	GND connection
OE1	4	10	I*	Output enable (OE) input for CLK1. Internal pull-up. Pull low to tri-state CLK1.
CLK1	5	11	O	Output clock
OE2	7	13	I*	Output enable (OE) input for CLK2. Internal pull-up. Pull low to tri-state CLK2.
CLK2	8	14	O	Output clock
XOUT	10	16	O	Crystal output. Do not connect when using a reference clock.
XIN	11	1	I	Crystal input
OE3	13	3	I*	Output enable (OE) input for CLK3. Internal pull-up. Pull low to tri-state CLK3.
CLK3	14	4	O	Output clock
OE0	16	6	I*	Output enable (OE) input for CLK0. Internal pull-up. Pull low to tri-state CLK0.

* **Note:** These pins include an internal 60K Ω pull up.

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LAYOUT RECOMMENDATIONS

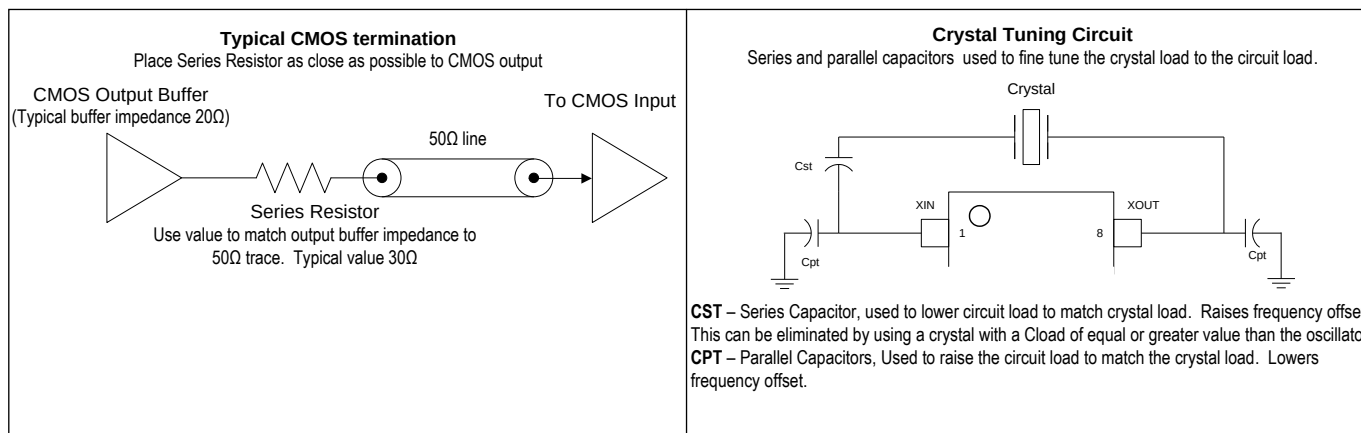
The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the V_{DD} pin(s) to limit noise from the power supply
- Multiple V_{DD} pins should be decoupled separately for best performance.
- Addition of a ferrite bead in series with V_{DD} can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical value to use is 0.1 μ F.



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	V_I	-0.5	$V_{DD}+0.5$	V
Output Voltage Range	V_O	-0.5	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	$^{\circ}$ C
Ambient Operating Temperature*		-40	85	$^{\circ}$ C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

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AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency	Fundamental crystal	10		40	MHz
Settling Time	At power-up ($V_{DD} \geq 1.62V$)			2	ms
Output Enable Time	OE Function; $T_a = 25^\circ C$			10	ns
V_{DD} Sensitivity	Frequency vs. V_{DD} , $\pm 10\%$	-2		2	ppm
Output Rise Time	15pF Load, 10/90% V_{DD} , 3.3V		2	4	ns
Output Fall Time	15pF Load, 90/10% V_{DD} , 3.3V		2	4	ns
Output to Output Skew	Under all conditions			1	ns
Duty Cycle	Under all conditions	45	50	55	%

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Dynamic	I_{DD}	$V_{DD} = 3.3V$, 25MHz, No Load		6.5		mA
		$V_{DD} = 2.5V$, 25MHz, No Load		4.4		mA
		$V_{DD} = 1.8V$, 25MHz, No Load		3.2		mA
Operating Voltage	V_{DD}		1.62		3.63	V
Output Low Voltage	V_{OL}	$I_{OL} = +4mA$, 3.3V			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$, 3.3V	2.4			V
Output Current	I_{OSD}	$V_{OL} = 0.4V$, $V_{OH} = 2.4V$	8			mA

CRYSTAL SPECIFICATIONS

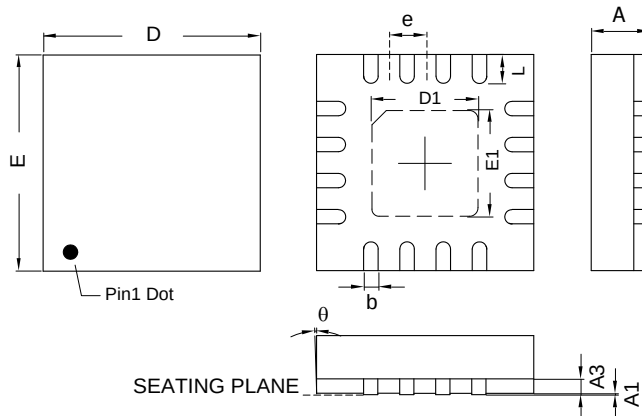
PARAMETERS		SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency		F_{XIN}	10		40	MHz
Crystal Loading Rating		$C_{L(xtal)}$		15		pF
Operating Drive Level				0.1	2	mW
Metal Can Crystal	Shunt Capacitance	C_0			5.5	pF
	ESR Max	ESR			40	Ω
Small SMD Crystal	Shunt Capacitance	C_0			2.5	pF
	ESR Max	ESR			60	Ω

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PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

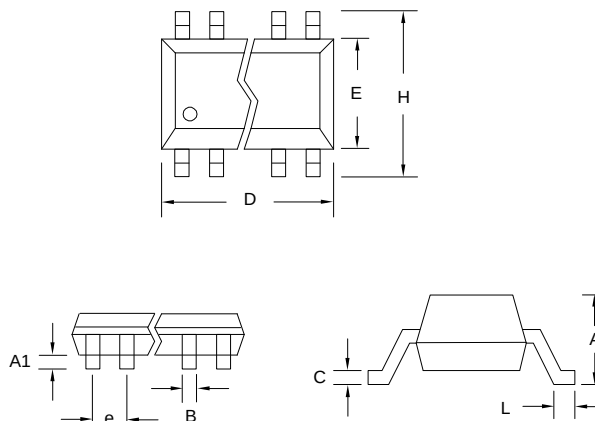
QFN 16L

Symbol	Dimension in MM	
	Min.	Max.
A	0.07	0.8
A1	0.05	0.05
A3	0.20	
b	0.18	0.30
D	3.00 BSC	
E	3.00 BSC	
D1	--	1.70
E1	--	1.70
L	0.30	0.50
e	0.50 BSC	



TSSOP 16L

Symbol	Dimension in MM	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
b	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.20	6.60
L	0.45	0.75
e	0.635 BSC	



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ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:

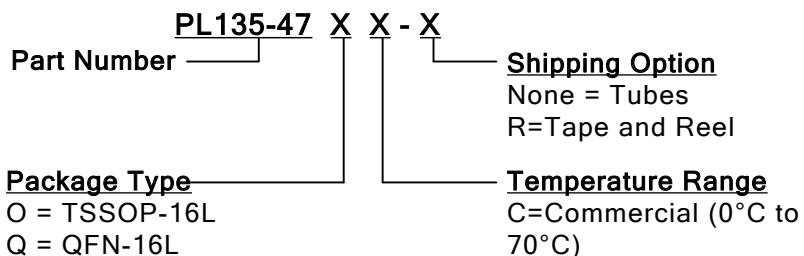
2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:

Part number, Package type and Operating temperature range



Part Number/Order Number	Marking	Package Option
PL135-47OC	P135-47	16-Pin TSSOP (Tube)
PL135-47OC-R	OC LLLLL	16-Pin TSSOP (Tape and Reel)
PL135-47QC-R	P135 47 LLL	16-Pin QFN (Tape and Reel)

*Note: "LLL" or "LLLLL" designates lot number

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[PL135-47OC](#) [PL135-47OC-R](#) [PL135-47SC](#) [PL135-47QC-R](#) [PL135-47QC](#) [PL135-47QI-R](#) [PL135-47QI](#) [PL135-47OI-R](#) [PL135-47OI](#)