

PIC32MK MCM 100-pin Motor Control Plug-In Module (PIM) Information Sheet

The PIC32MK MCM 100-pin Motor Control Plug-in Module (PIM) (MA320211) is designed to demonstrate the capabilities of the PIC32MK MCM 100-pin Motor Control device, PIC32MK1024MCM100, using external or internal on-chip op amps with the following hardware:

- dsPICDEM™ MCLV-2 development board (DM330021-2)
- dsPICDEM™ MCHV-2 development board (DM330023-2)
- dsPICDEM™ MCHV-3 development board (DM330023-3)

All above development boards support 100-pin PIM interfaces.

Selecting the External On-board Op Amp Configuration

To operate the PIC32MK MCM 100-pin Motor Control PIM using external on-board op amps, insert the External Op amp Configuration Board, which is included with the development board, into the appropriate header for the hardware in use:

- J14 (dsPICDEM™ MCLV-2 development board)
- J4 (dsPICDEM™ MCHV-2/MCHV-3 development board). In addition, for MCHV-2/MCHV-3, ensure that jumpers are set at position 1-2 for J12, J13, J14, and position 5-6 for J11.

Figure 1 shows the connection location for the external on-board op amp on the dsPICDEM MCLV-2 development board.

FIGURE 1: EXTERNAL OP AMP CONFIGURATION BOARD



Selecting the Internal On-board Op Amp Configuration

To operate the PIC32MK MCM 100-pin Motor Control PIM using internal on-chip op amps, insert the Internal Op Amp Configuration Board, which is included with the development board, into the appropriate header for the hardware in use:

- J14 (dsPICDEM MCLV-2 development board)
- J4 (dsPICDEM MCHV-2/MCHV-3 development board)

Figure 2 shows the connection locations for the internal on-board op amp on the dsPICDEM MCLV-2 development board.

FIGURE 2: INTERNAL OP AMP CONFIGURATION BOARD



WARNING: Do not connect non-isolated oscilloscope probes to probe any traces while using the PIM with the dsPICDEM MCHV-2 or dsPICDEM MCHV-3 development boards. Instead, use a high-voltage differential probe, rate in excess of 600 VRMS (Common mode). Failure to heed this warning could result in hardware damage.

Table 1 provides the static mapping between the 100-pin PIM pins and the 100-pin device pins.

Figure 3 shows the 100-pin PIM header schematic.

Figure 4 shows the 100-pin PIM device schematic.

TABLE 1: PIN MAP

PIM Pin Number	PIC32MK MCM		dsPICDEM MCLV2 Board 100-pin PIM Header		dsPICDEM MCHV2/MCHV3 Board 100-pin PIM Header	
	Pin Number	Pin Name	Pin Name	Pin Functionality	Pin Name	Pin Functionality
1	1	RG15	DBG_LED2	Debug LED 2	DBG_LED1	Debug LED 1
2	2	VDD	VDD	VDD	+3.3V_DIG	VDD
3	93	PWM3H	PWM1H3	Phase M3 High-Side PWM	PWM1H3	Phase M3 High-Side PWM
4	6	PWM5L	N/A	N/A	N/A	N/A
5	N/A	N/A	N/A	N/A	N/A	N/A
6	8	PWM6L	N/A	N/A	N/A	N/A
7	9	PWM6H	N/A	N/A	N/A	N/A
8	17	AN22	N/A	N/A	N/A	N/A
9	18	AN21	N/A	N/A	N/A	N/A
10	N/A	N/A	N/A	N/A	N/A	N/A
11	N/A	N/A	N/A	N/A	N/A	N/A
12	N/A	N/A	N/A	N/A	N/A	N/A
13	13	$\overline{\text{MCLR}}$	$\overline{\text{MCLR}}$	Master Clear Reset ($\overline{\text{MCLR}}$)	$\overline{\text{MCLR}}$	Master Clear Reset ($\overline{\text{MCLR}}$)
14	N/A	N/A	N/A	N/A	N/A	N/A
15	15	VSS	VSS	VSS	GND_DIG	VSS
16	16	VDD	VDD	VDD	+3.3V_DIG	VDD
17	N/A	N/A	N/A	N/A	N/A	N/A
18	50	FLT15	FAULT_MC	Motor Fault	FAULT	Motor Fault
19	42	FLT6	N/A	N/A	PFC_FAULT	PFC Fault
20	23	AN1/RPA1	PIM_V_M3	Phase M3 Voltage Feedback Signal	PIM_IND _X /POT/ V_M3	QE1 - IND _X /Potentiometer Signal/Phase M3 Voltage Feedback Signal

TABLE 1: PIN MAP (CONTINUED)

PIM Pin Number	PIC32MK MCM		dsPICDEM MCLV2 Board 100-pin PIM Header		dsPICDEM MCHV2/MCHV3 Board 100-pin PIM Header	
	Pin Number	Pin Name	Pin Name	Pin Functionality	Pin Name	Pin Functionality
21	26	AN4/RPB2	PIM_V_M2	Phase M2 Voltage Feedback Signal	PIM_QEB/IB/V_M2	QE1 - B/ Phase B Current Signal/ Phase M2 Voltage Feedback Signal
22	34	AN8/RPC2	PIM_V_M1	Phase M1 Voltage Feedback Signal	PIM_QEA/IA/V_M1	QE1 - A/ Phase A Current Signal/ Phase M1 Voltage Feedback Signal
23	72	AN25	PIM_IMOTOR_SUM	DC Bus Current Signal	PIM_IBUS/VBUS	DC Bus Voltage Signal
24	21	AN9	PIM_IMOTOR2	Phase B Current Signal	PIM_IB/POT	AC Input Zero Cross/AC Input Voltage (downscaled)/ Potentiometer Signal
25	51	AN24	PIM_IMOTOR1	Phase A Current Signal	PIM_IA/IPFC	PFC Current signal
26	70	PGEC2	PGC	Device Programming Clock Line	PGD	Device Programming Clock Line
27	69	PGED2	PGD	Device Programming Clock Line	PGC	Device Programming Clock Line
28	N/A	N/A	VREF	AVDD/2	AVDD/2	AVDD/2
29	11	AN18	PIM_REC_NEUTR	Recreated Motor Neutral Voltage	PIM_REC_NEUTR	Recreated Motor Neutral Voltage
30	30	AVDD	AVDD	AVDD	AVDD	AVDD
31	31	AVSS	AVSS	AVSS	AVSS	AVSS
32	44	AN15	PIM_POT	Potentiometer Signal	PIM_POT	Potentiometer Signal
33	35	AN11	N/A	N/A	PIM_POT	Potentiometer Signal
34	38	RG11	PIM_GEN2	General I/O	PIM_GEN2	General I/O
35	20	AN10	PIM_VBUS	DC Bus Voltage Signal	PIM_DC_BUS	DC Bus Voltage Signal

TABLE 1: PIN MAP (CONTINUED)

PIM Pin Number	PIC32MK MCM		dsPICDEM MCLV2 Board 100-pin PIM Header		dsPICDEM MCHV2/MCHV3 Board 100-pin PIM Header	
	Pin Number	Pin Name	Pin Name	Pin Functionality	Pin Name	Pin Functionality
36	36	VSS	VSS	VSS	GND_DIG	VSS
37	37	VDD	VDD	VDD	+3.3V_DIG	VDD
38	39	RF13	N/A	N/A	PIM_VAC_VOL2	AC Input Voltage Signal (unbuffered)
39	40	RF12	N/A	N/A	PIM_IPFC_C_SHUNT	PFC Shunt Signal
40	41	RE12	N/A	N/A	PIM_PFC_L	PFC Shunt Signal
41	14	RPG9/AN16	PIM_MONITOR_1	Hall sensor A/Phase A Current signal/Phase M1 Voltage feedback signal	PIM_V_M1/POT	Hall sensor A/QEI - A/Phase A Current signal/Phase M1 Voltage feedback signal
42	12	RPG8/AN17	PIM_MONITOR_2	Hall sensor B/Phase B Current signal/Phase M2 Voltage feedback signal	PIM_V_M2	Hall sensor B/QEI - B/Phase B Current signal/Phase M2 Voltage feedback signal
43	53	RPE1/AN41	PIM_MONITOR_3	Hall sensor C/DC Bus Current signal/Phase M3 Voltage feedback signal	PIM_V_M3/IBUS	Hall sensor C/QEI - INDX/DC Bus Current signal/Phase M3 Voltage feedback signal/ Potentiometer Signal
44	47	RD14	N/A	N/A	N/A	N/A
45	45	VSS	VSS	VSS	GND_DIG	VSS
46	46	VDD	VDD	VDD	+3.3V_DIG	VDD
47	43	RPE14	HALLB	Hall Sensor B/QEI - B Input	HALLB/QEB	Hall sensor B/QEI - B

TABLE 1: PIN MAP (CONTINUED)

PIM Pin Number	PIC32MK MCM		dsPICDEM MCLV2 Board 100-pin PIM Header		dsPICDEM MCHV2/MCHV3 Board 100-pin PIM Header	
	Pin Number	Pin Name	Pin Name	Pin Functionality	Pin Name	Pin Functionality
48	66	RPA14	HALLC	Hall Sensor C/QEI - INDX Input	HALLC/INDX	Hall sensor C/QEI - INDX
49	81	RPC8	RX	UART Rx	RX	UART Rx
50	76	RPB9	TX	UART Tx	TX	UART Tx
51	3	RPA7	USB_TX	USB - UART Bridge Tx	N/A	N/A
52	67	RPA15	USB_RX	USB - UART Bridge Rx	N/A	N/A
53	58	VBUS2	N/A	N/A	N/A	N/A
54	59	D2-	N/A	N/A	N/A	N/A
55	60	D2+	N/A	N/A	N/A	N/A
56	77	USBID2	N/A	N/A	N/A	N/A
57	71	DAC2	N/A	N/A	N/A	N/A
58	80	RD13	PIM_FLT_OUT2	General I/O	PIM_FLT_OUT2	General I/O
59	91	RF6	PIM_FLT_OUT1	General I/O	PIM_FLT_OUT1	General I/O
60	61	RF5	DBG_LED1	Debug LED 1	DBG_LED2	Debug LED2
61	10	RPG6	HOME	Quadrature Encoder Home Input	HOME	Quadrature Encoder Home Input
62	62	VDD	VDD	VDD	+3.3V_DIG	VDD
63	63	CLKI	OSCI/CLKI	Oscillator Clock In	OSCI	Oscillator Clock In
64	64	CLKO	OSCO/CLKO	Oscillator Clock Out	OSCO	Oscillator Clock Out
65	65	VSS	VSS	VSS	GND_DIG	VSS
66	N/A	N/A	PIM_IBUS+	DC Bus current shunt signal (+)	PIM_IBUS+	DC Bus Current Shunt Signal (+)
67	N/A	N/A	PIM_IBUS-	DC Bus current shunt signal (-)	PIM_IBUS-	DC Bus Current Shunt Signal (-)
68	68	RD8	LIN_CS	LIN Chip Select Signal	BTN	Push Button Switch
69	79	RD12	LIN_FAULT	LIN Fault Signal	N/A	N/A

TABLE 1: PIN MAP (CONTINUED)

PIM Pin Number	PIC32MK MCM		dsPICDEM MCLV2 Board 100-pin PIM Header		dsPICDEM MCHV2/MCHV3 Board 100-pin PIM Header	
	Pin Number	Pin Name	Pin Name	Pin Functionality	Pin Name	Pin Functionality
70	81	RPC8	RX	UART Rx	RX	UART Rx
71	7	PWM5H	N/A	N/A	PIM_PFC_PWM	PFC PWM
72	67	RPA15	USB_RX	USB - UART Bridge Rx	N/A	N/A
73	N/A	N/A	PIM_IB+	Phase B current shunt signal (+)	PIM_IB+	Phase B current shunt signal (+)
74	N/A	N/A	PIM_IA+	Phase A current shunt signal (+)	PIM_IA+	Phase A current shunt signal (+)
75	75	VSS	VSS	VSS	GND_DIG	VSS
76	3	RPA7	USB_TX	USB - UART Bridge Tx	N/A	N/A
77	52	RPE0	CAN_TX	CAN Tx	N/A	N/A
78	87	RPF0	CAN_RX	CAN Rx	N/A	N/A
79	19	RE9	N/A	N/A	VACZX	AC Voltage Zero Crossing
80	84	RPC9	HALLA	Hall Sensor A/ QEI - A Input	HALLA/QEA	Hall Sensor A/ QEI - A Input
81	N/A	N/A	N/A	N/A	N/A	N/A
82	82	RD5	PIM_GEN1	General I/O	PIM_GEN1	General I/O
83	89	RG1	BTN_1	Push Button S2 Input	N/A	N/A
84	78	RC7	BTN_2	Push Button S3 Input	N/A	N/A
85	49	DAC3	N/A	N/A	N/A	N/A
86	86	VDD	VDD	VDD	+3.3V_DIG	VDD
87	87	RPF0	CAN_RX	CAN Rx	N/A	N/A
88	52	RPE0	CAN_TX	CAN Tx	N/A	N/A
89	88	RF1	N/A	N/A	N/A	N/A
90	90	RG0	N/A	N/A	N/A	N/A
91	73	SOSCI	N/A	N/A	N/A	N/A
92	74	SOSCO	N/A	N/A	N/A	N/A

TABLE 1: PIN MAP (CONTINUED)

PIM Pin Number	PIC32MK MCM		dsPICDEM MCLV2 Board 100-pin PIM Header		dsPICDEM MCHV2/MCHV3 Board 100-pin PIM Header	
	Pin Number	Pin Name	Pin Name	Pin Functionality	Pin Name	Pin Functionality
93	5	PWM1L	PWM1L1	Phase M1 Low-Side PWM	PWM1L1	Phase M1 Low-Side PWM
94	4	PWM1H	PWM1H1	Phase M1 High-Side PWM	PWM1H1	Phase M1 High-Side PWM
95	95	RG14	N/A	N/A	N/A	N/A
96	96	RG12	N/A	N/A	N/A	N/A
97	97	RG13	N/A	N/A	N/A	N/A
98	99	PWM2L	PWM1L2	Phase M2 Low-Side PWM	PWM1L2	Phase M2 Low-Side PWM
99	98	PWM2H	PWM1H2	Phase M2 High-Side PWM	PWM1H2	Phase M2 High-Side PWM
100	94	PWM3L	PWM1L3	Phase M3 Low-Side PWM	PWM1L3	Phase M3 Low-Side PWM

FIGURE 3: 100-PIN PIM HEADER SCHEMATIC

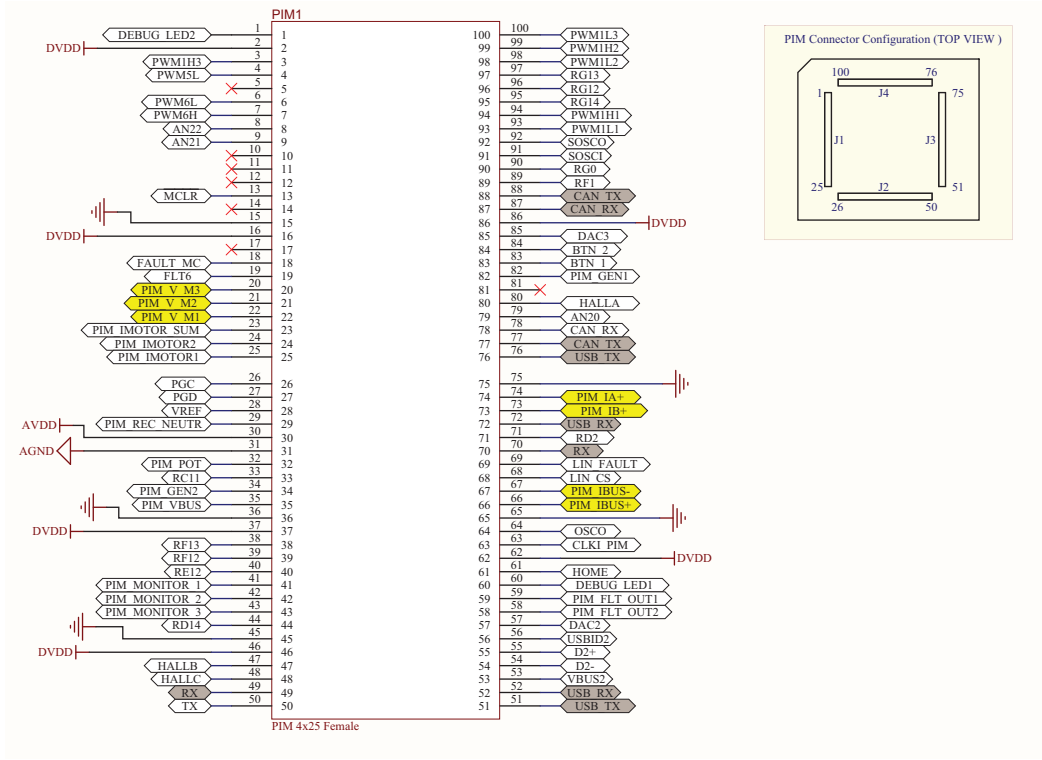
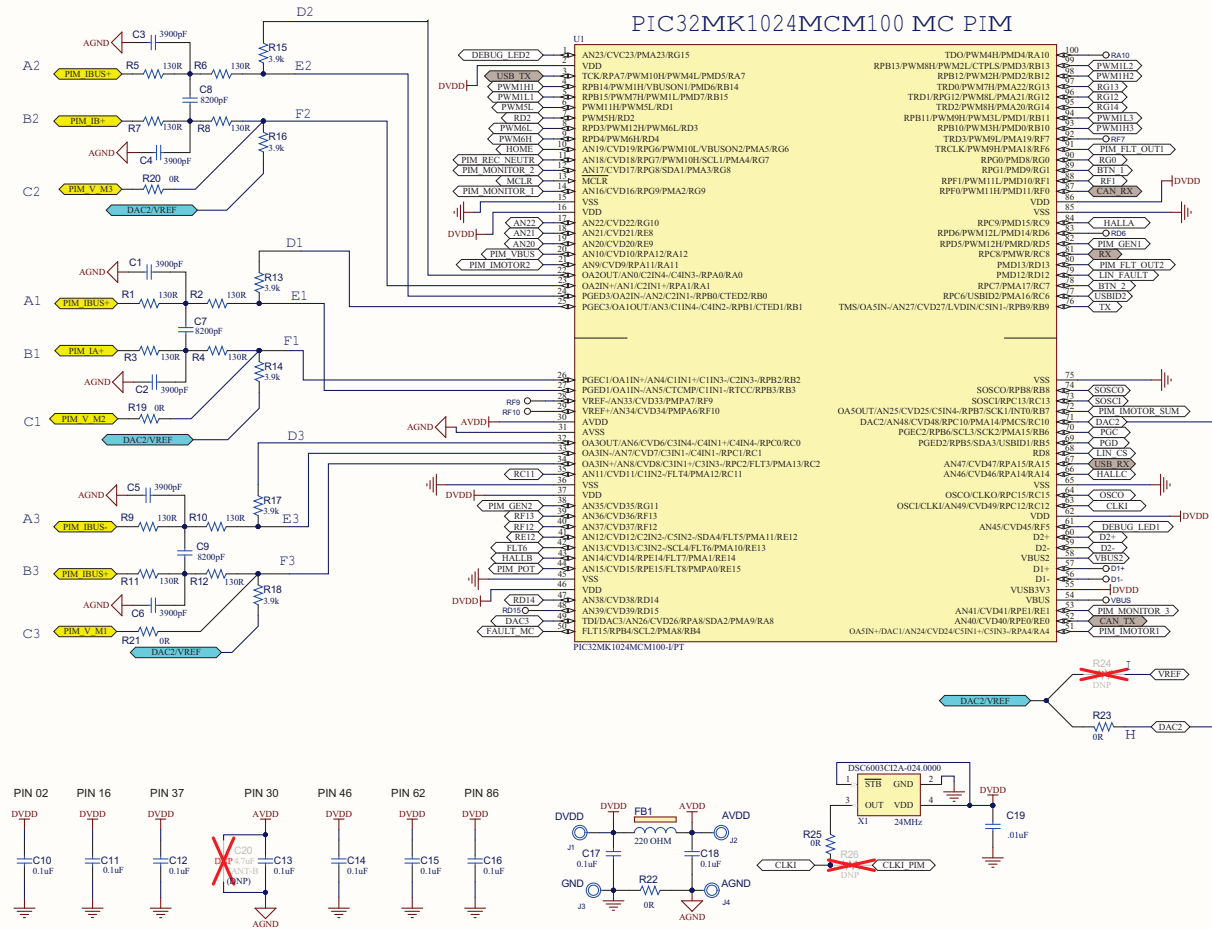


FIGURE 4: 100-PIN PIM DEVICE SCHEMATIC

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The reference voltage (VREF) biases the op amps to VDD/2, therefore the bidirectional motor phase current can be sensed using unipolar op amps. The source of VREF can be selected either from the development board or from the internally generated reference voltage using DAC2 and resistors R23/R24, as shown in [Figure 4](#). By default, the PIM is configured to source the reference voltage, internally generated using DAC2 by populating R23 and keeping R24 depopulated.

To source the reference voltage from Motor Control PIM, R23 needs to be depopulated and R24 must be populated with a zero ohm resistor.

The internal op amp configuration and passive resistor-capacitive network configures the filter bandwidth, op amp bias and op amp gain, as shown in [Figure 4](#).

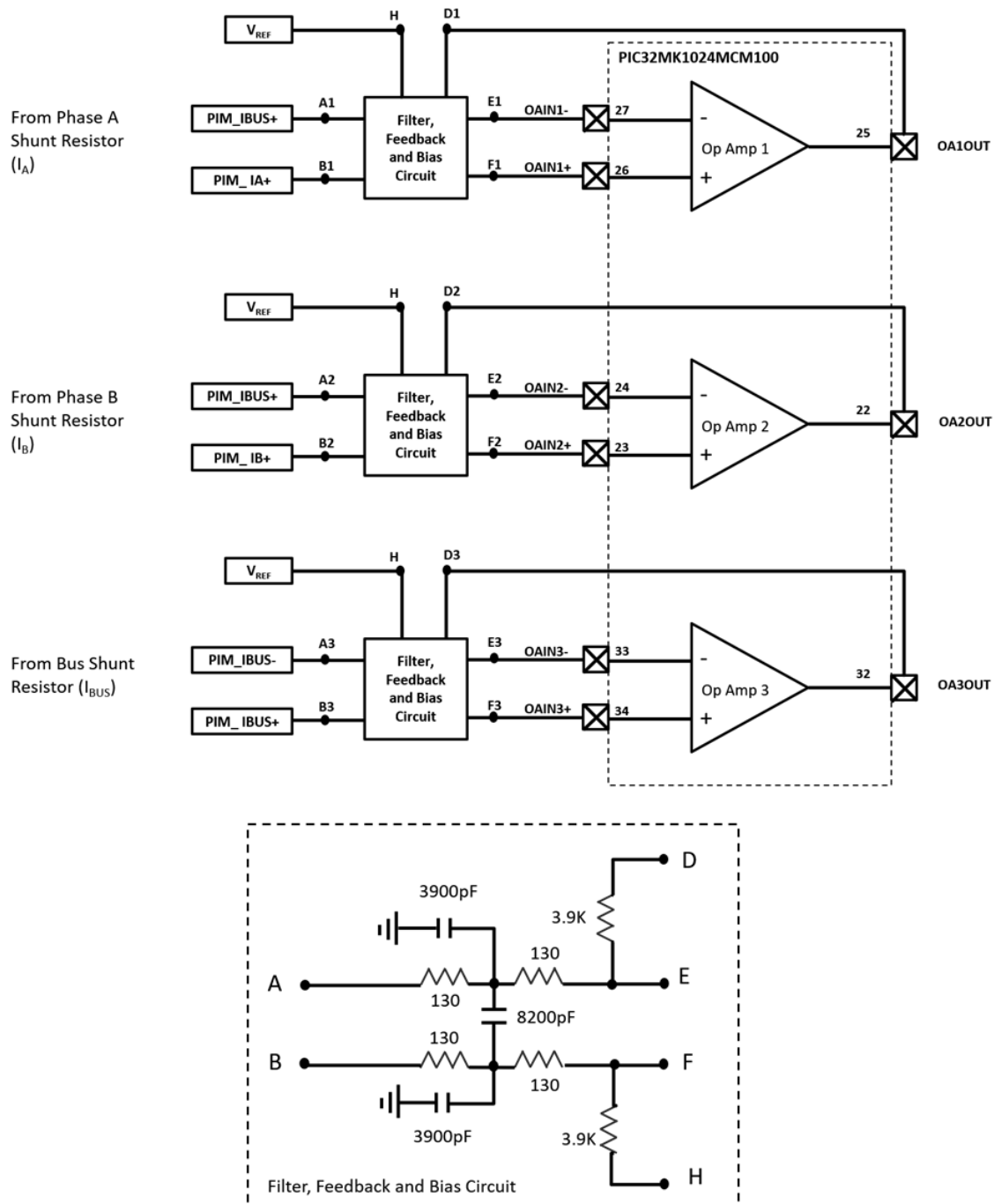
[Table 2](#) classifies the passive components according to their functionality and also specifies the design equations for filter bandwidth and op amp gain.

TABLE 2: ANALOG FUNCTIONALITY LISTING

Op Amp Number	Analog Function	Passive Components	Design Equations
1	Low-Pass Filter	R1, R2, R3, R4, C1, C2, C7	$R1 = R2 = R3 = R4 = R$ $C1 = C2 = C$
	Differential Amplifier Input	R1, R2, R3, R4	
	Differential Amplifier Feedback	R13	$Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} + C_7\right)}$ $Differential\ Amplifier\ Gain = \frac{R_{13}}{2R}$
2	Low-Pass Filter	R5, R6, R7, R8, C3, C4, C8	$R5 = R6 = R7 = R8 = R$ $C3 = C4 = C$
	Differential Amplifier Input	R5, R6, R7, R8	
	Differential Amplifier Feedback	R15	$Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} + C_8\right)}$ $Differential\ Amplifier\ Gain = \frac{R_{15}}{2R}$
3	Low-Pass Filter	R9, R10, R11, R12, C5, C6, C9	$R9 = R10 = R11 = R12 = R$ $C5 = C6 = C$
	Differential Amplifier Input	R9, R10, R11, R12	
	Differential Amplifier Feedback	R17	$Common\ mode\ f_{-3dB} \cong \frac{1}{2\pi RC}$ $Differential\ mode\ f_{-3dB} \cong \frac{1}{2\pi(2R)\left(\frac{C}{2} + C_9\right)}$ $Differential\ Amplifier\ Gain = \frac{R_{17}}{2R}$

Figure 5 illustrates a typical block diagram of the op amp circuit.

FIGURE 5: OP AMP CIRCUIT BLOCK DIAGRAM



$$\text{Differential Amplifier Gain} = \frac{3.9k\Omega}{2 * 130\Omega} = 15$$

$$\text{Differential mode } f_{-3dB} \cong \frac{1}{2\pi(2 * 130\Omega) \left(\frac{3900pF}{2} + 8200pF \right)} \cong 60.3kHz$$

$$\text{Common mode } f_{-3dB} \cong \frac{1}{2\pi(130\Omega)(3900pF)} \cong 313.9kHz$$

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