PIC32MK GENERAL PURPOSE AND MOTOR CONTROL (GP/MC) FAMILY

32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB Live-Update Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps

Operating Conditions: 2.2V to 3.6V

- -40ºC to +85ºC, DC to 120 MHz
- -40ºC to +125ºC, DC to 80 MHz

Core: 120 MHz (up to 198 DMIPS)

- MIPS32® microAptiv™ MCU core with Floating Point Unit
- microMIPS™ mode for up to 40% smaller code size
- DSP-enhanced core:
  - Four 64-bit accumulators
  - Single-cycle MAC, saturating and fractional math
- Code-efficient (C and Assembly) architecture
- Two 32-bit core register files to reduce interrupt latency

Clock Management

- 8 MHz ±5% (FRC) internal oscillator 0ºC to +70ºC
- Programmable PLLs and oscillator clock sources:
  - HS and EC clock modes
- Secondary USB PLL
- 32 kHz Internal Low-power RC oscillator (LPRC)
- Independent external low-power 32 kHz crystal oscillator
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timers (WDT) and Deadman Timer (DMT)
- Fast wake-up and start-up
- Four Fractional clock out (REFCLKO) modules

Power Management

- Low-power management modes (Deep Sleep, Sleep, and Idle)
- Integrated:
  - Power-on Reset (POR) and Brown-out Reset (BOR)
- On-board capacitorless regulator

Motor Control PWM

- Eight PWM pairs
- Six additional Single-Ended PWM modules
- Dead Time for rising and falling edges
- Dead-Time Compensation
- 8.33 ns PWM Resolution
- Clock Chopping for High-Frequency Operation
- PWM Support for:
  - DC/DC, AC/DC, inverters, PFC, lighting
  - BLDC, PMSM, ACIM, SRM motors
- Choice of six Fault and Current Limit Inputs
- Flexible Trigger Configuration for ADC Triggering

Motor Encoder Interface

- Six Quadrature Encoder Interface (QEI) modules:
  - Four inputs: Phase A, Phase B, Home, and Index

Audio/Graphics/Touch Interfaces

- External Graphics interfaces through PMP
- Up to six I^2S audio data communication interfaces
- Up to six SPI audio control interfaces
- Programmable audio master clock:
  - Generation of fractional clock frequencies
  - Can be synchronized with USB clock
  - Can be tuned in run-time

Unique Features

- Permanent non-volatile 4-word unique device serial number

Direct Memory Access (DMA)

- Up to eight channels with automatic data size detection
- Programmable Cyclic Redundancy Check (CRC)
- Up to 64 KB transfers

Security Features

- Advanced Memory Protection:
  - Peripheral and memory region access control

Advanced Analog Features

- 12-bit ADC module:
  - Sum of all individual ADC's combined, 25.45 Msps 12-bit mode or 33.79 Msps 8-bit mode
  - 7 individual ADC modules
  - 3.75 Msps per S&H with dedicated DMA
  - Up to 42 analog inputs
- Flexible and independent ADC trigger sources
- Four Op amps and five Comparators
- Up to three 12-bit CDACs
- Internal temperature sensor ±2ºC accuracy
- Capacitive Touch Divider (CVD)

Communication Interfaces

- Up to four CAN modules (with dedicated DMA channels):
  - 2.0B Active with DeviceNet™ addressing support
- Up to six UART modules (up to 25 Mbps):
  - Supports LIN 1.2 and IrDA® protocols
- Six SPI/I^2S modules (SPI 50 Mbps)
- Parallel Master Port (PMP)
- Up to two FS USB 2.0-compliant On-The-Go (OTG) controllers
- Peripheral Pin Select (PPS) to enable remappable pin functions

Timers/Output Compare/Input Capture/RTCC

- Up to 14 16-bit or one 16-bit and eight 32-bit timers/counters for GP and MC devices and six additional QEI 32-bit timers for MC devices
- 16 Output Compare (OC) modules
- 16 Input Capture (IC) modules
- PPS to enable function remap
- Real-Time Clock and Calendar (RTCC) module

Input/Output

- 5V-tolerant pins with up to 22 mA source/sink
- Selectable internal open drain, pull-ups, and pull-downs
- External interrupts on all I/O pins
- Five programmable edge/level-triggered interrupt pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1 -40ºC to +125ºC) (planned)
- Class B Safety Library, IEC 60730 (planned)
- Back-up internal oscillator
- Clock monitor with back-up internal oscillator
- Global register locking

Debugger Development Support

- In-circuit and in-application programming
- 2-wire or 4-wire MIPS® Enhanced JTAG interface
- Unlimited software and 12 complex breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Non-intrusive hardware-based instruction trace

Software and Tools Support

- C/C++ compiler with native DSP/fractional support
- MPLAB® Harmony Integrated Software Framework
- TCP/IP, USB, Graphics, and mTouch™ middleware
- MFi, Android™ and Bluetooth® audio frameworks
- RTOS Kernels: Express Logic ThreadX, FreeRTOS™, OPENRTOS®, Micriμm® μC/OS™, and SEGGER embOS®

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Packages

Type	VQFN	TQFP	
Pin Count	64	64	100
I/O Pins (up to)	48 (GP devices) 49 (MC devices)	48 (GP devices) 49 (MC devices)	77 (GP devices) 78 (MC devices)
Contact/Lead Pitch	0.50 mm	0.50 mm	0.40 mm
Dimensions	9x9x0.9 mm	10x10x1 mm	12x12x1 mm

TABLE 1: PIC32MK GENERAL PURPOSE (GP) FAMILY FEATURES

Device	Program Memory (KB)	Data Memory (KB)	EE Memory (KB)	Floating Point Unit (FPU)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals						DMA Channels (Programmable/Dedicated)	ADC (Channels)	Op amp/Comparator	USB 2.0 FS OTG	PMP	RTCC	REFCLK	CDAC	CTMU	I/O Pins	JTAG/ICSP	Trace
								Remappable Pins	Timers/Capture/Compare(1)	UART	SPI/I²S	External Interrupts(2)	CAN 2.0B												
PIC32MK0512GPD064	512	128	4	Y	64	TQFP, VQFN	16	Y	9/16/16	6	6	5	—	8/13	26	4/5	1	Y	1	4	3	1	48	Y	Y
PIC32MK1024GPD064	1024	256																							
PIC32MK0512GPD100	512	128	4	Y	100	TQFP	16	Y	9/16/16	6	6	5	—	8/13	42	4/5	2	Y	1	4	3	1	77	Y	Y
PIC32MK1024GPD100	1024	256																							
PIC32MK0512GPE064	512	128	4	Y	64	TQFP, VQFN	16	Y	9/16/16	6	6	5	4	8/13	26	4/5	1	Y	1	4	3	1	48	Y	Y
PIC32MK1024GPE064	1024	256																							
PIC32MK0512GPE100	512	128	4	Y	100	TQFP	16	Y	9/16/16	6	6	5	4	8/13	42	4/5	2	Y	1	4	3	1	77	Y	Y
PIC32MK1024GPE100	1024	256																							

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.
Legend: An '—' indicates this feature is not available for the listed device.

TABLE 2: PIC32MK MOTOR CONTROL (MC) FAMILY FEATURES

Device	Program Memory (KB)	Data Memory (KB)	EE Memory (KB)	Floating Point Unit (FPU)	Pins	Packages	Boot Flash Memory (KB)	Remappable Peripherals						DMA Channels (Programmable/Dedicated)	ADC (Channels)	Op amp/Comparator	USB 2.0 FS OTG	PMP	QEI	MCPWM	RTCC	REFCLK	CDAC	CTMU	I/O Pins	JTAG/ICSP	Trace
								Remappable Pins	Timers/Capture/Compare(1)	UART	SPI/I²S	External Interrupts(2)	CAN 2.0B														
PIC32MK0512MCF064	512	128	4	Y	64	TQFP, VQFN	16	Y	9/16/16	6	6	5	4	8/13	26	4/5	1	Y	6	12	1	4	3	1	49	Y	Y
PIC32MK1024MCF064	1024	256																									
PIC32MK0512MCF100	512	128	4	Y	100	TQFP	16	Y	9/16/16	6	6	5	4	8/13	42	4/5	2	Y	6	12	1	4	3	1	78	Y	Y
PIC32MK1024MCF100	1024	256																									

Note 1: Eight out of nine timers are remappable.
2: Four out of five external interrupts are remappable.

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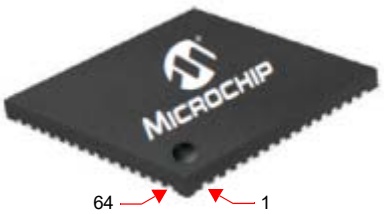
Device Pin Tables

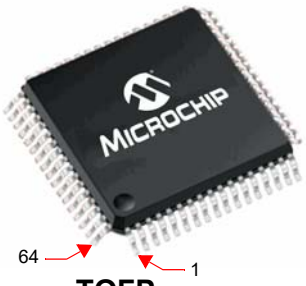
TABLE 3: PIN NAMES FOR 64-PIN GENERAL PURPOSE (GPD/GPE) DEVICES

64-PIN VQFN(4) AND TQFP (TOP VIEW)

PIC32MK0512GPD064
PIC32MK0512GPE064
PIC32MK1024GPD064
PIC32MK1024GPE064



VQFN(4)



TQFP

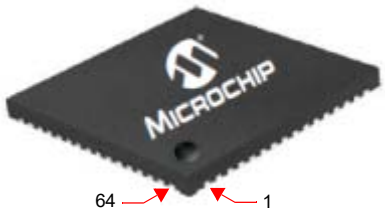
Pin #	Full Pin Name	Pin #	Full Pin Name
1	TCK/RPA7/PMD5/RA7	33	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
2	RPB14/VBUSON1/PMD6/RB14	34	VBUS
3	RPB15/PMD7/RB15	35	VUSB3V3
4	AN19/CVD19/RPG6/PMA5/RG6	36	D-
5	AN18/CVD18/RPG7/PMA4/RG7(6)	37	D+
6	AN17/CVD17/RPG8/PMA3/RG8(7)	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/AN49/CVD49/RPC12/RC12
8	AN16/CVD16/RPG9/PMA2/RG9	40	OSCO/CLKO/RPC15/RC15
9	VSS	41	VSS
10	VDD	42	VBAT
11	AN10/CVD10/RPA12/RA12	43	PGD2/RPB5/USBID1/RB5(7)
12	AN9/CVD9/RPA11/RA11	44	PGC2/RPB6/SCK2/PMA15/RB6(6)
13	OA2OUT/ANO/C2IN4-/C4IN3-/RPA0/RA0	45	DAC2/AN48/CVD48/RPC10/PMA14/PMCS/RC10
14	OA2IN+/AN1/C2IN1+/RPA1/RA1	46	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7
15	PGD3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	47	SOSCI/RPC13(5)/RC13(5)
16	PGC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/RPB1/CTED1/PMA6/RB1	48	SOSCO/RPB8(5)/RB8(5)
17	PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	49	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9
18	PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	50	TRCLK/RPC6/RC6
19	AVDD	51	TRD0/RPC7/RC7
20	AVSS	52	TRD1/RPC8/PMWR/RC8
21	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	53	TRD2/RPD5/PMRD/RD5
22	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/PMA7/RC1	54	TRD3/RPD6/RD6
23	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/PMA13/RC2	55	RPC9/RC9
24	AN11/CVD11/C1IN2-/PMA12/RC11	56	VSS
25	VSS	57	VDD
26	VDD	58	RPF0/RF0
27	AN12/CVD12/C2IN2-/C5IN2-/PMA11/RE12(7)	59	RPF1/RF1
28	AN13/CVD13/C3IN2-/PMA10/RE13(6)	60	RPB10/PMD0/RB10
29	AN14/CVD14/RPE14/PMA1/RE14	61	RPB11/PMD1/RB11
30	AN15/CVD15/RPE15/PMA0/RE15	62	RPB12/PMD2/RB12
31	TDI/DAC3/AN26/CVD26/RPA8/PMA9/RA8(7)	63	RPB13/CTPLS/PMD3/RB13
32	RPB4/PMA8/RB4(6)	64	TDO/PMD4/RA10

Note
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
5: Functions are restricted to input functions only and inputs will be slower than the standard inputs.
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock, that is SCL.
7: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, that is, SDA.
8: VBAT functionality is compromised. For additional information, refer to specific errata documents. This pin must be connected to VDD.

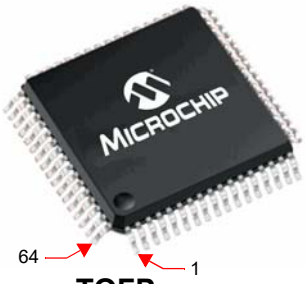
TABLE 4: PIN NAMES FOR 64-PIN MOTOR CONTROL (MCF) DEVICES

64-PIN VQFN(4) AND TQFP (TOP VIEW)

PIC32MK0512MCF064
PIC32MK1024MCF064



VQFN(4)



TQFP

Pin #	Full Pin Name	Pin #	Full Pin Name
1	TCK/RPA7/PWM10H/PWM4L/PMD5/RA7	33	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
2	RPB14/PWM1H/VBUSON1/PMD6/RB14	34	VBUS
3	RPB15/PWM7H/PWM1L/PMD7/RB15	35	VUSB3V3
4	AN19/CVD19/RPG6/PMA5/RG6	36	D-
5	AN18/CVD18/RPG7/PMA4/RG7(6)	37	D+
6	AN17/CVD17/RPG8/PMA3/RG8(7)	38	VDD
7	$\overline{\text{MCLR}}$	39	OSCI/CLKI/AN49/CVD49/RPC12/RC12
8	AN16/CVD16/RPG9/PMA2/RG9	40	OSCO/CLKO/RPC15/RC15
9	VSS	41	VSS
10	VDD	42	RD8
11	AN10/CVD10/RPA12/RA12	43	PGD2/RPB5/USBID1/RB5(7)
12	AN9/CVD9/RPA11/USBOEN1/RA11	44	PGC2/RPB6/SCK2/PMA15/RB6(6)
13	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	45	DAC2/AN48/CVD48/RPC10/PMA14/PMCS/RC10
14	OA2IN+/AN1/C2IN1+/RPA1/RA1	46	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7
15	PGD3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	47	SOSCI/RPC13(5)/RC13(5)
16	PGC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/RPB1/CTED1/PMA6/RB1	48	SOSCO/RPB8(5)/RB8(5)
17	PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	49	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9
18	PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	50	TRCLK/RPC6/PWM6H/RC6
19	AVDD	51	TRD0/RPC7/PWM12H/PWM6L/RC7
20	AVSS	52	TRD1/RPC8/PWM5H/PMWR/RC8
21	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	53	TRD2/RPD5/PWM12H/PMRD/RD5
22	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/PMA7/RC1	54	TRD3/RPD6/PWM12L/RD6
23	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMA13/RC2	55	RPC9/PWM11H/PWM5L/RC9
24	AN11/CVD11/C1IN2-/FLT4/PMA12/RC11	56	VSS
25	VSS	57	VDD
26	VDD	58	RPF0/PWM11H/RF0
27	AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMA11/RE12(7)	59	RPF1/PWM11L/RF1
28	AN13/CVD13/C3IN2-/FLT6/PMA10/RE13(6)	60	RPB10/PWM3H/PMD0/RB10
29	AN14/CVD14/RPE14/FLT7/PMA1/RE14	61	RPB11/PWM9H/PWM3L/PMD1/RB11
30	AN15/CVD15/RPE15/FLT8/PMA0/RE15	62	RPB12/PWM2H/PMD2/RB12
31	TDI/DAC3/AN26/CVD26/RPA8/PMA9/RA8(7)	63	RPB13/PWM8H/PWM2L/CTPLS/PMD3/RB13
32	FLT15/RPB4/PMA8/RB4(6)	64	TDO/PWM4H/PMD4/RA10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
5: Functions are restricted to input functions only and inputs will be slower than standard inputs.
6: The I^2C Library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock, that is, SCL.
7: The I^2C Library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, that is, SDA.

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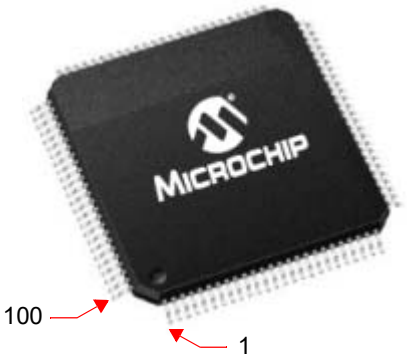
TABLE 5: PIN NAMES FOR 100-PIN GENERAL PURPOSE (GPD/GPE) DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MK0512GPD100
PIC32MK0512GPE100
PIC32MK1024GPD100
PIC32MK1024GPE100



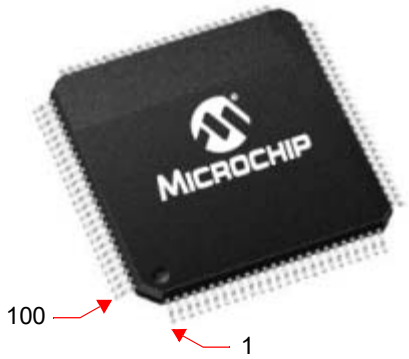
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/CVD23/PMA23/RG15	36	VSS
2	VDD	37	VDD
3	TCK/RPA7/PMD5/RA7	38	AN35/CVD35/RG11
4	RPB14/VBUSON1/PMD6/RB14	39	AN36/CVD36/RF13
5	RPB15/PMD7/RB15	40	AN37/CVD37/RF12
6	RD1	41	AN12/CVD12/C2IN2-/C5IN2-/SDA4/PMA11/RE12(6)
7	RD2	42	AN13/CVD13/C3IN2-/SCL4/PMA10/RE13(5)
8	RPD3/RD3	43	AN14/CVD14/RPE14/PMA1/RE14
9	RPD4/RD4	44	AN15/CVD15/RPE15/PMA0/RE15
10	AN19/CVD19/RPG6/VBUSON2/PMA5/RG6	45	VSS
11	AN18/CVD18/RPG7/SCL1/PMA4/RG7(5)	46	VDD
12	AN17/CVD17/RPG8/SDA1/PMA3/RG8(6)	47	AN38/CVD38/RD14
13	$\overline{\text{MCLR}}$	48	AN39/CVD39/RD15
14	AN16/CVD16/RPG9/PMA2/RG9	49	TDI/DAC3/AN26/CVD26/RPA8/SDA2/PMA9/RA8(6)
15	VSS	50	RPB4/SCL2/PMA8/RB4(5)
16	VDD	51	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
17	AN22/CVD22/RG10	52	AN40/CVD40/RPE0/RE0
18	AN21/CVD21/RE8	53	AN41/CVD41/RPE1/RE1
19	AN20/CVD20/RE9	54	VBUS1
20	AN10/CVD10/RPA12/RA12	55	VUSB3V3
21	AN9/CVD9/RPA11/RA11	56	D1-
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	57	D1+
23	OA2IN+/AN1/C2IN1+/RPA1/RA1	58	VBUS2
24	PGD3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	59	D2-
25	PGC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1	60	D2+
26	PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	61	AN45/CVD45/RF5
27	PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	62	VDD
28	VREF-/AN33/CVD33/PMA7/RF9	63	OSCI/CLKI/AN49/CVD49/RPC12/RC12
29	VREF+/AN34/CVD34/PMA6/RF10	64	OSCO/CLKO/RPC15/RC15
30	AVDD	65	VSS
31	AVSS	66	AN46/CVD46/RPA14/RA14
32	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	67	AN47/CVD47/RPA15/RA15
33	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/RC1	68	VBAT
34	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/PMA13/RC2	69	PGD2/RPB5/SDA3/USBID1/RB5(6)
35	AN11/CVD11/C1IN2-/PMA12/RC11	70	PGC2/RPB6/SCL3/SCK2/PMA15/RB6(5)

Note
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock, that is, SCL.
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, that is, SDA.
7: V_{BAT} functionality is compromised. For additional information, refer to specific errata documents. This pin must be connected to V_{DD}.

TABLE 5: PIN NAMES FOR 100-PIN GENERAL PURPOSE (GPD/GPE) DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MK0512GPD100
PIC32MK0512GPE100
PIC32MK1024GPD100
PIC32MK1024GPE100



Pin #	Full Pin Name
71	DAC2/AN48/CVD48/RPC10/PMA14/PMCS/RC10
72	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7
73	SOSCI/RPC13(4)/RC13(4)
74	SOSCO/RPB8(4)/RB8(4)
75	VSS
76	TMS/OA5IN-/AN27/CVD27/LVDIN/C5IN1-/RPB9/RB9
77	RPC6/USBID2/PMA16/RC6
78	RPC7/PMA17/RC7
79	PMD12/RD12
80	PMD13/RD13
81	RPC8/PMWR/RC8
82	RPD5/PMRD/RD5
83	RPD6/PMD14/RD6
84	RPC9/PMD15/RC9
85	VSS

Pin #	Full Pin Name
86	VDD
87	RPF0/PMD11/RF0
88	RPF1/PMD10/RF1
89	RPG1/PMD9/RG1
90	RPG0/PMD8/RG0
91	TRCLK/PMA18/RF6
92	TRD3/PMA19/RF7
93	RPB10/PMD0/RB10
94	RPB11/PMD1/RB11
95	TRD2/PMA20/RG14
96	TRD1/RPG12/PMA21/RG12
97	TRD0/PMA22/RG13
98	RPB12/PMD2/RB12
99	RPB13/CTPLS/PMD3/RB13
100	TDO/PMD4/RA10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock, that is, SCL.
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, that is, SDA.
7: V_{BAT} functionality is compromised. For additional information, refer to specific errata documents. This pin must be connected to V_{DD}.

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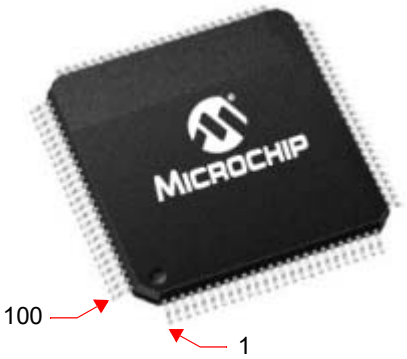
TABLE 6: PIN NAMES FOR 100-PIN MOTOR CONTROL (MCF) DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MK0512MCF100
PIC32MK1024MCF100



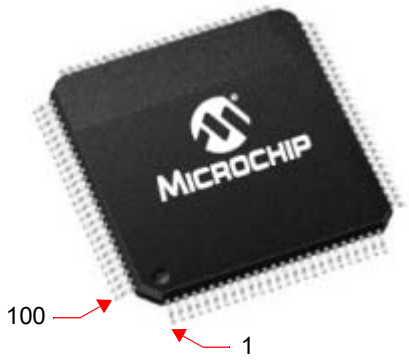
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/CVD23/PMA23/RG15	36	VSS
2	VDD	37	VDD
3	TCK/RPA7/PWMH10/PWML4/PMD5/RA7	38	AN35/CVD35/RG11
4	RPB14/PWMH1/VBUSON1/PMD6/RB14	39	AN36/CVD36/RF13
5	RPB15/PWMH7/PWML1/PMD7/RB15	40	AN37/CVD37/RF12
6	PWMH11/PWML5/RD1	41	AN12/CVD12/C2IN2-/C5IN2-/SDA4/FLT5/PMA11/RE12(6)
7	PWMH5/RD2	42	AN13/CVD13/C3IN2-/SCL4/FLT6/PMA10/RE13(5)
8	RPD3/PWMH12/PWML6/RD3	43	AN14/CVD14/RPE14/FLT7/PMA1/RE14
9	RPD4/PWMH6/RD4	44	AN15/CVD15/RPE15/FLT8/PMA0/RE15
10	AN19/CVD19/RPG6/VBUSON2/PMA5/RG6	45	VSS
11	AN18/CVD18/RPG7/SCL1/PMA4/RG7(5)	46	VDD
12	AN17/CVD17/RPG8/SDA1/PMA3/RG8(6)	47	AN38/CVD38/RD14
13	$\overline{\text{MCLR}}$	48	AN39/CVD39/RD15
14	AN16/CVD16/RPG9/PMA2/RG9	49	TDI/DAC3/AN26/CVD26/RPA8/SDA2/PMA9/RA8(6)
15	VSS	50	FLT15/RPB4/SCL2/PMA8/RB4(5)
16	VDD	51	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/RA4
17	AN22/CVD22/RG10	52	AN40/CVD40/RPE0/RE0
18	AN21/CVD21/RE8	53	AN41/CVD41/RPE1/RE1
19	AN20/CVD20/RE9	54	VBUS1
20	AN10/CVD10/RPA12/RA12	55	VUSB3V3
21	AN9/CVD9/RPA11/RA11	56	D1-
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	57	D1+
23	OA2IN+/AN1/C2IN1+/RPA1/RA1	58	VBUS2
24	PGD3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	59	D2-
25	PGC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1	60	D2+
26	PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	61	AN45/CVD45/RF5
27	PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	62	VDD
28	VREF-/AN33/CVD33/PMA7/RF9	63	OSCI/CLKI/AN49/CVD49/RPC12/RC12
29	VREF+/AN34/CVD34/PMA6/RF10	64	OSCO/CLKO/RPC15/RC15
30	AVDD	65	VSS
31	AVSS	66	AN46/CVD46/RPA14/RA14
32	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	67	AN47/CVD47/RPA15/RA15
33	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/RC1	68	RD8
34	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMA13/RC2	69	PGD2/RPB5/SDA3/USBID1/RB5(6)
35	AN11/CVD11/C1IN2-/FLT4/PMA12/RC11	70	PGC2/RPB6/SCL3/SCK2/PMA15/RB6(5)

Note
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).

TABLE 6: PIN NAMES FOR 100-PIN MOTOR CONTROL (MCF) DEVICES (CONTINUED)

100-PIN TQFP (TOP VIEW)

PIC32MK0512MCF100
PIC32MK1024MCF100



Pin #	Full Pin Name	Pin #	Full Pin Name
71	DAC2/AN48/CVD48/RPC10/PMA14/PMCS/RC10	86	VDD
72	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/INT0/RB7	87	RPF0/PWMH11/PMD11/RF0
73	SOSCI/RPC13(4)/RC13(4)	88	RPF1/PWML11/PMD10/RF1
74	SOSCO/RPB8(4)/RB8(4)	89	RPG1/PMD9/RG1
75	VSS	90	RPG0/PMD8/RG0
76	TMS/OA5IN-/AN27/CVD27/LVDIN/C5IN1-/RPB9/RB9	91	TRCLK/PMA18/RF6
77	RPC6/USBID2/PMA16/RC6	92	TRD3/PMA19/RF7
78	RPC7/PMA17/RC7	93	RPB10/PWMH3/PMD0/RB10
79	PMD12/RD12	94	RPB11/PWMH9/PWML3/PMD1/RB11
80	PMD13/RD13	95	TRD2/PMA20/RG14
81	RPC8/PMWR/RC8	96	TRD1/RPG12/PMA21/RG12
82	RPD5/PWMH12/PMRD/RD5	97	TRD0/PMA22/RG13
83	RPD6/PWML12/PMD14/RD6	98	RPB12/PWMH2/PMD2/RB12
84	RPC9/PMD15/RC9	99	RPB13/PWMH8/PWML2/CTPLS/PMD3/RB13
85	VSS	100	TDO/PWMH4/PMD4/RA10

Note
1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **13.3 "Peripheral Pin Select (PPS)"** for restrictions.
2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **13.0 "I/O Ports"** for more information.
3: Shaded pins are 5V tolerant.
4: Functions are restricted to input functions only and inputs will be slower than standard inputs.
5: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C master/slave clock. (i.e., SCL).
6: The I^2C library is available in MPLAB Harmony. For future hardware or silicon compatibility, it is recommended to use these pins for the I^2C data I/O, (i.e., SDA).

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 web site: http://www.microchip.com/pic32.

- **Section 1. "Introduction"** (DS60001127)
- **Section 4. "Prefetch Cache Module"** (DS60001119)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)
- **Section 39. "Op amp/Comparator"** (DS60001178)
- **Section 42. "Oscillators with Enhanced PLL"** (DS60001250)
- **Section 43. "Quadrature Encoder Interface (QEI)"** (DS60001346)
- **Section 44. "Motor Control PWM (MCPWM)** (DS60001393)
- **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193)
- **Section 58. "Data EEPROM"** (DS60001341)

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NOTES:

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1.0 DEVICE OVERVIEW

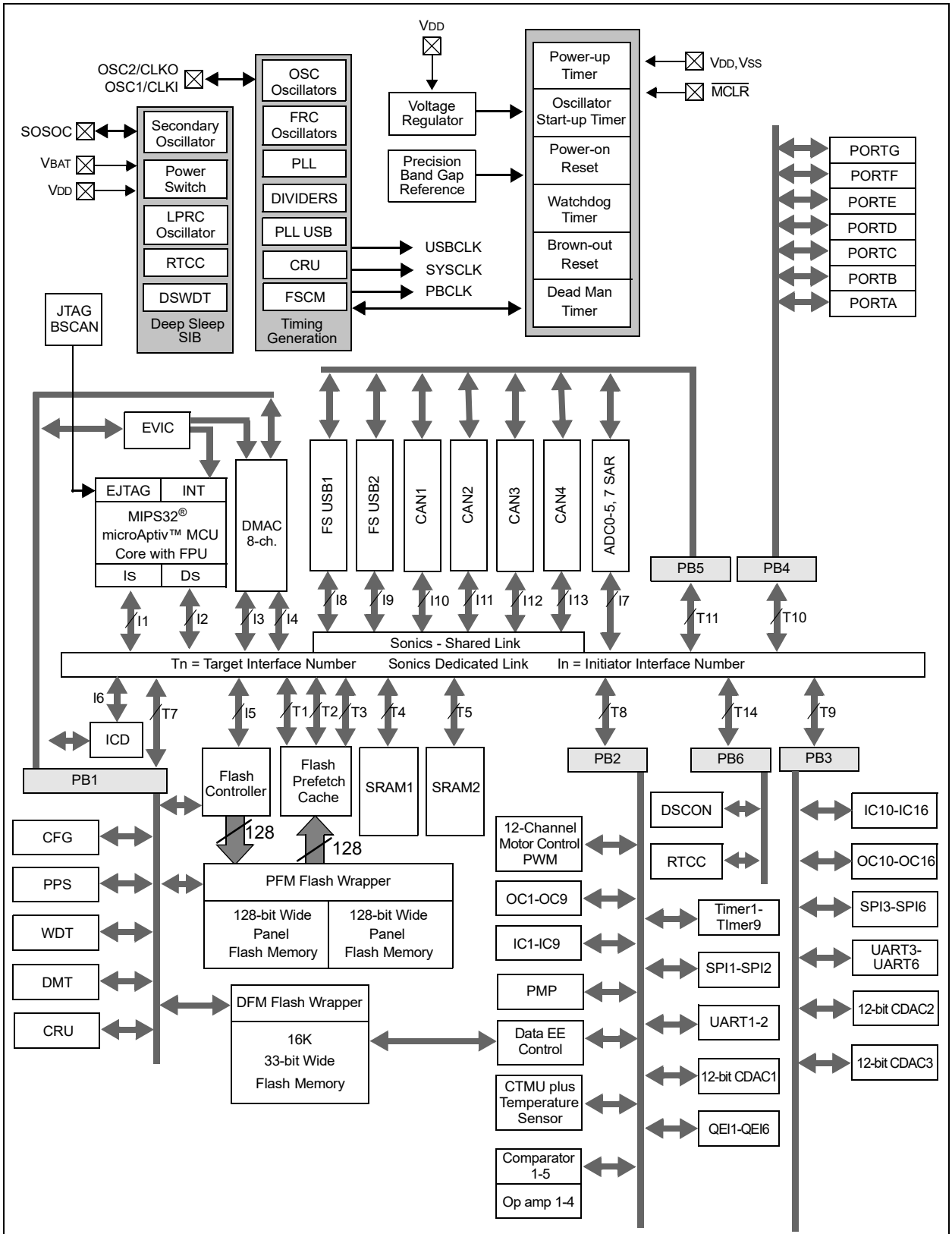
Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This data sheet contains device-specific information for PIC32MK GP/MC devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MK GP/MC family of devices.

Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 3 and Table 5).

FIGURE 1-1: PIC32MK GP/MC FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to the family feature tables (Table 1 and Table 2) for the list of available features by device.

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TABLE 1-1: ADC ANALOG PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
AN0	22	13	I	Analog	Analog Input Channels
AN1	23	14	I	Analog	
AN2	24	15	I	Analog	
AN3	25	16	I	Analog	
AN4	26	17	I	Analog	
AN5	27	18	I	Analog	
AN6	32	21	I	Analog	
AN7	33	22	I	Analog	
AN8	34	23	I	Analog	
AN9	21	12	I	Analog	
AN10	20	11	I	Analog	
AN11	35	24	I	Analog	
AN12	41	27	I	Analog	
AN13	42	28	I	Analog	
AN14	43	29	I	Analog	
AN15	44	30	I	Analog	
AN16	14	8	I	Analog	
AN17	12	6	I	Analog	
AN18	11	5	I	Analog	
AN19	10	4	I	Analog	
AN20	19	—	I	Analog	
AN21	18	—	I	Analog	
AN22	17	—	I	Analog	
AN23	1	—	I	Analog	
AN24	51	33	I	Analog	
AN25	72	46	I	Analog	
AN26	49	31	I	Analog	
AN27	76	49	I	Analog	
AN33	28	—	I	Analog	
AN34	29	—	I	Analog	
AN35	38	—	I	Analog	
AN36	39	—	I	Analog	
AN37	40	—	I	Analog	
AN38	47	—	I	Analog	
AN39	48	—	I	Analog	
AN40	52	—	I	Analog	
AN41	53	—	I	Analog	
AN45	61	—	I	Analog	
AN46	66	—	I	Analog	
AN47	67	—	I	Analog	
AN48	71	45	I	Analog	
AN49	63	39	I	Analog	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-2: OSCILLATOR PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CLKI	63	39	I	ST	External clock source input. Always associated with OSC1 pin function.
CLKO	64	40	O	CMOS	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	63	39	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	64	40	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	73	47	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	74	48	O	CMOS	32.768 low-power oscillator crystal output.
REFCLKI	PPS	PPS	I	—	One of several alternate REFCLKOx user-selectable input clock sources.
REFCLKO1	PPS	PPS	O	—	Reference Clock Generator Outputs 1-4
REFCLKO2	PPS	PPS	O	—	
REFCLKO3	PPS	PPS	O	—	
REFCLKO4	PPS	PPS	O	—	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer
Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input

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TABLE 1-3: CVD, CAPACITIVE TOUCH ASSIST PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/TQFP			
CVD6	32	21	Input	Analog	Capacitive Touch Assist
CVD7	33	22	Input	Analog	
CVD8	34	23	Input	Analog	
CVD9	21	12	Input	Analog	
CVD10	20	11	Input	Analog	
CVD11	35	24	Input	Analog	
CVD12	41	27	Input	Analog	
CVD13	42	28	Input	Analog	
CVD14	43	29	Input	Analog	
CVD15	44	30	Input	Analog	
CVD16	14	8	Input	Analog	
CVD17	12	6	Input	Analog	
CVD18	11	5	Input	Analog	
CVD19	10	4	Input	Analog	
CVD20	19	—	Input	Analog	
CVD21	18	—	Input	Analog	
CVD22	17	—	Input	Analog	
CVD23	1	—	Input	Analog	
CVD24	51	33	Input	Analog	
CVD25	72	46	Input	Analog	
CVD26	49	31	Input	Analog	
CVD27	76	49	Input	Analog	
CVD33	28	—	Input	Analog	
CVD34	29	—	Input	Analog	
CVD35	38	—	Input	Analog	
CVD36	39	—	Input	Analog	
CVD37	40	—	Input	Analog	
CVD38	47	—	Input	Analog	
CVD39	48	—	Input	Analog	
CVD40	52	—	Input	Analog	
CVD41	53	—	Input	Analog	
CVD45	61	—	Input	Analog	
CVD46	66	—	Input	Analog	
CVD47	67	—	Input	Analog	
CVD48	71	45	Input	Analog	
CVD49	63	39	Input	Analog	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-4: IC1 THROUGH IC16 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Input Capture					
IC1	PPS	PPS	I	ST	Input Capture Inputs 1-6
IC2	PPS	PPS	I	ST	
IC3	PPS	PPS	I	ST	
IC4	PPS	PPS	I	ST	
IC5	PPS	PPS	I	ST	
IC6	PPS	PPS	I	ST	
IC7	PPS	PPS	I	ST	
IC8	PPS	PPS	I	ST	
IC9	PPS	PPS	I	ST	
IC10	PPS	PPS	I	ST	
IC11	PPS	PPS	I	ST	
IC12	PPS	PPS	I	ST	
IC13	PPS	PPS	I	ST	
IC14	PPS	PPS	I	ST	
IC15	PPS	PPS	I	ST	
IC16	PPS	PPS	I	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

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TABLE 1-5: OC1 THROUGH OC16 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Output Compare					
OC1	PPS	PPS	O	—	Output Compare Outputs 1-16
OC2	PPS	PPS	O	—	
OC3	PPS	PPS	O	—	
OC4	PPS	PPS	O	—	
OC5	PPS	PPS	O	—	
OC6	PPS	PPS	O	—	
OC7	PPS	PPS	O	—	
OC8	PPS	PPS	O	—	
OC9	PPS	PPS	O	—	
OC10	PPS	PPS	O	—	
OC11	PPS	PPS	O	—	
OC12	PPS	PPS	O	—	
OC13	PPS	PPS	O	—	
OC14	PPS	PPS	O	—	
OC15	PPS	PPS	O	—	
OC16	PPS	PPS	O	—	
OCFA	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	PPS	PPS	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-6: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
External Interrupts					
INT0	72	46	I	ST	External Interrupt 0
INT1	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-7: PORTA THROUGH PORTG PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PORTA					
RA0	22	13	I/O	ST	PORTA is a bidirectional I/O port
RA1	23	14	I/O	ST	
RA4	51	33	I/O	ST	
RA7	3	1	I/O	ST	
RA8	49	31	I/O	ST	
RA10	100	64	I/O	ST	
RA11	21	12	I/O	ST	
RA12	20	11	I/O	ST	
RA14	66	—	I/O	ST	
RA15	67	—	I/O	ST	
PORTB					
RB0	24	15	I/O	ST	PORTB is a bidirectional I/O port
RB1	25	16	I/O	ST	
RB2	26	17	I/O	ST	
RB3	27	18	I/O	ST	
RB4	50	32	I/O	ST	
RB5	69	43	I/O	ST	
RB6	70	44	I/O	ST	
RB7	72	46	I/O	ST	
RB8	74	48	I	ST	
RB9	76	49	I/O	ST	
RB10	93	60	I/O	ST	
RB11	94	61	I/O	ST	
RB12	98	62	I/O	ST	
RB13	99	63	I/O	ST	
RB14	4	2	I/O	ST	
RB15	5	3	I/O	ST	
PORTC					
RC0	32	21	I/O	ST	PORTC is a bidirectional I/O port
RC1	33	22	I/O	ST	
RC2	34	23	I/O	ST	
RC6	77	50	I/O	ST	
RC7	78	51	I/O	ST	
RC8	81	52	I/O	ST	
RC9	84	55	I/O	ST	
RC10	71	45	I/O	ST	
RC11	35	24	I/O	ST	
RC12	63	39	I/O	ST	
RC13	73	47	I	ST	
RC15	64	40	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on 100-pin general purpose devices.
2: This function does not exist on 64-pin general purpose devices.
3: This function does not exist on any general purpose devices.

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TABLE 1-7: PORTA THROUGH PORTG PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PORTD					
RD1	6	—	I/O	ST	PORTD is a bidirectional I/O port
RD2	7	—	I/O	ST	
RD3	8	—	I/O	ST	
RD4	9	—	I/O	ST	
RD5	82	53	I/O	ST	
RD6	83	54	I/O	ST	
RD8(3)	68	42	I/O	ST	
RD12	79	—	I/O	ST	
RD13	80	—	I/O	ST	
RD14	47	—	I/O	ST	
RD15	48	—	I/O	ST	
PORTE					
RE0	52	—	I/O	ST	PORTE is a bidirectional I/O port
RE1	53	—	I/O	ST	
RE8	18	—	I/O	ST	
RE9	19	—	I/O	ST	
RE12	41	27	I/O	ST	
RE13	42	28	I/O	ST	
RE14	43	29	I/O	ST	
RE15	44	30	I/O	ST	
PORTF					
RF0	87	58	I/O	ST	PORTF is a bidirectional I/O port
RF1	88	59	I/O	ST	
RF5	61	—	I/O	ST	
RF6	91	—	I/O	ST	
RF7	92	—	I/O	ST	
RF9	28	—	I/O	ST	
RF10	29	—	I/O	ST	
RF12	40	—	I/O	ST	
RF13	39	—	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on 100-pin general purpose devices.
2: This function does not exist on 64-pin general purpose devices.
3: This function does not exist on any general purpose devices.

TABLE 1-7: PORTA THROUGH PORTG PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PORTG					
RG0	90	—	I/O	ST	PORTG is a bidirectional I/O port
RG1	89	—	I/O	ST	
RG6	10	4	I/O	ST	
RG7	11	5	I/O	ST	
RG8	12	6	I/O	ST	
RG9	14	8	I/O	ST	
RG10	17	—	I/O	ST	
RG11	38	—	I/O	ST	
RG12	96	—	I/O	ST	
RG13	97	—	I/O	ST	
RG14	95	—	I/O	ST	
RG15	1	—	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on 100-pin general purpose devices.
2: This function does not exist on 64-pin general purpose devices.
3: This function does not exist on any general purpose devices.

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TABLE 1-8: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Universal Asynchronous Receiver Transmitter 1					
U1RX	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	O	—	UART1 Transmit
U1CTS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2					
U2RX	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	O	—	UART2 Transmit
U2CTS	PPS	PPS	I	ST	UART2 Clear To Send
U2RTS	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3					
U3RX	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	O	—	UART3 Transmit
U3CTS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4					
U4RX	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	O	—	UART4 Transmit
U4CTS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5					
U5RX	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	O	—	UART5 Transmit
U5CTS	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6					
U6RX	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	O	—	UART6 Transmit
U6CTS	PPS	PPS	I	ST	UART6 Clear to Send
U6RTS	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-9: SPI1 THROUGH SPI 6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Serial Peripheral Interface 1					
SCK1	72	46	I/O	ST/CMOS	SPI1 Synchronous Serial Clock Input/Output
SDI1	PPS	PPS	I	ST	SPI1 Data In
SDO1	PPS	PPS	O	CMOS	SPI1 Data Out
SS1	PPS	PPS	I/O	ST/CMOS	SPI1 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 2					
SCK2	70	44	I/O	ST/CMOS	SPI2 Synchronous Serial Clock Input/output
SDI2	PPS	PPS	I	ST	SPI2 Data In
SDO2	PPS	PPS	O	CMOS	SPI2 Data Out
SS2	PPS	PPS	I/O	ST/CMOS	SPI2 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 3					
SCK3	PPS	PPS	I/O	ST/CMOS	SPI3 Synchronous Serial Clock Input/Output
SDI3	PPS	PPS	I	ST	SPI3 Data In
SDO3	PPS	PPS	O	CMOS	SPI3 Data Out
SS3	PPS	PPS	I/O	ST/CMOS	SPI3 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 4					
SCK4	PPS	PPS	I/O	ST/CMOS	SPI4 Synchronous Serial Clock Input/Output
SDI4	PPS	PPS	I	ST	SPI4 Data In
SDO4	PPS	PPS	O	CMOS	SPI4 Data Out
SS4	PPS	PPS	I/O	ST/CMOS	SPI4 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 5					
SCK5	PPS	PPS	I/O	ST/CMOS	SPI5 Synchronous Serial Clock Input/Output
SDI5	PPS	PPS	I	ST	SPI5 Data In
SDO5	PPS	PPS	O	CMOS	SPI5 Data Out
SS5	PPS	PPS	I/O	ST/CMOS	SPI5 Slave Synchronization Or Frame Pulse I/O
Serial Peripheral Interface 6					
SCK6	PPS	PPS	I/O	ST/CMOS	SPI6 Synchronous Serial Clock Input/Output
SDI6	PPS	PPS	I	ST	SPI6 Data In
SDO6	PPS	PPS	O	CMOS	SPI6 Data Out
SS6	PPS	PPS	I/O	ST/CMOS	SPI6 Slave Synchronization Or Frame Pulse I/O

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

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TABLE 1-10: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Timer1 through Timer9					
T1CK	51	33	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar					
RTCC	27	18	O	—	Real-Time Clock Alarm/Seconds Output (not in VBAT power domain, requires V_{DD})

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-11: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PMA0	44	30	O	TTL/CMOS	Parallel Master Port Address (Demultiplexed Master mode) or Address/ Data (Multiplexed Master modes)
PMA1	43	29	O	TTL/CMOS	
PMA2	14	8	O	TTL/CMOS	
PMA3	12	6	O	TTL/CMOS	
PMA4	11	5	O	TTL/CMOS	
PMA5	10	4	O	TTL/CMOS	
PMA6	29	16	O	TTL/CMOS	
PMA7	28	22	O	TTL/CMOS	
PMA8	50	32	O	TTL/CMOS	
PMA9	49	31	O	TTL/CMOS	
PMA10	42	28	O	TTL/CMOS	
PMA11	41	27	O	TTL/CMOS	
PMA12	35	24	O	TTL/CMOS	
PMA13	34	23	O	TTL/CMOS	
PMA14	71	45	O	TTL/CMOS	
PMA15	70	44	O	TTL/CMOS	
PMA16	77	—	O	TTL/CMOS	
PMA17	78	—	O	TTL/CMOS	
PMA18	91	—	O	TTL/CMOS	
PMA19	92	—	O	TTL/CMOS	
PMA20	95	—	O	TTL/CMOS	
PMA21	96	—	O	TTL/CMOS	
PMA22	97	—	O	TTL/CMOS	
PMA23	1	—	O	TTL/CMOS	
PMCS1	71	45	O	TTL/CMOS	Parallel Master Port Chip Select 1 for PMA(13:0)
PMCS2	70	44	O	TTL/CMOS	Parallel Master Port Chip Select 2 for PMA(14:0)
PMPRD	82	53	O	TTL/CMOS	Parallel Master Port Read Strobe
PMWR	81	52	O	TTL/CMOS	Parallel Master Port Write Strobe
PMCS1A	97	—	O	TTL/CMOS	Parallel Master Port Chip Select 1 for PMA(21:0)
PMCS2A	1	—	O	TTL/CMOS	Parallel Master Port Chip Select 2 for PMA(22:0)

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

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TABLE 1-11: PMP PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
PMD0	93	60	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	94	61	I/O	TTL/ST	
PMD2	98	62	I/O	TTL/ST	
PMD3	99	63	I/O	TTL/ST	
PMD4	100	64	I/O	TTL/ST	
PMD5	3	1	I/O	TTL/ST	
PMD6	4	2	I/O	TTL/ST	
PMD7	5	3	I/O	TTL/ST	
PMD8	90	—	I/O	TTL/ST	
PMD9	89	—	I/O	TTL/ST	
PMD10	88	—	I/O	TTL/ST	
PMD11	87	—	I/O	TTL/ST	
PMD12	79	—	I/O	TTL/ST	
PMD13	80	—	I/O	TTL/ST	
PMD14	83	—	I/O	TTL/ST	
PMD15	84	—	I/O	TTL/ST	
PMALH	43	29	O	TTL/CMOS	Parallel Master Port Address Latch Enable High Byte (Multiplexed Master modes)
PMALL	44	30	O	—	Parallel Master Port Address Latch Enable Low Byte (Multiplexed Master modes)

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-12: COMPARATOR 1 THROUGH COMPARATOR 5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Comparator 1					
C1IN1+	26	17	I	Analog	Comparator 1 Positive Input
C1IN1-	27	18	I	Analog	Comparator 1 Negative Input 1-4
C1IN2-	35	24	I	Analog	
C1IN3-	26	17	I	Analog	
C1IN4-	25	16	I	Analog	
C1OUT	PPS	PPS	O	—	Comparator 1 Output
Comparator 2					
C2IN1+	23	14	I	Analog	Comparator 2 Positive Input
C2IN1-	24	15	I	Analog	Comparator 2 Negative Input 1-4
C2IN2-	41	27	I	Analog	
C2IN3-	26	17	I	Analog	
C2IN4-	22	13	I	Analog	
C2OUT	PPS	PPS	O	—	Comparator 2 Output
Comparator 3					
C3IN1+	34	23	I	Analog	Comparator 3 Positive Input
C3IN1-	33	22	I	Analog	Comparator 3 Negative Input 1-4
C3IN2-	42	28	I	Analog	
C3IN3-	34	23	I	Analog	
C3IN4-	32	21	I	Analog	
C3OUT	PPS	PPS	O	—	Comparator 3 Output
Comparator 4					
C4IN1+	32	21	I	Analog	Comparator 4 Positive Input
C4IN1-	33	22	I	Analog	Comparator 4 Negative Input 1-4
C4IN2-	25	16	I	Analog	
C4IN3-	22	13	I	Analog	
C4IN4-	32	21	I	Analog	
C4OUT	PPS	PPS	O	—	Comparator 4 Output
Comparator 5					
C5IN1+	51	33	I	Analog	Comparator 5 Positive Input
C5IN1-	76	49	I	Analog	Comparator 5 Negative Input 1-4
C5IN2-	41	27	I	Analog	
C5IN3-	51	33	I	Analog	
C5IN4-	72	46	I	Analog	
C1OUT	PPS	PPS	O	—	Comparator 5 Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

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TABLE 1-13: OP AMP 1 THROUGH OP AMP 3, AND OP AMP 5 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Op amp 1					
OA1OUT	25	16	O	Analog	Op amp 1 Output
OA1IN+	26	17	I	Analog	Op amp 1 Positive Input
OA1IN-	27	18	I	Analog	Op amp 1 Negative Input
Op amp 2					
OA2OUT	22	13	O	Analog	Op amp 2 Output
OA2IN+	23	14	I	Analog	Op amp 2 Positive Input
OA2IN-	24	15	I	Analog	Op amp 2 Negative Input
Op amp 3					
OA3OUT	32	21	O	Analog	Op amp 3 Output
OA3IN+	34	23	I	Analog	Op amp 3 Positive Input
OA3IN-	33	22	I	Analog	Op amp 3 Negative Input
Op amp 5					
OA5OUT	72	46	O	Analog	Op amp 5 Output
OA5IN+	51	33	I	Analog	Op amp 5 Positive Input
OA5IN-	76	49	I	Analog	Op amp 5 Negative Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-14: CAN1 THROUGH CAN4 PINOUT I/O DESCRIPTIONS

Pin Name (see Note 1)	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
C1TX	PPS	PPS	O	—	CAN1 Bus Transmit Pin
C1RX	PPS	PPS	I	ST	CAN1 Bus Receive Pin
C2TX	PPS	PPS	O	—	CAN2 Bus Transmit Pin
C2RX	PPS	PPS	I	ST	CAN2 Bus Receive Pin
C3TX	PPS	PPS	O	—	CAN3 Bus Transmit Pin
C3RX	PPS	PPS	I	ST	CAN3 Bus Receive Pin
C4TX	PPS	PPS	O	—	CAN4 Bus Transmit Pin
C4RX	PPS	PPS	I	ST	CAN4 Bus Receive Pin

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: This function does not exist on PIC32MKXXXGPDXXX devices.

TABLE 1-15: USB1 AND USB2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
VUSB3V3	55	35	P	—	USB internal transceiver supply. This pin should be connected to VDD.
VBUS1	54	34	I	Analog	USB1 Bus Power Monitor (Tied to VSS if USB1 not used.)
VBUSON1	4	2	O	CMOS	USB1 VBUS Power Control Output
VBUSON2	10	—	O	CMOS	USB2 VBUS Power Control Output
D1+	57	37	I/O	Analog	USB1 D+ (Connect through 10K to VSS if USB1 not used.)
D1-	56	36	I/O	Analog	USB1 D-(Connect through 10K to VSS if USB1 not used.)
USBID1	69	43	I	ST	USB1 OTG ID Detect
VBUS2	58	—	I	Analog	USB2 Bus Power Monitor (Tied to VSS if USB2 not used.)
D2+	60	—	I/O	Analog	USB2 D+ (Connect through 10K to VSS if USB2 not used.)
D2-	59	—	I/O	Analog	USB2 D- (Connect through 10K to VSS if USB2 not used.)
USBID2	77	—	I	ST	USB2 OTG ID detect

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-16: CTMU PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CTED1	25	16	I	ST	CTMU External Edge Input 1
CTED2	24	15	I	ST	CTMU External Edge Input 2
CTCMP	27	18	I	Analog	CTMU external capacitor input for pulse generation
CTPLS	PPS	PPS	O	CMOS	CTMU Pulse Generator Output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-17: CDAC1 THROUGH CDAC3 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
CDAC1	51	33	O	Analog	12-bit CDAC1 output
CDAC2	71	45	O	Analog	12-bit CDAC2 output
CDAC3	49	31	O	Analog	12-bit CDAC3 output

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

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TABLE 1-18: MCPWM1 THROUGH MCPWM12 PINOUT I/O DESCRIPTIONS (MOTOR CONTROL DEVICES ONLY)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-Pin TQFP	64-Pin QFN/ TQFP			
PWM1H	4	2	O	CMOS	MCPWM1 High Side Output
PWM1L	5	3	O	CMOS	MCPWM1 Low Side Output (Only if PWMAPIN1 (CFGCON<18>) = 0, default)
PWM2H	98	62	O	CMOS	MCPWM2 High Side Output
PWM2L	99	63	O	CMOS	MCPWM2 Low Side Output (Only if PWMAPIN2 (CFGCON<19>) = 0, default)
PWM3H	93	60	O	CMOS	MCPWM3 High Side Output
PWM3L	94	61	O	CMOS	MCPWM3 Low Side Output (Only if PWMAPIN3 (CFGCON<20>) = 0, default)
PWM4H	100	64	O	CMOS	MCPWM4 High Side Output
PWM4L	3	1	O	CMOS	MCPWM4 Low Side Output (Only if PWMAPIN4 (CFGCON<21>) = 0, default)
PWM5H	7	52	O	CMOS	MCPWM5 High Side Output
PWM5L	6	55	O	CMOS	MCPWM5 Low Side Output (Only if PWMAPIN5 (CFGCON<22>) = 0, default)
PWM6H	9	50	O	CMOS	MCPWM6 High Side Output
PWM6L	8	51	O	CMOS	MCPWM6 Low Side Output (Only if PWMAPIN6 (CFGCON<23>) = 0, default)
PWM7H	5	3	O	CMOS	If PWMAPIN1 (CFGCON<18>) = 1), PWM1L is replaced by PWM7H.
PWM8H	99	63	O	CMOS	If PWMAPIN2 (CFGCON<19>) = 1), PWM2L is replaced by PWM8H.
PWM9H	94	61	O	CMOS	If PWMAPIN3 (CFGCON<20>) = 1), PWM3L is replaced by PWM9H.
PWM10H	3	1	O	CMOS	If PWMAPIN4 (CFGCON<21>) = 1), PWM4L is replaced by PWM10H.
PWM11H	87	55	O	CMOS	MCPWM11 High Side Output
	6	58	O	CMOS	If PWMAPIN5 (CFGCON<22>) = 1), PWM5L is replaced by PWM11H.
PWM11L	88	59	O	CMOS	MCPWM11 Low Side Output
PWM12H	82	51	O	CMOS	MCPWM12 High Side Output
	8	55	O	CMOS	If PWMAPIN6 (CFGCON<23>) = 1), PWM6L is replaced by PWM12H.
PWM12L	83	54	O	CMOS	MCPWM12 Low Side Output

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-Transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-19: MCPWM FAULT, CURRENT-LIMIT, AND DEAD TIME COMPENSATION PINOUT I/O DESCRIPTIONS (MOTOR CONTROL DEVICES ONLY)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-Pin TQFP	64-Pin QFN/ TQFP			
FLT1	PPS	PPS	I	ST	PWM Fault Input Control
FLT2	PPS	PPS	I	ST	
FLT3	34	23	I	ST	
FLT4	35	24	I	ST	
FLT5	41	27	I	ST	
FLT6	42	28	I	ST	
FLT7	43	29	I	ST	
FLT8	44	30	I	ST	
FLT15	50	32	I	ST	

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-Transistor Logic input buffer
Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input

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TABLE 1-20: QEI1 THROUGH QEI6 PINOUT I/O DESCRIPTIONS (MOTOR CONTROL DEVICES ONLY)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-Pin TQFP	64-Pin QFN/ TQFP			
Quadrature Encoder Interface 1					
QEA1	PPS	PPS	I	ST	QEI1 Phase A Input in QEI mode
QEB1	PPS	PPS	I	ST	QEI1 Phase B Input in QEI Mode. Auxiliary timer external clock/gate input in Timer mode.
INDX1	PPS	PPS	I	ST	QEI1 Index Pulse Input
HOME1	PPS	PPS	I	ST	QEI1 Position Counter Input Capture Trigger Control
QEICMP1	PPS	PPS	O	CMOS	QEI1 Capture Compare Match Output
Quadrature Encoder Interface 2					
QEA2	PPS	PPS	I	ST	QEI2 Phase A Input in QEI mode
QEB2	PPS	PPS	I	ST	QEI2 Phase B Input in QEI Mode. Auxiliary timer external clock/gate input in Timer mode.
INDX2	PPS	PPS	I	ST	QEI2 Index Pulse Input
HOME2	PPS	PPS	I	ST	QEI2 Position Counter Input Capture Trigger Control
QEICMP2	PPS	PPS	O	CMOS	QEI2 Capture Compare Match Output
Quadrature Encoder Interface 3					
QEA3	PPS	PPS	I	ST	QEI3 Phase A Input in QEI mode
QEB3	PPS	PPS	I	ST	QEI3 Phase B Input in QEI Mode. Auxiliary timer external clock/gate input in Timer mode.
INDX3	PPS	PPS	I	ST	QEI3 Index Pulse Input
HOME3	PPS	PPS	I	ST	QEI3 Position Counter Input Capture Trigger Control
QEICMP3	PPS	PPS	O	CMOS	QEI3 Capture Compare Match Output
Quadrature Encoder Interface 4					
QEA4	PPS	PPS	I	ST	QEI4 Phase A Input in QEI mode
QEB4	PPS	PPS	I	ST	QEI4 Phase B Input in QEI Mode. Auxiliary timer external clock/gate input in Timer mode.
INDX4	PPS	PPS	I	ST	QEI4 Index Pulse Input
HOME4	PPS	PPS	I	ST	QEI4 Position Counter Input Capture Trigger Control
QEICMP4	PPS	PPS	O	CMOS	QEI4 Capture Compare Match Output
Quadrature Encoder Interface 5					
QEA5	PPS	PPS	I	ST	QAI5 Phase A Input in QEI mode
QEB5	PPS	PPS	I	ST	QAI5 Phase B Input in QEI Mode. Auxiliary timer external clock/gate input in Timer mode.
INDX5	PPS	PPS	I	ST	QAI5 Index Pulse Input
HOME5	PPS	PPS	I	ST	QAI5 Position Counter Input Capture Trigger Control
QEICMP5	PPS	PPS	O	CMOS	QAI5 Capture Compare Match Output
Quadrature Encoder Interface 6					
QEA6	PPS	PPS	I	ST	QEI6 Phase A Input in QEI mode
QEB6	PPS	PPS	I	ST	QEI6 Phase B Input in QEI Mode. Auxiliary timer external clock/gate input in Timer mode.
INDX6	PPS	PPS	I	ST	QEI6 Index Pulse Input
HOME6	PPS	PPS	I	ST	QEI6 Position Counter Input Capture Trigger Control
QEICMP6	PPS	PPS	O	CMOS	QEI6 Capture Compare Match Output

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-Transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 1-21: POWER, GROUND, AND VOLTAGE REFERENCE PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
Power and Ground					
AVDD	30	19	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	31	20	P	P	Ground reference for analog modules. This pin must be connected at all times.
VDD	2, 16, 37, 46, 62, 86	10, 26, 38, 57	P	—	Positive supply for peripheral logic and I/O pins. This pin must be connected at all times.
VSS	15, 36, 45, 65, 75, 85	9, 25, 41, 56	P	—	Ground reference for logic, I/O pins, and USB. This pin must be connected at all times.
VBAT(1)	68	42	P	P	Battery backup for selected peripherals; otherwise connect to VDD.
Voltage Reference					
VREF+	29	16	I	Analog	Analog Voltage Reference (High) Input
VREF-	28	15	I	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

Note 1: VBAT functionality is compromised, see errata for additional information. This pin should be connected to VDD.

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TABLE 1-22: JTAG, TRACE, AND PROGRAMMING/DEBUGGING PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	100-pin TQFP	64-pin QFN/ TQFP			
JTAG					
TCK	3	1	I	ST	JTAG Test Clock Input Pin
TDI	49	31	I	ST	JTAG Test Data Input Pin
TDO	100	64	O	—	JTAG Test Data Output Pin
TMS	76	49	I	ST	JTAG Test Mode Select Pin
Trace					
TRCLK	91	50	O	CMOS	Trace Clock
TRD0	97	54	O	CMOS	Trace Data bits 0-3 Trace support is available through the MPLAB® REAL ICE™ In-circuit Emulator.
TRD1	96	53	O	CMOS	
TRD2	95	52	O	CMOS	
TRD3	92	51	O	CMOS	
Programming/Debugging					
PGED1	27	18	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	26	17	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	69	43	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	70	44	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
PGED3	24	15	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3
PGEC3	25	16	I	ST	Clock input pin for Programming/Debugging Communication Channel 3
$\overline{\text{MCLR}}$	13	7	I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

NOTES:

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2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUS

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Getting started with the PIC32MK GP/MC family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **2.3 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.4 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **2.7 "External Oscillator Pins"**)

The following pins may be required:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

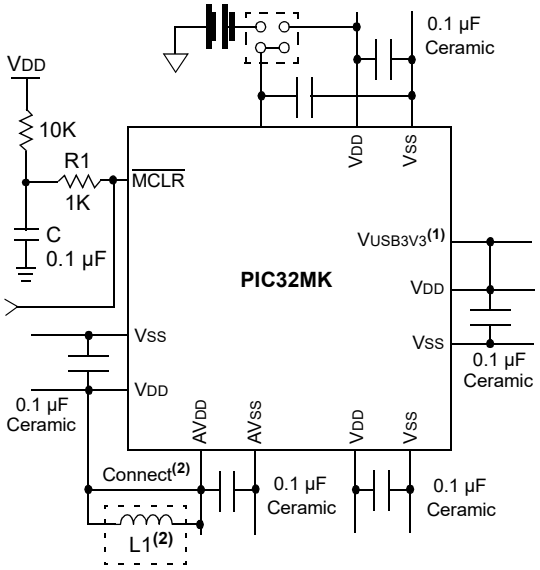
2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: This pin must be connected to VDD, regardless of whether the USB module is or is not used.

2: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 3Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

3: Aluminum or electrolytic capacitors should not be used. ESR ≤ 3Ω from -40ºC to 125ºC @ SYSCLK frequency (i.e., MIPS).

2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

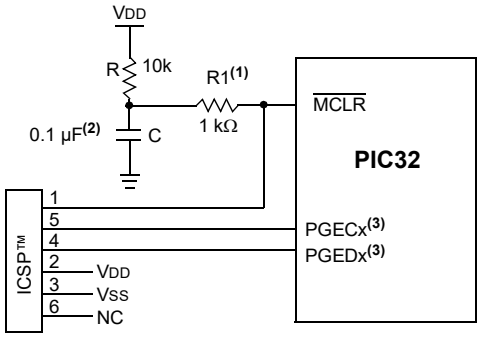
- Device Reset
- Device programming and debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: 470Ω ≤ R1 ≤ 1 KΩ will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

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2.4 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For additional information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) DS50001765
- *"MPLAB® ICD 3 Design Advisory"* DS50001764
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide"* DS50001616
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) DS50001749

2.5 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

2.6 Trace

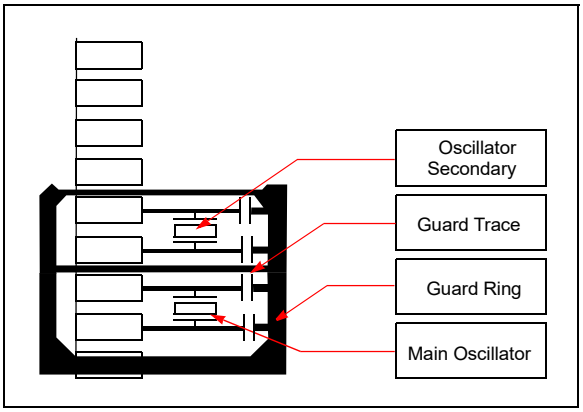
When present on select pin counts, the trace pins can be connected to a hardware trace-enabled programmer to provide a compressed real-time instruction trace. When used for trace, the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22 Ohm series resistor between the trace pins and the trace connector.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.7.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- CIN = PIC32_OSC2_Pin Capacitance = 4 pF
- COUT = PIC32_OSC1_Pin Capacitance = 4 pF
- PCB stray capacitance (i.e., 12 mm length) = 2.5 pF
- C1 and C2 = the loading capacitors to use on your crystal circuit design to guarantee that the effective capacitance as seen by the crystal in circuit meets the crystal manufacturer specification

MFG Crystal Data Sheet CLOAD spec:

CLOAD = {([Cin + C1] * [COUT + C2]) / [Cin + C1 + C2 + COUT] } + oscillator PCB stray capacitance

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION

Crystal manufacturer data sheet spec example: C_{LOAD} = 15 *pF*

Therefore:

$$MFG\ C_{LOAD} = \{([C_{IN} + C1] * [C_{OUT} + C2]) / [C_{IN} + C1 + C2 + C_{OUT}] \} + estimated\ oscillator\ PCB\ stray\ capacitance$$

Assuming *C1 = C2* and PIC32 *Cin = Cout*, the formula can be further simplified and restated to solve for *C1* and *C2* by:

$$C1 = C2 = ((2 * MFG\ Cload\ spec) - Cin - (2 * PCB\ capacitance))$$
$$= ((2 * 15) - 4 - (2 * 2.5\ pF))$$
$$= (30 - 4 - 5)$$
$$= 21\ pF$$

Therefore:

C1 = C2 = 21 pF is the correct loading capacitors to use on your crystal circuit design to guarantee that the effective capacitance as seen by the crystal in circuit in this example is 15 pF to meet the crystal manufacturer specification.

Tips to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

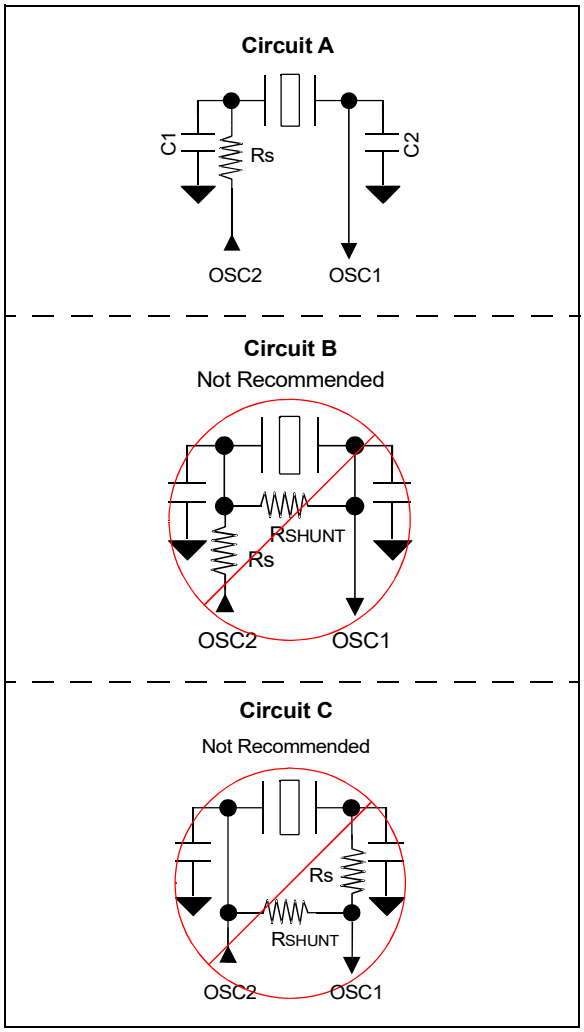
- Select an crystal oscillator with a lower XTAL manufacturing “ESR” rating.
- Add a parallel resistor across the crystal. The greater the resistor value the greater the gain.
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- Likewise, C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.

Note: Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, RS, as shown in circuit “A” in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. When measuring the oscillator signal you must use an active-powered scope probe with ≤ 1 pF or the scope probe itself will unduly change the gain and peak-to-peak levels.

2.7.1.1 Additional Microchip References

- AN588 *“PICmicro® Microcontroller Oscillator Design Guide”*
- AN826 *“Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices”*
- AN849 *“Basic PICmicro® Oscillator Design”*

FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS



Note: Refer to the *“PIC32MK GP/MC Family Silicon Errata and Data Sheet Clarification”* (DS80000737B), which is available for download from the Microchip web site (www.microchip.com) for the recommended Rs values versus crystal/frequency.

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2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

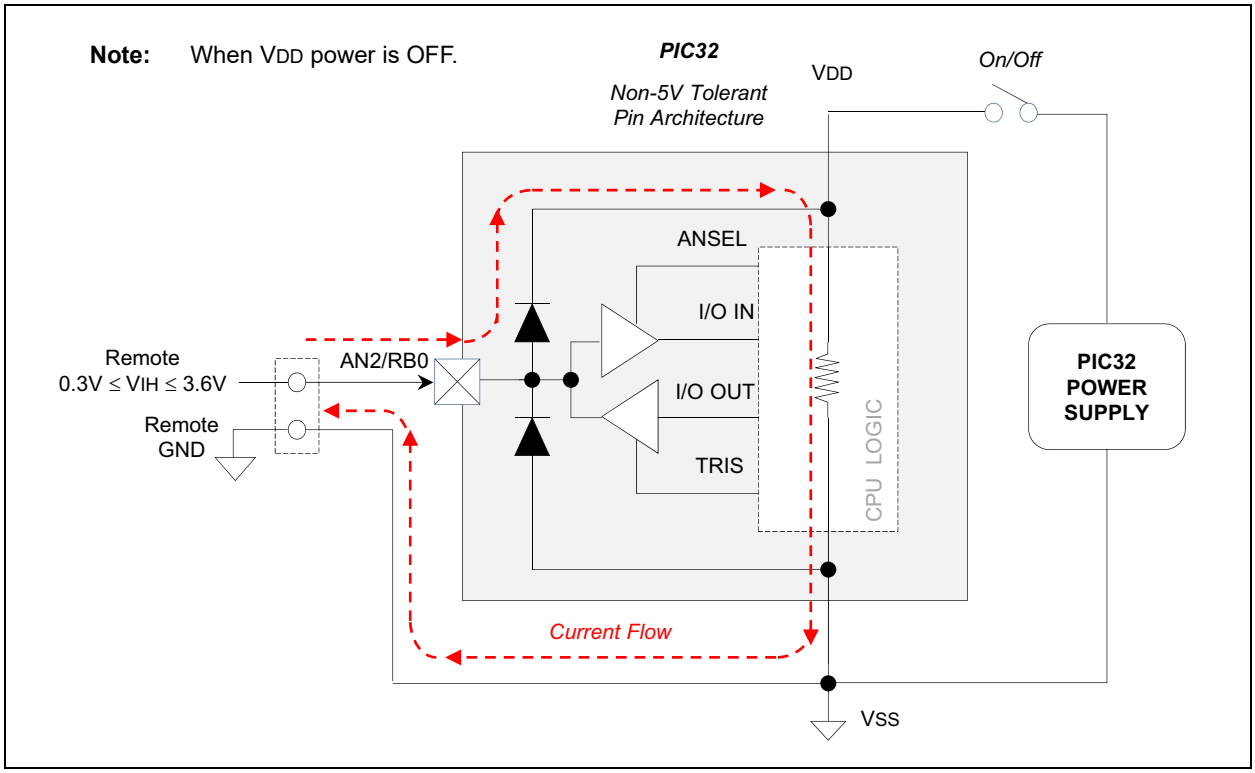
Alternatively, inputs can be reserved by connecting the pin to VSS through a 1k resistor and configuring the pin as an input.

2.9 Considerations When Interfacing to Remotely Powered Circuits

2.9.1 NON-5V TOLERANT INPUT PINS

A quick review of the absolute maximum rating section in **36.0 "Electrical Characteristics"** will indicate that the voltage on any non-5v tolerant pin may not exceed VDD + 0.3V unless the input current is limited to meet the respective injection current specifications defined by parameters DI60a, DI60b, and DI60c in **Table 36-10: "DC Characteristics: I/O Pin Input Injection current Specifications"**. Figure 2-5 shows an example of a remote circuit using an independent power source, which is powered while connected to a PIC32 non-5V tolerant circuit that is not powered.

FIGURE 2-5: PIC32 NON-5V TOLERANT CIRCUIT EXAMPLE

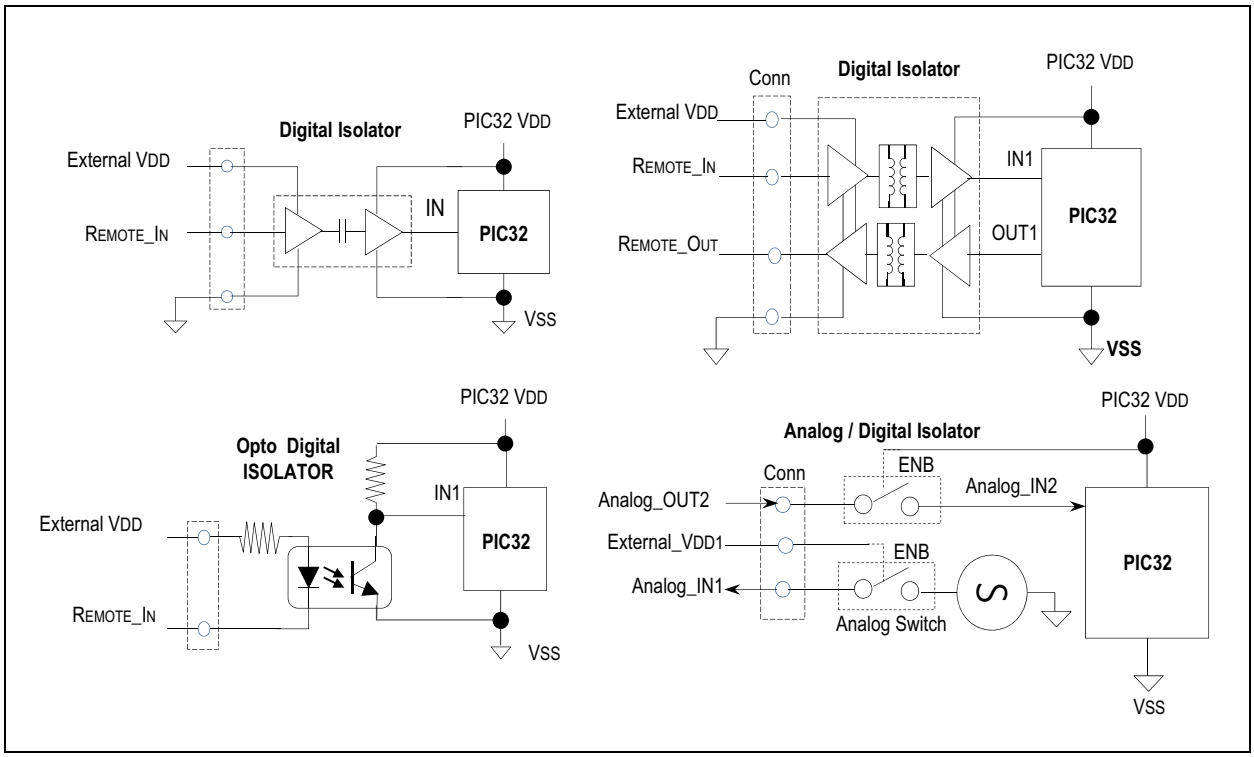


Without proper signal isolation, on non-5V tolerant pins, the remote signal can actually power the PIC32 device through the high side ESD protection diodes. Besides violating the absolute maximum rating specification when VDD of the PIC32 device is restored and ramping up or ramping down, it can also negatively affect the internal Power-on Reset (POR) and Brown-out Reset (BOR) circuits, which can lead to improper initialization of internal PIC32 logic circuits. In these cases, it is recommended to implement digital or analog signal isolation as depicted in Figure 2-6, as appropriate. This is indicative of all industry microcontrollers and not just Microchip products.

TABLE 2-1: EXAMPLES OF DIGITAL/ ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION

Example Digital/Analog Signal Isolation Circuits	Inductive Coupling	Capacitive Coupling	Opto Coupling	Analog/Digital Switch
ADuM7241 / 40 ARZ (1 Mbps)	X	—	—	—
ADuM7241 / 40 CRZ (25 Mbps)	X	—	—	—
ISO721	—	X	—	—
LTV-829S (2 Channel)	—	—	X	—
LTV-849S (4 Channel)	—	—	X	—
FSA266 / NC7WB66	—	—	—	X

FIGURE 2-6: EXAMPLE DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS



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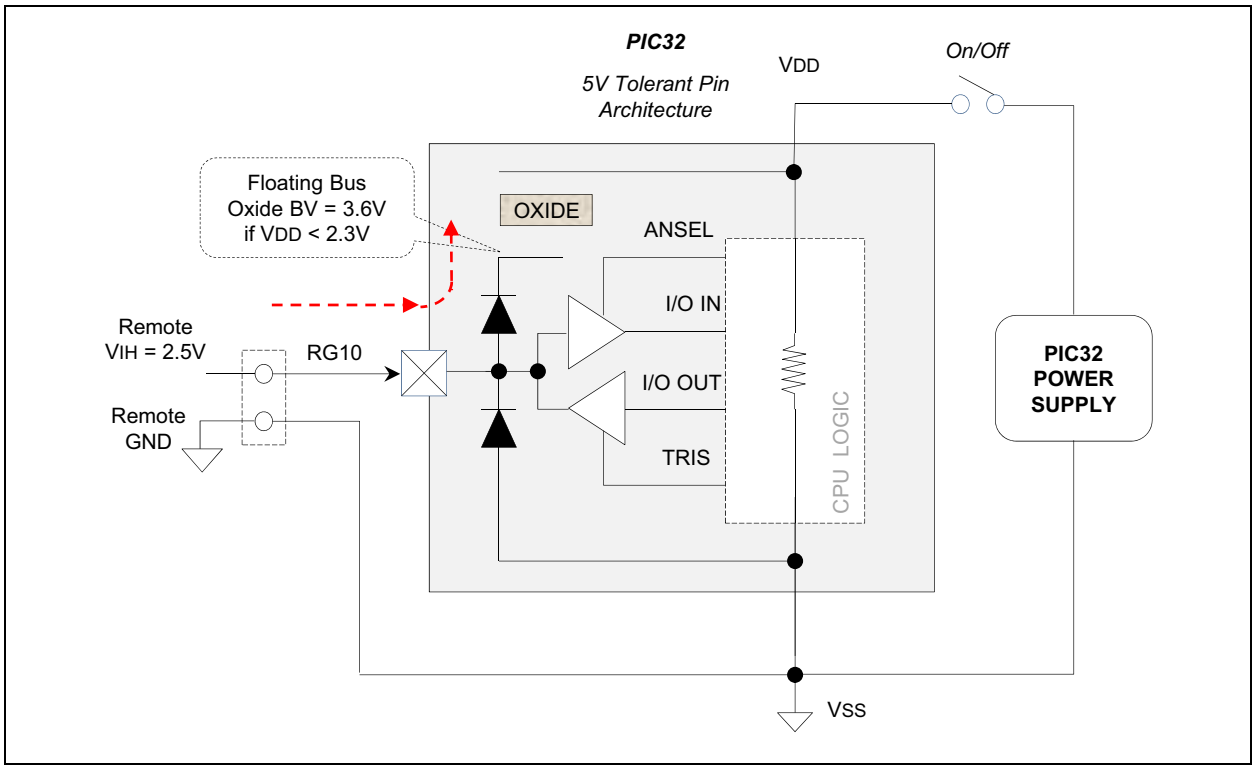
2.9.2 5V TOLERANT INPUT PINS

The internal high side diode on 5v tolerant pins are bussed to an internal floating node, rather than being connected to VDD, as shown in Figure 2-7. Voltages on these pins, if VDD < 2.3V, should not exceed roughly 3.2V relative to VSS of the PIC32 device. Voltage of 3.6V or higher will violate the absolute maximum specification, and will stress the oxide layer separating the high side floating node, which impacts device reliability. If a remotely powered "digital-only" signal can be guaranteed to always be ≤ 3.2V relative to Vss on the PIC32 device side, a 5V tolerant pin could be used without the need for a digital isolator. This is assuming there is not a ground loop issue, logic ground of the two circuits not at the same absolute level, and a remote logic low input is not less than VSS - 0.3V.

FIGURE 2-7: PIC32 5V TOLERANT PIN ARCHITECTURE EXAMPLE



2.10 Designing for High-Speed Peripherals

The PIC32MK GP/MC family devices have peripherals that operate at frequencies much higher than typical for an embedded environment. Table 2-2 lists the peripherals that produce high-speed signals on their external pins:

TABLE 2-2: PERIPHERALS THAT PRODUCE HS SIGNALS ON EXTERNAL PINS

Peripheral	High-Speed Signal Pins	Maximum Speed on Signal Pin
SPI/I^{2}S	SCKx, SDOx, SDIx	50 MHz
REFCLKx	REFCLKx	50 MHz

Due to these high-speed signals, it is important to consider several factors when designing a product that uses these peripherals, as well as the PCB on which these components will be placed. Adhering to these recommendations will help achieve the following goals:

- Minimize the effects of electromagnetic interference to the proper operation of the product
- Ensure signals arrive at their intended destination at the same time
- Minimize crosstalk
- Maintain signal integrity
- Reduce system noise
- Minimize ground bounce and power sag

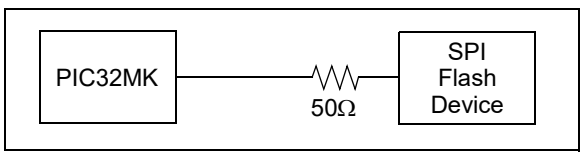
2.10.1 SYSTEM DESIGN

2.10.1.1 Impedance Matching

When selecting parts to place on high-speed buses, particularly the SPI bus and/or REFCLKx output(s), if the impedance of the peripheral device does not match the impedance of the pins on the PIC32MK GP/MC device to which it is connected, signal reflections could result, thereby degrading the quality of the signal.

If it is not possible to select a product that matches impedance, place a series resistor at the load to create the matching impedance. See Figure 2-8 for an example.

FIGURE 2-8: SERIES RESISTOR



2.10.1.2 PCB Layout Recommendations

The following list contains recommendations that will help ensure the PCB layout will promote the goals previously listed.

- **Component Placement**
  - Place bypass capacitors as close to their component power and ground pins as possible, and place them on the same side of the PCB
  - Devices on the same bus that have larger setup times should be placed closer to the PIC32MK GP/MC device
- **Power and Ground**
  - Multi-layer PCBs will allow separate power and ground planes
  - Each ground pin should be connected to the ground plane individually
  - Place bypass capacitor vias as close to the pad as possible (preferably inside the pad)
  - If power and ground planes are not used, maximize width for power and ground traces
  - Use low-ESR, surface-mount bypass capacitors
- **Clocks and Oscillators**
  - Place crystals as close as possible to the PIC32MK GP/MC device OSC/SOSC pins
  - Do not route high-speed signals near the clock or oscillator
  - Avoid via usage and branches in clock lines (SCK)
  - Place termination resistors at the end of clock lines
- **Traces**
  - Higher-priority signals should have the shortest traces
  - Avoid long run lengths on parallel traces to reduce coupling
  - Make the clock traces as straight as possible
  - Use rounded turns rather than right-angle turns
  - Have traces on different layers intersect on right angles to minimize crosstalk
  - Maximize the distance between traces, preferably no less than three times the trace width
  - Power traces should be as short and as wide as possible
  - High-speed traces should be placed close to the ground plane

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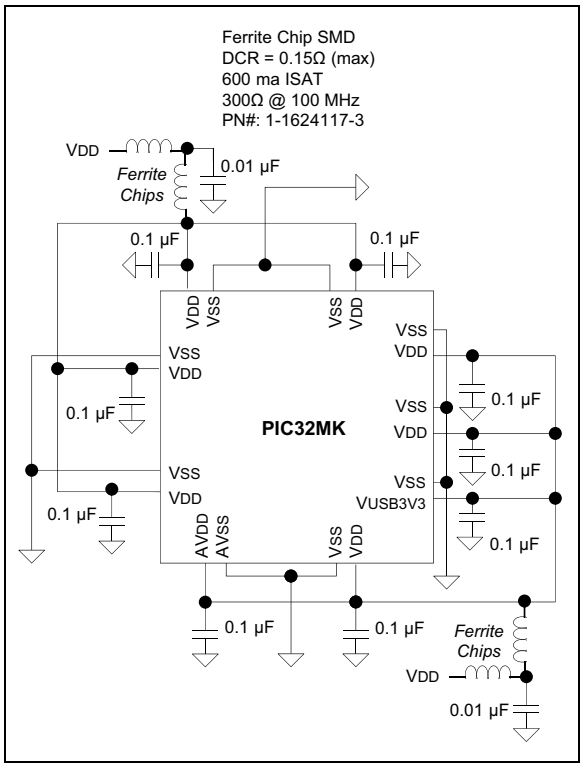
2.10.1.3 EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations

The use of LDO regulators is preferred to reduce overall system noise and provide a cleaner power source. However, when utilizing switching Buck/Boost regulators as the local power source for PIC32MK GP devices, as well as in electrically noisy environments or test conditions required for IEC 61000-4-4 and IEC 61000-4-2, users should evaluate the use of T-Filters (i.e., L-C-L) on the power pins, as shown in Figure 2-9. In addition to a more stable power source, use of this type of T-Filter can greatly reduce susceptibility to EMI sources and events.

FIGURE 2-9: EMI/EMC/EFT SUPPRESSION CIRCUIT



2.11 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-10, Figure 2-11, and Figure 2-12.

FIGURE 2-10: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION

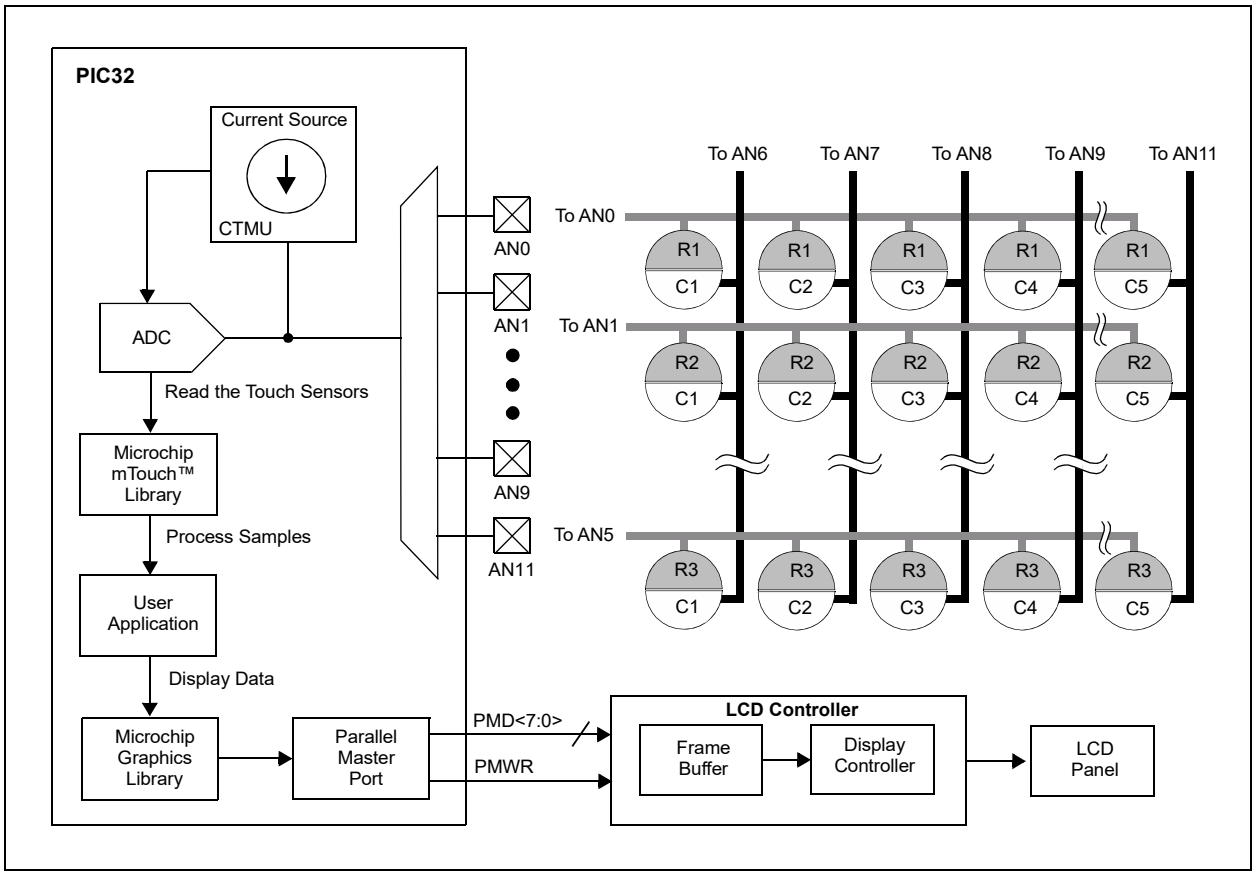


FIGURE 2-11: AUDIO PLAYBACK APPLICATION

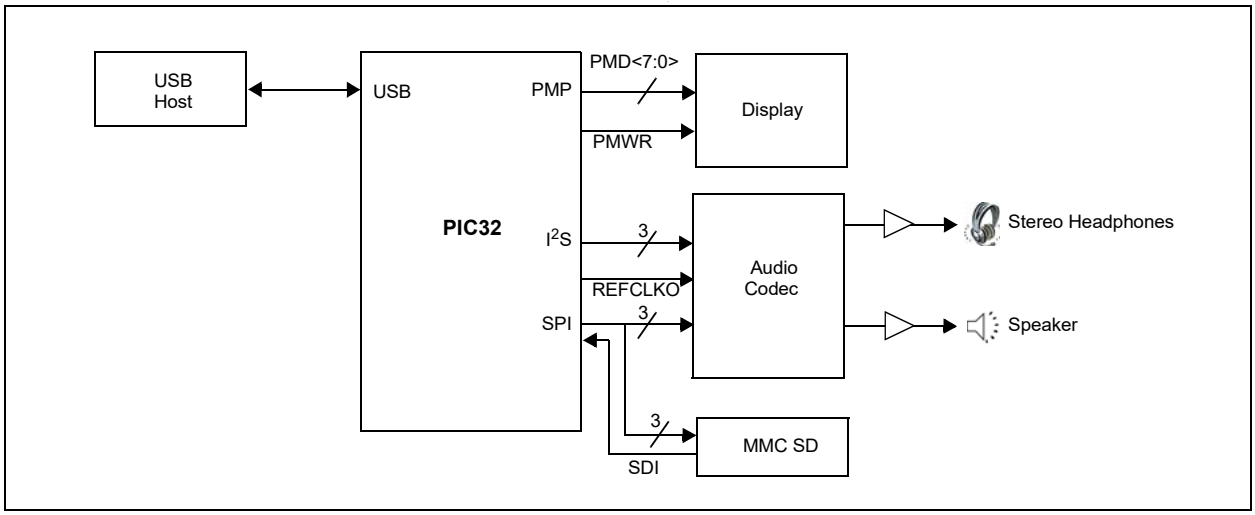


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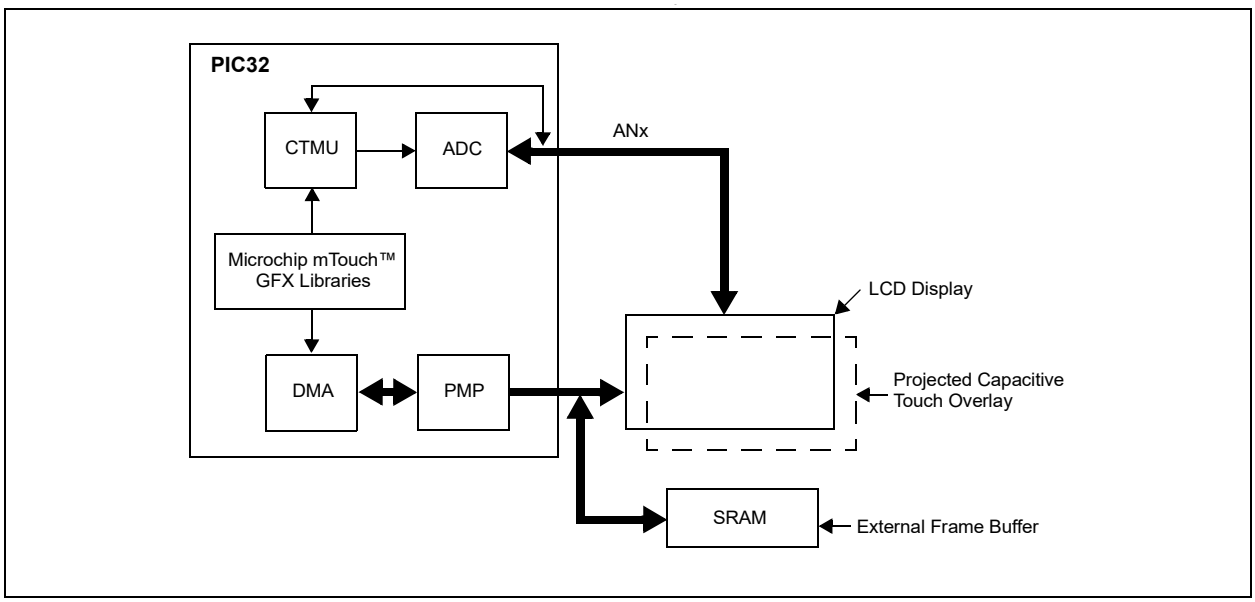
FIGURE 2-12: LOW-COST CONTROLLERLESS (LCC) GRAPHICS APPLICATION WITH PROJECTED CAPACITIVE TOUCH



NOTES:

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3.0 CPU

Note 1: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: The microAptiv™ CPU core resources are available at: www.imgtec.com.

The MIPS32® microAptiv™ MCU Core is the heart of the PIC32MK GP/MC family device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

Key features include:

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 5):
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions
  - Virtual memory support
- microMIPS™ compatible instruction set:
  - Improves code size density over MIPS32, while maintaining MIPS32 performance.
  - Supports all MIPS32 instructions (except branch-likely instructions)
  - Fifteen additional 32-bit instructions and 39 16-bit instructions corresponding to commonly-used MIPS32 instructions
  - Stack pointer implicit in instruction
  - MIPS32 assembly and ABI compatible
- Autonomous Multiply/Divide Unit (MDU):
  - Maximum issue rate of one 32x32 multiply per clock
  - Early-in iterative divide. Minimum 12 and maximum 38 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control:
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace:
  - Support for single stepping
  - Virtual instruction and data address/value breakpoints
  - Hardware breakpoint supports both address match and address range triggering.
  - Eight instruction and four data complex breakpoints
- iFlowtrace® version 2.0 support:
  - Real-time instruction program counter
  - Special events trace capability
  - Two performance counters with 34 user-selectable countable events
  - Disabled if the processor enters Debug mode
  - Program Counter sampling
- DSP ASE Extension:
  - Native fractional format data type operations
  - Register Single Instruction Multiple Data (SIMD) operations (add, subtract, multiply, shift)
  - GPR-based shift
  - Bit manipulation
  - Compare-Pick
  - DSP Control Access
  - Indexed-Load
  - Branch
  - Multiplication of complex operands
  - Variable bit insertion and extraction
  - Virtual circular buffers
  - Arithmetic saturation and overflow handling
  - Zero-cycle overhead saturation and rounding operations
- Floating Point Unit (FPU):
  - 1985 IEEE-754 compliant Floating Point Unit
  - Supports single and double precision datatypes
  - 2008 IEEE-754 compatibility control of NaN handling and Abs/Neg instructions
  - Runs at 1:1 core/FPU clock ratio

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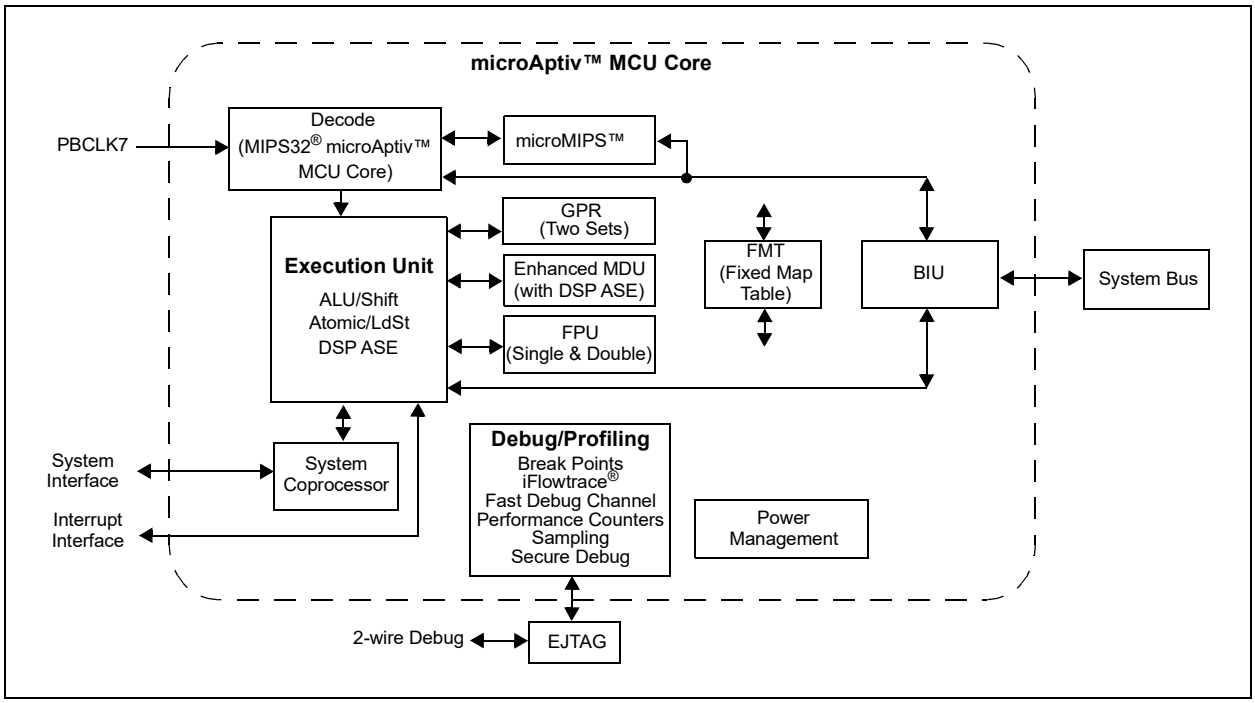
A block diagram of the PIC32MK GP/MC family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MK GP/MC FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



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3.1 Architecture Overview

The MIPS32 microAptiv MCU core in the PIC32MK GP/MC family devices contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System control coprocessor (CP0)
- Floating Point Unit (FPU)
- Power Management
- microMIPS support
- Enhanced JTAG (EJTAG) controller

3.1.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow sets (containing thirty-two registers) are added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Trap condition comparator
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner
- DSP ALU and logic block for performing DSP instructions, such as arithmetic/shift/compare operations

3.1.2 MULTIPLY/DIVIDE UNIT (MDU)

The processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations, and DSP ASE multiply instructions. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 Booth recoded multiplier, a pair of result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown (‘32’ of 32x16) represents the rs operand. The second number ‘16’ of 32x16) represents the *rt* operand.

The MDU supports execution of one multiply or multiply-accumulate operation every clock cycle.

Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent `MDU` instruction while a divide is still active causes an IU pipeline stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the processor core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MIPS32® microAptiv™ MCU CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU, MADD/MADDU, MSUB/MSUBU` (HI/LO destination)	16 bits	5	1
	32 bits	5	1
`MUL` (GPR destination)	16 bits	5	1
	32 bits	5	1
`DIV/DIVU`	8 bits	12/14	12/14
	16 bits	20/22	20/22
	24 bits	28/30	28/30
	32 bits	36/38	36/38

The MIPS architecture defines that the result of a multiply or divide operation be placed in one of four pairs of HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

The MDU also implements various shift instructions operating on the HI/LO register and multiply instructions as defined in the DSP ASE. The MDU supports all of the data types required for this purpose and includes three extra HI/LO registers as defined by the ASE.

Table 3-2 lists the latencies and repeat rates for the DSP multiply and dot-product operations. The approximate latencies and repeat rates are listed in terms of pipeline clocks.

TABLE 3-2: DSP-RELATED LATENCIES AND REPEAT RATES

Op code	Latency	Repeat Rate
Multiply and dot-product without saturation after accumulation	5	1
Multiply and dot-product with saturation after accumulation	5	1
Multiply without accumulation	5	1

3.1.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as the presence of options like microMIPS is also available by accessing the CP0 registers, listed in Table 3-3.

TABLE 3-3: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MK GP Family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers in Non-privileged mode.
8	BadVAddr	Reports the address for the most recent address-related exception.
	BadInstr	Reports the instruction that caused the most recent exception.
	BadInstrP	Reports the branch instruction if a delay slot caused the most recent exception.
9	Count	Processor cycle count.
10	Reserved	Reserved in the PIC32MK GP Family core.
11	Compare	Core timer interrupt control.
12	Status	Processor status and control.
	IntCtl	Interrupt control of vector spacing.
	SRSCtl	Shadow register set control.
	SRSMap	Shadow register mapping control.
	View_IPL	Allows the Priority Level to be read/written without extracting or inserting that bit from/to the Status register.
	SRSMAP2	Contains two 4-bit fields that provide the mapping from a vector number to the shadow set number to use when servicing such an interrupt.
13	Cause	Describes the cause of the last exception.
	NestedExc	Contains the error and exception level status bit values that existed prior to the current exception.
	View_RIPL	Enables read access to the RIPL bit that is available in the Cause register.
14	EPC	Program counter at last exception.
	NestedEPC	Contains the exception program counter that existed prior to the current exception.

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TABLE 3-3: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	Reserved	Reserved in the PIC32MK GP Family core.
18	Reserved	Reserved in the PIC32MK GP Family core.
19	Reserved	Reserved in the PIC32MK GP Family core.
20-22	Reserved	Reserved in the PIC32MK GP Family core.
23	Debug	EJTAG debug register.
	TraceControl	EJTAG trace control.
	TraceControl2	EJTAG trace control 2.
	UserTraceData1	EJTAG user trace data 1 register.
	TraceBPC	EJTAG trace breakpoint register.
	Debug2	Debug control/exception status 1.
24	DEPC	Program counter at last debug exception.
	UserTraceData2	EJTAG user trace data 2 register.
25	PerfCtl0	Performance counter 0 control.
	PerfCnt0	Performance counter 0.
	PerfCtl1	Performance counter 1 control.
	PerfCnt1	Performance counter 1.
26	Reserved	Reserved in the PIC32MK GP Family core.
27	Reserved	Reserved in the PIC32MK GP Family core.
28	Reserved	Reserved in the PIC32MK GP Family core.
29	Reserved	Reserved in the PIC32MK GP Family core.
30	ErrorEPC	Program counter at last error exception.
31	DeSave	Debug exception save.

3.1.4 FLOATING POINT UNIT (FPU)

The Floating Point Unit (FPU), Coprocessor (CP1), implements the MIPS Instruction Set Architecture for floating point computation. The implementation supports the ANSI/IEEE Standard 754 (IEEE for Binary Floating Point Arithmetic) for single- and double-precision data formats. The FPU can be programmed to have thirty-two 32-bit or 64-bit floating point registers used for floating point operations.

The performance is optimized for single precision formats. Most instructions have one FPU cycle throughput and four FPU cycle latency. The FPU implements the multiply-add (MADD) and multiply-sub (MSUB) instructions with intermediate rounding after the multiply function. The result is guaranteed to be the same as executing a MUL and an ADD instruction separately, but the instruction latency, instruction fetch, dispatch bandwidth, and the total number of register accesses are improved.

IEEE denormalized input operands and results are supported by hardware for some instructions. IEEE denormalized results are not supported by hardware in general, but a fast flush-to-zero mode is provided to optimize performance. The fast flush-to-zero mode is enabled through the FCCR register, and use of this mode is recommended for best performance when denormalized results are generated.

The FPU has a separate pipeline for floating point instruction execution. This pipeline operates in parallel with the integer core pipeline and does not stall when the integer pipeline stalls. This allows long-running FPU operations, such as divide or square root, to be partially masked by system stalls and/or other integer unit instructions. Arithmetic instructions are always dispatched and completed in order, but loads and stores can complete out of order. The exception model is “precise” at all times.

Table 3-4 contains the floating point instruction latencies and repeat rates for the processor core. In this table, 'Latency' refers to the number of FPU cycles necessary for the first instruction to produce the result needed by the second instruction. The “Repeat Rate” refers to the maximum rate at which an instruction can be executed per FPU cycle.

TABLE 3-4: FPU INSTRUCTION LATENCIES AND REPEAT RATES

Op code	Latency (FPU Cycles)	Repeat Rate (FPU Cycles)
ABS.[S,D], NEG.[S,D], ADD.[S,D], SUB.[S,D], C.cond.[S,D], MUL.S	4	1
MADD.S, MSUB.S, NMADD.S, NMSUB.S, CABS.cond.[S,D]	4	1
CVT.D.S, CVT.PS.PW, CVT.[S,D].[W,L]	4	1
CVT.S.D, CVT.[W,L].[S,D], CEIL.[W,L].[S,D], FLOOR.[W,L].[S,D], ROUND.[W,L].[S,D], TRUNC.[W,L].[S,D]	4	1
MOV.[S,D], MOVF.[S,D], MOVN.[S,D], MOVT.[S,D], MOVZ.[S,D]	4	1
MUL.D	5	2
MADD.D, MSUB.D, NMADD.D, NMSUB.D	5	2
RECIP.S	13	10
RECIP.D	26	21
RSQRT.S	17	14
RSQRT.D	36	31
DIV.S, SQRT.S	17	14
DIV.D, SQRT.D	32	29
MTC1, DMTC1, LWC1, LDC1, LDXC1, LUXC1, LWXC1	4	1
MFC1, DMFC1, SWC1, SDC1, SDXC1, SUXC1, SWXC1	1	1

Legend: S = Single D = Double
W = Word L = Long word

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The FPU implements a high-performance 7-stage pipeline:

- Decode, register read and unpack (FR stage)
- Multiply tree - double pumped for double (M1 stage)
- Multiply complete (M2 stage)
- Addition first step (A1 stage)
- Addition second and final step (A2 stage)
- Packing to IEEE format (FP stage)
- Register writeback (FW stage)

The FPU implements a bypass mechanism that allows the result of an operation to be forwarded directly to the instruction that needs it without having to write the result to the FPU register and then read it back.

Table 3-5 lists the Coprocessor 1 Registers for the FPU.

TABLE 3-5: FPU (CP1) REGISTERS

Register Number	Register Name	Function
0	FIR	Floating Point implementation register. Contains information that identifies the FPU.
25	FCCR	Floating Point condition codes register.
26	FEXR	Floating Point exceptions register.
28	FENR	Floating Point enables register.
31	FCSR	Floating Point Control and Status register.

3.2 Power Management

The processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during Idle periods.

3.2.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the `WAIT` instruction. For more information on power management, see **32.0 "Power-Saving Features"**.

3.2.2 LOCAL CLOCK GATING

The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MK family makes extensive use of local gated-clocks to reduce this dynamic power consumption.

3.3 EJTAG Debug Support

The processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the processor core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (`DERET`) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification specify which registers are selected and how they are used.

3.4 MIPS DSP ASE Extension

The MIPS DSP Application-Specific Extension Revision 2 is an extension to the MIPS32 architecture. This extension comprises new integer instructions and states that include new HI/LO accumulator register pairs and a DSP control register. This extension is crucial in a wide range of DSP, multimedia, and DSP-like algorithms covering Audio and Video processing applications. The extension supports native fractional format data type operations, register Single Instruction Multiple Data (SIMD) operations, such as add, subtract, multiply, and shift. In addition, the extension includes the following features that are essential in making DSP algorithms computationally efficient:

- Support for multiplication of complex operands
- Variable bit insertion and extraction
- Implementation and use of virtual circular buffers
- Arithmetic saturation and overflow handling support
- Zero cycle overhead saturation and rounding operations

3.5 microMIPS ISA

The processor core supports the microMIPS ISA, which contains all MIPS32 ISA instructions (except for branch-likely instructions) in a new 32-bit encoding scheme, with some of the commonly used instructions also available in 16-bit encoded format. This ISA improves code density through the additional 16-bit instructions while maintaining a performance similar to MIPS32 mode. In microMIPS mode, 16-bit or 32-bit instructions will be fetched and recoded to legacy MIPS32 instruction opcodes in the pipeline's I stage, so that the processor core can have the same microAptiv MPU microarchitecture. Because the microMIPS instruction stream can be intermixed with 16-bit halfword or 32-bit word size instructions on halfword or word boundaries, additional logic is in place to address the word misalignment issues, thus minimizing performance loss.

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3.6 MIPS32® microAptiv™ MCU Core Configuration

Register 3-1 through Register 3-5 show the default configuration of the MIPS32 microAptiv MCU core, which is included on the PIC32MK GP/MC family of devices.

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	ISP
23:16	R-0	R-0	R-1	R-0	U-0	R-1	R-0	R-0
	DSP	UDI	SB	MDU	—	MM<1:0>		BM
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-1
	BE	AT<1:0>		AR<2:0>			U-0	U-0
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	—	—
	—	—	—	—	—	K0<2:0>		

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the Config1 register.

bit 30-25 **Unimplemented:** Read as '0'

bit 24 **ISP:** Instruction Scratch Pad RAM bit
0 = Instruction Scratch Pad RAM is not implemented

bit 23 **DSP:** Data Scratch Pad RAM bit
0 = Data Scratch Pad RAM is not implemented

bit 22 **UDI:** User-defined bit
0 = CorExtend User-Defined Instructions are not implemented

bit 21 **SB:** SimpleBE bit
1 = Only Simple Byte Enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit
0 = Fast, high-performance MDU

bit 19 **Unimplemented:** Read as '0'

bit 18-17 **MM<1:0>:** Merge Mode bits
10 = Merging is allowed

bit 16 **BM:** Burst Mode bit
0 = Burst order is sequential

bit 15 **BE:** Endian Mode bit
0 = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits
00 = MIPS32

bit 12-10 **AR<2:0>:** Architecture Revision Level bits
001 = MIPS32 Release 2

bit 9-3 **Unimplemented:** Read as '0'

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

bit 2-0 **K0<2:0>:** Kseg0 Coherency Algorithm bits
000 = Reserved
001 = Reserved
010 = Instruction Prefetch uncached (Default)
011 = Instruction Prefetch cached (Recommended)
100 = Reserved
•
•
•
111 = Reserved

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REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R-0	R-0	R-0	R-0	R-0	R-0	U-0
	—	MMUSIZE<5:0>						—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-1	R-1	R-0	R-1	R-1
	—	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to a '1' to indicate the presence of the Config2 register.

bit 30-25 **MMUSIZE<5:0>:** MMU Size bits

Note: This bit field is read as '0' decimal in the fixed table-based MMU core, as no TLB is present.

bit 24-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit
1 = The processor core contains Performance Counters

bit 3 **WR:** Watch Register Presence bit
1 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating Point Unit bit
1 = Floating Point Unit is present

REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R/W-y
	—	IPLW<1:0>		MMAR<2:0>			MCU	ISAONEXC(1)
15:8	R-y	R-y	R-1	R-1	R-1	R-1	U-0	R-1
	ISA<1:0>(1)		ULRI	RXI	DSP2P	DSPP	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-0
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired as '1' to indicate the presence of the Config4 register

bit 30-23 **Unimplemented:** Read as '0'

bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8-bits in width

bit 20-18 **MMAR<2:0>:** microMIPS Architecture Revision Level bits
000 = Release 1

bit 17 **MCU:** MIPS® MCU™ ASE Implemented bit
1 = MCU ASE is implemented

bit 16 **ISAONEXC:** ISA on Exception bit(1)
1 = microMIPS is used on entrance to an exception vector
0 = MIPS32 ISA is used on entrance to an exception vector

bit 15-14 **ISA<1:0>:** Instruction Set Availability bits(1)
11 = Both MIPS32 and microMIPS are implemented; microMIPS is used when coming out of reset
10 = Both MIPS32 and microMIPS are implemented; MIPS32 ISA used when coming out of reset

bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented

bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented

bit 11 **DSP2P:** MIPS DSP ASE Revision 2 Presence bit
1 = DSP Revision 2 is present

bit 10 **DSPP:** MIPS DSP ASE Presence bit
1 = DSP is present

bit 9 **Unimplemented:** Read as '0'

bit 8 **ITL:** Indicates that iFlowtrace® hardware is present
1 = The iFlowtrace® 2.0 hardware is implemented in the core

bit 7 **Unimplemented:** Read as '0'

bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented.

bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented

bit 4 **SP:** Small Page bit
0 = 4 KB page size

bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented

Note 1: These bits are set based on the value of the BOOTISA Configuration bit (DEVCFG0<6>).

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REGISTER 3-4: CONFIG4: CONFIGURATION REGISTER 4; CP0 REGISTER 16, SELECT 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	M	—	—	—	—	—	—	—
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	KScr Exist<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	—	—	—

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **M:** Config5 Register Present bit
1 = Config5 register is present
0 = Config5 register is not present

bit 30-24 **Unimplemented:** Read as '0'

bit 23-16 **KScr Exist<7:0>:** Number of Scratch Registers Available to Kernel Mode bits
Indicates how many scratch registers are available to Kernel mode software within CP0 Register 31. Each bit represents a select for Coprocessor0 Register 31. Bit 16 represents Select 0. Bit 23 represents Select 7. If the bit is set, the associated scratch register is implemented and is available for Kernel mode software.

Note: These bits are read-only, and this field is all zeros on these products, as is read as '0'.

bit 15-0 **Reserved:** Read/write as '0'

REGISTER 3-5: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend:	r = Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

REGISTER 3-6: CONFIG7: CONFIGURATION REGISTER 7; CP0 REGISTER 16, SELECT 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	WII	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **WII:** Wait IE Ignore bit

1 = Indicates that this processor will allow an interrupt to unblock a WAIT instruction

bit 30-0 **Unimplemented:** Read as '0'

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REGISTER 3-7: FIR: FLOATING POINT IMPLEMENTATION REGISTER; CP1 REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-1	U-0	U-0	U-0	R-1
	—	—	—	UFRP	—	—	—	FC
23:16	R-1	R-1	R-1	R-1	R-0	R-0	R-1	R-1
	HAS2008	F64	L	W	MIPS3D	PS	D	S
15:8	R-1	R-0	R-1	R-0	R-0	R-1	R-1	R-1
	PRID<7:0>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	REVISION<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **UFRP:** User Mode FR Switching Instruction bit
1 = User mode FR switching instructions are supported
0 = User mode FR switching instructions are not supported

bit 27-25 **Unimplemented:** Read as '0'

bit 24 **FC:** Full Convert Ranges bit
1 = Full convert ranges are implemented (all numbers can be converted to another type by the FPU)
0 = Full convert ranges are not implemented

bit 23 **HAS008:** IEEE-754-2008 bit
1 = MAC2008, ABS2008, NAN2008 bits exist within the FCSR register
0 = MAC2009, ABS2008, and NAN2008 bits do not exist within the FCSR register

bit 22 **F64:** 64-bit FPU bit
1 = This is a 64-bit FPU
0 = This is not a 64-bit FPU

bit 21 **L: L**ong Fixed Point Data Type bit
1 = Long fixed point data types are implemented
0 = Long fixed point data types are not implemented

bit 20 **W:** Word Fixed Point data type bit
1 = Word fixed point data types are implemented
0 = Word fixed point data types are not implemented

bit 19 **MIPS3D:** MIPS-3D ASE bit
1 = MIPS-3D is implemented
0 = MIPS-3D is not implemented

bit 18 **PS:** Paired Single Floating Point data bit
1 = PS floating point is implemented
0 = PS floating point is not implemented

bit 17 **D:** Double-precision floating point data bit
1 = Double-precision floating point data types are implemented
0 = Double-precision floating point data types are not implemented

bit 16 **S:** Single-precision Floating Point Data bit
1 = Single-precision floating point data types are implemented
0 = Single-precision floating point data types are not implemented

bit 15-8 **PRID<7:0>:** Processor Identification bits
These bits allow software to distinguish between the various types of MIPS processors. For PIC32 devices with the MIPS32 microAptiv MCU core, this value is 0x9D.

bit 7-0 **REVISION<7:0>:** Processor Revision Identification bits
These bits allow software to distinguish between one revision and another of the same processor type. This number is increased on major revisions of the processor core

REGISTER 3-8: FCCR: FLOATING POINT CONDITION CODES REGISTER; CP1 REGISTER 25

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	FCC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FCC<7:0>:** Floating Point Condition Code bits

These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

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REGISTER 3-9: FEXR: FLOATING POINT EXCEPTIONS STATUS REGISTER; CP1 REGISTER 26

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
	—	—	—	—	—	—	CAUSE<5:4>	
							E	V
15:8	R/W-x	R/W-x	R/W-x	U-0	U-0	U-0	U-0	U-0
	CAUSE<3:0>				—	—	—	—
	Z	O	U	I				
7:0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	U-0	U-0
	—	FLAGS<4:0>					—	—
		V	Z	O	U	I		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-18 **Unimplemented:** Read as '0'

bit 17-12 **CAUSE<5:0>:** FPU Exception Cause bits
These bits indicated the exception conditions that arise during execution of an FPU arithmetic instruction.

bit 17 **E:** Unimplemented Operation bit

bit 16 **V:** Invalid Operation bit

bit 15 **Z:** Divide-by-Zero bit

bit 14 **O:** Overflow bit

bit 13 **U:** Underflow bit

bit 12 **I:** Inexact bit

bit 11-7 **Unimplemented:** Read as '0'

bit 6-2 **FLAGS<4:0>:** FPU Flags bits
These bits show any exception conditions that have occurred for completed instructions since the flag was last reset by software.

bit 6 **V:** Invalid Operation bit

bit 4 **Z:** Divide-by-Zero bit

bit 4 **O:** Overflow bit

bit 3 **U:** Underflow bit

bit 2 **I:** Inexact bit

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 3-10: FENR: FLOATING POINT EXCEPTIONS AND MODES ENABLE REGISTER; CP1 REGISTER 28

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	ENABLES<4:1>			
					V	Z	O	U
7:0	R/W-x	U-0	U-0	U-0	U-0	R-x	R/W-x	R/W-x
	ENABLES<0>	—	—	—	—	FS	RM<1:0>	
	I							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-7 **ENABLES<4:0>:** FPU Exception Enable bits

These bits control whether or not a trap is taken when an IEEE exception condition occurs for any of the five conditions. The trap occurs when both an enable bit and its corresponding cause bit are set either during an FPU arithmetic operation or by moving a value to the FCSR or one of its alternative representations.

bit 11 **V:** Invalid Operation bit

bit 10 **Z:** Divide-by-Zero bit

bit 9 **O:** Overflow bit

bit 8 **U:** Underflow bit

bit 7 **I:** Inexact bit

bit 6-3 **Unimplemented:** Read as '0'

bit 2 **FS:** Flush to Zero control bit

1 = Denormal input operands are flushed to zero. Tiny results are flushed to either zero or the applied format's smallest normalized number (MinNorm) depending on the rounding mode settings.

0 = Denormal input operands result in an Unimplemented Operation exception.

bit 1-0 **RM<1:0>:** Rounding Mode control bits

11 = Round towards Minus Infinity ($-\infty$)
10 = Round towards Plus Infinity ($+\infty$)
01 = Round toward Zero (0)
00 = Round to Nearest

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REGISTER 3-11: FCSR: FLOATING POINT CONTROL AND STATUS REGISTER; CP1 REGISTER 31

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	FCC<7:1>							FS
23:16	R/W-x	R/W-x	R/W-x	R-0	R-1	R-1	R/W-x	R/W-x
	FCC<0>	FO	FN	MAC2008	ABS2008	NAN2008	CAUSE<5:4>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CAUSE<3:0>				ENABLES<4:1>			
					V	Z	O	U
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	ENABLES<0>	FLAGS<4:0>					RM<1:0>	
	I	V	Z	O	U	I		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **FCC<7:1>:** Floating Point Condition Code bits
These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

bit 24 **FS:** Flush to Zero control bit
1 = Denormal input operands are flushed to zero. Tiny results are flushed to either zero or the applied format's smallest normalized number (MinNorm) depending on the rounding mode settings.
0 = Denormal input operands result in an Unimplemented Operation exception.

bit 23 **FCC<0>:** Floating Point Condition Code bits
These bits record the results of floating point compares and are tested for floating point conditional branches and conditional moves.

bit 22 **FO:** Flush Override Control bit
1 = The intermediate result is kept in an internal format, which can be perceived as having the usual mantissa precision but with unlimited exponent precision and without forcing to a specific value or taking an exception.
0 = Handling of Tiny Result values depends on setting of the FS bit.

bit 21 **FN:** Flush to Nearest Control bit
1 = Final result is rounded to either zero or 2E_min (MinNorm), whichever is closest when in Round to Nearest (RN) rounding mode. For other rounding modes, a final result is given as if FS was set to 1.
0 = Handling of Tiny Result values depends on setting of the FS bit.

bit 20 **MAC2008:** Fused Multiply Add mode control bit
0 = Unfused multiply-add. Intermediary multiplication results are rounded to the destination format.

bit 19 **ABS2008:** Absolute value format control bit
1 = ABS.fmt and NEG.fmt instructions compliant with IEEE Standard 754-2008. The ABS and NEG functions accept QNAN inputs without trapping.

bit 18 **NAN2008:** NaN Encoding control bit
1 = Quiet and signaling NaN encodings recommended by the IEEE Standard 754-2008. A quiet NaN is encoded with the first bit of the fraction being 1 and a signaling NaN is encoded with the first bit of the fraction being 0.

bit 17-12 **CAUSE<5:0>:** FPU Exception Cause bits
These bits indicated the exception conditions that arise during execution of an FPU arithmetic instruction.

REGISTER 3-11: FCSR: FLOATING POINT CONTROL AND STATUS REGISTER; CP1 REGISTER 31

bit 17 **E:** Unimplemented Operation bit

bit 16 **V:** Invalid Operation bit

bit 15 **Z:** Divide-by-Zero bit

bit 14 **O:** Overflow bit

bit 13 **U:** Underflow bit

bit 12 **I:** Inexact bit

bit 11-7 **ENABLES<4:0>:** FPU Exception Enable bits
These bits control whether or not a trap is taken when an IEEE exception condition occurs for any of the five conditions. The trap occurs when both an enable bit and its corresponding cause bit are set either during an FPU arithmetic operation or by moving a value to the FCSR or one of its alternative representations.

bit 11 **V:** Invalid Operation bit

bit 10 **Z:** Divide-by-Zero bit

bit 9 **O:** Overflow bit

bit 8 **U:** Underflow bit

bit 7 **I:** Inexact bit

bit 6-2 **FLAGS<4:0>:** FPU Flags bits
These bits show any exception conditions that have occurred for completed instructions since the flag was last reset by software.

bit 6 **V:** Invalid Operation bit

bit 5 **Z:** Divide-by-Zero bit

bit 4 **O:** Overflow bit

bit 3 **U:** Underflow bit

bit 2 **I:** Inexact bit

bit 1-0 **RM<1:0>:** Rounding Mode control bits
11 = Round towards Minus Infinity (− ∞)
10 = Round towards Plus Infinity (+ ∞)
01 = Round toward Zero (0)
00 = Round to Nearest

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4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. For detailed information, refer to **Section 48. "Memory Organization and Permissions"** (DS60001214), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MK GP/MC microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs) and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, PIC32MK GP/MC devices allow execution from data memory.

Key features of this module include:

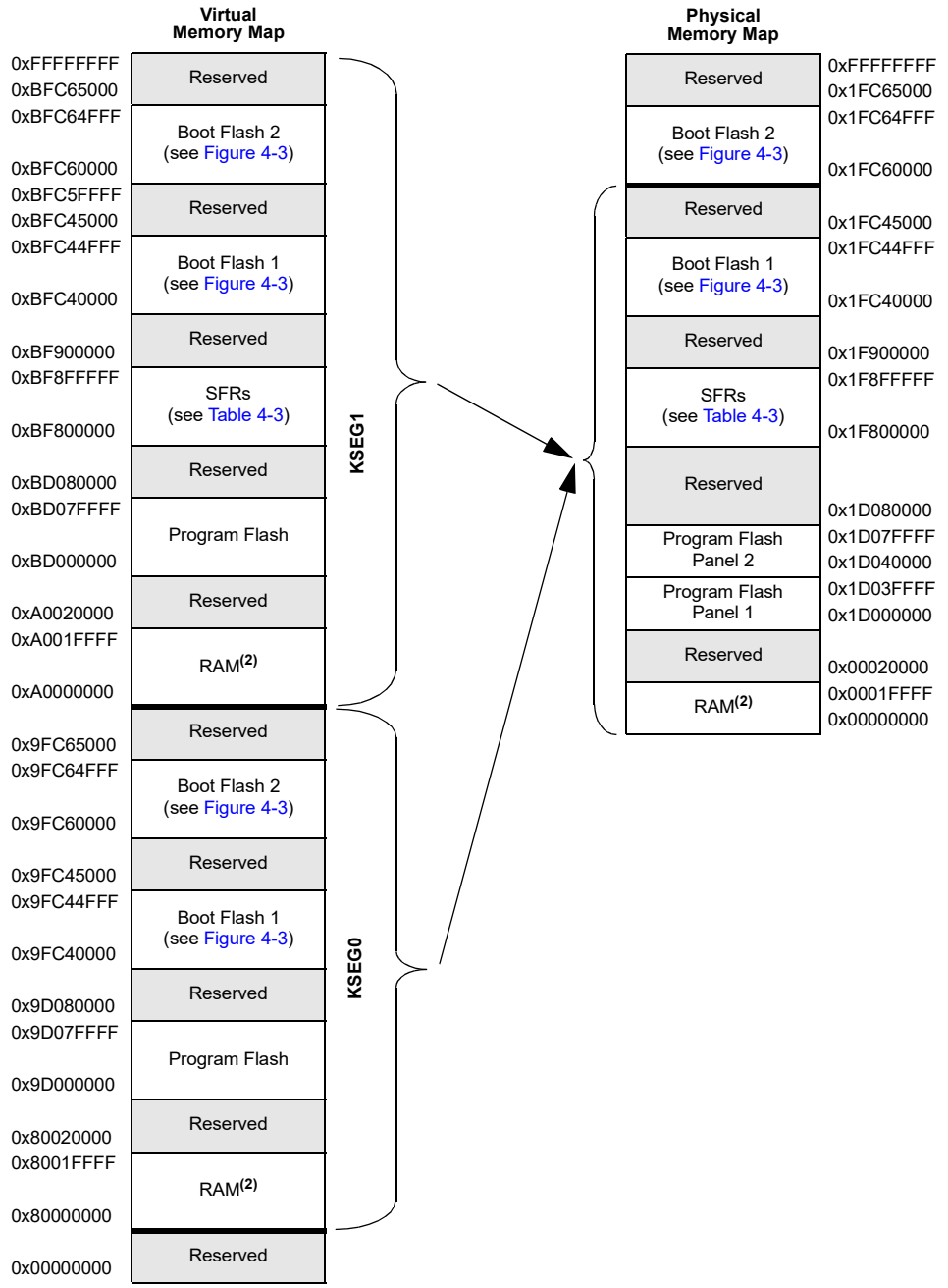
- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/ KSEG1) mode address space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Read/write permission access to predefined memory regions

4.1 Memory Layout

PIC32MK GP/MC microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The main memory maps for the PIC32MK GP/MC devices are illustrated in Figure 4-1 through Figure 4-2. Figure 4-3 provides memory map information for boot Flash and boot alias. Table 4-3 provides memory map information for SFRs.

FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 512 KB PROGRAM MEMORY AND 128 KB RAM



Note 1: Memory areas are not shown to scale.

2: RAM memory is divided into two equal banks: RAM Bank 1 and RAM Bank 2 on a half boundary.

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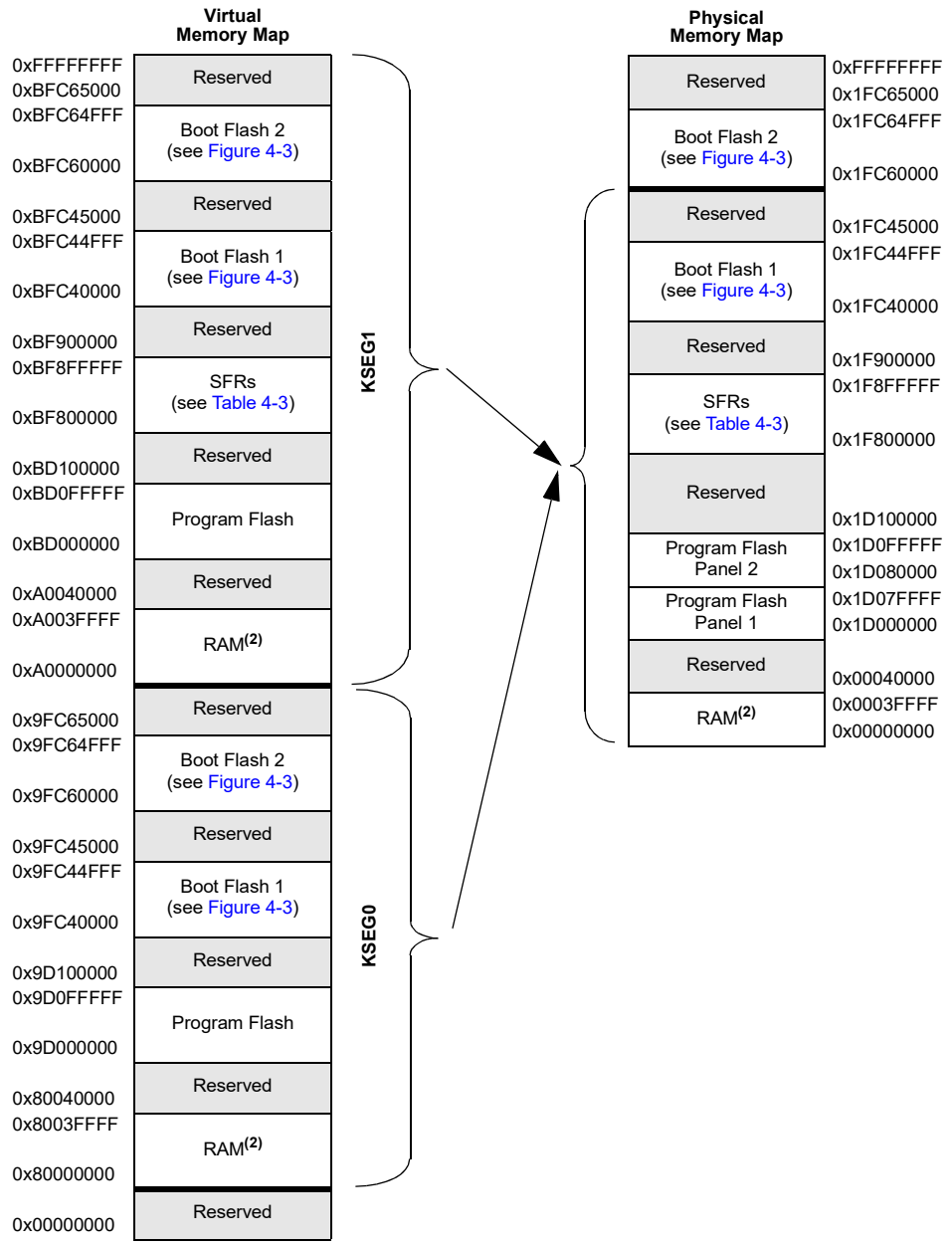
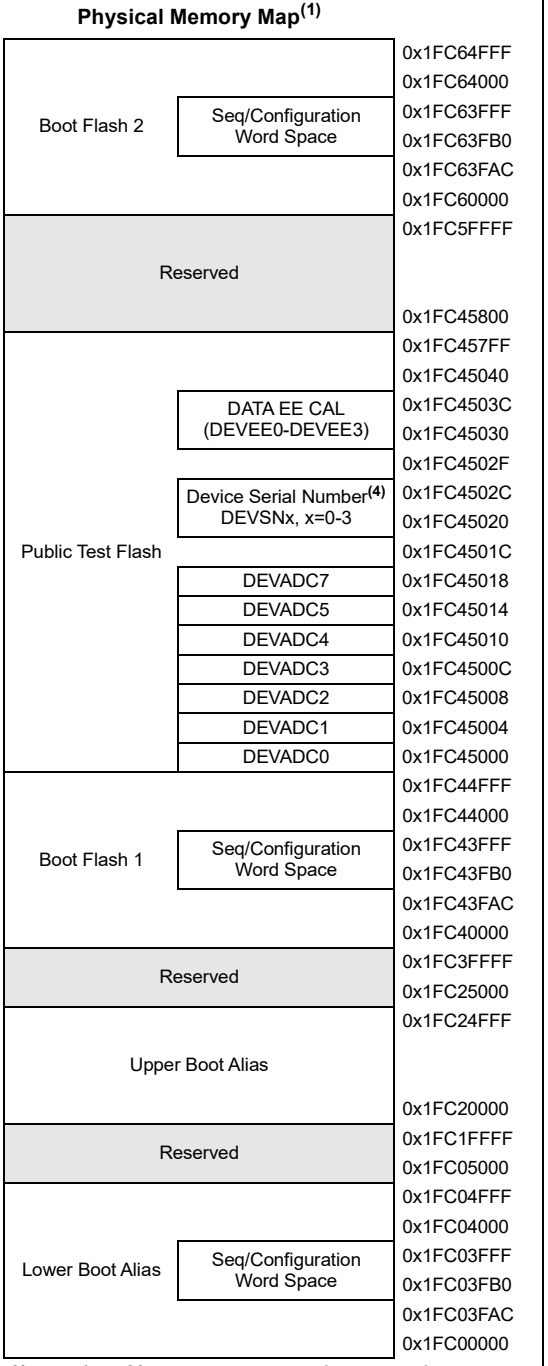
FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 1024 KB PROGRAM MEMORY AND 256 KB RAM



Note 1: Memory areas are not shown to scale.

2: RAM memory is divided into two equal banks: RAM Bank 1 and RAM Bank 2 on a half boundary.

FIGURE 4-3: BOOT AND ALIAS MEMORY MAP



Note 1: Memory areas are not shown to scale.
2: Memory locations 0x1FC03FB0 through 0x1FC03FFC are used to initialize Configuration registers (see **33.0 "Special Features"**).
3: Refer to **4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.
4: Memory locations 0x1FC5020 and 0x1FC502C contain a unique device serial number (see **33.0 "Special Features"**).
5: This configuration space cannot be used for executing code in the upper Boot Alias.

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
CFG-PMD	0xBF800000	0x0000
CACHE		0x0800
FC-NVM		0x0A00
WDT		0x0C00
DMT		0x0E00
ICD		0x1000
CRU		0x1200
PPS		0x1400
PLVD		0x1800
EVIC	0xBF810000	0x0000
DMA		0x1000
Timer1-Timer9	0xBF820000	0x0000
IC1-IC9		0x2000
OC1-OC9		0x4000
I2C1-I2C2		0x6000
SPI1-SPI2		0x7000
UART1-UART2		0x8000
DATAEE		0x9000
PWM1-PWM12		0xA000
QEI1-QEI6		0xB200
CMP		0xC000
CDAC1		0xC200
CTMU		0xD000
PMP		0xE000
IC10-IC16	0xBF840000	0x3200
OC10-OC16		0x5200
I2C3-I2C4		0x6400
SPI3-SPI6		0x7400
UART3-UART6		0x8400
CDAC2-CDAC3		0xC400
PORTA-PORTG	0xBF860000	0x0000
CAN1-CAN4	0xBF880000	0x0000
ADC		0x7000
USB1-USB2		0x9000
RTCC	0xBF8C0000	0x0000
Deep Sleep		0x0200
SSX CTL	0xBF8F0000	0x0000

Note 1: Refer to **4.2 "System Bus Arbitration"** for important legal information.

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4.1.1 BOOT FLASH SEQUENCE AND CONFIGURATION SPACES

Sequence space is used to identify which boot Flash is aliased by aliased regions. If the value programmed into the TSEQ<15:0> bits of the BF1SEQ word is equal to or greater than the value programmed into the TSEQ<15:0> bits of the BF2SEQ word, Boot Flash 1 is aliased by the lower boot alias region, and Boot Flash 2 is aliased by the upper boot alias region. If the TSEQ<15:0> bits of the BF2SEQ word is greater than the TSEQ<15:0> bits of the BF1SEQ word, the opposite is true (see Table 4-2 and Table 4-3 for BFxSEQ word memory locations).

Once boot Flash memories are aliased, configuration space located in the lower boot alias region is used as the basis for the Configuration words, DEVSIGN0, DEVCP0, and DEVCFGx. This means that the boot Flash region to be aliased by lower boot alias region memory must contain configuration values in the appropriate memory locations.

Note:	Use only Quad Word program operation (NVMOP<3:0> = `0010`) when programming data into the sequence and configuration spaces.

TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits															All Reset
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3FC0	BF1DEVCFG3	31:0	**Note:** See Table 33-1 for the bit descriptions.																xxxx
3FC4	BF1DEVCFG2	31:0																	xxxx
3FC8	BF1DEVCFG1	31:0																	xxxx
3FCC	BF1DEVCFG0	31:0																	xxxx
3FDC	BF1DEVCP	31:0																	xxxx
3FEC	BF1DEVSIGN	31:0																	xxxx
3FF0	BF1SEQ	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 4-3: BOOT FLASH 2 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC6_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3FC0	BF2DEVCFG3	31:0	**Note:** See Table 33-1 for the bit descriptions.																xxxx
3FC4	BF2DEVCFG2	31:0																	xxxx
3FC8	BF2DEVCFG1	31:0																	xxxx
3FCC	BF2DEVCFG0	31:0																	xxxx
3FDC	BF2DEVCP	31:0																	xxxx
3FEC	BF2DEVSIGN	31:0																	xxxx
3FF0	BF2SEQ	31:16	CSEQ<15:0>																xxxx
		15:0	TSEQ<15:0>																xxxx

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

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REGISTER 4-1: BFxSEQ: BOOT FLASH 'x' SEQUENCE REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<7:0>							
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CSEQ<15:0>:** Boot Flash Complement Sequence Number bits

bit 15-0 **TSEQ<15:0>:** Boot Flash True Sequence Number bits

4.2 System Bus Arbitration

Note: The System Bus interconnect implements one or more instantiations of the SonicsSX® interconnect from Sonics, Inc. This document contains materials that are (c) 2003-2015 Sonics, Inc., and that constitute proprietary information of Sonics, Inc. SonicsSX is a registered trademark of Sonics, Inc. All such materials and trademarks are used under license from Sonics, Inc.

As shown in the PIC32MK GP/MC Family Block Diagram (see Figure 1-1), there are multiple initiator modules (I1 through I13) in the system that can access various target modules (T1 through T14). Table 4-4 illustrates which initiator can access which target. The System Bus supports simultaneous access to targets by initiators, so long as the initiators are accessing different targets. The System Bus will perform arbitration, if multiple initiators attempt to access the same target.

TABLE 4-4: INITIATORS TO TARGETS ACCESS ASSOCIATION

Target #	Initiator ID:	1	2	3	4	5	6	7	8	9	10	11	12	13
	Name:	CPU IS	CPU ID	DMA Read	DMA Write	Flash	ICD JTAG	ADC Mem.	USB1	USB2	CAN1	CAN2	CAN3	CAN4
1	Program Flash	X		X										
2	Data		X											
3	Peripheral Module			X			X		X	X	X	X	X	X
4	RAM Bank 1	X	X	X	X	X	X	X	X	X	X	X	X	X
5	RAM Bank 2	X	X	X	X	X	X	X	X	X	X	X	X	X
7	**Peripheral Bus 1:** DMT, CVR, PPS Input, PPS Output, WDT						X							
8	**Peripheral Bus 2:** Timer1-Timer9, I2C1-I2C2, SPI1-SPI2, UART1-UART2, CDAC1, OC1-OC9, IC1-IC9, PMP, Comparator 1-Comparator 5, Op amp 1-Op amp 4 PWM1-PWM12 QEI1-QEI6		X	X	X		X							
9	**Peripheral Bus 3:** IC10-IC16, OC10-OC16, SPI3-SPI6, I2C3-I2C4, UART3-UART6, CDAC2-CDAC3		X	X	X		X							
10	**Peripheral Bus 4:** PORTA-PORTG		X	X	X		X							
11	**Peripheral Bus 5:** USB1-USB2, CAN1-CAN4 ADC		X				X							
14	**Peripheral Bus 6:** DSCON, RTCC		X				X							

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The System Bus arbitration scheme implements a non-programmable, Least Recently Serviced (LRS) priority, which provides Quality Of Service (QOS) for most initiators. However, some initiators can use Fixed High Priority (HIGH) arbitration to guarantee their access to data.

The arbitration scheme for the available initiators is shown in Table 4-5.

TABLE 4-5: INITIATOR ID AND QOS

Name	ID	QOS
CPU-IS	1	LRS
CPU-DS	2	LRS
DMA Read	3	LRS
DMA Write	4	LRS
Flash Controller	5	HIGH
ICD-JTAG	6	LRS
ADC	7	LRS
USB1	8	LRS
USB2	9	LRS
CAN1	10	LRS
CAN2	11	LRS
CAN3	12	LRS
CAN4	13	LRS

4.3 Permission Access and System Bus Registers

The System Bus on PIC32MK GP/MC family of microcontrollers provides access control capabilities for the transaction initiators on the System Bus.

The System Bus divides the entire memory space into fourteen target regions and permits access to each target by initiators through permission groups. Four Permission Groups (0 through 3) can be assigned to each initiator. Each permission group is independent of the others and can have exclusive or shared access to a region.

Using the CFGPG register (see Register 33-8 in **33.0 "Special Features"**), Boot firmware can assign a permission group to each initiator, which can make requests on the System Bus.

The available targets and their regions, as well as the associated control registers to assign protection, are described and listed in Table 4-6.

Register 4-2 through Register 4-10 are used for setting and controlling access permission groups and regions.

To change these registers, they must be unlocked in hardware. The register lock is controlled by the PGLOCK Configuration bit (CFGCON<11>). Setting the PGLOCK bit prevents writes to the control registers and clearing the PGLOCK bit allows writes.

To set or clear the PGLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

TABLE 4-6: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS

Target Number	Target Description	SBTxREGy Register					SBTxRDy Register		SBTxWRy Register	
		Name	Region	Physical Start Address	Region Size	Priority Level	Name	Read Permission (Group3, Group2, Group1, Group0)	Name	Write Permission (Group3, Group2, Group1, Group0)
0	System Bus	SBT0REG0	Region 0	1F8F0000		0	SBT0RD0	1,1,1,1	SBT0WR0	1,1,1,1
		SBT0REG1	Region 1	1F8F8000	32 KB	3	SBT0RD1	0,0,0,1	SBT0WR1	0,0,0,1
1	Flash Memory (CPU Instruction) Program Flash Boot Flash Prefetch	SBT1REG0	Region 0	1D000000		0	SBT1RD0	1,1,1,1	SBT1WR0	0,0,0,0
		SBT1REG2	Region 2	1FC04000	4 KB	2	SBT1RD2	0,0,0,1	SBT1WR2	0,0,0,0
		SBT1REG3	Region 3	1FC24000	4 KB	2	SBT1RD3	0,0,0,1	SBT1WR3	0,0,0,0
		SBT1REG4	Region 4	1FC44000	4 KB	2	SBT1RD4	0,0,0,1	SBT1WR4	0,0,0,0
		SBT1REG5	Region 5	1FC64000	4 KB	2	SBT1RD5	0,0,0,1	SBT1WR5	0,0,0,0
2	Flash Memory (CPU data) Program Flash	SBT2REG0	Region 0	1D000000		0	SBT2RD0	1,1,1,1	SBT2WR0	0,0,0,0
		SBT2REG2	Region 2	1FC04000	4 KB	2	SBT2RD2	0,0,0,1	SBT2WR2	0,0,0,0
		SBT2REG3	Region 3	1FC24000	4 KB	2	SBT2RD3	0,0,0,1	SBT2WR3	0,0,0,0
		SBT2REG4	Region 4	1FC44000	4 KB	2	SBT2RD4	0,0,0,1	SBT2WR4	0,0,0,0
		SBT2REG5	Region 5	1FC64000	4 KB	2	SBT2RD5	0,0,0,1	SBT2WR5	0,0,0,0
3	Flash Memory (peripheral) Program Flash	SBT3REG0	Region 0	1D000000		0	SBT3RD0	1,1,1,1	SBT3WR0	0,0,0,0
		SBT3REG2	Region 2	1FC04000	4 KB	2	SBT3RD2	0,0,0,1	SBT3WR2	0,0,0,0
		SBT3REG3	Region 3	1FC24000	4 KB	2	SBT3RD3	0,0,0,1	SBT3WR3	0,0,0,0
		SBT3REG4	Region 4	1FC44000	4 KB	2	SBT3RD4	0,0,0,1	SBT3WR4	0,0,0,0
		SBT3REG5	Region 5	1FC64000	4 KB	2	SBT3RD5	0,0,0,1	SBT3WR5	0,0,0,0

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

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TABLE 4-7: SYSTEM BUS REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0510	SBFLAG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T3PGV	T2PGV	T1PGV	T0PGV	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: SYSTEM BUS TARGET 0 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8020	SBT0ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8024	SBT0ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8028	SBT0ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8030	SBT0ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8038	SBT0ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8040	SBT0REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8050	SBT0RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8058	SBT0WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8060	SBT0REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8070	SBT0RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8078	SBT0WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

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TABLE 4-9: SYSTEM BUS TARGET 1 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8420	SBT1ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8424	SBT1ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8428	SBT1ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8430	SBT1ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8438	SBT1ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8440	SBT1REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8450	SBT1RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8458	SBT1WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8480	SBT1REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8490	SBT1RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8498	SBT1WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84A0	SBT1REG3	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84B0	SBT1RD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84B8	SBT1WR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84C0	SBT1REG4	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84D0	SBT1RD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84D8	SBT1WR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

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TABLE 4-9: SYSTEM BUS TARGET 1 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
84E0	SBT1REG5	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84F0	SBT1RD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84F8	SBT1WR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

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TABLE 4-10: SYSTEM BUS TARGET 2 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8820	SBT2ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8824	SBT2ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8828	SBT2ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT2ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT2ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT2REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8850	SBT2RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8858	SBT2WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8860	SBT2REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8870	SBT2RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8878	SBT2WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8880	SBT2REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8890	SBT2RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8898	SBT2WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

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TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8C40	SBT3REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

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REGISTER 4-2: SBFLAG: SYSTEM BUS STATUS FLAG REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	T3PGV	T2PGV	T1PGV	T0PGV

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **T3PGV:T0PGV:** Target Permission Group Violation Status bits

Refer to Table 4-6 for the list of available targets and their descriptions.

1 = Target is reporting a Permission Group (PG) violation
0 = Target is not reporting a PG violation

Note: All errors are cleared at the source, that is, SBTxELOG1, SBTxELOG2, SBTxECLRS, or SBTxECLRM registers.

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REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0, C	U-0	U-0	U-0	R/W-0, C	R/W-0, C	R/W-0, C	R/W-0, C
	MULTI	—	—	—	CODE<3:0>			
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	INITID<7:0>							
7:0	R-0	R-0	R-0	R-0	U-0	R-0	R-0	R-0
	REGION<3:0>				—	CMD<2:0>		

Legend:	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31 **MULTI:** Multiple Permission Violations Status bit
This bit is cleared by writing a '1'.
1 = Multiple errors have been detected
0 = No multiple errors have been detected

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CODE<3:0>:** Error Code bits
Indicates the type of error that was detected. These bits are cleared by writing a '1'.
1111 = Reserved
1101 = Reserved
•
•
•
0011 = Permission violation
0010 = Reserved
0001 = Reserved
0000 = No error

bit 23-16 **Unimplemented:** Read as '0'

bit 15-8 **INITID<7:0>:** Initiator ID of Requester bits
11111111 = Reserved
•
•
•
00001111 = Reserved
00001110 = Reserved
00001101 = CAN4
00001100 = CAN3
00001011 = CAN2
00001010 = CAN1
00001001 = USB2
00001000 = USB1
00000111 = ADC0-ADC5, ADC7
00000110 = Reserved
00000101 = Flash Controller
00000100 = DMA Read
00000011 = DMA Read
00000010 = CPU (CPUPRI (CFGCON<24>) = 1)
00000001 = CPU (CPUPRI (CFGCON<25>) = 0)
00000000 = Reserved

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-3) (CONTINUED)

bit 7-4 **REGION<3:0>:** Requested Region Number bits
1111 - 0000 = Target's region that reported a permission group violation

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **CMD<2:0>:** Transaction Command of the Requester bits
111 = Reserved
110 = Reserved
101 = Write (a non-posted write)
100 = Reserved
011 = Read (a locked read caused by a Read-Modify-Write transaction)
010 = Read
001 = Write
000 = Idle

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

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REGISTER 4-4: SBTxELOG2: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 2 ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	GROUP<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-3 **Unimplemented:** Read as '0'

bit 1-0 **GROUP<1:0>:** Requested Permissions Group bits
11 = Reserved
10 = Reserved
01 = Group 1
00 = Group 0 (default group of CPU at Reset)

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-5: SBTxECON: SYSTEM BUS TARGET 'x' ERROR CONTROL REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ERRP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ERRP:** Error Control bit
1 = Report protection group violation errors
0 = Do not report protection group violation errors

bit 23-0 **Unimplemented:** Read as '0'

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-6: SBTxECLRS: SYSTEM BUS TARGET 'x' SINGLE ERROR CLEAR REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Single Error on Read bit
A single error as reported through SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-7: SBTxECLRM: SYSTEM BUS TARGET 'x' MULTIPLE ERROR CLEAR REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Multiple Errors on Read bit
Multiple errors as reported through SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

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REGISTER 4-8: SBTxREGy: SYSTEM BUS TARGET 'x' REGION 'y' REGISTER ('x' = 0-3; 'y' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W0	R/W-0	R/W0	R/W-0	R/W0	R/W-0	R/W0	R/W-0
	BASE<21:14>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASE<13:6>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	U-0
	BASE<5:0>						PRI	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	SIZE<4:0>					—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-10 **BASE<21:0>:** Region Base Address bits

bit 9 **PRI:** Region Priority Level bit
1 = Level 2
0 = Level 1

bit 8 **Unimplemented:** Read as '0'

bit 7-3 **SIZE<4:0>:** Region Size bits
Permissions for a region are only active is the SIZE is non-zero.
11111 = Region size = $2^{(SIZE - 1)}$ x 1024 (bytes)
•
•
•
00001 = Region size = $2^{(SIZE - 1)}$ x 1024 (bytes)
00000 = Region is not present

bit 2-0 **Unimplemented:** Read as '0'

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.
2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

REGISTER 4-9: SBTxRDy: SYSTEM BUS TARGET 'x' REGION 'y' READ PERMISSIONS REGISTER ('x' = 0-3; 'y' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **GROUP3:** Group 3 Read Permissions bits
1 = Privilege Group 3 has read permission
0 = Privilege Group 3 does not have read permission

bit 2 **GROUP2:** Group 2 Read Permissions bits
1 = Privilege Group 2 has read permission
0 = Privilege Group 2 does not have read permission

bit 1 **GROUP1:** Group 1 Read Permissions bits
1 = Privilege Group 1 has read permission
0 = Privilege Group 1 does not have read permission

bit 0 **GROUP0:** Group 0 Read Permissions bits
1 = Privilege Group 0 has read permission
0 = Privilege Group 0 does not have read permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.
2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

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REGISTER 4-10: SBTxWRy: SYSTEM BUS TARGET 'x' REGION 'y' WRITE PERMISSIONS REGISTER ('x' = 0-3; 'y' = 0-2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **GROUP3:** Group 3 Write Permissions bits
- 1 = Privilege Group 3 has write permission
- 0 = Privilege Group 3 does not have write permission

bit 2 **GROUP2:** Group 2 Write Permissions bits
- 1 = Privilege Group 2 has write permission
- 0 = Privilege Group 2 does not have write permission

bit 1 **GROUP1:** Group 1 Write Permissions bits
- 1 = Privilege Group 1 has write permission
- 0 = Privilege Group 1 does not have write permission

bit 0 **GROUP0:** Group 0 Write Permissions bits
- 1 = Privilege Group 0 has write permission
- 0 = Privilege Group 0 does not have write permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.
2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

NOTES:

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5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MK GP/MC devices contain an internal Flash program memory for executing user code, which includes the following features:

- Two Flash banks for live update support
- Dual boot support
- Write protection for program and boot Flash

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming (ICSP)

RTSP is performed by software executing from either Flash or RAM memory. For information about RTSP techniques, refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) in the *"PIC32 Family Reference Manual".*

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip web site (www.microchip.com).

Note: In PIC32MK GP/MC devices, the Flash page size is 1024 Instruction Words and the row size is 128 Instruction Words.

5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0A00	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	PFSWAP	BFSWAP	—	—	NVMOP<3:0>				0000
0A10	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
0A20	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
0A30	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
0A40	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
0A50	NVMDATA2	31:16	NVMDATA2<31:0>																0000
		15:0																	0000
0A60	NVMDATA3	31:16	NVMDATA3<31:0>																0000
		15:0																	0000
0A70	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
0A80	NVMPWP(1)	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
0A90	NVMBWP(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LBWPULOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPULOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF
0AA0	NVMCON2(1)	31:16	ERSCNT<3:0>				—	—	—	—	—	—	—	LPRDWS<4:0>					001F
		15:0	LPRD	—	CREAD1	VREAD1	—	—	ERETRY<1:0>		SWAPLOCK<1:0>		—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	U-0
	WR(1)	WREN(1)	WRERR(1)	LVDERR(1)	—	—	—	—
7:0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	PFSWAP(2)	BFSWAP(2,3)	—	—	NVMOP<3:0>			

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit(1)

This bit cannot be cleared and can be set only when WREN = 1 and the unlock sequence has been performed.
1 = Initiate a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit(1)

1 = Enable writes to the WR bit and disables writes to the NVMOP<3:0> bits
0 = Disable writes to WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **PFSWAP:** Program Flash Bank Swap Control bit(2)

1 = Program Flash Bank 2 is mapped to the lower mapped region and Program Flash Bank 1 is mapped to the upper mapped region
0 = Program Flash Bank 1 is mapped to the lower mapped region and Program Flash Bank 2 is mapped to the upper mapped region

bit 6 **BFSWAP:** Boot Flash Bank Swap Control bit(2,3)

1 = Boot Flash Bank 2 is mapped to the lower boot region and program Boot Flash Bank 1 is mapped to the upper boot region
0 = Boot Flash Bank 1 is mapped to the lower boot region and program Boot Flash Bank 2 is mapped to the upper boot region

bit 5-4 **Unimplemented:** Read as '0'

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This bit can only be modified when the WREN bit = 0, the NVMKEY unlock sequence is satisfied, and the SWAPLOCK<1:0> bits (NVMCON2<7:6>) are cleared to '0'.

3: The BFSWAP value is determined by the values of the user-programmed Sequence Numbers in each boot panel.

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER (CONTINUED)

bit 3-0 **NVMOP<3:0>:** NVM Operation bits

These bits are only writable when WREN = 0.

1111 = Reserved

•

•

•

1000 = Reserved

0111 = Program erase operation: erase all of program Flash memory (all pages must be unprotected, PWP<23:0> = 0x000000)

0110 = Upper program Flash memory erase operation: erases only the upper mapped region of program Flash (all pages in that region must be unprotected)

0101 = Lower program Flash memory erase operation: erases only the lower mapped region of program Flash (all pages in that region must be unprotected)

0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected

0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected

0010 = Quad Word (128-bit) program operation: programs the 128-bit Flash word selected by NVMADDR, if it is not write-protected

0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected

0000 = No operation

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This bit can only be modified when the WREN bit = 0, the NVMKEY unlock sequence is satisfied, and the SWAPLOCK<1:0> bits (NVMCON2<7:6>) are cleared to '0'.

3: The BFSWAP value is determined by the values of the user-programmed Sequence Numbers in each boot panel.

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REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** Unlock Register bits
These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** Flash Address bits(1)

NVMOP<3:0> Selection	Flash Address Bits (NVMADDR<31:0>)
Page Erase	Address identifies the page to erase (NVMADDR<11:0> are ignored).
Row Program	Address identifies the row to program (NVMADDR<8:0> are ignored).
Word Program	Address identifies the word to program (NVMADDR<1:0> are ignored).
Quad Word Program	Address identifies the quad word (128-bit) to program (NVMADDR<3:0> bits are ignored).

Note 1: For all other NVMOP<3:0> bit settings, the Flash address is ignored. See the NVMCON register (Register 5-1) for additional information on these bits.

Note: The bits in this register are only reset by a POR and are not affected by other reset sources.

REGISTER 5-4: NVMDATAx: FLASH DATA REGISTER (x = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATA<31:0>:** Flash Data bits
Word Program: Writes NVMDATA0 to the target Flash address defined in NVMADDR
Quad Word Program: Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the Least Significant Instruction Word.

Note: The bits in this register are only reset by a POR and are not affected by other reset sources.

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits
The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a POR and are not affected by other reset sources.

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REGISTER 5-6: NVMPWP: PROGRAM FLASH WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	PWPULOCK	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<23:16>							
15:8	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **PWPULOCK:** Program Flash Memory Page Write-protect Unlock bit
1 = Register is not locked and can be modified
0 = Register is locked and cannot be modified
This bit is only clearable and cannot be set except by any reset.

bit 30-24 **Unimplemented:** Read as '0'

bit 23-0 **PWP<23:0>:** Flash Program Write-protect (Page) Address bits
Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>. When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

REGISTER 5-7: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	LBWPULOCK	—	—	LBWP4(1)	LBWP3(1)	LBWP2(1)	LBWP1(1)	LBWP0(1)
7:0	R/W-1	r-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	UBWPULOCK	—	—	UBWP4(1)	UBWP3(1)	UBWP2(1)	UBWP1(1)	UBWP0(1)

Legend:		r = Reserved	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **LBWPULOCK:** Lower Boot Alias Write-protect Unlock bit
1 = LBWPx bits are not locked and can be modified
0 = LBWPx bits are locked and cannot be modified
This bit is only clearable and cannot be set except by any reset.

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **LBWP4:** Lower Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC10000 through 0x1FC13FFF enabled
0 = Write protection for physical address 0x01FC10000 through 0x1FC13FFF disabled

bit 11 **LBWP3:** Lower Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC0C000 through 0x1FC0FFFF enabled
0 = Write protection for physical address 0x01FC0C000 through 0x1FC0FFFF disabled

bit 10 **LBWP2:** Lower Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC08000 through 0x1FC0BFFF enabled
0 = Write protection for physical address 0x01FC08000 through 0x1FC0BFFF disabled

bit 9 **LBWP1:** Lower Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC04000 through 0x1FC07FFF enabled
0 = Write protection for physical address 0x01FC04000 through 0x1FC07FFF disabled

bit 8 **LBWP0:** Lower Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC00000 through 0x1FC03FFF enabled
0 = Write protection for physical address 0x01FC00000 through 0x1FC03FFF disabled

bit 7 **UBWPULOCK:** Upper Boot Alias Write-protect Unlock bit
1 = UBWPx bits are not locked and can be modified
0 = UBWPx bits are locked and cannot be modified
This bit is only user-clearable and cannot be set except by any reset.

bit 6 **Reserved:** This bit is reserved for use by development tools

bit 5 **Unimplemented:** Read as '0'

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

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REGISTER 5-7: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

bit 4 **UBWP4:** Upper Boot Alias Page 4 Write-protect bit(1)
1 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF enabled
0 = Write protection for physical address 0x01FC30000 through 0x1FC33FFF disabled

bit 3 **UBWP3:** Upper Boot Alias Page 3 Write-protect bit(1)
1 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF enabled
0 = Write protection for physical address 0x01FC2C000 through 0x1FC2FFFF disabled

bit 2 **UBWP2:** Upper Boot Alias Page 2 Write-protect bit(1)
1 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF enabled
0 = Write protection for physical address 0x01FC28000 through 0x1FC2BFFF disabled

bit 1 **UBWP1:** Upper Boot Alias Page 1 Write-protect bit(1)
1 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF enabled
0 = Write protection for physical address 0x01FC24000 through 0x1FC27FFF disabled

bit 0 **UBWP0:** Upper Boot Alias Page 0 Write-protect bit(1)
1 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF enabled
0 = Write protection for physical address 0x01FC20000 through 0x1FC23FFF disabled

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

REGISTER 5-8: NVMCON2: FLASH PROGRAMMING CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	ERSCNT<3:0>				—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	LPRDWS<4:0>(1)				
15:8	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	LPRD(1)	—	CREAD1(1)	VREAD1(1)	—	—	ERETRY<1:0>	
7:0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SWAPLOCK<1:0>		—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **ERSCNT<1:0>:** Erase Retry State Count bits

These bits can be used by software to track the erase retry state count in the event of a Master Clear or BOR. These bits are purely for software tracking purpose and are not used by hardware in any way.

bit 27-21 **Unimplemented:** Read as '0'

bit 20-16 **LPRDWS<4:0>:** Wait State bits(1)

11111 = 31 Wait States (32 total System Clocks)
11110 = 30 Wait States (31 total System Clocks)
•
•
•
00010 = 2 Wait States (3 total System Clocks)
00001 = 1 Wait State (2 total System Clocks)
00000 = 0 Wait State (1 total System Clock)

Note: When VREAD1 = 1, NVMWS only affects the panel containing NVMADDR. When LPRD = 1, LPRDWS affects all reads to all panels.

Required Flash Wait States LPRDWS<4:0>	SYSCLK (MHz)
3 - Wait State	0 < SYSCLK < 60 MHz
4 - Wait State	60 MHz < SYSCLK < 80 MHz
5 - Wait State	80 MHz < SYSCLK ≤ 120 MHz

Note 1: When the LPRD bit = 0, Flash read access wait states are governed by the PFMWS<2:0> bits (CHECON<2:0>).

2: When the LPRD bit = 1, Flash read access wait states are governed by the LPRDWS<4:0> bits.

bit 15 **LPRD:** Low-Power Read Control bit(1)

1 = Configures Flash for Low Power reads (increases access time).
0 = Configures Flash for Low Latency reads

When LPRD = 1, the LPRDWS<4:0> bits control the Flash wait states; otherwise, the PFMWS<2:0> bits control the Flash wait states.

bit 14 **Unimplemented:** Read as '0'

Note 1: This bit can only be modified when the WREN bit = 0, and the NVMKEY unlock sequence is satisfied.

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REGISTER 5-8: NVMCON2: FLASH PROGRAMMING CONTROL REGISTER 2 (CONTINUED)

bit 13 **CREAD1:** Compare Read of Logic 1 bit(1)

1 = Compare Read is enabled (only if VERIFYREAD1 = 1)
0 = Compare Read is disabled

Compare Read 1 causes all bits in a Flash Word to be evaluated during the read. If all bits are '1', the lowest Word in the Flash Word evaluates to 0x00000001, all other words are 0x00010000. If any bit is '0', the read evaluates to 0x00000000 for all Words in the Flash Word.

bit 12 **VREAD1:** Verify Read of Logic 1 Control bit(1)

1 = Selects Erase Retry Procedure with Verify Read
0 = Selects Single Erase w/o Verify Read

When VREAD1 = 1, Flash wait state control is from the LPRDWS<4:0> bits for the panel containing NVMADDR.

bit 11-10 **Unimplemented:** Read as '0'

bit 9-8 **ERETRY<1:0>:** Erase Retry Control bits

11 = Erase strength for last retry cycle
10 = Erase strength for third retry cycle
01 = Erase strength for second retry cycle
00 = Erase strength for first retry cycle

The user application should start with '00' (first retry cycle) and move on to higher strength if the programming does not complete.

This bit is used only when VREAD1 = 1 and when VREAD1 = 1.

bit 7-6 **SWAPLOCK<1:0>:** Flash Memory Swap Lock Control bits

11 = PFSWAP and BFSWAP are not writable and SWAPLOCK is not writable
10 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable
01 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable
00 = PFSWAP and BFSWAP are writable and SWAPLOCK is writable

bit 5-0 **Unimplemented:** Read as '0'

Note 1: This bit can only be modified when the WREN bit = 0, and the NVMKEY unlock sequence is satisfied.

NOTES:

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6.0 DATA EEPROM

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 58. "Data EEPROM"** (DS60001341), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Data EEPROM module provides the following features:

- 1K x 32-bit (4K x 8-bit) Emulated Data EEPROM using the 1K x 16 x 33-bit (66 KB)
- Register-based indirect access
- Register-based, non-memory mapped, SFR Program/Erase/Read interface
- Read:
  - Byte or Word read
  - Read start Control bit and read complete status flag
  - Read complete interrupt
- Program/Erase:
  - No user erase required prior to program
  - Hardware Word program verify
  - Automatic page erase as part of wear-leveling scheme
  - Hardware page erase verify
  - Bulk and page erase
  - Write complete and error interrupts
- Brown-out protection for all commands
- Concurrent Data EEPROM read with Program Flash read/write
- Endurance:
  - 160K program cycles per address location
  - Transparent wear-leveling scheme
  - No software overhead
  - Automatic page erase (once every 17 program write operations)
  - "Worn out" page detection and error flag
  - "Imminent Page Erase" prediction status flag to allow user to schedule wear leveling page erasure
- Low-power features:
  - Always in stand-by unless accessed
  - Power down in Sleep and/or Idle mode
  - Independent Data EEPROM Flash power down in Idle Control bit

6.1 Data EEPROM Flash

Table 6-1 provides the status of the Data EEPROM Flash.

TABLE 6-1: DATA EEPROM FLASH

Data EE Wait Status EEWS<7:0> bits (CFGCON2<7:0>) =	PBCLK (FSYSCLK / PBDIV<6:0> bits (PB2DIV<6:0>))
0	0-39 MHz
1	40-59 MHz
2	60-79 MHz
3	80-97 MHz
4	98-117 MHz
5	118-120 MHz

Note 1: The Data EEPROM Flash must have its calibration trim bits reinitialized after each cold power-up before any attempted accesses. Refer to **Section 58. "Data EEPROM"** (DS60001341) of the *"PIC32 Family Reference Manual"* for additional information.

2: Before any attempts to access the Data EEPROM module, the user application must configure the appropriate number of Wait states by configuring the EEWS<7:0> bits (CFGCON2< 7:0>) according to the details provided in Table 6-1.

6.2 Control Registers

TABLE 6-2: DATA EEPROM SFR SUMMARY

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9000	EECON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	RDY	SIDL	ABORT	—	—	—	—	RW	WREN	ERR<1:0>		ILW	CMD<2:0>			0000
9010	EEKEY(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	EEKEY<15:0>																0000
9020	EEADDR(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	EEADDR<11:0>												0000
9030	EEDATA	31:16	EEDATA<31:16>																0000
		15:0	EEDATA<15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: This register has corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register is a write-only register. Reads always result in '0'.

3: Because the EEPROM word size is 32 bits, for reads and writes the last two bits (EEADDR<1:0>) must always be '0'.

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REGISTER 6-1: EECON: EEPROM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R-0	R/W-0	R/W-0, HC	U-0	U-0	U-0	U-0
	ON	RDY	SIDL	ABORT	—	—	—	—
7:0	R/W-0, HC	R/W-0	R/W-0, HS, HC	R/W-0, HS, HC	R/W-0, HS	R/W-0	R/W-0	R/W-0
	RW	WREN(1)	ERR<1:0>		ILW	CMD<2:0>(1)		

Legend:	HS = Hardware settable	HC = Hardware clearable
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Data EEPROM Power Control bit

1 = Data EEPROM is enabled
0 = Data EEPROM is disabled

Attempting to clear this bit will have no effect if the RW bit is set. In addition, this bit is not cleared during Sleep if the FSLEEP bit in the DEVCFG register is set.

bit 14 **RDY:** Data EEPROM Ready bit

1 = Data EEPROM is ready for access
0 = Data EEPROM is not ready for access

RDY is cleared by hardware whenever a POR or BOR event occurs. It is set by hardware when the ON bit = 1 and the power-up timer has expired.

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **ABORT:** Data EEPROM Abort Operation Control bit

1 = Set by software to abort the on-going write command as soon as possible
0 = Data EEPROM panel is ready/Normal operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **RW:** Start Command Execution Control bit

When WREN = 1:

1 = Start memory word program or erase command
0 = Cleared by hardware to indicate program or erase operation has completed

When WREN = 0:

1 = Start memory word read command
0 = Cleared by hardware to indicate read operation has completed

This bit cannot be set if the ON bit = 0, or if the ON bit = 1 and the power-up timer has not yet expired (i.e., The RDY bit = 0). A BOR reset will indirectly clear this bit by forcing any executing command to terminate and to clear the RW bit afterwards.

bit 6 **WREN:** Data EEPROM Write Enable Control bit(1)

1 = Enables program or erase operations
0 = Disables program or erase of memory elements, and enables read operations

Note 1: This bit cannot be modified when the RW bit = 1.

2: The Configuration Write command (CMD<2:0> = 100) must be executed after any power-up before the Data EEPROM is ready for use. Refer to **Example 58-1 "Data EEPROM Initialization Code"** in **Section 58. "Data EEPROM"** (DS60001341) for details.

REGISTER 6-1: EECON: EEPROM CONTROL REGISTER (CONTINUED)

bit 5-4 **ERR<1:0>:** Data EEPROM Sequence Error Status bits

11 = A BOR event has occurred
10 = An attempted execution of a read or write operation with an invalid write OR command with a misaligned address (EEADDR<1:0> ≠ 00)
01 = A Bulk or Page Erase or a Word Program verify error has occurred
00 = No error condition

These bits can be cleared by software, or as the result of the successful execution of the next operation, or when the ON bit = 0. These bits may also be set by software (when the RW bit = 0) without affecting the operation of the module.

bit 3 **ILW:** Data EEPROM Imminent Long Write Status bit

1 = The next write to the EEPROM address (held in the EEADDR register) will require more time (~ 20 ms) than usual
0 = The next write to the EEPROM address (held in the EEADDR register) will be a normal write cycle

This bit can be cleared by software, or as the result of a write to the EEADDR register. This bit is set by hardware after a write command.

bit 2-0 **CMD<2:0>:** Data EEPROM Command Selection bits(1)

These bits are cleared only on a POR event.

111 = Reserved
•
•
•
100 = Configuration register Write command (WREN bit must be set)(2)
011 = Data EEPROM memory Bulk Erase command (WREN bit must be set)
010 = Data EEPROM memory Page Erase command (WREN bit must be set)
001 = Word Write command (WREN bit must be set)
000 = Word Read command (WREN bit must be clear)

Note 1: This bit cannot be modified when the RW bit = 1.

2: The Configuration Write command (CMD<2:0> = 100) must be executed after any power-up before the Data EEPROM is ready for use. Refer to **Example 58-1 "Data EEPROM Initialization Code"** in **Section 58. "Data EEPROM"** (DS60001341) for details.

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REGISTER 6-2: EEKEY: EEPROM KEY REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	EEKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	EEKEY<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **EEKEY<15:0>:** Data EEPROM Key bits

Writing the value 0xEDB7 followed by writing the value 0x1248 to this register will unlock the EECON register for write/erase operations. Reads have no effect on this register and return '0'.

Writing any other value will lock the EECON register.

REGISTER 6-3: EEADDR: EEPROM ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	EEADDR<11:8>(1,2)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEADDR<7:0>(1)							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-12 **Unimplemented:** Read as '0'

bit 11-0 **EEADR<11:0>:** Data EEPROM Address bits(1)

This register holds the address in the EEPROM memory upon which to operate. EEADDR<1:0> must always be '00' when the RW bit (EECON<7>) is set or an error will occur.

Note 1: The bits in this register cannot be modified when the RW bit (EECON<7>) = 1.

2: EEDATA is organized in 32-bit words, not by byte, hence the EEADDR bit must always be 32-bit word address aligned. Check that the EEADDR<1:0> bits are = 0'b00 at the beginning of any command when the user sets EEGO to '1'. If the EEADDR<1:0> bits are not 0'b00, it will forcefully clear the EEGO bit to '0' and will also set the ERR<1:0> bits (EECON<5:4>) to 0'b10.

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REGISTER 6-4: EEDATA: EEPROM DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDATA<31:24>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDATA<23:16>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDATA<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEDATA<7:0>(1)							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-0 **EEDATA<31:0>:** Data EEPROM Data bits(1)

This register holds the data in the EEPROM memory to store during write operations, or the data from memory after a read operation.

Note 1: These bits cannot be modified when the RW bit (EECON<7>) = 1. In addition, reading this register, when the RW bit = 1 may not return valid data, as the read operation may not have completed.

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7.0 RESETS

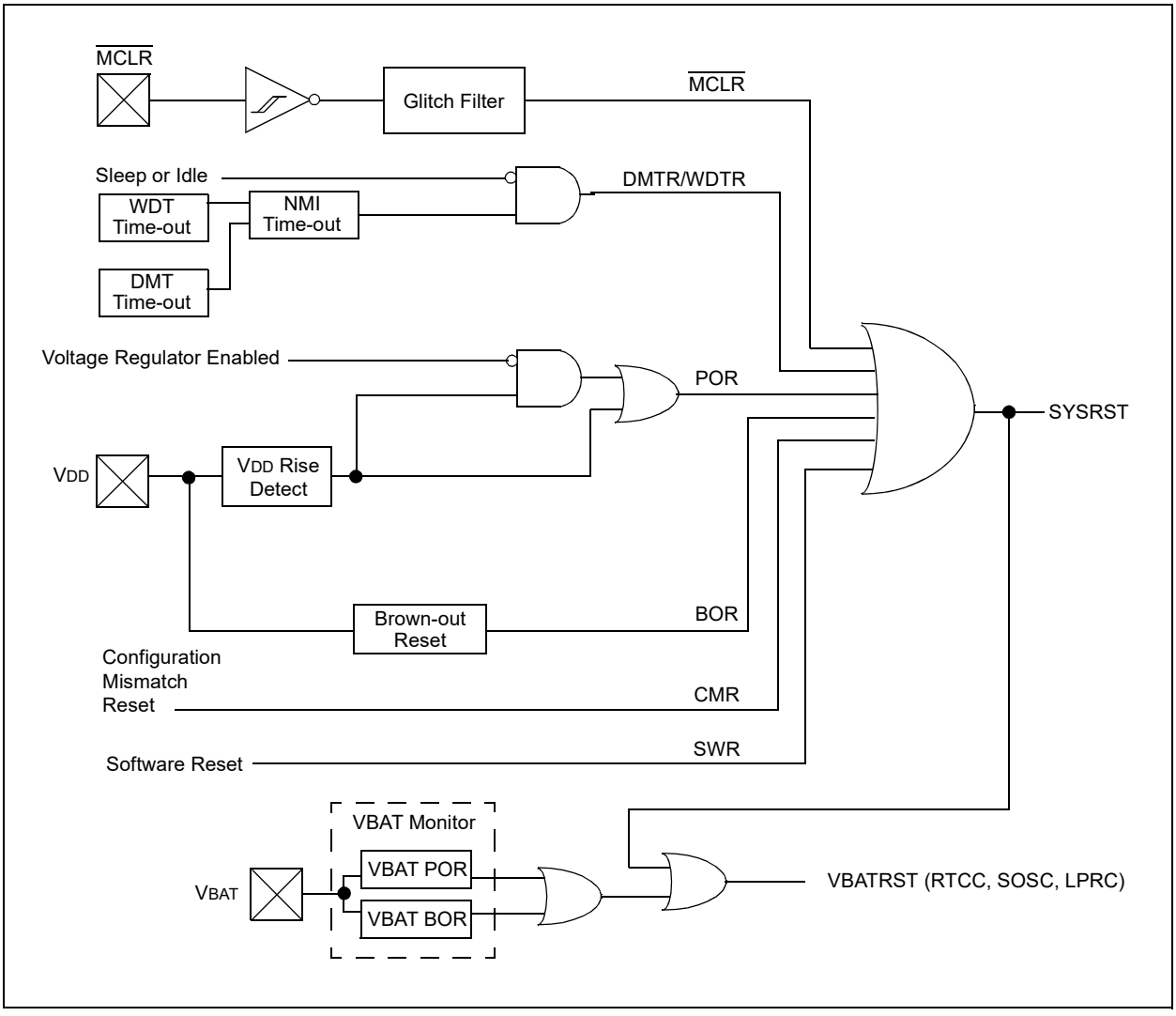
Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset pin ($\overline{MCLR}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

A simplified block diagram of the Reset module is illustrated in Figure 7-1.

FIGURE 7-1: SYSTEM RESET BLOCK DIAGRAM



7.1 Reset Control Registers

TABLE 7-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1240	RCON	31:16	PORIO	PORCORE	—	—	—	—	—	—	—	—	—	—	—	—	VBPOR	VBAT	0003
		15:0	—	—	—	—	—	DPSLP	CMR	—	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR	POR	0003
1250	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
1260	RNMICON	31:16	—	—	—	—	—	—	DMTO	WDTO	SWNMI	—	—	—	GNMI	---	CF	WDTS	0000
		15:0	NMICNT<15:0>																0000
1270	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	VREGRUN<1:0>		VREGSLP<1:0>		—	—	—	VREGS	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 7-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0, HS	R/W-0, HS	U-0	U-0	U-0	U-0	U-0	U-0
	PORIO	PORCORE	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1, HS	R/W-1, HS
	—	—	—	—	—	—	VBPOR	VBAT
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0
	—	—	—	—	—	DPSLP(1)	CMR	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR	SWR	DMTO	WDTO	SLEEP	IDLE	BOR(2)	POR(2)

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **PORIO:** I/O Voltage POR Flag bit
1 = A Power-up Reset has occurred due to I/O Voltage
0 = A Power-up Reset has not occurred due to I/O Voltage

Note: Set by hardware at detection of an I/O POR event. User software must clear this bit to view the next detection; however, writing a '1' to this bit does not cause a PORIO.

bit 30 **PORCORE:** Core Voltage POR Flag bit
1 = A Power-up Reset has occurred due to Core Voltage
0 = A Power-up Reset has not occurred due to Core Voltage

Note: Set by hardware at detection of a Core POR event. User software must clear this bit to view the next detection; however, writing a '1' to this bit does not cause a PORCORE.

bit 29-18 **Unimplemented:** Read as '0'

bit 17 **VBPOR:** VBPOR Mode Flag bit
1 = A VBAT domain POR has occurred
0 = A VBAT domain POR has not occurred

bit 16 **VBAT:** VBAT Mode Flag bit
1 = A POR exit from VBAT has occurred (a true POR must be established with the valid VBAT voltage on the VBAT pin)
0 = A POR exit from VBAT has not occurred

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **DPSLP:** Deep Sleep Mode Flag bit(1)
1 = Deep Sleep mode has occurred
0 = Deep Sleep mode has not occurred

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **Unimplemented:** Read as '0'

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed

Note 1: User software must clear this bit to view the next detection.

REGISTER 7-1: RCON: RESET CONTROL REGISTER

bit 5 **DMTO:** Deadman Timer Time-out Flag bit
1 = A DMT time-out has occurred
0 = A DMT time-out has not occurred

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view the next detection.

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REGISTER 7-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1,2)

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1,2)
1 = Enable software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Once this bit is set, any read of the RSWRST register will cause a Reset to occur.

REGISTER 7-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMTO	WDTO
23:16	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0, HS, HC	R/W-0
	SWNMI	—	—	—	GNMI	—	CF	WDTS
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<7:0>							

Legend:	HC = Hardware Clear	HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DMTO:** Deadman Timer Time-out Flag bit
1 = DMT time-out has occurred and caused a NMI
0 = DMT time-out has not occurred
Setting this bit will cause a DMT NMI event, and NMICNT will begin counting.

bit 24 **WDTO:** Watchdog Timer Time-Out Flag bit
1 = WDT time-out has occurred and caused a NMI
0 = WDT time-out has not occurred
Setting this bit will cause a WDT NMI event, and MNICNT will begin counting.

bit 23 **SWNMI:** Software NMI Trigger.
1 = An NMI will be generated
0 = An NMI will not be generated

bit 22-20 **Unimplemented:** Read as '0'

bit 19 **GNMI:** General NMI bit
1 = A general NMI event has been detected or a user-initiated NMI event has occurred
0 = A general NMI event has not been detected

Setting GNMI to a '1' causes a user-initiated NMI event. This bit is also set by writing 0x4E to the NMIKEY<7:0> (INTCON<31:24>) bits.

bit 18 **Unimplemented:** Read as '0'

bit 17 **CF:** Clock Fail Detect bit
1 = FSCM has detected clock failure and caused an NMI
0 = FSCM has not detected clock failure

Note: On a clock fail event if enabled by the FCKSM<1:0> bits (DEVCFG1<15:14>) = '0b11, this bit and the OSCCON<CF> bit will be set. The user software must clear both the bits inside the CF NMI before attempting to exit the ISR. Software or hardware settings of the CF bit (OSCCON<3>) will cause a CF NMI event and an automatic clock switch to the FRC provided the FCKSM<1:0> = '0b11. Unlike the CF bit (OSCCON<3>), software or hardware settings of the CF bit (RNMICON<17>) will cause a CF NMI event but will not cause a clock switch to the FRC. After a Clock Fail event, a successful user software clock switch if implemented, hardware will automatically clear the CF bit (RNMICON<17>), but not the CF bit (OSCCON<3>). The CF bit (OSCCON<3>) must be cleared by software using the OSCCON register unlock procedure.

Note 1: When a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is triggered the NMICNT will start decrementing. When NMICNT reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit is written. Refer to the **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

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REGISTER 7-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep
0 = WDT time-out has not occurred during Sleep mode
Setting this bit will cause a WDT NMI.

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI reset counter.
11111111-00000001 = Number of SYSCLK cycles before a device Reset occurs(1)
00000000 = No delay between NMI assertion and device Reset event

Note 1: When a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is triggered the NMICNT will start decrementing. When NMICNT reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit is written. Refer to the **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 7-4: PWRCON: POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	VREGS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **VREGS:** Internal Voltage Regulator Stand-by Enable bit
1 = Voltage regulator will remain active during Sleep
0 = Voltage regulator will go to Stand-by mode during Sleep

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8.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupt Controller"** (DS60001108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MK GP/MC devices generate interrupt requests in response to interrupt events from peripheral modules. The Interrupt Controller module exists outside of the CPU and prioritizes the interrupt events before presenting them to the CPU.

The CPU handles interrupt events as part of the exception handling mechanism, which is described in **8.1 "CPU Exceptions"**.

The Interrupt Controller module includes the following features:

- Up to 216 interrupt sources and vectors with dedicated programmable offsets, eliminating the need for redirection
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- Two shadow register sets that can be used for any priority level, eliminating software context switch and reducing interrupt latency
- Software can generate any interrupt

Table 8-1 provides Interrupt Service routine (ISR) latency information.

TABLE 8-1: ISR LATENCY INFORMATION

Condition	Compiler Automatic Run-time						User/MPLAB® Harmony Responsibility	Comment
	CP0 REGISTER 16, SELECT 0 <K0>	PERCHEEN bit (CHECON<26>)	DCHEEN bit (CHECON<25>)	ICHEEN bit (CHECON<24>)	PREFEN<1:0> bits (CHECON<5:4>)	PFMWS <2:0> bits CHECON<2:0>)	User source file ISR declaration/invocation. **Note:** The user is responsible for the ISR declaration for the fastest ISR latency response.	Interrupt Latency (SYSCLK Cycles) (Time from interrupt event to first user source code instruction execution inside ISR).

Reset Values	0’b010	0’b1	0’b1	0’b1	0’b00	0’b111	`void __ISR(<Vector Number n>, ipl7auto)ISR(void)`
							`{`
							`  // “n” = Vector Number, see data sheet`
							`  // User ISR code`
							`}`
								257

Recommended user optimized CPU and ISR Latency Settings (2)	0’b011	0’b1	0’b1	0’b1	0’b01	0’b011	`void __attribute__((interrupt(iplXauto), at_vector(n), aligned(16))) isr ()`
							`{`
							`  // “n”=Vector Number, see data sheet`
							`  // “X”=IPL 1-7`
							`  // User ISR code`
							`}`
								43 + (7 – IPL) (Latency per interrupt)

Note 1: The CPU ISR latency can cause unexpected behavior in high data rate peripherals when a high repetitive rate of CPU interrupts. For example, it is possible that if multiple interrupt sources occur simultaneously, or if a high-speed peripheral like ADC occurs faster than the CPU can read the results from the first original interrupt, then that data may be overwritten by the second interrupt. If the possibility exists in user application that the CPU servicing requirements are less than the combined sum of all possible overlapping interrupt rate specified above, to avoid buffer overflows or data overwrites, it is recommended to use the DMA to service the data and buffer instead of the CPU.

2: For the best optimized CPU and ISR performance, to complete the optimization, the user application should define ISRs that use the “at vector” attribute as shown in Table 8-1. In addition, if the ADC combined sum throughput rate of all the ADC modules in use is greater than (SYSCLK/43) = 2.8 Msps, it is recommended to use the ADC CPU early interrupt generation defined in the ADCxTIME and ADCEIENx registers. This will reduce the probability of the ADC results being overwritten by the next conversion before the CPU can read the previous ADC result if not using the DMA for ADC. Do not use the early interrupts if using the ADC in DMA mode.

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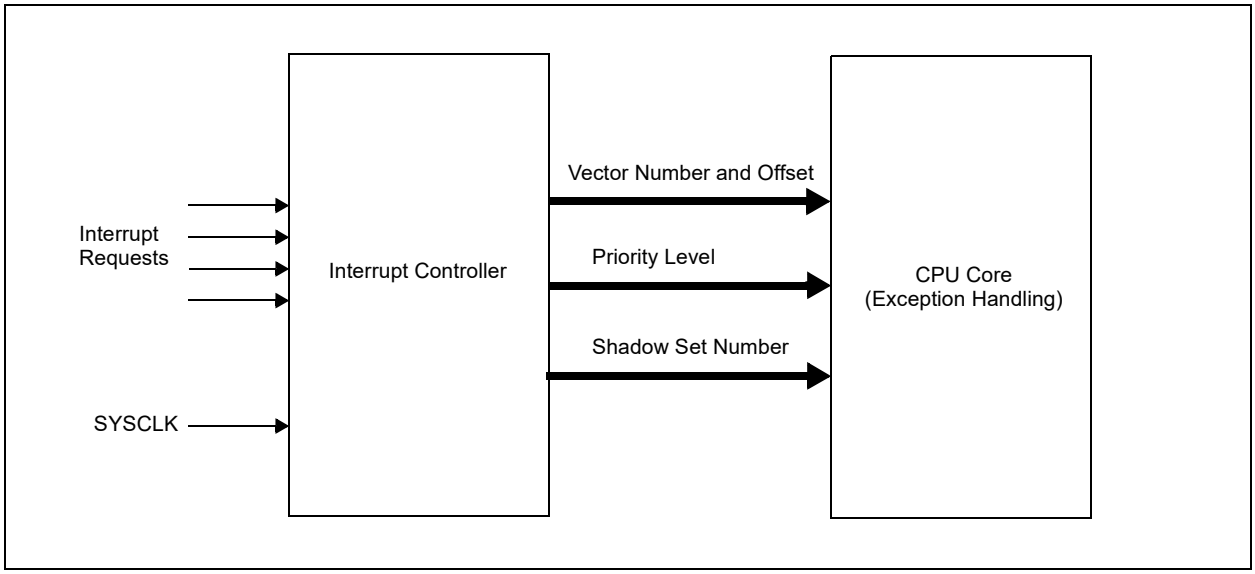
Figure 8-1 illustrates the block diagram of the Interrupt Controller and CPU exceptions.

FIGURE 8-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM



8.1 CPU Exceptions

CPU co-processor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 8-2 lists the exception types in order of priority.

TABLE 8-2: MIPS32® microAptiv™ MCU CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR).	0xBFC0_0000	BEV, ERL	—	—	_on_reset
Soft Reset	Assertion of a software Reset.	0xBFC0_0000	BEV, SR, ERL	—	—	_on_reset
DSS	EJTAG debug single step.	0xBFC0_0480	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by the assertion of the external EJ_DINT input or by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480	—	DINT	—	—
NMI	Assertion of NMI signal.	0xBFC0_0000	BEV, NMI, ERL	—	—	_nmi_handler
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 8-3.	IPL<2:0>	—	0x00	See Table 8-3.
Deferred Watch	Deferred watch (unmasked by K|DM=>!(K|DM) transition).	EBASE+0x180	WP, EXL	—	0x17	_general_exception_handler
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480	—	DIB	—	—
WATCH	A reference to an address that is in one of the Watch registers (fetch).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Fetch address alignment error. Fetch reference to protected address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
IBE	Instruction fetch bus error.	EBASE+0x180	EXL	—	0x06	_general_exception_handler
Instruction Validity Exceptions	An instruction could not be completed because it was not allowed to access the required resources (Coprocessor Unusable) or was illegal (Reserved Instruction). If both exceptions occur on the same instruction, the Coprocessor Unusable Exception takes priority over the Reserved Instruction Exception.	EBASE+0x180	EXL	—	0x0A or 0x0B	_general_exception_handler
Execute Exception	An instruction-based exception occurred: Integer overflow, trap, system call, breakpoint, floating point, or DSP ASE state disabled exception.	EBASE+0x180	EXL	—	0x08-0x0C	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE+0x180	EXL	—	0x0D	_general_exception_handler
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).	0xBFC0_0480	—	DDBL or DDBS	—	—
WATCH	A reference to an address that is in one of the Watch registers (data).	EBASE+0x180	EXL	—	0x17	_general_exception_handler

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TABLE 8-2: MIPS32® microAptiv™ MCU CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
AdEL	Load address alignment error. User mode load reference to kernel address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
AdES	Store address alignment error. User mode store to kernel address.	EBASE+0x180	EXL	—	0x05	_general_exception_handler
DBE	Load or store bus error.	EBASE+0x180	EXL	—	0x07	_general_exception_handler
DDBL	EJTAG data hardware breakpoint matched in load data compare.	0xBFC0_0480	—	DDBL	—	—
CBrk	EJTAG complex breakpoint.	0xBFC0_0480	—	DIBIMPR, DDBLIMPR, and/or DDBSIMPR	—	—
Lowest Priority						

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8.2 Interrupts

The PIC32MK GP/MC family uses variable offsets for vector spacing. This allows the interrupt vector spacing to be configured according to application needs. A unique interrupt vector offset can be set for each vector using its associated OFFx register.

For details on the Variable Offset feature, refer to **8.5.2 "Variable Offset"** in **Section 8. "Interrupt Controller"** (DS60001108) of the *"PIC32 Family Reference Manual"*.

Table 8-3 provides the Interrupt IRQ, vector and bit location information.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Highest Natural Order Priority								
Core Timer Interrupt	_CORE_TIMER_VECTOR	0	OFF000<17:1>	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software Interrupt 0	_CORE_SOFTWARE_0_VECTOR	1	OFF001<17:1>	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software Interrupt 1	_CORE_SOFTWARE_1_VECTOR	2	OFF002<17:1>	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External Interrupt 0	_EXTERNAL_0_VECTOR	3	OFF003<17:1>	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
Timer1	_TIMER_1_VECTOR	4	OFF004<17:1>	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
Input Capture 1 Error	_INPUT_CAPTURE_1_ERROR_VECTOR	5	OFF005<17:1>	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
Input Capture 1	_INPUT_CAPTURE_1_VECTOR	6	OFF006<17:1>	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	Yes
Output Compare 1	_OUTPUT_COMPARE_1_VECTOR	7	OFF007<17:1>	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
External Interrupt 1	_EXTERNAL_1_VECTOR	8	OFF008<17:1>	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
Timer2	_TIMER_2_VECTOR	9	OFF009<17:1>	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
Input Capture 2 Error	_INPUT_CAPTURE_2_ERROR_VECTOR	10	OFF010<17:1>	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	Yes
Input Capture 2	_INPUT_CAPTURE_2_VECTOR	11	OFF011<17:1>	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	Yes
Output Compare 2	_OUTPUT_COMPARE_2_VECTOR	12	OFF012<17:1>	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
External Interrupt 2	_EXTERNAL_2_VECTOR	13	OFF013<17:1>	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Timer3	_TIMER_3_VECTOR	14	OFF014<17:1>	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
Input Capture 3 Error	_INPUT_CAPTURE_3_ERROR_VECTOR	15	OFF015<17:1>	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	Yes
Input Capture 3	_INPUT_CAPTURE_3_VECTOR	16	OFF016<17:1>	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
Output Compare 3	_OUTPUT_COMPARE_3_VECTOR	17	OFF017<17:1>	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
External Interrupt 3	_EXTERNAL_3_VECTOR	18	OFF018<17:1>	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer4	_TIMER_4_VECTOR	19	OFF019<17:1>	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
Input Capture 4 Error	_INPUT_CAPTURE_4_ERROR_VECTOR	20	OFF020<17:1>	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
Input Capture 4	_INPUT_CAPTURE_4_VECTOR	21	OFF021<17:1>	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes
Output Compare 4	_OUTPUT_COMPARE_4_VECTOR	22	OFF022<17:1>	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	No
External Interrupt 4	_EXTERNAL_4_VECTOR	23	OFF023<17:1>	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	No
Timer5	_TIMER_5_VECTOR	24	OFF024<17:1>	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	No
Input Capture 5 Error	_INPUT_CAPTURE_5_ERROR_VECTOR	25	OFF025<17:1>	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	Yes
Input Capture 5	_INPUT_CAPTURE_5_VECTOR	26	OFF026<17:1>	IFS0<26>	IEC0<26>	IPC6<20:18>	IPC6<17:16>	Yes
Output Compare 5	_OUTPUT_COMPARE_5_VECTOR	27	OFF027<17:1>	IFS0<27>	IEC0<27>	IPC6<28:26>	IPC6<25:24>	No
Reserved	—	28	—	—	—	—	—	—

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Reserved	—	29	—	—	—	—	—	—
Real Time Clock	_RTCC_VECTOR	30	OFF030<17:1>	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	Yes
Flash Control Event	_FLASH_CONTROL_VECTOR	31	OFF031<17:1>	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
Comparator 1 Interrupt	_COMPARATOR_1_VECTOR	32	OFF032<17:1>	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
Comparator 2 Interrupt	_COMPARATOR_2_VECTOR	33	OFF033<17:1>	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	Yes
USB1 Interrupts	_USB_1_VECTOR	34	OFF034<17:1>	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	Yes
SPI1 Fault	_SPI1_FAULT_VECTOR	35	OFF035<17:1>	IFS1<3>	IEC1<3>	IPC8<28:26>	IPC8<25:24>	No
SPI1 Receive Done	_SPI1_RX_VECTOR	36	OFF036<17:1>	IFS1<4>	IEC1<4>	IPC9<4:2>	IPC9<1:0>	No
SPI1 Transfer Done	_SPI1_TX_VECTOR	37	OFF037<17:1>	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	Yes
UART1 Fault	_UART1_FAULT_VECTOR	38	OFF038<17:1>	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	Yes
UART1 Receive Done	_UART1_RX_VECTOR	39	OFF039<17:1>	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	No
UART1 Transfer Done	_UART1_TX_VECTOR	40	OFF040<17:1>	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	No
Reserved	—	41	—	—	—	—	—	—
Reserved	—	42	—	—	—	—	—	—
Reserved	—	43	—	—	—	—	—	—
PORTA Input Change Interrupt	_CHANGE_NOTICE_A_VECTOR	44	OFF044<17:1>	IFS1<12>	IEC1<12>	IPC11<4:2>	IPC11<1:0>	Yes
PORTB Input Change Interrupt	_CHANGE_NOTICE_B_VECTOR	45	OFF045<17:1>	IFS1<13>	IEC1<13>	IPC11<12:10>	IPC11<9:8>	Yes
PORTC Input Change Interrupt	_CHANGE_NOTICE_C_VECTOR	46	OFF046<17:1>	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
PORTD Input Change Interrupt	_CHANGE_NOTICE_D_VECTOR	47	OFF047<17:1>	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	Yes
PORTE Input Change Interrupt	_CHANGE_NOTICE_E_VECTOR	48	OFF048<17:1>	IFS1<16>	IEC1<16>	IPC12<4:2>	IPC12<1:0>	Yes
PORTF Input Change Interrupt	_CHANGE_NOTICE_F_VECTOR	49	OFF049<17:1>	IFS1<17>	IEC1<17>	IPC12<12:10>	IPC12<9:8>	Yes
PORTG Input Change Interrupt	_CHANGE_NOTICE_G_VECTOR	50	OFF050<17:1>	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	Yes
Parallel Master Port	_PMP_VECTOR	51	OFF051<17:1>	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	Yes
Parallel Master Port Error	_PMP_ERROR_VECTOR	52	OFF052<17:1>	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
SPI2 Fault	_SPI2_FAULT_VECTOR	53	OFF053<17:1>	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
SPI2 Receive Done	_SPI2_RX_VECTOR	54	OFF054<17:1>	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
SPI2 Transfer Done	_SPI2_TX_VECTOR	55	OFF055<17:1>	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes
UART2 Fault	_UART2_FAULT_VECTOR	56	OFF056<17:1>	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
UART2 Receive Done	_UART2_RX_VECTOR	57	OFF057<17:1>	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
UART2 Transfer Done	_UART2_TX_VECTOR	58	OFF058<17:1>	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	Yes
Reserved	—	59	—	—	—	—	—	—
Reserved	—	60	—	—	—	—	—	—
Reserved	—	61	—	—	—	—	—	—
UART3 Fault	_UART3_FAULT_VECTOR	62	OFF062<17:1>	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	Yes
UART3 Receive Done	_UART3_RX_VECTOR	63	OFF063<17:1>	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	Yes
UART3 Transfer Done	_UART3_TX_VECTOR	64	OFF064<17:1>	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	Yes
UART4 Fault	_UART4_FAULT_VECTOR	65	OFF065<17:1>	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
UART4 Receive Done	_UART4_RX_VECTOR	66	OFF066<17:1>	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
UART4 Transfer Done	_UART4_TX_VECTOR	67	OFF067<17:1>	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
UART5 Fault	_UART5_FAULT_VECTOR	68	OFF068<17:1>	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
UART5 Receive Done	_UART5_RX_VECTOR	69	OFF069<17:1>	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
UART5 Transfer Done	_UART5_TX_VECTOR	70	OFF070<17:1>	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
CTMU Interrupt	_CTMU_VECTOR	71	OFF071<17:1>	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
DMA Channel 0	_DMA0_VECTOR	72	OFF072<17:1>	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
DMA Channel 1	_DMA1_VECTOR	73	OFF073<17:1>	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
DMA Channel 2	_DMA2_VECTOR	74	OFF074<17:1>	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	Yes
DMA Channel 3	_DMA3_VECTOR	75	OFF075<17:1>	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	Yes
Timer6	_TIMER_6_VECTOR	76	OFF076<17:1>	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	Yes
Input Capture 6 Error	_INPUT_CAPTURE_6_ERROR_VECTOR	77	OFF077<17:1>	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	Yes
Input Capture 6	_INPUT_CAPTURE_6_VECTOR	78	OFF078<17:1>	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	Yes
Output Compare 6	_OUTPUT_COMPARE_6_VECTOR	79	OFF079<17:1>	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	Yes
Timer7	_TIMER_7_VECTOR	80	OFF080<17:1>	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	Yes
Input Capture 7 Error	_INPUT_CAPTURE_7_ERROR_VECTOR	81	OFF081<17:1>	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	Yes
Input Capture 7	_INPUT_CAPTURE_7_VECTOR	82	OFF082<17:1>	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	Yes
Output Compare 7	_OUTPUT_COMPARE_7_VECTOR	83	OFF083<17:1>	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Timer8	_TIMER_8_VECTOR	84	OFF084<17:1>	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	Yes
Input Capture 8 Error	_INPUT_CAPTURE_8_ERROR_VECTOR	85	OFF085<17:1>	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	Yes
Input Capture 8	_INPUT_CAPTURE_8_VECTOR	86	OFF086<17:1>	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	Yes
Output Compare 8	_OUTPUT_COMPARE_8_VECTOR	87	OFF087<17:1>	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	Yes
Timer9	_TIMER_9_VECTOR	88	OFF088<17:1>	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	Yes
Input Capture 9 Error	_INPUT_CAPTURE_9_ERROR_VECTOR	89	OFF089<17:1>	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	Yes
Input Capture 9	_INPUT_CAPTURE_9_VECTOR	90	OFF090<17:1>	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	Yes
Output Compare 9	_OUTPUT_COMPARE_9_VECTOR	91	OFF091<17:1>	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	Yes
ADC Global Interrupt	_ADC_VECTOR	92	OFF092<17:1>	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	Yes
Reserved	—	93	—	—	—	—	—	—
ADC Digital Comparator 1	_ADC_DC1_VECTOR	94	OFF094<17:1>	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
ADC Digital Comparator 2	_ADC_DC2_VECTOR	95	OFF095<17:1>	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	Yes
ADC Digital Filter 1	_ADC_DF1_VECTOR	96	OFF096<17:1>	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	Yes
ADC Digital Filter 2	_ADC_DF2_VECTOR	97	OFF097<17:1>	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	Yes
ADC Digital Filter 3	_ADC_DF3_VECTOR	98	OFF098<17:1>	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	Yes
ADC Digital Filter 4	_ADC_DF4_VECTOR	99	OFF099<17:1>	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	Yes
ADC Fault	_ADC_FAULT_VECTOR	100	OFF100<17:1>	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	Yes
ADC End of Scan	_ADC_EOS_VECTOR	101	OFF101<17:1>	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	Yes
ADC Ready	_ADC_ARDY_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
ADC Update Ready After Suspend	_ADC_URDY_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	Yes
ADC First Class Channels DMA	_ADC_DMA_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
ADC Early Group Interrupt	_ADC_EARLY_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes
ADC Data 0	_ADC_DATA0_VECTOR	106	OFF106<17:1>	IFS3<10>	IEC3<10>	IPC26<20:18>	IPC26<17:16>	Yes
ADC Data 1	_ADC_DATA1_VECTOR	107	OFF107<17:1>	IFS3<11>	IEC3<11>	IPC26<28:26>	IPC26<25:24>	Yes
ADC Data 2	_ADC_DATA2_VECTOR	108	OFF108<17:1>	IFS3<12>	IEC3<12>	IPC26<4:2>	IPC27<1:0>	Yes
ADC Data 3	_ADC_DATA3_VECTOR	109	OFF109<17:1>	IFS3<13>	IEC3<13>	IPC27<12:10>	IPC27<9:8>	Yes
ADC Data 4	_ADC_DATA4_VECTOR	110	OFF110<17:1>	IFS3<14>	IEC3<14>	IPC27<20:18>	IPC27<17:16>	Yes
ADC Data 5	_ADC_DATA5_VECTOR	111	OFF111<17:1>	IFS3<15>	IEC3<15>	IPC27<28:26>	IPC27<25:24>	Yes
ADC Data 6	_ADC_DATA6_VECTOR	112	OFF112<17:1>	IFS3<16>	IEC3<16>	IPC28<4:2>	IPC28<1:0>	Yes
ADC Data 7	_ADC_DATA7_VECTOR	113	OFF113<17:1>	IFS3<17>	IEC3<17>	IPC28<12:10>	IPC28<9:8>	Yes
ADC Data 8	_ADC_DATA8_VECTOR	114	OFF114<17:1>	IFS3<18>	IEC3<18>	IPC28<20:18>	IPC28<17:16>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 9	_ADC_DATA9_VECTOR	115	OFF115<17:1>	IFS3<19>	IEC3<19>	IPC28<28:26>	IPC28<25:24>	Yes
ADC Data 10	_ADC_DATA10_VECTOR	116	OFF116<17:1>	IFS3<20>	IEC3<20>	IPC29<4:2>	IPC29<1:0>	Yes
ADC Data 11	_ADC_DATA11_VECTOR	117	OFF117<17:1>	IFS3<21>	IEC3<21>	IPC29<12:10>	IPC29<9:8>	Yes
ADC Data 12	_ADC_DATA12_VECTOR	118	OFF118<17:1>	IFS3<22>	IEC3<22>	IPC29<20:18>	IPC29<17:16>	Yes
ADC Data 13	_ADC_DATA13_VECTOR	119	OFF119<17:1>	IFS3<23>	IEC3<23>	IPC29<28:26>	IPC29<25:24>	Yes
ADC Data 14	_ADC_DATA14_VECTOR	120	OFF120<17:1>	IFS3<24>	IEC3<24>	IPC30<4:2>	IPC30<1:0>	Yes
ADC Data 15	_ADC_DATA15_VECTOR	121	OFF121<17:1>	IFS3<25>	IEC3<25>	IPC30<12:10>	IPC30<9:8>	Yes
ADC Data 16	_ADC_DATA16_VECTOR	122	OFF122<17:1>	IFS3<26>	IEC3<26>	IPC30<20:18>	IPC30<17:16>	Yes
ADC Data 17	_ADC_DATA17_VECTOR	123	OFF123<17:1>	IFS3<27>	IEC3<27>	IPC30<28:26>	IPC30<25:24>	Yes
ADC Data 18	_ADC_DATA18_VECTOR	124	OFF124<17:1>	IFS3<28>	IEC3<28>	IPC31<4:2>	IPC31<1:0>	Yes
ADC Data 19	_ADC_DATA19_VECTOR	125	OFF125<17:1>	IFS3<29>	IEC3<29>	IPC31<12:10>	IPC31<9:8>	Yes
ADC Data 20	_ADC_DATA20_VECTOR	126	OFF126<17:1>	IFS3<30>	IEC3<30>	IPC31<20:18>	IPC31<17:16>	Yes
ADC Data 21	_ADC_DATA21_VECTOR	127	OFF127<17:1>	IFS3<31>	IEC3<31>	IPC31<28:26>	IPC31<25:24>	Yes
ADC Data 22	_ADC_DATA22_VECTOR	128	OFF128<17:1>	IFS4<0>	IEC4<0>	IPC32<4:2>	IPC32<1:0>	Yes
ADC Data 23	_ADC_DATA23_VECTOR	129	OFF129<17:1>	IFS4<1>	IEC4<1>	IPC32<12:10>	IPC32<9:8>	Yes
ADC Data 24	_ADC_DATA24_VECTOR	130	OFF130<17:1>	IFS4<2>	IEC4<2>	IPC32<20:18>	IPC32<17:16>	Yes
ADC Data 25	_ADC_DATA25_VECTOR	131	OFF131<17:1>	IFS4<3>	IEC4<3>	IPC32<28:26>	IPC32<25:24>	Yes
ADC Data 26	_ADC_DATA26_VECTOR	132	OFF132<17:1>	IFS4<4>	IEC4<4>	IPC33<4:2>	IPC33<1:0>	Yes
ADC Data 27	_ADC_DATA27_VECTOR	133	OFF133<17:1>	IFS4<5>	IEC4<5>	IPC33<12:10>	IPC33<9:8>	Yes
Reserved	—	134	—	—	—	—	—	—
Reserved	—	135	—	—	—	—	—	—
Reserved	—	136	—	—	—	—	—	—
Reserved	—	137	—	—	—	—	—	—
Reserved	—	138	—	—	—	—	—	—
ADC Data 33	_ADC_DATA33_VECTOR	139	OFF139<17:1>	IFS4<11>	IEC4<11>	IPC34<28:26>	IPC34<25:24>	Yes
ADC Data 34	_ADC_DATA34_VECTOR	140	OFF140<17:1>	IFS4<12>	IEC4<12>	IPC35<4:2>	IPC35<1:0>	Yes
ADC Data 35	_ADC_DATA35_VECTOR	141	OFF141<17:1>	IFS4<13>	IEC4<13>	IPC35<12:10>	IPC35<9:8>	Yes
ADC Data 36	_ADC_DATA36_VECTOR	142	OFF142<17:1>	IFS4<14>	IEC4<14>	IPC35<20:18>	IPC35<17:16>	Yes
ADC Data 37	_ADC_DATA37_VECTOR	143	OFF143<17:1>	IFS4<15>	IEC4<15>	IPC35<28:26>	IPC35<25:24>	Yes
ADC Data 38	_ADC_DATA38_VECTOR	144	OFF144<17:1>	IFS4<16>	IEC4<16>	IPC36<4:2>	IPC36<1:0>	Yes
ADC Data 39	_ADC_DATA39_VECTOR	145	OFF145<17:1>	IFS4<17>	IEC4<17>	IPC36<12:10>	IPC36<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 40	_ADC_DATA40_VECTOR	146	OFF146<17:1>	IFS4<18>	IEC4<18>	IPC36<20:18>	IPC36<17:16>	Yes
ADC Data 41	_ADC_DATA41_VECTOR	147	OFF147<17:1>	IFS4<19>	IEC4<19>	IPC36<28:26>	IPC36<25:24>	Yes
Reserved	—	148	—	—	—	—	—	—
Reserved	—	149	—	—	—	—	—	—
Reserved	—	150	—	—	—	—	—	—
ADC Data 45	_ADC_DATA45_VECTOR	151	OFF151<17:1>	IFS4<23>	IEC4<23>	IPC37<28:26>	IPC37<25:24>	Yes
ADC Data 46	_ADC_DATA46_VECTOR	152	OFF152<17:1>	IFS4<24>	IEC4<24>	IPC38<4:2>	IPC38<1:0>	Yes
ADC Data 47	_ADC_DATA47_VECTOR	153	OFF153<17:1>	IFS4<25>	IEC4<25>	IPC38<12:10>	IPC38<9:8>	Yes
ADC Data 48	_ADC_DATA48_VECTOR	154	OFF154<17:1>	IFS4<26>	IEC4<26>	IPC38<20:18>	IPC38<17:16>	Yes
ADC Data 49	_ADC_DATA49_VECTOR	155	OFF155<17:1>	IFS4<27>	IEC4<27>	IPC38<28:26>	IPC38<25:24>	Yes
ADC Data 50	_ADC_DATA50_VECTOR	156	OFF156<17:1>	IFS4<28>	IEC4<28>	IPC39<4:2>	IPC39<1:0>	Yes
ADC Data 51	_ADC_DATA51_VECTOR	157	OFF157<17:1>	IFS4<29>	IEC4<29>	IPC39<12:10>	IPC39<9:8>	Yes
ADC Data 52	_ADC_DATA52_VECTOR	158	OFF158<17:1>	IFS4<30>	IEC4<30>	IPC39<20:18>	IPC39<17:16>	Yes
ADC Data 53	_ADC_DATA53_VECTOR	159	OFF159<17:1>	IFS4<31>	IEC4<31>	IPC39<28:26>	IPC39<25:24>	Yes
Comparator 3 Interrupt	_COMPARATOR_3_VECTOR	160	OFF160<17:1>	IFS5<0>	IEC5<0>	IPC40<4:2>	IPC40<1:0>	Yes
Comparator 4 Interrupt	_COMPARATOR_4_VECTOR	161	OFF161<17:1>	IFS5<1>	IEC5<1>	IPC40<12:10>	IPC40<9:8>	Yes
Comparator 5 Interrupt	_COMPARATOR_5_VECTOR	162	OFF162<17:1>	IFS5<2>	IEC5<2>	IPC40<20:18>	IPC40<17:16>	Yes
Reserved	—	163	—	—	—	—	—	—
UART6 Fault	_UART6_FAULT_VECTOR	164	OFF164<17:1>	IFS5<4>	IEC5<4>	IPC41<4:2>	IPC41<1:0>	Yes
UART6 Receive Done	_UART6_RX_VECTOR	165	OFF165<17:1>	IFS5<5>	IEC5<5>	IPC41<12:10>	IPC41<9:8>	Yes
UART6 Transfer Done	_UART6_TX_VECTOR	166	OFF166<17:1>	IFS5<6>	IEC5<6>	IPC41<20:18>	IPC41<17:16>	Yes
CAN1 Global Interrupt	_CAN1_VECTOR	167	OFF167<17:1>	IFS5<7>	IEC5<7>	IPC41<28:26>	IPC41<25:24>	Yes
CAN2 Global Interrupt	_CAN2_VECTOR	168	OFF168<17:1>	IFS5<8>	IEC5<8>	IPC42<4:2>	IPC42<1:0>	Yes
QEI1 Interrupt	_QEI1_VECTOR	169	OFF169<17:1>	IFS5<9>	IEC5<9>	IPC42<12:10>	IPC42<9:8>	Yes
QEI2 Interrupt	_QEI2_VECTOR	170	OFF170<17:1>	IFS5<10>	IEC5<10>	IPC42<20:18>	IPC42<17:16>	Yes
PWM Primary Event	_PWM_PRI_VECTOR	171	OFF171<17:1>	IFS5<11>	IEC5<11>	IPC42<28:26>	IPC42<25:24>	Yes
PWM Sec Event	_PWM_SEC_VECTOR	172	OFF172<17:1>	IFS5<12>	IEC5<12>	IPC43<4:2>	IPC43<1:0>	Yes
PWM1 Combined Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM1_VECTOR	173	OFF173<17:1>	IFS5<13>	IEC5<13>	IPC43<12:10>	IPC43<9:8>	Yes
PWM2 Combined Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM2_VECTOR	174	OFF174<17:1>	IFS5<14>	IEC5<14>	IPC43<20:18>	IPC43<17:16>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
PWM3 Combined Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM3_VECTOR	175	OFF175<17:1>	IFS5<15>	IEC5<15>	IPC43<28:26>	IPC43<25:24>	Yes
PWM4 Combined Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM4_VECTOR	176	OFF176<17:1>	IFS5<16>	IEC5<16>	IPC44<4:2>	IPC44<1:0>	Yes
PWM5 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM5_VECTOR	177	OFF177<17:1>	IFS5<17>	IEC5<17>	IPC44<12:10>	IPC44<9:8>	Yes
PWM6 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM6_VECTOR	178	OFF178<17:1>	IFS5<18>	IEC5<18>	IPC44<20:18>	IPC44<17:16>	Yes
Reserved	—	179	—	—	—	—	—	—
Reserved	—	180	—	—	—	—	—	—
Reserved	—	181	—	—	—	—	—	—
DMA Channel 4	_DMA4_VECTOR	182	OFF182<17:1>	IFS5<22>	IEC5<22>	IPC45<20:18>	IPC45<17:16>	Yes
DMA Channel 5	_DMA5_VECTOR	183	OFF183<17:1>	IFS5<23>	IEC5<23>	IPC45<28:26>	IPC45<25:24>	Yes
DMA Channel 6	_DMA6_VECTOR	184	OFF184<17:1>	IFS5<24>	IEC5<24>	IPC46<4:2>	IPC46<1:0>	Yes
DMA Channel 7	_DMA7_VECTOR	185	OFF185<17:1>	IFS5<25>	IEC5<25>	IPC46<12:10>	IPC46<9:8>	Yes
Data EEPROM Global Interrupt	_DATA_EE_VECTOR	186	OFF186<17:1>	IFS5<26>	IEC5<26>	IPC46<20:18>	IPC46<17:16>	Yes
CAN3 Global Interrupt	_CAN3_VECTOR	187	OFF187<17:1>	IFS5<27>	IEC5<27>	IPC46<28:26>	IPC46<25:24>	Yes
CAN4 Global Interrupt	_CAN4_VECTOR	188	OFF188<17:1>	IFS5<28>	IEC5<28>	IPC47<4:2>	IPC47<1:0>	Yes
QEI3 Interrupt	_QEI2_VECTOR	189	OFF189<17:1>	IFS5<29>	IEC5<29>	IPC47<12:10>	IPC47<9:8>	Yes
QEI4 Interrupt	_QEI3_VECTOR	190	OFF190<17:1>	IFS5<30>	IEC5<30>	IPC47<20:18>	IPC47<17:16>	Yes
QEI5 Interrupt	_QEI5_VECTOR	191	OFF191<17:1>	IFS5<31>	IEC5<31>	IPC47<28:26>	IPC47<25:24>	Yes
QEI6 Interrupt	_QEI6_VECTOR	192	OFF192<17:1>	IFS6<0>	IEC6<0>	IPC48<4:2>	IPC48<1:0>	Yes
Reserved	—	193	—	—	—	—	—	—
Reserved	—	194	—	—	—	—	—	—
Reserved	—	195	—	—	—	—	—	—
Reserved	—	196	—	—	—	—	—	—
Input Capture 10 Error	_INPUT_CAPTURE_10_ERROR_VECTOR	197	OFF197<17:1>	IFS6<5>	IEC6<5>	IPC49<12:10>	IPC49<9:8>	Yes
Input Capture 10	_INPUT_CAPTURE_10_VECTOR	198	OFF198<17:1>	IFS6<6>	IE6<6>	IPC49<20:18>	IPC49<17:16>	Yes
Output Compare 10	_OUTPUT_COMPARE_10_VECTOR	199	OFF199<17:1>	IFS6<7>	IEC6<7>	IPC49<28:26>	IPC49<25:24>	Yes
Input Capture 11 Error	_INPUT_CAPTURE_11_ERROR_VECTOR	200	OFF200<17:1>	IFS6<8>	IEC6<8>	IPC50<4:2>	IPC50<1:0>	Yes
Input Capture 11	_INPUT_CAPTURE_11_VECTOR	201	OFF201<17:1>	IFS6<9>	IEC6<9>	IPC50<12:10>	IPC50<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Output Compare 11	_OUTPUT_COMPARE_11_VECTOR	202	OFF202<17:1>	IFS6<10>	IEC6<10>	IPC50<20:18>	IPC50<17:16>	Yes
Input Capture 12 Error	_INPUT_CAPTURE_12_ERROR_VECTOR	203	OFF203<17:1>	IFS6<11>	IEC6<11>	IPC50<28:26>	IPC50<25:24>	Yes
Input Capture 12	_INPUT_CAPTURE_12_VECTOR	204	OFF204<17:1>	IFS6<12>	IEC6<12>	IPC51<4:2>	IPC51<1:0>	Yes
Output Compare 12	_OUTPUT_COMPARE_12_VECTOR	205	OFF205<17:1>	IFS6<13>	IEC6<13>	IPC51<12:10>	IPC51<9:8>	Yes
Input Capture 13 Error	_INPUT_CAPTURE_13_ERROR_VECTOR	206	OFF206<17:1>	IFS6<14>	IEC6<14>	IPC51<20:18>	IPC51<17:16>	Yes
Input Capture 13	_INPUT_CAPTURE_13_VECTOR	207	OFF207<17:1>	IFS6<15>	IEC6<15>	IPC51<28:26>	IPC51<25:24>	Yes
Output Compare 13	_OUTPUT_COMPARE_13_VECTOR	208	OFF208<17:1>	IFS6<16>	IEC6<16>	IPC52<4:2>	IPC52<1:0>	Yes
Input Capture 14 Error	_INPUT_CAPTURE_14_ERROR_VECTOR	209	OFF209<17:1>	IFS6<17>	IEC6<17>	IPC52<12:10>	IPC52<9:8>	Yes
Input Capture 14	_INPUT_CAPTURE_14_VECTOR	210	OFF210<17:1>	IFS6<18>	IEC6<18>	IPC52<20:18>	IPC52<17:16>	Yes
Output Compare 14	_OUTPUT_COMPARE_14_VECTOR	211	OFF211<17:1>	IFS6<19>	IEC6<19>	IPC52<28:26>	IPC52<25:24>	Yes
Input Capture 15 Error	_INPUT_CAPTURE_15_ERROR_VECTOR	212	OFF212<17:1>	IFS6<20>	IEC6<20>	IPC53<4:2>	IPC53<1:0>	Yes
Input Capture 15	_INPUT_CAPTURE_15_VECTOR	213	OFF213<17:1>	IFS6<21>	IEC6<21>	IPC53<12:10>	IPC53<9:8>	Yes
Output Compare 15	_OUTPUT_COMPARE_15_VECTOR	214	OFF214<17:1>	IFS6<22>	IEC6<22>	IPC53<20:18>	IPC53<17:16>	Yes
Input Capture 16 Error	_INPUT_CAPTURE_16_ERROR_VECTOR	215	OFF215<17:1>	IFS6<23>	IEC6<23>	IPC53<28:26>	IPC53<25:24>	Yes
Input Capture 16	_INPUT_CAPTURE_16_VECTOR	216	OFF216<17:1>	IFS6<24>	IEC6<24>	IPC54<4:2>	IPC54<1:0>	Yes
Output Compare 16	_OUTPUT_COMPARE_16_VECTOR	217	OFF217<17:1>	IFS6<25>	IEC6<25>	IPC54<12:10>	IPC54<9:8>	Yes
SPI3 Fault	_SPI3_FAULT_VECTOR	218	OFF218<17:1>	IFS6<26>	IEC6<26>	IPC54<20:18>	IPC54<17:16>	Yes
SPI3 Receive Done	_SPI3_RX_VECTOR	219	OFF219<17:1>	IFS6<27>	IEC6<27>	IPC54<28:26>	IPC54<25:24>	Yes
SPI3 Transfer Done	_SPI3_TX_VECTOR	220	OFF220<17:1>	IFS6<28>	IEC6<28>	IPC55<4:2>	IPC55<1:0>	Yes
SPI4 Fault	_SPI4_FAULT_VECTOR	221	OFF221<17:1>	IFS6<29>	IEC6<29>	IPC55<12:10>	IPC55<9:8>	Yes
SPI4 Receive Done	_SPI4_RX_VECTOR	222	OFF222<17:1>	IFS6<30>	IEC6<30>	IPC55<20:18>	IPC55<17:16>	Yes
SPI4 Transfer Done	_SPI4_TX_VECTOR	223	OFF223<17:1>	IFS6<31>	IEC6<31>	IPC55<28:26>	IPC55<25:24>	Yes
SPI5 Fault	_SPI5_FAULT_VECTOR	224	OFF224<17:1>	IFS7<0>	IEC7<0>	IPC56<4:2>	IPC56<1:0>	Yes
SPI5 Receive Done	_SPI5_RX_VECTOR	225	OFF225<17:1>	IFS7<1>	IEC7<1>	IPC56<12:10>	IPC56<9:8>	Yes
SPI5 Transfer Done	_SPI5_TX_VECTOR	226	OFF226<17:1>	IFS7<2>	IEC7<2>	IPC56<20:18>	IPC56<17:16>	Yes
SPI6 Fault	_SPI6_FAULT_VECTOR	227	OFF227<17:1>	IFS7<3>	IEC7<3>	IPC56<28:26>	IPC56<25:24>	Yes
SPI6 Receive Done	_SPI6_RX_VECTOR	228	OFF228<17:1>	IFS7<4>	IEC7<4>	IPC57<4:2>	IPC57<1:0>	Yes
SPI6 Transfer Done	_SPI6_TX_VECTOR	229	OFF229<17:1>	IFS7<5>	IEC7<5>	IPC57<12:10>	IPC57<9:8>	Yes
System Bus Protection Violation	_SYSTEM_BUS_PROTECTION_VECTOR	230	OFF230<17:1>	IFS7<6>	IEC7<6>	IPC57<20:18>	IPC57<17:16>	Yes
Reserved	—	231	—	—	—	—	—	—
Reserved	—	232	—	—	—	—	—	—

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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TABLE 8-3: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Reserved	—	233	—	—	—	—	—	—
Reserved	—	234	—	—	—	—	—	—
Reserved	—	235	—	—	—	—	—	—
Reserved	—	236	—	—	—	—	—	—
Reserved	—	237	—	—	—	—	—	—
PWM7 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM7_VECTOR	238	OFF238<17:1>	IFS7<14>	IEC7<14>	IPC59<20:18>	IPC59<17:16>	Yes
PWM8 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM8_VECTOR	239	OFF239<17:1>	IFS7<15>	IEC7<15>	IPC59<28:26>	IPC59<25:24>	Yes
PWM9 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM9_VECTOR	240	OFF240<17:1>	IFS7<16>	IEC7<16>	IPC60<4:2>	IPC60<1:0>	Yes
PWM10 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM10_VECTOR	241	OFF241<17:1>	IFS7<17>	IEC7<17>	IPC60<12:10>	IPC60<9:8>	Yes
PWM11 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM11_VECTOR	242	OFF242<17:1>	IFS7<18>	IEC7<18>	IPC60<20:18>	IPC60<17:16>	Yes
PWM12 Interrupt (Period, Fault, Trigger, Current-Limit)	_PWM12_VECTOR	243	OFF243<17:1>	IFS7<19>	IEC7<19>	IPC60<28:26>	IPC60<25:24>	Yes
USB2 Combined Interrupt(2)	_USB_2_VECTOR	244	OFF244<17:1>	IFS7<20>	IEC7<20>	IPC61<4:2>	IPC61<1:0>	Yes
ADC Digital Comparator 3	_ADC_DC3_VECTOR	245	OFF245<17:1>	IFS7<21>	IEC7<21>	IPC61<12:10>	IPC61<9:8>	Yes
ADC Digital Comparator 4	_ADC_DC4_VECTOR	246	OFF246<17:1>	IFS7<22>	IEC7<22>	IPC61<20:18>	IPC61<17:16>	Yes
Reserved	—	247	—	—	—	—	—	—
Reserved	—	248	—	—	—	—	—	—
Reserved	—	249	—	—	—	—	—	—
Reserved	—	250	—	—	—	—	—	—
Reserved	—	251	—	—	—	—	—	—
Reserved	—	252	—	—	—	—	—	—
Reserved	—	253	—	—	—	—	—	—
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	254	OFF254<17:1>	IFS7<30>	IEC7<30>	IPC63<20:18>	IPC63<17:16>	—
Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	255	OFF255<17:1>	IFS7<31>	IEC7<31>	IPC63<28:26>	IPC63<25:24>	—
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

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8.3 Interrupt Control Registers

TABLE 8-4: INTERRUPT REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	INTCON	31:16	SWNMIKEY<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
0010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
0020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
0030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
0040	IFS0(7)	31:16	FCEIF	RTCCIF	—	—	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
0050	IFS1(7)	31:16	U3RXIF	U3EIF	—	—	—	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	SPI2RXIF	SPI2EIF	PMPEIF	PMPIF	CNGIF	CNFIF	CNEIF	0000
		15:0	CNDIF	CNCIF	CNBIF	CNAIF	—	—	—	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	USB1IF	CMP2IF	CMP1IF	0000
0060	IFS2(7)	31:16	AD1DC2IF	AD1DC1IF	-	AD1IF	OC9IF	IC9IF	IC9EIF	T9IF	OC8IF	IC8IF	IC8EIF	T8IF	OC7IF	IC7IF	IC7EIF	T7IF	0000
		15:0	OC6IF	IC6IF	IC6EIF	T6IF	DMA3IF	DMA2IF	DMA1IF	DMA0IF	CTMUIF	U5TXIF	U5RXIF	U5EIF	U4TXIF	U4RXIF	U4EIF	U3TXIF	0000
0070	IFS3(7)	31:16	AD1D21IF	AD1D20IF	AD1D19IF	AD1D18IF	AD1D17IF	AD1D16IF	AD1D15IF	AD1D14IF	AD1D13IF	AD1D12IF	AD1D11IF	AD1D10IF	AD1D9IF	AD1D8IF	AD1D7IF	AD1D6IF	0000
		15:0	AD1D5IF	AD1D4IF	AD1D3IF	AD1D2IF	AD1D1IF	AD1D0IF	AD1G1IF	AD1FCBTIF	AD1RSIF	AD1ARIF	AD1EOSIF	AD1F1IF	AD1DF4IF	AD1DF3IF	AD1DF2IF	AD1DF1IF	0000
0080	IFS4(7)	31:16	AD1D53IF	AD1D52IF	AD1D51IF	AD1D50IF	AD1D49IF	AD1D48IF	AD1D47IF	AD1D46IF	AD1D45IF	—	—	—	AD1D41IF	AD1D40IF	AD1D39IF	AD1D38IF	0000
		15:0	AD1D37IF	AD1D36IF	AD1D35IF	AD1D34IF	AD1D33IF	—	—	—	—	—	AD1D27IF	AD1D26IF	AD1D25IF	AD1D24IF	AD1D23IF	AD1D22IF	0000
0090	IFS5(7)	31:16	QEI5IF	QEI4IF	QEI3IF	CAN4IF(3)	CAN3IF(3)	DATAEEIF	DMA7IF	DMA6IF	DMA5IF	DMA4IF	—	—	—	PWM6IF	PWM5IF	PWM4IF	0000
		15:0	PWM3IF	PWM2IF	PWM1IF	PWM SEVTIF	PWM PEVTIF	QEI2IF	QEI1IF	CAN2IF(3)	CAN1IF(3)	U6TXIF	U6RXIF	U6EIF	—	CMP5IF	CMP4IF	CMP3IF	0000
00A0	IFS6(7)	31:16	SPI4TXIF	SPI4RXIF	SPI4EIF	SPI3TXIF	SPI3RXIF	SPI3EIF	OC16IF	IC16IF	IC16EIF	OC15IF	IC15IF	IC15EIF	OC14IF	C14IF	IC14EIF	OC13IF	0000
		15:0	IC13IF	IC13EIF	OC12IF	IC12IF	IC12EIF	OC11IF	IC11IF	IC11EIF	OC10IF	IC10IF	IC10EIF	—	—	—	—	QEI6IF	0000
00B0	IFS7(7)	31:16	—	CPCIF	—	—	—	—	—	—	—	AD1DC4IF	AD1DC3IF	USB2IF(2)	PWM12IF	PWM11IF	PWM10IF	PWM9IF	0000
		15:0	PWM8IF	PWM7IF	—	—	—	—	—	—	—	SBIF	SPI6TXIF	SPI6RXIF	SPI6EIF	SPI5TXIF	SPI5RXIF	SPI5EIF	0000
00C0	IEC0	31:16	FCEIE	RTCCIE	-	-	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
00D0	IEC1	31:16	U3RXIE	U3EIE	—	—	—	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	SPI2RXIE	SPI2EIE	PMPEIE	PMPIE	CNGIE	CNFIE	CNEIE	0000
		15:0	CNDIE	CNCIE	CNBIE	CNAIE	—	—	—	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	USB1IE	CMP2IE	CMP1IE	0000
00E0	IEC2	31:16	AD1DC2IE	AD1DC1IE	-	AD1IE	OC9IE	IC9IE	IC9EIE	T9IE	OC8IE	IC8IE	IC8EIE	T8IE	OC7IE	IC7IE	IC7EIE	T7IE	0000
		15:0	OC6IE	IC6IE	IC6EIE	T6IE	DMA3IE	DMA2IE	DMA1IE	DMA0IE	CTMUIE	U5TXIE	U5RXIE	U5EIE	U4TXIE	U4RXIE	U4EIE	U3TXIE	0000
00F0	IEC3	31:16	AD1D21IE	AD1D20IE	AD1D19IE	AD1D18IE	AD1D17IE	AD1D16IE	AD1D15IE	AD1D14IE	AD1D13IE	AD1D12IE	AD1D11IE	AD1D10IE	AD1D09IE	AD1D08IE	AD1D07IE	AD1D06IE	0000
		15:0	AD1D05IE	AD1D04IE	AD1D03IE	AD1D02IE	AD1D01IE	AD1D00IE	AD1G1IE	AD1FCBTIE	AD1RSIE	AD1ARIE	AD1EOSIE	AD1F1IE	AD1DF4IE	AD1DF3IE	AD1DF2IE	AD1DF1IE	0000
0100	IEC4	31:16	AD1D53IE	AD1D52IE	AD1D51IE	AD1D50IE	AD1D49IE	AD1D48IE	AD1D47IE	AD1D46IE	AD1D45IE	—	—	—	AD1D41IE	AD1D40IE	AD1D39IE	AD1D38IE	0000
		15:0	AD1D37IE	AD1D36IE	AD1D35IE	AD1D34IE	AD1D33IE	—	—	—	—	—	AD1D27IE	AD1D26IE	AD1D25IE	AD1D24IE	AD1D23IE	AD1D22IE	0000
0110	IEC5	31:16	QEI5IE	QEI4IE	QEI3IE	CAN4IE(3)	CAN3IE(3)	DATAEEIE	DMA7IE	DMA6IE	DMA5IE	DMA4IE	—	—	—	PWM6IE	PWM5IE	PWM4IE	0000
		15:0	PWM3IE	PWM2IE	PWM1IE	PWM SEVTIE	PWM PEVTIE	QEI2IE	QEI1IE	CAN2IE(3)	CAN1IE(3)	U6TXIE	U6RXIE	U6EIE	—	CMP5IE	CMP4IE	CMP3IE	0000
0120	IEC6	31:16	SPI4TXIE	SPI4RXIE	SPI4EIE	SPI3TXIE	SPI3RXIE	SPI3EIE	OC16IE	IC16IE	IC16EIE	OC15IE	IC15IE	IC15EIE	OC14IE	C14IE	IC14EIE	OC13IE	0000
		15:0	IC13IE	IC13EIE	OC12IE	IC12IE	IC12EIE	OC11IE	IC11IE	IC11EIE	OC10IE	IC10IE	IC10EIE	—	—	—	—	QEI6IE	0000
0130	IEC7	31:16	—	CPCIE	—	—	—	—	—	—	—	AD1DC4IE	AD1DC3IE	USB2IE(2)	PWM12IE	PWM11IE	PWM10IE	PWM9IE	0000
		15:0	—	—	—	—	—	—	—	—	—	SBIE	SPI6TXIE	SPI6RXIE	SPI6EIE	SPI5TXIE	SPI5RXIE	SPI5EIE	0000
0140	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
0150	IPC1	31:16	—	—	—	OC1IP<2:0>			OC1IS<1:0>		—	—	—	IC1IP<2:0>			IC1IS<1:0>		0000
		15:0	—	—	—	IC1EIP<2:0>			IC1EIS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
0160	IPC2	31:16	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	IC2EIP<2:0>			IC2EIS<1:0>		0000
		15:0	—	—	—	T2IP<2:0>			T2IS<1:0>		—	—	—	INT1IP<2:0>			INT1IS<1:0>		0000
0170	IPC3	31:16	—	—	—	IC3EIP<2:0>			IC3EIS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
		15:0	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
0180	IPC4	31:16	—	—	—	T4IP<2:0>			T4IS<1:0>		—	—	—	INT3IP<2:0>			INT3IS<1:0>		0000
		15:0	—	—	—	OC3IP<2:0>			OC3IS<1:0>		—	—	—	IC3IP<2:0>			IC3IS<1:0>		0000
0190	IPC5	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	IC4EIP<2:0>			IC4EIS<1:0>		0000
01A0	IPC6	31:16	—	—	—	OC5IP<2:0>			OC5IS<1:0>		—	—	—	IC5IP<2:0>			IC5IS<1:0>		0000
		15:0	—	—	—	IC5EIP<2:0>			IC5EIS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
01B0	IPC7	31:16	—	—	—	FCEIP<2:0>			FCEIS<1:0>		—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
01C0	IPC8	31:16	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		—	—	—	USB1IP<2:0>			USB1IS<1:0>		0000
		15:0	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
01D0	IPC9	31:16	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	U1EIP<2:0>			U1EIS<1:0>		0000
		15:0	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
01E0	IPC10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
01F0	IPC11	31:16	—	—	—	CNDIP<2:0>			CNDIS<1:0>		—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
		15:0	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
0200	IPC12	31:16	—	—	—	PMPIP<2:0>			PMPIS<1:0>		—	—	—	CNGIP<2:0>			CNGIS<1:0>		0000
		15:0	—	—	—	CNFIP<2:0>			CNFIS<1:0>		—	—	—	CNEIP<2:0>			CNEIS<1:0>		0000
0210	IPC13	31:16	—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		0000
		15:0	—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		—	—	—	PMPEIP<2:0>			PMPEIS<1:0>		0000
0220	IPC14	31:16	—	—	—	—	—	—	—	—	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		0000
		15:0	—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		—	—	—	U2EIP<2:0>			U2EIS<1:0>		0000
0230	IPC15	31:16	—	—	—	U3RXIP<2:0>			U3RXIS<1:0>		—	—	—	U3EIP<2:0>			U3EIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0240	IPC16	31:16	—	—	—	U4TXIP<2:0>			U4TXIS<1:0>		—	—	—	U4RXIP<2:0>			U4RXIS<1:0>		0000
		15:0	—	—	—	U4EIP<2:0>			U4EIS<1:0>		—	—	—	U3TXIP<2:0>			U3TXIS<1:0>		0000
0250	IPC17	31:16	—	—	—	CTMUIP<2:0>			CTMUIS<1:0>		—	—	—	U5TXIP<2:0>			U5TXIS<1:0>		0000
		15:0	—	—	—	U5RXIP<2:0>			U5RXIS<1:0>		—	—	—	U5EIP<2:0>			U5EIS<1:0>		0000
0260	IPC18	31:16	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
		15:0	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
0270	IPC19	31:16	—	—	—	OC6IP<2:0>			OC6IS<1:0>		—	—	—	IC6IP<2:0>			IC6IS<1:0>		0000
		15:0	—	—	—	IC6EIP<2:0>			IC6EIS<1:0>		—	—	—	T6IP<2:0>			T6IS<1:0>		0000
0280	IPC20	31:16	—	—	—	OC7IP<2:0>			OC7IS<1:0>		—	—	—	IC7IP<2:0>			IC7IS<1:0>		0000
		15:0	—	—	—	IC7EIP<2:0>			IC7EIS<1:0>		—	—	—	T7IP<2:0>			T7IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0290	IPC21	31:16	—	—	—	OC8IP<2:0>			OC8IS<1:0>		—	—	—	IC8IP<2:0>			IC8IS<1:0>		0000
		15:0	—	—	—	IC8EIP<2:0>			IC8EIS<1:0>		—	—	—	T8IP<2:0>			T8IS<1:0>		0000
02A0	IPC22	31:16	—	—	—	OC9IP<2:0>			OC9IS<1:0>		—	—	—	IC9IP<2:0>			IC9IS<1:0>		0000
		15:0	—	—	—	IC9EIP<2:0>			IC9EIS<1:0>		—	—	—	T9IP<2:0>			T9IS<1:0>		0000
02B0	IPC23	31:16	—	—	—	AD1DC2IP<2:0>			AD1DC2IS<1:0>		—	—	—	AD1DC1IP<2:0>			AD1DC1IS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	AD1IP<2:0>			AD1IS<1:0>		0000
02C0	IPC24	31:16	—	—	—	AD1DF4IP<2:0>			AD1DF4IS<1:0>		—	—	—	AD1DF3IP<2:0>			AD1DF3IS<1:0>		0000
		15:0	—	—	—	AD1DF2IP<2:0>			AD1DF2IS<1:0>		—	—	—	AD1DF1IP<2:0>			AD1DF1IS<1:0>		0000
02D0	IPC25	31:16	—	—	—	AD1RSIP<2:0>			AD1RSIS<1:0>		—	—	—	AD1ARIP<2:0>			AD1ARIS<1:0>		0000
		15:0	—	—	—	AD1EOSIP<2:0>			AD1EOSIS<1:0>		—	—	—	AD1F1IP<2:0>			AD1F1IS<1:0>		0000
02E0	IPC26	31:16	—	—	—	AD1D01IP<2:0>			AD1D01IS<1:0>		—	—	—	AD1D00IP<2:0>			AD1D00IS<1:0>		0000
		15:0	—	—	—	AD1G1IP<2:0>			AD1G1IS<1:0>		—	—	—	AD1FCBTIP<2:0>			AD1FCBTIS<1:0>		0000
02F0	IPC27	31:16	—	—	—	AD1D05IP<2:0>			AD1D05IS<1:0>		—	—	—	AD1D04IP<2:0>			AD1D04IS<1:0>		0000
		15:0	—	—	—	AD1D03IP<2:0>			AD1D03IS<1:0>		—	—	—	AD1D02IP<2:0>			AD1D02IS<1:0>		0000
0300	IPC28	31:16	—	—	—	AD1D09IP<2:0>			AD1D09IS<1:0>		—	—	—	AD1D08IP<2:0>			AD1D08IS<1:0>		0000
		15:0	—	—	—	AD1D07IP<2:0>			AD1D07IS<1:0>		—	—	—	AD1D06IP<2:0>			AD1D06IS<1:0>		0000
0310	IPC29	31:16	—	—	—	AD1D13IP<2:0>			AD1D13IS<1:0>		—	—	—	AD1D12IP<2:0>			AD1D12IS<1:0>		0000
		15:0	—	—	—	AD1D11IP<2:0>			AD1D11IS<1:0>		—	—	—	AD1D10IP<2:0>			AD1D10IS<1:0>		0000
0320	IPC30	31:16	—	—	—	AD1D17IP<2:0>			AD1D17IS<1:0>		—	—	—	AD1D16IP<2:0>			AD1D16IS<1:0>		0000
		15:0	—	—	—	AD1D15IP<2:0>			AD1D15IS<1:0>		—	—	—	AD1D14IP<2:0>			AD1D14IS<1:0>		0000
0330	IPC31	31:16	—	—	—	AD1D21IP<2:0>			AD1D21IS<1:0>		—	—	—	AD1D20IP<2:0>			AD1D20IS<1:0>		0000
		15:0	—	—	—	AD1D19IP<2:0>			AD1D19IS<1:0>		—	—	—	AD1D18IP<2:0>			AD1D18IS<1:0>		0000
0340	IPC32	31:16	—	—	—	AD1D25IP<2:0>			AD1D25IS<1:0>		—	—	—	AD1D24IP<2:0>			AD1D24IS<1:0>		0000
		15:0	—	—	—	AD1D23IP<2:0>			AD1D23IS<1:0>		—	—	—	AD1D22IP<2:0>			AD1D22IS<1:0>		0000
0350	IPC33	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AD1D27IP<2:0>			AD1D27IS<1:0>		—	—	—	AD1D26IP<2:0>			AD1D26IS<1:0>		0000
0360	IPC34	31:16	—	—	—	AD1D33IP<2:0>			AD1D33IS<1:0>		—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0370	IPC35	31:16	—	—	—	AD1D37IP<2:0>			AD1D37IS<1:0>		—	—	—	AD1D36IP<2:0>			AD1D36IS<1:0>		0000
		15:0	—	—	—	AD1D35IP<2:0>			AD1D35IS<1:0>		—	—	—	AD1D34IP<2:0>			AD1D34IS<1:0>		0000
0380	IPC36	31:16	—	—	—	AD1D41IP<2:0>			AD1D41IS<1:0>		—	—	—	AD1D40IP<2:0>			AD1D40IS<1:0>		0000
		15:0	—	—	—	AD1D39IP<2:0>			AD1D39IS<1:0>		—	—	—	AD1D38IP<2:0>			AD1D38IS<1:0>		0000
0390	IPC37	31:16	—	—	—	AD1D45IP<2:0>			AD1D45IS<1:0>		—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
03A0	IPC38	31:16	—	—	—	AD1D49IP<2:0>			AD1D49IS<1:0>		—	—	—	AD1D48IP<2:0>			AD1D48IS<1:0>		0000
		15:0	—	—	—	AD1D47IP<2:0>			AD1D47IS<1:0>		—	—	—	AD1D46IP<2:0>			AD1D46IS<1:0>		0000
03B0	IPC39	31:16	—	—	—	AD1D53IP<2:0>			AD1D53IS<1:0>		—	—	—	AD1D52IP<2:0>			AD1D52IS<1:0>		0000
		15:0	—	—	—	AD1D51IP<2:0>			AD1D51IS<1:0>		—	—	—	AD1D50IP<2:0>			AD1D50IS<1:0>		0000
03C0	IPC40	31:16	—	—	—	—	—	—	—	—	—	—	—	CMP5IP<2:0>			CMP5IS<1:0>		0000
		15:0	—	—	—	CMP4IP<2:0>			CMP4IS<1:0>		—	—	—	CMP3IP<2:0>			CMP3IS<1:0>		0000
03D0	IPC41	31:16	—	—	—	CAN1IP<2:0>(3)			CAN1IS<1:0>(3)		—	—	—	U6TXIP<2:0>			U6TXIS<1:0>		0000
		15:0	—	—	—	U6RXIP<2:0>			U6RXIS<1:0>		—	—	—	U6EIP<2:0>			U6EIS<1:0>		0000
03E0	IPC42	31:16	—	—	—	PWMPEVTIP<2:0>			PWMSEVTIP<1:0>		—	—	—	QEI2IP<2:0>			QEI2SIP<1:0>		0000
		15:0	—	—	—	QEI1IP<2:0>			QEI1SIP<1:0>		—	—	—	CAN2IP<2:0>(3)			CAN2IS<1:0>(3)		0000
03F0	IPC43	31:16	—	—	—	PWM3IP<2:0>			PWM3SIP<1:0>		—	—	—	PWM2IP<2:0>			PWM2SIP<1:0>		0000
		15:0	—	—	—	PWM1IP<2:0>			PWM1SIP<1:0>		—	—	—	PWMSEVTIP<2:0>			PWMSEVTSIP<1:0>		0000
0400	IPC44	31:16	—	—	—	—	—	—	—	—	—	—	—	PWM6IP<2:0>			PWM6SIP<1:0>		0000
		15:0	—	—	—	PWM5IP<2:0>			PWM5SIP<1:0>		—	—	—	PWM4IP<2:0>			PWM4SIP<1:0>		0000
0410	IPC45	31:16	—	—	—	DMA5IP<2:0>			DMA5IS<1:0>		—	—	—	DMA4IP<2:0>			DMA4IS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0420	IPC46	31:16	—	—	—	CAN3IP<2:0>(3)			CAN3IS<1:0>(3)		—	—	—	DATAEEIP<2:0>			DATAEEIS<1:0>		0000
		15:0	—	—	—	DMA7IP<2:0>			DMA7IS<1:0>		—	—	—	DMA6IP<2:0>			DMA6IS<1:0>		0000
0430	IPC47	31:16	—	—	—	QEI5IP<2:0>			QEI5SIP<1:0>		—	—	—	QEI4IP<2:0>			QEI4SIP<1:0>		0000
		15:0	—	—	—	QEI3IP<2:0>			QEI3SIP<1:0>		—	—	—	CAN4IP<2:0>(3)			CAN4IS<1:0>(3)		0000
0440	IPC48	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	QEI6IP<2:0>			QEI6SIP<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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0450	IPC49	31:16	—	—	—	OC10IP<2:0>			OC10IS<1:0>		—	—	—	IC10IP<2:0>			IC10IS<1:0>		0000
		15:0	—	—	—	IC10EIP<2:0>			IC10EIS<1:0>		—	—	—	—	—	—	—	—	0000
0460	IPC50	31:16	—	—	—	IC12EIP<2:0>			IC12EIS<1:0>		—	—	—	OC11IP<2:0>			OC11IS<1:0>		0000
		15:0	—	—	—	IC11IP<2:0>			IC11IS<1:0>		—	—	—	IC11EIP<2:0>			IC11EIS<1:0>		0000
0470	IPC51	31:16	—	—	—	IC13IP<2:0>			IC13IS<1:0>		—	—	—	IC13EIP<2:0>			IC13EIS<1:0>		0000
		15:0	—	—	—	OC12IP<2:0>			OC12IS<1:0>		—	—	—	IC12IP<2:0>			IC12IS<1:0>		0000
0480	IPC52	31:16	—	—	—	OC14IP<2:0>			OC14IS<1:0>		—	—	—	C14IP<2:0>			C14IS<1:0>		0000
		15:0	—	—	—	IC14EIP<2:0>			IC14EIS<1:0>		—	—	—	OC13IP<2:0>			OC13IS<1:0>		0000
0490	IPC53	31:16	—	—	—	IC16EIP<2:0>			IC16EIS<1:0>		—	—	—	OC15IP<2:0>			OC15IS<1:0>		0000
		15:0	—	—	—	IC15IP<2:0>			IC15IS<1:0>		—	—	—	IC15EIP<2:0>			IC15EIS<1:0>		0000
04A0	IPC54	31:16	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>		—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		0000
		15:0	—	—	—	OC16IP<2:0>			OC16IS<1:0>		—	—	—	IC16IP<2:0			IC16IS<1:0>		0000
04B0	IPC55	31:16	—	—	—	SPI4TXIP<2:0>			SPI4TXIS<1:0>		—	—	—	SPI4RXIP<2:0>			SPI4RXIS<1:0>		0000
		15:0	—	—	—	SPI4EIP<2:0>			SPI4EIS<1:0>		—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
04C0	IPC56	31:16	—	—	—	SPI6EIP<2:0>			SPI6EIS<1:0>		—	—	—	SPI5TXIP<2:0>			SPI5TXIS<1:0>		0000
		15:0	—	—	—	SPI5RXIP<2:0>			SPI5RXIS<1:0>		—	—	—	SPI5EIP<2:0>			SPI5EIS<1:0>		0000
04D0	IPC57	31:16	—	—	—	—	—	—	—	—	—	—	—	SBIP<2:0>			SBIS<1:0>		0000
		15:0	—	—	—	SPI6TXIP<2:0>			SPI6TXIS<1:0>		—	—	—	SPI6RXIP<2:0>			SPI6RXIS<1:0>		0000
04F0	IPC59	31:16	—	—	—	PWM8IP<2:0>			PWM8SIP<1:0>		—	—	—	PWM7IP<2:0>			PWM7SIP<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0500	IPC60	31:16	—	—	—	PWM12IP<2:0>			PWM12SIP<1:0>		—	—	—	PWM11IP<2:0>			PWM11SIP<1:0>		0000
		15:0	—	—	—	PWM10IP<2:0>			PWM10SIP<1:0>		—	—	—	PWM9IP<2:0>			PWM9SIP<1:0>		0000
0510	IPC61	31:16	—	—	—	—	—	—	—	—	—	—	—	AD1DC4IP<2:0>			AD1DC4IS<1:0>		0000
		15:0	—	—	—	AD1DC3IP<2:0>			AD1DC3IS<1:0>		—	—	—	USB2IP<2:0>(2)			USB2IS<1:0>(2)		0000
0530	IPC63	31:16	—	—	—	—	—	—	—	—	—	—	—	CPCIP<2:0>			CPCIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0540	OFF000	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0544	OFF001	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0548	OFF002	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
054C	OFF003	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0550	OFF004	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0554	OFF005	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0558	OFF006	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
055C	OFF007	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0560	OFF008	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0564	OFF009	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0568	OFF010	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
056C	OFF011	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0570	OFF012	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0574	OFF013	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0578	OFF014	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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3: This bit is not available on devices without a CAN module.

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7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
057C	OFF015	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0580	OFF016	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0584	OFF017	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0588	OFF018	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
058C	OFF019	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0590	OFF020	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0594	OFF021	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0598	OFF022	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
059C	OFF023	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05A0	OFF024	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05A4	OFF025	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05A8	OFF026	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05AC	OFF027	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05B8	OFF030	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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3: This bit is not available on devices without a CAN module.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05BC	OFF031	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C0	OFF032	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C4	OFF033	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C8	OFF034	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05CC	OFF035	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D0	OFF036	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D4	OFF037	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D8	OFF038	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05DC	OFF039	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E0	OFF040	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E4	OFF041	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E8	OFF042	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05EC	OFF043	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F0	OFF044	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
05F4	OFF045	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F8	OFF046	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05FC	OFF047	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0600	OFF048	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0604	OFF049	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0608	OFF050	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
060C	OFF051	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0610	OFF052	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0614	OFF053	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0618	OFF054	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
061C	OFF055	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0620	OFF056	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0624	OFF057	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0628	OFF058	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
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062C	OFF059	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0630	OFF060	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0634	OFF061	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0638	OFF062	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
063C	OFF063	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0640	OFF064	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0644	OFF065	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0648	OFF066	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
064C	OFF067	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0650	OFF068	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0654	OFF069	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0658	OFF070	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
065C	OFF071	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0660	OFF072	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

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7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0664	OFF073	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0668	OFF074	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
066C	OFF075	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0670	OFF076	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0674	OFF077	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0678	OFF078	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
067C	OFF079	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0680	OFF080	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0684	OFF081	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0688	OFF082	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
068C	OFF083	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0690	OFF084	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0694	OFF085	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0698	OFF086	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
069C	OFF087	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A0	OFF088	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A4	OFF089	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A8	OFF090	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06AC	OFF091	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06B0	OFF092	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06B8	OFF094	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06BC	OFF095	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06C0	OFF096	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06C4	OFF097	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06C8	OFF098	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06CC	OFF099	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06D0	OFF100	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06D4	OFF101	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
06D8	OFF102	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06DC	OFF103	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06E0	OFF104	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06E4	OFF105	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06E8	OFF106	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06EC	OFF107	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F0	OFF108	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F4	OFF109	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06F8	OFF110	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06FC	OFF111	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0700	OFF112	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0704	OFF113	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0708	OFF114	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
070C	OFF115	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0710	OFF116	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0714	OFF117	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0718	OFF118	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
071C	OFF119	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0720	OFF120	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0724	OFF121	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0728	OFF122	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
072C	OFF123	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0730	OFF124	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0734	OFF125	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0738	OFF126	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
073C	OFF127	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0740	OFF128	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0744	OFF129	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0748	OFF130	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
074C	OFF131	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0750	OFF132	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0754	OFF133	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
076C	OFF139	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0770	OFF140	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0774	OFF141	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0778	OFF142	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
077C	OFF143	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0780	OFF144	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0784	OFF145	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0788	OFF146	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
078C	OFF147	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0790	OFF148	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0794	OFF149	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0798	OFF150	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
079C	OFF151	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A0	OFF152	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A4	OFF153	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07A8	OFF154	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07AC	OFF155	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B0	OFF156	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B4	OFF157	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07B8	OFF158	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07BC	OFF159	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C0	OFF160	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C4	OFF161	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07C8	OFF162	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07D0	OFF164	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D4	OFF165	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07D8	OFF166	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07DC	OFF167	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E4	OFF169	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E8	OFF170	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07EC	OFF171	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F0	OFF172	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F4	OFF173	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F8	OFF174	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07FC	OFF175	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0800	OFF176	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0804	OFF177	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0808	OFF178	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
080C	OFF179	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0810	OFF180	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0814	OFF181	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0818	OFF182	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
081C	OFF183	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0820	OFF184	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0824	OFF185	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0828	OFF186	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
082C	OFF187	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0830	OFF188	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0834	OFF189	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0838	OFF190	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
083C	OFF191	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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3: This bit is not available on devices without a CAN module.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0840	OFF192	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0848	OFF194	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
084C	OFF195	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0850	OFF196	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0854	OFF197	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0858	OFF198	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
085C	OFF199	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0860	OFF200	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0864	OFF201	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0868	OFF202	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
086C	OFF203	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0870	OFF204	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0874	OFF205	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0878	OFF206	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
087C	OFF207	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0880	OFF208	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0884	OFF209	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0888	OFF210	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
088C	OFF211	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0890	OFF212	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0894	OFF213	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0898	OFF214	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
089C	OFF215	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08A0	OFF216	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08A4	OFF217	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08A8	OFF218	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08AC	OFF219	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08B0	OFF220	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
08B4	OFF221	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08B8	OFF222	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08BC	OFF223	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08C0	OFF224	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08C4	OFF225	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08C8	OFF226	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08CC	OFF227	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08D0	OFF228	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08D4	OFF229	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08D8	OFF230	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08F8	OFF238	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
08FC	OFF239	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0900	OFF240	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0904	OFF241	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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TABLE 8-4: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0908	OFF242	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
090C	OFF243	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0910	OFF244	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0914	OFF245	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0918	OFF246	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0938	OFF254	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0938C	OFF255	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on 64-pin devices.

3: This bit is not available on devices without a CAN module.

4: This bit is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 22 is not available on 64-pin devices.

7: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition has occurred. The IFSx bits are persistent, they must be cleared if they are set by user software after an IFSx user bit interrogation.

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REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMIKEY<7:0>							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	MVEC	—	TPC<2:0>		
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **NMIKEY<7:0>:** Software Generated NMI Key Register bits
Software NMI event when the correct key (4Eh) is written.
Software NMI event not generated when any other value (not the key) is written.

bit 23-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multi Vector Configuration bit
1 = Interrupt controller configured for multi vectored mode
0 = Interrupt controller configured for single vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
001 = Interrupts of group priority 1 start the Interrupt Proximity timer
000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

REGISTER 8-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
1111 = Reserved
.
.
.
0010 = Reserved
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0 (default)

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1111 = Reserved
.
.
.
0010 = Reserved
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0 (default)

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
1111 = Reserved
.
.
.
0010 = Reserved
0001 = Interrupt with a priority level of 5 uses Shadow Set 1
0000 = Interrupt with a priority level of 5 uses Shadow Set 0 (default)

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
1111 = Reserved
.
.
.
0010 = Reserved
0001 = Interrupt with a priority level of 4 uses Shadow Set 1
0000 = Interrupt with a priority level of 4 uses Shadow Set 0 (default)

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

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REGISTER 8-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0 (default)

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0 (default)

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0 (default)

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

REGISTER 8-3: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	SRIPL<2:0>		
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SIRQ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits for Single Vector Mode bits
111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits
11111111-00000000 = The last interrupt request number serviced by the CPU

REGISTER 8-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits
Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

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REGISTER 8-5: IFSx: INTERRUPT FLAG STATUS REGISTER 'x' ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS9	IFS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS7	IFS6	IFS5	IFS4	IFS3	IFS2	IFS1	IFS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS31-IFS0:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 8-3 for the exact bit definitions.

REGISTER 8-6: IECx: INTERRUPT ENABLE CONTROL REGISTER 'x' ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC31-IEC0:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 8-3 for the exact bit definitions.

REGISTER 8-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER 'x' ('x' = 0-63)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 8-3 for the exact bit definitions.

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REGISTER 8-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER 'x' ('x' = 0-63) (CONTINUED)

bit 12-10 **IP1<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 9-8 **IS1<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP0<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS0<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

Note: This register represents a generic definition of the IPCx register. Refer to Table 8-3 for the exact bit definitions.

REGISTER 8-8: OFFx: INTERRUPT VECTOR ADDRESS OFFSET REGISTER (x = 0-190)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	VOFF<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VOFF<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	VOFF<7:1>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 17-1 **VOFF<17:1>:** Interrupt Vector 'x' Address Offset bits

bit 0 **Unimplemented:** Read as '0'

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9.0 OSCILLATOR CONFIGURATION

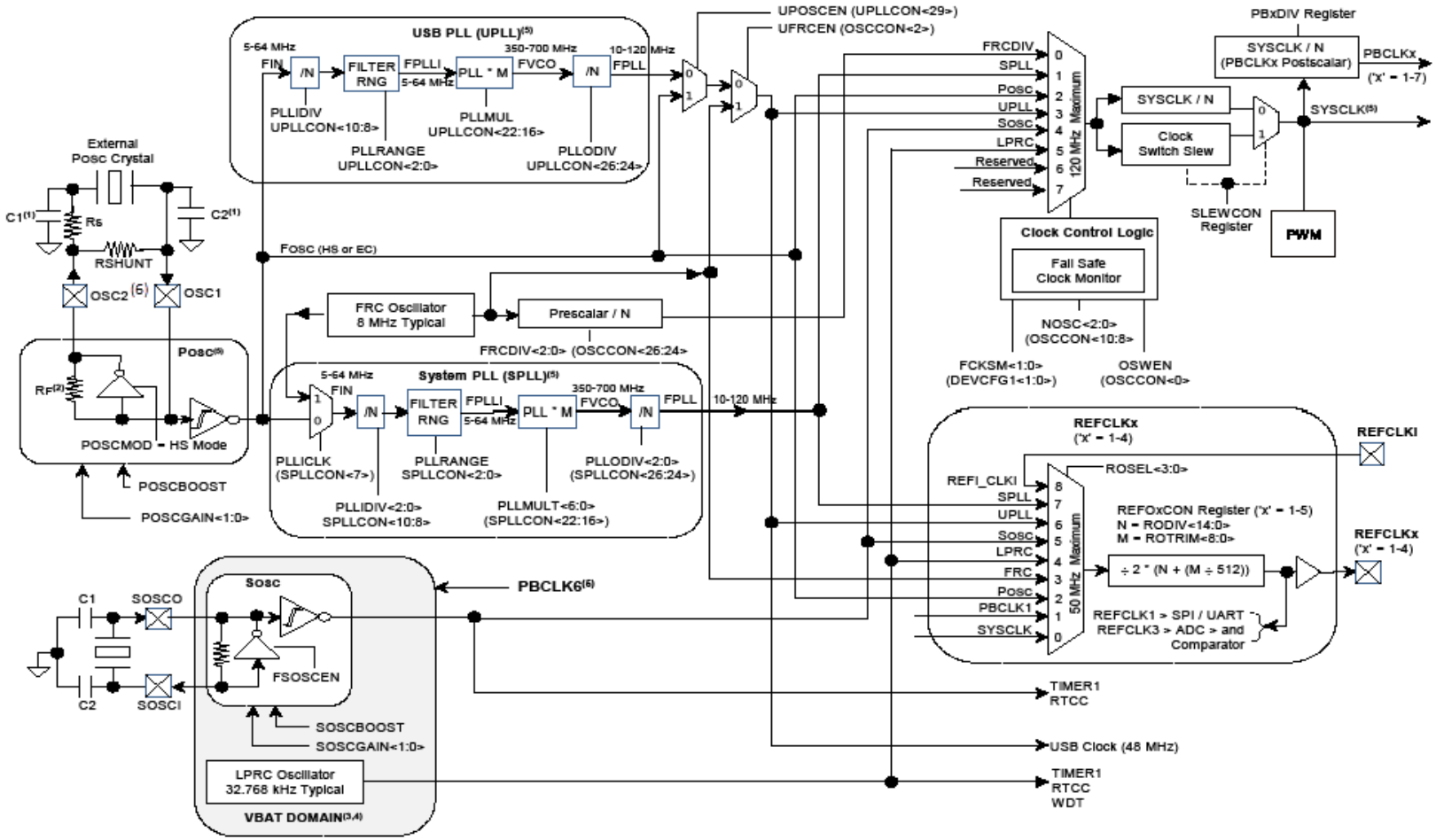
Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MK GP/MC oscillator system has the following modules and features:

- Five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shut-down with dedicated FRC
- Dedicated On-Chip PLL for USB modules
- Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility

A block diagram of the oscillator system is provided in Figure 9-1. The clock distribution is shown in Table 9-1.

FIGURE 9-1: PIC32MK GP/MC FAMILY OSCILLATOR DIAGRAM



Note 1: Refer to **2.0 "Guidelines for Getting Started with 32-bit MCUs"** for recommended external crystal component values and restrictions.
2: The internal POSC feedback resistor, RF, is typically in the range of 2 to 10 M.
3: The maximum PBCLK6 clock rate to the peripherals in the VBAT power domain is 30 MHz. This is not the power-up default and must be configured by the user before attempting any access to those peripherals.
4: The shaded region indicates peripherals contained and powered from VBAT on devices that support battery operation from the VBAT pin.
5: Refer to Table 36-16 in **36.0 "Electrical Characteristics"** for PBCLK6 frequency limitations.
6: CLKO on OSC2 pin, if enabled in configuration word, available in EC & FRC mode is PBCLK1 / 2.

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TABLE 9-1: SYSTEM AND PERIPHERAL CLOCK DISTRIBUTION

Peripheral	Clock Source																	
	FRC	LPRC	SOSC	POSC	SYSCLK	SPLL	UPLL	PBCLK1(1)	PBCLK2	PBCLK3	PBCLK4	PBCLK5	PBCLK6	PBCLK7	REFCLKO1	REFCLKO2	REFCLKO3	REFCLKO4
ADC1-ADC7												X					X	
CAN1-CAN4												X						
CFG PMD								X										
CLKO(6)								X										
Comparator 1-5									X									
CPU	X	X	X	X		X	X							X				
CRU								X										
CTMU									X									
CDAC1									X									
CDAC2-CDAC3										X								
DATAEE	X								X									
DMA					X													
DMT								X										
DSCTRL(5)		X											X					
EVIC					X													
Flash	X							X						X				
Input Capture 10-16										X								
Input Capture 1-9									X									
ICD								X										
Output Compare 10-16										X								
Output Compare 1-9									X									
Op amp 1-3, 5									X									
PMP									X									
PORTA-PORTG											X							
PPS								X							X	X	X	X
RTCC		X	X										X					
SPI1-SPI2									X						X			
SPI3-SPI6										X					X			
SSX Control					X													
Timer1		X	X						X									
Timer2-Timer9									X									
UART1-UART2	X				X				X						X			
UART3-UART6	X				X					X					X			
USB1-USB2	X			X			X					X						
WDT		X						X										

Note 1: PBCLK1 is used by system modules and cannot be turned off.
2: SYSCLK/PBCLK5 is used to fetch data from/to the Flash Controller, while the FRC clock is used for programming.
3: Special Function Register (SFR) access only.
4: Timer1 only.
5: DSCTRL is the Deep Sleep Control Block.
6: PBCLK1 divided by 2 is available on CLKO function pin on oscillator in EC or FRC mode.

9.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MK GP/MC oscillator system includes a Fail-safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a NMI. When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

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9.2 Oscillator Control Registers

TABLE 9-2: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1200	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			DRMEN	—	SLP2SPD	—	—	—	—	—	0xx0
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	—	—	SLPEN	CF	UFRCEN	SOSCEN	OSWEN	xxxx
1210	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0020
1220	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>							0xxx
		15:0	—	—	—	—	—	PLLIDIV<2:0>			PLLICLK	—	—	—	—	PLLRANGE<2:0>			0xxx
1230	UPLLCON	31:16	—	—	UPOSCEN	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>							0xxx
		15:0	—	—	—	—	—	PLLIDIV<2:0>			—	—	—	—	—	PLLRANGE<2:0>			0x0x
1280	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
1290	REFO1TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12A0	REFO2CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12B0	REFO2TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12C0	REFO3CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12D0	REFO3TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12E0	REFO4CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12F0	REFO4TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1300	PB1DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1310	PB2DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1320	PB3DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1330	PB4DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
2: Refer to Table 36-16 in **36.0 "Electrical Characteristics"** for PBCLK6 frequency limitations.
3: The PB7DIV register is read-only.

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TABLE 9-2: OSCILLATOR CONFIGURATION REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1340	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1350	PB6DIV(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1360	PB7DIV(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8800
1380	SLEWCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	SYSDIV<3:0>				0000
		15:0	—	—	—	—	—	SLWDIV<2:0>			—	—	—	—	—	UPEN	DNEN	BUSY	0000
1390	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	UPLLRDY	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
2: Refer to Table 36-16 in **36.0 "Electrical Characteristics"** for PBCLK6 frequency limitations.
3: The PB7DIV register is read-only.

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REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FRCDIV<2:0>		
23:16	R/W-0	U-0	R/W-y	U-0	U-0	U-0	U-0	U-0
	DRMEN	—	SLP2SPD	—	—	—	—	—
15:8	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0, HS	R/W-0	R/W-y	R/W-y
	CLKLOCK	—	—	SLPEN	CF	UFRCEN	SOSCEN	OSWEN(1)

Legend:	y = Value set from Configuration bits on POR		HS = Hardware Set
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits
- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2
- 000 = FRC divided by 1 (default setting)

bit 23 **DRMEN:** Dream Mode Enable bit
- 1 = Dream mode is enabled
- 0 = Dream mode is disabled

bit 22 **Unimplemented:** Read as '0'

bit 21 **SLP2SPD:** Sleep Two-speed Start-up Control bit
- 1 = Use FRC as SYSCLK until the selected clock is ready
- 0 = Use the selected clock directly

bit 20-15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits
- 111 = Reserved
- 110 = Reserved
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = USB PLL (UPLL) input clock and divider are set by UPLLCON
- 010 = Primary Oscillator (POSC) (HS or EC)
- 001 = System PLL (SPLL) input clock and divider set by SPLLCON
- 000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV) supports FRN divided by N, where 'N' is 1, 2, 4, 8, 16, 32, 64, and 256

bit 11 **Unimplemented:** Read as '0'

Note 1: The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits

111 = Reserved
110 = Reserved
101 = Internal Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = USB PLL (UPLL) input clock and divider are set by UPLLCON
010 = Primary Oscillator (POSC) (HS or EC)
001 = System PLL (SPLL) input clock and divider set by SPLLCON
000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV) supports FRN divided by N, where 'N' is 1, 2, 4, 8, 16, 32, 64, and 256

On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit

1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit

1 = Device will enter Sleep mode when a WAIT instruction is executed
0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit

1 = FSCM has detected a clock failure
0 = No clock failure has been detected

Note: On a clock fail event if enabled by the FCKSM<1:0> bits (DEVCFG1<15:14>) = '0b11, this bit and the RNMICON<CF> bit will be set. The user software must clear both the bits inside the CF NMI before attempting to exit the ISR. Software or hardware settings of the CF bit (OSCCON<3>) will cause a CF NMI event and an automatic clock switch to the FRC provided the FCKSM<1:0> = '0b11. Unlike the CF bit (OSCCON<3>), software or hardware settings of the CF bit (RNMICON<17>) will cause a CF NMI event but will not cause a clock switch to the FRC. After a Clock Fail event, a successful user software clock switch if implemented, hardware will automatically clear the CF bit (RNMICON<17>), but not the CF bit (OSCCON<3>). The CF bit (OSCCON<3>) must be cleared by software using the OSCCON register unlock procedure.

bit 2 **UFRCEN:** USB FRC Sleep Clock Enable bit

1 = FRC is the USB input clock for wake from Sleep mode
0 = USB input clock is determined by the UPOSCEN bit (UPLLCON<29>)

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit

1 = Enable Secondary Oscillator
0 = Disable Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit(1)

1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: The reset value for this bit depends on the setting of the IESO bit (DEVCFG1<7>). When IESO = 1, the reset value is '1'. When IESO = 0, the reset value is '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

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REGISTER 9-2: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

111111 = +1.453%

•

•

•

100000 = 0.000% (Nominal Center Frequency, default)

•

•

•

000000 =-1.500%

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized nor tested.

Note: Writes to this register require an unlock sequence. Refer to the **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 9-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	—					PLLIDIV<2:0>		
7:0	R/W-y	U-0	U-0	U-0	U-0	R/W-y	R/W-y	R/W-y
	PLLICLK	—	—	—	—	PLLRANGE<2:0>		

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits

111 = Reserved
110 = Reserved
101 = PLL Divide by 32
100 = PLL Divide by 16
011 = PLL Divide by 8
010 = PLL Divide by 4
001 = PLL Divide by 2
000 = Reserved

The default setting is specified by the FPLLODIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits

1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

The default setting is specified by the FPLLMULT<6:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

bit 15-11 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

3: While the PLL is active, and if updating the PLL bits in the OSCCON register at run-time, the user application must remain within the following limits at all times for all nodes in the PLL clock tree. Therefore, the order in which the PLL values may be modified, (i.e., PLLODIV, PLLMULT, PLLODIV) becomes important. Failure to maintain PLL nodes within min/max ranges may result in unstable PLL and system behavior.

- Output and input to PLLIDIV block (i.e., FPLLI) 5 MHz to 64 MHz (min/max at all times)
- VCO output, (i.e., FVCO) 350 MHz to 700 MHz (min/max at all times)
- Output of PLLODIV, (i.e., FPLL) 10 MHz to 120 MHz (min/max at all times)

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REGISTER 9-3: SPLLCON: SYSTEM PLL CONTROL REGISTER

bit 10-8 **PLLIDIV<2:0>:** System PLL Input Clock Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

The default setting is specified by the FPLLIDIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information. If the PLLICLK is set for FRC, this setting is ignored by the PLL and the divider is set to Divide-by-1.

bit 7 **PLLICLK:** System PLL Input Clock Source bit

1 = FRC is selected as the input to the System PLL
0 = POSC is selected as the input to the System PLL
The POR default is specified by the FPLLICLK Configuration bit in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

bit 6-3 **Unimplemented:** Read as '0'

bit 2-0 **PLLRANGE<2:0>:** System PLL Frequency Range Selection bits

111 = Reserved
110 = 54-64 MHz
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

Use the highest filter range that covers the input freq to the VCO multiplier block that corresponds to the PLLIDIV output freq to minimize PLL system jitter (see Figure 9-1). For example, Crystal = 20 MHz, PLLIDIV<2:0> = 0b1; therefore, the filter input frequency is equal to 10 MHz and UPLLRANGE<2:0> = '0b010. The default setting is specified by the FPLLRNG<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the SPLL is selected as a clock source (COSC<2:0> = 001).

3: While the PLL is active, and if updating the PLL bits in the OSCCON register at run-time, the user application must remain within the following limits at all times for all nodes in the PLL clock tree. Therefore, the order in which the PLL values may be modified, (i.e., PLLODIV, PLLMULT, PLLODIV) becomes important. Failure to maintain PLL nodes within min/max ranges may result in unstable PLL and system behavior.

- Output and input to PLLIDIV block (i.e., FPLLI) 5 MHz to 64 MHz (min/max at all times)
- VCO output, (i.e., FVCO) 350 MHz to 700 MHz (min/max at all times)
- Output of PLLODIV, (i.e., FPLL) 10 MHz to 120 MHz (min/max at all times)

REGISTER 9-4: UPLLCON: USB PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	UPOSCEN	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—					PLLIDIV<2:0>		
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	PLLRANGE<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **UPOSCEN:** Output Enable bit
1 = USB input clock is POSC
0 = USB input clock is UPLL

bit 28-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits
111 = Reserved
110 = Reserved
101 = PLL Divide by 32
100 = PLL Divide by 16
011 = PLL Divide by 8
010 = PLL Divide by 4
001 = PLL Divide by 2
000 = Reserved

The default setting is specified by the FPLLODIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

bit 23 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the UPLL is selected as a clock source (COSC<2:0> = 011).

3: While the PLL is active, and if updating the PLL bits in the OSCCON register at run-time, the user application must remain within the following limits at all times for all nodes in the PLL clock tree. Therefore, the order in which the PLL values may be modified, (i.e., PLLODIV, PLLMULT, PLLODIV) becomes important. Failure to maintain PLL nodes within min/max ranges may result in unstable PLL and system behavior.

- Output and input to PLLIDIV block (i.e., FPLLI) 5 MHz to 64 MHz (minimum/maximum at all times)
- VCO output, (i.e., FVCO) 350 MHz to 700 MHz (minimum/maximum at all times)
- Output of PLLODIV, (i.e., FPLL) 10 MHz to 120 MHz (minimum/maximum at all times)

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REGISTER 9-4: UPLLCON: USB PLL CONTROL REGISTER

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier Output Clock Divider bits

1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
•
•
•
0000010 = Multiply by 3
0000001 = Multiply by 2
0000000 = Multiply by 1

The default setting is specified by the FPLLMULT<6:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **PLLIDIV<2:0>:** System PLL Input Clock Divider bits

111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

The default setting is specified by the FPLLIDIV<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information. If the PLLICLK is set for FRC, this setting is ignored by the PLL and the divider is set to Divide-by-1.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **PLLRANGE<2:0>:** System PLL Frequency Range Selection bits

111 = Reserved
110 = 54-90 MHz
101 = 34-68 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

Use the highest filter range that covers the input freq to the VCO multiplier block that corresponds to the PLLIDIV output freq to minimize PLL system jitter (see Figure 9-1). For example, Crystal = 20 MHz, PLLIDIV<2:0> = 0b1; therefore, the filter input frequency is equal to 10 MHz and UPLLRANGE<2:0> = 0b010. The default setting is specified by the FPLLRNG<2:0> Configuration bits in the DEVCFG2 register. Refer to Register 33-5 in **33.0 "Special Features"** for information.

Note 1: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

2: Writes to this register are not allowed if the UPLL is selected as a clock source (COSC<2:0> = 011).

3: While the PLL is active, and if updating the PLL bits in the OSCCON register at run-time, the user application must remain within the following limits at all times for all nodes in the PLL clock tree. Therefore, the order in which the PLL values may be modified, (i.e., PLLODIV, PLLMULT, PLLODIV) becomes important. Failure to maintain PLL nodes within min/max ranges may result in unstable PLL and system behavior.

- Output and input to PLLIDIV block (i.e., FPLLI) 5 MHz to 64 MHz (minimum/maximum at all times)
- VCO output, (i.e., FVCO) 350 MHz to 700 MHz (minimum/maximum at all times)
- Output of PLLODIV, (i.e., FPLL) 10 MHz to 120 MHz (minimum/maximum at all times)

REGISTER 9-5: REFOxCON: REFERENCE OSCILLATOR CONTROL REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits
The value selects the reference clock divider bits (see Figure 9-1 for details). A value of '0' selects no divider.

bit 15 **ON:** Output Enable bit(1)
1 = Reference Oscillator Module enabled
0 = Reference Oscillator Module disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit
1 = Reference clock is driven out on REFCLKOx pin
0 = Reference clock is not driven out on REFCLKOx pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)
1 = Reference Oscillator Module output continues to run in Sleep
0 = Reference Oscillator Module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit
1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

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REGISTER 9-5: REFOxCON: REFERENCE OSCILLATOR CONTROL REGISTER ('x' = 1-4)

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(3)
1111 = Reserved
•
•
•
1001 = Reserved
1000 = REFCLKI
0111 = SPLL
0110 = UPLL
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = PBCLK1
0000 = SYSCLK

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

REGISTER 9-6: REFOxTRIM: REFERENCE OSCILLATOR TRIM REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

111111111 = 511/512 divisor added to RODIV value
111111110 = 510/512 divisor added to RODIV value
•
•
•
100000000 = 256/512 divisor added to RODIV value
•
•
•
000000010 = 2/512 divisor added to RODIV value
000000001 = 1/512 divisor added to RODIV value
000000000 = 0 divisor added to RODIV value

bit 22-0 **Unimplemented:** Read as '0'

Note 1: While the ON bit (REFOxCON<15>) is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

2: Do not write to this register when the ON bit (REFOxCON<15>) is not equal to the ACTIVE bit (REFOxCON<8>).

3: Specified values in this register do not take effect if RODIV<14:0> (REFOxCON<30:16>) = 0.

4: REFCLKOx Frequency = ((Selected Source Clock / 2) * (N + (M / 512)))
where, Selected source clock = ROSEL, N = RODIV<14:0>, and M = ROTRIM<8:0>.
If the value of REFCLKOx Frequency is not a whole integer value, the output clock will have jitter as it will cause the REFCLKOx circuit to clock cycle steal to produce an average frequency equivalent to the user application's desired frequency. The amount of jitter, (i.e., clock cycle steals), become less as the fractional remainder value becomes closer to a whole number and is greatest at any value plus 0.5.

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REGISTER 9-7: PBxDIV: PERIPHERAL BUS 'x' CLOCK DIVISOR CONTROL REGISTER ('x' = 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	U-0	R-1	U-0	U-0	U-0
	ON(1)	—	—	—	PBDIVRDY	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1(2)
	—	PBDIV<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Peripheral Bus 'x' Output Clock Enable bit(1)
- 1 = Output clock is enabled
- 0 = Output clock is disabled

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **PBDIVRDY:** Peripheral Bus 'x' Clock Divisor Ready bit
- 1 = Clock divisor logic is not switching divisors and the PBxDIV<6:0> bits may be written
- 0 = Clock divisor logic is currently switching values and the PBxDIV<6:0> bits cannot be written

bit 10-7 **Unimplemented:** Read as '0'

bit 6-0 **PBDIV<6:0>:** Peripheral Bus 'x' Clock Divisor Control bits
- 1111111 = PBCLKx is SYSCLK divided by 128
- 1111110 = PBCLKx is SYSCLK divided by 127
- •
- •
- •
- 0000011 = PBCLKx is SYSCLK divided by 4 (default value for x = 6)
- 0000010 = PBCLKx is SYSCLK divided by 3
- 0000001 = PBCLKx is SYSCLK divided by 2 (default value for x < 6)
- 0000000 = PBCLKx is SYSCLK divided by 1 (default value for x = 7)

Note 1: The clock for Peripheral Bus 1 and Peripheral Bus 7 cannot be turned off. Therefore, the ON bit in the PB1DIV register and the PB7DIV register cannot be written as a '0'.

2: The default value for CPU clock PB7DIV Lsb = 0, where PB7CLK = SYSCLK (PB7DIV is read-only).

Note: Writes to this register require an unlock sequence. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 9-8: SLEWCON: OSCILLATOR SLEW CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SYSDIV<3:0>(1)			
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SLWDIV<2:0>		
7:0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R-0, HS, HC
	—	—	—	—	—	UPEN	DNEN	BUSY

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-16 **SYSDIV<3:0>:** System Clock Divide Control bits(1)

1111 = SYSCLK is divided by 16
1110 = SYSCLK is divided by 15
.
.
.
0010 = SYSCLK is divided by 3
0001 = SYSCLK is divided by 2
0000 = SYSCLK is not divided

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **SLWDIV<2:0>:** Slew Divisor Steps Control bits

These bits control the maximum division steps used when slewing during a frequency change.
111 = Steps are divide by 128, 64, 32, 16, 8, 4, 2, and then no divisor
110 = Steps are divide by 64, 32, 16, 8, 4, 2, and then no divisor
101 = Steps are divide by 32, 16, 8, 4, 2, and then no divisor
100 = Steps are divide by 16, 8, 4, 2, and then no divisor
011 = Steps are divide by 8, 4, 2, and then no divisor
010 = Steps are divide by 4, 2, and then no divisor
001 = Steps are divide by 2, and then no divisor
000 = No divisor is used during slewing
The steps apply in reverse order (i.e., 2, 4, 8, etc.) during a downward frequency change.

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **UPEN:** Upward Slew Enable bit

1 = Slewing enabled for switching to a higher frequency
0 = Slewing disabled for switching to a higher frequency

bit 1 **DNEN:** Downward Slew Enable bit

1 = Slewing enabled for switching to a lower frequency
0 = Slewing disabled for switching to a lower frequency

bit 0 **BUSY:** Clock Switching Slewing Active Status bit

1 = Clock frequency is being actively slewed to the new frequency
0 = Clock switch has reached its final value

Note 1: The SYSDIV<3:0> bit settings are ignored if both UPEN and DNEN = 0, and SYSCLK will be divided by 1.

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REGISTER 9-9: CLKSTAT: OSCILLATOR CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	UPLLRDY
7:0	R-0	U-0	R-0	R-0	U-0	R-0	U-0	R-0
	SPLLRDY	—	LPRCRDY	SOSCRDY	—	POSCRDY	—	FRCRDY

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8 **UPLLRDY:** USB PLL (UPLL) Ready Status bit
1 = UPLL is ready
0 = UPLL is not ready

bit 7 **SPLLRDY:** System PLL (SPLL) Ready Status bit
1 = SPLL is ready
0 = SPLL is not ready

bit 5 **LPRCRDY**: Low-Power RC (LPRC) Oscillator Ready Status bit
1 = LPRC is stable and ready
0 = LPRC is disabled or not operating

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready Status bit
1 = SOSC is stable and ready
0 = SOSC is disabled or not operating

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready Status bit
1 = POSC is stable and ready
0 = POSC is disabled or not operating

bit 1 **Unimplemented:** Read as '0'

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready Status bit
1 = FRC is stable and ready
0 = FRC is disabled for not operating

NOTES:

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10.0 PREFETCH MODULE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Prefetch Cache Module"** (DS60001119), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Prefetch module is a performance enhancing module that is included in the PIC32MK GP/MC family of devices. When running at high-clock rates, Wait states must be inserted into Program Flash Memory (PFM) read transactions to meet the access time of the PFM. Wait states can be hidden to the core by prefetching and storing instructions in a temporary holding area that the CPU can access quickly. Although the data path to the CPU is 32 bits wide, the data path to the PFM is 128 bits wide. This wide data path provides the same bandwidth to the CPU as a 32-bit path running at four times the frequency.

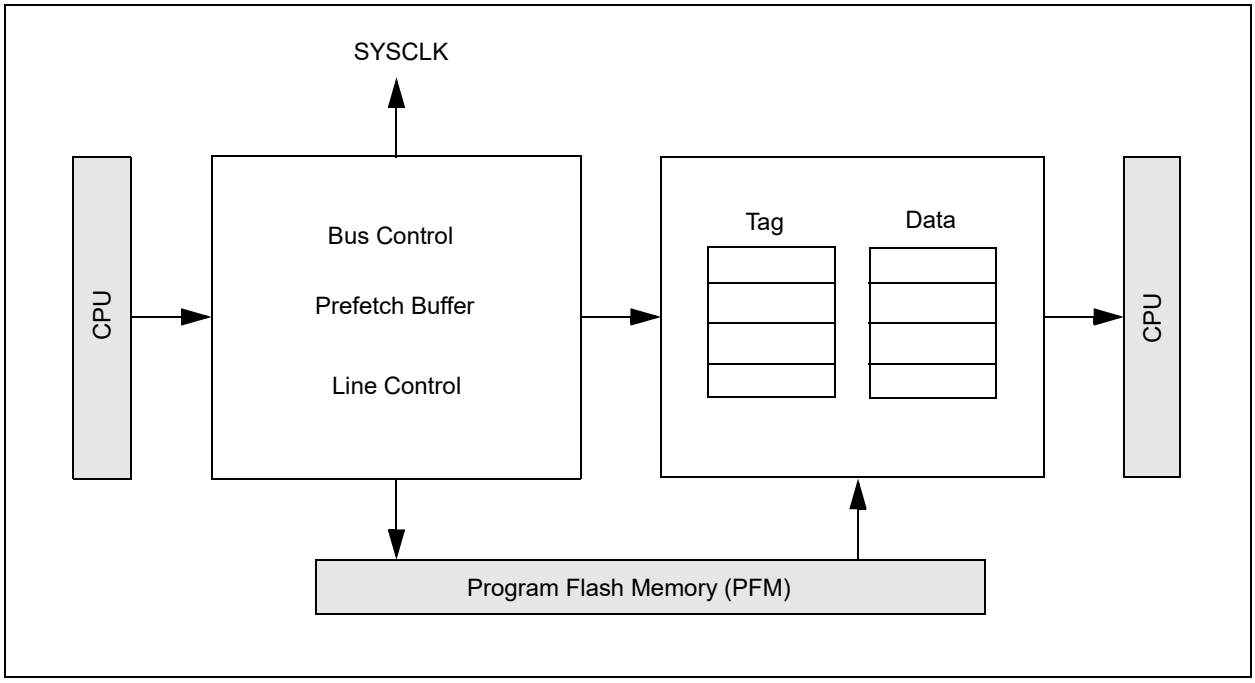
The Prefetch module holds a subset of PFM in temporary holding spaces known as lines. Each line contains a tag and data field. Normally, the lines hold a copy of what is currently in memory to make instructions or data available to the CPU without Flash Wait states.

10.1 Prefetch Cache Features

- 36x16 byte fully-associative lines
- 16 lines for CPU instructions
- Four lines for CPU data
- Four lines for peripheral data
- 16-byte parallel memory fetch
- Configurable predictive prefetch

A simplified block diagram of the Prefetch module is shown in Figure 10-1.

FIGURE 10-1: PREFETCH MODULE BLOCK DIAGRAM



10.2 Prefetch Control Registers

TABLE 10-1: PREFETCH REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0800	CHECON	31:16	—	—	—	—	—	PERCHEEN	DCHEEN	ICHEEN	—	PERCHEINV	DCHEINV	ICHEINV	—	PERCHECOH	DCHECOH	ICHECOH	0700
		15:0	—	—	—	CHEPERFEN	—	—	—	PFMAWSEN	—	—	PREFEN<1:0>		—	PFMWS<2:0>			0107
0820	CHEHIT	31:16	CHEHIT<31:16>																0000
		15:0	CHEHIT<15:0>																0000
0830	CHEMIS	31:16	CHEMIS<31:16>																0000
		15:0	CHEMIS<15:0>																0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 10-1: CHECON: CACHE MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	—	—	—	PERCHEEN	DCHEEN	ICHEEN
23:16	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	PER CHEINV(1)	DCHEINV(1)	ICHEINV(1)	—	PER CHECOH(2)	DCHECOH(2)	ICHECOH(2)
15:8	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-1
	—	—	—	CHE PERFEN	—	—	—	PFM AWSEN
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	PREFEN<1:0>		—	PFMWS<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **PERCHEEN:** Peripheral Cache Enable bit
1 = Peripheral cache is enabled
0 = Peripheral cache is disabled

bit 25 **DCHEEN:** Data Cache Enable bit
1 = Data cache is enabled
0 = Data cache is disabled

bit 24 **ICHEEN:** Instruction Cache Enable bit
1 = Instruction cache is enabled
0 = Instruction cache is disabled

bit 23 **Unimplemented:** Read as '0'

bit 22 **PERCHEINV:** Peripheral Cache Invalidate bit(1)
1 = Force invalidate cache/invalidate busy
0 = Cache Invalidation follows CHECOH/invalid complete

bit 21 **DCHEINV:** Data Cache Invalidate bit(1)
1 = Force invalidate cache/invalidate busy
0 = Cache Invalidation follows CHECOH/invalid complete

bit 20 **ICHEINV:** Instruction Cache Invalidate bit(1)
1 = Force invalidate cache/invalidate busy
0 = Cache Invalidation follows CHECOH/invalid complete

bit 19 **Unimplemented:** Read as '0'

bit 18 **PERCHECOH:** Peripheral Auto-cache Coherency Control bit(2)
1 = Automatically invalidate cache on a programming event
0 = Do not automatically invalidate cache on a programming event

Note 1: Hardware automatically clears this bit when cache invalidate completes. Bits may clear at different times.
2: The PERCHECOH, DCHECOH, and ICHECOH bits must be stable before initiation of programming to ensure correct invalidation of data.

REGISTER 10-1: CHECON: CACHE MODULE CONTROL REGISTER (CONTINUED)

bit 17 **DCHECOH:** Data Auto-cache Coherency Control bit(2)
1 = Automatically invalidate cache on a programming event
0 = Do not automatically invalidate cache on a programming event

bit 16 **ICHECOH:** Instruction Auto-cache Coherency Control bit(2)
1 = Automatically invalidate cache on a programming event
0 = Do not automatically invalidate cache on a programming event

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **CHEPERFEN:** Cache Performance Counters Enable bit
1 = Performance counters are enabled
0 = Performance counters are disabled

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **PFMAWSEN:** PFM Address Wait State Enable bit
1 = Add one more Wait State to flash address setup (suggested for higher system clock frequencies)
0 = Add no Wait States to the flash address setup (suggested for lower system clock frequencies to achieve higher performance)

When this bit is set to '1', total Flash wait states are PFMWS plus PFMAWSEN.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits
11 = Disable predictive prefetch
10 = Disable predictive prefetch
01 = Enable predictive prefetch for CPU instructions only
00 = Disable predictive prefetch

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSCLK Wait States bits
111 = Seven Wait states
•
•
•
010 = Two Wait states
001 = One Wait state
000 = Zero Wait states

Required Flash Wait States	SYSCLK (MHz)
1 - Wait State	0 < SYSCLK ≤ 60 MHz
3 - Wait State	60 MHz < SYSCLK ≤ 120 MHz

Note 1: When the LPRD bit (NVMCON<15>) = 0, Flash read access wait states are governed by the PFMWS<2:0> bits.
2: When the LPRD bit = 1, Flash read access wait states are governed by the LPRDWS<4:0> bits (NVMCOM2<20:16>).

Note 1: Hardware automatically clears this bit when cache invalidate completes. Bits may clear at different times.
2: The PERCHECOH, DCHECOH, and ICHECOH bits must be stable before initiation of programming to ensure correct invalidation of data.

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REGISTER 10-2: CHEHIT: CACHE HIT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEHIT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEHIT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEHIT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEHIT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEHIT<31:0>:** Instruction Cache Hit Count bits

When the CHEPERFEN bit (CHECON<12>) = 1, the CHEHIT<31:0> bits increment each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

The CHEHIT<31:0> bits are reset on a '0' to '1' transition of the CHEPERFEN bit.

REGISTER 10-3: CHEMIS: CACHE MISS STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHEMIS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHEMIS<31:0>:** Instruction Cache Miss Count bits

When the CHEPERFEN bit (CHECON<12>) = 1, the CHEMIS<31:0> bits increment each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

The CHEMIS<31:0> bits are reset on a '0' to '1' transition of the CHEPERFEN bit.

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11.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

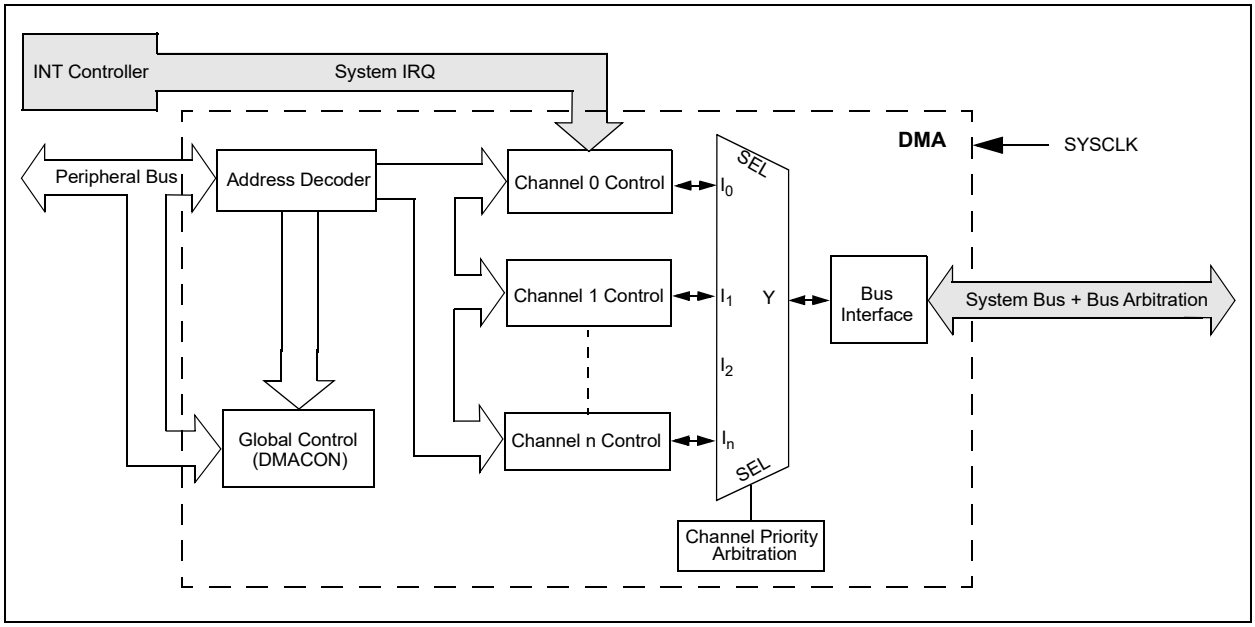
Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Direct Memory Access (DMA) Controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the device such as SPI, UART, PMP, etc., or memory itself.

Following are some of the key features of the DMA Controller module:

- Eight identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory-to-memory and memory-to-peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Up to 2-byte Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent error address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

FIGURE 11-1: DMA BLOCK DIAGRAM



11.1 DMA Control Registers

TABLE 11-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
1010	DMASTAT	31:16	RDWR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	DMACH<2:0>			0000
1020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

TABLE 11-2: DMA CRC REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
1040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
1050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1060	DCH0CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1070	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1080	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1090	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
10A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
10B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
10C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
10D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
10E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
10F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1100	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1110	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1120	DCH1CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1130	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1140	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1150	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1160	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
11A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
11B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
11C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
11D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
11E0	DCH2CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
11F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1210	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1220	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
12A0	DCH3CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
12B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
12C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
12D0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
12E0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
12F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1360	DCH4CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1370	DCH4ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1380	DCH4INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1390	DCH4SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
13A0	DCH4DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
13B0	DCH4SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
13C0	DCH4DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
13D0	DCH4SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
13E0	DCH4DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
13F0	DCH4CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1400	DCH4CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1410	DCH4DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1420	DCH5CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1430	DCH5ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1440	DCH5INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1450	DCH5SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1460	DCH5DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1470	DCH5SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1480	DCH5DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1490	DCH5SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14A0	DCH5DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
14B0	DCH5CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
14C0	DCH5CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
14D0	DCH5DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
14E0	DCH6CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
14F0	DCH6ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1500	DCH6INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1510	DCH6SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1520	DCH6DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1530	DCH6SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1540	DCH6DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1550	DCH6SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1560	DCH6DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1570	DCH6CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1580	DCH6CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1590	DCH6DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
15A0	DCH7CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 11-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15B0	DCH7ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
15C0	DCH7INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
15D0	DCH7SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
15E0	DCH7DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
15F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 11-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	ON	—	—	SUSPEND(1)	DMABUSY	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit(1)
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active and is transferring data
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

Note 1: If the user application clears this bit, it may take a number of cycles before the DMA module completes the current transaction and responds to this request. The user application should poll the BUSY bit to verify that the request has been honored.

REGISTER 11-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RDWR	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	DMACH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **RDWR:** Read/Write Status bit

1 = Last DMA bus access when an error was detected was a read
0 = Last DMA bus access when an error was detected was a write

bit 30-3 **Unimplemented:** Read as '0'

bit 2-0 **DMACH<2:0>:** DMA Channel bits

These bits contain the value of the most recent active DMA channel when an error was detected.

Note: The DMASTAT register will be cleared when its contents are read. If more than one errors at the same time, the read transaction will be recorded. Additional transfers that occur later with an error will not update this register until it has been read or cleared.

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REGISTER 11-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access when an error was detected.

Note: The DMAADDR register will be cleared when its contents are read. If more than one errors at the same time, the read transaction will be recorded. Additional transfers that occur later with an error will not update this register until it has been read or cleared.

REGISTER 11-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO(1)	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>(1,2,3)				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP(1)	CRCTYP	—	—	CRCCH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
- 00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit(1)
- 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits(1,2,3)

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

2: The maximum CRC length supported by the DMA module is 32.

3: This bit is unused when CRCTYP is equal to '1'.

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REGISTER 11-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 6 **CRCAPP:** CRC Append Mode bit(1)
- 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
- 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination

bit 5 **CRCTYP:** CRC Type Selection bit
- 1 = The CRC module will calculate an IP header checksum
- 0 = The CRC module will calculate a LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
- 111 = CRC is assigned to Channel 7
- 110 = CRC is assigned to Channel 6
- 101 = CRC is assigned to Channel 5
- 100 = CRC is assigned to Channel 4
- 011 = CRC is assigned to Channel 3
- 010 = CRC is assigned to Channel 2
- 001 = CRC is assigned to Channel 1
- 000 = CRC is assigned to Channel 0

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.
2: The maximum CRC length supported by the DMA module is 32.
3: This bit is unused when CRCTYP is equal to '1'.

REGISTER 11-5: DCRCDATA: DMA CRC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return '0' on any read.

REGISTER 11-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

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REGISTER 11-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPIGN<7:0>							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
	CHBUSY	—	CHIPGNEN	—	CHPATLEN	—	—	CHCHNS(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN(2)	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **CHPIGN<7:0>:** Channel Register Data bits
Pattern Terminate mode:
Any byte matching these bits during a pattern match may be ignored during the pattern match determination when the CHPIGNEN bit is set. If a byte is read that is identical to this data byte, the pattern match logic will treat it as a "don't care" when the pattern matching logic is enabled and the CHPIGEN bit is set.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
1 = Channel is active or has been enabled
0 = Channel is inactive or has been disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CHPIGNEN:** Enable Pattern Ignore Byte bit
1 = Treat any byte that matches the CHPIGN<7:0> bits as a "don't care" when pattern matching is enabled
0 = Disable this feature

bit 12 **Unimplemented:** Read as '0'

bit 11 **CHPATLEN:** Pattern Length bit
1 = 2 byte length
0 = 1 byte length

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
1 = Channel is enabled
0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
1 = Channel start/abort events will be registered, even if the channel is disabled
0 = Channel start/abort events will be ignored if the channel is disabled

bit 5 **CHCHN:** Channel Chain Enable bit
1 = Allow channel to be chained
0 = Do not allow channel to be chained

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 11-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER ('x' = 0-7) (CONTINUED)

bit 4 **CHAEN:** Channel Automatic Enable bit
1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit
1 = An event has been detected
0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits
11 = Channel has priority 3 (highest)
10 = Channel has priority 2
01 = Channel has priority 1
00 = Channel has priority 0

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

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REGISTER 11-8: DCHxECON: DMA CHANNEL x EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0>(1)							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0>(1)							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
•
•
•
00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)

11111111 = Interrupt 255 will initiate a DMA transfer
•
•
•
00000001 = Interrupt 1 will initiate a DMA transfer
00000000 = Interrupt 0 will initiate a DMA transfer

Note: The DMA does not support I^2C, Change Notification, Input Capture, CTMU, QEI, and MC PWMs. Using any of these DMA trigger transfer events could lead to unexpected behavior.

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'
0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'
0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match
0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See **Table 8-3: "Interrupt IRQ, Vector and Bit Location"** for the list of available interrupt IRQ sources.

REGISTER 11-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
0 = No interrupt is pending

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REGISTER 11-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER (CONTINUED)

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
0 = No interrupt is pending

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected
Either the source or the destination address is invalid.
0 = No interrupt is pending

REGISTER 11-10: DCHxSSA: DMA CHANNEL x SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.
Note: This must be the physical address of the source.

REGISTER 11-11: DCHxDSA: DMA CHANNEL x DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.
Note: This must be the physical address of the destination.

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REGISTER 11-12: DCHxSSIZ: DMA CHANNEL x SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size
•
•
•
0000000000000010 = 2 byte source size
0000000000000001 = 1 byte source size
0000000000000000 = 65,536 byte source size

REGISTER 11-13: DCHxDSIZ: DMA CHANNEL x DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size
•
•
•
0000000000000010 = 2 byte destination size
0000000000000001 = 1 byte destination size
0000000000000000 = 65,536 byte destination size

REGISTER 11-14: DCHxSPTR: DMA CHANNEL x SOURCE POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSPTR<15:0>:** Channel Source Pointer bits

1111111111111111 = Points to byte 65,535 of the source
•
•
•
0000000000000001 = Points to byte 1 of the source
0000000000000000 = Points to byte 0 of the source

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

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REGISTER 11-15: DCHxDPTR: DMA CHANNEL x DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDPTR<15:0>:** Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination

•

•

•

0000000000000001 = Points to byte 1 of the destination

0000000000000000 = Points to byte 0 of the destination

REGISTER 11-16: DCHxCSIZ: DMA CHANNEL x CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event
•
•
•
0000000000000010 = 2 bytes transferred on an event
0000000000000001= 1 byte transferred on an event
0000000000000000 = 65,536 bytes transferred on an event

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REGISTER 11-17: DCHxCPTR: DMA CHANNEL x CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<15:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
•
•
•
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 11-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHPDAT<15:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All other modes:
Unused.

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12.0 USB ON-THE-GO (OTG)

Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host, full-speed device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32MK USB OTG module is presented in Figure 12-1.

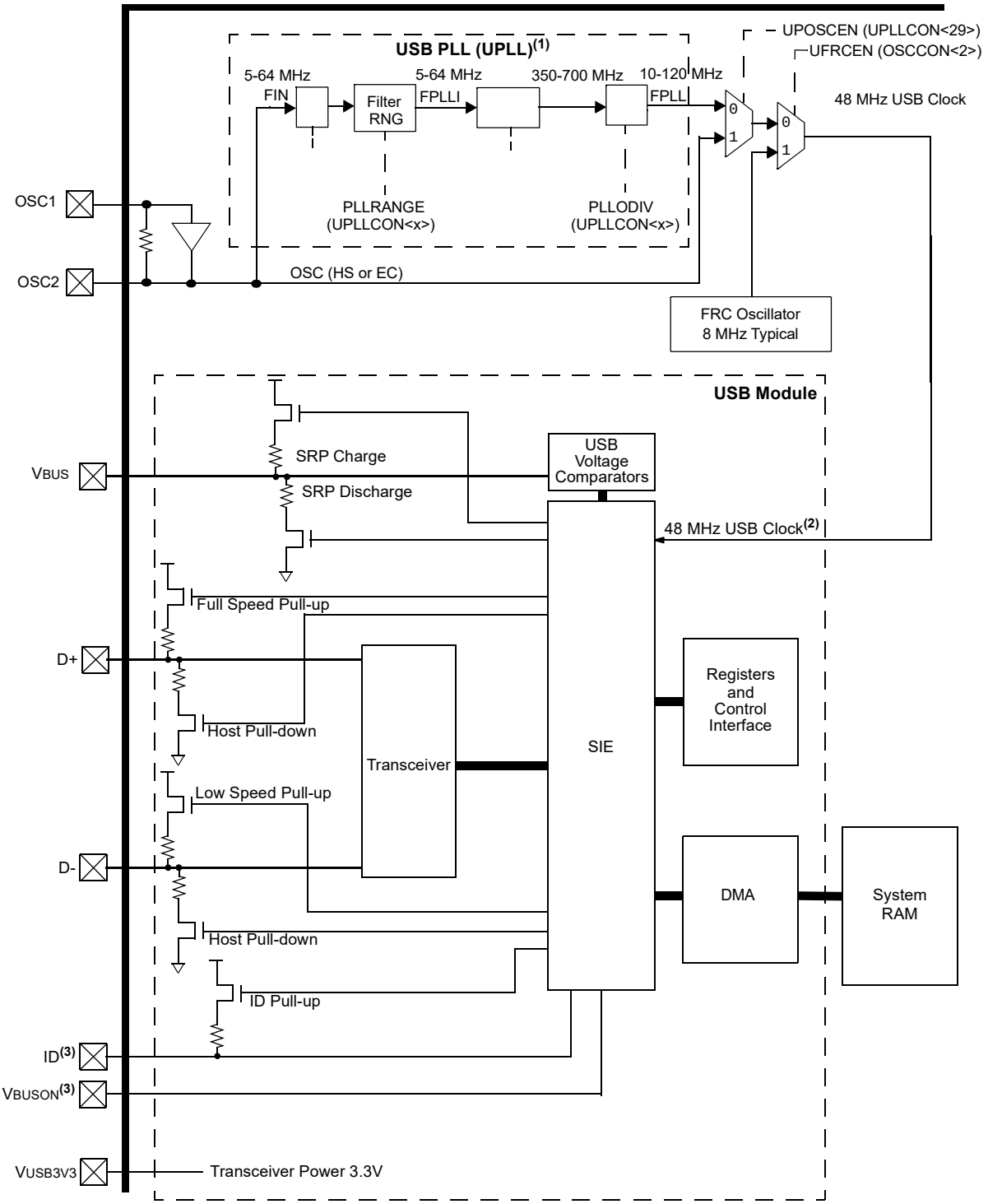
The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The PIC32MK USB module includes the following features:

- USB full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

Note: The implementation and use of the USB specifications, and other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

FIGURE 12-1: USB INTERFACE DIAGRAM



Note 1: These bits are contained in the DEVCFG2 register.
2: A 48 MHz clock is required for proper USB operation.
3: Pins can be used as GPIO when the USB module is disabled or when the USB module is enabled but the FVBUSIOx bit (DEVCFG3<31>) = 0 or the FUSBIDIOx bit (DEVCFG3<30>) = 0.

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12.1 Control Registers

TABLE 12-1: USB1 AND USB2 REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9040	U1OTGIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
9050	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
9060	U1OTGSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
9070	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
9080	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND(4)	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
9200	U1IR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
9210	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000
9220	U1EIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF	PIDEF	0000
																	EOFEF		0000
9230	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE	PIDEE	0000
																	EOFEE		0000
9240	U1STAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>				DIR	PPBI	—	—	0000
9250	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE	SE0	PKTDIS	USBRST	HOSTEN	RESUME	PPBRST	USBEN	0000
													TOKBUSY					SOFEN	0000
9260	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
9270	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<15:9>							—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET, and INV registers.

4: Reset value for this bit is undefined.

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TABLE 12-1: USB1 AND USB2 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9280	U1FRML(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	FRML<7:0>								0000
9290	U1FRMH(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	FRMH<2:0>			0000
92A0	U1TOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PID<3:0>				EP<3:0>				0000
92B0	U1SOF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNT<7:0>								0000
92C0	U1BDTP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRH<23:16>								0000
92D0	U1BDTP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRU<31:24>								0000
92E0	U1CNFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UTEYE	UOEMON	—	USBSIDL	LSDEV	—	—	UASUSPND	0000
9300	U1EP0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
9310	U1EP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
9320	U1EP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
9330	U1EP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
9340	U1EP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
9350	U1EP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
9360	U1EP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
9370	U1EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
9380	U1EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET, and INV registers.

4: Reset value for this bit is undefined.

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TABLE 12-1: USB1 AND USB2 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
9390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
93F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A040	U2OTGIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
A050	U2OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
A060	U2OTGSTAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
A070	U2OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
A080	U2PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND(4)	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
A200	U2IR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF	0000
																		DETACHIF	0000
A210	U2IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE	0000
																		DETACHIE	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET, and INV registers.

4: Reset value for this bit is undefined.

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TABLE 12-1: USB1 AND USB2 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A220	U2EIR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF	PIDEF	0000 0000
A230	U2EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE EOFEE	PIDEE	0000 0000
A240	U2STAT(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>				DIR	PPBI	—	—	0000
A250	U2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE	SE0	PKTDIS TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN SOFEN	0000 0000
A260	U2ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000
A270	U2BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<15:9>							—	0000
A280	U2FRML(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	FRML<7:0>								0000
A290	U2FRMH(3)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	FRMH<2:0>			0000
A2A0	U2TOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PID<3:0>				EP<3:0>				0000
A2B0	U2SOF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNT<7:0>								0000
A2C0	U2BDTP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRH<23:16>								0000
A2D0	U2BDTP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRU<31:24>								0000
A2E0	U2CNFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UTEYE	UOEMON	—	USBSIDL	LSDEV	—	—	UASUSPND	0000
A300	U2EP0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET, and INV registers.

4: Reset value for this bit is undefined.

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TABLE 12-1: USB1 AND USB2 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A310	U2EP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A320	U2EP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A330	U2EP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A340	U2EP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A350	U2EP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A360	U2EP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A370	U2EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A380	U2EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A390	U2EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3A0	U2EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3B0	U2EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3C0	U2EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3D0	U2EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3E0	U2EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
A3F0	U2EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET, and INV registers.

4: Reset value for this bit is undefined.

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REGISTER 12-1: UxOTGIR: USB OTG INTERRUPT STATUS REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = Change in ID state is detected
- 0 = No change in ID state is detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1millisecond, but different from last time
- 0 = USB line state has not been stable for 1 millisecond

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = Change on the session valid input is detected
- 0 = No change on the session valid input is detected

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REGISTER 12-2: UxOTGIE: USB OTG INTERRUPT ENABLE REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
1 = ID interrupt is enabled
0 = ID interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = 1 millisecond timer interrupt is enabled
0 = 1 millisecond timer interrupt is disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit
1 = Line state interrupt is enabled
0 = Line state interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = ACTIVITY interrupt is enabled
0 = ACTIVITY interrupt is disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Session valid interrupt is enabled
0 = Session valid interrupt is disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit
1 = B-session end interrupt is enabled
0 = B-session end interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit
1 = A-VBUS valid interrupt is enabled
0 = A-VBUS valid interrupt is disabled

REGISTER 12-3: UxOTGSTAT: USB OTG STATUS REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit
- 1 = No cable is attached or a Type-B cable has been plugged into the USB receptacle
- 0 = A Type-A cable has been plugged into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit
- 1 = USB line state (SE0 (UxCON<6>) and JSTATE (UxCON<7>)) has been stable for the previous 1 ms
- 0 = USB line state (SE0 and JSTATE) has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A or B device
- 0 = VBUS voltage is below Session Valid on the A or B device

bit 2 **SESEND:** B-Device Session End Indicator bit
- 1 = VBUS voltage is below Session Valid on the B device
- 0 = VBUS voltage is above Session Valid on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A device
- 0 = VBUS voltage is below Session Valid on the A device

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REGISTER 12-4: UxOTGCON: USB OTG CONTROL REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit
1 = D+ data line pull-up resistor is enabled
0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit
1 = D- data line pull-up resistor is enabled
0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
1 = D+ data line pull-down resistor is enabled
0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit
1 = D- data line pull-down resistor is enabled
0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit
1 = VBUS line is powered
0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Functionality Enable bit
1 = DPPULUP, DMPULUP, DPPULDWN, and DMPULDWN bits are under software control
0 = DPPULUP, DMPULUP, DPPULDWN, and DMPULDWN bits are under USB hardware control

bit 1 **VBUSCHG:** VBUS Charge Enable bit
1 = VBUS line is charged through a pull-up resistor
0 = VBUS line is not charged through a resistor

bit 0 **VBUSDIS:** VBUS Discharge Enable bit
1 = VBUS line is discharged through a pull-down resistor
0 = VBUS line is not discharged through a resistor

REGISTER 12-5: UxPWRC: USB POWER CONTROL REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	—	—	USLPGRD	USBBUSY(1)	—	USUSPEND	USBPWR

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB hardware has detected a change in link status; however, an interrupt is pending and has not yet been generated. Software should not put the device into Sleep mode.
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

Note: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit
- 1 = USB module is turned on
- 0 = USB module is disabled (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

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REGISTER 12-6: UxIR: USB INTERRUPT REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R-0	R/WC-0, HS
	STALLIF	ATTACHIF(1)	RESUMEIF(2)	IDLEIF	TRNIF(3)	SOFIF	UERRIF(4)	URSTIF(5) / DETACHIF(6)

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
1 = In Host mode, a STALL handshake was received during the handshake phase of the transaction
In Device mode, a STALL handshake was transmitted during the handshake phase of the transaction
0 = STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit(1)
1 = Peripheral attachment was detected by the USB module
0 = Peripheral attachment was not detected

bit 5 **RESUMEIF:** Resume Interrupt bit(2)
1 = K-State is observed on the D+ or D- pin for 2.5 µs
0 = K-State is not observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
1 = Idle condition detected (constant Idle state of 3 ms or more)
0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit(3)
1 = Processing of current token is complete; a read of the UxSTAT register will provide endpoint information
0 = Processing of current token not complete

bit 2 **SOFIF:** SOF Token Interrupt bit
1 = SOF token received by the peripheral or the SOF threshold reached by the host
0 = SOF token was not received nor threshold reached

bit 1 **UERRIF:** USB Error Condition Interrupt bit(4)
1 = Unmasked error condition has occurred
0 = Unmasked error condition has not occurred

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)(5)
1 = Valid USB Reset has occurred
0 = No USB Reset has occurred

bit 0 **DETACHIF:** USB Detach Interrupt bit (Host mode)(6)
1 = Peripheral detachment was detected by the USB module
0 = Peripheral detachment was not detected

Note 1: This bit is valid only if the HOSTEN bit is set (see Register 12-11), there is no activity on the USB for 2.5 µs, and the current bus state is not SE0.
2: When not in Suspend mode, this interrupt should be disabled.
3: Clearing this bit will cause the STAT FIFO to advance.
4: Only error conditions enabled through the UxEIE register will set this bit.
5: Device mode.
6: Host mode.

REGISTER 12-7: UxIE: USB INTERRUPT ENABLE REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE(1)	URSTIE(2) / DETACHIE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
1 = STALL interrupt is enabled
0 = STALL interrupt is disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit
1 = ATTACH interrupt is enabled
0 = ATTACH interrupt is disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit
1 = RESUME interrupt is enabled
0 = RESUME interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
1 = Idle interrupt is enabled
0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
1 = TRNIF interrupt is enabled
0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
1 = SOFIF interrupt is enabled
0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
1 = USB Error interrupt is enabled
0 = USB Error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
1 = URSTIF interrupt is enabled
0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit(3)
1 = DATTCHIF interrupt is enabled
0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (UxIE<1>) must be set.
2: Device mode.
3: Host mode.

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REGISTER 12-8: UxEIR: USB ERROR INTERRUPT STATUS REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS
	BTSEF	BMXEF	DMAEF(1)	BTOEF(2)	DFN8EF	CRC16EF	CRC5EF(4) / EOFEF(3,5)	PIDEF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit
- 1 = Packet rejected due to bit stuff error
- 0 = Packet accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
- 1 = The base address, of the BDT, or the address of an individual buffer pointed to by a BDT entry, is invalid.
- 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit(1)
- 1 = USB DMA error condition detected
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit(2)
- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit
- 1 = Data field received is not an integral number of bytes
- 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
- 1 = Data packet rejected due to CRC16 error
- 0 = Data packet accepted

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

REGISTER 12-8: UxEIR: USB ERROR INTERRUPT STATUS REGISTER ('x' = 1 AND 2)

bit 1 **CRC5EF:** CRC5 Host Error Flag bit(4)
1 = Token packet rejected due to CRC5 error
0 = Token packet accepted
EOFEF: EOF Error Flag bit(3,5)
1 = EOF error condition detected
0 = No EOF error condition

bit 0 **PIDEF:** PID Check Failure Flag bit
1 = PID check failed
0 = PID check passed

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

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REGISTER 12-9: UxEIE: USB ERROR INTERRUPT ENABLE REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE(1) / EOFEE(2)	PIDEE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

Note 1: Device mode.
2: Host mode.

Note: For an interrupt to propagate USBIF, the UERRIE bit (UxIE<1>) must be set.

REGISTER 12-10: UxSTAT: USB STATUS REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
	ENDPT<3:0>				DIR	PPBI	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits
(Represents the number of the BDT, updated by the last USB transfer.)

1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last BD Direction Indicator bit

1 = Last transaction was a transmit transfer (TX)
0 = Last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong BD Pointer Indicator bit

1 = The last transaction was to the ODD BD bank
0 = The last transaction was to the EVEN BD bank

bit 1-0 **Unimplemented:** Read as '0'

Note: The UxSTAT register is a window into a 4-byte FIFO maintained by the USB module. UxSTAT value is only valid when the TRNIF bit (UxIR<3>) is active. Clearing the TRNIF bit advances the FIFO. Data in register is invalid when the TRNIF bit = 0.

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REGISTER 12-11: UxCON: USB CONTROL REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	JSTATE	SE0	PKTDIS(4) / TOKBUSY(1,5)	USBRST(5)	HOSTEN(2)	RESUME(3)	PPBRST	USBEN(4) / SOFEN(5)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit
1 = JSTATE detected on the USB
0 = No JSTATE detected

bit 6 **SE0:** Live Single-Ended Zero flag bit
1 = Single Ended Zero detected on the USB
0 = No Single Ended Zero detected

bit 5 **PKTDIS:** Packet Transfer Disable bit(4)
1 = Token and packet processing disabled (set upon SETUP token received)
0 = Token and packet processing enabled
TOKBUSY: Token Busy Indicator bit(1,5)
1 = Token being executed by the USB module
0 = No token being executed

bit 4 **USBRST:** Module Reset bit(5)
1 = USB reset is generated
0 = USB reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit(2)
1 = USB host capability is enabled
0 = USB host capability is disabled

bit 2 **RESUME:** RESUME Signaling Enable bit(3)
1 = RESUME signaling is activated
0 = RESUME signaling is disabled

Note 1: Software is required to check this bit before issuing another token command to the UxTOK register (see Register 12-15).
2: All host control logic is reset any time that the value of this bit is toggled.
3: Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
4: Device mode.
5: Host mode.

REGISTER 12-11: UxCON: USB CONTROL REGISTER ('x' = 1 AND 2) (CONTINUED)

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Reset all Even/Odd buffer pointers to the EVEN BD banks
0 = Even/Odd buffer pointers not being Reset

bit 0 **USBEN:** USB Module Enable bit(4)
1 = USB module and supporting circuitry is enabled
0 = USB module and supporting circuitry is disabled

SOFEN: SOF Enable bit(5)
1 = SOF token sent every 1 ms
0 = SOF token disabled

Note 1: Software is required to check this bit before issuing another token command to the UxTOK register (see Register 12-15).
2: All host control logic is reset any time that the value of this bit is toggled.
3: Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
4: Device mode.
5: Host mode.

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REGISTER 12-12: UxADDR: USB ADDRESS REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low Speed Enable Indicator bit
1 = Next token command to be executed at Low Speed
0 = Next token command to be executed at Full Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 12-13: UxFRML: USB FRAME NUMBER LOW REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 12-14: UxFRMH: USB FRAME NUMBER HIGH REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	FRMH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 12-15: UxTOK: USB TOKEN REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PID<3:0>(1)				EP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits(1)
0001 = OUT (TX) token type transaction
1001 = IN (RX) token type transaction
1101 = SETUP (TX) token type transaction
Note: All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
The four bit value must specify a valid endpoint.

Note 1: All other values are reserved and must not be used.

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REGISTER 12-16: UxSOF: USB SOF THRESHOLD REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:
01001010 = 64-byte packet
00101010 = 32-byte packet
00011010 = 16-byte packet
00010010 = 8-byte packet

REGISTER 12-17: UxBDTP1: USB BDT PAGE 1 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BDTPTRL<15:9>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'

REGISTER 12-18: UxBDTP2: USB BDT PAGE 2 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<23:16>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

REGISTER 12-19: UxBDTP3: USB BDT PAGE 3 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<31:24>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

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REGISTER 12-20: UxCNFG1: USB CONFIGURATION 1 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	UTEYE	UOEMON	—	USBSIDL	LSDEV	—	—	UASUSPND

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit
1 = Eye-Pattern Test is enabled
0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB $\overline{OE}$ Monitor Enable bit
1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving
0 = OE signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 3 **LSDEV:** Low-Speed Device Enable bit
1 = USB module to operate in Low-Speed Device mode
0 = USB module to operate in OTG, Host, or Full-Speed Device mode

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit
1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (UxPWRC<1>) in Register 12-5.
0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (UxPWRC<1>) to suspend the module, including the USB 48 MHz clock

REGISTER 12-21: UxEP0-UxEP15: USB ENDPOINT CONTROL REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (Host mode and UxEP0 only)
1 = Direct connection to a low-speed device is enabled
0 = Direct connection to a low-speed device is disabled; hub required with PRE_PID

bit 6 **RETRYDIS:** Retry Disable bit (Host mode and UxEP0 only)
1 = Retry NAKed transactions is disabled
0 = Retry NAKed transactions is enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN = 1 and EPRXEN = 1:
1 = Disable Endpoint n from Control transfers; only TX and RX transfers allowed
0 = Enable Endpoint n for Control (SETUP) transfers; TX and RX transfers also allowed
Otherwise, this bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint n receive is enabled
0 = Endpoint n receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint n transmit is enabled
0 = Endpoint n transmit is disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit
1 = Endpoint n was stalled
0 = Endpoint n was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint Handshake is enabled
0 = Endpoint Handshake is disabled (typically used for isochronous endpoints)

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13.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

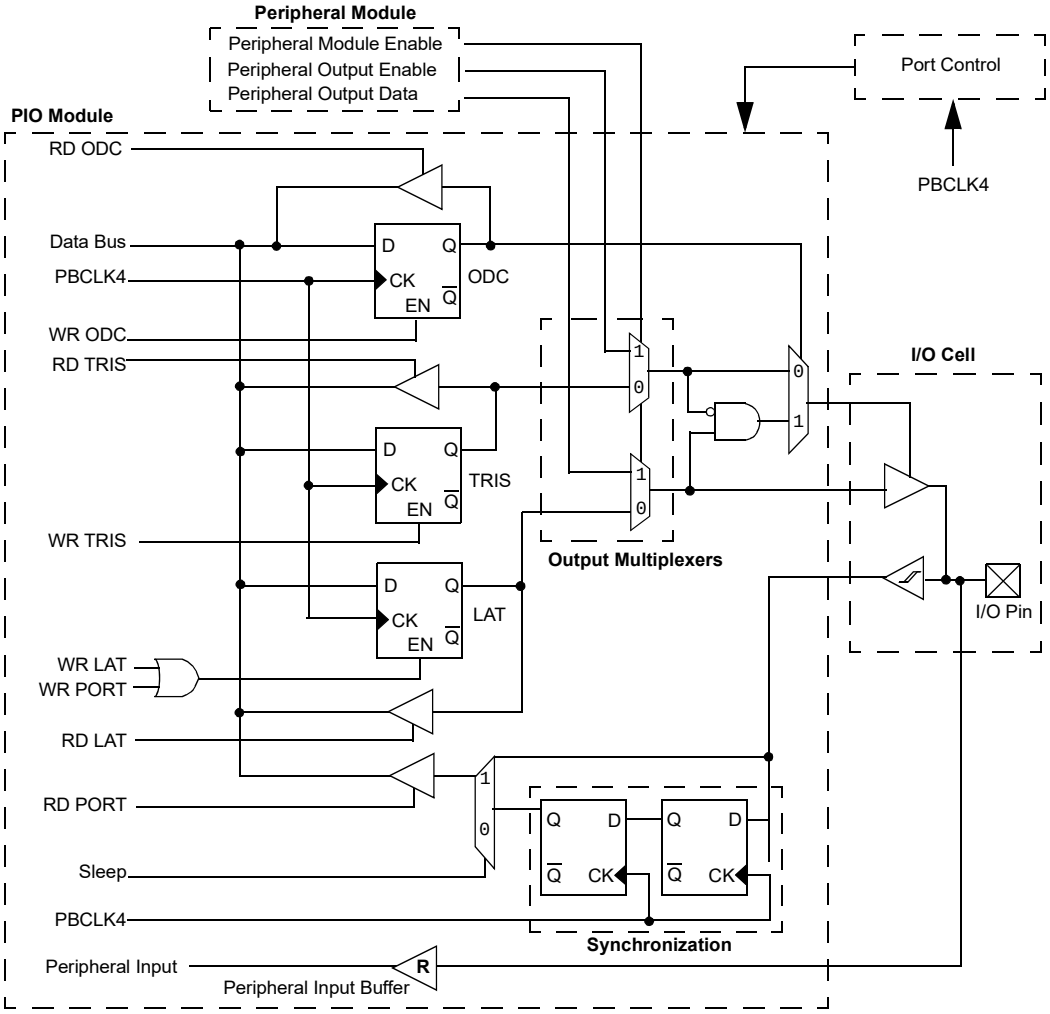
General purpose I/O pins are the simplest of peripherals. They allow the PIC32MK GP/MC family device to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

The following are key features of the I/O ports:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep mode and Idle mode
- Fast bit manipulation using CLR, SET, and INV registers

Figure 13-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 13-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



Legend: R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

Note: This block diagram is a general representation of a shared port/peripheral structure for illustration purposes only. The actual structure for any specific port/peripheral combination may be different than it is shown here.

13.1 Parallel I/O (PIO) Ports

All port pins have ten registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

13.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

Refer to the pin name tables (Table 3 and Table 5) for the available pins and their functionality.

13.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

13.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be an NOP.

13.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MK GP/MC devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx and CNNEx registers contain the CN interrupt enable control bits for each of the input pins. Setting these bits enables a CN interrupt for the corresponding pins. The CNENx register enables a mismatch CN interrupt condition when the EDGEDETECT bit (CNCONx<11>) is not set. When the EDGEDETECT bit is set, the CNNEx register controls the negative edge while the CNENx register controls the positive edge.

The CNSTATx and CNFx registers indicate the status of change notice based on the setting of the EDGEDETECT bit. If the EDGEDETECT bit is set to '0', the CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit. If the EDGEDETECT bit is set to '1', the CNFx register indicates whether a change has occurred and through the CNNEx and CNENx registers the edge type of the change that occurred is also indicated.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

An additional control register (CNCONx) is shown in Register 13-3.

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13.2 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

13.3 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

13.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

13.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (UART, SPI, and CAN), general purpose timer clock inputs, timer-related peripherals (input capture and output compare), interrupt-on-change inputs, and reference clocks (input and output).

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

13.3.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

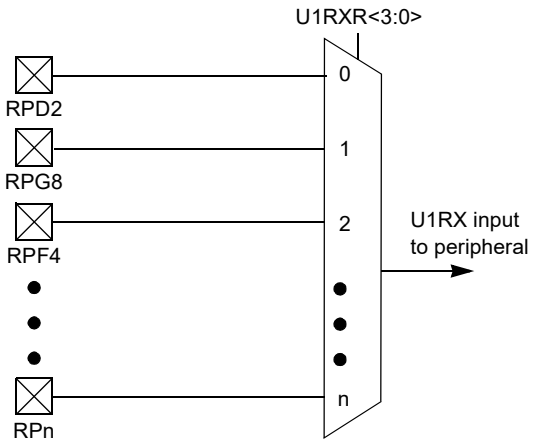
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

13.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 13-1, are used to configure peripheral input mapping (see Register 13-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 13-1.

Figure 13-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 13-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

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TABLE 13-1: INPUT PIN SELECTION

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT4	INT4R<3:0>	INT4R	0000 = RPA0
T2CK	T2CKR<3:0>	T2CKR	0001 = RPB3
T6CK	T6CKR<3:0>	T6CKR	
IC4	IC4R<3:0>	IC4R	0010 = RPB4
IC7	IC7R<3:0>	IC7R	0011 = RPB15
IC12	IC12R<3:0>	IC12R	
IC15	IC15R<3:0>	IC15R	0100 = RPB7
U3RX	U3RXR<3:0>	U3RXR	0101 = RPC7
$\overline{\text{U4CTS}}$	U4CTSR<3:0>	U4CTSR	
U6RX	U6RXR<3:0>	U6RXR	0110 = RPC0
SDI1	SDI1R<3:0>	SDI1R	0111 = Reserved
SDI3	SDI3R<3:0>	SDI3R	
SCK4	SCK4R<3:0>	SCK4R	1000 = RPA11
SDI5	SDI5R<3:0>	SDI5R	1001 = RPD5
$\overline{\text{SS6}}$	SS6R<3:0>	SS6R	
QEA1	QEA1R<3:0>	QEA1R	1010 = RPG6
HOME2	HOME2R<3:0>	HOME2R	1011 = RPF1
QAEA3	QAEA3R<3:0>	QEA3R	
HOME4	HOME4R<3:0>	HOME4R	1100 = RPE0(1)
QEA5	QEA5R<3:0>	QEA5R	1101 = RPA15(1)
HOME6	HOME6R<3:0>	HOME6R	
FLT1	FLT1R<3:0>	FLT1R	1110 = Reserved
C3RX	C3RXR<3:0>	C3RXR	
REFCLKI	REFIR<3:0>	REFIR	1111 = Reserved

Note 1: This selection is not available on 64-pin devices.

TABLE 13-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT3	INT3R<3:0>	INT3R	0000 = RPA1
T3CK	T3CKR<3:0>	T3CKR	0001 = RPB5
T7CK	T7CKR<3:0>	T7CKR	0010 = RPB1
IC3	IC3R<3:0>	IC3R	0011 = RPB11
IC8	IC8R<3:0>	IC8R	0100 = RPB8
IC11	IC11R<3:0>	IC11R	0101 = RPA8
IC16	IC16R<3:0>	IC16R	0110 = RPC8
$\overline{\text{U1CTS}}$	U1CTSR<3:0>	U1CTSR	0111 = RPB12
U2RX	U2RXR<3:0>	U2RXR	1000 = RPA12
$\overline{\text{U5CTS}}$	U5CTSR<3:0>	U5CTSR	1001 = RPD6
SDI2	SDI2R<3:0>	SDI2R	1010 = RPG7
SDI4	SDI4R<3:0>	SDI4R	1011 = RPG0(1)
SCK6	SCK6R<3:0>	SCK6R	1100 = RPE1(1)
QEB1	QEB1R<3:0>	QEB1R	1101 = RPA14(1)
INDX2	INDX2R<3:0>	INDX2R	1110 = Reserved
QEB3	QEB3R<3:0>	QEB3R	1111 = Reserved
INDX4	INDX4R<3:0>	INDX4R	
QEB5	QEB5R<3:0>	QEB5R	
INDX6	INDX6R<3:0>	INDX6R	
C2RX	C2RXR<3:0>	C2RXR	
FLT2	FLT2R<3:0>	FLT2R	

Note 1: This selection is not available on 64-pin devices.

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TABLE 13-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT2	INT2R<3:0>	INT2R	0000 = RPB6
T4CK	T4CKR<3:0>	T4CKR	0001 = RPC15
T8CK	T8CKR<3:0>	T8CKR	0010 = RPA4
IC1	IC1R<3:0>	IC1R	0011 = RPB13
IC5	IC5R<3:0>	IC5R	0100 = RPB2
IC9	IC9R<3:0>	IC9R	0101 = RPC6
IC13	IC13R<3:0>	IC13R	0110 = RPC1
U1RX	U1RXR<3:0>	U1RXR	0111 = RPA7
$\overline{\text{U2CTS}}$	U2CTSR<3:0>	U2CTSR	1000 = RPE14
U5RX	U5RXR<3:0>	U5RXR	1001 = RPC13
$\overline{\text{SS1}}$	SS1R<3:0>	SS1R	1010 = RPG8
$\overline{\text{SS3}}$	SS3R<3:0>	SS3R	1011 = Reserved
$\overline{\text{SS4}}$	SS4R<3:0>	SS4R	1100 = RPF0
$\overline{\text{SS5}}$	SS5R<3:0>	SS5R	1101 = RPD4(1)
INDX1	INDX1R<3:0>	INDX1R	1110 = Reserved
QEB2	QEB2R<3:0>	QEB2R	1111 = Reserved
INDX3	INDX3R<3:0>	INDX3R	
QEB4	QEB4R<3:0>	QEB4R	
INDX5	INDX5R<3:0>	INDXR5	
QEB6	QEB6R<3:0>	QEB6R	
C1RX	C1RXR<3:0>	C1RXR	
OCFB	OCFBR<3:0>	OCFBR	

Note 1: This selection is not available on 64-pin devices.

TABLE 13-1: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT1	INT1R<3:0>	INT1R	0000 = RPB14
T5CK	T5CKR<3:0>	T5CKR	0001 = RPC12
T9CK	T9CKR<3:0>	T9CKR	
IC2	IC2R<3:0>	IC2R	0010 = RPB0
IC6	IC6R<3:0>	IC6R	0011 = RPB10
IC10	IC10R<3:0>	IC10R	0100 = RPB9
IC14	IC14R<3:0>	IC14R	
$\overline{\text{U3CTS}}$	U3CTSR<3:0>	U3CTSR	0101 = RPC9
U4RX	U4RXR<3:0>	U4RXR	0110 = RPC2
$\overline{\text{U6CTS}}$	U6CTSR<3:0>	U6CTSR	
$\overline{\text{SS2}}$	SS2R<3:0>	SS2R	0111 = Reserved
SCK3	SCK3R<3:0>	SCK3R	1000 = RPE15
SCK5	SCK5R<3:0>	SCK5R	1001 = RPC10
SDI6	SDI6R<3:0>	SDI6R	
HOME1	HOME1R<3:0>	HOME1R	1010 = RPG9
QEA2	QEA2R<3:0>	QEA2R	1011 = RPG12(1)
HOME3	HOME3R<3:0>	HOME3R	
QEA4	QEA4R<3:0>	QEA4R	1100 = RPG1(1)
HOME5	HOME5R<3:0>	HOME5R	1101 = RPD3(1)
QEA6	QEA6R<3:0>	QEA6R	1110 = Reserved
C4RX	C4RXR<3:0>	C4RXR	
OCFA	OCFAR<3:0>	OCFAR	1111 = Reserved

Note 1: This selection is not available on 64-pin devices.

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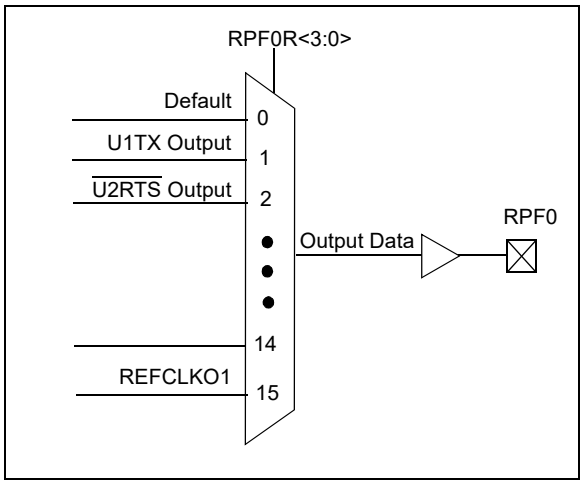
13.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 13-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 13-2 and Figure 13-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 13-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPF0



13.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. The PIC32MK GP/MC devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

13.3.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting the IOLOCK bit prevents writes to the control registers and clearing the IOLOCK bit allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to the **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

13.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If the IOLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

TABLE 13-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPA0	RPA0R	RPA0R<4:0>	00000 = Off 00001 = U1TX 00010 = U2RTS 00011 = SDO1 00100 = SDO2 00101 = OCI 00110 = OC7 00111 = C2OUT 01000 = C4OUT 01001 = OC13 01010 = Reserved 01011 = U5RTS 01100 = C1TX 01101 = Reserved 01110 = SDO3 01111 = SCK4 10000 = SDO5 10001 = SS6 10010 = REFCLKO4 10011 = Reserved 10100 = QEICMP1 10101 = QEICMP5 10110 = Reserved . . . 11111 = Reserved
RPB3	RPB3R	RPB3R<4:0>	
RPB4	RPB4R	RPB4R<4:0>	
RPB15	RPB15R	RPB15R<4:0>	
RPB7	RPB7R	RPB7R<4:0>	
RPC7	RPC7R	RPC7R<4:0>	
RPC0	RPC0R	RPC0R<4:0>	
RPA11	RPA11R	RPA11R<4:0>	
RPD5	RPD5R	RPD5R<4:0>	
RPG6	RPG6R	RPG6R<4:0>	
RPF1	RPF1R	RPF1R<4:0>	
RPE0(1)	RPE0R(1)	RPE0R<4:0> (1)	
RPA15(1)	RPA15R(1)	RPA15R<4:0> (1)	

Note 1: This selection is not available on 64-pin devices.

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TABLE 13-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPA1	RPA1R	RPA1R<4:0>	00000 = Off 00001 = U3RTS 00010 = U4TX 00011 = SDO1 00100 = SDO2 00101 = OC2 00110 = OC8 00111 = C3OUT 01000 = OC9 01001 = OC12 01010 = OC16 01011 = U6RTS 01100 = C4TX 01101 = Reserved 01110 = SDO3 01111 = SDO4 10000 = SDO5 10001 = SCK6 10010 = REFCLKO3 10011 = Reserved 10100 = QEICMP2 10101 = QEICMP6 10110 = Reserved . . . 11111 = Reserved
RPB5	RPB5R	RPB5R<4:0>	
RPB1	RPB1R	RPB1R<4:0>	
RPB11	RPB11R	RPB11R<4:0>	
RPA8	RPA8R	RPA8R<4:0>	
RPC8	RPC8R	RPC8R<4:0>	
RPB12	RPB12R	RPB12R<4:0>	
RPA12	RPA12R	RPA12R<4:0>	
RPD6	RPD6R	RPD6R<4:0>	
RPG7	RPG7R	RPG7R<4:0>	
RPG0(1)	RPG0R(1)	RPG0R<4:0> (1)	
RPE1(1)	RPE1R(1)	RPE1R<4:0> (1)	
RPA14(1)	RPA14R(1)	RPA14R<4:0> (1)	

Note 1: This selection is not available on 64-pin devices.

TABLE 13-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPB6	RPB6R	RPB6R<4:0>	00000 = Off 00001 = U3TX 00010 = U4RTS 00011 = SS1 00100 = Reserved 00101 = OC4 00110 = OC5 00111 = REFCLKO1 01000 = C5OUT 01001 = OC10 01010 = OC14 01011 = U6TX 01100 = C3TX 01101 = Reserved 01110 = SS3 01111 = SS4 10000 = SS5 10001 = SDO6 10010 = REFCLKO2 10011 = Reserved 10100 = QEICMP3 10101 = Reserved . . . 11111 = Reserved
RPC15	RPC15R	RPC15R<4:0>	
RPA4	RPA4R	RPA4R<4:0>	
RPB13	RPB13R	RPB13R<4:0>	
RPB2	RPB2R	RPB2R<4:0>	
RPC6	RPC6R	RPC6R<4:0>	
RPC1	RPC1R	RPC1R<4:0>	
RPA7	RPA7R	RPA7R<4:0>	
RPE14	RPE14R	RPE14R<4:0>	
RPG8	RPG8R	RPG8R<4:0>	
RPF0	RPF0R	RPF0R<4:0>	
RPD4(1)	RPD4R(1)	RPD4R<4:0> (1)	

Note 1: This selection is not available on 64-pin devices.

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TABLE 13-2: OUTPUT PIN SELECTION (CONTINUED)

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPB14	RPB14R	RPB14R<4:0>	00000 = Off 00001 = U1RTS 00010 = U2TX 00011 = Reserved 00100 = SS2 00101 = OC3 00110 = OC6 00111 = C1OUT 01000 = Reserved 01001 = OC11 01010 = OC15 01011 = U5TX 01100 = C2TX 01101 = Reserved 01110 = SCK3 01111 = SDO4 10000 = SCK5 10001 = SDO6 10010 = CTPLS 10011 = Reserved 10100 = QEICMP4 10101 = Reserved • • • 11111 = Reserved
RPC12	RPC12R	RPC12R<4:0>	
RPB0	RPB0R	RPB0R<4:0>	
RPB10	RPB10R	RPB10R<4:0>	
RPB9	RPB9R	RPB9R<4:0>	
RPC9	RPC9R	RPC9R<4:0>	
RPC2	RPC2R	RPC2R<4:0>	
RPE15	RPE15R	RPE15R<4:0>	
RPC10	RPC10R	RPC10R<4:0>	
RPG9	RPG9R	RPG9R<4:0>	
RPG12(1)	RPG12R(1)	RPG12R<4:0>	
RPG1(1)	RPG1R(1)	RPG1R<4:0> (1)	
RPD3(1)	RPD3R(1)	RPD3R<4:0> (1)	

Note 1: This selection is not available on 64-pin devices.

13.4 I/O Ports Control Registers

TABLE 13-3: PORTA REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSA15	ANSA14	—	ANSA12	ANSA11	—	—	ANSA8	—	—	—	ANSA4	—	—	ANSA1	ANSA0	D813
0010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	TRISA12	TRISA11	TRISA10	—	TRISA8	TRISA7	—	—	TRISA4	—	—	TRISA1	TRISA0	DD93
0020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	RA12	RA11	RA10	—	RA8	RA7	—	—	RA4	—	—	RA1	RA0	xxxx
0030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	LATA12	LATA11	LATA10	—	LATA8	LATA7	—	—	LATA4	—	—	LATA1	LATA0	xxxx
0040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	ODCA12	ODCA11	ODCA10	—	ODCA8	ODCA7	—	—	ODCA4	—	—	ODCA1	ODCA0	0000
0050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUA15	CNPUA14	—	CNPUA12	CNPUA11	CNPUA10	—	CNPUA8	CNPUA7	—	—	CNPUA4	—	—	CNPUA1	CNPUA0	0000
0060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDA15	CNPDA14	—	CNPDA12	CNPDA11	CNPDA10	—	CNPDA8	CNPDA7	—	—	CNPDA4	—	—	CNPDA1	CNPDA0	0000
0070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEA15	CNIEA14	—	CNIEA12	CNIEA11	CNIEA10	—	CNIEA8	CNIEA7	—	—	CNIEA4	—	—	CNIEA1	CNIEA0	0000
0090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATA15	CN STATA14	—	CN STATA12	CN STATA11	CN STATA10	—	CN STATA8	CN STATA7	—	—	CN STATA4	—	—	CN STATA1	CN STATA0	0000
00A0	CNNEA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEA15	CNNEA14	—	CNNEA12	CNNEA11	CNNEA10	—	CNNEA8	CNNEA7	—	—	CNNEA4	—	—	CNNEA1	CNNEA0	0000
00B0	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFA15	CNFA14	—	CNFA12	CNFA11	CNFA10	—	CNFA8	CNFA7	—	—	CNFA4	—	—	CNFA1	CNFA0	0000
00C0	SRCON0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR0A10	—	SR0A8	SR0A7	—	—	—	—	—	—	—	0000
00D0	SRCON1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR1A10	—	SR1A8	SR1A7	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-4: PORTA REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ANSA12	ANSA11	—	—	ANSA8	—	—	—	ANSA4	—	—	ANSA1	ANSA0	0623
0010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	TRISA12	TRISA11	TRISA10	—	TRISA8	TRISA7	—	—	TRISA4	—	—	TRISA1	TRISA0	06FF
0020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	RA12	RA11	RA10	—	RA8	RA7	—	—	RA4	—	—	RA1	RA0	xxxx
0030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	LATA12	LATA11	LATA10	—	LATA8	LATA7	—	—	LATA4	—	—	LATA1	LATA0	xxxx
0040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ODCA12	ODCA11	ODCA10	—	ODCA8	ODCA7	—	—	ODCA4	—	—	ODCA1	ODCA0	0000
0050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNPUA12	CNPUA11	CNPUA10	—	CNPUA8	CNPUA7	—	—	CNPUA4	—	—	CNPUA1	CNPUA0	0000
0060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNPDA12	CNPDA11	CNPDA10	—	CNPDA8	CNPDA7	—	—	CNPDA4	—	—	CNPDA1	CNPDA0	0000
0070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNIEA12	CNIEA11	CNIEA10	—	CNIEA8	CNIEA7	—	—	CNIEA4	—	—	CNIEA1	CNIEA0	0000
0090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CN STATA12	CN STATA11	CN STATA10	—	CN STATA8	CN STATA7	—	—	CN STATA4	—	—	CN STATA1	CN STATA0	0000
00A0	CNNEA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNNEA12	CNNEA11	CNNEA10	—	CNNEA8	CNNEA7	—	—	CNNEA4	—	—	CNNEA1	CNNEA0	0000
00B0	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CNFA12	CNFA11	CNFA10	—	CNFA8	CNFA7	—	—	CNFA4	—	—	CNFA1	CNFA0	0000
00C0	SRCON0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR0A10	—	SR0A8	SR0A7	—	—	—	—	—	—	—	0000
00D0	SRCON1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SR1A10	—	SR1A8	SR1A7	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-5: PORTB REGISTER MAP FOR 64-PIN AND 100-PIN DEVICES

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSB9	—	ANSB7	—	—	—	ANSB3	ANSB2	ANSB1	ANSB0	008F
0110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
0120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
0130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
0140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
0150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
0160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
0170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
0190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000
01A0	CNNEB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEB15	CNNEB14	CNNEB13	CNNEB12	CNNEB11	CNNEB10	CNNEB9	CNNEB8	CNNEB7	CNNEB6	CNNEB5	CNNEB4	CNNEB3	CNNEB2	CNNEB1	CNNEB0	0000
01B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB15	CNFB14	CNFB13	CNFB12	CNFB11	CNFB10	CNFB9	CNFB8	CNFB7	CNFB6	CNFB5	CNFB4	CNFB3	CNFB2	CNFB1	CNFB0	0000
01C0	SRCON0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0B15	SR0B14	SR0B13	SR0B12	SR0B11	SR0B10	—	—	SR0B7	SR0B6	—	SR0B4	—	—	—	—	0000
01D0	SRCON1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1B15	SR1B14	SR1B13	SR1B12	SR1B11	SR1B10	—	—	SR1B7	SR1B6	—	SR1B4	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-6: PORTC REGISTER MAP FOR 64-PIN AND 100-PIN DEVICES

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ANSC12	ANSC11	ANSC10	—	—	—	—	—	—	—	ANSC2	ANSC1	ANSC0	1007
0210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC15	TRISC14	TRISC13	TRISC12	TRISC11	TRISC10	TRIS92	TRISC8	TRISC7	TRISC6	—	—	—	TRISC2	TRISC1	TRISC0	FFC7
0220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8	RC7	RC6	—	—	—	RC2	RC1	RC0	xxxx
0230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC15	LATC14	LATC13	LATC12	LATC11	LATC10	LATC9	LATC8	LATC7	LATC6	—	—	—	LATC2	LATC1	LATC0	xxxx
0240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC15	ODCC14	ODCC13	ODCC12	ODCC11	ODCC10	ODCC9	ODCC8	ODCC7	ODCC6	—	—	—	ODCC2	ODCC1	ODCC0	0000
0250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC15	CNPUC14	CNPUC13	CNPUC12	CNPUC11	CNPUC10	CNPUC9	CNPUC8	CNPUC7	CNPUC6	—	—	—	CNPUC2	CNPUC1	CNPUC0	0000
0260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC15	CNPDC14	CNPDC13	CNPDC12	CNPDC11	CNPDC10	CNPDC9	CNPDC8	CNPDC7	CNPDC6	—	—	—	CNPDC2	CNPDC1	CNPDC0	0000
0270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0280	CNENC	31:16	—	—		—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEC15	CNIEC14	CNIEC13	CNIEC12	CNIEC11	CNIEC10	CNIEC9	CNIEC8	CNIEC7	CNIEC7	—	—	—	CNIEC2	CNIEC1	CNIEC0	0000
0290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATC15	CN STATC14	CN STATC13	CN STATC12	CN STATC11	CN STATC10	CN STATC9	CN STATC8	CN STATC7	CN STATC6	—	—	—	CN STATC2	CN STATC1	CN STATC0	0000
02A0	CNNEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEC15	CNNEC14	CNNEC13	CNNEC12	CNNEC11	CNNEC10	CNNEC9	CNNEC8	CNNEC7	CNNEC6	—	—	—	CNNEC2	CNNEC1	CNNEC0	0000
02B0	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC15	CNFC14	CNFC13	CNFC12	CNFC11	CNFC10	CNFC9	CNFC8	CNFC7	CNFC6	—	—	—	CNFC2	CNFC1	CNFC0	0000
02C0	SRCON0C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0C15	—	—	—	SR0C11	—	SR0C9	SR0C8	SR0C7	SR0C6	—	—	—	—	—	—	0000
02D0	SRCON1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1C15	—	—	—	SR1C11	—	SR1C9	SR1C8	SR1C7	SR1C6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-7: PORTD REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD15	ANSD14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	—	—	—	TRISD8(2)	—	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	—	F1FE
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	—	—	—	RD8(2)	—	RD6	RD5	RD4	RD3	RD2	RD1	—	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	—	—	—	LATD8(2)	—	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	—	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	—	—	—	ODCD8(2)	—	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	—	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	—	—	—	CNPUD8(2)	—	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	—	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	—	—	—	CNPDD8(2)	—	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	—	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIED15	CNIED14	CNIED13	CNIED12	—	—	—	CNIED8(2)	—	CNIED6	CNIED5	CNIED4	CNIED3	CNIED2	CNIED1	—	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNS TATD15	CN STATD14	CN STATD13	CN STATD12	—	—	—	CN STATD8(2)	—	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	—	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNED15	CNNED14	CNNED13	CNNED12	—	—	—	CNNED8(2)	—	CNNED6	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	—	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFD15	CNFD14	CNFD13	CNFD12	—	—	—	CNFD8(2)	—	CNFD6	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	—	0000
03C0	SRCON0D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR0D8(2)	—	SR0D6	SR0D5	SR0D4	SR0D3	SR0D2	SR0D1	—	0000
03D0	SRCON1D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR1D8(2)	—	SR1D6	SR1D5	SR1D4	SR1D3	SR1D2	SR1D1	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on general purpose devices.

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TABLE 13-8: PORTD REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TRISD8(2)	—	TRISD6	TRISD5	—	—	—	—	—	0160
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RD8(2)	—	RD6	RD5	—	—	—	—	—	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	LATD8(2)	—	LATD6	LATD5	—	—	—	—	—	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	ODCD8(2)	—	ODCD6	ODCD5	—	—	—	—	—	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNPUD8(2)	—	CNPUD6	CNPUD5	—	—	—	—	—	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNPDD8(2)	—	CNPDD6	CNPDD5	—	—	—	—	—	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNIED8(2)	—	CNIED6	CNIED5	—	—	—	—	—	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CN STATD8(2)	—	CN STATD6	CN STATD5	—	—	—	—	—	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNNED8(2)	—	CNNED6	CNNED5	—	—	—	—	—	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	CNFD8(2)	—	CNFD6	CNFD5	—	—	—	—	—	0000
03C0	SRCON0D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR0D8(2)	—	SR0D6	SR0D5	—	—	—	—	—	0000
03D0	SRCON1D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	SR1D8(2)	—	SR1D6	SR1D5	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This bit is not available on general purpose devices.

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TABLE 13-9: PORTE REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSE15	ANSE14	ANSE13	ANSE12	—	—	ANSE9	ANSE8	—	—	—	—	—	—	ANSE1	ANSE0	F303
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISE15	TRISE14	TRISE13	TRISE12	—	—	TRISE9	TRISE8	—	—	—	—	—	—	TRISE1	TRISE0	F303
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RE15	RE14	RE13	RE12	—	—	RE9	RE8	—	—	—	—	—	—	RE1	RE0	xxxx
0440	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATE15	LATE14	LATE13	LATE12	—	—	LATE9	LATE8	—	—	—	—	—	—	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCE15	ODCE14	ODCE13	ODCE12	—	—	ODCE9	ODCE8	—	—	—	—	—	—	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	—	CNPUE9	CNPUE8	—	—	—	—	—	—	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	—	CNPDE9	CNPDE8	—	—	—	—	—	—	CNPDE1	CNPDE0	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIEE9	CNIEE8	—	—	—	—	—	—	CNIEE1	CNIEE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATE15	CN STATE14	CN STATE13	CN STATE12	—	—	CN STATE9	CN STATE8	—	—	—	—	—	—	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEE15	CNNEE14	CNNEE13	CNNEE12	—	—	CNNEE9	CNNEE8	—	—	—	—	—	—	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFE15	CNFE14	CNFE13	CNFE12	—	—	CNFE9	CNFE8	—	—	—	—	—	—	CNFE1	CNFE0	0000
04C0	SRCON0E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0E15	SR0E14	SR0E13	SR0E12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1E15	SR1E14	SR1E13	SR1E12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-10: PORTE REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSE15	ANSE14	ANSE13	ANSE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISE15	TRISE14	TRISE13	TRISE12	—	—	—	—	—	—	—	—	—	—	—	—	F000
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RE15	RE14	RE13	RE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0440	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATE15	LATE14	LATE13	LATE12	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCE15	ODCE14	ODCE13	ODCE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUE15	CNPUE14	CNPUE13	CNPUE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDE15	CNPDE14	CNPDE13	CNPDE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATE15	CN STATE14	CN STATE13	CN STATE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEE15	CNNEE14	CNNEE13	CNNEE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFE15	CNFE14	CNFE13	CNFE12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04C0	SRCON0E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR0E15	SR0E14	SR0E13	SR0E12	—	—	—	—	—	—	—	—	—	—	—	—	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SR1E15	SR1E14	SR1E13	SR1E12	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-11: PORTF REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0500	ANSELF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ANSF13	ANSF12	—	ANSF10	ANSF9	—	—	—	ANSF5	—	—	—	—	—	3620
0510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	TRISF10	TRISF9	—	TRISF7	TRISF6	TRISF5	—	—	—	TRISF1	TRISF0	36E3
0520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	RF10	RF9	—	RF7	RF6	RF5	—	—	—	RF1	RF0	xxxx
0530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	LATF10	LATF9	—	LATF7	LATF6	LATF5	—	—	—	LATF1	LATF0	xxxx
0540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	ODCF10	ODCF9	—	ODCF7	ODCF6	ODCF5	—	—	—	ODCF1	ODCF0	0000
0550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPUF13	CNPUF12	—	CNPUF10	CNPUF9	—	CNPUF7	CNPUF6	CNPUF5	—	—	—	CNPUF1	CNPUF0	0000
0560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPDF13	CNPDF12	—	CNPDF10	CNPDF9	—	CNPDF7	CNPDF6	CNPDF5	—	—	—	CNPDF1	CNPDF0	0000
0570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNIEF13	CNIEF12	—	CNIEF10	CNIEF9	—	CNIEF7	CNIEF6	CNIEF5	—	—	—	CNIEF1	CNIEF0	0000
0590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CN STATF13	CN STATF12	—	CN STATF10	CN STATF9	—	CN STATF7	CN STATF6	CN STATF5	—	—	—	CN STATF1	CN STATF0	0000
05A0	CNNEF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNNEF13	CNNEF12	—	CNNEF10	CNNEF9	—	CNNEE7	CNNEF6	CNNEF5	—	—	—	CNNEF1	CNNEF0	0000
05B0	CNFF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNFF13	CNFF12	—	CNFF10	CNFF9	—	CNFE7	CNFF6	CNFF5	—	—	—	CNFF1	CNFF0	0000
05C0	SRCON0F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR0F1	SR0F0	0000
05D0	SRCON1F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR1F1	SR1F0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-12: PORTF REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF1	TRISF0	0003
0520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF1	RF0	xxxx
0530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF1	LATF0	xxxx
0540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF1	ODCF0	0000
0550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF1	CNPUF0	0000
0560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF1	CNPDF0	0000
0570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF1	CNIEF0	0000
0590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CN STATF1	CN STATF0	0000
05A0	CNNEF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNNEF1	CNNEF0	0000
05B0	CNFF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNFF1	CNFF0	0000
05C0	SRCON0F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR0F1	SR0F0	0000
05D0	SRCON1F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR1F1	SR1F0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-13: PORTG REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSG15	—	—	—	ANSG11	ANSG10	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	8FC0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISG15	TRISG14	TRISG13	TRISG12	TRISG11	TRISG10	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	TRISG1	TRISG0	FFC3
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RG15	RG14	RG13	RG12	RG11	RG10	RG9	RG8	RG7	RG6	—	—	—	—	RG1	RG0	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATG15	LATG14	LATG13	LATG12	LATG11	LATG10	LATG9	LATG8	LATG7	LATG6	—	—	—	—	LATG1	LATG0	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCG15	ODCG14	ODCG13	ODCG12	ODCG11	ODCG10	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	ODCG1	ODCG0	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUG15	CNPUG14	CNPUG13	CNPUG12	CNPUG11	CNPUG10	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	CNPUG1	CNPUG0	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDG15	CNPDG14	CNPDG13	CNPDG12	CNPDG11	CNPDG10	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	CNPDG1	CNPDG0	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIEG15	CNIEG14	CNIEG13	CNIEG12	CNIEG11	CNIEG10	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	CNIEG1	CNIEG0	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATG15	CN STATG14	CN STATG13	CN STATG12	CN STATG11	CN STATG10	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	CN STATG1	CN STATG0	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEG15	CNNEG14	CNNEG13	CNNEG12	CNNEG11	CNNEG10	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	CNNEG1	CNNEG0	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFG15	CNFG14	CNFG13	CNFG12	CNFG11	CNFG10	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	CNFG1	CNFG0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-14: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIEG9	CNIEG8	CNIEG7	CNIEG6	—	—	—	—	—	—	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	—	—	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	—	—	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1404	INT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT1R<3:0>				0000
1408	INT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT2R<3:0>				0000
140C	INT3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT3R<3:0>				0000
1410	INT4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT4R<3:0>				0000
1418	T2CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T2CKR<3:0>				0000
141C	T3CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T3CKR<3:0>				0000
1420	T4CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T4CKR<3:0>				0000
1424	T5CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T5CKR<3:0>				0000
1428	T6CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T6CKR<3:0>				0000
142C	T7CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T7CKR<3:0>				0000
1430	T8CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T8CKR<3:0>				0000
1434	T9CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T9CKR<3:0>				0000
1438	IC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC1R<3:0>				0000
143C	IC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC2R<3:0>				0000
1440	IC3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

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4: This register is only available on motor control variants.

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TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1444	IC4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC4R<3:0>				0000
1448	IC5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC5R<3:0>				0000
144C	IC6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC6R<3:0>				0000
1450	IC7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC7R<3:0>				0000
1454	IC8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC8R<3:0>				0000
1458	IC9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC9R<3:0>				0000
145C	OCFAR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	OCFAR<3:0>				0000
1460	OCFBR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	OCFBR<3:0>				0000
1464	U1RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1RXR<3:0>				0000
1468	U1CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1CTSR<3:0>				0000
146C	U2RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2RXR<3:0>				0000
1470	U2CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2CTSR<3:0>				0000
1474	U3RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U3RXR<3:0>				0000
1478	U3CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U3CTSR<3:0>				0000
147C	U4RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U4RXR<3:0>				0000

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Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1480	U4CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U4CTSR<3:0>				0000
1484	U5RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U5RXR<3:0>				0000
1488	U5CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U5CTSR<3:0>				0000
148C	U6RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U6RXR<3:0>				0000
1490	U6CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U6CTSR<3:0>				0000
1498	SDI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI1R<3:0>				0000
149C	SS1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS1R<3:0>				0000
14A4	SDI2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI2R<3:0>				0000
14A8	SS2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS2R<3:0>				0000
14AC	SCK3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK3R<3:0>				0000
14B0	SDI3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI3R<3:0>				0000
14B4	SS3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS3R<3:0>				0000
14B8	SCK4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK4R<3:0>				0000
14BC	SDI4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI4R<3:0>				0000
14C0	SS4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS4R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14C4	C1RXR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C1RXR<3:0>				0000
14C8	C2RXR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C2RXR<3:0>				0000
14CC	REFIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFIR<3:0>				0000
14D0	QEA1R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA1R<3:0>				0000
14D4	QEB1R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB1R<3:0>				0000
14D8	INDX1R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INDX1R<3:0>				0000
14DC	HOME1R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HOME1R<3:0>				0000
14E0	QEA2R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA2R<3:0>				0000
14E4	QEB2R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB2R<3:0>				0000
14E8	INDX2R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INDX2R<3:0>				0000
14EC	HOME2R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HOME2R<3:0>				0000
14F0	FLT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	FLT1R<3:0>				0000
14F4	FLT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	FLT2R<3:0>				0000
14F8	IC10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC10R<3:0>				0000
14FC	IC11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC11R<3:0>				0000

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1500	IC12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC12R<3:0>				0000
1504	IC13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC13R<3:0>				0000
1508	IC14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC14R<3:0>				0000
150C	IC15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC15R<3:0>				0000
1510	IC16R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC16R<3:0>				0000
1514	SCK5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK5R<3:0>				
1518	SDI5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI5R<3:0>				0000
151C	SS5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS5R<3:0>				0000
1520	SCK6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SCK6R<3:0>				
1524	SDI6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI6R<3:0>				0000
1528	SS6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS6R<3:0>				0000
152C	C3RXR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C3RXR<3:0>				0000
1530	C4RXR(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	C4RXR<3:0>				0000
1534	QEA3R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA3R<3:0>				0000
1538	QEB3R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

3: This register is only available on PIC32MKXXX*XGPE*/MCF*XXX devices.

4: This register is only available on motor control variants.

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TABLE 13-15: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
153C	INDX3R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INDX3R<3:0>				0000
1540	HOME3R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HOME3R<3:0>				0000
1544	QEA4R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA4R<3:0>				0000
1548	QEB4R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB4R<3:0>				0000
154C	INDX4R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INDX4R<3:0>				0000
1550	HOME4R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HOME4R<3:0>				0000
1554	QEA5R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA5R<3:0>				0000
1558	QEB5R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB5R<3:0>				0000
155C	INDX5R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INDX5R<3:0>				0000
1560	HOME5R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HOME5R<3:0>				0000
1564	QEA6R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEA6R<3:0>				0000
1568	QEB6R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	QEB6R<3:0>				0000
156C	INDX6R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INDX6R<3:0>				0000
1570	HOME6R(4)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	HOME6R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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4: This register is only available on motor control variants.

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TABLE 13-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1600	RPA0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA0R<4:0>					0000
1604	RPA1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA1R<4:0>					0000
1608	RPA2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA2R<4:0>					0000
160C	RPA3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA3R<4:0>					0000
1610	RPA4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA4R<4:0>					0000
161C	RPA7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA7R<4:0>					0000
1620	RPA8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA8R<4:0>					0000
162C	RPA11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA11R<4:0>					0000
1630	RPA12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA12R<4:0>					0000
1638	RPA14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA14R<4:0>					0000
163C	RPA15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPA15R<4:0>					0000
1640	RPB0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB0R<4:0>					0000
1644	RPB1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB1R<4:0>					0000
1648	RPB2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB2R<4:0>					0000
164C	RPB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB3R<4:0>					0000
1650	RPB4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB4R<4:0>					0000
1654	RPB5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB5R<4:0>					0000
1658	RPB6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB6R<4:0>					0000
165C	RPB7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB7R<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 13-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1664	RPB9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB9R<4:0>					0000
1668	RPB10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB10R<4:0>					0000
166C	RPB11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB11R<4:0>					0000
1670	RPB12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB12R<4:0>					0000
1674	RPB13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB13R<4:0>					0000
1678	RPB14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB14R<4:0>					0000
167C	RPB15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPB15R<4:0>					0000
1680	RPC0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC0R<4:0>					0000
1684	RPC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC1R<4:0>					0000
1688	RPC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC2R<4:0>					0000
1690	RPC4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC4R<4:0>					0000
1698	RPC6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC6R<4:0>					0000
169C	RPC7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC7R<4:0>					0000
16A0	RPC8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC8R<4:0>					0000
16A4	RPC9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC9R<4:0>					0000
16A8	RPC10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC10R<4:0>					0000
16B0	RPC12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC12R<4:0>					0000
16BC	RPC15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPC15R<4:0>					0000
16CC	RPD3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD3R<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 13-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
16D0	RPD4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD4R<4:0>					0000
16D4	RPD5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD5R<4:0>					0000
16D8	RPD6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPD6R<4:0>					0000
1700	RPE0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE0R<4:0>					0000
1704	RPE1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE1R<4:0>					0000
1738	RPE14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF14R<4:0>					0000
173C	RPE15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPE15R<4:0>					0000
1740	RPF0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF0R<4:0>					0000
1744	RPF1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPF1R<4:0>					0000
1780	RPG0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG0R<4:0>					0000
1784	RPG1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG1R<4:0>					0000
1798	RPG6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG6R<4:0>					0000
179C	RPG7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG7R<4:0>					0000
17A0	RPG8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG8R<4:0>					0000
17A4	RPG9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG9R<4:0>					0000
17B0	RPG12R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	RPG12R<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 13-1: [*pin name*]R: PERIPHERAL PIN SELECT INPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	[*pin name*]R<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **[*pin name*]R<3:0>:** Peripheral Pin Select Input bits
Where [*pin name*] refers to the pins that are used to configure peripheral input mapping. See Table 13-1 for input pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

REGISTER 13-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RPnR<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **RPnR<4:0>:** Peripheral Pin Select Output bits
See Table 13-2 for output pin selection values.

Note: Register values can only be changed if the IOLOCK Configuration bit (CFGCON<13>) = 0.

REGISTER 13-3: CNCONx: CHANGE NOTICE CONTROL FOR PORTx REGISTER (x = A – G)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	r-0	U-0	U-0
	ON	—	SIDL	—	EDGEDETECT	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit
- 1 = CN is enabled
- 0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = CPU Idle mode halts CN operation
- 0 = CPU Idle mode does not affect CN operation

bit 12 **Unimplemented:** Read as '0'

bit 11 **EDGEDETECT:** Edge Detection Type Control bit
- 1 = Detects any edge on the pin (CNx is used for the CN event)
- 0 = Detects any edge on the pin (CNSTATx is used for the CN event)

bit 10 **Reserved:** Always write '0'

bit 9-0 **Unimplemented:** Read as '0'

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14.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MK GP/MC devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the low-power Secondary Oscillator (SOSC) for real-time clock applications.

The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

14.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers
- Asynchronous mode can be used with the SOSC to function as a real-time clock
- ADC event trigger

14.2 TImer1 Usage Model Guidelines

14.2.1 EXTERNAL CLOCK MODE OPERATION

When the Timer is operating with an external clock mode with the TCS bit (TxCON<1>) = 1, the mode bits of the TxCON register must be initialized using a separate Write operation from that used to enable the Timer. Specifically, the TCS, TSYNC, etc. bits must be written first, and then the ON bit (TxCON<15>) must be set in a subsequent write.

Once the ON bit is set, any writes to the TxCON register may cause erroneous counter operation.

Note: The ON bit should be clear when updates are made to any other bits in the TxCON register.

14.2.2 ASYNCHRONOUS MODE OPERATION

When writing the ON bit when the Timer is configured in Asynchronous mode or in an external clock mode with the prescaler enabled, the act of setting the ON bit does not take effect until two rising edges of the external clock input have occurred.

14.2.3 ASYNCHRONOUS MODE OPERATION WITH A PENDING TMRx REGISTER WRITE

When the Timer is configured in Asynchronous mode and the Timer is attempting to write to the TMRx register while a previous write is awaiting synchronization, the value written to the timer can become corrupted.

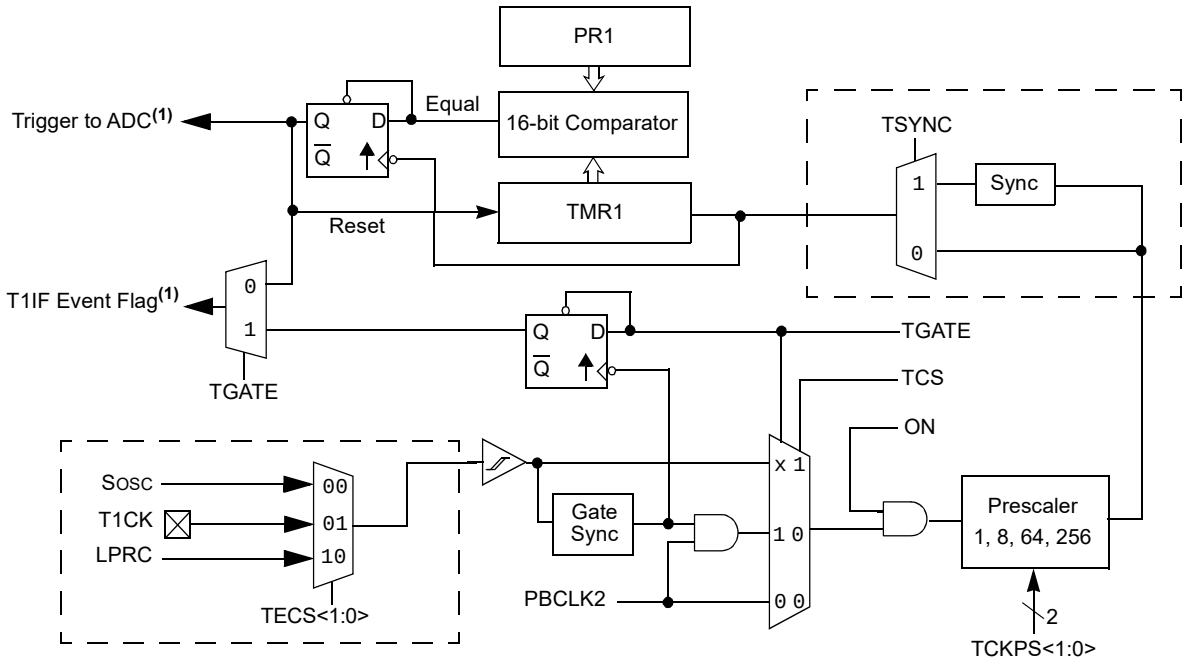
To ensure that writes will not cause the TMRx value to become corrupted, the TWDIS bit (TxCON<12>), when set, will ignore a write to the TMRx register when a previous write to the TMRx register is awaiting synchronization into the Asynchronous Timer Clock domain.

The TWIP bit (TxCON<11>) indicates when write synchronization is complete, and it is safe to write another value to the timer.

14.2.4 PRx REGISTER WRITES

Writing to the PRx register while the Timer is active, may cause erratic operation.

FIGURE 14-1: TIMER1 BLOCK DIAGRAM



Note 1: Timer1 ADC trigger and interrupt occurs on match plus 1 count; therefore, set the period to PR1 minus 1 to compensate, regardless of the prescaler.

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14.3 Timer1 Control Register

TABLE 14-1: TIMER1 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>		TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0010	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 14-1: T1CON: TYPE A TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit
1 = Timer is enabled
0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when device enters Idle mode
0 = Continue operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit
In Asynchronous Timer mode:
1 = Asynchronous write to TMR1 register in progress
0 = Asynchronous write to TMR1 register complete
In Synchronous Timer mode:
This bit is read as '0'.

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
11 = Reserved
10 = External clock comes from the LPRC
01 = External clock comes from the T1CK pin
00 = External clock comes from the SOSC

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

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REGISTER 14-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit
When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit
1 = External clock is defined by the TECS<1:0> bits
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

NOTES:

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15.0 TIMER2 THROUGH TIMER9

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

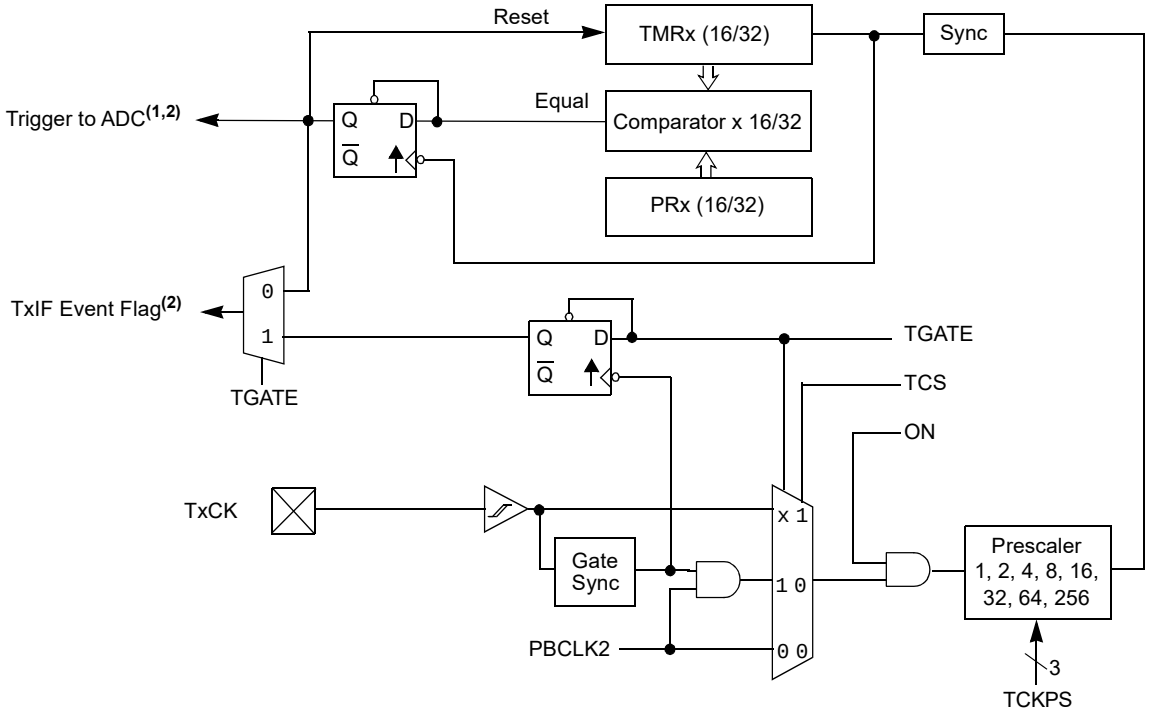
The PIC32MK GP/MC family of devices features eight native synchronous/asynchronous 16/32-bit timers (default 16-bit mode) that can operate as free-running interval timers for various timing applications and counting external events.

15.1 Features

The following are key features of the timers:

- External 16-bit/32-bit Counter Input mode
- Asynchronous external clock with/without selectable prescaler
- Synchronous internal clock with/without selectable prescaler
- External gate control (External pulse width measurement)
- Automatic timer synchronization control
- Operation in Idle mode
- Interrupt on a period register match or falling edge of external gate signal
- Time base for Input Capture and/or Output Compare modules

FIGURE 15-1: TIMER2 THROUGH TIMER9 BLOCK DIAGRAM (16/32-BIT)



Note 1: The ADC event trigger is available on Timer1, Timer3, and Timer5 only.
2: Timer2-Timer9 ADC trigger and interrupt occurs on match plus 1 count; therefore, set the period to PRx minus 1 to compensate, regardless of the prescaler.

15.2 Timer2-Timer9 Control Registers

TABLE 15-1: TIMER2 THROUGH TIMER9 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0210	TMR2	31:16	TMR2<31:16>																0000
		15:0	TMR2<15:0>																0000
0220	PR2	31:16	PR2<31:16>																FFFF
		15:0	PR2<15:0>																FFFF
0400	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0410	TMR3	31:16	TMR3<31:16>																0000
		15:0	TMR3<15:0>																0000
0420	PR3	31:16	PR3<31:16>																FFFF
		15:0	PR3<15:0>																FFFF
0600	T4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0610	TMR4	31:16	TMR4<31:16>																0000
		15:0	TMR4<15:0>																0000
0620	PR4	31:16	PR4<31:16>																FFFF
		15:0	PR4<15:0>																FFFF
0800	T5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0810	TMR5	31:16	TMR5<31:16>																0000
		15:0	TMR5<15:0>																0000
0820	PR5	31:16	PR5<31:16>																FFFF
		15:0	PR5<15:0>																FFFF
0A00	T6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0A10	TMR6	31:16	TMR6<31:16>																0000
		15:0	TMR6<15:0>																0000
0A20	PR6	31:16	PR6<31:16>																FFFF
		15:0	PR6<15:0>																FFFF
0C00	T7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 15-1: TIMER2 THROUGH TIMER9 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C10	TMR7	31:16	TMR7<31:16>																0000
		15:0	TMR7<15:0>																0000
0C20	PR7	31:16	PR7<31:16>																FFFF
		15:0	PR7<15:0>																FFFF
0E00	T8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0E10	TMR8	31:16	TMR8<31:16>																0000
		15:0	TMR8<15:0>																0000
0E20	PR8	31:16	PR8<31:16>																FFFF
		15:0	PR8<15:0>																FFFF
1000	T9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	SYNC	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
1010	TMR9	31:16	TMR9<31:16>																0000
		15:0	TMR9<15:0>																0000
1020	PR9	31:16	PR9<31:16>																FFFF
		15:0	PR9<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 15-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
	ON	—	SIDL	—	—	—	—	SYNC
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE	TCKPS<2:0>			T32	—	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when device enters Idle mode
0 = Continue operation even in Idle mode

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **SYNC:** TMRx Synchronized Timer Start/Stop Enable bit
1 = TMRx synchronized timer start/stop is enabled
0 = TMRx synchronized timer start/stop is disabled

Note: Setting this bit chains all timers whose corresponding SYNC bit is also set such that when the TON bit of all corresponding timers is set, the timers are enabled simultaneously. If any timers in the group are disabled, they are all disabled simultaneously.

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored and is read as '0'.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits
111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timer Mode Select bit
1 = 32-bit Timer mode
0 = 16-bit Timer mode

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

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16.0 DEADMAN TIMER (DMT)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

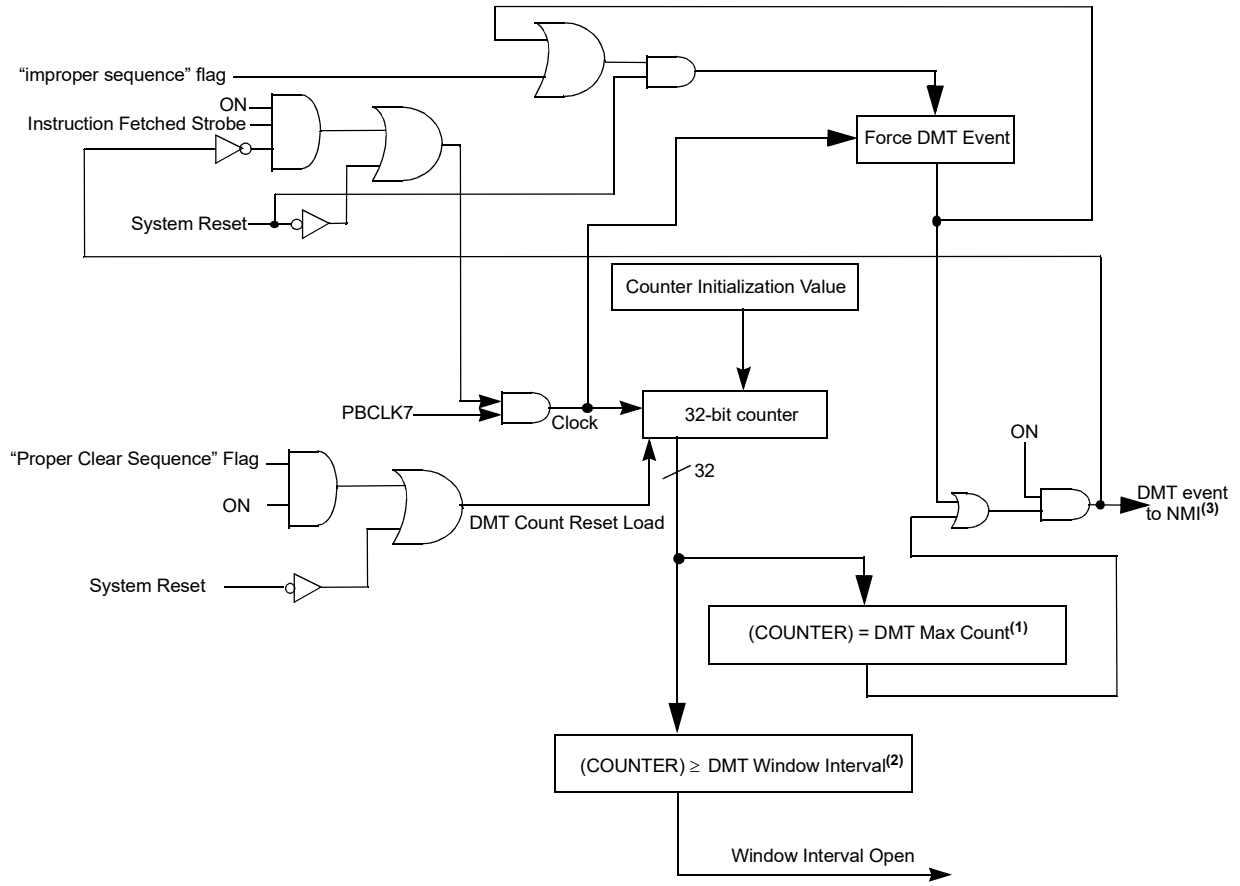
The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

The DMT consists of a 32-bit counter with a time-out count match value as specified by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.

A Deadman Timer is typically used in mission critical and safety critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 16-1 shows a block diagram of the Deadman Timer module.

FIGURE 16-1: DEADMAN TIMER BLOCK DIAGRAM



Note 1: DMT Max Count is controlled by the DMTCNT<3:0> bits in the DEVCFG1 Configuration register.
2: DMT Window Interval is controlled by the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.
3: Refer to **7.0 "Resets"** for more information.

16.1 Deadman Timer Control Registers

TABLE 16-1: DEADMAN TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0E00	DMTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0E10	DMTPRECLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STEP1<7:0>								—	—	—	—	—	—	—	—	0000
0E20	DMCLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STEP2<7:0>								0000
0E30	DMTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
0E40	DMTCNT	31:16	COUNTER<31:0>																0000
		15:0																	0000
0E60	DMTPSCNT	31:16	PSCNT<31:0>																0000
		15:0																	0000
0E70	DMTPSINTV	31:16	PSINTV<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 16-1: DMTCON: DEADMAN TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Deadman Timer Module Enable bit(1)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is disabled

bit 13-0 **Unimplemented:** Read as '0'

Note 1: This bit only has control when the FDMTEN bit (DEVCFG1<3>) = 0.

REGISTER 16-2: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP1<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STEP1<7:0>:** Preclear Enable bits
01000000 = Enables the Deadman Timer Preclear (Step 1)
All other write patterns = Set BAD1 flag.
These bits are cleared when a DMT reset event occurs. STEP1<7:0> is also cleared if the STEP2<7:0> bits are loaded with the correct value in the correct sequence.

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 16-3: DMTCLR: DEADMAN TIMER CLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP2<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **STEP2<7:0>:** Clear Timer bits

00001000 = Clears STEP1<7:0>, STEP2<7:0> and the Deadman Timer if, and only if, preceded by correct loading of STEP1<7:0> bits in the correct sequence. The write to these bits may be verified by reading DMTCNT and observing the counter being reset.

All other write patterns = Set BAD2 bit, the value of STEP1<7:0> will remain unchanged, and the new value being written STEP2<7:0> will be captured. These bits are also cleared when a DMT reset event occurs.

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REGISTER 16-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HC	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R-0
	BAD1	BAD2	DMTEVENT					WINOPN

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Bad STEP1<7:0> Value Detect bit

1 = Incorrect STEP1<7:0> value or out of sequence write to step2<7:0> was detected
0 = Incorrect STEP1<7:0> value was not detected

bit 6 **BAD2:** Bad STEP2<7:0> Value Detect bit

1 = Incorrect STEP2<7:0> value was detected
0 = Incorrect STEP2<7:0> value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit

1 = Deadman timer event was detected (counter expired or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)
0 = Deadman timer even was not detected

Note: This bit is cleared only on a Reset.

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit

1 = Deadman timer clear window is open
0 = Deadman timer clear window is not open

REGISTER 16-5: DMTCNT: DEADMAN TIMER COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **COUNTER<31:0>:** Read current contents of DMT counter

REGISTER 16-6: DMTPSCNT: POST STATUS CONFIGURE DMT COUNT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<15:8>							
7:0	R-0	R-0	R-0	R-y	R-y	R-y	R-y	R-y
	PSCNT<7:0>							

Legend:		y= Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **PSCNT<31:0>:** DMT Instruction Count Value Configuration Status bits
This is always the value of the DMTCNT<4:0> bits in the DEVCFG1 Configuration register.

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REGISTER 16-7: DMTPSINTV: POST STATUS CONFIGURE DMT INTERVAL STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-y	R-y	R-y
	PSINTV<7:0>							

Legend:		y= Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **PSINTV<31:0>:** DMT Window Interval Configuration Status bits
This is always the value of the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.

NOTES:

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17.0 WATCHDOG TIMER (WDT)

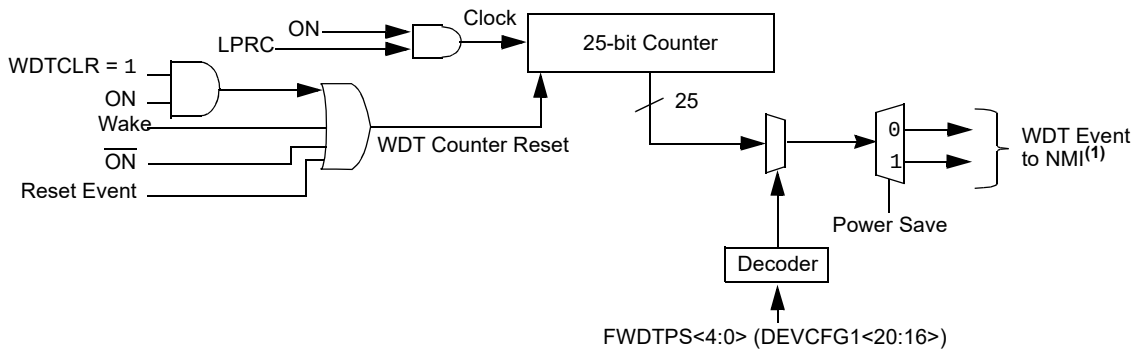
Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

When enabled, the Watchdog Timer (WDT) operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are as follows:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep mode or Idle mode

FIGURE 17-1: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: Refer to **7.0 "Resets"** for more information.

17.1 Watchdog Timer Control Registers

TABLE 17-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C00	WDTCON(1)	31:16	WDTCLRKEY<15:0>																0000
		15:0	ON	—	—	RUNDIV<4:0>					—	—	SLPDIV<4:0>					WDTWINEN	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 17-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	U-0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0
	—	—	SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value 0x5743 to these bits using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The Watchdog Timer module is enabled
0 = The Watchdog Timer module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** Watchdog Timer Postscaler Value in Run Mode bits
In Run mode, these bits are set to the values of the WDTPS<4:0> Configuration bits in the DEVCFG1 register.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-1 **SLPDIV<4:0>:** Watchdog Timer Postscaler Value in Sleep Mode bits
In Sleep mode, these bits are set to the values of the WDTPS <4:0> Configuration bits in the DEVCFG1 register.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

Note 1: This bit only has control when FWDTEN (DEVCFG1<23>) = 0.

NOTES:

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18.0 INPUT CAPTURE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin.

Capture events are caused by the following factors:

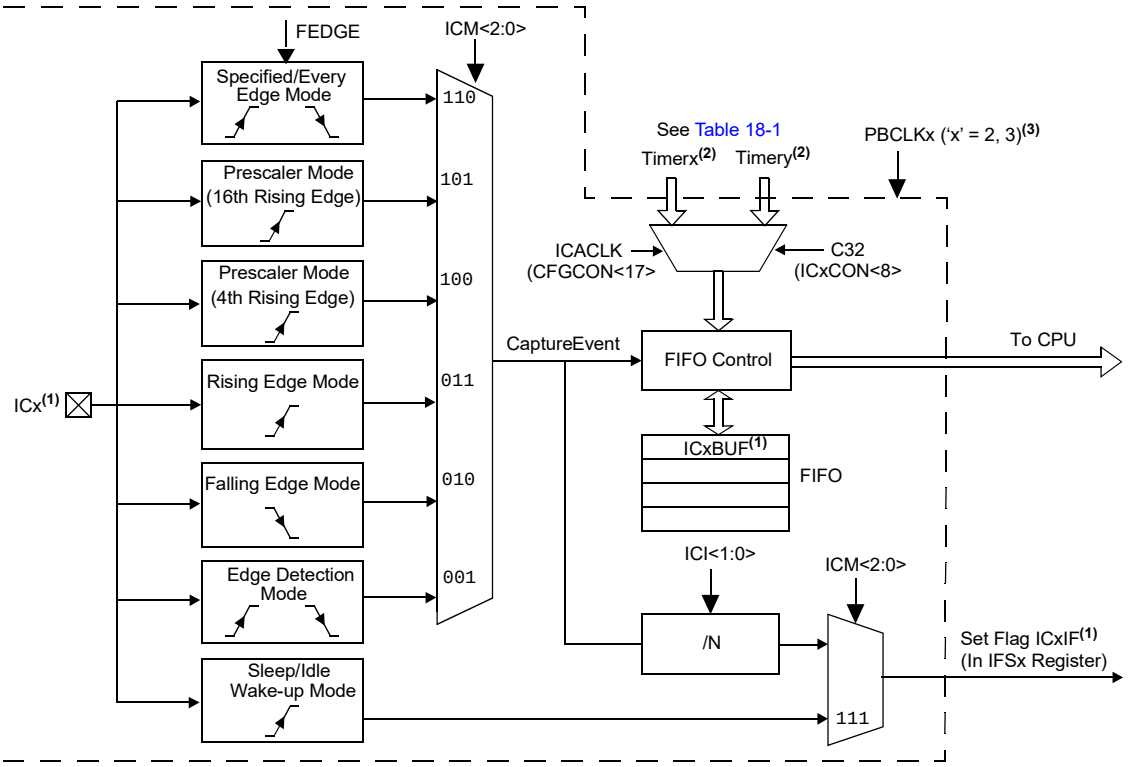
- Capture timer value on every edge (rising and falling), specified edge first
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin
  - Capture every falling edge of input at ICx pin
  - Capture every rising edge of input at ICx pin
  - Capture every 4th rising edge of input at ICx pin
  - Capture every 16th rising edge of input at ICx pin
  - Capture every rising and falling edge of input at ICx pin
  - Capture timer values based on internal or external clocks

Each input capture channel can select between either eight 16-bit time bases or four 32-bit time base. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

FIGURE 18-1: INPUT CAPTURE BLOCK DIAGRAM



Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

2: See Table 18-1 for Timerx and Timery selections.

3: PBCLK2 = Input Capture 1 through Input Capture 9; PBCLK3 = Input Capture 10 through Input Capture 16.

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The timer source for each Input Capture module depends on the setting of the ICACLK bit in the CFGCON register and the C32 bit in the ICxCON register. The available configurations are shown in Table 18-1.

TABLE 18-1: TIMER SOURCE CONFIGURATIONS

ICAPx	CFGCON<ICACLK>	ICxCON<IC32>	ICxCON<ICTMR>	TIMER_x	TIMER_y	ICxBUF CONTENT
ICAP[3-1]	0	0	0	—	0x0000_TMR3 [15:0]	0x0000_TMR3 [15:0]
			1	0x0000_TMR2 [15:0]	—	0x0000_TMR2 [15:0]
	0	1	0	—	TMR2 [31:0]	TMR2 [31:0]
			1	TMR2 [31:0]	---	TMR2 [31:0]
	1	0	0	—	0x0000_TMR5 [15:0]	0x0000_TMR5 [15:0]
			1	0x0000_TMR4 [15:0]	—	0x0000_TMR4 [15:0]
	1	1	0	—	TMR4 [31:0]	TMR4 [31:0]
			1	TMR4 [31:0]	—	TMR4 [31:0]
ICAP[6-4] ICAP[16-13]	0	0	0	—	0x0000_TMR3 [15:0]	0x0000_TMR3 [15:0]
			1	0x0000_TMR2 [15:0]	—	0x0000_TMR2 [15:0]
	0	1	0	—	TMR2 [31:0]	TMR2 [31:0]
			1	TMR2 [31:0]	—	TMR2 [31:0]
	1	0	0	—	0x0000_TMR3 [15:0]	0x0000_TMR3 [15:0]
			1	0x0000_TMR2 [15:0]	—	0x0000_TMR2 [15:0]
	1	1	0	—	TMR2 [31:0]	TMR2 [31:0]
			1	TMR2 [31:0]	—	TMR2 [31:0]
ICAP[9-7]	0	0	0	—	0x0000_TMR3 [15:0]	0x0000_TMR3 [15:0]
			1	0x0000_TMR2 [15:0]	—	0x0000_TMR2 [15:0]
	0	1	0	—	TMR2 [31:0]	TMR2 [31:0]
			1	TMR2 [31:0]	—	TMR2 [31:0]
	1	0	0	—	0x0000_TMR7 [15:0]	0x0000_TMR7 [15:0]
			1	0x0000_TMR6 [15:0]	—	0x0000_TMR6 [15:0]
	1	1	0	—	TMR6 [31:0]	TMR6 [31:0]
			1	TMR6 [31:0]	—	TMR6 [31:0]
ICAP[12-10]	0	0	0	—	0x0000_TMR3 [15:0]	0x0000_TMR3 [15:0]
			1	0x0000_TMR2 [15:0]	—	0x0000_TMR2 [15:0]
	0	1	0	—	TMR2 [31:0]	TMR2 [31:0]
			1	TMR2 [31:0]	—	TMR2 [31:0]
	1	0	0	—	0x0000_TMR9 [15:0]	0x0000_TMR9 [15:0]
			1	0x0000_TMR8 [15:0]	—	0x0000_TMR8 [15:0]
	1	1	0	—	TMR8 [31:0]	TMR8 [31:0]
			1	TMR8 [31:0]	—	TMR8 [31:0]
ICAP[16-13]	0	0	0	—	0x0000_TMR3 [15:0]	0x0000_TMR3 [15:0]
			1	0x0000_TMR2 [15:0]	—	0x0000_TMR2 [15:0]
	0	1	0	—	TMR2 [31:0]	TMR2 [31:0]
			1	TMR2 [31:0]	—	TMR2 [31:0]
	1	0	0	—	0x0000_TMR3 [15:0]	0x0000_TMR3 [15:0]
			1	0x0000_TMR2 [15:0]	—	0x0000_TMR2 [15:0]
	1	1	0	—	TMR2 [31:0]	TMR2 [31:0]
			1	TMR2 [31:0]	—	TMR2 [31:0]

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18.1 Input Capture Control Registers

TABLE 18-2: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 9 REGISTER MAP

Virtual Address BF82_#	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	IC1CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																xxxx
		15:0																	xxxx
2200	IC2CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																xxxx
		15:0																	xxxx
2400	IC3CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																xxxx
		15:0																	xxxx
2600	IC4CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																xxxx
		15:0																	xxxx
2800	IC5CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																xxxx
		15:0																	xxxx
2A00	IC6CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2A10	IC6BUF	31:16	IC6BUF<31:0>																xxxx
		15:0																	xxxx
2C00	IC7CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2C10	IC7BUF	31:16	IC7BUF<31:0>																xxxx
		15:0																	xxxx
2E00	IC8CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2E10	IC8BUF	31:16	IC8BUF<31:0>																xxxx
		15:0																	xxxx
3000	IC9CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3010	IC9BUF	31:16	IC9BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 18-3: INPUT CAPTURE 10 THROUGH INPUT CAPTURE 16 REGISTER MAP

Virtual Address BF84_#	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3200	IC10CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3210	IC10BUF	31:16	IC10BUF<31:0>																xxxx
		15:0																	xxxx
3400	IC11CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3410	IC11BUF	31:16	IC11BUF<31:0>																xxxx
		15:0																	xxxx
3600	IC12CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3610	IC12BUF	31:16	IC12BUF<31:0>																xxxx
		15:0																	xxxx
3800	IC13CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3810	IC13BUF	31:16	IC13BUF<31:0>																xxxx
		15:0																	xxxx
3A00	IC14CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3A10	IC14BUF	31:16	IC14BUF<31:0>																xxxx
		15:0																	xxxx
3C00	IC15CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3C10	IC15BUF	31:16	IC15BUF<31:0>																xxxx
		15:0																	xxxx
3E00	IC16CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3E10	IC16BUF	31:16	IC16BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER ('x' = 1-16)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR(1)	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Bit Value at POR: ('0', '1', x = unknown)	P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit
1 = Module enabled
0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
1 = Halt in CPU Idle mode
0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
1 = Capture rising edge first
0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
1 = 32-bit timer resource capture
0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')(1)
0 = Timery is the counter source for capture
1 = Timerx is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
1 = Input capture buffer is not empty; at least one more capture value can be read
0 = Input capture buffer is empty

Note 1: Refer to Table 18-1 for Timerx and Timery selections.

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ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER ('x' = 1-16) (CONTINUED)

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits

111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
101 = Prescaled Capture Event mode – every sixteenth rising edge
100 = Prescaled Capture Event mode – every fourth rising edge
011 = Simple Capture Event mode – every rising edge
010 = Simple Capture Event mode – every falling edge
001 = Edge Detect mode – every edge (rising and falling)
000 = Input Capture module is disabled

Note 1: Refer to Table 18-1 for Timerx and Timery selections.

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19.0 OUTPUT COMPARE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

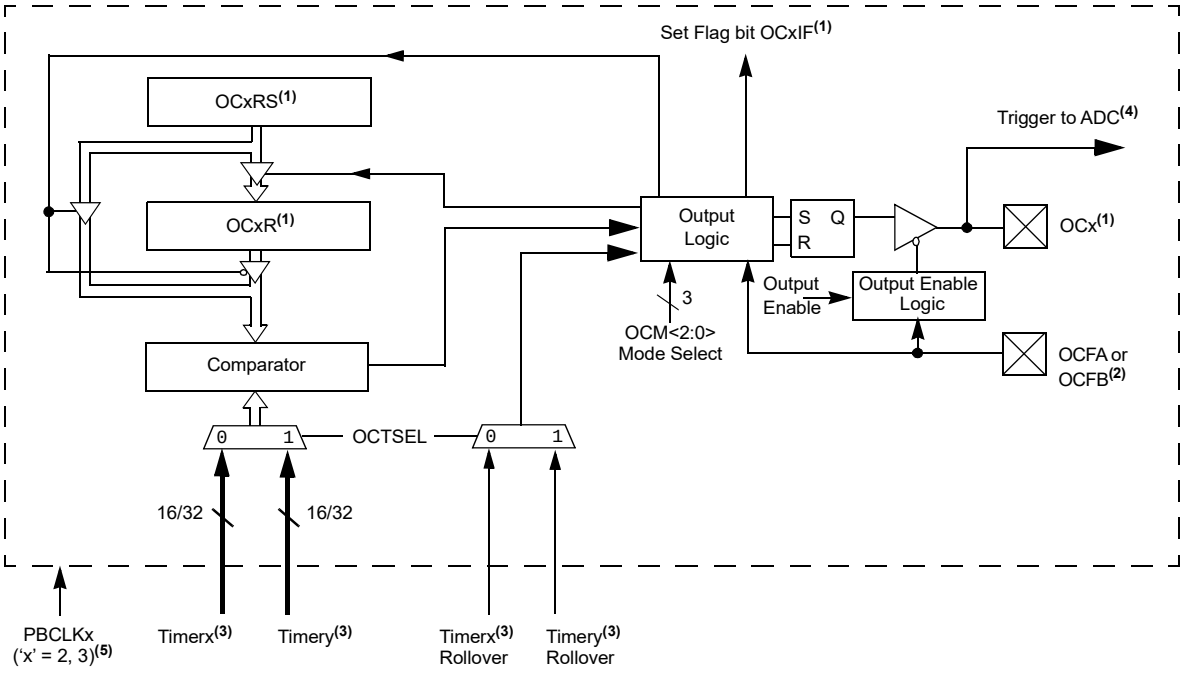
The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events.

For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are some of the key features of the Output Compare:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base
- ADC event trigger for OC1 through OC4

FIGURE 19-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 9.

2: The OCFA pin controls the OCMP1-OCMP3, OCMP7-OCMP9, and OCMP13-OCMP15 channels. The OCFB pin controls the OCMP4-OCMP6, OCMP10-OCMP12, and OCMP16 channels.

3: Refer to Table 19-1 for Timerx and Timery selections.

4: The ADC event trigger is only available on OC1 through OC4.

5: PBCLK2 = Output Compare 1 through Output Compare 9; PBCLK3 = Output Compare 10 through Output Compare 16.

The timer source for each Output Compare module depends on the setting of the OCACLK bit in the CFGCON register, the OC32 bit in the OCxCON register, and the OCTSEL bit in the OCxCON register. The available configurations are shown in Table 19-1.

TABLE 19-1: TIMER SOURCE CONFIGURATIONS

OCx	OCACLK CFGCON<16>	OC32 (OCxCON<5>	OCTSEL OCxCON<3>	Timerx	Timery	Output Compare Timer Source
OC1-OC3	0	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	0	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
	1	0	0	TMR4<15:0>	—	TMR4<15:0>
			1	—	TMR5<15:0>	TMR5<15:0>
	1	1	0	TMR4<31:0>	—	TMR4<31:0>
			1	—	TMR4<31:0>	TMR4<31:0>
OC4-OC6, OC13-OC16	0	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	0	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
	1	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	1	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
OC7-OC9	0	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	0	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
	1	0	0	TMR6<15:0>	—	TMR6<15:0>
			1	—	TMR7<15:0>	TMR7<15:0>
	1	1	0	TMR6<31:0>	—	TMR6<31:0>
			1	—	TMR6<31:0>	TMR6<31:0>
OC10-OC12	0	0	0	TMR2<15:0>	—	TMR2<15:0>
			1	—	TMR3<15:0>	TMR3<15:0>
	0	1	0	TMR2<31:0>	—	TMR2<31:0>
			1	—	TMR2<31:0>	TMR2<31:0>
	1	0	0	TMR8<15:0>	—	TMR8<15:0>
			1	—	TMR9<15:0>	TMR9<15:0>
	1	1	0	TMR8<31:0>	—	TMR8<31:0>
			1	—	TMR8<31:0>	TMR8<31:0>

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19.1 Output Compare Control Registers

TABLE 19-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP

Virtual Address BF82_#	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	OC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4010	OC1R	31:16	OC1R<31:0>																xxxx
		15:0																	xxxx
4020	OC1RS	31:16	OC1RS<31:0>																xxxx
		15:0																	xxxx
4200	OC2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4210	OC2R	31:16	OC2R<31:0>																xxxx
		15:0																	xxxx
4220	OC2RS	31:16	OC2RS<31:0>																xxxx
		15:0																	xxxx
4400	OC3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4410	OC3R	31:16	OC3R<31:0>																xxxx
		15:0																	xxxx
4420	OC3RS	31:16	OC3RS<31:0>																xxxx
		15:0																	xxxx
4600	OC4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4610	OC4R	31:16	OC4R<31:0>																xxxx
		15:0																	xxxx
4620	OC4RS	31:16	OC4RS<31:0>																xxxx
		15:0																	xxxx
4800	OC5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4810	OC5R	31:16	OC5R<31:0>																xxxx
		15:0																	xxxx
4820	OC5RS	31:16	OC5RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 19-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP (CONTINUED)

Virtual Address BF82_#	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4A00	OC6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4A10	OC6R	31:16	OC6R<31:0>																xxxx
		15:0																	xxxx
4A20	OC6RS	31:16	OC6RS<31:0>																xxxx
		15:0																	xxxx
4C00	OC7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4C10	OC7R	31:16	OC7R<31:0>																xxxx
		15:0																	xxxx
4C20	OC7RS	31:16	OC7RS<31:0>																xxxx
		15:0																	xxxx
4E00	OC8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4E10	OC8R	31:16	OC8R<31:0>																xxxx
		15:0																	xxxx
4E20	OC8RS	31:16	OC8RS<31:0>																xxxx
		15:0																	xxxx
5000	OC9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5010	OC9R	31:16	OC9R<31:0>																xxxx
		15:0																	xxxx
5020	OC9RS	31:16 15:0	OC9RS<31:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 19-3: OUTPUT COMPARE 10 THROUGH OUTPUT COMPARE 16 REGISTER MAP

Virtual Address BF84_#	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5200	OC10CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5210	OC10R	31:16	OC10R<31:0>																xxxx
		15:0																	xxxx
5220	OC10RS	31:16	OC10RS<31:0>																xxxx
		15:0																	xxxx
5400	OC11CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5410	OC11R	31:16	OC11R<31:0>																xxxx
		15:0																	xxxx
5420	OC11RS	31:16	OC11RS<31:0>																xxxx
		15:0																	xxxx
5600	OC12CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5610	OC12R	31:16	OC12R<31:0>																xxxx
		15:0																	xxxx
5620	OC12RS	31:16	OC12RS<31:0>																xxxx
		15:0																	xxxx
5800	OC13CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5810	OC13R	31:16	OC13R<31:0>																xxxx
		15:0																	xxxx
5820	OC13RS	31:16	OC13RS<31:0>																xxxx
		15:0																	xxxx
5A00	OC14CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5A10	OC14R	31:16	OC14R<31:0>																xxxx
		15:0																	xxxx
5A20	OC14RS	31:16	OC14RS<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 19-3: OUTPUT COMPARE 10 THROUGH OUTPUT COMPARE 16 REGISTER MAP (CONTINUED)

Virtual Address BF84_#	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5C00	OC15CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5C10	OC15R	31:16	OC15R<31:0>																xxxx
		15:0																	xxxx
5C20	OC15RS	31:16	OC15RS<31:0>																xxxx
		15:0																	xxxx
5E00	OC16CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5E10	OC16R	31:16	OC16R<31:0>																xxxx
		15:0																	xxxx
5E20	OC16RS	31:16 15:0	OC16RS<31:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 19-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER ('x' = 1-16)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT(1)	OCTSEL(2)	OCM<2:0>		

Legend:	HS = Set in hardware	HC = Cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit
- 1 = Output Compare peripheral is enabled
- 0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when CPU enters Idle mode
- 0 = Continue operation in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(1)
- 1 = PWM Fault condition has occurred (cleared in HW only)
- 0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit(2)
- 1 = Timery is the clock source for this Output Compare module
- 0 = Timerx is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

Note 1: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

2: Refer to Table 19-1 for Timerx and Timery selections.

NOTES:

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20.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

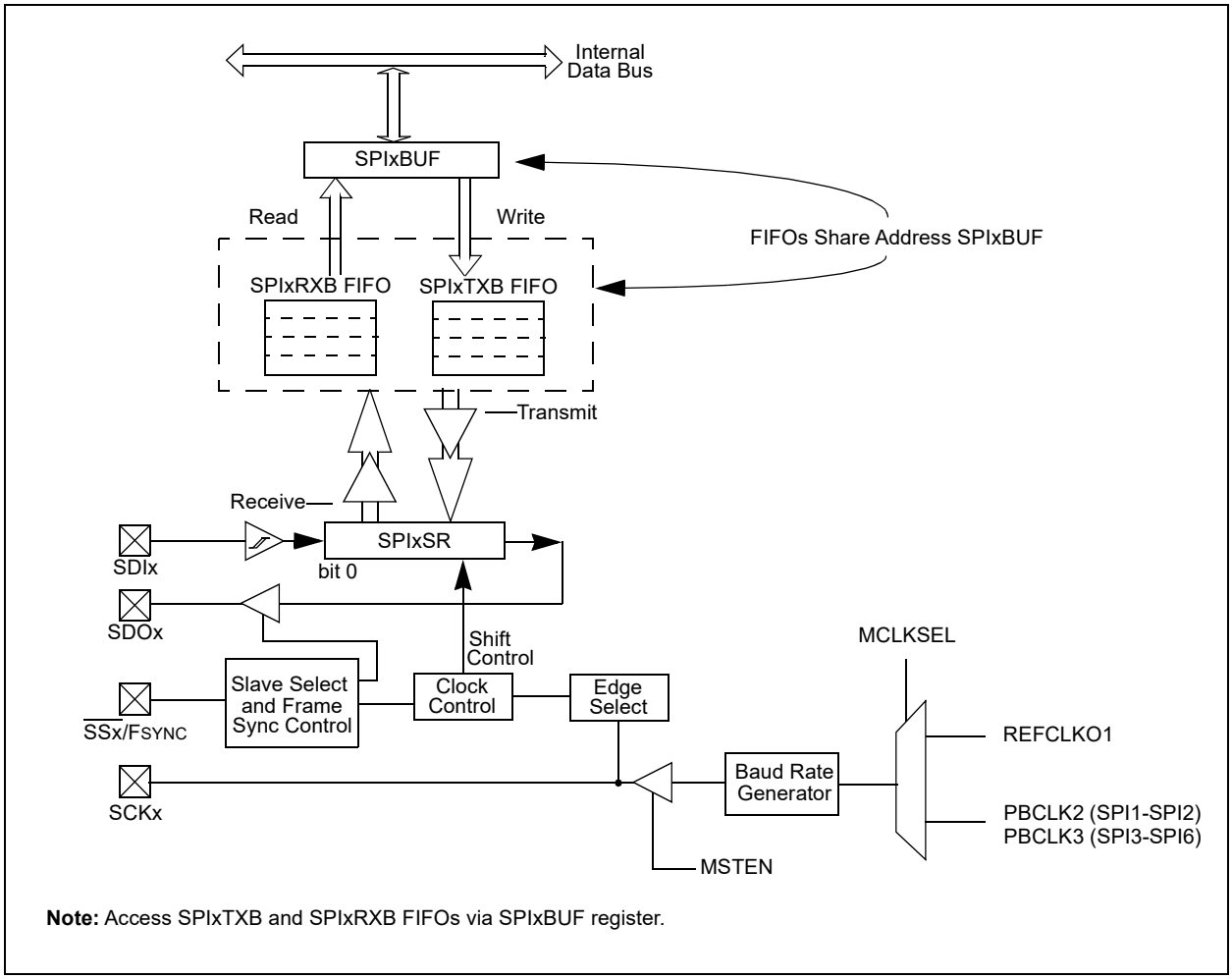
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, analog-to-digital converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

The following are some of the key features of the SPI module:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 32/24/16/8-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/24/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio codec support:
  - I^2S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 20-1: SPI/I^2S MODULE BLOCK DIAGRAM



Note: Access SPIxTXB and SPIxRXB FIFOs via SPIxBUF register.

20.1 SPI Control Registers

TABLE 20-1: SPI1 AND SPI2 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
7010	SPI1STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
7020	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
7030	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
7040	SPI1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00
7200	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
7210	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
7220	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
7230	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
7240	SPI2CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 20-2: SPI3 THROUGH SPI6 REGISTER MAP

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7400	SPI3CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
7410	SPI3STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
7420	SPI3BUF	31:16	DATA<31:0>																0000
		15:0																	0000
7430	SPI3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
7440	SPI3CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00
7600	SPI4CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
7610	SPI4STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
7620	SPI4BUF	31:16	DATA<31:0>																0000
		15:0																	0000
7630	SPI4BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
7640	SPI4CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00
7800	SPI5CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
7810	SPI5STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
7820	SPI5BUF	31:16	DATA<31:0>																0000
		15:0																	0000
7830	SPI5BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
7840	SPI5CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 20-2: SPI3 THROUGH SPI6 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7A00	SPI6CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
7A10	SPI6STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
7A20	SPI6BUF	31:16	DATA<31:0>																0000
		15:0																	0000
7A30	SPI6BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
7A40	SPI6CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMOD<1:0>		0C00

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 20-1: SPIxCON: SPI CONTROL REGISTER (x=1-6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL(1)	—	—	—	—	—	SPIFE	ENHBUF(1)
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	DISSDO(4)	MODE32	MODE16	SMP	CKE(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP(3)	MSTEN	DISSDI(4)	STXISEL<1:0>		SRXISEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The $\overline{SS}$ pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.

bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits
Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
111 = Reserved
110 = Reserved
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character

bit 23 **MCLKSEL:** Master Clock Enable bit(1)
1 = REFCLKO1 is used by the Baud Rate Generator
0 = PBCLK2 is used by the Baud Rate Generator for SPI1 and SPI2 or PBCLK3 if SPI3 through SPI6

bit 22-18 **Unimplemented:** Read as '0'

Note 1: This bit can only be written when the ON bit = 0. Refer to **36.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **13.3 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 20-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)(x=1-6)

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(1)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPI/I2S Module On bit
1 = SPI/I2S module is enabled
0 = SPI/I2S module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **DISSDO:** Disable SDOx pin bit(4)
1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
1	0	32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame
0	1	16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame
0	0	16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPI Clock Edge Select bit(2)
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = $\overline{SSx}$ pin used for Slave mode
0 = $\overline{SSx}$ pin not used for Slave mode, pin controlled by port function.

bit 6 **CKP:** Clock Polarity Select bit(3)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

Note 1: This bit can only be written when the ON bit = 0. Refer to **36.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **13.3 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 20-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)(x=1-6)

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDI bit(4)
1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
0 = SDI pin is controlled by the SPI module

bit 3-2 **STXISEL<1:0>:** SPI Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPI Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

Note 1: This bit can only be written when the ON bit = 0. Refer to **36.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **13.3 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 20-2: SPIxCON2: SPI CONTROL REGISTER 2 (x=1-6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN(1)	—	—	—	AUDMONO(1,2)	—	AUDMOD<1:0>(1,2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit
1 = Data from RX FIFO is sign extended
0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
1 = Frame Error overflow generates error events
0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
1 = Receive overflow generates error events
0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
1 = Transmit Underrun Generates Error Events
0 = Transmit Underrun Does Not Generates Error Events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
0 = A ROV is a critical error which stop SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
0 = A TUR is a critical error which stop SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit(1)
1 = Audio protocol enabled
0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
1 = Audio data is mono (Each data word is transmitted on both left and right channels)
0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit(1,2)
11 = PCM/DSP mode
10 = Right Justified mode
01 = Left Justified mode
00 = I^2S mode

Note 1: This bit can only be written when the ON bit = 0.
2: This bit is only valid for AUDEN = 1.

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REGISTER 20-3: SPIxSTAT: SPI STATUS REGISTER (x=1-6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0, HS, HC	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0, HS, HC	R/C-0, HS	R-1, HS, HC	U-0	R-1, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	HC = Cleared in hardware	HS = Set in hardware	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **FRMERR:** SPI Frame Error status bit
1 = Frame error detected
0 = No Frame error detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

REGISTER 20-3: SPIxSTAT: SPI STATUS REGISTER (CONTINUED)(x=1-6)

bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit
1 = Transmit not yet started, SPITXB is full
0 = Transmit buffer is not full
Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.
Enhanced Buffer Mode:
Set when CWPTR + 1 = SRPTR; cleared otherwise

bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB is full
0 = Receive buffer, SPIxRXB is not full
Standard Buffer Mode:
Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer Mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise

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REGISTER 20-4: SPIxBUF: SPIx BUFFER REGISTER ('x' = 1-6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>** FIFO Data bits
When MODE32 or MODE16 selects 32-bit data, the SPI uses DATA<31:0>.
When MODE32 or MODE16 selects 24-bit data, the SPI only uses DATA<24:0>.
When MODE32 or MODE16 selects 16-bit data, the SPI only uses DATA<15:0>.
When MODE32 or MODE16 selects 8-bit data, the SPI only uses DATA<7:0>.

REGISTER 20-5: SPIxBRG: SPIx BAUD RATE GENERATOR REGISTER ('x' = 1-6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	BRG<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BRG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **BRG<12:0>** Baud Rate Generator Divisor bits
Baud Rate = FPBCLKx / (2 * (SPIxBRG + 1)), where x = 2 and 3, (FPBCLK2 for SPI1-SPI2, FPBCLK3 for SPI3-SPI6.) Therefore, the maximum baud rate possible is FPBCLKx / 2 (SPIXBRG = 0) and the minimum baud rate possible is FPBCLKx / 16384.

Note: Changing the BRG value when the ON bit is equal to '1' causes undefined behavior.

NOTES:

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21.0 INTER-INTEGRATED CIRCUIT (I^2C)

The I^2C software library is available in MPLAB Harmony. If the user application is to implement I^2C, for future device pin compatibility, it is recommended to assign software I^2C functions according to the details provided in the device pin tables (Table 3 through Table 6):

- For 64-pin packages, refer to Notes 6 and 7 in Table 3 and Table 4.
- For 100-lead packages, refer to Notes 5 and 6 in Table 5 and Table 6.

21.1 Software I^2C Performance

Table 21-1 provides the performance details of the I^2C.

TABLE 21-1: I^2C PERFORMANCE

I^2C Baud Rate	I^2C Transactions/ Second	I^2C CPU Utilization
400 kHz	22070 (continuous)	50.76%
	16841	38.73%
	4079	9.38%
	429	0.99%
100 kHz	5581 (continuous)	12.84%
	4077	9.38%
	429	0.99%

NOTES:

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22.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

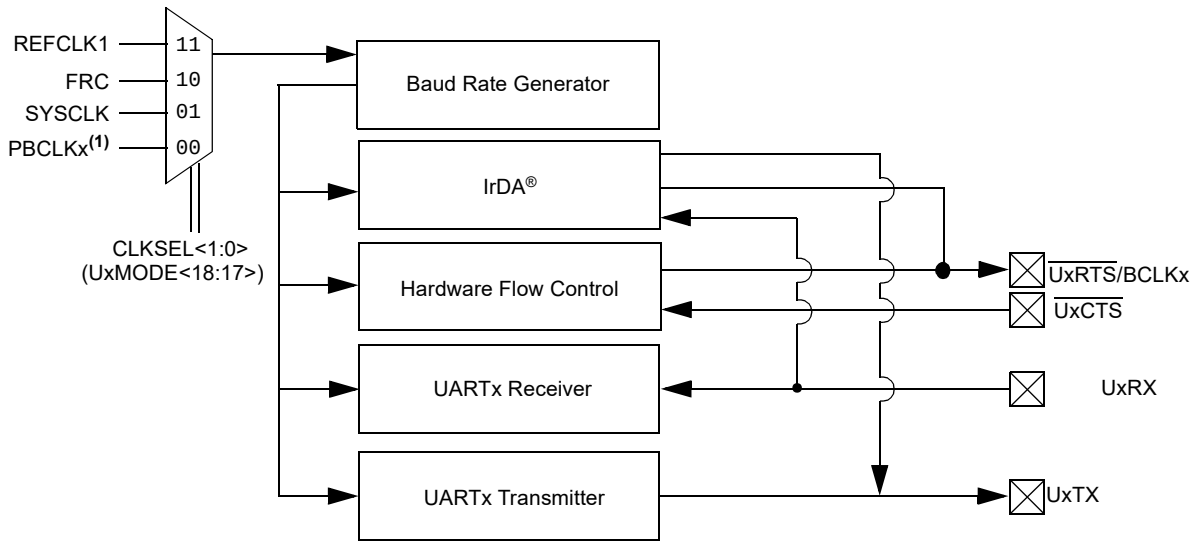
The UART module is one of the serial I/O modules available in PIC32MK GP/MC family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The following are key features of the UART module:

- Ability to receive data during Sleep mode
- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Auto-baud support
- Four clock source inputs for asynchronous clocking
- Transmit and Receive (TX/RX) polarity control
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates up to 30 Mbps
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 22-1 illustrates a simplified block diagram of the UART module.

FIGURE 22-1: UART SIMPLIFIED BLOCK DIAGRAM



Note 1: 'x' = 2 for UART1 and UART2; 'x' = 3 for UART3 through UART6.

22.1 UART Control Registers

TABLE 22-1: UART1 AND UART2 REGISTER MAP

Virtual Address BF82_#	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8000	U1MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	CKRDY	—	—	—	CLKSEL<1:0>		RUNOV	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
8010	U1STA(1)	31:16	ADDRMSK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
8020	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
8030	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
8040	U1BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	U1BRG<19:16>				0000
		15:0	U1BRG<15:0>																0000
8200	U2MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	CKRDY	—	—	—	CLKSEL<1:0>		RUNOV	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
8210	U2STA(1)	31:16	ADDRMSK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
8220	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
8230	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
8240	U2BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BRG<19:16>				0000
		15:0	BRG<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 22-2: UART3 THROUGH UART6 REGISTER MAP

Virtual Address BF84_#	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8400	U3MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	CKRDY	—	—	—	CLKSEL<1:0>		RUNOV	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
8410	U3STA(1)	31:16	ADDRMSK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
8420	U3TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
8430	U3RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
8440	U3BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BRG<19:16>				0000
		15:0	BRG<15:0>																0000
8600	U4MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	CKRDY	—	—	—	CLKSEL<1:0>		RUNOV	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
8610	U4STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
8620	U4TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
8630	U4RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
8640	U4BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BRG<19:16>				0000
		15:0	BRG<15:0>																0000
8800	U5MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	CKRDY	—	—	—	CLKSEL<1:0>		RUNOV	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
8810	U5STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
8820	U5TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
8830	U5RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
8840	U5BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BRG<19:16>				0000
		15:0	BRG<15:0>																0000
8A00	U6MODE(1)	31:16	—	—	—	—	—	—	—	—	SLPEN	CKRDY	—	—	—	CLKSEL<1:0>		RUNOV	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
8A10	U6STA(1)	31:16	MASK<7:0>								ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 22-2: UART3 THROUGH UART6 REGISTER MAP (CONTINUED)

Virtual Address BF84_#	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8A20	U6TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
8A30	U6RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
8A40	U6BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	BRG<19:16>				0000
		15:0	BRG<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 22-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R-0, HS, HC	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	SLPEN	CLKRDY	—	—	—	CLKSEL<1:0>(1)		RUNOV
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>(2)	
7:0	R-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:	HS = Set by hardware	HC = cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **SLPEN:** Run During Sleep Enable bit
- 1 = BRG clock runs during Sleep mode
- 0 = BRG clock is turned off during Sleep mode

Note: SLPEN = 1 only applies if CLKSEL = FRC, or in some cases, REFCLK depending on the selected REFCLK input source if running while in Sleep mode. All clocks, as well as the UART are disabled in Deep Sleep mode.

bit 22 **CLKRDY:** USART Clock Status bit
- 1 = UART clock is ready (User software *should not* update the UxMODE register)
- 0 = UART clock is not ready (User software *can* update the UxMODE register)

bit 21-19 **Unimplemented:** Read as '0'

bit 18-17 **CLKSEL<1:0>:** UART Baud Rate Generator Clock Selection bits(1)
- 11 = BRG clock is REFCLK1
- 10 = BRG clock is FRC
- 01 = BRG clock is SYSCLK (off in Sleep mode)
- 00 = BRG clock is PBCLKx (off in Sleep mode)

bit 16 **RUNOV:** Run During Overflow Mode bit
- 1 = Shift register continues to run when Overflow (OERR) condition is detected
- 0 = Shift register stops accepting new data when Overflow (OERR) condition is detected

bit 15 **ON:** UARTx Enable bit
- 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits
- 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation in Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

Note 1: These bits can be changed only when the ON bit (UxMODE<15>) is set to '0'.

2: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **13.3 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 22-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits(2)
11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
1 = Wake-up is enabled
0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Loopback mode is enabled
0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Note 1: These bits can be changed only when the ON bit (UxMODE<15>) is set to '0'.
2: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices (see **13.3 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 22-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MASK<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN(1)	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0, HS	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

Legend:	HS = Set by hardware	HC = cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **MASK<7:0>:** Address Match Mask bits

These bits are used to mask the ADDR<7:0> bits.

11111111 = Corresponding matching ADDR<7:0> bits are used to detect the address match

Note: This setting allows the user to assign individual address as well as a group broadcast address to a UART.

00000000 = Corresponding ADDRx bits are not used to detect the address match.

See **22.2 "UART Broadcast Mode Example"** for additional information.

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

1 = Corresponding MASKx bits are used to detect the address match.

Note: This setting allows the user to assign individual address as well as a group broadcast address to a UART.

0 = Corresponding MASKx bits are not used to detect the address match.

See **22.2 "UART Broadcast Mode Example"** for additional information.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits

11 = Reserved, do not use
10 = Interrupt is generated and asserted while the transmit buffer is empty
01 = Interrupt is generated and asserted when all characters have been transmitted
00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):
1 = UxTX Idle state is '0'
0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):
1 = IrDA encoded UxTX Idle state is '1'
0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** Receiver Enable bit

1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON bit (UxMODE<15>) = 1)
0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module and released to the PORT

Note: The event of disabling an enabled receiver will release the RX pin to the PORT function; however, the receive buffers will not be reset. Disabling the receiver has no effect on the receive status flags.

Note 1: This bit should not be enabled until after the ON bit (UxMODE<15>) = 1. If TX interrupts are enabled, setting this bit will immediately cause a TX interrupt based on the value of the UTXISEL bit.

REGISTER 22-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 11 **UTXBRK:** Transmit Break bit
1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
0 = Break transmission is disabled or completed

bit 10 **UTXEN:** Transmit Enable bit(1)
1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON bit (UxMODE<15>) = 1)
0 = UARTx transmitter is disabled
The event of disabling an enabled transmitter will release the TX pin to the PORT function and reset the transmit buffers to empty. Any pending transmission is aborted and data characters in the transmit buffers are lost. All transmit status flags are cleared and the TRMT bit is set.

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
1 = Transmit buffer is full
0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
When RUNOV = 0, clearing a previously set OERR bit will clear and reset the receive buffer and shift register.
When RUNOV = 1, Clearing a previously set OERR bit will not reset the receive buffer and shift register
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: This bit should not be enabled until after the ON bit (UxMODE<15>) = 1. If TX interrupts are enabled, setting this bit will immediately cause a TX interrupt based on the value of the UTXISEL bit.

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REGISTER 22-3: UxRXREG: UARTx RECEIVE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	RX<8>
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RX<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8 **RX<8>:** Data bit 8 of the received character (in 9-bit mode)

bit 7-0 **RX<7:0>:** Data bits 7-0 of the received character

REGISTER 22-4: UxTXREG: UARTx TRANSMIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-x	U-x	U-x	U-x	U-x	U-x	U-x	U-x
	—	—	—	—	—	—	—	—
23:16	U-x	U-x	U-x	U-x	U-x	U-x	U-x	U-x
	—	—	—	—	—	—	—	—
15:8	U-x	U-x	U-x	U-x	U-x	U-x	U-x	W-x
	—	—	—	—	—	—	—	TX<8>
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	TX<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as initialized data

bit 8 **TX<8>:** Data bit 8 of the transmitted character (in 9-bit mode)

bit 7-0 **TX<7:0>:** Data bits 7-0 of the transmitted character

REGISTER 22-5: UxBRG: UARTx BAUD RATE GENERATOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	BRG<19:16>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BRG<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BRG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-0 **BRG<19:0>:** Baud Rate Generator Divisor bits

Note: The UxBRG register cannot be changed while UARTx is enabled (ON bit (UxMODE<15>) = 1)).

TABLE 22-3: UART BAUD RATE CALCULATIONS

UART Baud Rate With	UxBRG Equals
BRGH = 0	UxBRG = ((CLKSEL Frequency / (16 * Desired Baud Rate)) – 1)
BRGH = 1	UxBRG = ((CLKSEL Frequency / (4 * Desired Baud Rate)) – 1)

Note: UART1 and UART2 on PBCLK2; UART3 through UART6 on PBCLK3.

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22.2 UART Broadcast Mode Example

As shown in Table 22-4, the group hardware address identifier bit was arbitrarily chosen as bit 7 with bit 4 chosen as the software group or individual UART target ID. Therefore, the collective group address assigned for all UARTs (i.e, [w, x, y, z]) is ‘0b100100xx, while the individual addresses are ‘0b10000000 through ‘0b10000011, respectively.

Any MASK register bit = 0 means the corresponding ADDR<7:0> bit is a “don't care” from a hardware address matching point of view. Using this scheme, multiple UART subnet groups could be created within a network. If not using address match with a broadcast mode, set the ADDRMSK<7:0> bits (UxSTAT<31:24) = 0x00, which is the default.

To send a broadcast message to all UARTs in the group identified by bit 7 = 1, send UxTXREG = (0x190), address bit 9 set. All the UARTs in that group, bit 7 = 1, would generate an interrupt for an address match because of the bit <7:5>,<3:2> match, Logic AND of MASK and ADDR registers equal “true”. User software would check if bit 4 = 1, and if true, the RX<7:0> bits register value is valid for all UARTS.

To send a specific message to UARTy within the group, the user would send UxTXREG = (0x182), address bit 9 set. All of the UARTs in that group identified with bit 7 = 1 would still generate an interrupt for an address match because of the bit <7:5>,<3:2> address match, Logic AND of MASK and ADDR registers equal True. In this case, user software would check if bit 4 = 0, and if true, the RX<7:0> bits register value would be intended only for UARTy, with all others ignored.

TABLE 22-4: PDSEL<1:0> (UxMODE<2:1>) = ‘0b11 AND ADM_EN (UxSTA<24>) = 1

Networked UARTS	Register Bit	7	6	5	4	3	2	1	0	Individual/ Group Addresses
UARTx	ADDRMSK	1	1	1	0	1	1	0	0	0xBC
UARTw	ADDR	1	0	0	1 = Group 0 = Individual	0	0	0	0	0x80/0x9X
UARTx	ADDR	1	0	0	1 = Group 0 = Individual	0	0	0	1	0x81/0x9X
UARTy	ADDR	1	0	0	1 = Group 0 = Individual	0	0	1	0	0x82/0x9X
UARTz	ADDR	1	0	0	1 = Group 0 = Individual	0	0	1	1	0x83/0x9X

22.3 Module Operation

22.3.1 INITIALIZATION

Clearing the ON bit (i.e, = 0), which disables the UART module, will do the following:

- Aborts all pending transmissions and receptions and resets the module, as follows:
  - Reset the RX/TX buffers/FIFO to empty states (any data characters in the buffers are lost)
  - Resets the baud rate counter (UxBRG is not affected, only the counter)
  - Resets all error and status flags: URXDA, OERR, FERR, PERR, UTXBRK, UTXBF are cleared and RIDLE, TRMT are set
- Stop clocks to the entire module with the exception of the SFRs, saving power
- Surrenders control of the module I/O pins

Note:	Once the ON bit is set, it should not be cleared until the CLKRDY bit is read to be a logic '1'. This allows proper synchronization of the status and output signals. Otherwise, glitches in the status signals or BRG clock can occur.

Setting the ON bit (i.e., = 1), which enables the UART module, will do the following:

- The UART module controls the I/O pins as defined by the UEN bits, overriding the port TRIS and LATCH register bit settings
- UxTX is forced as an output driving the idle state defined by the UTXINV bit, when no transmissions are taking place
- UxRX is configured as an input
- If CTS and RTS are enabled, CTS is forced as an input and the RTS/BCLK pin functions as RTS output
- If BCLK is enabled, the RTS/BCLK output drives the 16x baud clock output

Note:	The ON bit should not be set (i.e., = 1) unless the CLKRDY bit is read to be a logic '0'.

22.4 Serial Protocols Usage

22.4.1 DATA TERMINAL EQUIPMENT (DTE) WITH FLOW CONTROL

When connecting to the DTE (typically a PC) and flow control is desired, set the UEN bit = 10 to enable CTS and RTS, and set the RTSMD bit = 0.

22.4.2 IEEE-485

To use the UART module in the IEEE-485 protocol, use the address detection feature to detect message frames. Normally, set the UEN bit = '01' to drive the RTS pin and control the bus driver, and set the RTSMD bit = 1.

22.4.3 LIN BUS

To transmit on a LIN bus, the transmitter must send a frame in 8,N,1 format consisting of a break, a synchronization character (0x55), and the message body. The module has extensive support for the LIN protocol including bus wake-up for a slave node as well as auto-baud detection and BREAK character transmit for master nodes. When in LIN mode, the software should program the BRGH bit = 0, which insures a 16x baud clock is used with majority detect.

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22.5 Transmit and Receive Timing

Figure 22-2 and Figure 22-3 illustrate typical receive and transmit timing for the UART module.

FIGURE 22-2: UART RECEPTION

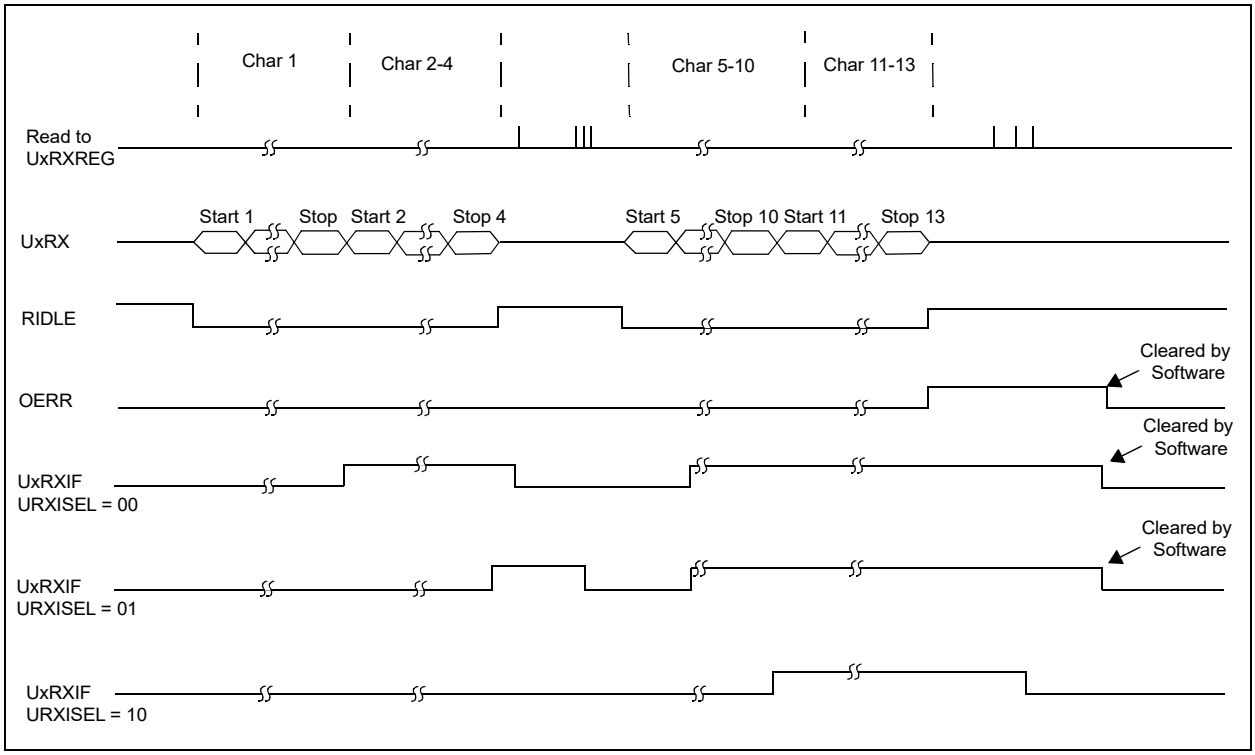
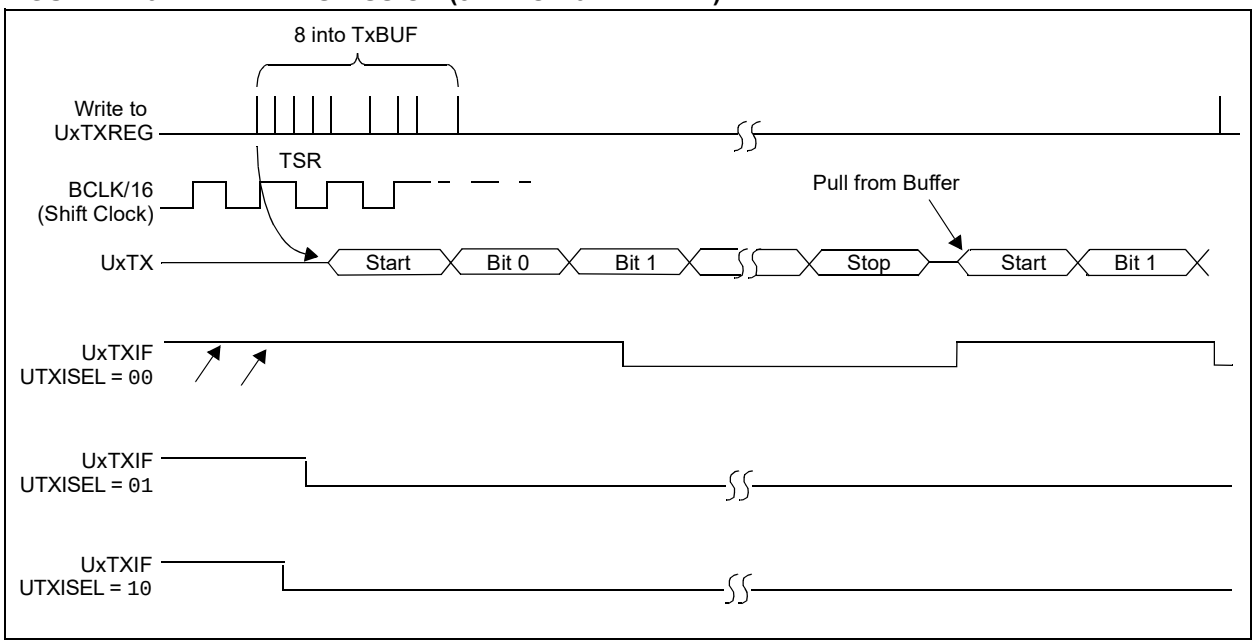


FIGURE 22-3: TRANSMISSION (8-BIT OR 9-BIT DATA)



NOTES:

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23.0 PARALLEL MASTER PORT (PMP)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable.

The following are key features of the PMP module:

- 8-bit or 16-bit data interface
- 14/22 address lines with two Chip Selects
- 15/23 address lines with one Chip Select
- 16/24 address lines without Chip Select
- Address auto-increment/auto-decrement
- Selectable address bus width for resource limited I/O
- Individual read and write strobes or read/write strobe with enable strobe
- Partially multiplexed address/data mode (eight bits of address) with an address latch strobe
- Fully multiplexed address/data mode (16 bits of address) with address latch high and low strobes
- Programmable wait states
- Programmable polarity on selected control signals
- Interrupt on cycle end, busy flag for polling
- Persistent Interrupt capability for DMA access
- Little and Big-Endian Compatible addressing styles
- Extended address mode with addresses up to 24 bits
- Dual (4) word buffer mode with separate read and write registers.
- Operate during CPU Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers
- Freeze option for in-circuit debugging

Note: On 64-pin devices, data pins PMD<15:8> and PMA<23:16> are not available.

TABLE 23-1: PMP SUPPORTED CONFIGURATIONS

Pins	Alternate PMP Pin Functions	100-pin Devices	64-pin Devices
PMD<7:0>	Multiplexed PMA<7:0> and PMA<15:8>	X	X
PMD<15:8>	Multiplexed PMA<7:0> and PMA<15:8>	X	—
PMA<0>	PMALL	X	X
PMA<1>	PMALH	X	X
PMA<13:2>	—	X	X
PMA<14>	PMCS1 or PMCS	X	X
PMA<15>	PMCS2	X	X
PMA<21:16>	—	X	—
PMA<22>	PMCS1A	X	—
PMA<23>	PMCS2A	X	—
PMRD	PMWR	X	X
PMWR	PMENB	X	X

ADRMUX<1:0> bits:

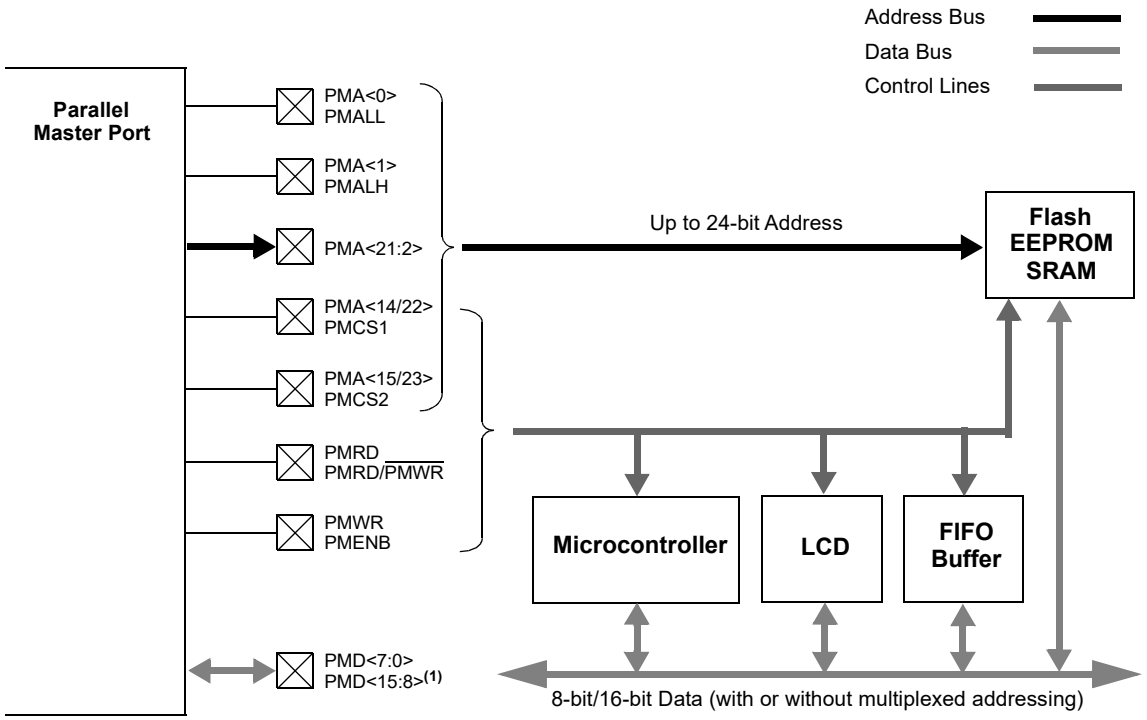
11 = All 16 bits of address are multiplexed with the 16 bits of data (PMA<15:0>/PMD<15:0>) using two phases.

10 = All 16 bits of address are multiplexed with the lower 8 bits of data (PMA<15:8>/PMA<7:0>/PMD<7:0>) using three phases

01 = Lower 8 bits of address are multiplexed with lower 8 bits of data (PMA<7:0>/PMD<7:0>)

00 = Address and data pins are not multiplexed

FIGURE 23-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



Note: On 64-pin devices, data pins PMD<15:8> and PMA<23:16> are not available.

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23.1 Control Registers

TABLE 23-2: PARALLEL MASTER PORT REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
E000	PMCON	31:16	—	—	—	—	—	—	—	—	RDSTART	—	—	—	—	—	DUALBUF	EXADR	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
E010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
E020	PMADDR	31:16	—	—	—	—	—	—	—	—	PMCS2A	PMCS1A	ADDR<21:16>						0000
			—	—	—	—	—	—	—	—	ADDR23	ADDR22	—	—	—	—	—	—	0000
		15:0	CS2	CS1	ADDR<13:0>														0000
			ADDR15	ADDR14															0000
E030	PMDOUT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAOUT<15:0>																0000
E040	PMDIN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAIN<15:0>																0000
E050	PMAEN	31:16	—	—	—	—	—	—	—	—	PTEN<23:16>								0000
		15:0	PTEN<15:0>																0000
E060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F
E070	PMWADDR	31:16	—	—	—	—	—	—	—	—	WCS2A	WCS1A	WADDR<21:16>						0000
			—	—	—	—	—	—	—	—	WADDR23	WADDR22	—	—	—	—	—	—	0000
		15:0	WCS2	WCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			WADDR15	WADDR14	WADDR<13:0>														0000
E080	PMRADDR	31:16	—	—	—	—	—	—	—	—	RCS2A	RCS1A	RADDR<21:16>						0000
			—	—	—	—	—	—	—	—	RADDR23	RADDR22							0000
		15:0	RCS2	RCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			RADDR15	RADDR14	RADDR<13:0>														0000
E090	PMRDIN	31:16	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	15:0	RDATAIN<15:0>															0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DUALBUF	EXADR
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(2)		ALP(2)	CS2P(2)	CS1P(2)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start Read Cycle on PMP Bus bit
- 1 = Start a ready cycle on the PMP bus
- 0 = No effect

Note: This bit is cleared by hardware at the end of the read cycle when the BUSY bit (PMMODE<15>) is equal to '0'.

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Parallel Master Port Dual Read/Write Buffer Enable bit

This bit is only valid in Master mode.
- 1 = PMP uses separate registers for reads and writes
  Reads: PMRADDR and PMRDIN
  Writes: PMRWADDR and PMDOUT
- 0 = PMP uses legacy registers for reads and writes
  Reads/Writes: PMADDR and PMRDIN

bit 16 **EXADR:** Parallel Master Port Extended 24-bit Addressing bit (Master mode only)
- 1 = PMP 24-bit addressing is enabled
- 0 = PMP 24-bit addressing is disabled

bit 15 **ON:** Parallel Master Port Enable bit(1)
- 1 = PMP is enabled
- 0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

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REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
- 11 = All 16-bit of address are multiplexed with the 16-bits of data (PMA<15:0> or PMD<15:0>) using two phases
- 10 = All 16-bit of address are multiplexed with the lower 8-bits of data (PMA<15:8>, PMA<7:0>, or PMD<7:0>) using three phases
- 01 = Lower 8-bits of address are multiplexed with lower 8-bits of data (PMA<7:0> or PMD<7:0>)
- 00 = Address and data pins are not multiplexed

Note: The ADRMUX bits are independent of the MODE16 bit. Therefore, if ADDRMUX = 11 and MODE16 = 0, only the lower 8 bits of the address will be driven out. Additionally, if ADDRMUX = 10 and MODE16 = 1, the upper 8 bits of the data will be driven out on PMD<15:8>.

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
- 1 = PMWR/PMENB port is enabled
- 0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
- 1 = PMRD/PMWR port is enabled
- 0 = PMRD/PMWR port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
- 11 = Reserved
- 10 = PMCS2/(a) and PMCS1/(a) used as Chip Select
- 01 = PMCS2/(a) used as Chip Select, PMCS1/(a) used as address bit 14 or (22 when EXADR = 1)
- 00 = PMCS2/(a) and PMCS1/(a) used as address bits (15 and 14) or (23 and 22 when EXADR = 1)

Note: When the CSx bit is used as an address, it is subject to auto-increment/decrement.

bit 5 **ALP:** Address Latch Polarity bit(2)
- 1 = Active-high (PMCS2) / (PMPCS2a)
- 0 = Active-low (PMCS2) / (PMPCS2a)

Note: When the PMCS2/(a) pin is used as an address pin, the setting of the CS2P bit does not affect the polarity.

bit 4 **CS2P:** Chip Select 1 Polarity bit(2)
- 1 = Active-high (PMCS2) / (PMPCS2a)
- 0 = Active-low (PMCS2) / (PMPCS2a)

When the PMCS2/PMPCS2a pin is used as an address pin, the setting of the CS2P bit does not affect the polarity.

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
- 1 = Active-high ($\overline{\text{PMCS1}}$) / (PMPCS1a)
- 0 = Active-low (PMCS1) / (PMPCS1a)

Note: When the PMCS1/PMPCS1a pin is used as an address pin, the setting of the CS1P bit does not affect the polarity.

bit 2 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 1 **WRSP:** Write Strobe Polarity bit

For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):

1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)

For Master mode 1 (MODE<1:0> = 11):

1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit

For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):

1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)

For Master mode 1 (MODE<1:0> = 11):

1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

2: These bits have no effect when their corresponding pins are used as address lines.

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REGISTER 23-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAITB<1:0>(1)		WAITM<3:0>(1)				WAITE<1:0>(1)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)
- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits
- 11 = Reserved, do not use
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (Addressable Slave mode only)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
- 11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)
- 10 = Decrement ADDR<15:0> by 1 every read/write cycle(2)
- 01 = Increment ADDR<15:0> by 1 every read/write cycle(2)
- 00 = No increment or decrement of address

bit 10 **MODE16:** 8-bit/16-bit Data Mode bit
- 1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer
- 0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
- 11 = PMP mode, control signals (PMA<23/15:0>, PMD<23/15:0>, PMCS2(a), PMCS1(a), PMPRD/PMWR, PMENB)
- 10 = PMP mode, control signals (PMA<23/15:0>, PMD<23/15:0>, PMCS2(a), PMCS1(a), PMPRD, PMWR (byte_enable))
- 01 = Enhanced PSP mode, control signals (PMPRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
- 00 = Legacy Parallel Slave Port mode, control signals (PMPRD, PMWR, PMCS1, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits(1)
- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

REGISTER 23-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits(1)

1111 = Wait of 16 TPB
•
•
•
0001 = Wait of 2 TPB
0000 = Wait of 1 TPB (default)

bit 1-0 **WAITE<1:0>:** Data Hold After Read/Write Strobe Wait States bits(1)

11 = Wait of 4 TPB
10 = Wait of 3 TPB
01 = Wait of 2 TPB
00 = Wait of 1 TPB (default)

For Read operations:
11 = Wait of 3 TPB
10 = Wait of 2 TPB
01 = Wait of 1 TPB
00 = Wait of 0 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

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REGISTER 23-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2a	CS1a	ADDR<21:16>					
	WADDR23	WADDR22						
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2	CS1	ADDR<13:8>					
	ADDR15	ADDR14						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CS2a:** Chip Select 2a bit
This bit is only valid when the CSF<1:0> bits = 10 or 01.
1 = Chip Select 2a is enabled
0 = Chip Select 2a is disabled

bit 23 **WADDR23:** Address bits
This bit is only valid when the CSF<1:0> bits = 00 and the EXADR bit = 1 and the DUALBUF bit = 0.

bit 22 **CS1a:** Chip Select 1a bit
This bit is only valid when the CSF<1:0> bits = 10.
1 = Chip Select 1a is enabled
0 = Chip Select 1a is disabled

bit 22 **WADDR22:** Address bits
This bit is only valid when the CSF<1:0> bits = 00 and the EXADR bit = 1 and the DUALBUF bit = 0.

bit 21-16 **ADDR<21:16>:** Address bits
These bits are only valid when the EXADR bit = 1 and the DUALBUF bit = 0.

bit 15 **CS2:** Chip Select 2 bit
This bit is only valid when the CSF<1:0> bits = 10 or 01 and the EXADR bit = 0.
1 = Chip Select 2 is enabled
0 = Chip Select 2 is disabled

bit 15 **ADDR<15>:** Target Address bit 15
This bit is only valid when the CSF<1:0> bits = 10 or 01 and the EXADDR bit = 0.

bit 14 **CS1:** Chip Select 1 bit
This bit is only valid when the CSF<1:0> bits = 10 or 01 or EXADR bit = 0.
1 = Chip Select 1 is enabled
0 = Chip Select 1 is disabled

bit 14 **ADDR<14>:** Target Address bit 14
This bit is only valid when the CSF<1:0> bits = 01 or 00 or EXADR bit = 1.

bit 13-0 **ADDR<13:0>:** Address bits

Note: If the DUALBUF bit (PMCON<17>) = 0, the bits in this register control both read and write target addressing. If the DUALBUF bit = 1, the bits in this register are not used. In this instance, use the PMRADDR register for Read operations and the PMWADDR register for Write operations.

REGISTER 23-4: PMDOUT: PARALLEL PORT OUTPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAOUT<15:0>:** Port Data Output bits

This register is used for Read operations in the Enhanced Parallel Slave mode and Write operations for Dual Buffer Master mode.

In Dual Buffer Master mode, the DUALBUF bit (PMPCON<17>) = 1, a write to the MSB triggers the transaction on the PMP port. When MODE16 = 1, MSB = DATAOUT<15:8>. When MODE16 = 0, MSB = DATAOUT<7:0>.

Note: In Master mode, a read will return the last value written to the register. In Slave mode, a read will return indeterminate results.

REGISTER 23-5: PMDIN: PARALLEL PORT INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAIN<15:0>:** Port Data Input bits

This register is used for both Parallel Master Port mode and Enhanced Parallel Slave mode.

In Parallel Master mode, a write to the MSB triggers the write transaction on the PMP port. Similarly, a read to the MSB triggers the read transaction on the PMP port.

When MODE16 = 1, MSB = DATAIN<15:8>. When MODE16 = 0, MSB = DATAIN<7:0>.

Note: This register is not used in Dual Buffer Master mode (i.e., DUALBUF bit (PMPCON<17>) = 1).

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REGISTER 23-6: PMAEN: PARALLEL PORT PIN ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<15:14>(1)		PTEN<13:8>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTEN<7:2>						PTEN<1:0>(2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Write '0'; ignore read

bit 23-16 **PTEN<23:16>:** Port Enable bits

Valid if the EXADR bit is enabled in Master mode only. PAD enables for PMPCS2a, PMPCS1a, and ADDR<21:16>.

bit 15-14 **PTEN<15:14>:** PMCSx Address Port Enable bits

1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1(1)
0 = PMA15 and PMA14 function as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits

1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Address Port Enable bits

1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)
0 = PMA1 and PMA0 pads function as port I/O

Note 1: The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

2: The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by the ADRMUX<1:0> bits in the PMCON register.

REGISTER 23-7: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HS, SC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HS, SC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:	HS = Hardware Set	SC = Software Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
- 0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits
- 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)
- 0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

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REGISTER 23-8: PMWADDR: PARALLEL PORT WRITE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2a	CS1a	WADDR<21:16>					
	WADDR23	WADDR22						
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WCS2	WCS1	WADDR<13:8>					
	WADDR15	WADDR14						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CS2a:** Chip Select 2a bit
This bit is only valid when the CSF<1:0> bits = 10 or 01.
1 = Chip Select 2a is active
0 = Chip Select 2a is inactive

bit 23 **WADDR<23>:** Target Address bit 23
This bit is only valid when the CSF<1:0> bits = 00 and the EXADR bit = 1 and the DUALBUF bit = 1.

bit 22 **CS1a:** Chip Select 1a bit
This bit is only valid when the CSF<1:0> bits = 10.
1 = Chip Select 1a is active
0 = Chip Select 1a is inactive

bit 22 **WADDR<22>:** Target Address bit 22
This bit is only valid when the CSF<1:0> bits = 00 and the EXADR bit = 1 and the DUALBUF bit = 1.

bit 21-16 **WADDR<21:16>:** Address bits
This bit is only valid when the EXADR bit = 1 and the DUALBUF bit = 1.

bit 15 **WCS2:** Chip Select 2 bit
This bit is only valid when the CSF<1:0> bits = 10 or 01.
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive

bit 15 **WADDR<15>:** Target Address bit 15
This bit is only valid when the CSF<1:0> bits = 00.

bit 14 **WCS1:** Chip Select 1 bit
This bit is only valid when the CSF<1:0> bits = 10.
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive

bit 14 **WADDR<14>:** Target Address bit 14
This bit is only valid when the CSF<1:0> bits = 00 or 01.

bit 13-0 **WADDR<13:0>:** Address bits

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.

REGISTER 23-9: PMRADDR: PARALLEL PORT READ ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2a	CS1a	RADDR<21:16>					
	RADDR23	RADDR22						
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RCS2	RCS1	RADDR<13:8>					
	RADDR15	RADDR14						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CS2a:** Chip Select 2a bit
This bit is only valid when the CSF<1:0> bits = 10 or 01.
1 = Chip Select 2a is active
0 =Chip Select 2a is inactive

bit 23 **RADDR<23>:** Target Address bit 23
This bit is only valid when the CSF<1:0> bits = 00 and the EXADR bit = 1 and the DUALBUF bit = 1.

bit 22 **CS1a:** Chip Select 1a bit
This bit is only valid when the CSF<1:0> bits = 10.
1 = Chip Select 1a is active
0 = Chip Select 1a is inactive

bit 22 **RADDR<22>:** Target Address bit 22
This bit is only valid when the CSF<1:0> bits = 00 and the EXADR bit = 1 and the DUALBUF bit = 1.

bit 21-16 **RADDR<21:16>:** Address bits
This bit is only valid when the EXADR bit = 1 and the DUALBUF bit = 1.

bit 15 **RCS2:** Chip Select 2 bit
This bit is only valid when the CSF<1:0> bits = 10 or 01.
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive (RADDR15 function is selected)

bit 15 **RADDR<15>:** Target Address bit 15
This bit is only valid when the CSF<1:0> bits = 00.

bit 14 **RCS1:** Chip Select 1 bit
This bit is only valid when the CSF<1:0> bits = 10.
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive (RADDR14 function is selected)

bit 14 **RADDR<14>:** Target Address bit 14
This bit is only valid when the CSF<1:0> bits = 00 or 01.

bit 13-0 **RADDR<13:0>:** Address bits

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.

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REGISTER 23-10: PMRDIN: PARALLEL PORT READ INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RDATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RDATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **RDATAIN<15:8>:** Port Data <15:8> Input bits
Only valid when MODE16 = 1. Used for read operations in Dual Buffer Master mode only.

bit 7-0 **RDATAIN<7:0>:** Port Data <7:0> Input bits
Used for read operations in Dual Buffer Master mode only.

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1' and exclusively for reads. If the DUALBUF bit is '0', the PMDIN register (Register 23-5) is used for reads instead of PMRDIN.

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24.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

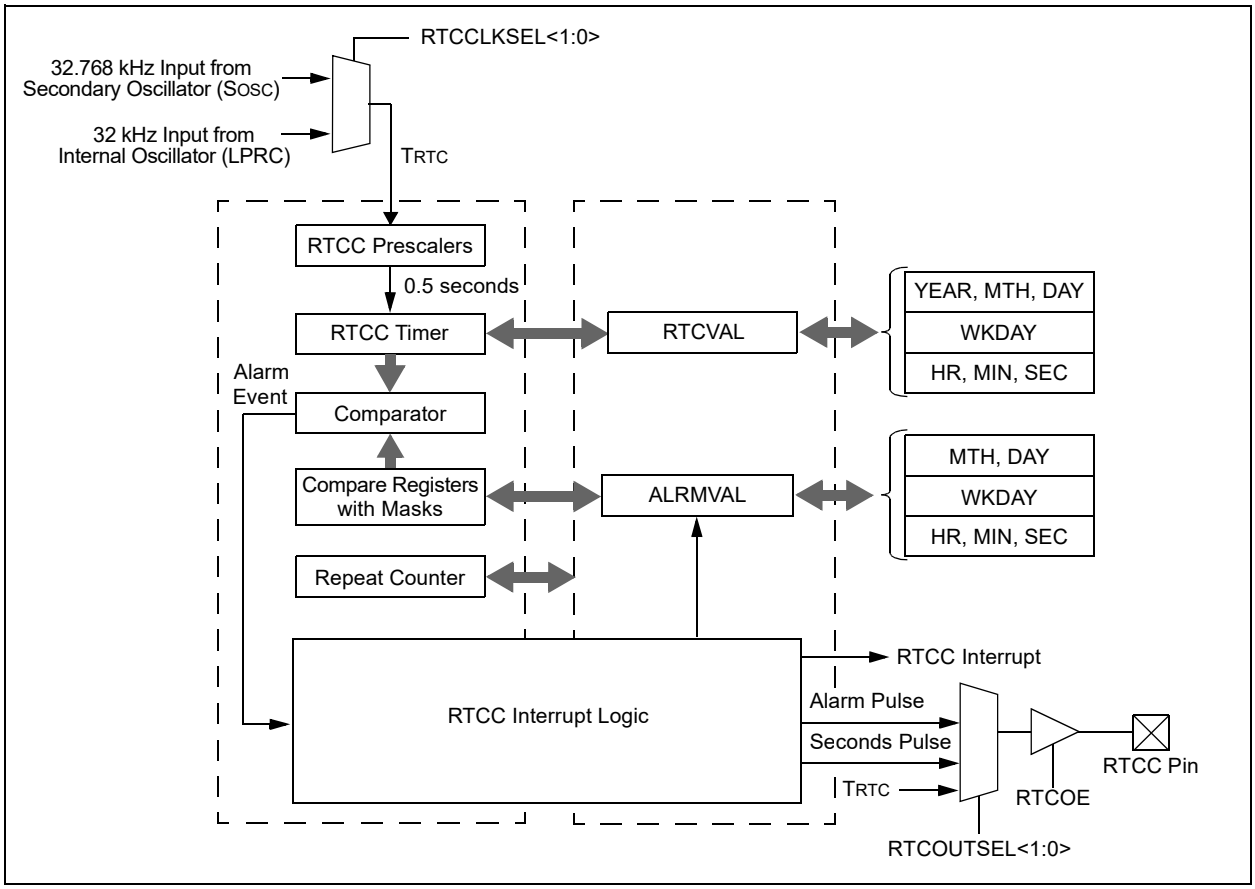
Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are key features of the RTCC module:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin (not in VBAT power domain, requires VDD)

FIGURE 24-1: RTCC BLOCK DIAGRAM



24.1 RTCC Control Registers

TABLE 24-1: RTCC REGISTER MAP

Virtual Address (BF8C_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	RTCCLKSEL<1:0>		RTCOUTSEL<1:0>		RTCCLKON	—	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0010	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>				ARPT<7:0>								0000
0020	RTCTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0030	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				MONTH10<3:0>				MONTH01<3:0>				xxxx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx00
0040	ALRMTIME	31:16	HR10<3:0>				HR01<3:0>				MIN10<3:0>				MIN01<3:0>				xxxx
		15:0	SEC10<3:0>				SEC01<3:0>				—	—	—	—	—	—	—	—	xx00
0050	ALRMDATE	31:16	—	—	—	—	—	—	—	—	MONTH10<3:0>				MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	WDAY01<3:0>				xx0x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 24-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CAL<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAL<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	—	—	RTCCLKSEL<1:0>		RTC OUTSEL<1>(2)
7:0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0
	RTC OUTSEL<0>(2)	RTC CLKON(5)	—	—	RTC WREN(3)	RTC SYNC	HALFSEC(4)	RTCOE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** Real-Time Clock Drift Calibration bits, which contain a signed 10-bit integer value

0111111111 = Maximum positive adjustment, adds 511 real-time clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 real-time clock pulse every one minute
0000000000 = No adjustment
1111111111 = Minimum negative adjustment, subtracts 1 real-time clock pulse every one minute
•
•
•
1000000000 = Maximum negative adjustment, subtracts 512 real-time clock pulses every one minute

bit 15 **ON:** RTCC On bit(1)

1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Disables RTCC operation when CPU enters Idle mode
0 = Continue normal operation when CPU enters Idle mode

bit 12-11 **Unimplemented:** Read as '0'

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).
5: This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

Note: This register is reset only on a POR.

REGISTER 24-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER

bit 10-9 **RTCCLKSEL<1:0>:** RTCC Clock Select bits
When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.
11 = Reserved
10 = Reserved
01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)
00 = RTCC uses the internal 32 kHz oscillator (LPRC)

bit 8-7 **RTCOUTSEL<1:0>:** RTCC Output Data Select bits(2)
11 = Reserved
10 = RTCC Clock is presented on the RTCC pin
01 = Seconds Clock is presented on the RTCC pin
00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit(5)
1 = RTCC Clock is actively running
0 = RTCC Clock is not running

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **RTCWREN:** Real-Time Clock Value Registers Write Enable bit(3)
1 = Real-Time Clock Value registers can be written to by the user
0 = Real-Time Clock Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** Real-Time Clock Value Registers Read Synchronization bit
1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = Real-time clock value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(4)
1 = Second half period of a second
0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is not enabled

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).
5: This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

Note:	This register is reset only on a POR.

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REGISTER 24-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN(1,2)	CHIME(2)	PIV(2)	ALRMSYNC	AMASK<3:0>(2)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit(1,2)
- 1 = Alarm is enabled
- 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)
- 1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit
- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing.
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is more than 32 real-time clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(2)
- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved
- 1011 = Reserved
- 11xx = Reserved

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note: The RTCALRM register is reset on a $\overline{\text{MCLR}}$, Power-on Reset (POR), or any time on an exit from Deep Sleep or VBAT mode.

REGISTER 24-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(2)

11111111 = Alarm will trigger 256 times
•
•
•
00000000 = Alarm will trigger one time
The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note:	The RTCALRM register is reset on a $\overline{\text{MCLR}}$, Power-on Reset (POR), or any time on an exit from Deep Sleep or VBAT mode.

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REGISTER 24-3: RTCTIME: REAL-TIME CLOCK TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **HR10<3:0>:** Binary-Coded Decimal Value of Hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary-Coded Decimal Value of Hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary-Coded Decimal Value of Minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary-Coded Decimal Value of Minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary-Coded Decimal Value of Seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary-Coded Decimal Value of Seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

REGISTER 24-4: RTCDATE: REAL-TIME CLOCK DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	YEAR10<3:0>				YEAR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<3:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **YEAR10<3:0>:** Binary-Coded Decimal Value of Years bits, 10 digits

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1 digit

bit 23-20 **MONTH10<3:0>:** Binary-Coded Decimal Value of Months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary-Coded Decimal Value of Days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary-Coded Decimal Value of Days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary-Coded Decimal Value of Weekdays bits,1 digit; contains a value from 0 to 6

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

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REGISTER 24-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **HR10<3:0>:** Binary Coded Decimal value of hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary Coded Decimal value of minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary Coded Decimal value of seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 24-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<1:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1 digit; contains a value from 0 to 6

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25.0 12-BIT HIGH-SPEED SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The 12-bit High-Speed Successive Approximation Register (SAR) analog-to-digital converter (ADC) includes the following features:

- 12-bit resolution
- Seven ADC modules with dedicated Sample and Hold (S&H) circuits
- Two dedicated ADC modules can be combined in Turbo mode to provide double conversion rate
- Up to 45 analog input sources, in addition to the internal CTMU, VBAT, internal voltage reference and internal temperature sensor
- Single-ended and/or differential inputs
- Supports touch sense applications
- Four digital comparators
- Four digital filters supporting two modes:
  - Oversampling mode
  - Averaging mode
- Early interrupt generation resulting in faster processing of converted data
- Designed for power conversion and general purpose applications
- Operation during Sleep and Idle modes

A simplified block diagram of the ADC module is illustrated in Figure 25-1.

The 12-bit HS SAR ADC has up to six dedicated ADC modules (ADC0-ADC5) and one shared ADC module (ADC7). The dedicated ADC modules use a single input (or its alternate) and are intended for high-speed and precise sampling of time-sensitive or transient inputs. The shared ADC module incorporates a multiplexer on the input to facilitate a larger group of inputs, with slower sampling, and provides flexible automated scanning option through the input scan logic.

For each ADC module, the analog inputs are connected to the S&H capacitor. The clock, sampling time, and output data resolution for each ADC module can be set independently. The ADC module performs the conversion of the input analog signal based on the configurations set in the registers. When conversion is complete, the final result is stored in the result buffer for the specific analog input and is passed to the digital filter and digital comparator if configured to use data from this particular sample. Input to ADCx mapping is illustrated in Figure 25-2.

25.1 Activation Sequence

The following ADCx activation sequence is to be followed at all times:

Step 1: Initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

Then, configure the AICPMPEN bit (ADCCON1<12> and the IOANCPEN bit (CFGCON<7>) = 1 if and only if VDD is less than 2.5V. The default is '0', which assumes VDD is greater than or equal to 2.5V.

Step 2: The user writes all the essential ADC configuration SFRs including the ADC control clock and all ADC core clocks setup:

- ADCCON1, keeping the ON bit = 0
- ADCCON2, especially paying attention to ADCDIV<6:0> and SAMC<9:0>
- ADCANCON, keeping all analog enables ANENx bit = 0
- ADCCON3, keeping all DIGEN5x = 0, especially paying attention to ADCSEL<1:0>, CONCLKDIV <5:0>, and VREFSEL<2:0>
- ADCxTIME, especially paying attention to ADCDIVx<6:0> and SAMCx<9:0>
- ADCTRGMODE, ADCIMCONx, ADCTRGSNS, ADCCSSx, ADCGIRQENx, ADCTRGx, ADCBASE
- Comparators, Filters, etc.

Step 3: The user sets the ON bit to '1', which enables the ADC control clock.

Step 4: The user waits for the interrupt/polls the status bit BGVRRDY = 1, which signals that the device analog environment (band gap and VREF) is ready.

Step 5: The user sets the ANENx bit to '1' for the ADC SAR Cores needed (which internally in the ADC module enables the control clock to generate by division the core clocks for the desired ADC SAR Cores, which in turn enables the bias circuitry for these ADC SAR Cores).

Step 6: The user waits for the interrupt/polls the warm-up ready bits WKRDYx = 1, which signals that the respective ADC SAR Cores are ready to operate.

Step 7: The user sets the DIGENx bit to '1', which enables the digital circuitry to immediately begin processing incoming triggers to perform data conversions.

Note:	For the best optimized CPU and ISR performance, refer to **TABLE 8-1: "ISR Latency Information"**. To complete the optimization, the user application should define ISRs that use the 'at vector' attribute (see Table 8-1). The CPU interrupt latency is ~43 SYSCLK cycles if no other interrupts are pending. If not using ADC DMA, and the ADC combined sum throughput rate of all the ADC modules in use is greater than (SYSCLK/ 43) = 2.8 Msps, it is recommended to use the ADC CPU early interrupt generation, defined in the ADCxTIME and ADCEIENx registers (see Register 25-33, Register 25-34, and Register 25-35). This will reduce the probability of the ADC results being overwritten by the next conversion before the CPU can read the previous ADC results. Do not use the early interrupts if using the ADC in the DMA module.

Do not activate ADC triggers sources until after ADC has been completely initialized, enabled, and warm up time complete.

NOTE: If using ADC DMA, ADC source clock must be SYSCLK only.

Dedicated Class 1 ADCx Throughput rate =

1/((Sample time + Conversion time)(TAD))

= 1 / ((SAMC+# bit resolution+1)(TAD))

Example:

SAMC = 3 TAD, 12-bit mode, TAD = 16.667 ns = 60 MHz:

Throughput rate = 1 / ((3+12+1)(16.667 ns))

= 1/(16 * 16.667 ns)

= 3.75 Msps

TABLE 25-1: PIC32MKXXX BASED ON A 60 MHz TAD CLOCK (16.667 ns)

Number of Class 1 Interleaved ADC Modules (12-bit mode)	TAD Trigger Spacing and Sampling time (SAMC)	Max. effective sampling rate
2	8	7.50 Msps
3	6	10.00 Msps
4	4	15.00 Msps
5	4	15.00 Msps
6	3	20.00 Msps

Note 1: Interleaved ADCs in this context means connecting the same analog source signal to multiple dedicated Class_1 ADCs (that is, ADC0-ADC5), and using independent staggered trigger sources accordingly for each interleaved ADC.

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FIGURE 25-1: ADC BLOCK DIAGRAM

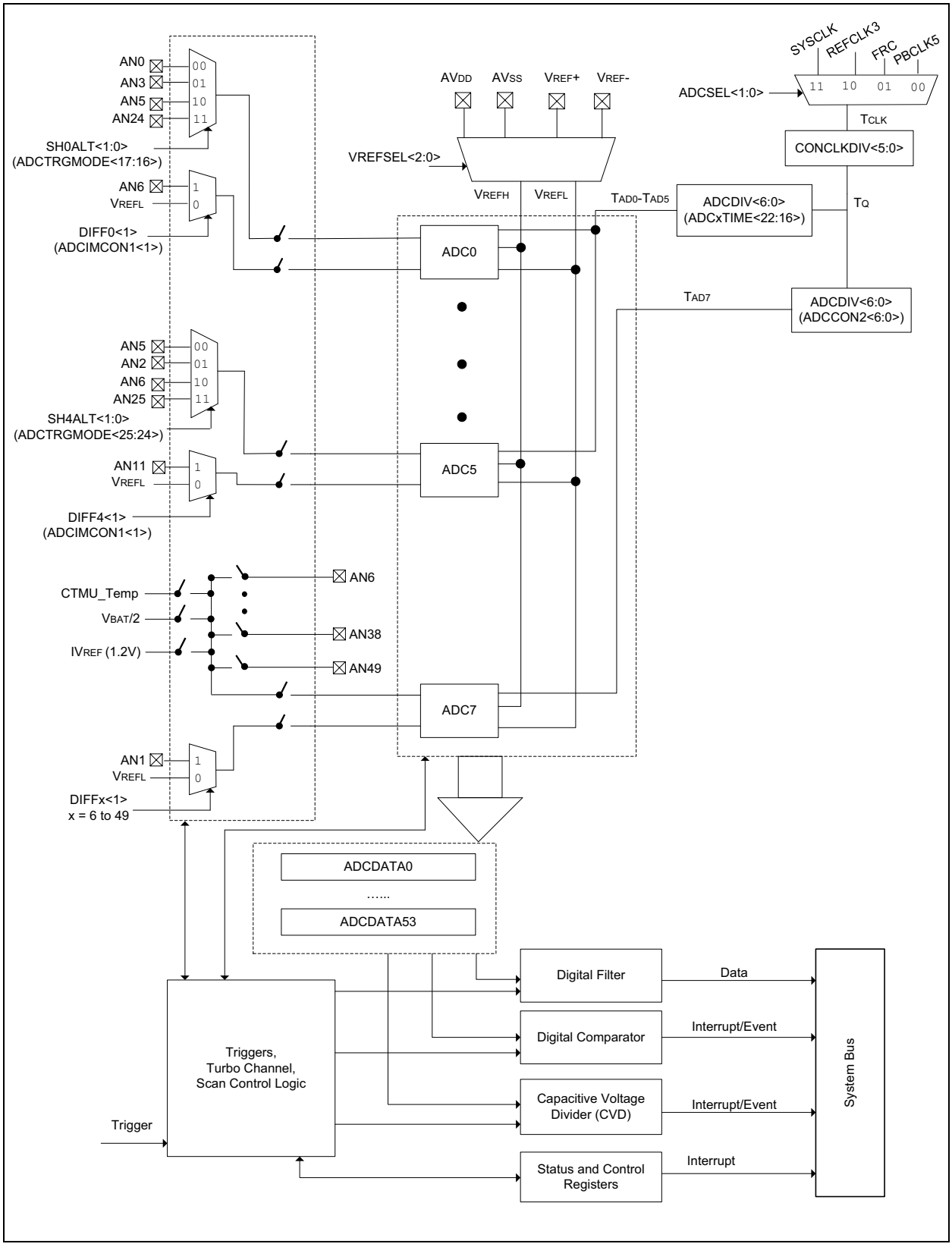
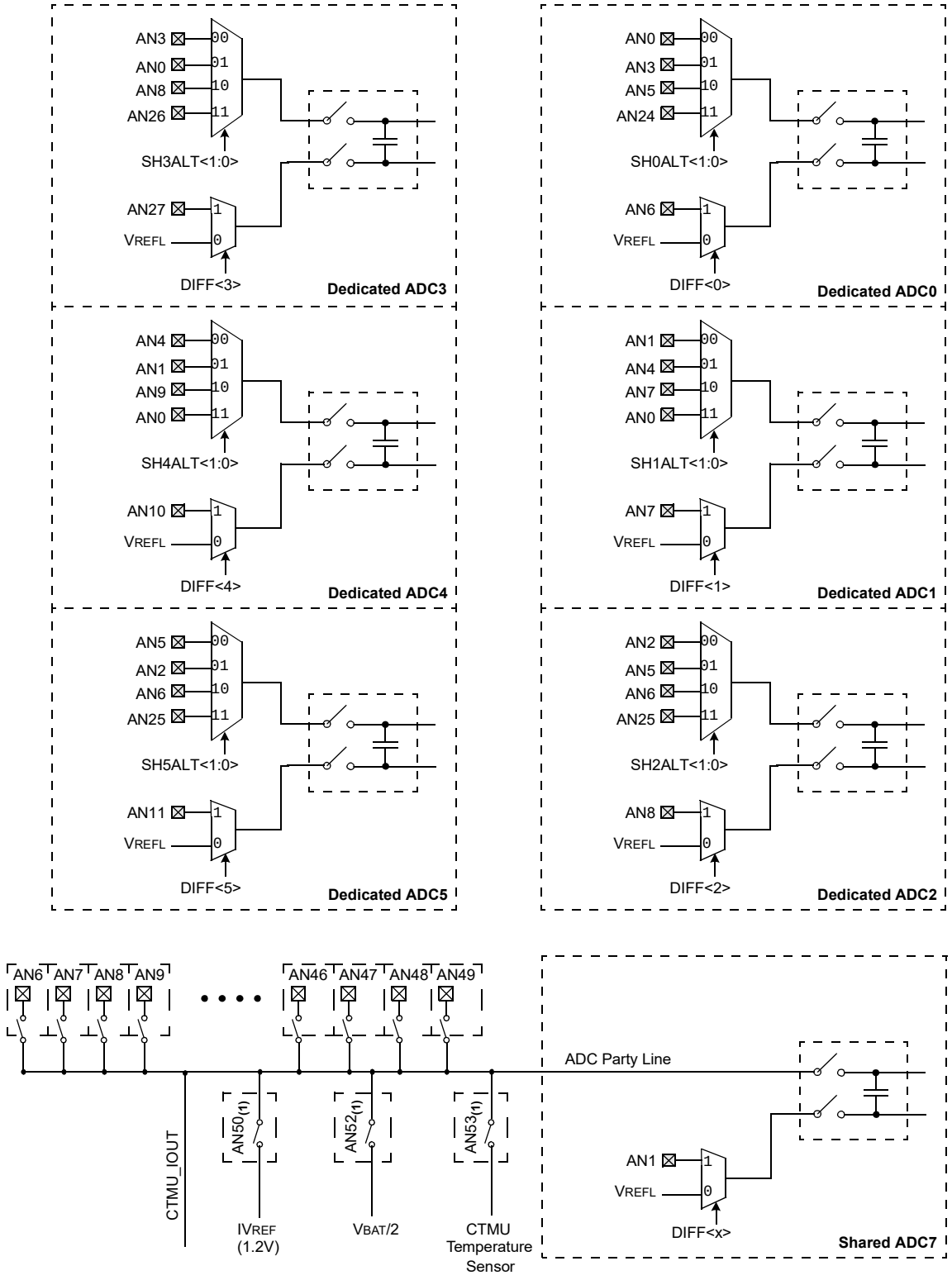


FIGURE 25-2: S&H BLOCK DIAGRAM



Note 1: AN50 through AN53 are internal analog input sources.

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25.2 ADC Control Registers

TABLE 25-2: ADC REGISTER MAP

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	ADCCON1	31:16	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>			FRACT	SELRES<1:0>		STRGSRC<4:0>					0600
		15:0	ON	—	SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—	—	IRQVS<2:0>			STRGLVL	—	—	—	0000
7010	ADCCON2	31:16	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>		SAMC<9:0>											0000
		15:0	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>			—	ADCDIV<6:0>							0000
7020	ADCCON3	31:16	ADCSEL<1:0>		CONCLKDIV<5:0>						DIGEN7	—	DIGEN5	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0	0000
		15:0	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT	GLSWTRG	GSWTRG	ADINSEL<5:0>						0000
7030	ADCTRGMODE	31:16	—	—	—	—	SH5ALT<1:0>		SH4ALT<1:0>		SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>		0000
		15:0	—	—	STRGEN5	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0	—	—	SSAMPEN5	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0	0000
7040	ADCIMCON1	31:16	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8	0000
		15:0	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0	0000
7050	ADCIMCON2	31:16	—	—	—	—	—	—	—	—	DIFF27	SIGN27	DIFF26	SIGN26	DIFF25	SIGN25	DIFF24	SIGN24	0000
		15:0	DIFF23(1)	SIGN23(1)	DIFF22(1)	SIGN22(1)	DIFF21(1)	SIGN21(1)	DIFF20(1)	SIGN20(1)	DIFF19	SIGN19	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16	0000
7060	ADCIMCON3	31:16	DIFF47(1)	SIGN47(1)	DIFF46(1)	SIGN46(1)	DIFF45(1)	SIGN45(1)	—	—	—	—	—	—	DIFF41(1)	SIGN41(1)	DIFF40(1)	SIGN40(1)	0000
		15:0	DIFF39(1)	SIGN39(1)	DIFF38(1)	SIGN38(1)	DIFF37(1)	SIGN37(1)	DIFF36(1)	SIGN36(1)	DIFF35(1)	SIGN35(1)	DIFF34(1)	SIGN34(1)	DIFF33(1)	SIGN33(1)	—	—	0000
7070	ADCIMCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	DIFF49	SIGN49	DIFF48	SIGN48	0000
7080	ADCGIRQEN1	31:16	—	—	—	—	AGIEN27	AGIEN26	AGIEN25	AGIEN24	AGIEN23(1)	AGIEN22(1)	AGIEN21(1)	AGIEN20(1)	AGIEN19	AGIEN18	AGIEN17	AGIEN16	0000
		15:0	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0	0000
7090	ADCGIRQEN2	31:16	—	—	—	—	—	—	—	—	—	—	AGIEN53(3)	AGIEN52(3)	AGIEN51(3)	AGIEN50(3)	AGIEN49	AGIEN48	0000
		15:0	AGIEN47(1)	AGIEN46(1)	AGIEN45(1)	—	—	—	AGIEN41(1)	AGIEN40(1)	AGIEN39(1)	AGIEN38(1)	AGIEN37(1)	AGIEN36(1)	AGIEN35(1)	AGIEN34(1)	AGIEN33(1)	AGIEN32(1)	0000
70A0	ADCCSS1	31:16	—	—	—	—	CSS27	CSS26	CSS25	CSS24	CSS23(1)	CSS22(1)	CSS21(1)	CSS20(1)	CSS19	CSS18	CSS17	CSS16	0000
		15:0	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
70B0	ADCCSS2	31:16	—	—	—	—	—	—	—	—	—	—	CSS53	CSS52	—	CSS50	CSS49	CSS48	0000
		15:0	CSS47(1)	CSS46(1)	CSS45(1)	—	—	—	CSS41(1)	CSS40(1)	CSS39(1)	CSS38(1)	CSS37(1)	CSS36(1)	CSS35(1)	CSS34(1)	CSS33(1)	—	0000
70C0	ADCDSTAT1	31:16	—	—	—	—	ARDY27	ARDY26	ARDY25	ARDY24	ARDY23(1)	ARDY22(1)	ARDY21(1)	ARDY20(1)	ARDY19	ARDY18	ARDY17	ARDY16	0000
		15:0	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0	0000
70D0	ADCDSTAT2	31:16	—	—	—	—	—	—	—	—	—	—	ARDY53	ARDY52	—	ARDY50	ARDY49	ARDY48	0000
		15:0	ARDY47(1)	ARDY46(1)	ARDY45(1)	—	—	—	ARDY41(1)	ARDY40(1)	ARDY39(1)	ARDY38(1)	ARDY37(1)	ARDY36(1)	ARDY35(1)	ARDY34(1)	ARDY33(1)	—	0000
70E0	ADCCMPEN1	31:16	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
70F0	ADCCMP1	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7100	ADCCMPEN2	31:16	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
7110	ADCCMP2	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
7120	ADCCMPEN3	31:16	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
7130	ADCCMP3	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
7140	ADCCMPEN4	31:16	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
7150	ADCCMP4	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
71A0	ADCFLTR1	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
71B0	ADCFLTR2	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
71C0	ADCFLTR3	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
71D0	ADCFLTR4	31:16	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY	—	—	—	CHNLID<4:0>					0000
		15:0	FLTRDATA<15:0>																0000
7200	ADCTRG1	31:16	—	—	—	TRGSRC3<4:0>					—	—	—	TRGSRC2<4:0>					0000
		15:0	—	—	—	TRGSRC1<4:0>					—	—	—	TRGSRC0<4:0>					0000
7210	ADCTRG2	31:16	—	—	—	TRGSRC7<4:0>					—	—	—	TRGSRC6<4:0>					0000
		15:0	—	—	—	TRGSRC5<4:0>					—	—	—	TRGSRC4<4:0>					0000
7220	ADCTRG3	31:16	—	—	—	TRGSRC11<4:0>					—	—	—	TRGSRC10<4:0>					0000
		15:0	—	—	—	TRGSRC9<4:0>					—	—	—	TRGSRC8<4:0>					0000
7230	ADCTRG4	31:16	—	—	—	TRGSRC15<4:0>					—	—	—	TRGSRC14<4:0>					0000
		15:0	—	—	—	TRGSRC13<4:0>					—	—	—	TRGSRC12<4:0>					0000
7240	ADCTRG5	31:16	—	—	—	TRGSRC19<4:0>(1)					—	—	—	TRGSRC18<4:0>					0000
		15:0	—	—	—	TRGSRC17<4:0>					—	—	—	TRGSRC16<4:0>					0000
7250	ADCTRG6(1)	31:16	—	—	—	TRGSRC23<4:0>					—	—	—	TRGSRC22<4:0>					0000
		15:0	—	—	—	TRGSRC21<4:0>					—	—	—	TRGSRC20<4:0>					0000
7260	ADCTRG7	31:16	—	—	—	TRGSRC27<4:0>					—	—	—	TRGSRC26<4:0>					0000
		15:0	—	—	—	TRGSRC25<4:0>					—	—	—	TRGSRC24<4:0>					0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7280	ADCCMPCON1	31:16	CVDDATA<15:0>																0000
		15:0	—	—	AINID<5:0>						ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
7290	ADCCMPCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
72A0	ADCCMPCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
72B0	ADCCMPCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AINID<4:0>					ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO	0000
7300	ADCBASE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADCBASE<15:0>																0000
7310	ADCDSTAT	31:16	DMAEN	—	RBFIEN5	RBFIEN4	RBFIEN3	RBFIEN2	RBFIEN1	RBFIEN0	WOVERR	—	RBF5	RBF4	RBF3	RBF2	RBF1	RBF0	0000
		15:0	DMACEN	—	RAFIEN5	RAFIEN4	RAFIEN3	RAFIEN2	RAFIEN1	RAFIEN0	—	—	RAF5	RAF4	RAF3	RAF2	RAF1	RAF0	0000
7320	ADCCNTB	31:16	ADCCNTB<31:16>																0000
		15:0	ADCCNTB<15:0>																0000
7330	ADCDMAB	31:16	ADCDMAB<31:16>																0000
		15:0	ADCDMAB<15:0>																0000
7340	ADCTRGSNS	31:16	—	—	—	—	LVL27	LVL26	LVL25	LVL24	LVL23(1)	LVL22(1)	LVL21(1)	LVL20(1)	LVL19	LVL18	LVL17	LVL16	0000
		15:0	LVL15	LVL14	LVL13	LVL12	LVL11	LVL10	LVL9	LVL8	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0	0000
7350	ADC0TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
7360	ADC1TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
7370	ADC2TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
7380	ADC3TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
7390	ADC4TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
73A0	ADC5TIME	31:16	—	—	—	ADCEIS<2:0>			SELRES<1:0>		BCHEN	ADCDIV<6:0>							0300
		15:0	—	—	—	—	—	—	SAMC<9:0>										0000
73C0	ADCEIEN1	31:16	—	—	—	—	EIEN27	EIEN26	EIEN25	EIEN24	EIEN23(1)	EIEN22(1)	EIEN21(1)	EIEN20(1)	EIEN19	EIEN18	EIEN17	EIEN16	0000
		15:0	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0	0000
73D0	ADCEIEN2	31:16	—	—	—	—	—	—	—	—	—	—	EIRDY53	EIRDY52	—	EIRDY50	EIRDY49	EIRDY48	0000
		15:0	EIRDY47(1)	EIRDY46(1)	EIRDY45(1)	—	—	—	EIEN41(1)	EIEN40(1)	EIEN39(1)	EIEN38(1)	EIEN37(1)	EIEN36(1)	EIEN35(1)	EIEN34(1)	EIEN33(1)	—	0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
73E0	ADCEISTAT1	31:16	—	—	—	—	EIRDY27	EIRDY26	EIRDY25	EIRDY24	EIRDY23(1)	EIRDY22(1)	EIRDY21(1)	EIRDY20(1)	EIRDY19	EIRDY18	EIRDY17	EIRDY16	0000
		15:0	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0	0000
73F0	ADCEISTAT2	31:16	—	—	—	—	—	—	—	—	—	—	EIRDY53	EIRDY52	—	EIRDY50	EIRDY49	EIRDY48	0000
		15:0	EIRDY47(1)	EIRDY46(1)	EIRDY45(1)	—	—	—	EIRDY41(1)	EIRDY40(1)	EIRDY39(1)	EIRDY38(1)	EIRDY37(1)	EIRDY36(1)	EIRDY35(1)	EIRDY34(1)	EIRDY33(1)	—	0000
7400	ADCANCON	31:16	—	—	—	—	WKUPCLKCNT<3:0>				WKIEN7	—	WKIEN5	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0	0000
		15:0	WKRDY7	—	WKRDY5	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0	ANEN7	—	ANEN5	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0	0000
7600	ADCDATA0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7610	ADCDATA1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7620	ADCDATA2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7630	ADCDATA3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7640	ADCDATA4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7650	ADCDATA5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7660	ADCDATA6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7670	ADCDATA7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7680	ADCDATA8	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7690	ADCDATA9	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76A0	ADCDATA10	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76B0	ADCDATA11	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76C0	ADCDATA12	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76D0	ADCDATA13	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., V_{BAT}, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
76E0	ADCDATA14	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
76F0	ADCDATA15	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7700	ADCDATA16	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7710	ADCDATA17	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7720	ADCDATA18	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7730	ADCDATA19	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7740	ADCDATA20(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7750	ADCDATA21(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7760	ADCDATA22(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7770	ADCDATA23(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7780	ADCDATA24	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7790	ADCDATA25	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
77A0	ADCDATA26	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
77B0	ADCDATA27	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7810	ADCDATA33(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7820	ADCDATA34(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7830	ADCDATA35(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., VBAT, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7840	ADCDATA36(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7850	ADCDATA37(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7860	ADCDATA38(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7870	ADCDATA39(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7880	ADCDATA40(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7890	ADCDATA41(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78D0	ADCDATA45(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78E0	ADCDATA46(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
78F0	ADCDATA47(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7900	ADCDATA48	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7910	ADCDATA49	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7920	ADCDATA50(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7940	ADCDATA52(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7950	ADCDATA53(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
7E00	ADCSYSCFG0	31:16	—	—	—	—	AN27	AN26	AN25	AN24	AN23(1)	AN22(1)	AN21(1)	AN20(1)	AN19	AN18	AN17	AN16	0FxF
		15:0	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	FFFF
7E10	ADCSYSCFG1	31:16	—	—	—	—	—	—	—	—	—	—	AN53(1)	AN52(1)	—	AN50(1)	AN49	AN48	00xx
		15:0	AN47(1)	AN46(1)	AN45(1)	—	—	—	AN41(1)	AN40(1)	AN39(1)	AN38(1)	AN37(1)	AN36(1)	AN35(1)	AN34(1)	AN33(1)	—	xxxx
7D00	ADC0CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., V_{BAT}, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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TABLE 25-2: ADC REGISTER MAP (CONTINUED)

Virtual Address	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7D10	ADC1CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D20	ADC2CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D30	ADC3CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D40	ADC4CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D50	ADC5CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000
7D70	ADC7CFG(3)	31:16	ADCCFG<31:16>																0000
		15:0	ADCCFG<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This register is for internal ADC input sources (i.e., V_{BAT}, and CTMU Temperature Sensor.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively.

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REGISTER 25-1: ADCCON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>		
23:16	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRACT	SELRES<1:0>		STRGSRC<4:0>				
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	ON		SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	IRQVS<2:0>			STRGLVL	DMABL<2:0>		

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **TRBEN:** Turbo Channel Enable bit
1 = Enable the Turbo channel
0 = Disable the Turbo channel

bit 30 **TRBERR:** Turbo Channel Error Status bit
1 = An error occurred while setting the Turbo channel and Turbo channel function to be disabled regardless of the TRBEN bit being set to '1'.
0 = Turbo channel error did not occur

Note: The status of this bit is valid only after the TRBEN bit is set.

bit 29-27 **TRBMST<2:0>:** Turbo Master ADCx bits
111 = Reserved
110 = Reserved
101 = ADC5
100 = ADC4
011 = ADC3
010 = ADC2
001 = ADC1
000 = ADC0

bit 26-24 **TRBSLV<2:0>:** Turbo Slave ADCx bits
111 = Reserved
110 = Reserved
101 = ADC5
100 = ADC4
011 = ADC3
010 = ADC2
001 = ADC1
000 = ADC0

bit 23 **FRACT:** Fractional Data Output Format bit
1 = Fractional
0 = Integer

bit 22-21 **SELRES<1:0>:** Shared ADC7 (i.e., AN6-AN53) Resolution bits
11 = 12 bits (default)
10 = 10 bits
01 = 8 bits
00 = 6 bits

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REGISTER 25-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 20-16 **STRGSRC<4:0>:** Scan Trigger Source Select bits
11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control only)
11100 = PWM Generator 5 Current-Limit (Motor Control only)
11011 = PWM Generator 4 Current-Limit (Motor Control only)
11010 = PWM Generator 3 Current-Limit (Motor Control only)
11001 = PWM Generator 2 Current-Limit (Motor Control only)
11000 = PWM Generator 1 Current-Limit (Motor Control only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 period end
10010 = Output Compare 3 period end
10001 = Output Compare 2 period end
10000 = Output Compare 1 period end
01111 = PWM Generator 6 trigger (Motor Control only)
01110 = PWM Generator 5 trigger (Motor Control only)
01101 = PWM Generator 4 trigger (Motor Control only)
01100 = PWM Generator 3 trigger (Motor Control only)
01011 = PWM Generator 2 trigger (Motor Control only)
01010 = PWM Generator 1 trigger (Motor Control only)
01001 = Secondary PWM time base (Motor Control only)
01000 = Primary PWM time base (Motor Control only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: These triggers only apply to implemented analog inputs AN32-AN53. For AN0-AN27 refer to ADCTRG1-ADCTRG7.

bit 15 **ON:** ADC Module Enable bit
1 = ADC module is enabled
0 = ADC module is disabled

Note: The ON bit should be set only after the ADC module has been configured.

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

REGISTER 25-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 12 **AICPMPEN:** Analog Input Charge Pump Enable bit

1 = Analog input charge pump is enabled
0 = Analog input charge pump is disabled (default)

Note 1: For proper analog operation at VDD less than 2.5V, the AICPMPEN bit must be = 1, and the IOANCPEN bit in the CFGCON register must be set to '1'. This bit must not be set if VDD is greater than 2.5V.

2: ADC throughput rate performance is reduced, as defined in the following table, if AICPMPEN = 1 or IOANCPEN (CFGCON<7) = 1.

ADC0	ADC1	ADC2	ADC3	ADC4	ADC5	ADC7	Maximum Sum of Total ADC Throughputs
ON	OFF	OFF	OFF	OFF	OFF	OFF	2 Msps
ON	ON	OFF	OFF	OFF	OFF	OFF	4 Msps
ON	ON	ON	OFF	OFF	OFF	OFF	5 Msps
OFF	OFF	OFF	ON	OFF	OFF	OFF	2 Msps
OFF	OFF	OFF	ON	ON	OFF	OFF	4 Msps
OFF	OFF	OFF	ON	ON	ON	OFF	5 Msps
OFF	OFF	OFF	ON	ON	ON	ON	5 Msps
ON	ON	ON	ON	OFF	OFF	OFF	7 Msps
ON	ON	ON	ON	ON	OFF	OFF	9 Msps
ON	ON	ON	ON	ON	ON	OFF	10 Msps
ON	OFF	OFF	ON	ON	ON	ON	7 Msps
ON	ON	OFF	ON	ON	ON	ON	9 Msps
ON	ON	ON	ON	ON	ON	ON	10 Msps

bit 11 **CVDEN:** Capacitive Voltage Division Enable bit

1 = CVD operation is enabled
0 = CVD operation is disabled

bit 10 **FSSCLKEN:** Bypass Fast Synchronous DMA System Clock to ADC Control Clock

1 = Bypass synchronizer logic for DMA system clock to ADC control clocks

0 = Enable clock synchronizers for non-synchronized DMA to ADC clock sources

NOTE: Synchronizers required if ADCCON3<ADCSEL> = REFCLK3, or ADCCON3<ADCSEL> = FRC and FRC is not SYSCLK source otherwise this bit is n/a.

bit 9 **FSPBCLKEN:** Bypass Fast Synchronous Peripheral Bus Clock to ADC Control Clock

1 = Bypass synchronizer logic for peripheral clock to ADC control clocks

0 = Enable clock synchronizers for non-synchronized peripheral clock to ADC control clocks

NOTE: Synchronizers required if ADCCON3<ADCSEL> = REFCLK3, or ADCCON3<ADCSEL> = FRC and FRC is not SYSCLK source otherwise this bit is n/a.

bit 8-7 **Unimplemented:** Read as '0'

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REGISTER 25-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 6-4 **IRQVS<2:0>:** Interrupt Vector Shift bits

To determine interrupt vector address, this bit specifies the amount of left shift done to the AIRDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with the ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

111 = Shift x left 7 bit position
110 = Shift x left 6 bit position
101 = Shift x left 5 bit position
100 = Shift x left 4 bit position
011 = Shift x left 3 bit position
010 = Shift x left 2 bit position
001 = Shift x left 1 bit position
000 = Shift x left 0 bit position

bit 3 **STRGLVL:** Scan Trigger High Level/Positive Edge Sensitivity bit

1 = Scan trigger is high level sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), the scan trigger will continue for all selected analog inputs, until the STRIG option is removed.
0 = Scan trigger is positive edge sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), only a single scan trigger will be generated, which will complete the scan of all selected analog inputs.

bit 2-0 **DMABL<2:0>:** DMA to System RAM Buffer Length Size bits

These bits define the number of locations in system memory allocated per analog input for DMA interface use.

Because each output data is 16-bit wide, one location consists of 2 bytes. Therefore the actual size reserved in the System RAM follows the formula: RAM Buffer Length in bytes = 2(DMABL+1).

The DMABL field can also be thought of as a "Left Shift Amount +1" needed for the channel ID to create the DMA byte address offset to be added to the contents of ADDMAB in order to obtain the byte address of the beginning of the System RAM buffer area allocated for the given channel.

111 = Allocates 128 locations in system memory to each analog input, actually 256 bytes
110 = Allocates 64 locations in system memory to each analog input, actually 128 bytes
101 = Allocates 32 locations in system memory to each analog input, actually 64 bytes
100 = Allocates 16 locations in system memory to each analog input, actually 32 bytes
011 = Allocates 8 locations in system memory to each analog input, actually 16 bytes
010 = Allocates 4 locations in system memory to each analog input, actually 8 bytes
001 = Allocates 2 locations in system memory to each analog input, actually 4 bytes
000 = Allocates 1 location in system memory to each analog input, actually 2 bytes

REGISTER 25-2: ADCCON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>			SAMC<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	ADCDIV<6:0>						

Legend:	HC = Hardware Set	HS = Hardware Cleared	r = Reserved
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **BGVRRDY:** Band Gap Voltage/ADC Reference Voltage Status bit
1 = Both band gap voltage and ADC reference voltages (VREF) are ready
0 = Either or both band gap voltage and ADC reference voltages (VREF) are not ready

Data processing is valid only after BGVRRDY is set by hardware, so the application code must check that the BGVRRDY bit is set to ensure data validity. This bit set to '0' when ON (ADCCON1<15>) = 0.

bit 30 **REFFLT:** Band Gap/VREF/AVDD BOR Fault Status bit
1 = Fault in band gap or the VREF voltage while the ON bit (ADCCON1<15>) was set. Most likely a band gap or VREF fault will be caused by a BOR of the analog VDD supply.
0 = Band gap and VREF voltage are working properly

This bit is cleared when the ON bit (ADCCON1<15>) = 0 and the BGVRRDY bit = 1.

bit 29 **EOSRDY:** End of Scan Interrupt Status bit
1 = All analog inputs are considered for scanning through the scan trigger (all analog inputs specified in the ADCCSS1 and ADCCSS2 registers) have completed scanning
0 = Scanning has not completed

This bit is cleared when ADCCON2<31:24> are read in software.

bit 28-26 **CVDCPL<2:0>:** Capacitor Voltage Divider (CVD) Setting bits
111 = 7 * 2.5 pF = 17.5 pF
110 = 6 * 2.5 pF = 15 pF
101 = 5 * 2.5 pF = 12.5 pF
100 = 4 * 2.5 pF = 10 pF
011 = 3 * 2.5 pF = 7.5 pF
010 = 2 * 2.5 pF = 5 pF
001 = 1 * 2.5 pF = 2.5 pF
000 = 0 * 2.5 pF = 0 pF

Note: These bits are available only on shared ADC7 inputs AN6-AN49. Once enabled (CVDCPL<2:0>) > 000), the internal capacitors are internally connected to all ADC7 inputs. To determine user ADC sampling time requirements (SAMC<9:0> bits (ADCCON2<25:16>)) with CVDCPL selection, refer to **Table 36-41: "ADC Sample Times with CVD Enabled"**.

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REGISTER 25-2: ADCCON2: ADC CONTROL REGISTER 2 (CONTINUED)

bit 25-16 **SAMC<9:0>:** Sample Time for the Shared ADC (ADC7) bits

1111111111 = 1025 TAD
•
•
•
0000000001 = 3 TAD
0000000000 = 2 TAD

Where TAD = period of the ADC conversion clock for the Shared ADC (ADC7) controlled by the ADCDIV<6:0> bits.

Note: Unlike the High-Speed Class 1 ADC modules, the trigger event for the shared Class 3 ADC7 module initiates the SAMC *sampling* sequence, rather than the *convert* sequence.

Shared ADC7 Throughput rate:

= ((1/((Sample time + Conversion Time)(TAD))) / Number of ADC inputs used in scan list)

= ((1 / ((SAMC + Number of Bit Resolution + 1)(TAD))) / Number of ADC inputs used in scan list)

Example:

Scan mode enabled with two ANx inputs in the scan list (i.e., ADCCSSx<CSSy>),
SAMC = 4 TAD, 12-bit mode, TAD = 16.667 ns = 60 MHz:

Throughput rate = ((1 / ((4+12 + 1)(16.667 ns))) / 2)

= ((1 / (17 * 16.667 ns)) / 2)

= 1.764706 msps

bit 15 **BGVRIEN:** Band Gap/VREF Voltage Ready Interrupt Enable bit

1 = Interrupt will be generated when the BGVRDDY bit is set
0 = No interrupt is generated when the BGVRRDY bit is set

bit 14 **REFFLTIEN:** Band Gap/VREF Voltage Fault Interrupt Enable bit

1 = Interrupt will be generated when the REFFLT bit is set
0 = No interrupt is generated when the REFFLT bit is set

bit 13 **EOSIEN:** End of Scan Interrupt Enable bit

1 = Interrupt will be generated when EOSRDY bit is set
0 = No interrupt is generated when the EOSRDY bit is set

bit 12 **ADCEIOVR:** Early Interrupt Request Override bit

1 = Early interrupt generation is overridden and interrupt generation is controlled by the ADCGIRQEN1 and ADCGIRQEN2 registers
0 = Early interrupt generation is not overridden and interrupt generation is controlled by the ADCEIEN1 and ADCEIEN2 registers

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **ADCEIS<2:0>:** Shared ADC (ADC7) Early Interrupt Select bits

These bits select the number of clocks (TAD7) prior to the arrival of valid data that the associated interrupt is generated.

111 = The data ready interrupt is generated 8 ADC clocks prior to end of conversion
110 = The data ready interrupt is generated 7 ADC clocks prior to end of conversion
•
•
•
001 = The data ready interrupt is generated 2 ADC module clocks prior to end of conversion
000 = The data ready interrupt is generated 1 ADC module clock prior to end of conversion

Note: All options are available when the selected resolution, set by the SELRES<1:0> bits (ADCCON1<22:21>), is 12-bit or 10-bit. For a selected resolution of 8-bit, options from '000' to '101' are valid. For a selected resolution of 6-bit, options from '000' to '011' are valid.

bit 7 **Unimplemented:** Read as '0'

REGISTER 25-2: ADCCON2: ADC CONTROL REGISTER 2 (CONTINUED)

bit 6-0 **ADCDIV<6:0>:** Shared ADC (ADC7) Clock Divider bits

1111111 = 254 * TQ = TAD
•
•
•
0000011 = 6 * TQ = TAD
0000010 = 4 * TQ = TAD
0000001 = 2 * TQ = TAD
0000000 = Reserved

The ADCDIV<6:0> bits divide the ADC control clock (TQ) to generate the clock for the Shared ADC, ADC7 (TAD7).

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REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCSEL<1:0>		CONCLKDIV<5:0>					
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIGEN7	—	DIGEN5	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R-0, HS, HC
	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP(1,2,3,4)	RQCNVRT
7:0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GLSWTRG	GSWTRG	ADINSEL<5:0>					

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **ADCSEL<1:0>:** Analog-to-Digital Clock Source (TCLK) bits
11 = SYSCLK (Required if using DMA for ADC)
10 = REFCLK3
01 = FRC
00 = PBCLK5

bit 29-24 **CONCLKDIV<5:0>:** Analog-to-Digital Control Clock (TQ) Divider bits
111111 = 126 * TCLK = TQ
•
•
•
000011 = 6 * TCLK = TQ
000010 = 4 * TCLK = TQ
000001 = 2 * TCLK = TQ
000000 = TCLK = TQ

bit 23 **DIGEN7:** Shared ADC (ADC7) Digital Enable bit
1 = ADC7 is digital enabled
0 = ADC7 is digital disabled

bit 22 **Unimplemented:** Read as '0'

bit 21 **DIGEN5:** ADC5 Digital Enable bit
1 = ADC5 is digital enabled (required for active operation)
0 = ADC5 is digital disabled (power-saving mode)

bit 20 **DIGEN4:** ADC4 Digital Enable bit
1 = ADC4 is digital enabled (required for active operation)
0 = ADC4 is digital disabled (power-saving mode)

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion (ADC).

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 19 **DIGEN3:** ADC3 Digital Enable bit
1 = ADC3 is digital enabled (required for active operation)
0 = ADC3 is digital disabled (power-saving mode)

bit 18 **DIGEN2:** ADC2 Digital Enable bit
1 = ADC2 is digital enabled (required for active operation)
0 = ADC2 is digital disabled (power-saving mode)

bit 17 **DIGEN1:** ADC1 Digital Enable bit
1 = ADC1 is digital enabled (required for active operation)
0 = ADC1 is digital disabled (power-saving mode)

bit 16 **DIGEN0:** ADC0 Digital Enable bit
1 = ADC0 is digital enabled (required for active operation)
0 = ADC0 is digital disabled (power-saving mode)

bit 15-13 **VREFSEL<2:0>:** Voltage Reference (VREF) Input Selection bits

VREFSEL<2:0>	ADC VREFH	ADC VREFL
1xx	Reserved	Reserved
011	VREF+	VREF-
010	AVDD	VREF-
001	VREF+	AVSS
000	AVDD	AVSS

bit 12 **TRGSUSP:** Trigger Suspend bit
1 = Triggers are blocked from starting a new analog-to-digital conversion, but the ADC module is not disabled
0 = Triggers are not blocked

bit 11 **UPDIEN:** Update Ready Interrupt Enable bit
1 = Interrupt will be generated when the UPDRDY bit is set by hardware
0 = No interrupt is generated

bit 10 **UPDRDY:** ADC Update Ready Status bit
1 = ADC SFRs can be updated
0 = ADC SFRs cannot be updated

Note: This bit is only active while the TRGSUSP bit is set and there are no more running conversions of any ADC modules.

bit 9 **SAMP:** Shared ADC7 Analog Input Sampling Enable bit**(1,2,3,4)**
1 = The ADC S&H amplifier is sampling
0 = The ADC S&H amplifier is holding

bit 8 **RQCNVRT:** Individual ADC Input Conversion Request bit
This bit and its associated ADINSEL<5:0> bits enable the user to individually request an analog-to-digital conversion of an analog input through software.
1 = Trigger the conversion of the selected ADC input as specified by the ADINSEL<5:0> bits
0 = Do not trigger the conversion

Note: This bit is automatically cleared in the next ADC clock cycle.

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion (ADC).

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

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REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 7 **GLSWTRG:** Global Level Software Trigger bit
1 = Trigger conversion for ADC inputs that have selected the GLSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register
0 = Do not trigger an analog-to-digital conversion

bit 6 **GSWTRG:** Global Software Trigger bit
1 = Trigger conversion for ADC inputs that have selected the GSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register
0 = Do not trigger an analog-to-digital conversion
Note: This bit is automatically cleared in the next ADC clock cycle.

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion (ADC).

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 25-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 5-0 **ADINSEL<5:0>:** Analog Input Select bits

These bits select the analog input to be converted when the RQCNVRT bit is set.

111111 = Reserved
.
.
.
110110 = Reserved
110101 = CTMU Temperature Sensor (internal AN53)
110100 = VBAT/2 (internal AN52)
110011 = Reserved
110010 = IVREF 1.2V (internal AN50)
110001 = AN49
.
.
.
101101 = AN45
101100 = Reserved
.
.
.
101010 = Reserved
101001 = AN41
.
.
.
100001 = AN33
100000 = Reserved
.
.
.
011100 = Reserved
011011 = AN27
.
.
.
000000 = AN0

Note: AN20-AN23, AN33-AN41, and AN45-AN47 are not available on 64-pin devices. Refer to **TABLE 1-1: "ADC Analog Pinout I/O Descriptions"** for details.

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion (ADC).

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

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REGISTER 25-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SH5ALT<1:0>		SH4ALT<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>	
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	STRGEN5	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	SSAMPEN5	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-26 **SH5ALT<1:0>:** ADC5 Analog Input Select bit
- 11 = AN25(1)
- 10 = AN6(1)
- 01 = AN2(1)
- 00 = AN5

bit 25-24 **SH4ALT<1:0>:** ADC4 Analog Input Select bit
- 11 = AN0(1)
- 10 = AN9(1)
- 01 = AN1(1)
- 00 = AN4

bit 23-22 **SH3ALT<1:0>:** ADC3 Analog Input Select bit
- 11 = AN26(1)
- 10 = AN8(1)
- 01 = AN0(1)
- 00 = AN3

bit 21-20 **SH2ALT<1:0>:** ADC2 Analog Input Select bit
- 11 = AN25(1)
- 10 = AN6(1)
- 01 = AN5(1)
- 00 = AN2

bit 19-18 **SH1ALT<1:0>:** ADC1 Analog Input Select bit
- 11 = AN0(1)
- 10 = AN7(1)
- 01 = AN4(1)
- 00 = AN1

bit 17-16 **SH0ALT<1:0>:** ADC0 Analog Input Select bit
- 11 = AN24(1)
- 10 = AN5(1)
- 01 = AN3(1)
- 00 = AN0

bit 15-14 **Unimplemented:** Read as '0'

Note 1: Regardless of which alternate input is selected by SHxALT, for ADC0-ADC5 only, all control and results are handled by the native SHxALT = '0b00 input. For example, SH0ALT = '0b11 = AN24. However, from a software and silicon hardware control and results register perspective, the user must initialize the ADC0 module as if AN24 were actually AN0.

REGISTER 25-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

bit 13 **STRGEN5:** ADC5 Presynchronized Triggers bit
1 = ADC5 uses presynchronized triggers
0 = ADC5 does not use presynchronized triggers

bit 12 **STRGEN4:** ADC4 Presynchronized Triggers bit
1 = ADC4 uses presynchronized triggers
0 = ADC4 does not use presynchronized triggers

bit 11 **STRGEN3:** ADC3 Presynchronized Triggers bit
1 = ADC3 uses presynchronized triggers
0 = ADC3 does not use presynchronized triggers

bit 10 **STRGEN2:** ADC2 Presynchronized Triggers bit
1 = ADC2 uses presynchronized triggers
0 = ADC2 does not use presynchronized triggers

bit 9 **STRGEN1:** ADC1 Presynchronized Triggers bit
1 = ADC1 uses presynchronized triggers
0 = ADC1 does not use presynchronized triggers

bit 8 **STRGEN0:** ADC0 Presynchronized Triggers bit
1 = ADC0 uses presynchronized triggers
0 = ADC0 does not use presynchronized triggers

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **SSAMPEN5:** ADC5 Synchronous Sampling bit
1 = ADC5 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC5 does not use synchronous sampling

bit 4 **SSAMPEN4:** ADC4 Synchronous Sampling bit
1 = ADC4 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC4 does not use synchronous sampling

bit 3 **SSAMPEN3:** ADC3 Synchronous Sampling bit
1 = ADC3 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC3 does not use synchronous sampling

bit 2 **SSAMPEN2:** ADC2Synchronous Sampling bit
1 = ADC2 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC2 does not use synchronous sampling

bit 1 **SSAMPEN1:** ADC1 Synchronous Sampling bit
1 = ADC1 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC1 does not use synchronous sampling

bit 0 **SSAMPEN0:** ADC0 Synchronous Sampling bit
1 = ADC0 uses synchronous sampling for the first sample after being idle or disabled
0 = ADC0 does not use synchronous sampling

Note 1: Regardless of which alternate input is selected by SHxALT, for ADC0-ADC5 only, all control and results are handled by the native SHxALT = 'b00 input. For example, SH0ALT = 'b11 = AN24. However, from a software and silicon hardware control and results register perspective, the user must initialize the ADC0 module as if AN24 were actually AN0.

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REGISTER 25-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DIFF15:** AN15 Mode bit
1 = Selects AN15 differential input pair as AN15+ and AN1-
0 = AN15 is using Single-ended mode

bit 30 **SIGN:15** AN15 Signed Data Mode bit
1 = AN15 is using Signed Data mode
0 = AN15 is using Unsigned Data mode

bit 29 **DIFF14:** AN14 Mode bit
1 = Selects AN14 differential input pair as AN14+ and AN1-
0 = AN14 is using Single-ended mode

bit 28 **SIGN14:** AN14 Signed Data Mode bit
1 = AN14 is using Signed Data mode
0 = AN14 is using Unsigned Data mode

bit 27 **DIFF13:** AN13 Mode bit
1 = Selects AN13 differential input pair as AN13+ and AN1-
0 = AN13 is using Single-ended mode

bit 26 **SIGN13:** AN13 Signed Data Mode bit
1 = AN13 is using Signed Data mode
0 = AN13 is using Unsigned Data mode

bit 25 **DIFF12:** AN12 Mode bit
1 = Selects AN12 differential input pair as AN12+ and AN1-
0 = AN12 is using Single-ended mode

bit 24 **SIGN12:** AN12 Signed Data Mode bit
1 = AN12 is using Signed Data mode
0 = AN12 is using Unsigned Data mode

bit 23 **DIFF11:** AN11 Mode bit
1 = Selects AN11 differential input pair as AN11+ and AN1-
0 = AN11 is using Single-ended mode

bit 22 **SIGN11:** AN11 Signed Data Mode bit
1 = AN11 is using Signed Data mode
0 = AN11 is using Unsigned Data mode

REGISTER 25-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 21 **DIFF10:** AN10 Mode bit
1 = Selects AN10 differential input pair as AN10+ and AN1-
0 = AN10 is using Single-ended mode

bit 20 **SIGN10:** AN10 Signed Data Mode bit
1 = AN10 is using Signed Data mode
0 = AN10 is using Unsigned Data mode

bit 19 **DIFF9:** AN9 Mode bit
1 = Selects AN9 differential input pair as AN9+ and AN1-
0 = AN9 is using Single-ended mode

bit 18 **SIGN9:** AN9 Signed Data Mode bit
1 = AN9 is using Signed Data mode
0 = AN9 is using Unsigned Data mode

bit 17 **DIFF8:** AN 8 Mode bit
1 = Selects AN8 differential input pair as AN8+ and AN1-
0 = AN8 is using Single-ended mode

bit 16 **SIGN8:** AN8 Signed Data Mode bit
1 = AN8 is using Signed Data mode
0 = AN8 is using Unsigned Data mode

bit 15 **DIFF7:** AN7 Mode bit
1 = Selects AN7 differential input pair as AN7+ and AN1-
0 = AN7 is using Single-ended mode

bit 14 **SIGN7:** AN7 Signed Data Mode bit
1 = AN7 is using Signed Data mode
0 = AN7 is using Unsigned Data mode

bit 13 **DIFF6:** AN6 Mode bit
1 = Selects AN6 differential input pair as AN6+ and AN1-
0 = AN6 is using Single-ended mode

bit 12 **SIGN6:** AN6 Signed Data Mode bit
1 = AN6 is using Signed Data mode
0 = AN6 is using Unsigned Data mode

bit 11 **DIFF5:** AN5 Mode bit
1 = Selects AN5 differential input pair as AN5+ and AN11-
0 = AN5 is using Single-ended mode

bit 10 **SIGN5:** AN5 Signed Data Mode bit
1 = AN5 is using Signed Data mode
0 = AN5 is using Unsigned Data mode

bit 9 **DIFF4:** AN4 Mode bit
1 = Selects AN4 differential input pair as AN4+ and AN10-
0 = AN4 is using Single-ended mode

bit 8 **SIGN4:** AN4 Signed Data Mode bit
1 = AN4 is using Signed Data mode
0 = AN4 is using Unsigned Data mode

bit 7 **DIFF3:** AN3 Mode bit
1 = Selects AN3 differential input pair as AN3+ and AN27-
0 = AN3 is using Single-ended mode

bit 6 **SIGN3:** AN3 Signed Data Mode bit
1 = AN3 is using Signed Data mode
0 = AN3 is using Unsigned Data mode

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REGISTER 25-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 5 **DIFF2:** AN2 Mode bit
1 = Selects AN2 differential input pair as AN2+ and AN8-
0 = AN2 is using Single-ended mode

bit 4 **SIGN2:** AN2 Signed Data Mode bit
1 = AN2 is using Signed Data mode
0 = AN2 is using Unsigned Data mode

bit 3 **DIFF1:** AN1 Mode bit
1 = Selects AN1 differential input pair as AN1+ and AN7-
0 = AN1 is using Single-ended mode

bit 2 **SIGN1:** AN1 Signed Data Mode bit
1 = AN1 is using Signed Data mode
0 = AN1 is using Unsigned Data mode

bit 1 **DIFF0:** AN0 Mode bit
1 = Selects AN0 differential input pair as AN0+ and AN6-
0 = AN0 is using Single-ended mode

bit 0 **SIGN0:** AN0 Signed Data Mode bit
1 = AN0 is using Signed Data mode
0 = AN0 is using Unsigned Data mode

REGISTER 25-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF27	SIGN27	DIFF26	SIGN26	DIFF25	SIGN25	DIFF24	SIGN24
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF23(1)	SIGN23(1)	DIFF22(1)	SIGN22(1)	DIFF21(1)	SIGN21(1)	DIFF20(1)	SIGN20(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF19	SIGN19	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **DIFF27:** AN27 Mode bit
1 = Selects AN27 differential pair input as AN27+ and AN1-
0 = AN27 is using Single-ended mode

bit 22 **SIGN27:** AN27 Signed Data Mode bit
1 = AN27 is using Signed Data mode
0 = AN27 is using Unsigned Data mode

bit 21 **DIFF26:** AN26 Mode bit
1 = Selects AN26 differential pair input as AN26+ and AN1-
0 = AN26 is using Single-ended mode

bit 20 **SIGN26:** AN26 Signed Data Mode bit
1 = AN26 is using Signed Data mode
0 = AN26 is using Unsigned Data mode

bit 19 **DIFF25:** AN25 Mode bit
1 = Selects AN25 differential pair input as AN25+ and AN1-
0 = AN25 is using Single-ended mode

bit 18 **SIGN25:** AN25 Signed Data Mode bit
1 = AN25 is using Signed Data mode
0 = AN25 is using Unsigned Data mode

bit 17 **DIFF24:** AN24 Mode bit
1 = Selects AN24 differential pair input as AN24+ and AN1-
0 = AN24 is using Single-ended mode

bit 16 **SIGN24:** AN24 Signed Data Mode bit
1 = AN24 is using Signed Data mode
0 = AN24 is using Unsigned Data mode

bit 15 **DIFF23:** AN23 Mode bit(1)
1 = Selects AN23 differential pair input as AN23+ and AN1-
0 = AN23 is using Single-ended mode

Note 1: This bit is not available on 64-pin devices.

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REGISTER 25-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2 (CONTINUED)

bit 14 **SIGN23:** AN23 Signed Data Mode bit(1)
1 = AN23 is using Signed Data mode
0 = AN23 is using Unsigned Data mode

bit 13 **DIFF22:** AN22 Mode bit(1)
1 = Selects AN22 differential pair input as AN22+ and AN1-
0 = AN22 is using Single-ended mode

bit 12 **SIGN22:** AN22 Signed Data Mode bit(1)
1 = AN22 is using Signed Data mode
0 = AN22 is using Unsigned Data mode

bit 11 **DIFF21:** AN21 Mode bit(1)
1 = Selects AN21 differential pair input as AN21+ and AN1-
0 = AN21 is using Single-ended mode

bit 10 **SIGN21:** AN21 Signed Data Mode bit(1)
1 = AN21 is using Signed Data mode
0 = AN21 is using Unsigned Data mode

bit 9 **DIFF20:** AN20 Mode bit(1)
1 = Selects AN20 differential pair input as AN20+ and AN1-
0 = AN20 is using Single-ended mode

bit 8 **SIGN20:** AN20 Signed Data Mode bit(1)
1 = AN20 is using Signed Data mode
0 = AN20 is using Unsigned Data mode

bit 7 **DIFF19:** AN19 Mode bit
1 = Selects AN19 differential pair input as AN19+ and AN1-
0 = AN19 is using Single-ended mode

bit 6 **SIGN19:** AN19 Signed Data Mode bit
1 = AN19 is using Signed Data mode
0 = AN19 is using Unsigned Data mode

bit 5 **DIFF18:** AN18 Mode bit
1 = Selects AN18 differential pair input as AN18+ and AN1-
0 = AN18 is using Single-ended mode

bit 4 **SIGN18:** AN18 Signed Data Mode bit
1 = AN18 is using Signed Data mode
0 = AN18 is using Unsigned Data mode

bit 3 **DIFF17:** AN17 Mode bit
1 = Selects AN17 differential pair input as AN17+ and AN1-
0 = AN17 is using Single-ended mode

bit 2 **SIGN17:** AN17 Signed Data Mode bit
1 = AN17 is using Signed Data mode
0 = AN17 is using Unsigned Data mode

bit 1 **DIFF16:** AN16 Mode bit
1 = Selects AN16 differential pair input as AN16+ and AN1-
0 = AN16 is using Single-ended mode

bit 0 **SIGN16:** AN16 Signed Data Mode bit
1 = AN16 is using Signed Data mode
0 = AN16 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	DIFF47(1)	SIGN47(1)	DIFF46(1)	SIGN46(1)	DIFF45(1)	SIGN45(1)	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DIFF41(1)	SIGN41(1)	DIFF40(1)	SIGN40(1)
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF39(1)	SIGN39(1)	DIFF38(1)	SIGN38(1)	DIFF37(1)	SIGN37(1)	DIFF36(1)	SIGN36(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	DIFF35(1)	SIGN35(1)	DIFF34(1)	SIGN34(1)	DIFF33(1)	SIGN33(1)	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DIFF47:** AN47 Mode bit(1)
1 = Selects AN47 differential input pair as AN47+ and AN1-
0 = AN47 is using Single-ended mode

bit 30 **SIGN47:** AN47 Signed Data Mode bit(1)
1 = AN41 is using Signed Data mode
0 = AN41 is using Unsigned Data mode

bit 29 **DIFF46:** AN46 Mode bit(1)
1 = Selects AN46 differential input pair as AN46+ and AN1-
0 = AN41 is using Single-ended mode

bit 28 **SIGN46:** AN46 Signed Data Mode bit(1)
1 = AN46 is using Signed Data mode
0 = AN46 is using Unsigned Data mode

bit 27 **DIFF45:** AN45 Mode bit(1)
1 = Selects AN45 differential input pair as AN45+ and AN1-
0 = AN45 is using Single-ended mode

bit 26 **SIGN46:** AN45 Signed Data Mode bit(1)
1 = AN45 is using Signed Data mode
0 = AN45 is using Unsigned Data mode

bit 25-20 **Unimplemented:** Read as '0'

bit 19 **DIFF41:** AN41 Mode bit(1)
1 = Selects AN41 differential input pair as AN41+ and AN1-
0 = AN41 is using Single-ended mode

bit 18 **SIGN41:** AN41 Signed Data Mode bit(1)
1 = AN41 is using Signed Data mode
0 = AN41 is using Unsigned Data mode

bit 17 **DIFF40:** AN40 Mode bit(1)
1 = Selects AN40 differential input pair as AN40+ and AN1-
0 = AN40 is using Single-ended mode

bit 16 **SIGN40:** AN40 Signed Data Mode bit(1)
1 = AN40 is using Signed Data mode
0 = AN40 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

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REGISTER 25-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3 (CONTINUED)

bit 15 **DIFF39:** AN39 Mode bit(1)
1 = Selects AN39 differential input pair as AN39+ and AN1-
0 = AN39 is using Single-ended mode

bit 14 **SIGN39:** AN39 Signed Data Mode bit(1)
1 = AN39 is using Signed Data mode
0 = AN39 is using Unsigned Data mode

bit 13 **DIFF38:** AN38 Mode bit(1)
1 = Selects AN38 differential input pair as AN38+ and AN1-
0 = AN38 is using Single-ended mode

bit 12 **SIGN38:** AN38 Signed Data Mode bit(1)
1 = AN38 is using Signed Data mode
0 = AN38 is using Unsigned Data mode

bit 11 **DIFF37:** AN37 Mode bit(1)
1 = Selects AN37 differential input pair as AN37+ and AN1-
0 = AN37 is using Single-ended mode

bit 10 **SIGN37:** AN37 Signed Data Mode bit(1)
1 = AN37 is using Signed Data mode
0 = AN37 is using Unsigned Data mode

bit 9 **DIFF36:** AN36 Mode bit(1)
1 = Selects AN36 differential input pair as AN36+ and AN1-
0 = AN36 is using Single-ended mode

bit 8 **SIGN36:** AN36 Signed Data Mode bit(1)
1 = AN36 is using Signed Data mode
0 = AN36 is using Unsigned Data mode

bit 7 **DIFF35:** AN35 Mode bit(1)
1 = Selects AN35 differential input pair as AN35+ and AN1-
0 = AN35 is using Single-ended mode

bit 6 **SIGN35:** AN35 Signed Data Mode bit(1)
1 = AN35 is using Signed Data mode
0 = AN35 is using Unsigned Data mode

bit 5 **DIFF34:** AN34 Mode bit(1)
1 = Selects AN34 differential input pair as AN34+ and AN1-
0 = AN34 is using Single-ended mode

bit 4 **SIGN34:** AN34 Signed Data Mode bit(1)
1 = AN34 is using Signed Data mode
0 = AN34 is using Unsigned Data mode

bit 3 **DIFF33:** AN33 Mode bit(1)
1 = Selects AN33 differential input pair as AN33+ and AN1-
0 = AN33 is using Single-ended mode

bit 2 **SIGN33:** AN33 Signed Data Mode bit(1)
1 = AN33 is using Signed Data mode
0 = AN33 is using Unsigned Data mode

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-8: ADCIMCON4: ADC INPUT MODE CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DIFF49	SIGN49	DIFF48	SIGN48

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **DIFF49:** AN49 Mode bit
1 = Selects AN49 differential input pair as AN49+ and AN1-
0 = AN49 is using Single-ended mode

bit 2 **SIGN49:** AN41 Signed Data Mode bit
1 = AN49 is using Signed Data mode
0 = AN49 is using Unsigned Data mode

bit 1 **DIFF48:** AN48 Mode bit
1 = Selects AN40 differential input pair as AN48+ and AN1-
0 = AN48 is using Single-ended mode

bit 0 **SIGN48:** AN48 Signed Data Mode bit
1 = AN48 is using Signed Data mode
0 = AN48 is using Unsigned Data mode

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REGISTER 25-9: ADCGIRQEN1: ADC GLOBAL INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AGIEN27	AGIEN26	AGIEN25	AGIEN24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN23(1)	AGIEN22(1)	AGIEN21(1)	AGIEN20(1)	AGIEN19	AGIEN18	AGIEN17	AGIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AGIEN27:AGIEN0:** ADC Global Interrupt Enable bits

1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the AIRDY*x* bit of the ADCDSTAT1 register)

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-10: ADCGIRQEN2: ADC GLOBAL INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	AGIEN53	AGIEN52	AGIEN51	AGIEN50	AGIEN49	AGIEN48
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	AGIEN47(1)	AGIEN46(1)	AGIEN45(1)	—	—	—	AGIEN41(1)	AGIEN40(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	AGIEN39(1)	AGIEN38(1)	AGIEN37(1)	AGIEN36(1)	AGIEN35(1)	AGIEN34(1)	AGIEN33(1)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-13 **AGIEN53:AGIEN45** ADC Global Interrupt Enable bits
1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the AIRDY*x* bit of the ADCDSTAT2 register)
0 = Interrupts are disabled

bit 12-10 **Unimplemented:** Read as '0'

bit 9-1 **AGIEN41:AGIEN33** ADC Global Interrupt Enable bits
1 = Interrupts are enabled for the selected analog input. The interrupt is generated after the converted data is ready (indicated by the AIRDY*x* bit of the ADCDSTAT2 register)
0 = Interrupts are disabled

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

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REGISTER 25-11: ADCCSS1: ADC COMMON SCAN SELECT REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CSS27	CSS26	CSS25	CSS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS23(1)	CSS22(1)	CSS21(1)	CSS20(1)	CSS19	CSS18	CSS17	CSS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **CSS27:CSS0:** Analog Common Scan Select bits

Analog inputs AN27-AN6 are always Class 3 shared ADC7.

1 = Select AN*x* for input scan (i.e., ANx = CSSx and scan is sequential starting with the lowest to highest enabled CSSx analog input pin)
0 = Skip AN*x* for input scan

Note 1: This bit is not available on 64-pin devices.

Note 1: In addition to setting the appropriate bits in this register, Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSS*x* bits. Refer to the bit descriptions in the ADCTRGx registers for selecting the STRIG option.

2: If a Class 1 or Class 2 input is included in the scan by setting the CSSx bit to '1' and by setting the TRGSRCx<4:0> bits to STRIG mode ('0b11), the user application must ensure that no other triggers are generated for that input using the RQCNVRT bit in the ADCCON3 register or the hardware input or any digital filter. Otherwise, the scan behavior is unpredictable.

REGISTER 25-12: ADCCSS2: ADC COMMON SCAN SELECT REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	CSS53(2)	CSS52(2)	—	CSS50(2)	CSS49	CSS48
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	CSS47(1)	CSS46(1)	CSS45(1)	—	—	—	CSS41(1)	CSS40(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	CSS39(1)	CSS38(1)	CSS37(1)	CSS36(1)	CSS35(1)	CSS34(1)	CSS33(1)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-20 **CSS53:CSS52:** Analog Common Scan Select bits
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

bit 19 **Unimplemented:** Read as '0'

bit 21-20 **CSS50:CSS45:** Analog Common Scan Select bits
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

bit 9-1 **CSS41:CSS33:** Analog Common Scan Select bits
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.
2: CSS50-CSS53 are internal analog inputs with respect to (IVREF, IVREF Temp, VBAT/2, and CTMU Temp).

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REGISTER 25-13: ADCDSTAT1: ADC DATA READY STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	AIRDY27	AIRDY26	AIRDY25	AIRDY24
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY23(1)	AIRDY22(1)	AIRDY21(1)	AIRDY20(1)	AIRDY19	AIRDY18	AIRDY17	AIRDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY15	AIRDY14	AIRDY13	AIRDY12	AIRDY11	AIRDY10	AIRDY9	AIRDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	AIRDY7	AIRDY6	AIRDY5	AIRDY4	AIRDY3	AIRDY2	AIRDY1	AIRDY0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AIRDY27:AIRDY0:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register

0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-14: ADCDSTAT2: ADC DATA READY STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	AIRDY53	AIRDY52	AIRDY51	AIRDY50	AIRDY49	AIRDY48
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	AIRDY47(1)	AIRDY46(1)	AIRDY45(1)	—	—	—	AIRDY41(1)	AIRDY40(1)
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0
	AIRDY39(1)	AIRDY38(1)	AIRDY37(1)	AIRDY36(1)	AIRDY35(1)	AIRDY34(1)	AIRDY33(1)	—

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 23-13 **AIRDY53:AIRDY45:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register

0 = This bit is cleared when the associated data register is read

bit 12-10 **Unimplemented:** Read as '0'

bit 23-13 **AIRDY41:AIRDY33:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register

0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-15: ADCCMPENx: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER ('x' = 1 THROUGH 4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CMPE27	CMPE26	CMPE25	CMPE24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19	CMPE18	CMPE17	CMPE16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **CMPE27:CMPE0:** ADC Digital Comparator 'x' Enable bits

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: This bit is not available on 64-pin devices.

Note 1: CMPE*x* = AN*x*, where 'x' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).

2: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

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REGISTER 25-16: ADCCMPx: ADC DIGITAL COMPARATOR 'x' LIMIT VALUE REGISTER ('x' = 1 THROUGH 4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<15:8>(1,2,3)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPHI<7:0>(1,2,3)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<15:8>(1,2,3)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCMPLO<7:0>(1,2,3)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **DCMPHI<15:0>:** Digital Comparator 'x' High Limit Value bits(1,2,3)
These bits store the high limit value, which is used by digital comparator for comparisons with ADC converted data.

bit 15-0 **DCMPLO<15:0>:** Digital Comparator 'x' Low Limit Value bits(1,2,3)
These bits store the low limit value, which is used by digital comparator for comparisons with ADC converted data.

Note 1: Changing theses bits while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

2: The format of the limit values should match the format of the ADC converted value in terms of sign and fractional settings.

3: For Digital Comparator 0 used in CVD mode, the DCMPHI<15:0> and DCMPLO<15:0> bits must always be specified in signed format, as the CVD output data is differential and is always signed.

REGISTER 25-17: ADCFLTRx: ADC DIGITAL FILTER 'x' REGISTER ('x' = 1 THROUGH 6)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC
	AFEN	DATA16EN	DFMODE	OVRSAM<2:0>			AFGIEN	AFRDY
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CHNLID<4:0>				
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	FLTRDATA<15:8>							
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	FLTRDATA<7:0>							

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **AFEN:** Digital Filter 'x' Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled and the AFRDY status bit is cleared

bit 30 **DATA16EN:** Filter Significant Data Length bit
1 = All 16 bits of the filter output data are significant
0 = Only the first 12 bits are significant, followed by four zeros
Note: This bit is significant only if DFMODE = 1 (Averaging Mode) and FRACT (ADCCON1<23>) = 1 (Fractional Output Mode).

bit 29 **DFMODE:** ADC Filter Mode bit
1 = Filter 'x' works in Averaging mode
0 = Filter 'x' works in Oversampling Filter mode (default)

bit 28-26 **OVRSAM<2:0>:** Oversampling Filter Ratio bits
If DFMODE is '0':
111 = 128 samples (shift sum 3 bits to right, output data is in 15.1 format)
110 = 32 samples (shift sum 2 bits to right, output data is in 14.1 format)
101 = 8 samples (shift sum 1 bit to right, output data is in 13.1 format)
100 = 2 samples (shift sum 0 bits to right, output data is in 12.1 format)
011 = 256 samples (shift sum 4 bits to right, output data is 16 bits)
010 = 64 samples (shift sum 3 bits to right, output data is 15 bits)
001 = 16 samples (shift sum 2 bits to right, output data is 14 bits)
000 = 4 samples (shift sum 1 bit to right, output data is 13 bits)

If DFMODE is '1':
111 = 256 samples (256 samples to be averaged)
110 = 128 samples (128 samples to be averaged)
101 = 64 samples (64 samples to be averaged)
100 = 32 samples (32 samples to be averaged)
011 = 16 samples (16 samples to be averaged)
010 = 8 samples (8 samples to be averaged)
001 = 4 samples (4 samples to be averaged)
000 = 2 samples (2 samples to be averaged)

bit 25 **AFGIEN:** Digital Filter 'x' Interrupt Enable bit
1 = Digital filter interrupt is enabled and is generated by the AFRDY status bit
0 = Digital filter is disabled

Note 1: This selection is not available on 64-pin devices.

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REGISTER 25-17: ADCFLTRx: ADC DIGITAL FILTER 'x' REGISTER ('x' = 1 THROUGH 6) (CONTINUED)

bit 24 **AFRDY:** Digital Filter 'x' Data Ready Status bit
1 = Data is ready in the FLTRDATA<15:0> bits
0 = Data is not ready

Note: This bit is cleared by reading the FLTRDATA<15:0> bits or by disabling the Digital Filter module (by setting AFEN to '0').

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **CHNLID<4:0>:** Digital Filter Analog Input Selection bits
These bits specify the analog input to be used as the oversampling filter data source.
11111 = Reserved
•
•
•
11100 = Reserved
11011 = AN27 input
11010 = AN26 input
11001 = AN25 input
11000 = AN24 input
10111 = AN23(1) input
10110 = AN22(1) input
10101 = AN21(1) input
10100 = AN20(1) input
10011 = AN19 input
•
•
•
10110 = AN6 input
00101 = ADC5 Module
00100 = ADC4 Module
00011 = ADC3 Module
00010 = ADC2 Module
00001 = ADC1 Module
00000 = ADC0 Module

Note: Only the first 32 analog inputs (Class 1 and Class 2) can use a digital filter.

bit 15-0 **FLTRDATA<15:0>:** Digital Filter 'x' Data Output Value bits
The filter output data is as per the fractional format set in the FRACT (ADCCON1<23>) bit. The FRACT bit should not be changed while the filter is enabled. Changing the state of the FRACT bit after the operation of the filter ended will not update the value of FLTRDATA<15:0> to reflect the new format.

Note 1: This selection is not available on 64-pin devices.

REGISTER 25-18: ADCTRG1: ADC TRIGGER SOURCE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC3<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC2<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC1<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC3<4:0>:** Trigger Source for Conversion of ADC3 Module Select bits
11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control Variants Only)
11100 = PWM Generator 5 Current-Limit (Motor Control Variants Only)
11011 = PWM Generator 4 Current-Limit (Motor Control Variants Only)
11010 = PWM Generator 3 Current-Limit (Motor Control Variants Only)
11001 = PWM Generator 2 Current-Limit (Motor Control Variants Only)
11000 = PWM Generator 1 Current-Limit (Motor Control Variants Only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 (Rising Edge Only)
10010 = Output Compare 3 (Rising Edge Only)
10001 = Output Compare 2 (Rising Edge Only)
10000 = Output Compare 1 (Rising Edge Only)
01111 = PWM Generator 6 trigger (Motor Control Variants Only)
01110 = PWM Generator 5 trigger (Motor Control Variants Only)
01101 = PWM Generator 4 trigger (Motor Control Variants Only)
01100 = PWM Generator 3 trigger (Motor Control Variants Only)
01011 = PWM Generator 2 trigger (Motor Control Variants Only)
01010 = PWM Generator 1 trigger (Motor Control Variants Only)
01001 = Secondary Special Event trigger (Motor Control Variants Only)
01000 = Primary Special Event trigger (Motor Control Variants Only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger (see **Note**)
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

bit 23-21 **Unimplemented:** Read as '0'

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REGISTER 25-18: ADCTRG1: ADC TRIGGER SOURCE 1 REGISTER

bit 20-16 **TRGSRC2<4:0>:** Trigger Source for Conversion of ADC2 Module Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC1<4:0>:** Trigger Source for Conversion of ADC1 Module Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC0<4:0>:** Trigger Source for Conversion of ADC0 Module Select bits
See bits 28-24 for bit value definitions.

REGISTER 25-19: ADCTRG2: ADC TRIGGER SOURCE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC7<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC6<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC5<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC4<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC7<4:0>:** Trigger Source for Conversion of Analog Input AN7 Select bits
11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control Variants Only)
11100 = PWM Generator 5 Current-Limit (Motor Control Variants Only)
11011 = PWM Generator 4 Current-Limit (Motor Control Variants Only)
11010 = PWM Generator 3 Current-Limit (Motor Control Variants Only)
11001 = PWM Generator 2 Current-Limit (Motor Control Variants Only)
11000 = PWM Generator 1 Current-Limit (Motor Control Variants Only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 (Rising Edge Only)
10010 = Output Compare 3 (Rising Edge Only)
10001 = Output Compare 2 (Rising Edge Only)
10000 = Output Compare 1 (Rising Edge Only)
01111 = PWM Generator 6 trigger (Motor Control Variants Only)
01110 = PWM Generator 5 trigger (Motor Control Variants Only)
01101 = PWM Generator 4 trigger (Motor Control Variants Only)
01100 = PWM Generator 3 trigger (Motor Control Variants Only)
01011 = PWM Generator 2 trigger (Motor Control Variants Only)
01010 = PWM Generator 1 trigger (Motor Control Variants Only)
01001 = Secondary Special Event trigger (Motor Control Variants Only)
01000 = Primary Special Event trigger (Motor Control Variants Only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger (see **Note**)
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

bit 23-21 **Unimplemented:** Read as '0'

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REGISTER 25-19: ADCTRG2: ADC TRIGGER SOURCE 2 REGISTER

bit 20-16 **TRGSRC6<4:0>:** Trigger Source for Conversion of Analog Input AN6 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC5<4:0>:** Trigger Source for Conversion of ADC5 Module Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC4<4:0>:** Trigger Source for Conversion of ADC4 Module Select bits
See bits 28-24 for bit value definitions.

REGISTER 25-20: ADCTRG3: ADC TRIGGER SOURCE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC11<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC10<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC9<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC8<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC11<4:0>:** Trigger Source for Conversion of Analog Input AN11 Select bits
11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control only)
11100 = PWM Generator 5 Current-Limit (Motor Control only)
11011 = PWM Generator 4 Current-Limit (Motor Control only)
11010 = PWM Generator 3 Current-Limit (Motor Control only)
11001 = PWM Generator 2 Current-Limit (Motor Control only)
11000 = PWM Generator 1 Current-Limit (Motor Control only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 (Rising Edge Only)
10010 = Output Compare 3 (Rising Edge Only)
10001 = Output Compare 2 (Rising Edge Only)
10000 = Output Compare 1 (Rising Edge Only)
01111 = PWM Generator 6 trigger (Motor Control only)
01110 = PWM Generator 5 trigger (Motor Control only)
01101 = PWM Generator 4 trigger (Motor Control only)
01100 = PWM Generator 3 trigger (Motor Control only)
01011 = PWM Generator 2 trigger (Motor Control only)
01010 = PWM Generator 1 trigger (Motor Control only)
01001 = Secondary Special Event trigger (Motor Control only)
01000 = Primary Special Event trigger (Motor Control only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger (see **Note**)
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

bit 23-21 **Unimplemented:** Read as '0'

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REGISTER 25-20: ADCTRG3: ADC TRIGGER SOURCE 3 REGISTER

bit 20-16 **TRGSRC10<4:0>:** Trigger Source for Conversion of Analog Input AN10 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC9<4:0>:** Trigger Source for Conversion of Analog Input AN9 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC8<4:0>:** Trigger Source for Conversion of Analog Input AN8 Select bits
See bits 28-24 for bit value definitions.

REGISTER 25-21: ADCTRG4: ADC TRIGGER SOURCE 4 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC15<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC14<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC13<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC12<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC15<4:0>:** Trigger Source for Conversion of Analog Input AN15 Select bits
11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control only)
11100 = PWM Generator 5 Current-Limit (Motor Control only)
11011 = PWM Generator 4 Current-Limit (Motor Control only)
11010 = PWM Generator 3 Current-Limit (Motor Control only)
11001 = PWM Generator 2 Current-Limit (Motor Control only)
11000 = PWM Generator 1 Current-Limit (Motor Control only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 (Rising Edge Only)
10010 = Output Compare 3 (Rising Edge Only)
10001 = Output Compare 2 (Rising Edge Only)
10000 = Output Compare 1 (Rising Edge Only)
01111 = PWM Generator 6 trigger (Motor Control only)
01110 = PWM Generator 5 trigger (Motor Control only)
01101 = PWM Generator 4 trigger (Motor Control only)
01100 = PWM Generator 3 trigger (Motor Control only)
01011 = PWM Generator 2 trigger (Motor Control only)
01010 = PWM Generator 1 trigger (Motor Control only)
01001 = Secondary Special Event trigger (Motor Control only)
01000 = Primary Special Event trigger (Motor Control only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger (see **Note**)
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

bit 23-21 **Unimplemented:** Read as '0'

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REGISTER 25-21: ADCTRG4: ADC TRIGGER SOURCE 4 REGISTER

bit 20-16 **TRGSRC14<4:0>:** Trigger Source for Conversion of Analog Input AN14 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC13<4:0>:** Trigger Source for Conversion of Analog Input AN13 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC12<4:0>:** Trigger Source for Conversion of Analog Input AN12 Select bits
See bits 28-24 for bit value definitions.

REGISTER 25-22: ADCTRG5: ADC TRIGGER SOURCE 5 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC19<4:0>(1)				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC18<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC17<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC16<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC19<4:0>:** Trigger Source for Conversion of Analog Input AN19 Select bits
11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control only)
11100 = PWM Generator 5 Current-Limit (Motor Control only)
11011 = PWM Generator 4 Current-Limit (Motor Control only)
11010 = PWM Generator 3 Current-Limit (Motor Control only)
11001 = PWM Generator 2 Current-Limit (Motor Control only)
11000 = PWM Generator 1 Current-Limit (Motor Control only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 (Rising Edge only)
10010 = Output Compare 3 (Rising Edge only)
10001 = Output Compare 2 (Rising Edge only)
10000 = Output Compare 1 (Rising Edge only)
01111 = PWM Generator 6 trigger (Motor Control only)
01110 = PWM Generator 5 trigger (Motor Control only)
01101 = PWM Generator 4 trigger (Motor Control only)
01100 = PWM Generator 3 trigger (Motor Control only)
01011 = PWM Generator 2 trigger (Motor Control only)
01010 = PWM Generator 1 trigger (Motor Control only)
01001 = Secondary Special Event trigger (Motor Control only)
01000 = Primary Special Event trigger (Motor Control only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger (see **Note**)
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

Note 1: These bits are not available on 64-pin devices.

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REGISTER 25-22: ADCTRG5: ADC TRIGGER SOURCE 5 REGISTER

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC18<4:0>:** Trigger Source for Conversion of Analog Input AN18 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC17<4:0>:** Trigger Source for Conversion of Analog Input AN17 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC16<4:0>:** Trigger Source for Conversion of Analog Input AN16 Select bits
See bits 28-24 for bit value definitions.

Note 1: These bits are not available on 64-pin devices.

REGISTER 25-23: ADCTRG6: ADC TRIGGER SOURCE 6 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC23<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC22<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC21<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC20<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC23<4:0>:** Trigger Source for Conversion of Analog Input AN23 Select bits
11111 = Reserved
11110 = Reserved
11101 = PWM Generator 6 Current-Limit (Motor Control only)
11100 = PWM Generator 5 Current-Limit (Motor Control only)
11011 = PWM Generator 4 Current-Limit (Motor Control only)
11010 = PWM Generator 3 Current-Limit (Motor Control only)
11001 = PWM Generator 2 Current-Limit (Motor Control only)
11000 = PWM Generator 1 Current-Limit (Motor Control only)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = CTMU trip
10011 = Output Compare 4 (Rising Edge only)
10010 = Output Compare 3 (Rising Edge only)
10001 = Output Compare 2 (Rising Edge only)
10000 = Output Compare 1 (Rising Edge only)
01111 = PWM Generator 6 trigger (Motor Control only)
01110 = PWM Generator 5 trigger (Motor Control only)
01101 = PWM Generator 4 trigger (Motor Control only)
01100 = PWM Generator 3 trigger (Motor Control only)
01011 = PWM Generator 2 trigger (Motor Control only)
01010 = PWM Generator 1 trigger (Motor Control only)
01001 = Secondary Special Event trigger (Motor Control only)
01000 = Primary Special Event trigger (Motor Control only)
00111 = General Purpose Timer5
00110 = General Purpose Timer3
00101 = General Purpose Timer1
00100 = INT0
00011 = Scan trigger (see the following **Note**)
00010 = Software level trigger
00001 = Software edge trigger
00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

Note: This register is not available on 64-pin devices.

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REGISTER 25-23: ADCTRG6: ADC TRIGGER SOURCE 6 REGISTER

bit 23-21	**Unimplemented:** Read as '0'
bit 20-16	**TRGSRC22<4:0>:** Trigger Source for Conversion of Analog Input AN22 Select bits See bits 28-24 for bit value definitions.
bit 15-13	**Unimplemented:** Read as '0'
bit 12-8	**TRGSRC21<4:0>:** Trigger Source for Conversion of Analog Input AN21 Select bits See bits 28-24 for bit value definitions.
bit 7-5	**Unimplemented:** Read as '0'
bit 4-0	**TRGSRC20<4:0>:** Trigger Source for Conversion of Analog Input AN20 Select bits See bits 28-24 for bit value definitions.

Note: This register is not available on 64-pin devices.

REGISTER 25-24: ADCTRG7: ADC TRIGGER SOURCE 7 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC27<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC26<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC25<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC24<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC27<4:0>:** Trigger Source for Conversion of Analog Input AN27 Select bits
- 11111 = Reserved
- 11110 = Reserved
- 11101 = PWM Generator 6 Current-Limit (Motor Control only)
- 11100 = PWM Generator 5 Current-Limit (Motor Control only)
- 11011 = PWM Generator 4 Current-Limit (Motor Control only)
- 11010 = PWM Generator 3 Current-Limit (Motor Control only)
- 11001 = PWM Generator 2 Current-Limit (Motor Control only)
- 11000 = PWM Generator 1 Current-Limit (Motor Control only)
- 10111 = Reserved
- 10110 = Reserved
- 10101 = Reserved
- 10100 = CTMU trip
- 10011 = Output Compare 4 (Rising Edge only)
- 10010 = Output Compare 3 (Rising Edge only)
- 10001 = Output Compare 2 (Rising Edge only)
- 10000 = Output Compare 1 (Rising Edge only)
- 01111 = PWM Generator 6 trigger (Motor Control only)
- 01110 = PWM Generator 5 trigger (Motor Control only)
- 01101 = PWM Generator 4 trigger (Motor Control only)
- 01100 = PWM Generator 3 trigger (Motor Control only)
- 01011 = PWM Generator 2 trigger (Motor Control only)
- 01010 = PWM Generator 1 trigger (Motor Control only)
- 01001 = Secondary Special Event trigger (Motor Control only)
- 01000 = Primary Special Event trigger (Motor Control only)
- 00111 = General Purpose Timer5
- 00110 = General Purpose Timer3
- 00101 = General Purpose Timer1
- 00100 = INT0
- 00011 = Scan trigger (see **Note**)
- 00010 = Software level trigger
- 00001 = Software edge trigger
- 00000 = No Trigger

Note: For Scan Trigger, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSSx registers.

Note: This register is not available on 64-pin devices.

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REGISTER 25-24: ADCTRG7: ADC TRIGGER SOURCE 7 REGISTER

bit 23-21	**Unimplemented:** Read as '0'
bit 20-16	**TRGSRC26<4:0>:** Trigger Source for Conversion of Analog Input AN26 Select bits See bits 28-24 for bit value definitions.
bit 15-13	**Unimplemented:** Read as '0'
bit 12-8	**TRGSRC25<4:0>:** Trigger Source for Conversion of Analog Input AN25 Select bits See bits 28-24 for bit value definitions.
bit 7-5	**Unimplemented:** Read as '0'
bit 4-0	**TRGSRC24<4:0>:** Trigger Source for Conversion of Analog Input AN24 Select bits See bits 28-24 for bit value definitions.

Note: This register is not available on 64-pin devices.

REGISTER 25-25: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	CVDDATA<15:8>							
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	CVDDATA<7:0>							
15:8	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	AINID<5:0>					
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CVDDATA<15:0>:** CVD Data Status bits
In CVD mode, these bits obtain the CVD differential output data (subtraction of CVD positive and negative measurement), whenever a Digital Comparator interrupt is generated. The value in these bits is compliant with the FRACT bit (ADCCON1<23>) and is always signed.

bit 15-14 **Unimplemented:** Read as '0'

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REGISTER 25-25: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

bit 13-8 **AINID<5:0>:** Digital Comparator 1 Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by Digital Comparator 1.

In normal ADC mode, only analog inputs <31:0> can be processed by the Digital Comparator 1. The Digital Comparator 1 also supports the CVD mode, in which all Class 2 and Class 3 analog inputs may be stored in the AINID<5:0> bits.

111111 = Reserved
•
•
•
110110 = Reserved
110101 = Internal AN53 (CTMU temperature sensor)
110101 = Internal AN52 (VBAT/2)
110101 = Reserved
110010 = Internal AN50 (IVREF 1.2V)
110001 = AN49 is being monitored
•
•
•
101101 = AN45 is being monitored
101100 = Reserved
•
•
•
101010 = Reserved
101001 = AN41 is being monitored
•
•
•
100001 = AN33 is being monitored
111100 = Reserved
•
•
•
111000 = Reserved
111011 = AN27 is being monitored
•
•
•
000000 = AN0 is being monitored

Note: For 64-pin devices AN20-AN23 and AN33-AN47 inputs are not implemented.

bit 7 **ENDCMP:** Digital Comparator 1 Enable bit
1 = Digital Comparator 1 is enabled
0 = Digital Comparator 1 is not enabled, and the DCMPED status bit (ADCCMP0CON<5>) is cleared

bit 6 **DCMPGIEN:** Digital Comparator 1 Global Interrupt Enable bit
1 = A Digital Comparator 1 interrupt is generated when the DCMPED status bit (ADCCMP0CON<5>) is set
0 = A Digital Comparator 1 interrupt is disabled

bit 5 **DCMPED:** Digital Comparator 1 "Output True" Event Status bit
The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI, and IELOLO bits.

Note: This bit is cleared by reading the AINID<5:0> bits or by disabling the Digital Comparator module (by setting ENDCMP to '0').

1 = Digital Comparator 1 output true event has occurred (output of Comparator is '1')
0 = Digital Comparator 1 output is false (output of comparator is '0')

bit 4 **IEBTWN:** Between Low/High Digital Comparator 1 Event bit
1 = Generate a digital comparator event when DCMPLO<15:0> ≤ DATA<31:0> < DCMPHI<15:0>
0 = Do not generate a digital comparator event

REGISTER 25-25: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

bit 3 **IEHIHI:** High/High Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when DCMPHI<15:0> ≤ DATA<31:0>
0 = Do not generate an event

bit 2 **IEHILO:** High/Low Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when DATA<31:0> < DCMPHI<15:0>
0 = Do not generate an event

bit 1 **IELOHI:** Low/High Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when DCMPLO<15:0> ≤ DATA<31:0>
0 = Do not generate an event

bit 0 **IELOLO:** Low/Low Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when DATA<31:0> < DCMPLO<15:0>
0 = Do not generate an event

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REGISTER 25-26: ADCCMPCONx: ADC DIGITAL COMPARATOR 'x' CONTROL REGISTER ('x' = 2 THROUGH 4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	AINID<4:0>				
7:0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ENDCMP	DCMPGIEN	DCMPED	IEBTWN	IEHIHI	IEHILO	IELOHI	IELOLO

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **AINID<4:0>:** Digital Comparator 'x' Analog Input Identification (ID) bits

When a digital comparator event occurs (DCMPED = 1), these bits identify the analog input being monitored by the Digital Comparator.

Note: Only analog inputs <27:0> can be processed by the Digital Comparator module 'x' ('x' = 2-4).

11111 = Reserved
•
•
•
11100 = Reserved
11011 = AN27
11010 = AN26
11001 = AN25
11000 = AN24
10111 = AN23(1)
10110 = AN22(1)
10101 = AN21(1)
10100 = AN20(1)
10011 = AN19
•
•
•
00001 = AN1
00000 = AN0

bit 7 **ENDCMP:** Digital Comparator 'x' Enable bit

1 = Digital Comparator 'x' is enabled
0 = Digital Comparator 'x' is not enabled, and the DCMPED status bit (ADCCMP*x*CON<5>) is cleared

bit 6 **DCMPGIEN:** Digital Comparator 'x' Global Interrupt Enable bit

1 = A Digital Comparator 'x' interrupt is generated when the DCMPED status bit (ADCCMP*x*CON<5>) is set
0 = A Digital Comparator 'x' interrupt is disabled

Note 1: This setting is not available on 64-pin devices.

REGISTER 25-26: ADCCMPCONx: ADC DIGITAL COMPARATOR 'x' CONTROL REGISTER ('x' = 2 THROUGH 4) (CONTINUED)

bit 5 **DCMPED:** Digital Comparator 'x' "Output True" Event Status bit

The logical conditions under which the digital comparator gets "True" are defined by the IEBTWN, IEHIHI, IEHILO, IELOHI and IELOLO bits.

This bit is cleared by reading the AINID<5:0> bits (ADCCMPCONx<13:8>) or by disabling the Digital Comparator module (by setting ENDCMP to '0').

1 = Digital Comparator 'x' output true event has occurred (output of Comparator is '1')
0 = Digital Comparator 'x' output is false (output of Comparator is '0')

bit 4 **IEBTWN:** Between Low/High Digital Comparator 'x' Event bit

1 = Generate a digital comparator event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate a digital comparator event

bit 3 **IEHIHI:** High/High Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DCMPHI<15:0> bits ≤ DATA<31:0> bits
0 = Do not generate an event

bit 2 **IEHILO:** High/Low Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DATA<31:0> bits < DCMPHI<15:0> bits
0 = Do not generate an event

bit 1 **IELOHI:** Low/High Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DCMPLO<15:0> bits ≤ DATA<31:0> bits
0 = Do not generate an event

bit 0 **IELOLO:** Low/Low Digital Comparator 'x' Event bit

1 = Generate a Digital Comparator 'x' Event when the DATA<31:0> bits < DCMPLO<15:0> bits
0 = Do not generate an event

Note 1: This setting is not available on 64-pin devices.

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REGISTER 25-27: ADCBASE: ADC BASE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **Unimplemented:** Read as '0'

bit 15-0 **ADCBASE<15:0>:** ADC ISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS<2:0> bits of the ADCCON1 register specifying the amount of left shift done to the AIRDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active analog input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

REGISTER 25-28: ADCDSTAT: ADC DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMAEN	---	RBFIE5	RBFIE4	RBFIE3	RBFIE2	RBFIE1	RBFIE0
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	WOVERR	---	RBF5	RBF4	RBF3	RBF2	RBF1	RBF0
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DMACEN	---	RAFIE5	RAFIE4	RAFIE3	RAFIE2	RAFIE1	RAFIE0
7:0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	---	---	RAF5	RAF4	RAF3	RAF2	RAF1	RAF0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DMAEN:** Global ADC DMA Enable bit
1 = DMA interface is enabled
0 = DMA interface is disabled
When DMAEN = 0, no data is being saved into internal SRAM, no SRAM Writes occur and the DMA interface logic is being kept in reset state.

Note: Before setting the DMAEN bit to '1', the user application must ensure that the BCHEN bit (ADCxTIME<23>) is configured as needed.

bit 30 **Unimplemented:** Read as '0'

bit 29-24 **RBFIE5:RBFIE0:** RAM DMA Buffer B Full Interrupt Enable bits for ADC5-ADC0
1 = Enable ping-pong DMA Buffer B interrupt requests for ADC5-ADC0
0 = Disable ping-pong DMA Buffer B interrupt requests for ADC5-ADC0

bit 23 **WOVERR:** DMA Transfer Error
This bit is set by hardware and cleared by hardware after a software read of the ADCDSTAT register. If this bit is set the ADC conversion results transferred by DMA are erroneous. Recommend discarding the entire ADC ram buffer data.

bit 22 **Unimplemented:** Read as '0'

bit 21-16 **RBF5:RBF0:** RAM DMA Buffer B Full Status bits for ADC5-ADC0
1 = RAM DMA ping-pong Buffer B is full
0 = RAM DMA pin-pong Buffer B is not full

These bits are self-clearing upon being read by software. When RBFIEx = 1 and the RBFx bit status is set, the individual ADCx DMA interrupt request is generated.

bit 15 **DMACEN:** ADC DMA Buffer Sample Count Enable bit
The DMA interface will save the current sample count for each buffer in the table starting at the ADCCNTB address after each sample write into the corresponding buffer in the SRAM.

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **RAFIE5:RAFIE0:** RAM DMA Buffer A Full Interrupt Enable bits for ADC5-ADC0
1 = Enable ping-pong DMA Buffer A interrupt requests for ADC5-ADC0
0 = Disable ping-pong DMA Buffer A interrupt requests for ADC5-ADC0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RAF5:RAF0:** RAM DMA Ping-Pong Buffer A Full Status bits for ADC5-ADC0
1 = RAM DMA ping-pong Buffer A is full
0 = RAM DMA ping-pong Buffer A is not full

These bits are self-clearing upon being read by software. When RAFIEx = 1 and the RAFx bit status is set, the individual ADCx DMA interrupt request is generated.

Note: The individual Class 1 High-Speed ADC5-ADC0 modules have an independent DMA bus master and are completely separate from the assignable general purpose DMA channels.

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REGISTER 25-29: ADCCNTB: ADC CHANNEL SAMPLE COUNT BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCNTB<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCNTB<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCNTB<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCNTB<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ADCCNTB<31:0>:** ADC Channel Count Base Address bits

SRAM address for the DMA interface at which to save the first class channel buffer A sample count values into the System RAM. If First Class Channel 'x' (where 'x' = 0-5), is ready with a new available sample data, and the DMA interface is currently saving data for Channel 'x' to RAM Buffer 'z' (where 'z' == 0 means Buffer A and 'z' == 1 means Buffer B, with 'z' depending on 'x'), the DMA interface will increment (+1) the 1 byte count value stored at System RAM address (ADCCNTB + 2 * x + z). ADCCNTB works in conjunction with ADCDMAB. The DMA interface will use ADCCNTB to save the buffer sample counts only if the DMACEN bit in the ADCDSTAT register is set to '1'.

REGISTER 25-30: ADCDMAB: ADC CHANNEL SAMPLE COUNT BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCDMAB<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCDMAB<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCDMAB<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCDMAB<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ADCDMAB<31:0>:** DMA Interface Base Address bits

Address at which to save first class channels data into the System RAM. If First Class Channel 'x' (where 'x' = 0-5), is ready with a new available sample data, and the DMA interface is currently saving data for Channel 'x' to RAM Buffer 'z' (where 'z' == 0 means Buffer A and 'z' == 1 means Buffer B, 'z' depending on 'x'), and the current DMA x-counter value is 'y' (with 'y' depending on 'x'), the DMA interface will store the 2-byte output data value at System RAM address (ADCDMAB + (2 * x + z) * $2^{(DMABL+1)}$ + 2 * y. Also, if the DMACEN bit in the ADCDSTAT register is set to '1', the DMA interface will store without delay the value 'y' itself at the System RAM address (ADCCNTB + 2 * x + z).

REGISTER 25-31: ADCDATAx: ADC OUTPUT DATA REGISTER 'x' ('x' = 0-27, 33-41, AND 45-53)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

Note 1: The registers, ADCDATA23-20,ADCDATA41-33, and ADCDATA45-47, are not available on 64-pin devices.

2: The registers, ADCDATA32-28 and ADCDATA44-42, are not available on 64-pin and 100-pin devices.

3: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

4: Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

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REGISTER 25-32: ADCTRGSNS: ADC TRIGGER LEVEL/EDGE SENSITIVITY REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	LVL27	LVL26	LVL25	LVL24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LVL23(1)	LVL22(1)	LVL21(1)	LVL20(1)	LVL19	LVL18	LVL17	LVL16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LVL15	LVL14	LVL13	LVL12	LVL11	LVL10	LVL9	LVL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **LVL27:LVL0:** Trigger Level and Edge Sensitivity bits

1 = Analog input is sensitive to the high level of its trigger (level sensitivity implies retriggering as long as the trigger signal remains high)

0 = Analog input is sensitive to the positive edge of its trigger (this is the value after a reset)

Selecting edge trigger rather than level will add up to ±1 TAD of uncertainty in the trigger event point due to trigger signal synchronization and clock phasing; means the actual trigger worst case could be up to 2 TAD after the actual trigger event thereby extending the sample time by the same amount.

Note 1: This bit is not available on 64-pin devices.

Note 1: This register specifies the trigger level for analog inputs 0 to 27.

2: The higher analog input ID belongs to Class 3, and therefore, is only scan triggered. All Class 3 analog inputs use the Scan Trigger, for which the level/edge is defined by the STRGLVL bit (ADCCON1<3>).

REGISTER 25-33: ADCxTIME: DEDICATED HIGH-SPEED ADCx TIMING REGISTER ('x' = 0 THROUGH 5)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
	—	—	—	ADCEIS<2:0>			SELRES<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BCHEN	ADCDIV<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SAMC<9:8>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **ADCEIS<2:0>:** ADCx Early Interrupt Select bits
111 = The data ready interrupt is generated 8 ADC clocks prior to the end of conversion
110 = The data ready interrupt is generated 7 ADC clocks prior to the end of conversion
.
.
.
001 = The data ready interrupt is generated 2 ADC clocks prior to the end of conversion
000 = The data ready interrupt is generated 1 ADC clock prior to the end of conversion

Note: All options are available when the selected resolution, specified by the SELRES<1:0> bits (ADCxTIME<25:24>), is 12-bit or 10-bit. For a selected resolution of 8-bit, options from '000' to '101' are valid. For a selected resolution of 6-bit, options from '000' to '011' are valid.

bit 25-24 **SELRES<1:0>:** ADCx Resolution Select bits
11 = 12 bits
10 = 10 bits
01 = 8 bits
00 = 6 bits

bit 23 **BCHEN:** Buffer Channel Enable bit
1 = ADC data saved in DMA system ram buffer when DMAEN (ADCDSTAT<31>) = 1
0 = ADC data must be read by CPU from appropriate ADC result register

bit 22-16 **ADCDIV<6:0>:** ADCx Clock Divisor bits
These bits divide the ADC control clock with period TQ to generate the clock for ADCx (TADx).
1111111 = 254 * TQ = TADx
.
.
.
0000011 = 6 * TQ = TADx
0000010 = 4 * TQ = TADx
0000001 = 2 * TQ = TADx
0000000 = Reserved

bit 15-10 **Unimplemented:** Read as '0'

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REGISTER 25-33: ADCxTIME: DEDICATED HIGH-SPEED ADCx TIMING REGISTER (CONTINUED) ('x' = 0 THROUGH 5)

bit 9-0 **SAMC<9:0>:** ADCx Sample Time bits

Where TADx = period of the ADC conversion clock for the dedicated ADC controlled by the ADCDIV<6:0> bits.

1111111111 = 1025 TADx
.
.
.
0000000001 = 3 TADx
0000000000 = 2 TADx

Note: The SAMC sample time is always enforced regardless even if the conversion trigger occurs before SAMC expiration. The conversion trigger event is persistent and will be acknowledged and start the conversion if true, immediately after the SAMC period. ADC0-ADC5 will remain indefinitely in the sample state even after the expiration of SAMC until the trigger event, which will end sampling and start conversion, except when either of the following are true:

- The ADC filter is enabled and the DFMODE bit in the ADCFLTRx register = 0
- The TRGSRC3 bit in the ADCTRG1 register = Global level software trigger

REGISTER 25-34: ADCEIEN1: ADC EARLY INTERRUPT ENABLE REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	EIEN27	EIEN26	EIEN25	EIEN24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN23(1)	EIEN22(1)	EIEN21(1)	EIEN20(1)	EIEN19	EIEN18	EIEN17	EIEN16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN15	EIEN14	EIEN13	EIEN12	EIEN11	EIEN10	EIEN9	EIEN8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EIEN7	EIEN6	EIEN5	EIEN4	EIEN3	EIEN2	EIEN1	EIEN0

Legend:	HS = Hardware Set	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **EIEN27:EIEN0:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 31-0) of the ADCEISTAT1 register)

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

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REGISTER 25-35: ADCEIEN2: ADC EARLY INTERRUPT ENABLE REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	EIEN53	EIEN52	EIEN51	EIEN50	EIEN49	EIEN48
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	EIEN47(1)	EIEN46(1)	EIEN45(1)	—	—	—	EIEN41(1)	EIEN40(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	EIEN39(1)	EIEN38(1)	EIEN37(12)	EIEN36(1)	EIEN35(1)	EIEN34(1)	EIEN33(1)	—

Legend:	HS = Hardware Set	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-13 **EIEN53:EIEN45:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 44-32) of the ADCEISTAT2 register)

0 = Interrupts are disabled

bit 12-10 **Unimplemented:** Read as '0'

bit 9-1 **EIEN41:EIEN33:** Early Interrupt Enable for Analog Input bits

1 = Early Interrupts are enabled for the selected analog input. The interrupt is generated after the early interrupt event occurs (indicated by the EIRDYx bit ('x' = 44-32) of the ADCEISTAT2 register)

0 = Interrupts are disabled

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-36: ADCEISTAT1: ADC EARLY INTERRUPT STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	EIRDY27	EIRDY26	EIRDY25	EIRDY24
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY23(1)	EIRDY22(1)	EIRDY21(1)	EIRDY20(1)	EIRDY19	EIRDY18	EIRDY17	EIRDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0

Legend:	HS = Hardware Set	HC = Cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **EIRDY27:EIRDY0:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN1 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

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REGISTER 25-37: ADCEISTAT2: ADC EARLY INTERRUPT STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	EIRDY53	EIRDY52	EIRDY51	EIRDY50	EIRDY49	EIRDY48
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	EIRDY47(1)	EIRDY46(1)	EIRDY45(1)	—	—	—	EIRDY41(1)	EIRDY40(1)
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	U-0
	EIRDY39(1)	EIRDY38(1)	EIRDY37(1)	EIRDY36(1)	EIRDY35(1)	EIRDY34(1)	EIRDY33(1)	—

Legend:	HS = Hardware Set	HC = Cleared by hardware	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-13 **EIRDY53:EIRDY45:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN2 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

bit 12-10 **Unimplemented:** Read as '0'

bit 9-1 **EIRDY41:EIRDY33:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN2 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-38: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	WKUPCLKCNT<3:0>			
23:16	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WKIEN7	—	WKIEN5	WKIEN4	WKIEN3	WKIEN2	WKIEN1	WKIEN0
15:8	R-0, HS, HC	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	WKRDY7	—	WKRDY5	WKRDY4	WKRDY3	WKRDY2	WKRDY1	WKRDY0
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ANEN7	—	ANEN5	ANEN4	ANEN3	ANEN2	ANEN1	ANEN0

Legend:	HS = Hardware Set	HC = Cleared by Software	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-24 **WKUPCLKCNT<3:0>:** Wake-up Clock Count bits

These bits represent the number of ADC clocks required to warm-up the ADC module before it can perform conversion. Although the clocks are specific to each ADC, the WKUPCLKCNT bit is common to all ADC modules.

1111 = 2^{15} = 32,768 clocks
.
.
.
0110 = 2^{6} = 64 clocks
0101 = 2^{5} = 32 clocks
0100 = 2^{4} = 16 clocks
0011 = 2^{4} = 16 clocks
0010 = 2^{4} = 16 clocks
0001 = 2^{4} = 16 clocks
0000 = 2^{4} = 16 clocks

Note: Minimum required ADCx warm-up time, (i.e., WKUPCLKCNT), is the lesser of 500 ADC clocks, (i.e., T_{AD}), or 20 µs.

bit 23 **WKIEN7:** Shared ADC (ADC7) Wake-up Interrupt Enable bit

1 = Enable interrupt and generate interrupt when the WKRDY7 status bit is set
0 = Disable interrupt

bit 22 **Unimplemented:** Read as '0'

bit 21-16 **WKIEN5:WKIEN0:** ADC5-ADC0 Wake-up Interrupt Enable bit

1 = Enable interrupt and generate interrupt when the WKRDYx status bit is set
0 = Disable interrupt

bit 15 **WKRDY7:** Shared ADC (ADC7) Wake-up Status bit

1 = ADC7 Analog and Bias circuitry ready after the wake-up count number $2^{WKUPEXP}$ clocks after setting ANEN7 to '1'
0 = ADC7 Analog and Bias circuitry is not ready

Note: This bit is cleared by hardware when the ANEN7 bit is cleared

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **WKRDY5:WKRDY0:** ADC5-ADC0 Wake-up Status bit

1 = ADCx Analog and Bias circuitry ready after the wake-up count number $2^{WKUPEXP}$ clocks after setting ANEN*x* to '1'
0 = ADCx Analog and Bias circuitry is not ready

Note: These bits are cleared by hardware when the ANEN*x* bit is cleared

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REGISTER 25-38: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **ANEN5:ANEN0:** ADC5-ADC0 Analog and Bias Circuitry Enable bits
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled

REGISTER 25-39: ADCxCFG: ADCx CONFIGURATION REGISTER ('x' = 0 THROUGH 5 AND 7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCFG<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCFG<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCFG<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCCFG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ADCCFG<31:0>:** ADC Module Configuration Data bits

Note: These bits can only change when the applicable ANENx bit in the ADCANCON register is cleared. These are calibration values determined at product test time and are provided to the user to copy and write into these registers.

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REGISTER 25-40: ADCSYSCFG0: ADC SYSTEM CONFIGURATION REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	—	—	—	—	AN27	AN26	AN25	AN24
23:16	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN23(1)	AN22(1)	AN21(1)	AN20(1)	AN19	AN18	AN17	AN16
15:8	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8
7:0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Legend:	HS = Hardware Set	HC = Cleared by Software	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-0 **AN27:AN0>:** ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<31:0>: Reflects the presence or absence of the respective analog input (AN31-AN0).

Note 1: This bit is not available on 64-pin devices.

REGISTER 25-41: ADCSYSCFG1: ADC SYSTEM CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	HC, HS, R-0	HC, HS, R-0	r-1	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0
	—	—	AN53(2)	AN52(2)	—	AN50(2)	AN49	AN48
15:8	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	U-0	U-0	U-0	HC, HS, R-0	HC, HS, R-0
	AN47(1)	AN46(1)	AN45(1)	—	—	—	AN41(1)	AN40(1)
7:0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	HC, HS, R-0	U-0
	AN39(1)	AN38(1)	AN37(1)	AN36(1)	AN35(1)	AN34(1)	AN33(1)	—

Legend:	HS = Hardware Set	HC = Cleared by Software	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-20 **AN53:AN52:** ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<63:32>: Reflects the presence or absence of the respective analog input (AN63-AN32).

bit 19 **Unimplemented:** Read as '0'

bit 18-13 **AN50:AN45:** ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<63:32>: Reflects the presence or absence of the respective analog input (AN63-AN32).

bit 9-1 **AN41:AN33:** ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<63:32>: Reflects the presence or absence of the respective analog input (AN63-AN32).

bit 0 **Unimplemented:** Read as '0'

Note 1: This bit is not available on 64-pin devices.

2: Internal Analog inputs: AN50 = IVREF (1.2V), AN52 = VBAT/2, AN53 = CTMU_TEMP.

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26.0 CONTROLLER AREA NETWORK (CAN)

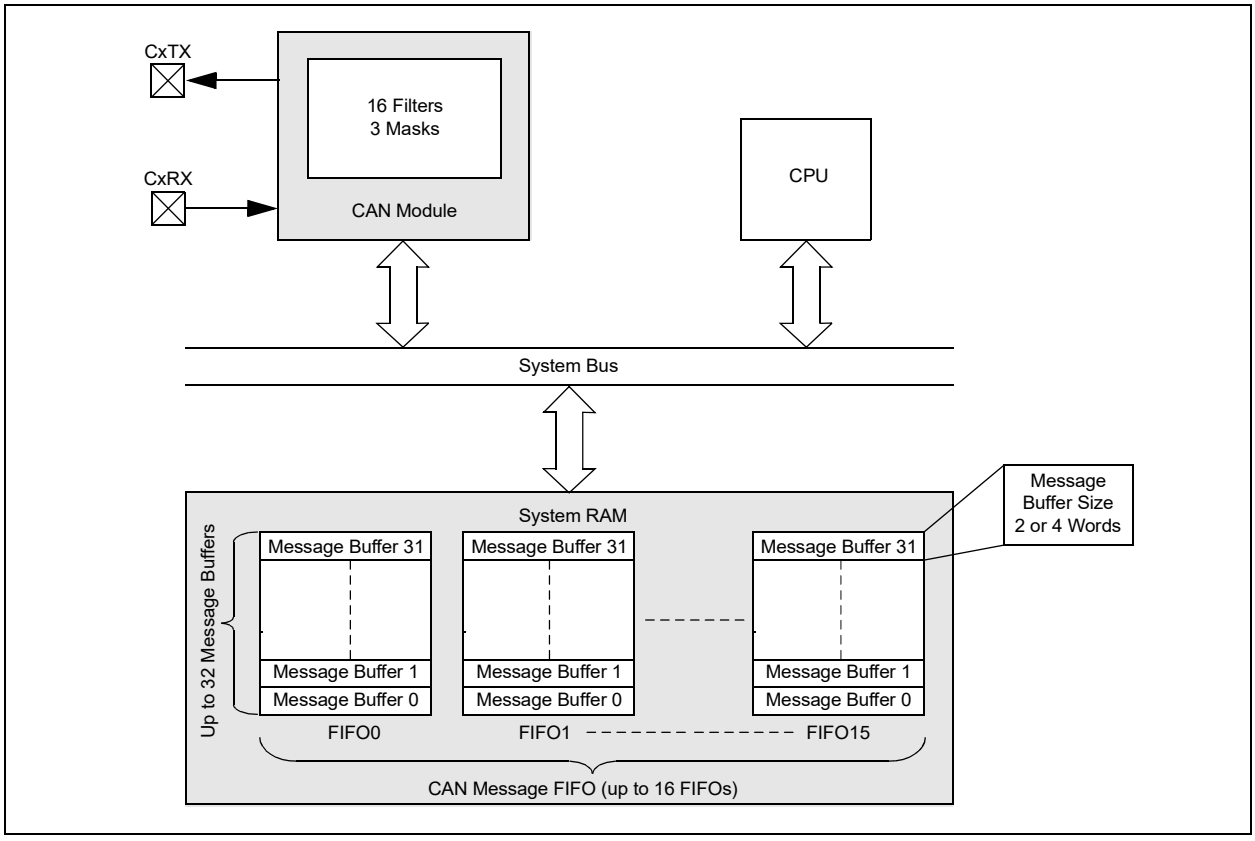
Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
  - 16 message FIFOs
  - Each FIFO can have up to 32 messages for a total of 512 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 16 acceptance filters for message filtering
  - Three acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
- Additional Features:
  - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus master on the PIC32MK system bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 26-1 illustrates the general structure of the CAN module.

FIGURE 26-1: PIC32MK CAN MODULE BLOCK DIAGRAM



26.1 Control Registers

TABLE 26-1: CAN1 THROUGH CAN4 REGISTER SUMMARY

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	C1CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
0010	C1CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>						0000
0020	C1INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
0030	C1VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
0040	C1TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
0050	C1FSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
0060	C1RXOVF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
0070	C1TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
0080	C1RXM0	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
0090	C1RXM1	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00A0	C1RXM2	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00B0	C1RXM3	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
00C0	C1FLTCON0	31:16	FLTEN3	MSEL3<1:0>	FSEL3<4:0>						FLTEN2	MSEL2<1:0>	FSEL2<4:0>						0000
		15:0	FLTEN1	MSEL1<1:0>	FSEL1<4:0>						FLTEN0	MSEL0<1:0>	FSEL0<4:0>						0000
00D0	C1FLTCON1	31:16	FLTEN7	MSEL7<1:0>	FSEL7<4:0>						FLTEN6	MSEL6<1:0>	FSEL6<4:0>						0000
		15:0	FLTEN5	MSEL5<1:0>	FSEL5<4:0>						FLTEN4	MSEL4<1:0>	FSEL4<4:0>						0000
00E0	C1FLTCON2	31:16	FLTEN11	MSEL11<1:0>	FSEL11<4:0>						FLTEN10	MSEL10<1:0>	FSEL10<4:0>						0000
		15:0	FLTEN9	MSEL9<1:0>	FSEL9<4:0>						FLTEN8	MSEL8<1:0>	FSEL8<4:0>						0000
00F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>	FSEL15<4:0>						FLTEN14	MSEL14<1:0>	FSEL14<4:0>						0000
		15:0	FLTEN13	MSEL13<1:0>	FSEL13<4:0>						FLTEN12	MSEL12<1:0>	FSEL12<4:0>						0000
0140	C1RXFn (n = 0-15)	31:16	SID<10:0>											-—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 26-1: CAN1 THROUGH CAN4 REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0																	0000
0350	C1FIFOCONn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
0360	C1FIFOINTn (n = 0-15)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
0370	C1FIFOUAn (n = 0-15)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
0380	C1FIFOCIn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000
1000	C2CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
1010	C2CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>		BRP<5:0>						0000
1020	C2INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
1030	C2VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
1040	C2TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
1050	C2FSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
1060	C2RXOVF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
1070	C2TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
1080	C2RXM0	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
1090	C2RXM1	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
10A0	C2RXM2	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
10B0	C2RXM3	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 26-1: CAN1 THROUGH CAN4 REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
10C0	C2FLTCON0	31:16	FLTEN3	MSEL3<1:0>		FSEL3<4:0>					FLTEN2	MSEL2<1:0>		FSEL2<4:0>					0000
		15:0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>					FLTEN0	MSEL0<1:0>		FSEL0<4:0>					0000
10D0	C2FLTCON1	31:16	FLTEN7	MSEL7<1:0>		FSEL7<4:0>					FLTEN6	MSEL6<1:0>		FSEL6<4:0>					0000
		15:0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>					FLTEN4	MSEL4<1:0>		FSEL4<4:0>					0000
10E0	C2FLTCON2	31:16	FLTEN11	MSEL11<1:0>		FSEL11<4:0>					FLTEN10	MSEL10<1:0>		FSEL10<4:0>					0000
		15:0	FLTEN9	MSEL9<1:0>		FSEL9<4:0>					FLTEN8	MSEL8<1:0>		FSEL8<4:0>					0000
10F0	C2FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000
1140	C2RXFn (n = 0-15)	31:16	SID<10:0>											-—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
1340	C2FIFOBA	31:16	C2FIFOBA<31:0>																0000
		15:0																	0000
1350	C2FIFOCONn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
1360	C2FIFOINTn (n = 0-15)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
1370	C2FIFOUAn (n = 0-15)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
1380	C2FIFOCIn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C2FIFOCI<4:0>					0000
4000	C3CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
4010	C3CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>			BRP<5:0>					0000
4020	C3INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
4030	C3VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
4040	C3TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
4050	C3FSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
4060	C3RXOVF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 26-1: CAN1 THROUGH CAN4 REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4070	C3TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
4080	C3RXM0	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
4090	C3RXM1	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
40A0	C3RXM2	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
40B0	C3RXM3	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
40C0	C3FLTCON0	31:16	FLTEN3	MSEL3<1:0>		FSEL3<4:0>					FLTEN2	MSEL2<1:0>		FSEL2<4:0>					0000
		15:0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>					FLTEN0	MSEL0<1:0>		FSEL0<4:0>					0000
40D0	C3FLTCON1	31:16	FLTEN7	MSEL7<1:0>		FSEL7<4:0>					FLTEN6	MSEL6<1:0>		FSEL6<4:0>					0000
		15:0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>					FLTEN4	MSEL4<1:0>		FSEL4<4:0>					0000
40E0	C3FLTCON2	31:16	FLTEN11	MSEL11<1:0>		FSEL11<4:0>					FLTEN10	MSEL10<1:0>		FSEL10<4:0>					0000
		15:0	FLTEN9	MSEL9<1:0>		FSEL9<4:0>					FLTEN8	MSEL8<1:0>		FSEL8<4:0>					0000
40F0	C3FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000
4140	C3RXFn (n = 0-15)	31:16	SID<10:0>											-—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
4340	C3FIFOBA	31:16	C3FIFOBA<31:0>																0000
		15:0																	0000
4350	C3FIFOCONn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
4360	C3FIFOINTn (n = 0-15)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
4370	C3FIFOUAn (n = 0-15)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
4380	C3FIFOCIn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C3FIFOCI<4:0>					0000
5000	C4CON	31:16	—	—	—	—	ABAT	REQOP<2:0>			OPMOD<2:0>			CANCAP	—	—	—	—	0480
		15:0	ON	—	SIDLE	—	CANBUSY	—	—	—	—	—	—	DNCNT<4:0>					0000
5010	C4CFG	31:16	—	—	—	—	—	—	—	—	—	WAKFIL	—	—	—	SEG2PH<2:0>			0000
		15:0	SEG2PHTS	SAM	SEG1PH<2:0>			PRSEG<2:0>			SJW<1:0>			BRP<5:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 26-1: CAN1 THROUGH CAN4 REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5020	C4INT	31:16	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE	0000
		15:0	IVRIF	WAKIF	CERRIF	SERRIF	RBOVIF	—	—	—	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF	0000
5030	C4VEC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	FILHIT<4:0>					—	ICODE<6:0>							0040
5040	C4TREC	31:16	—	—	—	—	—	—	—	—	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN	0000
		15:0	TERRCNT<7:0>								RERRCNT<7:0>								0000
5050	C4FSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0	0000
5060	C4RXOVF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
5070	C4TMR	31:16	CANTS<15:0>																0000
		15:0	CANTSPRE<15:0>																0000
5080	C4RXM0	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
5090	C4RXM1	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
50A0	C4RXM2	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
50B0	C4RXM3	31:16	SID<10:0>											-—	MIDE	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
50C0	C4FLTCON0	31:16	FLTEN3	MSEL3<1:0>		FSEL3<4:0>					FLTEN2	MSEL2<1:0>		FSEL2<4:0>					0000
		15:0	FLTEN1	MSEL1<1:0>		FSEL1<4:0>					FLTEN0	MSEL0<1:0>		FSEL0<4:0>					0000
50D0	C4FLTCON1	31:16	FLTEN7	MSEL7<1:0>		FSEL7<4:0>					FLTEN6	MSEL6<1:0>		FSEL6<4:0>					0000
		15:0	FLTEN5	MSEL5<1:0>		FSEL5<4:0>					FLTEN4	MSEL4<1:0>		FSEL4<4:0>					0000
50E0	C4FLTCON2	31:16	FLTEN11	MSEL11<1:0>		FSEL11<4:0>					FLTEN10	MSEL10<1:0>		FSEL10<4:0>					0000
		15:0	FLTEN9	MSEL9<1:0>		FSEL9<4:0>					FLTEN8	MSEL8<1:0>		FSEL8<4:0>					0000
50F0	C4FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000
5140	C4RXFn (n = 0-15)	31:16	SID<10:0>											-—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
5340	C4FIFOBA	31:16	C4FIFOBA<31:0>																0000
		15:0																	0000
5350	C4FIFOCONn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 26-1: CAN1 THROUGH CAN4 REGISTER SUMMARY (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5360	C4FIFOINTn (n = 0-15)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
5370	C4FIFOUAn (n = 0-15)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
5380	C4FIFOCIn (n = 0-15)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C4FIFOCI<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8, and 0xC, respectively. See **Section13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 26-1: CxCON: CAN MODULE CONTROL REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON(1)	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as '0'

bit 15 **ON:** CAN On bit(1)
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as '0'

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

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REGISTER 26-1: CxCON: CAN MODULE CONTROL REGISTER ('x' = 1-4) (CONTINUED)

bit 13 **SIDLE:** CAN Stop in Idle bit
1 = CAN Stops operation when system enters Idle mode
0 = CAN continues operation when system enters Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **CANBUSY:** CAN Module is Busy bit
1 = The CAN module is active
0 = The CAN module is completely disabled

bit 10-5 **Unimplemented:** Read as '0'

bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
10010 = Compare up to data byte 2 bit 6 with EID17 (CxRXFn<17>)
•
•
•
00001 = Compare up to data byte 0 bit 7 with EID0 (CxRXFn<0>)
00000 = Do not compare data bytes

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

REGISTER 26-2: CxCFG: CAN BAUD RATE CONFIGURATION REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0>(1,4)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS(1)	SAM(2)	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0>(3)		BRP<5:0>					

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as '0'

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

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REGISTER 26-2: CxCFG: CAN BAUD RATE CONFIGURATION REGISTER ('x' = 1-4) (CONTINUED)

bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits(3)
11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits
111111 = TQ = (2 x 64) / PBCLK5
111110 = TQ = (2 x 63) / PBCLK5
•
•
•
000001 = TQ = (2 x 2) / PBCLK5
000000 = TQ = (2 x 1) / PBCLK5

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

REGISTER 26-3: CxINT: CAN INTERRUPT REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIF	WAKIF	CERRIF	SERRIF(1)	RBOVIF	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 30 **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 29 **CERRIE:** CAN Bus Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 28 **SERRIE:** System Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 27 **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 26-20 **Unimplemented:** Read as '0'

bit 19 **MODIE:** Mode Change Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 18 **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 17 **RBIE:** Receive Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 16 **TBIE:** Transmit Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 15 **IVRIF:** Invalid Message Received Interrupt Flag bit
1 = An invalid messages interrupt has occurred
0 = An invalid message interrupt has not occurred

Note 1: This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CxCON<15>).

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REGISTER 26-3: CxINT: CAN INTERRUPT REGISTER ('x' = 1-4) (CONTINUED)

bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred

bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred

bit 12 **SERRIF:** System Error Interrupt Flag bit
1 = A system error occurred (typically an illegal address was presented to the system bus)
0 = A system error has not occurred

bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred

bit 10-4 **Unimplemented:** Read as '0'

bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred

bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred

bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending

bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

Note 1: This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CxCON<15>).

REGISTER 26-4: CxVEC: CAN INTERRUPT CODE REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	FILHIT<4:0>				
7:0	U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
	—	ICODE<6:0>(1)						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bit

11111 = Reserved
•
•
•
10000 = Reserved
01111 = Filter 15
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

Note 1: These bits are only updated for enabled interrupts.

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REGISTER 26-4: CxVEC: CAN INTERRUPT CODE REGISTER ('x' = 1-4)

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits(1)

1111111 = Reserved
•
•
•
1001001 = Reserved
1001000 = Invalid message received (IVRIF)
1000111 = CAN module mode change (MODIF)
1000110 = CAN timestamp timer (CTMRIF)
1000101 = Bus bandwidth error (SERRIF)
1000100 = Address error interrupt (SERRIF)
1000011 = Receive FIFO overflow interrupt (RBOVIF)
1000010 = Wake-up interrupt (WAKIF)
1000001 = Error Interrupt (CERRIF)
1000000 = No interrupt
0111111 = Reserved
•
•
•
0100000 = Reserved
0001111 = FIFO15 Interrupt (CxFSTAT<15> set)
•
•
•
0000001 = FIFO1 Interrupt (CxFSTAT<1> set)
0000000 = FIFO0 Interrupt (CxFSTAT<0> set)

Note 1: These bits are only updated for enabled interrupts.

REGISTER 26-5: CxTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)

bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)

bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)

bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)

bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)

bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning

bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter

bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 26-6: CxFSTAT: CAN FIFO STATUS REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FIFOIP<15:0>:** FIFOx Interrupt Pending bits

1 = One or more enabled FIFO interrupts are pending

0 = No FIFO interrupts are pending

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REGISTER 26-7: CxRXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVF<15:0>:** FIFOx Receive Overflow Interrupt Pending bit
1 = FIFO has overflowed
0 = FIFO has not overflowed

REGISTER 26-8: CxTMR: CAN TIMER REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTS<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CANTSPRE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CANTS<15:0>:** CAN Time Stamp Timer bits
This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (CxCON<20>) is set.

Note 1: CxTMR will be paused when CANCAP = 0.
2: The CxTMR prescaler count will be reset on any write to CxTMR (CANTSPRE will be unaffected).

REGISTER 26-8: CxTMR: CAN TIMER REGISTER ('x' = 1-4)

bit 15-0 **CANTSPRE<15:0>:** CAN Time Stamp Timer Prescaler bits

1111 1111 1111 1111 = CAN time stamp timer (CANTS) increments every 65,535 system clocks

.

.

.

0000 0000 0000 0000 = CAN time stamp timer (CANTS) increments every system clock

Note 1: CxTMR will be paused when CANCAP = 0.

2: The CxTMR prescaler count will be reset on any write to CxTMR (CANTSPRE will be unaffected).

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REGISTER 26-9: CxRXMn: CAN ACCEPTANCE FILTER MASK 'n' REGISTER ('x' = 1-4; 'n' = 0, 1, 2 OR 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SID<10:3>							
23:16	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SID<2:0>			—	MIDE	—	EID<17:16>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Include the SIDx bit in filter comparison
0 = The SIDx bit is a 'don't care' in filter operation

bit 20 **Unimplemented:** Read as '0'

bit 19 **MIDE:** Identifier Receive Mode bit
1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Include the EIDx bit in filter comparison
0 = The EIDx bit is a 'don't care' in filter operation

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

REGISTER 26-10: CxFLTCON0: CAN FILTER CONTROL REGISTER 0 ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

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REGISTER 26-10: CxFLTCON0: CAN FILTER CONTROL REGISTER 0 ('x' = 1-4) (CONTINUED)

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 26-11: CxFLTCON1: CAN FILTER CONTROL REGISTER 1 ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN7	MSEL7<1:0>		FSEL7<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN6	MSEL6<1:0>		FSEL6<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN5	MSEL5<1:0>		FSEL5<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN4	MSEL4<1:0>		FSEL4<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN7:** Filter 7 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL7<1:0>:** Filter 7 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 28-24 **FSEL7<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN6:** Filter 6 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL6<1:0>:** Filter 6 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 20-16 **FSEL6<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

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REGISTER 26-11: CxFLTCON1: CAN FILTER CONTROL REGISTER 1 ('x' = 1-4) (CONTINUED)

bit 15 **FLTEN5:** Filter 17 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL5<1:0>:** Filter 5 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL5<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4:** Filter 4 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL4<1:0>:** Filter 4 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL4<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 26-12: CxFLTCON2: CAN FILTER CONTROL REGISTER 2 ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN11	MSEL11<1:0>		FSEL11<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN10	MSEL10<1:0>		FSEL10<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN9	MSEL9<1:0>		FSEL9<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN8	MSEL8<1:0>		FSEL8<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN11:** Filter 11 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 28-24 **FSEL11<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN10:** Filter 10 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 20-16 **FSEL10<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

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REGISTER 26-12: CxFLTCON2: CAN FILTER CONTROL REGISTER 2 ('x' = 1-4) (CONTINUED)

bit 15 **FLTEN9:** Filter 9 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL9<1:0>:** Filter 9 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL9<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN8:** Filter 8 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL8<1:0>:** Filter 8 Mask Select bits
11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL8<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 26-13: CxFLTCON3: CAN FILTER CONTROL REGISTER 3 ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN15	MSEL15<1:0>		FSEL15<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN14	MSEL14<1:0>		FSEL14<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN13	MSEL13<1:0>		FSEL13<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN12	MSEL12<1:0>		FSEL12<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN15:** Filter 15 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL15<1:0>:** Filter 15 Mask Select bits
11 = 11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 28-24 **FSEL15<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN14:** Filter 14 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL14<1:0>:** Filter 14 Mask Select bits
11 = 11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 20-16 **FSEL14<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

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REGISTER 26-13: CxFLTCON3: CAN FILTER CONTROL REGISTER 3 ('x' = 1-4) (CONTINUED)

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = 11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = 11 = Reserved
10 = Acceptance Mask 2 is selected
01 = Acceptance Mask 1 is selected
00 = Acceptance Mask 0 is selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 26-14: CxRXFn: CAN ACCEPTANCE FILTER 'n' REGISTER 7 ('x' = 1-4; 'n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SID<10:3>							
23:16	R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
	SID<2:0>			—	EXID	—	EID<17:16>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Message address bit SIDx must be '1' to match filter
0 = Message address bit SIDx must be '0' to match filter

bit 20 **Unimplemented:** Read as '0'

bit 19 **EXID:** Extended Identifier Enable bits
1 = Match only messages with extended identifier addresses
0 = Match only messages with standard identifier addresses

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Message address bit EIDx must be '1' to match filter
0 = Message address bit EIDx must be '0' to match filter

Note: This register can only be modified when the filter is disabled (FLTENn = 0).

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REGISTER 26-15: CxFIFOBA: CAN MESSAGE BUFFER BASE ADDRESS REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CxFIFOBA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CxFIFOBA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CxFIFOBA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0(1)	R-0(1)
	CxFIFOBA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CxFIFOBA<31:0>:** CANx FIFO Base Address bits

These bits define the base address of all message buffers. Individual message buffers are located based on the size of the previous message buffers. This address is a physical address. Bits <1:0> are read-only and read as '0', forcing the messages to be 32-bit word-aligned in device RAM.

Note 1: This bit is unimplemented and will always read '0', which forces word-alignment of messages.

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CxCON<23:21>) = 100).

REGISTER 26-16: CxFIFOCONn: CAN FIFO CONTROL REGISTER 'n' ('x' = 1-4;'n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	FSIZE<4:0>(1)				
15:8	U-0	S/HC-0	S/HC-0	R/W-0	U-0	U-0	U-0	U-0
	—	FRESET	UINC	DONLY(1)	—	—	—	—
7:0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXEN	TXABAT(2)	TXLARB(3)	TXERR(3)	TXREQ	RTREN	TXPR<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **FSIZE<4:0>:** FIFO Size bits(1)
11111 = FIFO is 32 messages deep
•
•
•
00010 = FIFO is 3 messages deep
00001 = FIFO is 2 messages deep
00000 = FIFO is 1 message deep

bit 15 **Unimplemented:** Read as '0'

bit 14 **FRESET:** FIFO Reset bits
1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset. After setting, the user should poll whether this bit is clear before taking any action.
0 = No effect

bit 13 **UINC:** Increment Head/Tail bit
TXEN = 1: (FIFO configured as a Transmit FIFO)
When this bit is set the FIFO head will increment by a single message
TXEN = 0: (FIFO configured as a Receive FIFO)
When this bit is set the FIFO tail will increment by a single message

bit 12 **DONLY:** Store Message Data Only bit(1)
TXEN = 1: (FIFO configured as a Transmit FIFO)
This bit is not used and has no effect.
TXEN = 0: (FIFO configured as a Receive FIFO)
1 = Only data bytes will be stored in the FIFO
0 = Full message is stored, including identifier

bit 11-8 **Unimplemented:** Read as '0'

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CxCON<23:21>) = 100).
2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
3: This bit is reset on any read of this register or when the FIFO is reset.

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REGISTER 26-16: CxFIFOCONn: CAN FIFO CONTROL REGISTER 'n' ('x' = 1-4;'n' = 0 THROUGH 15) (CONTINUED)

bit 7 **TXEN:** TX/RX Buffer Selection bit
1 = FIFO is a Transmit FIFO
0 = FIFO is a Receive FIFO

bit 6 **TXABAT:** Message Aborted bit(2)
1 = Message was aborted
0 = Message completed successfully

bit 5 **TXLARB:** Message Lost Arbitration bit(3)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERR:** Error Detected During Transmission bit(3)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQ:** Message Send Request
TXEN = 1: (FIFO configured as a Transmit FIFO)
Setting this bit to '1' requests sending a message.
The bit will automatically clear when all the messages queued in the FIFO are successfully sent.
Clearing the bit to '0' while set ('1') will request a message abort.
TXEN = 0: (FIFO configured as a receive FIFO)
This bit has no effect.

bit 2 **RTREN:** Auto RTR Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXPR<1:0>:** Message Transmit Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CxCON<23:21>) = 100).
2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
3: This bit is reset on any read of this register or when the FIFO is reset.

REGISTER 26-17: CxFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('x' = 1-4); n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXNEMPTYIE
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	TXNFULLIF(1)	TXHALFIF	TXEMPTYIF(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R-0	R-0	R-0
	—	—	—	—	RXOVFLIF	RXFULLIF(1)	RXHALFIF(1)	RXNEMPTYIF(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

Note 1: This bit is read-only and reflects the status of the FIFO.

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REGISTER 26-17: CxFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' ('x' = 1-4); n' = 0 THROUGH 15) (CONTINUED)

bit 9 **TXHALFIF:** FIFO Transmit FIFO Half Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is ≤ half full
0 = FIFO is > half full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 8 **TXEMPTYIF:** Transmit FIFO Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is empty
0 = FIFO is not empty, at least 1 message queued to be transmitted
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **RXOVFLIF:** Receive FIFO Overflow Interrupt Flag bit
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = Overflow event has occurred
0 = No overflow event occured

bit 2 **RXFULLIF:** Receive FIFO Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is full
0 = FIFO is not full

bit 1 **RXHALFIF:** Receive FIFO Half Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **RXNEMPTYIF:** Receive Buffer Not Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is not empty, has at least 1 message
0 = FIFO is empty

Note 1: This bit is read-only and reflects the status of the FIFO.

REGISTER 26-18: CxFIFOUAn: CAN FIFO USER ADDRESS REGISTER 'n' ('x' = 1-4; 'n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CxFIFOUAn<31:24>							
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CxFIFOUAn<23:16>							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CxFIFOUAn<15:8>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-0(1)	R-0(1)
	CxFIFOUAn<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CxFIFOUAn<31:0>:** CANx FIFO User Address bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit will always read '0', which forces byte-alignment of messages.

Note: This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

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REGISTER 26-19: CxFIFOCIn: CAN MODULE MESSAGE INDEX REGISTER 'n' ('x' = 1-4; 'n' = 0 THROUGH 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	CxFIFOCI<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **CxFIFOCIn<4:0>:** CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a transmit buffer)
A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a receive buffer)
A read of this register will return an index to the message that the FIFO will use to save the next message.

NOTES:

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27.0 OP AMP/COMPARATOR MODULE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 39. "Op amp/Comparator"** (DS60001178), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

Depending on the device, the Op amp/Comparator module consists of a Comparator and Op amp modules. When available, the Op amps can be independently enabled or disabled from the Comparator.

Key features of the Comparator include:

- Differential inputs
- Rail-to-rail operation
- Selectable output and trigger event polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal voltage reference via a 12-bit CDAC output or an external pin
- Output debounce or Digital noise filter with these selectable clocks:
  - Peripheral Bus Clock (PBCLK2)
  - System Clock (SYSCLK)
  - Reference Clock 3 (REFCLK3)
  - PBCLK2/Timer PRx ('x' = 2-5)
  - PWM Secondary Special Event
- Outputs can be internally configured as trigger sources

The following are key features of the Op amps:

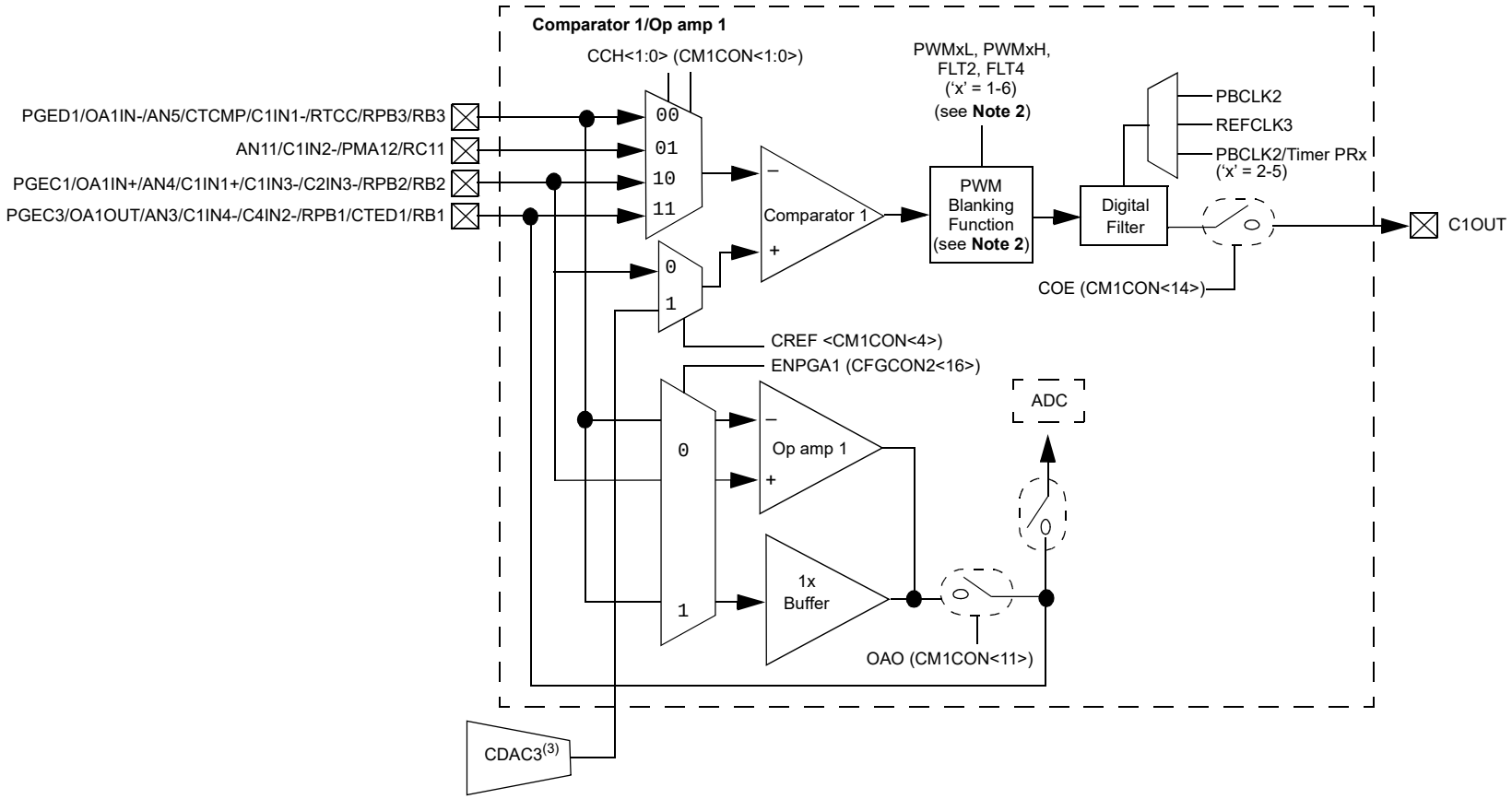
- Inverting and non-inverting Inputs and output accessible on pins
- Rail-to-rail operation ($3V \leq AV_{DD} \leq 3.6V$)
- Internal connection to ADC Sample and Hold circuits/SAR cores
- Special voltage follower mode for buffering signals

Please refer to the PIC32MK GP Family Features in **TABLE 1: "PIC32MK General Purpose (GP) Family Features"** for the actual number of available Op amp/ Comparator modules on your specific device.

Block diagrams of the Op amp/Comparator module are illustrated in Figure 27-1 through Figure 27-5.

Note: The Op amps are disabled by default (i.e., OPAxMD bit in the PMD2 register is equal to '1') on any Reset. Before use or access to any corresponding Op amp, ensure that the OPAxMD bit is equal to '0'.

FIGURE 27-1: OP AMP 1/COMPARATOR 1 MODULE BLOCK DIAGRAM



Note 1: Refer to the device pin tables (Table 3 and Table 5) for other analog inputs that may be also be connected to the Op amp and Comparator inputs.
2: The PWM Blank Function is available only on PIC32MKXXMCXXX devices.
3: Caution: To avoid false comparator output faults or glitches when using the internal DAC as a comparator reference, always initialize the DAC before initializing and enabling the comparator.

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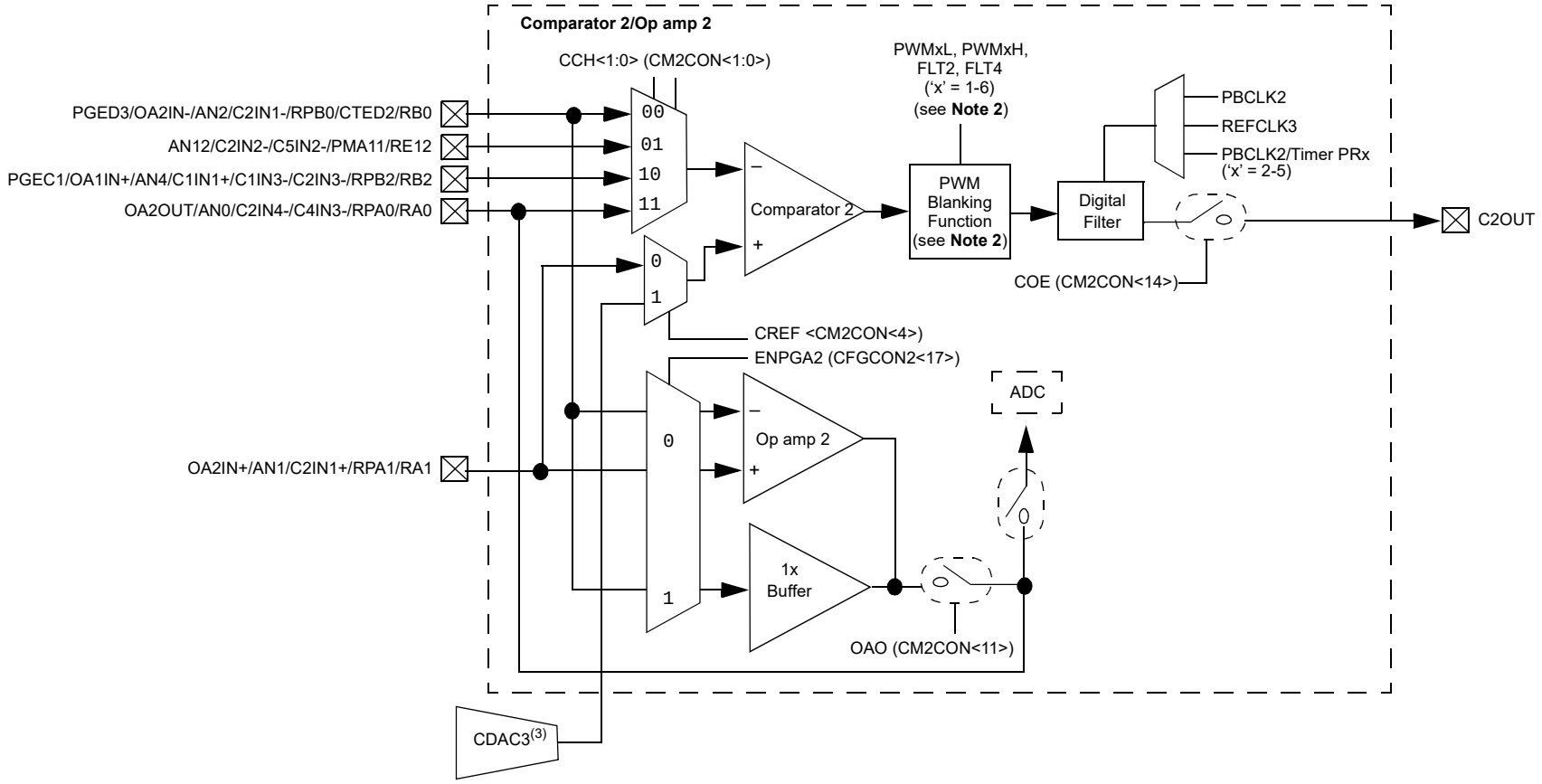
FIGURE 27-2: OP AMP 2/COMPARATOR 2 MODULE BLOCK DIAGRAM



Note 1: Refer to the device pin tables (Table 3 and Table 5) for other analog inputs that may be also be connected to the Op amp and Comparator inputs.
2: The PWM Blank Function is available only on PIC32MKXXMCXXX devices.
3: Caution: To avoid false comparator output faults or glitches when using the internal DAC as a comparator reference, always initialize the DAC before initializing and enabling the comparator.

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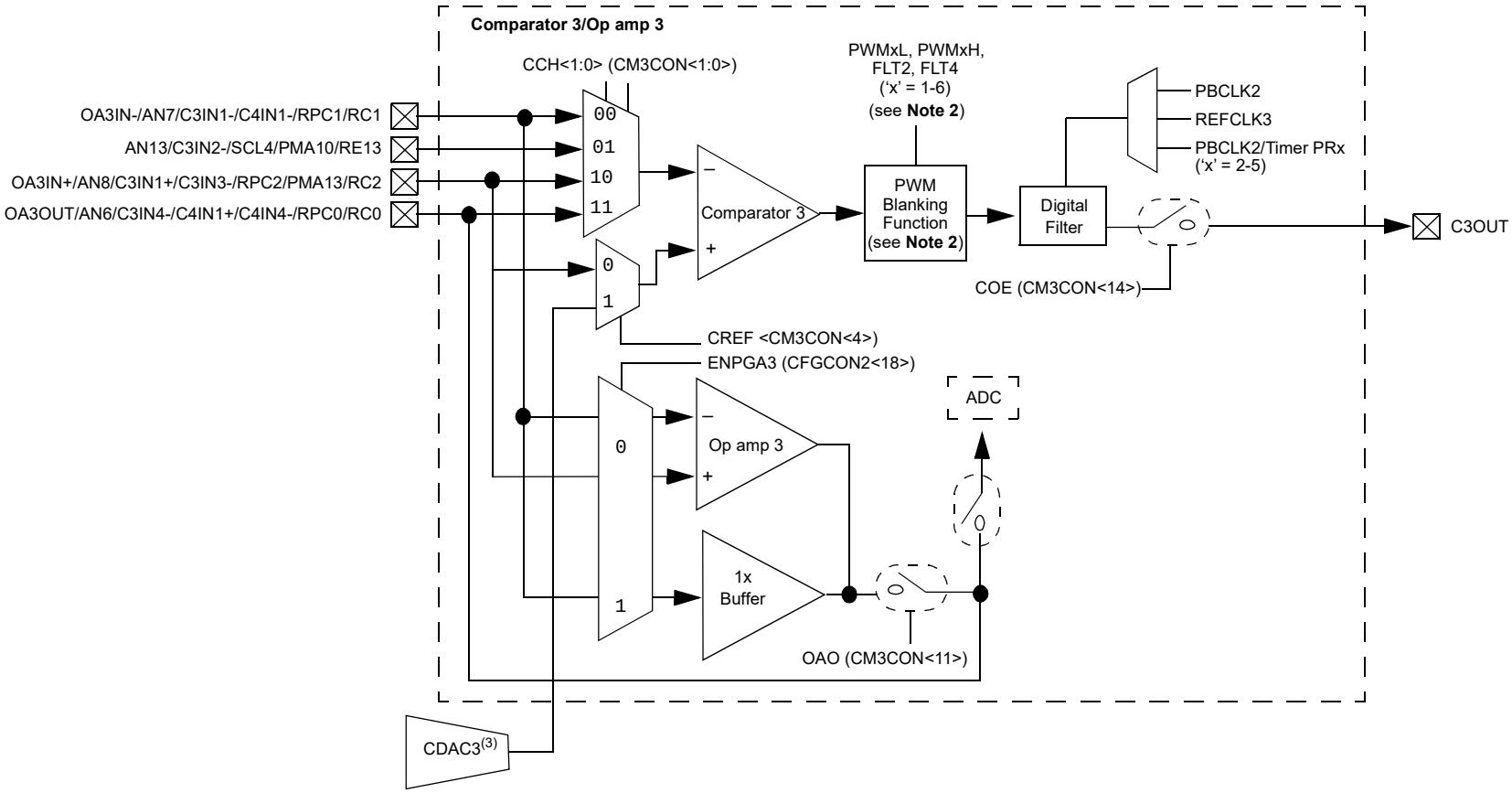
FIGURE 27-3: OP AMP 3/COMPARATOR 3 MODULE BLOCK DIAGRAM



Note 1: Refer to the device pin tables (Table 3 and Table 5) for other analog inputs that may be also be connected to the Op amp and Comparator inputs.
2: The PWM Blank Function is only available on PIC32MKXXMCXXX devices.
3: Caution: To avoid false comparator output faults or glitches when using the internal DAC as a comparator reference, always initialize the DAC before initializing and enabling the comparator.

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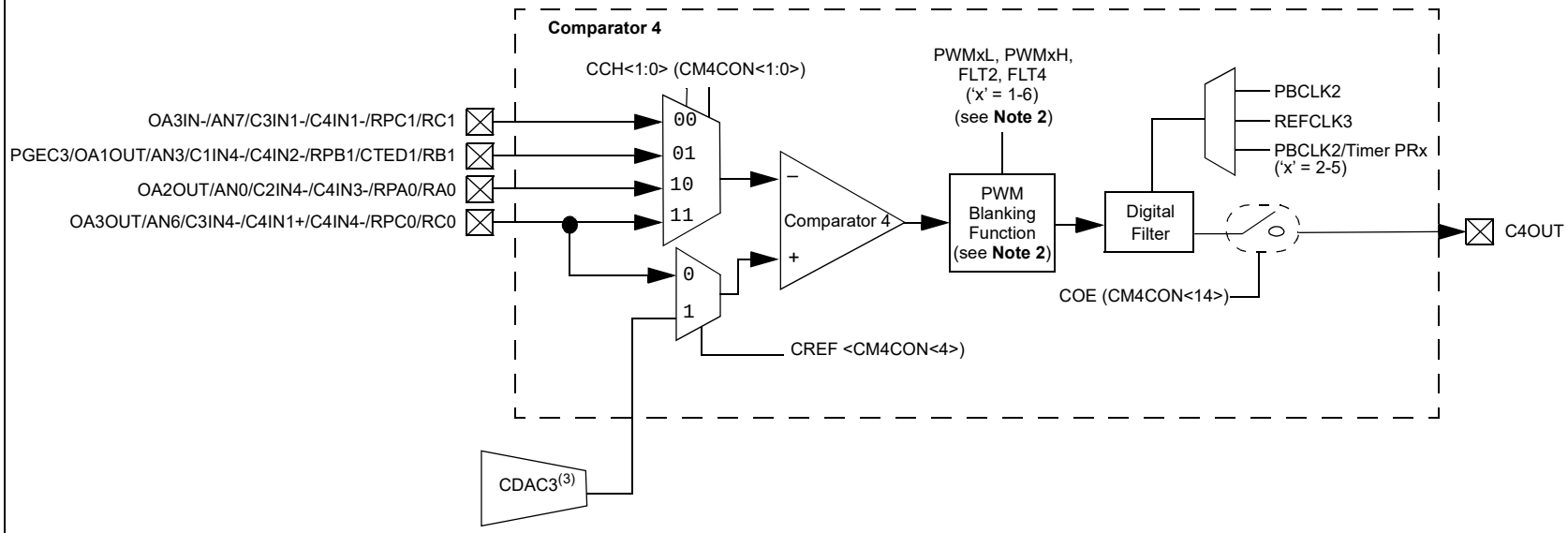
FIGURE 27-4: COMPARATOR 4 MODULE BLOCK DIAGRAM



Note 1: Refer to the device pin tables (Table 3 and Table 5) for other analog inputs that may be also be connected to the Op amp and Comparator inputs.
2: The PWM Blank Function is only available on PIC32MKXXMCXXX devices.
3: Caution: To avoid false comparator output faults or glitches when using the internal DAC as a comparator reference, always initialize the DAC before initializing and enabling the comparator.

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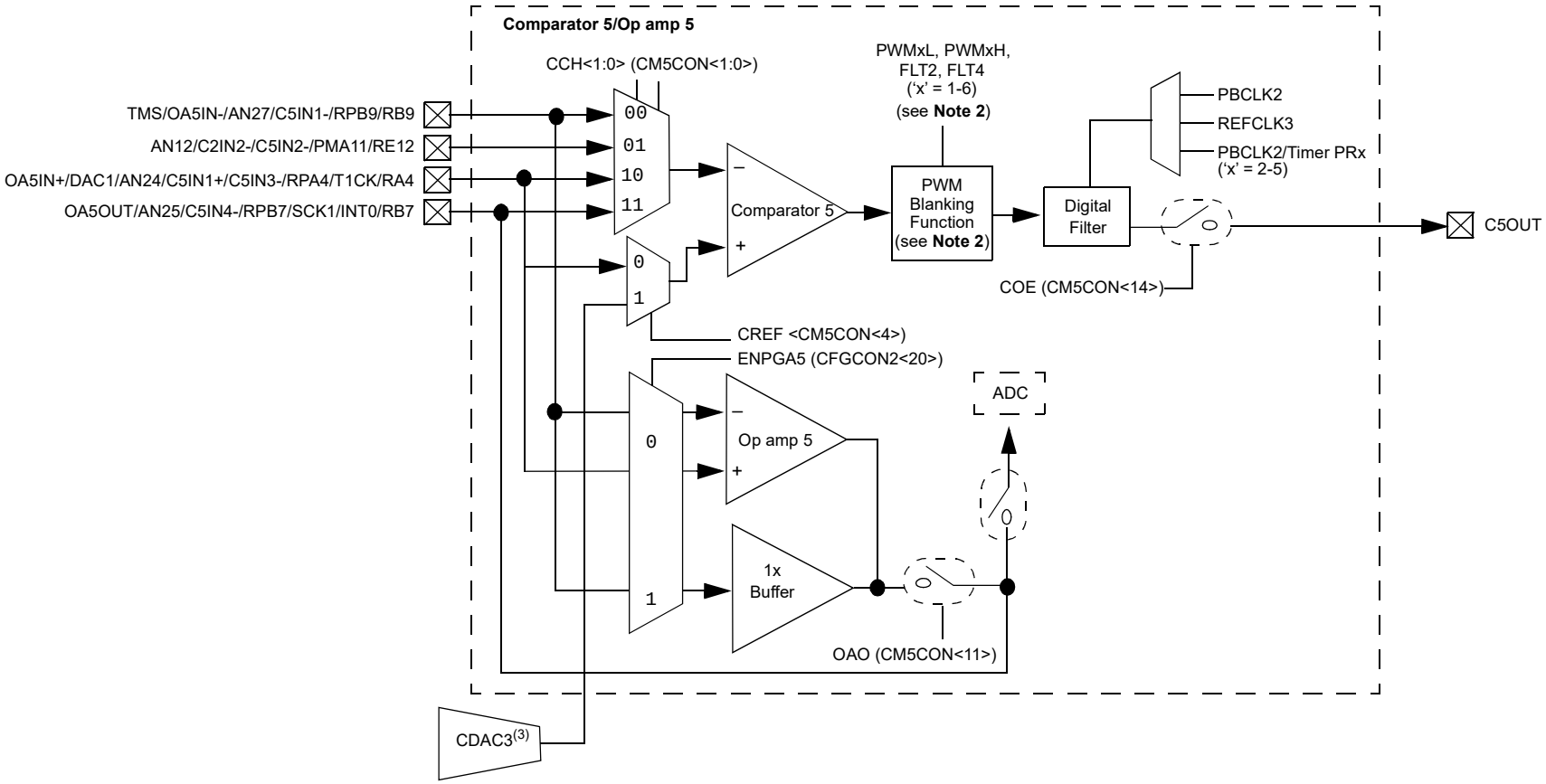
FIGURE 27-5: OP AMP 5/COMPARATOR 5 MODULE BLOCK DIAGRAM



Note 1: Refer to the device pin tables (Table 3 and Table 5) for other analog inputs that may be also be connected to the Op amp and Comparator inputs.
2: The PWM Blank Function is only available on PIC32MKXXMCXXX devices.
3: Caution: To avoid false comparator output faults or glitches when using the internal DAC as a comparator reference, always initialize the DAC before initializing and enabling the comparator.

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27.1 Op amp Interface

PIC32MK GP devices implement a total of five comparators and four Op amps. The Op amp Comparator module 4 does not implement the associated Op amp. The Op amp can be configured to operate in two different modes: Regular Op amp mode and Unity Gain mode.

When an Op amp is available on a Op amp/Comparator module, both of its inputs and output are accessible at the device pins. The Op amp's Unity Gain mode is the only exception to this rule, which is described in **27.6 "Op amp Unity Gain Mode"**. The Op amp is disabled at reset and has to be enabled by writing a '1' to the OAO bit (CMxCON <11>), followed by enabling the Op amp by writing a '1' to the AMPMOD bit (CMxCON <10>).

The Op amp outputs are capable of rail-to-rail operation, which are limited by the maximum output load current. Refer to **36.0 "Electrical Characteristics"** for the Op amp minimum gain requirements and VOH/VOL loading specifications.

Note:	The exception to the minimum gain specification is the special internal Unity Gain buffer mode.

Table 27-1 provides the different SFR bits and their logic states to set the Op amp in two different modes of operation.

TABLE 27-1: OP AMP OPERATION STATES

Configuration	OAO bit (CMxCON<11>)	AMPMOD bit (CMxCON<10>)	ENPGAx bits (CFGCON2<4, 2:0>)
Op amp	1	1	0
Unity Gain Buffer	1	1	1
No function/disabled	0	0	0
Reserved	Don't care	0	1

27.2 Comparator Interface

The Comparators also have both their inverting and non-inverting inputs accessible via device pins. The non-inverting input pins can be connected to an internal 12-bit CDAC to generate a precise reference or to an external reference through a pin. These references can be individually selected for each comparator module. The inverting inputs can be connected to one of four external pins or internally to outputs of the Op amps. The Comparator outputs can be entirely disabled from appearing on the output pins, which relieves a pin for other uses, remapped to different pins via the peripheral pin select module, and selected to active-high or active-low polarity.

In Comparator modules that do not implement the Op amp, the Comparator module has a different input selection configuration.

The stand-alone Comparator implements a 4 x 1 multiplexer at the inverting input to enable selection of the desired signal to compare against the non-inverting input. Up to three outputs of Op amps can be internally connected to the Comparator via the multiplexer.

The Comparator may be enabled or disabled using the corresponding ON bit (CMxCON<15>) in the Op amp/ Comparator Control register. When the Comparator is disabled, the corresponding trigger and interrupt generation is disabled as well.

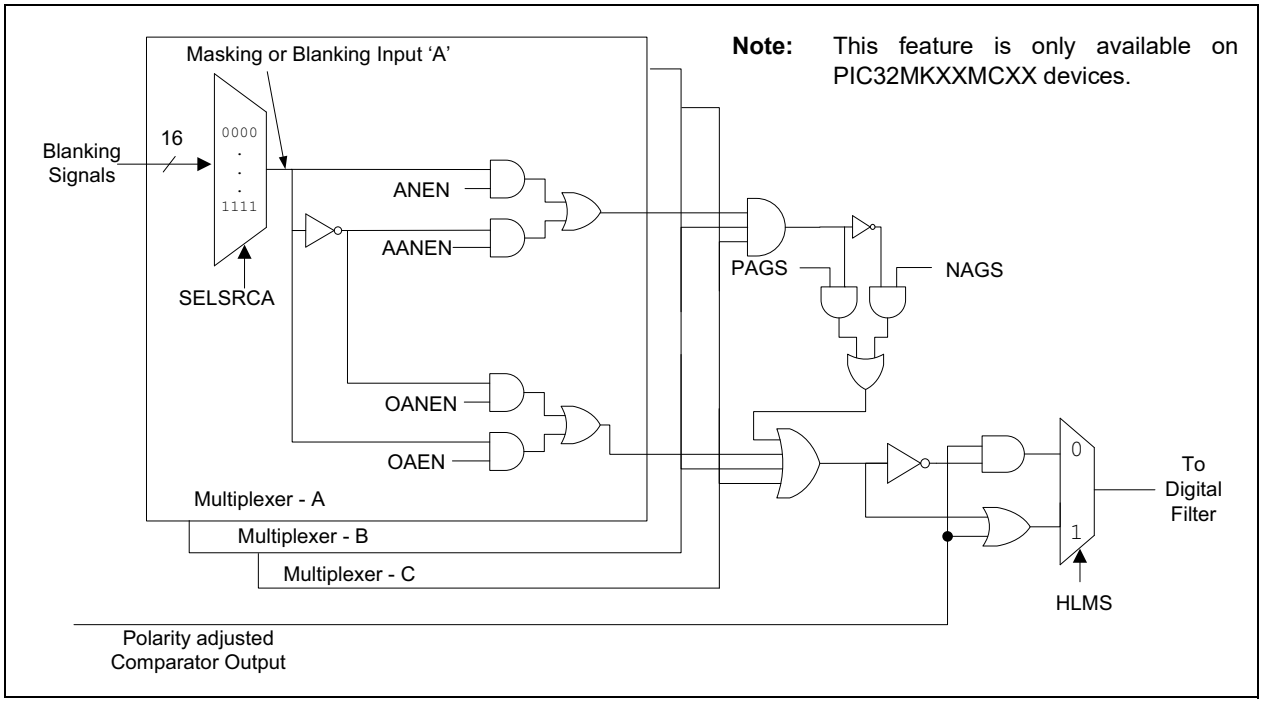
It is recommended to first configure the CMxCON register with all bits to the desired value, and then set the ON bit. When not used, the Comparator should be disabled expressly by writing a '0' to the ON bit.

27.3 Comparator Output Blanking

Comparator output blanking is a feature that is only available on PIC32MK Motor Control (i.e., PIC32MKXXMCXX) devices. The outputs of the Comparators can be further blanked/masked based on external events for programmable durations. This feature can be very useful in reducing the interrupt or trigger frequencies. It is primarily used to select Comparator events (interrupts and triggers) synchronized to desired edge transitions on external digital signals such as the PWM outputs from the MCPWM module. A prudent choice of these external signals has potential to greatly simplify software where otherwise extra software logic will be needed to arbitrate for the desired event source. Refer to the Comparator Mask Control Register, CMxMSKCON (Register 27-3), for details on the 16 different external signals that can be used for masking.

The logic AND, logic OR and multiplexer blocks shown in Figure 27-6 can be visualized as built-in programmable array logic used to reject the unwanted transitions of the comparator output. For each Comparator, the multiplexers A, B, and C can logically AND or OR either the positive or negative levels (edges) of the 16 different external signals. The outputs of the multiplexers can then be ANDed or ORed together with the AND logic outputs of the multiplexers being further capable of selection for positive or negative transitions as shown in the diagram. For a detailed usage of the output blanking feature, refer to **Section 39. "Op Amp/Comparator"** (DS60001178) of the *"PIC32 Family reference Manual"*.

FIGURE 27-6: USER PROGRAMMABLE BLANKING FUNCTION DIAGRAM



Note: This feature is only available on PIC32MKXXMCXX devices.

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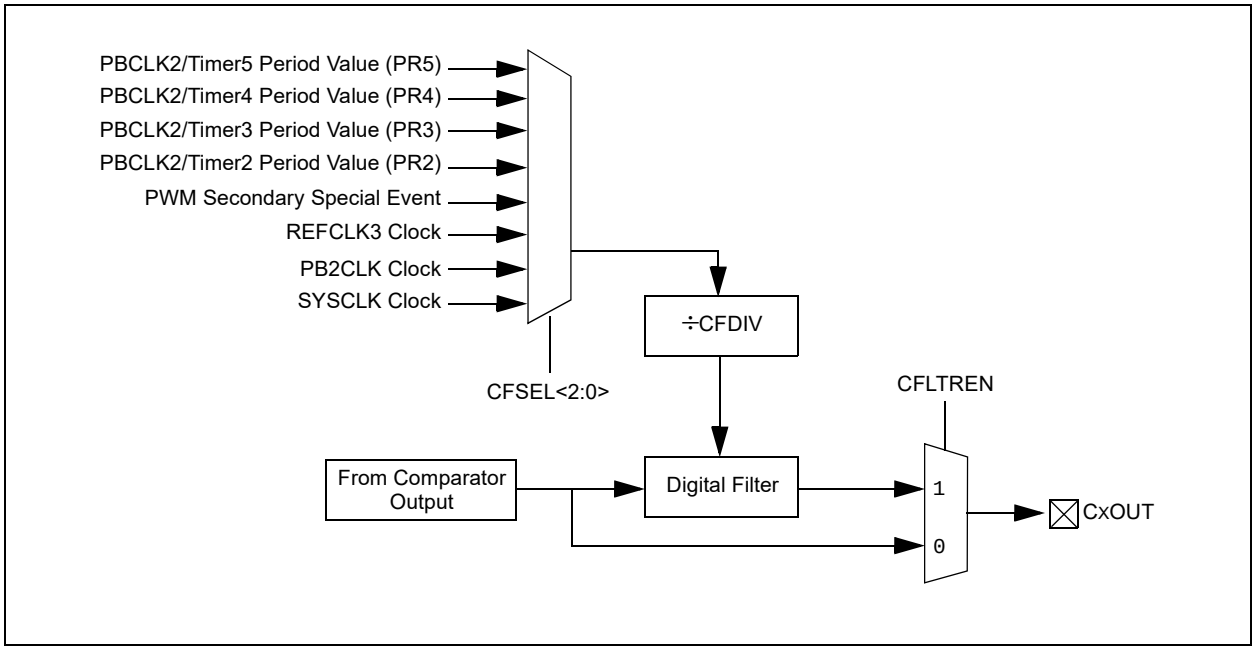
27.4 Comparator Output Filtering

The outputs can also be digitally filtered for glitches or noise. The digital filter has the capability to sample at different frequencies using different clock sources specified by the CFSEL<2:0> bits in the CxCON register. The digital filter looks for three consecutive samples of the same logic state before updating the comparator output. Since the digital filter affects the response times of the output, care should be taken while choosing the filter clock divisor to best suit the application at hand.

FIGURE 27-7: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



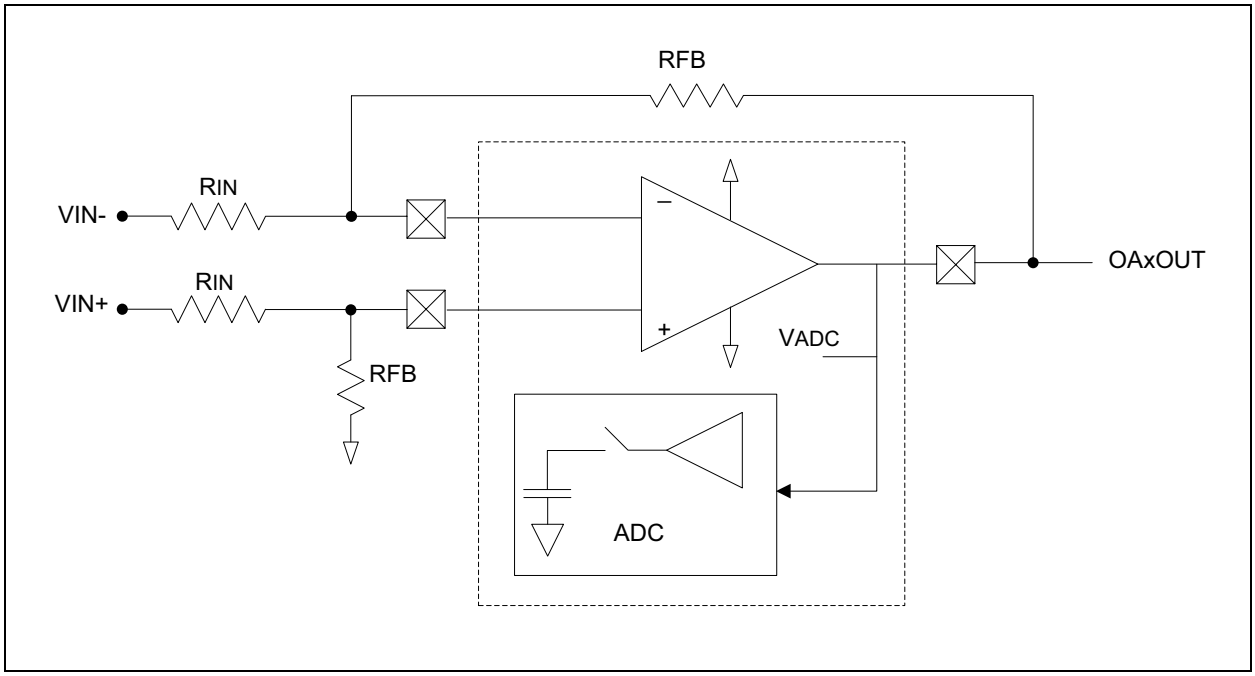
27.5 Op amp Mode

The Op amp in the Op amp/Comparator module can be enabled by writing a '1' to the AMPMOD bit (CMxCON<10>) and the OAO bit (CMxCON<11>). When configured this way, the output of the Op amp is available at the OAxOUT pin for the external gain/ filtering components to be added in the feedback path.

With the proper configuration of the ADC module, the op amp can be configured such that the ADC can directly sample the output of the op amp without the need to route the Op amp output to a separate analog input pin (see Figure 27-8).

Refer to Table 36-29 in **36.0 "Electrical Characteristics"** for minimum gain requirements and loading. The RFB in the differential amplifier configuration example must be part of any calculated max IOH/IOL load, see Figure 27-8.

FIGURE 27-8: OP AMPX DIFFERENTIAL AMPLIFIER EXAMPLE



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27.6 Op amp Unity Gain Mode

Usually the Op amps have a minimum gain stable setting as defined in Table 36-29 in **36.0 "Electrical Characteristics"**. However, there is one exception in that the Op amps have an internal 1x gain setting (i.e., the ENPGAx bits in the CFGCON2 register = 1). The mode utilizes only the inverting input pin of the Op amp. This configuration needs no external components. The Op amps will be placed in a unity gain/follower mode following a software write to these bits:

- CFGCON2<16> for Op amp 1
- CFGCON2<17> for Op amp 2
- CFGCON2<18> for Op amp 3
- CFGCON2<20> for Op amp 5

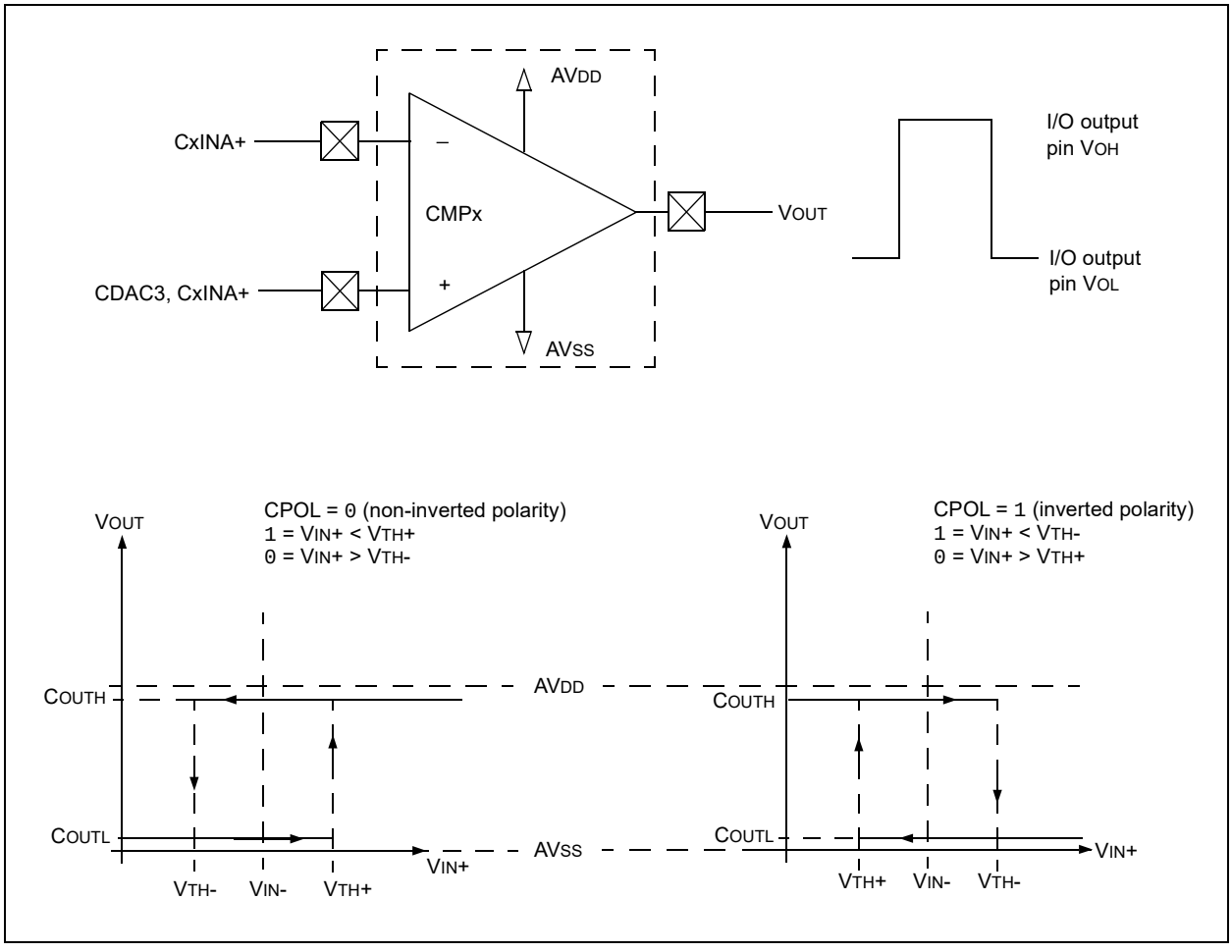
Please refer to **36.0 "Electrical Characteristics"** for the specifications in this mode.

27.7 Comparator Configuration

The Comparator and the relationship between the analog input levels and the digital output are illustrated in Figure 27-9. Each Comparator can be individually configured to compare against an external voltage reference or internal voltage reference. For more information on the internal op amp/comparator voltage reference, refer to **Section 45. "Control Digital-to-Analog converter"** (DS60001327) of the *"PIC32 Family Reference Manual"*.

A standard configuration with default built in hysteresis is shown in Figure 27-9. The external reference at VIN+ is a fixed voltage. The analog input signal at VIN- is compared to the reference signal at VIN+, and the digital output of the comparator is created by the difference between the two signals as shown in the figure. The polarity of the comparator output can be inverted by writing a '1' to the CPOL bit (CMxCON<13>) such that the output is a digital low level when VIN+ > VIN-.

FIGURE 27-9: COMPARATOR CONFIGURATION FOR DEFAULT BUILT-IN HYSTERESIS



27.8 Op amp/Comparator Control Registers

TABLE 27-2: OP AMP/COMPARATOR REGISTER MAP

Virtual Address (BF82)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
C000	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT	0000
C010	CM1CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	OAO	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C020	CM1MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C030	CM2CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	OAO	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C040	CM2MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C050	CM3CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	OAO	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C060	CM3MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C070	CM4CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C080	CM4MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
C090	CM5CON	31:16	—	—	—	—	—	—	—	—	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>			0000
		15:0	ON	COE	CPOL	—	OAO	AMPMOD	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
C0A0	CM5MSKCON(2)	31:16	—	—	—	—	SELSRCC<3:0>				SELSRCB<3:0>				SELSRCA<3:0>				0000
		15:0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: This register is only available on PIC32MKXXMCXX devices.

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REGISTER 27-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation of all Op amp/Comparators when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-5 **Unimplemented:** Read as '0'

bit 4-0 **C5OUT:C1OUT:** Op amp/Comparator 5 through Comparator 1 Output Status bit
When CPOL = 0:
1 = $V_{IN+} > V_{TH+}$
0 = $V_{IN+} < V_{TH-}$
When CPOL = 1:
1 = $V_{IN+} < V_{TH-}$
0 = $V_{IN+} > V_{TH+}$

REGISTER 27-2: CMxCON: OP AMP/COMPARATOR 'x' CONTROL REGISTER ('x' = 1-5)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	CFSEL<2:0>			CFLTREN	CFDIV<2:0>		
15:8	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	R-0
	ON	COE	CPOL	—	OAO(1)	AMPMOD(1)	—	COUT
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22-20 **CFSEL<2:0>:** Comparator Output Filter Clock Source Select bits
111 = PBCLK2/Timer5 Period Value (PR5)
110 = PBCLK2/Timer4 Period Value (PR4)
101 = PBCLK2/Timer3 Period Value (PR3)
100 = PBCLK2/Timer2 Period Value (PR2)
011 = REFCLK3 Clock
010 = PWM Secondary Special Event
001 = PPBCLK2 Clock
000 = SYSCLK Clock

bit 19 **CFLTREN:** Comparator Output Digital Filter Enable bit
1 = Digital Filters enabled
0 = Digital Filters disabled

bit 18-16 **CFDIV<2:0>:** Comparator Output Filter Clock Divide Select bits
These bits are based on the CFSEL clock source selection.
111 = 1:128 Clock Divide
110 = 1:64 Clock Divide
101 = 1:32 Clock Divide
100 = 1:16 Clock Divide
011 = 1:8 Clock Divide
010 = 1:4 Clock Divide
001 = 1:2 Clock Divide
000 = 1:1 Clock Divide

bit 15 **ON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

Note 1: Before attempting to initialize or enable any of the Op amp bit, the user application must clear the corresponding OPA5MD, OPA3MD, OPA2MD, and OPA1MD bits in the PMD register.

Note: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition is occurred. The IFSx bits are persistent, so they must be cleared if they are set by user software after an IFSx user bit interrogation.

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REGISTER 27-2: CMxCON: OP AMP/COMPARATOR 'x' CONTROL REGISTER ('x' = 1-5) (CONTINUED)

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12 **Unimplemented:** Read as '0'

bit 11 **OAO:** Op amp Output Enable bit(1)
1 = Op amp output is present on the OAxOUT pin
0 = Op amp output is not present on the OAxOUT pin

bit 10 **AMPMOD:** Op amp Mode Enable bit(1)
1 = Amplifier/Comparator operating in Dual mode (both Op amps and Comparators are enabled)
0 = Amplifier/Comparator operating in Comparator-only mode

bit 9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{TH+}$
0 = $V_{IN+} < V_{TH-}$

When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{TH-}$
0 = $V_{IN+} > V_{TH+}$

bit 7-6 **EVPOL<1:0>:** Trigger/Event Polarity Select bits
11 = Trigger/Event generated on any change of the comparator output
10 = Trigger/Event generated only on high-to-low transition of the polarity-selected comparator output
If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output
If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output
01 = Trigger/Event generated only on low-to-high transition of the polarity-selected comparator output
If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output
If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output
00 = Trigger/Event generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Op amp/Comparator Reference Select bit
1 = V_{IN+} input connects to internal CDAC3 output voltage
0 = V_{IN+} input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

Note 1: Before attempting to initialize or enable any of the Op amp bit, the user application must clear the corresponding OPA5MD, OPA3MD, OPA2MD, and OPA1MD bits in the PMD register.

Note: The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition is occurred. The IFSx bits are persistent, so they must be cleared if they are set by user software after an IFSx user bit interrogation.

REGISTER 27-2: CMxCON: OP AMP/COMPARATOR 'x' CONTROL REGISTER ('x' = 1-5) (CONTINUED)

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = CxIN4-
10 = CxIN3-
01 = CxIN2-
00 = CxIN1-

Note 1: Before attempting to initialize or enable any of the Op amp bit, the user application must clear the corresponding OPA5MD, OPA3MD, OPA2MD, and OPA1MD bits in the PMD register.

Note:	The IFSx bits, as with all interrupt flag status register bits, are set as long as the peripheral is enabled and an interrupt condition event occurs. Interrupts do not have to be enabled for the IFSx bits to be set. If the user application does not want to use an interrupt, it can poll the corresponding peripheral IFSx bit to see whether an interrupt condition is occurred. The IFSx bits are persistent, so they must be cleared if they are set by user software after an IFSx user bit interrogation.

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REGISTER 27-3: CMxMSKCON: COMPARATOR 'x' MASK CONTROL REGISTER ('x' = 1-5)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	SELSRCC<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SELSRCB<3:0>				SELSRCA<3:0>			
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-24 **SELSRCC<3:0>:** Mask C Input Select bits
See the definitions for the SELSRCA<3:0> bits.

bit 23-20 **SELSRCB<3:0>:** Mask B Input Select bits
See the definitions for the SELSRCA<3:0> bits.

bit 19-16 **SELSRCA<3:0>:** Mask A Input Select bits
1111 = FLT4 pin
1110 = FLT2 pin
1101 = Reserved
1100 = Reserved
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 15 **HLMS:** High or Low Level Masking Select bit
1 = The comparator deasserted state is 1, and the masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The comparator deasserted state is 0, and the masking (blanking) function will prevent any asserted ('1') comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate "C" Input Enable bit
1 = "C" input enabled as input to OR gate
0 = "C" input disabled as input to OR gate

Note: This register is only available on PIC32MKXXMCXXX devices.

REGISTER 27-3: CMxMSKCON: COMPARATOR 'x' MASK CONTROL REGISTER ('x' = 1-5) (CONTINUED)

bit 12 **OCNEN:** OR Gate "C" Input Inverted Enable bit
1 = "C" input (inverted) enabled as input to OR gate
0 = "C" input (inverted) disabled as input to OR gate

bit 11 **OBEN:** OR Gate "B" Input Enable bit
1 = "B" input enabled as input to OR gate
0 = "B" input disabled as input to OR gate

bit 10 **OBNEN:** OR Gate "B" Input Inverted Enable bit
1 = "B" input (inverted) enabled as input to OR gate
0 = "B" input (inverted) disabled as input to OR gate

bit 9 **OAEN:** OR Gate "A" Input Enable bit
1 = "A" input enabled as input to OR gate
0 = "A" input disabled as input to OR gate

bit 8 **OANEN:** OR Gate "A" Input Inverted Enable bit
1 = "A" input (inverted) enabled as input to OR gate
0 = "A" input (inverted) disabled as input to OR gate

bit 7 **NAGS:** Negative AND Gate Output Select bit
1 = The negative (inverted) output of the AND gate to the OR gate is enabled
0 = The negative (inverted) output of the AND gate to the OR gate is disabled

bit 6 **PAGS:** Positive AND Gate Output Select bit
1 = The positive output of the AND gate to the OR gate is enabled
0 = The positive output of the AND gate to the OR gate is disabled

bit 5 **ACEN:** AND Gate "C" Input Enable bit
1 = "C" input enabled as input to AND gate
0 = "C" input disabled as input to AND gate

bit 4 **ACNEN:** AND Gate "C" Inverted Input Enable bit
1 = "C" input (inverted) enabled as input to AND gate
0 = "C" input (inverted) disabled as input to AND gate

bit 3 **ABEN:** AND Gate "B" Input Enable bit
1 = "B" input enabled as input to AND gate
0 = "B" input disabled as input to AND gate

bit 2 **ABNEN:** AND Gate "B" Inverted Input Enable bit
1 = "B" input (inverted) enabled as input to AND gate
0 = "B" input (inverted) disabled as input to AND gate

bit 1 **AAEN:** AND Gate "A" Input Enable bit
1 = "A" input enabled as input to AND gate
0 = "A" input disabled as input to AND gate

bit 0 **AANEN:** AND Gate "A" Inverted Input Enable bit
1 = "A" input (inverted) enabled as input to AND gate
0 = "A" input (inverted) disabled as input to AND gate

Note: This register is only available on PIC32MKXXMCXXX devices.

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28.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

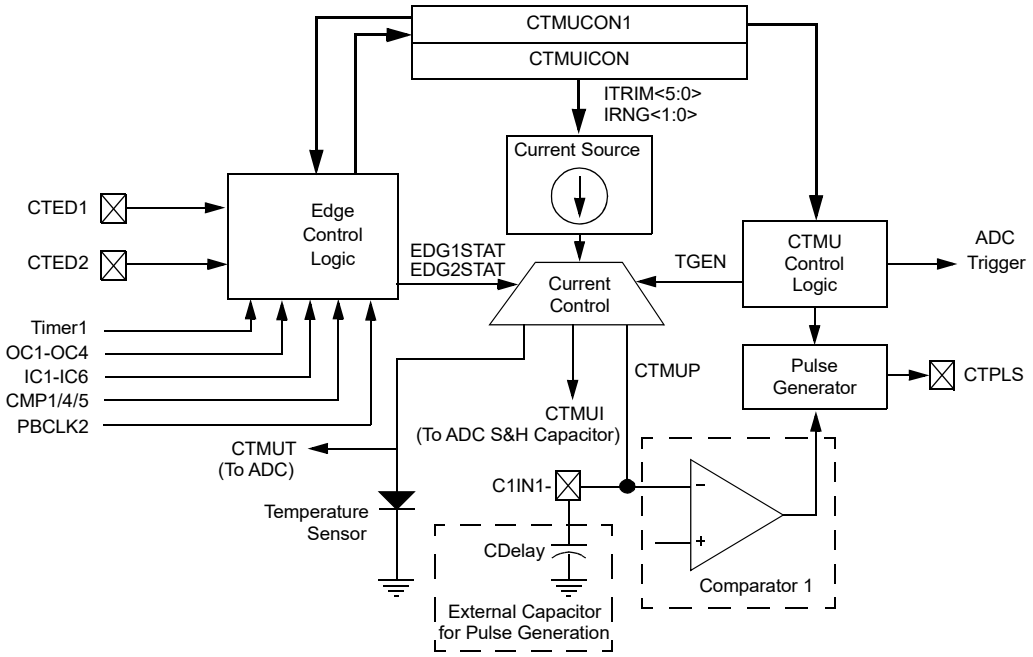
The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Two channels available for capacitive or time measurement input
- On-chip precision current source
- 16-edge input trigger sources
- Selection of edge or level-sensitive inputs
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- Control of current source during auto-sampling
- Four current source ranges
- Time measurement resolution of one nanosecond
- Up to 39 inputs for capacitive measurement

A block diagram of the CTMU is shown in Figure 28-1.

FIGURE 28-1: CTMU BLOCK DIAGRAM



Current Control Selection	TGEN	EDG1STAT, EDG2STAT
CTMUT	0	EDG1STAT = EDG2STAT
CTMUI	0	EDG1STAT ≠ EDG2STAT
CTMUP	1	EDG1STAT ≠ EDG2STAT
No Connect	1	EDG1STAT = EDG2STAT

28.1 Control Registers

TABLE 28-1: CTMU REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
D000	CTMUCON	31:16	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—	0000
		15:0	ON	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	ITRIM<5:0>						IRNG<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EDG1MOD	EDG1POL	EDG1SEL<3:0>				EDG2STAT	EDG1STAT
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	EDG2MOD	EDG2POL	EDG2SEL<3:0>				—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	CTMUSIDL	TGEN(1)	EDGEN	EDGSEQEN	IDISSEN(2)	CTTRIG
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ITRIM<5:0>						IRNG<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **EDG1MOD:** Edge 1 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 30 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 programmed for a positive edge response
0 = Edge 1 programmed for a negative edge response

bit 29-26 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = C5OUT Capture Event is selected
1110 = C4OUT pin is selected
1101 = C1OUT pin is selected
1100 = PBCLK2 is selected
1011 = IC5 Capture Event is selected
1010 = IC4 Capture Event is selected
1001 = IC3 pin is selected
1000 = IC2 pin is selected
0111 = IC1 pin is selected
0110 = OC4 pin is selected
0101 = OC3 pin is selected
0100 = OC2 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1101' to select C1OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 36-43) in **Section 36.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

5: For CTMU temperature measurements on this range, ADC sampling time ≥ 1.6 µs.

6: For CTMU temperature measurements on this range, ADC sampling time ≥ 300 ns.

REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 25 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control edge source
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 24 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control edge source
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 23 **EDG2MOD:** Edge 2 Edge Sampling Select bit
1 = Input is edge-sensitive
0 = Input is level-sensitive

bit 22 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 programmed for a positive edge response
0 = Edge 2 programmed for a negative edge response

bit 21-18 **EDG2SEL<3:0>:** Edge 2 Source Select bits
1111 = C5OUT Capture Event is selected
1110 = C4OUT pin is selected
1101 = C1OUT pin is selected
1100 = IC6 Capture Event is selected
1011 = IC5 Capture Event is selected
1010 = IC4 Capture Event is selected
1001 = IC3 pin is selected
1000 = IC2 pin is selected
0111 = IC1 pin is selected
0110 = OC4 pin is selected
0101 = OC3 pin is selected
0100 = OC2 pin is selected
0011 = CTED1 pin is selected
0010 = CTED2 pin is selected
0001 = OC1 Compare Event is selected
0000 = Timer1 Event is selected

bit 17-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ON Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1101' to select C1OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 36-43) in **Section 36.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

5: For CTMU temperature measurements on this range, ADC sampling time ≥ 1.6 µs.

6: For CTMU temperature measurements on this range, ADC sampling time ≥ 300 ns.

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REGISTER 28-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 12 **TGEN:** Time Generation Enable bit(1)
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Edges are not blocked
0 = Edges are blocked

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 must occur before Edge 2 can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
11 = 100 times base current (i.e., 55 µA Typical(6))
10 = 10 times base current (i.e., 5.5 µA Typical(5))
01 = Base current level (i.e., 0.55 µA Typical(4))
00 = 1000 times base current (i.e., 550 µA Typical(4))

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1101' to select C1OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 36-43) in **Section 36.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

5: For CTMU temperature measurements on this range, ADC sampling time ≥ 1.6 µs.

6: For CTMU temperature measurements on this range, ADC sampling time ≥ 300 ns.

NOTES:

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29.0 CONTROL DIGITAL-TO-ANALOG CONVERTER (CDAC)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 45. "Control Digital-to-Analog Converter (CDAC)"** (DS60001327), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MK GP/MC Family Control Digital-to-Analog Converter (CDAC) generates analog voltage corresponding to the digital inputs. The voltage can be used as a reference source for comparators or can be used as an offset to an Op amp. This module is targeted for control applications, as opposed to other DAC modules, which are used for audio applications.

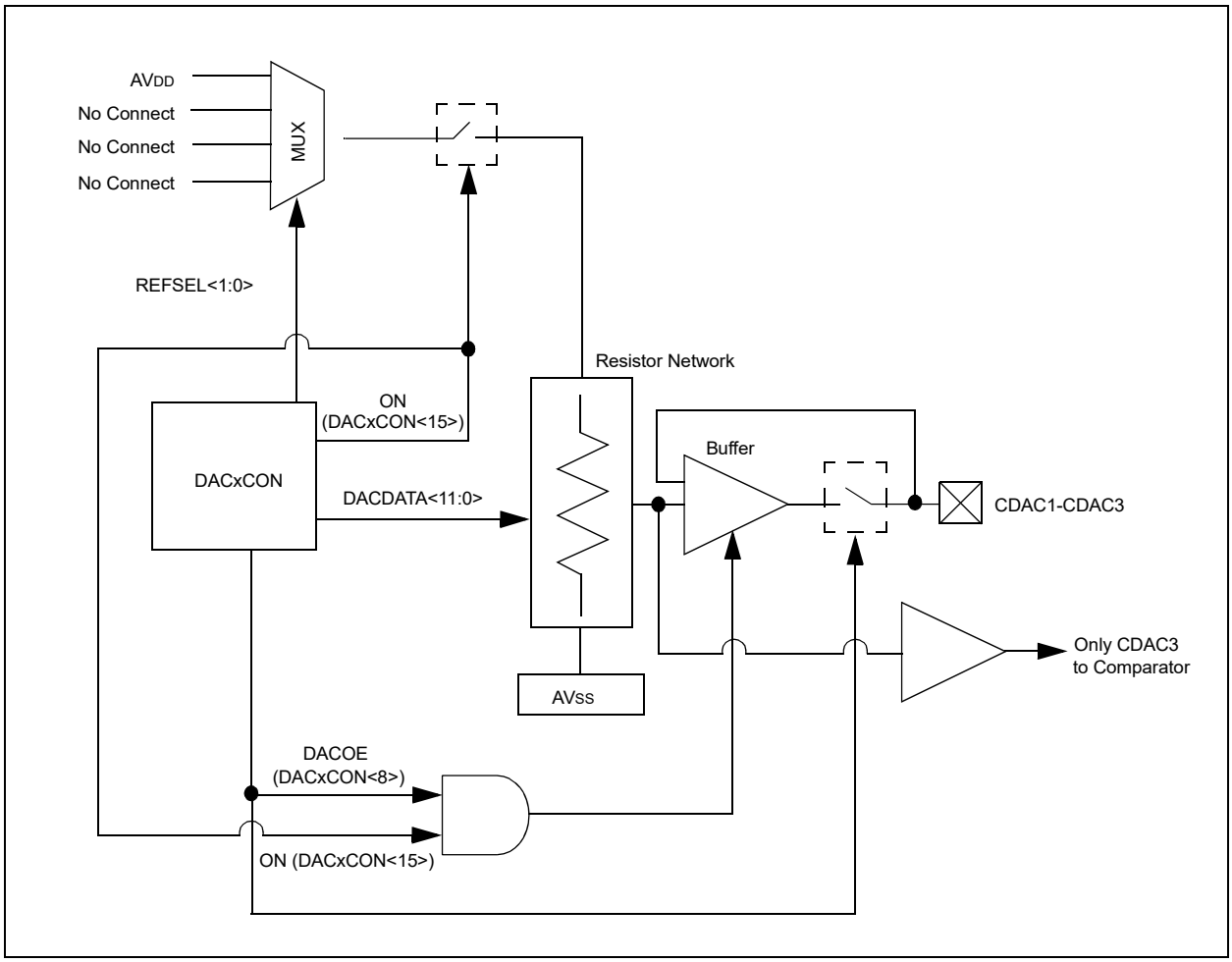
The following are key features of the CDAC module:

- Wide voltage range (1.8V to 3.6V)
- 12-bit resolution
- Fast conversion times, 1 Msps
- Buffered output for comparator use

Note: For additional information on conversion time, sampling rate, module turn-on time and glitch reduction circuit characteristics, refer to **Section 36.0 "Electrical Characteristics"**.

Figure 29-1 illustrates the functional block diagram of the CDAC module.

FIGURE 29-1: CDAC BLOCK DIAGRAM



29.1 Control Registers

TABLE 29-1: CDAC REGISTER MAP

Virtual Address	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
BF82_C200	DAC1CON	31:16	—	—	—	—	DACDAT<11:0>												0000
		15:0	ON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>		0000
BF84_C400	DAC2CON	31:16	—	—	—	—	DACDAT<11:0>												0000
		15:0	ON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>		0000
BF84_C600	DAC3CON	31:16	—	—	—	—	DACDAT<11:0>												0000
		15:0	ON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 29-1: DACxCON: CDAC CONTROL REGISTER 'x' ('x' = 1 THROUGH 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	DACDAT<11:8>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DACDAT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	ON(1)	—	—	—	—	—	—	DACOE(1)
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>(1,2)	

Legend:	y = Value set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27-16 **DACDAT<11:0>:** CDAC Data Port bits(1)
Data input register bits for the CDAC.

bit 15 **ON:** CDAC Enable bit
1 = The CDAC is enabled
0 = The CDAC is disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **DACOE:** CDAC Output Buffer Enable bit
1 = Output is enabled; CDAC voltage is connected to the pin
0 = Output is disabled; drive to pin is floating

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REFSEL<1:0>:** Reference Source Select bits(1,2)
11 = Positive reference voltage = AVDD
10 = No reference selected (no reference current consumption)
01 = No reference selected (no reference current consumption)
00 = No reference selected (no reference current consumption)

Note 1: To minimize CDAC start-up output transients, configure the DACDATA<15:0>, DACOE, and REFSEL<1:0> bits prior to enabling the CDAC (prior to making DACON = 1). Also, remember to wait TON time, after enabling the CDAC. This time is required to allow the CDAC output to stabilize. Refer to **Section 36.0 "Electrical Characteristics"** for the TON specification.

2: If the ON bit is '0', the reference source is disconnected from the internal resistor network.

NOTES:

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30.0 QUADRATURE ENCODER INTERFACE (QEI)

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 43. "Quadrature Encoder Interface (QEI)"** (DS60001346), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

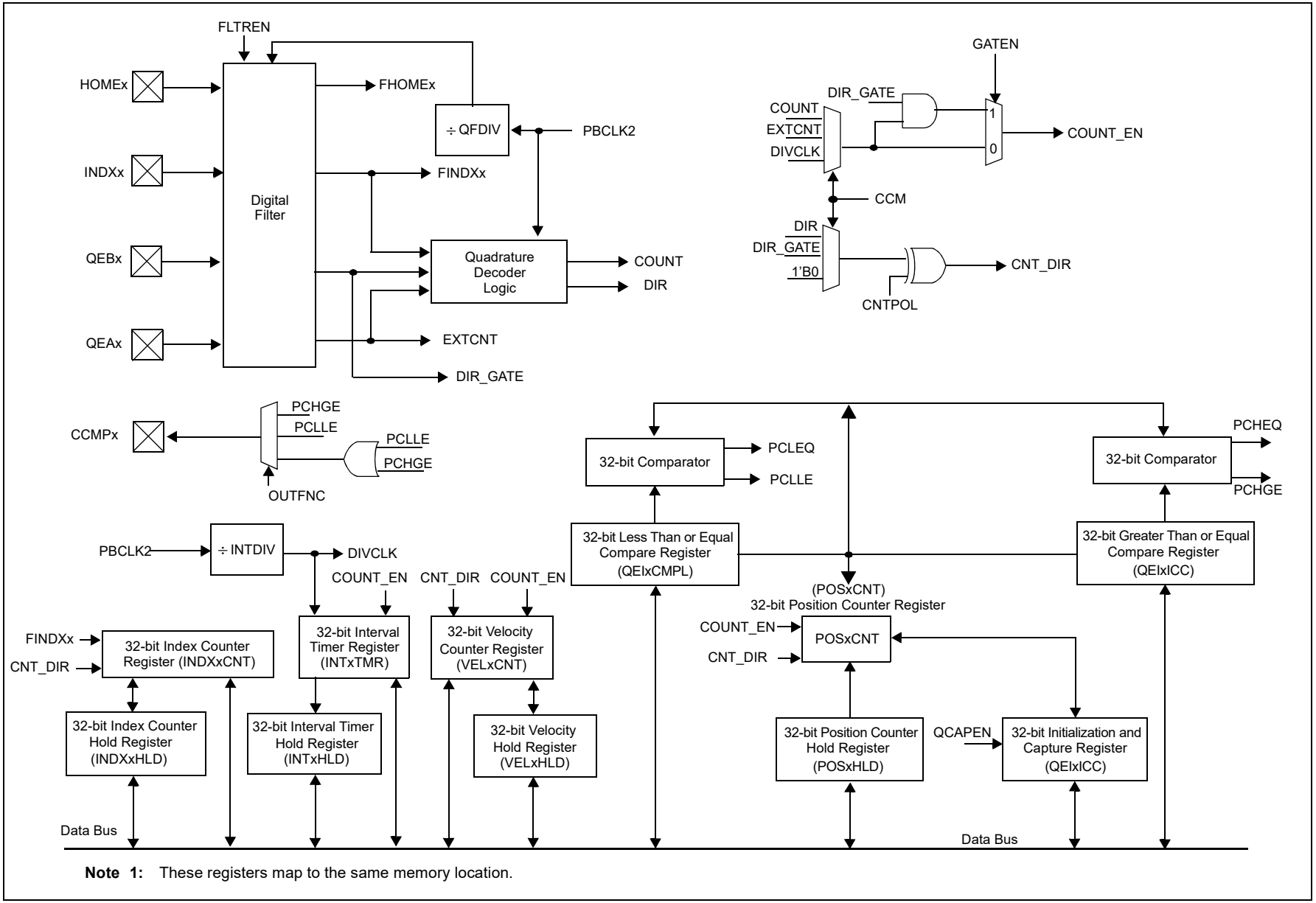
This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The QEI module consists of the following major features:

- Four input pins: two phase signals, an index pulse and a home pulse
- Programmable digital noise filters on inputs
- Quadrature decoder providing counter pulses and count direction
- Count direction status
- 4x count resolution
- Index (INDX) pulse to reset the position counter
- General purpose 32-bit Timer/Counter mode
- Interrupts generated by QEI or counter events
- 32-bit velocity counter
- 32-bit position counter
- 32-bit index pulse counter
- 32-bit interval timer
- 32-bit position Initialization/Capture register
- 32-bit Compare Less Than and Greater Than registers
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Interval Timer mode

Figure 30-1 illustrates the QEI block diagram.

FIGURE 30-1: QEI BLOCK DIAGRAM



Note 1: These registers map to the same memory location.

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30.1 QEI Control Registers

TABLE 30-1: QEI1 THROUGH QEI6 REGISTER MAP

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B200	QEI1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	QEIEN	—	QEISIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
B210	QEI1IOC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HCAPEN	0000
		15:0	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	0000
B220	QEI1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
B230	POS1CNT	31:16	POSCNT<31:16>																0000
		15:0	POSCNT<15:0>																0000
B240	POS1HLD	31:16	POSHLD<31:16>																0000
		15:0	POSHLD<15:0>																0000
B250	VEL1CNT	31:16	VELCNT<31:16>																0000
		15:0	VELCNT<15:0>																0000
B260	VEL1HLD	31:16	VELHLD<31:16>																0000
		15:0	VELHLD<15:0>																0000
B270	INT1TMR	31:16	INTTMR<31:16>																0000
		15:0	INTTMR<15:0>																0000
B280	INT1HLD	31:16	INTHLD<31:16>																0000
		15:0	INTHLD<15:0>																0000
B290	INDX1CNT	31:16	INDXCNT<31:16>																0000
		15:0	INDXCNT<15:0>																0000
B2A0	INDX1HLD	31:16	INDXHLD<31:16>																0000
		15:0	INDXHLD<15:0>																0000
B2B0	QEI1ICC	31:16	QEIICC<31:16>																0000
		15:0	QEIICC<15:0>																0000
B2C0	QEI1CMPL	31:16	QEICMPL<31:16>																0000
		15:0	QEICMPL<15:0>																0000
B400	QEI2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	QEIEN	—	QEISIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
B410	QEI2IOC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HCAPEN	0000
		15:0	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 30-1: QEI1 THROUGH QEI6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B420	QEI2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
B430	POS2CNT	31:16	POSCNT<31:16>																0000
		15:0	POSCNT<15:0>																0000
B440	POS2HLD	31:16	POSHLD<31:16>																0000
		15:0	POSHLD<15:0>																0000
B450	VEL2CNT	31:16	VELCNT<31:16>																0000
		15:0	VELCNT<15:0>																0000
B460	VEL2HLD	31:16	VELHLD<31:16>																0000
		15:0	VELHLD<15:0>																0000
B470	INT2TMR	31:16	INTTMR<31:16>																0000
		15:0	INTTMR<15:0>																0000
B480	INT2HLD	31:16	INTHLD<31:16>																0000
		15:0	INTHLD<15:0>																0000
B490	INDX2CNT	31:16	INDXCNT<31:16>																0000
		15:0	INDXCNT<15:0>																0000
B4A0	INDX2HLD	31:16	INDXHLD<31:16>																0000
		15:0	INDXHLD<15:0>																0000
B4B0	QEI2ICC	31:16	QEIICC<31:16>																0000
		15:0	QEIICC<15:0>																0000
B4C0	QEI2CMPL	31:16	QEICMPL<31:16>																0000
		15:0	QEICMPL<15:0>																0000
B600	QEI3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	QEIEN	—	QEISIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
B610	QEI3IOC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HCAPEN	0000
		15:0	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	0000
B620	QEI3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
B630	POS3CNT	31:16	POSCNT<31:16>																0000
		15:0	POSCNT<15:0>																0000
B640	POS3HLD	31:16	POSHLD<31:16>																0000
		15:0	POSHLD<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 30-1: QEI1 THROUGH QEI6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B650	VEL3CNT	31:16	VELCNT<31:16>																0000
		15:0	VELCNT<15:0>																0000
B660	VEL3HLD	31:16	VELHLD<31:16>																0000
		15:0	VELHLD<15:0>																0000
B670	INT3TMR	31:16	INTTMR<31:16>																0000
		15:0	INTTMR<15:0>																0000
B680	INT3HLD	31:16	INTHLD<31:16>																0000
		15:0	INTHLD<15:0>																0000
B690	INDX3CNT	31:16	INDXCNT<31:16>																0000
		15:0	INDXCNT<15:0>																0000
B6A0	INDX3HLD	31:16	INDXHLD<31:16>																0000
		15:0	INDXHLD<15:0>																0000
B6B0	QEI3ICC	31:16	QEIICC<31:16>																0000
		15:0	QEIICC<15:0>																0000
B6C0	QEI3CMPL	31:16	QEICMPL<31:16>																0000
		15:0	QEICMPL<15:0>																0000
B800	QEI4CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	QEIEN	—	QEISIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
B810	QEI4IOC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HCAPEN	0000
		15:0	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	0000
B820	QEI4STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
B830	POS4CNT	31:16	POSCNT<31:16>																0000
		15:0	POSCNT<15:0>																0000
B840	POS4HLD	31:16	POSHLD<31:16>																0000
		15:0	POSHLD<15:0>																0000
B850	VEL4CNT	31:16	VELCNT<31:16>																0000
		15:0	VELCNT<15:0>																0000
B860	VEL4HLD	31:16	VELHLD<31:16>																0000
		15:0	VELHLD<15:0>																0000
B870	INT4TMR	31:16	INTTMR<31:16>																0000
		15:0	INTTMR<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 30-1: QEI1 THROUGH QEI6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B880	INT4HLD	31:16	INTHLD<31:16>																0000
		15:0	INTHLD<15:0>																0000
B890	INDX4CNT	31:16	INDXCNT<31:16>																0000
		15:0	INDXCNT<15:0>																0000
B8A0	INDX4HLD	31:16	INDXHLD<31:16>																0000
		15:0	INDXHLD<15:0>																0000
B8B0	QEI4ICC	31:16	QEIICC<31:16>																0000
		15:0	QEIICC<15:0>																0000
B8C0	QEI4CMPL	31:16	QEICMPL<31:16>																0000
		15:0	QEICMPL<15:0>																0000
BA00	QEI5CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	QEIEN	—	QEISIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
BA10	QEI5IOC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HCAPEN	0000
		15:0	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	0000
BA20	QEI5STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
BA30	POS5CNT	31:16	POSCNT<31:16>																0000
		15:0	POSCNT<15:0>																0000
BA40	POS5HLD	31:16	POSHLD<31:16>																0000
		15:0	POSHLD<15:0>																0000
BA50	VEL5CNT	31:16	VELCNT<31:16>																0000
		15:0	VELCNT<15:0>																0000
BA60	VEL5HLD	31:16	VELHLD<31:16>																0000
		15:0	VELHLD<15:0>																0000
BA70	INT5TMR	31:16	INTTMR<31:16>																0000
		15:0	INTTMR<15:0>																0000
BA80	INT5HLD	31:16	INTHLD<31:16>																0000
		15:0	INTHLD<15:0>																0000
BA90	INDX5CNT	31:16	INDXCNT<31:16>																0000
		15:0	INDXCNT<15:0>																0000
BAA0	INDX5HLD	31:16	INDXHLD<31:16>																0000
		15:0	INDXHLD<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

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TABLE 30-1: QEI1 THROUGH QEI6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
BAB0	QEI5ICC	31:16	QEIICC<31:16>																0000
		15:0	QEIICC<15:0>																0000
BAC0	QEI5CMPL	31:16	QEICMPL<31:16>																0000
		15:0	QEICMPL<15:0>																0000
BC00	QEI6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	QEIEN	—	QEISIDL	PIMOD<2:0>			IMV<1:0>		—	INTDIV<2:0>			CNTPOL	GATEN	CCM<1:0>		0000
BC10	QEI6IOC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HCAPEN	0000
		15:0	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	0000
BC20	QEI6STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
BC30	POS6CNT	31:16	POSCNT<31:16>																0000
		15:0	POSCNT<15:0>																0000
BC40	POS6HLD	31:16	POSHLD<31:16>																0000
		15:0	POSHLD<15:0>																0000
BC50	VEL6CNT	31:16	VELCNT<31:16>																0000
		15:0	VELCNT<15:0>																0000
BC60	VEL6HLD	31:16	VELHLD<31:16>																0000
		15:0	VELHLD<15:0>																0000
BC70	INT6TMR	31:16	INTTMR<31:16>																0000
		15:0	INTTMR<15:0>																0000
BC80	INT6HLD	31:16	INTHLD<31:16>																0000
		15:0	INTHLD<15:0>																0000
BC90	INDX6CNT	31:16	INDXCNT<31:16>																0000
		15:0	INDXCNT<15:0>																0000
BCA0	INDX6HLD	31:16	INDXHLD<31:16>																0000
		15:0	INDXHLD<15:0>																0000
BCB0	QEI6ICC	31:16	QEIICC<31:16>																0000
		15:0	QEIICC<15:0>																0000
BCC0	QEI6CMPL	31:16	QEICMPL<31:16>																0000
		15:0	QEICMPL<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 13.2 "CLR, SET, and INV Registers"** for more information.

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REGISTER 30-1: QEIxCON: QEIx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	QEIEN	—	QEISIDL	PIMOD<2:0>(1)			IMV<1:0>(2)	
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	INTDIV<2:0>(3)			CNTPOL	GATEN	CCM<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **QEIEN:** Quadrature Encoder Interface Module Counter Enable bit
- 1 = Module counters are enabled
- 0 = Module counters are disabled, but SFRs can be read or written

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12-10 **PIMOD<2:0>:** Position Counter Initialization Mode Select bits(1)
- 111 = Modulo Count mode for position counter and every index event resets the position counter
- 110 = Modulo Count mode for position counter
- 101 = Resets the position counter when the position counter equals QEIxICCH register
- 100 = Second index event after home event initializes position counter with contents of QEIxICCH register
- 011 = First index event after home event initializes position counter with contents of QEIxICCH register
- 010 = Next index input event initializes the position counter with contents of QEIxICCH register
- 001 = Every Index input event resets the position counter
- 000 = Index input event does not affect position counter

bit 9-8 **IMV<1:0>:** Index Match Value bits(2)
- 11 = Index match occurs when QEB = 1 and QEA = 1
- 10 = Index match occurs when QEB = 1 and QEA = 0
- 01 = Index match occurs when QEB = 0 and QEA = 1
- 00 = Index match occurs when QEB = 0 and QEA = 0

bit 7 **Unimplemented:** Read as '0'

Note 1: When CCM equals modes '01', '10', and '11', all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM = 00 and QEA and QEB values match Index Match Value (IMV), the POSxCNTH and POSxCNTL registers are reset.

3: The selected clock rate must be at least twice the expected maximum quadrature count rate.

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REGISTER 30-1: QEIxCON: QEIx CONTROL REGISTER (CONTINUED)

bit 6-4 **INTDIV<2:0>:** Timer Input Clock Prescale Select bits (Interval timer, Main timer (position counter), velocity counter and index counter internal clock divider select)(3)

111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit **CNTPOL:** Position and Index Counter/Timer Direction Select bit

1 = Counter direction is negative unless modified by external Up/Down signal
0 = Counter direction is positive unless modified by external Up/Down signal

bit **GATEN:** External Count Gate Enable bit

1 = External gate signal controls position counter operation
0 = External gate signal does not affect position counter/timer operation

bit **CCM<1:0>:** Counter Control Mode Selection bits

11 = Internal Timer mode with optional QEB external clock gating input control based on GATEN.
QEB High = Timer Run, QEB Low = Timer Stop.
10 = QEA is the external clock input, QEB is optional clock gating input control based on GATEN.
QEB High = Clock Run, QEB Low = Clock Stop.
01 = QEA is the external clock input, QEB is external UP/DN direction input.
QEB High = Count Up, QEB Low = Count Down
00 = Quadrature Encoder Interface Count mode (x4 mode)

Note 1: When CCM equals modes '01', '10', and '11', all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM = 00 and QEA and QEB values match Index Match Value (IMV), the POSxCNTH and POSxCNTL registers are reset.

3: The selected clock rate must be at least twice the expected maximum quadrature count rate.

REGISTER 30-2: QEIxIOC: QEIx I/O CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	HCAPEN
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	QCAPEN	FLTREN	QFDIV<2:0>			OUTFNC<1:0>		SWPAB
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-17 **Unimplemented:** Read as '0'

bit 16 **HCAPEN:** Position Counter Input Capture by Home Event Enable bit
1 = HOMEx input event (positive edge) triggers a position capture event
0 = HOMEx input event (positive edge) does not trigger a position capture event

bit 15 **QCAPEN:** Position Counter Input Capture Enable bit
1 = Positive edge detect of Home input triggers position capture function
0 = Home input event (positive edge) does not trigger a capture even

bit 14 **FLTREN:** QEA/QEB/INDX/HOMEx Digital Filter Enable bit
1 = Input Pin Digital filter is enabled
0 = Input Pin Digital filter is disabled (bypassed)

bit 13-11 **QFDIV<2:0>:** QEA/QEB/INDX/HOMEx Digital Input Filter Clock Select bits
111 = 1:128 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 10-9 **OUTFNC<1:0>:** QEI Module Output Function Mode Select bits
11 = The CNTCMPx pin goes high when POSxCNT ≤ QEIxCMPL or POSxCNT ≥ QEIxICCH
10 = The CNTCMPx pin goes high when POSxCNT ≤ QEIxCMPL
01 = The CNTCMPx pin goes high when POSxCNT ≥ QEIxICCH
00 = Output is disabled

bit 8 **SWPAB:** Swap QEA and QEB Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped

bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

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REGISTER 30-2: QEIxIOC: QEIx I/O CONTROL REGISTER (CONTINUED)

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin after Polarity Control bit (read-only)
1 = Pin is at logic '1', if HOMPOL bit is set to '0'
Pin is at logic '0', if HOMPOL bit is set to '1'
0 = Pin is at logic '0', if HOMPOL bit is set to '0'
Pin is at logic '1', if HOMPOL bit is set to '1'

bit 2 **INDEX:** Status of INDXx Input Pin after Polarity Control bit (Read-Only)
1 = Pin is at logic '1', if IDXPOL bit is set to '0'
Pin is at logic '0', if IDXPOL bit is set to '1'
0 = Pin is at logic '0', if IDXPOL bit is set to '0'
Pin is at logic '1', if IDXPOL bit is set to '1'

bit 1 **QEB:** Status of QEBx Input Pin after Polarity Control and SWPAB Pin Swapping bit (read-only)
1 = Physical pin QEB is at logic '1', if QEBPOL bit is set to '0' and SWPAB bit is set to '0'
Physical pin QEB is at logic '0', if QEBPOL bit is set to '1' and SWPAB bit is set to '0'
Physical pin QEA is at logic '1', if QEBPOL bit is set to '0' and SWPAB bit is set to '1'
Physical pin QEA is at logic '0', if QEBPOL bit is set to '1' and SWPAB bit is set to '1'

0 = Physical pin QEB is at logic '0', if QEBPOL bit is set to '0' and SWPAB bit is set to '0'
Physical pin QEB is at logic '1', if QEBPOL bit is set to '1' and SWPAB bit is set to '0'
Physical pin QEA is at logic '0', if QEBPOL bit is set to '0' and SWPAB bit is set to '1'
Physical pin QEA is at logic '1', if QEBPOL bit is set to '1' and SWPAB bit is set to '1'

bit 0 **QEA:** Status of QEAx Input Pin after Polarity Control and SWPAB Pin Swapping bit (read-only)
1 = Physical pin QEA is at logic '1', if QEAPOL bit is set to '0' and SWPAB bit is set to '0'
Physical pin QEA is at logic '0', if QEAPOL bit is set to '1' and SWPAB bit is set to '0'
Physical pin QEB is at logic '1', if QEAPOL bit is set to '0' and SWPAB bit is set to '1'
Physical pin QEB is at logic '0', if QEAPOL bit is set to '1' and SWPAB bit is set to '1'

0 = Physical pin QEA is at logic '0', if QEAPOL bit is set to '0' and SWPAB bit is set to '0'
Physical pin QEA is at logic '1', if QEAPOL bit is set to '1' and SWPAB bit is set to '0'
Physical pin QEB is at logic '0', if QEAPOL bit is set to '0' and SWPAB bit is set to '1'
Physical pin QEB is at logic '1', if QEAPOL bit is set to '1' and SWPAB bit is set to '1'

REGISTER 30-3: QEIxSTAT: QEIx STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	RC-0, HS	R/W-0	RC-0, HS	R/W-0	RC-0, HS	R/W-0
	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
7:0	RC-0, HS	R/W-0	RC-0, HS	R/W-0	RC-0, HS	R/W-0	RC-0, HS	R/W-0
	PCIIRQ(1)	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **PCHEQIRQ:** Position Counter Greater Than Compare Status bit
1 = POSxCNT > QEIxICCH
0 = POSxCNT ≤ QEIxICCH

bit 12 **PCHEQIEN:** Position Counter Greater Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **PCLEQIRQ:** Position Counter Less Than Compare Status bit
1 = POSxCNT < QEIxCMPL
0 = POSxCNT ≥ QEIxCMPL

bit 10 **PCLEQIEN:** Position Counter Less Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = Overflow has not occurred

bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit(1)
1 = POSxCNT was reinitialized
0 = POSxCNT was not reinitialized

bit 6 **PCIIEN:** Position Counter (Homing) Initialization Process Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = Overflow has not occurred

bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: This status bit in only applies to PIMOD<2:0> modes '011' and '100'.

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REGISTER 30-3: QEIxSTAT: QEIx STATUS REGISTER (CONTINUED)

bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = Home event has not occurred

bit 2 **HOMIEN:** Home Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **IDXIRQ:** Status Flag for Index Event Status bit
1 = Index event has occurred
0 = Index event has not occurred

bit 0 **IDXIEN:** Index Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

Note 1: This status bit in only applies to PIMOD<2:0> modes '011' and '100'.

REGISTER 30-4: POSxCNT: POSITION COUNTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POSCNT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POSCNT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POSCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	POSCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **POSCNT<31:0>:** 32-bit Position Counter Register bits

The Operating mode of the position counter is controlled by the CCM bit in the QEIxCON register.

Quadrature Count mode: The QEA and QEB inputs are decoded to generate count pulses and direction information for controlling the position counter operation.

External Count with External Up/Down mode: The QEA/EXTCNT input is treated as an external count signal, and the QEB/DIR/GATE input provides the count direction information.

External Count with External Gate mode: The QEA/EXTCNT input is treated as an external count signal. If the GATEN bit in the QEIxCON register is equal to '1', the QEB/DIR/GATE input will gate the counter signal.

Internal Timer mode: The position counter uses PBCLK2 divided by the clock divider INTDIV as the count source.

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REGISTER 30-5: VELxCNT: VELOCITY COUNTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **VELCNT<31:0>:** 32-bit Velocity Counter bits

The velocity counter is automatically cleared after every processor read of the velocity counter. It is not reset by the index input or otherwise affected by any of the PIMOD<2:0> specified modes. The contents of the counter represents the distance traveled during the time between samples. Velocity equals the distance traveled per unit of time. The velocity counter can save the application software the trouble of performing 32-bit math operations between current and previous position counter values to calculate velocity. If the velocity counter rolls over from 0x7FFFFFFF to 0x80000000, or from 0x80000000 to 0x7FFFFFFF, an overflow/underflow condition is detected. If the VELOVIEN bit is set in the QEISTAT register, an interrupt will be generated.

REGISTER 30-6: VELxHLD: VELOCITY HOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELHLD<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELHLD<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELHLD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	VELHLD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **VELHLD<31:0>:** 32-bit Velocity Hold bits
When VELxCNT is read, the contents are captured at the same time into the VELxHLD register.

REGISTER 30-7: INTxHLD: INTERVAL TIMER HOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTHLD<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTHLD<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTHLD<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTHLD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **INTHLD<31:0>:** 32-bit Index Counter Hold bits
When the next count pulse is detected, the current contents of the interval timer (INTxTMR) are transferred to the Interval Hold register (INTxHLD) and the interval timer is cleared and the process repeats.

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REGISTER 30-8: INDxCNT: INDEX COUNTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INDxCNT<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INDxCNT<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INDxCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INDxCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IDXCNT<31:0>:** 32-bit Position Counter bits

REGISTER 30-9: INTxTMR: INTERVAL TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INTTMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **INTTMR<31:0>:** 32-bit Interval Timer Counter bits

The INTxTMR register provides a means to measure the time between each decoded quadrature count pulse to yield improved velocity information. The interval timer should be set to run at a frequency chosen such that the counter does not overflow at the expected minimum operating speed of the motor. The interval timer is automatically cleared when a count pulse is detected. The timer then counts at the specified rate based on the setting of the INTDIV bit in the QEIxCON register.

REGISTER 30-10: QEIxICC: QEIx INITIALIZE/CAPTURE/COMPARE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICCH<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ICCH<31:0>:** 32-bit Initialize/Capture/Compare High bits

REGISTER 30-11: QEIxCMPL: CAPTURE LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CMPL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CMPL<31:0>:** 32-bit Compare Low Value bits

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31.0 MOTOR CONTROL PWM MODULE

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 44. "Motor Control PWM (MCPWM)"** (DS60001393), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MK GP/MC Family of devices support a dedicated Motor Control Pulse-Width Modulation (PWM) module with up to 12 outputs.

The Motor Control PWM module consists of the following major features:

- Two master time base modules with special event triggers
- PWM module input clock prescaler
- Two synchronization inputs
- Two synchronization outputs
- Eight PWM generators with complimentary output pairs
- Four additional PWM generators with single ended outputs
- Period, duty cycle, phase shift and dead time minimum resolution of 1 / FSYSCLK in Edge-Aligned mode and 2 / FSYSCLK minimum resolution in Center-Aligned mode
- Cycle by cycle fault recovery and latched fault modes
- PWM time-base capture upon current limit
- Nine fault input pins are available for faults and current limits
- Programmable analog-to-digital trigger with interrupt for each PWM pair
- Complementary PWM outputs
- Push-Pull PWM outputs
- Redundant PWM outputs
- Edge-Aligned PWM mode
- Center-Aligned PWM mode
- Variable Phase PWM mode
- Multi-Phase PWM mode
- Fixed-Off Time PWM mode
- Current Limit PWM mode
- Current Reset PWM mode
- PWMxH and PWMxL output override control
- PWMxH and PWMxL output pin swapping
- Chopping mode (also known as Gated mode)
- Dead time insertion
- Dead time compensation
- Enhanced Leading-Edge Blanking (LEB)
- 15 mA PWM pin output drive

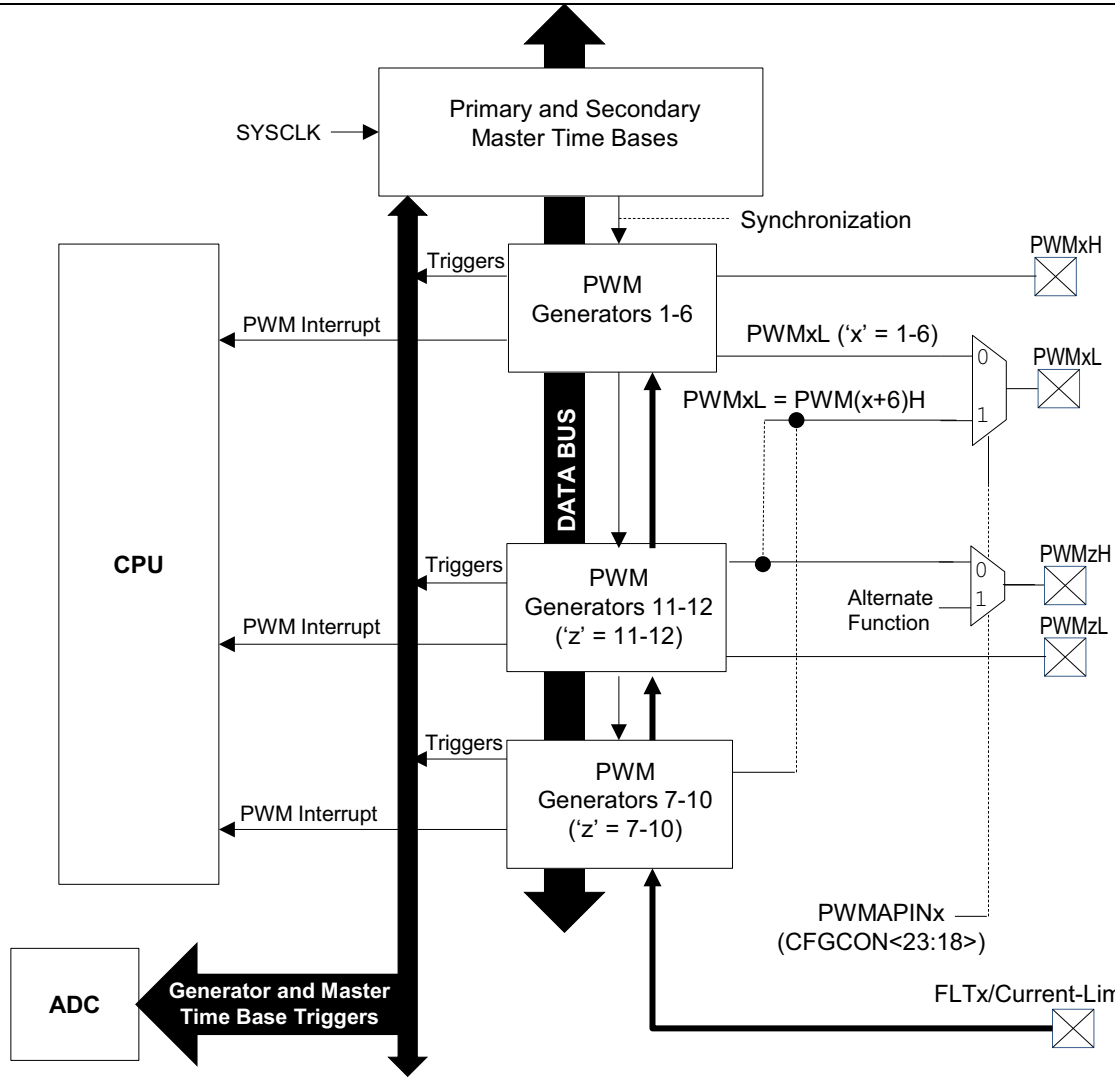
The Motor Control PWM module contains up to twelve PWM generators. Two master time base generators provide a synchronous signal as a common time base to synchronize the various PWM outputs. Each generator can operate independently or in synchronization with either of the two master time bases. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWM can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the Motor Control PWM module also generates two Special Event Triggers to the ADC module based on the two master time bases.

PWM generators 1 through 6, 11 and 12 have two outputs, PWMxH and PWMxL, brought out to the dedicated pins. The PWM generators 7 through 10 have only the PWMxH outputs on pins, but can alternately be mapped onto PWMxL, where 'x' = 1-4, based on the PWMAPINx bit in the CFGCON register. Generators 11 and 12 have their PWMxH additionally brought out on the PWMxL pins of the generators 5 and 6, based on the PWMAPINx bit in the CFGCON register. The configuration bits PWMAPINx (CFGCON<23:18>) contain bits that help arbitrate which PWM output takes control of the I/O pin. This is in addition to PENx control bits which decide the if the MCPWM module of the I/O module assumes ownership of the output pin.

Figure 31-1 illustrates an architectural overview of the Motor Control PWM module and its interconnection with the CPU and other peripherals.

FIGURE 31-1: MOTOR CONTROL PWM MODULE ARCHITECTURAL OVERVIEW



PWM	PIN	Function (DTC Enb)
PWM1/7	FLT3	DTCMP1
PWM2/8	FLT4	DTCMP2
PWM3/9	FLT5	DTCMP3
PWM4/10	FLT6	DTCMP4
PWM5/11	FLT7	DTCMP5
PWM6/12	FLT8	DTCMP6

NOTE: Because DTCOMPx, (that is, dead time compensation) , FLTx and Current Limit share the same digital input pins, their availability is mutually exclusive with fault function as the highest priority.

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31.1 PWM Faults

The PWM module incorporates multiple external Fault inputs to include FLT1 and FLT2, which are remappable using the PPS feature, and FLT15, which has been implemented with Class B safety features, and is available on a fixed pin at reset for Fault detection.

Fault pins are selectable for active level (active high or low). FLT pins provide a safe and reliable way to shut down the PWM outputs, tri-state, when the Fault input is asserted. Therefore, the user should provide the necessary external pull-up or pull-down to disable the high or low side FETs in motor control applications.

31.1.1 PWM FAULTS AT RESET

During any reset event, the PWM module maintains ownership of the Class B fault FLT15. At reset, this fault is enabled in latched mode to guarantee the fail-safe power-up of the application. The application software must clear the PWM fault before enabling the High-Speed Motor Control PWM module. To clear the fault condition, the FLT15 pin must first be pulled low externally or the internal pull down resistor in the CNPDx register can be enabled.

Note:	The Fault mode may be changed using the FLTMOD<1:0> bits (IOCONx<17:16>) regardless of the state of FLT15.

31.1.2 WRITE-PROTECTED REGISTERS

Write protection is implemented for the IOCONx register. The write protection feature prevents any inadvertent writes. This protection feature can be controlled by the PWMLOCK Configuration bit (DEVCFG3<20>). The default state of the write protection feature is disabled (PWMLOCK = 1). The write protection feature can be enabled by configuring the PWMLOCK = 0.

To gain write access, the application software must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. Every write to the IOCONx register requires a prior unlock operation.

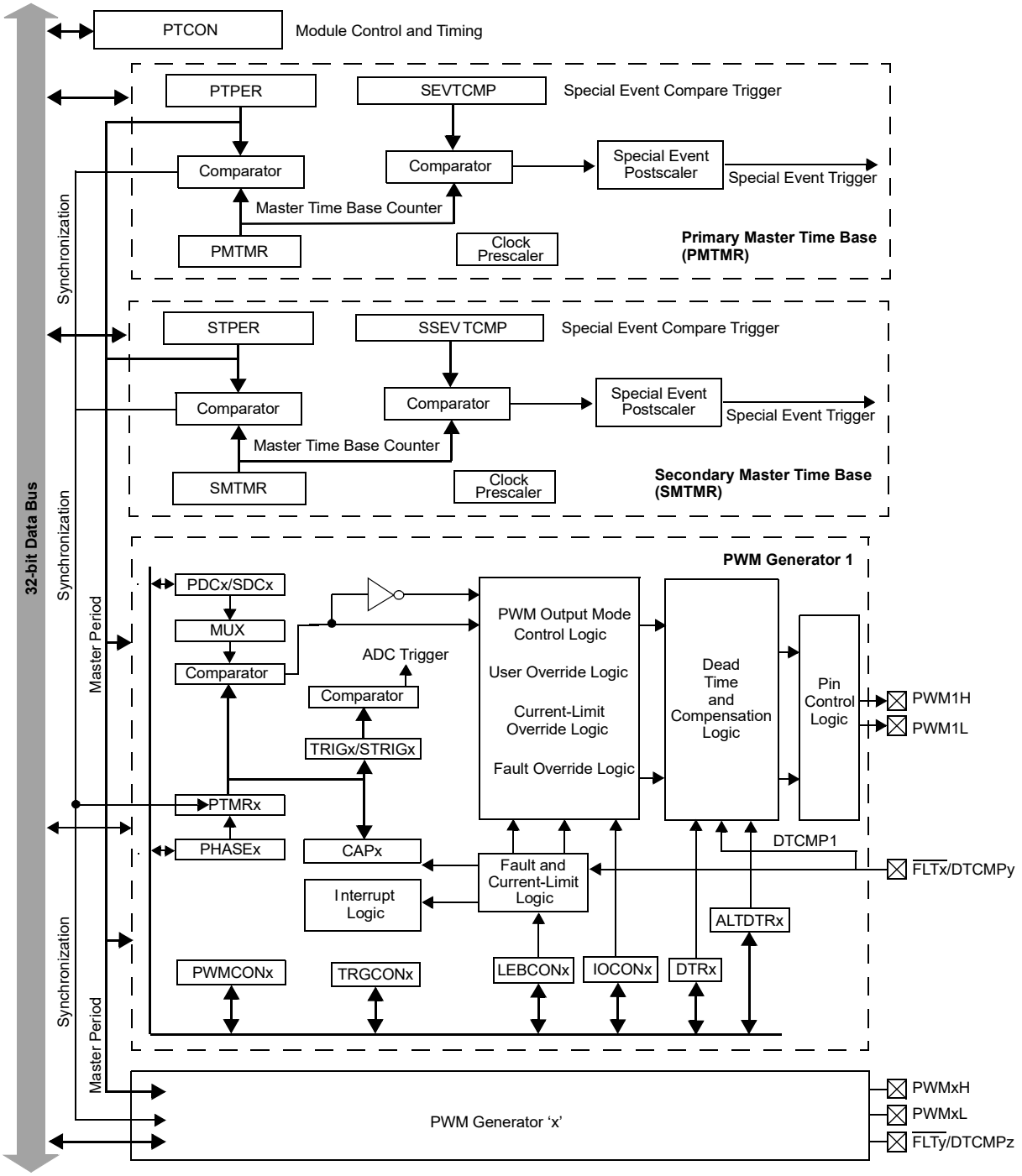
The unlocking sequence is described in Example 31-1.

Figure 31-2 shows the register interconnection diagram for the Motor Control PWM module.

EXAMPLE 31-1: PWM WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
Untested Code – For Information Purposes Only
; In the default Reset state, the FLT15 pin must be pulled low externally to clear and disable
; the fault.
; Writing to IOCONx register requires unlock sequence
di      v1
ehb                         ;Disable interrupts
mov     #0xXXXX,r3          ;Move desired IOCON4 register data to r3 register
mov     #0xabcd,r1          ;Load first unlock key to r1 register
mov     #0x4321,r2          ;Load second unlock key to r2 register
mov     r1, PWMKEY          ;Write first unlock key to PWMKEY register
mov     r2, PWMKEY          ;Write second unlock key to PWMKEY register
mov     r3,IOCON4           ;Write desired value to IOCON SFR for channel 4
mfc0    v0,c0_status
ori     v0,v0,0x1
mtc0    v0,c0_status
ehb                         ;Re-enable Interrupts
```

FIGURE 31-2: MOTOR CONTROL PWM MODULE REGISTER INTERCONNECTION DIAGRAM



Legend:

'x' = 1 through 12.
'y' = 1 through 8 and 15.
'z' = 3 through 8.

Note: Since DTCMPx and $\overline{\text{FLTx}}$ share the same digital input pins, their availability is mutually exclusive.

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31.2 Motor Control PWM Control Registers

TABLE 31-1: MCPWM REGISTER MAP

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	PTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN	—	PTSIDL	SESTAT	SEIEN	PWMRDY	—	—	—	PCLKDIV<2:0>			SEVTPS<3:0>				0000
A010	PTPER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTPER<15:0>																0020
A020	SEVTCMP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SEVTCMP<15:0>																0000
A030	PMTMR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PMTMR<15:0>																0000
A040	STCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	SSESTAT	SSEIEN	—	—	—	—	SCLKDIV<2:0>			SEVTPS<3:0>				0000
A050	STPER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STPER<15:0>																0020
A060	SSEVTCMP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SSEVTCMP<15:0>																0000
A070	SMTMR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SMTMR<15:0>																0000
A080	CHOP	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPCLKEN	—	—	—	—	—	CHOPCLK<9:0>										0000
A090	PWMKEY	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PWMKEY<15:0>																0000
A0C0	PWMCON1	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A0D0	IOCON1	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A0E0	PDC1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A0F0	SDC1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A100	PHASE1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A110	DTR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DTR<13:0>																0000

Legend: '—' = unimplemented; read as '0'.

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TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A120	ALTDTR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALTDTR<13:0>																0000
A130	DTCOMP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A140	TRIG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A150	TRGCON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A160	STRIG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A170	CAP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A180	LEBCON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A190	LEBDLY1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A1A0	AUXCON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A1B0	PTMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A1C0	PWMCON2	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A1D0	IOCON2	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A1E0	PDC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A1F0	SDC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A200	PHASE2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A210	DTR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
A220	ALTDTR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000

Legend: '—' = unimplemented; read as '0'.

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TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A230	DTCOMP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A240	TRIG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A250	TRGCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A260	STRIG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A270	CAP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A280	LEBCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A290	LEBDLY2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A2A0	AUXCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A2B0	PTMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A2C0	PWMCON3	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A2D0	IOCON3	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A2E0	PDC3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A2F0	SDC3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A300	PHASE3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A310	DTR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
A320	ALTDTR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
A330	DTCOMP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000

Legend: '—' = unimplemented; read as '0'.

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TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A340	TRIG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A350	TRGCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A360	STRIG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A370	CAP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A380	LEBCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A390	LEBDLY3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A3A0	AUXCON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A3B0	PTMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A3C0	PWMCON4	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A3D0	IOCON4	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A3E0	PDC4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A3F0	SDC4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A400	PHASE4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A410	DTR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
A420	ALTDTR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
A430	DTCOMP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A440	TRIG4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000

Legend: '—' = unimplemented; read as '0'.

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TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

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			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A450	TRGCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A460	STRIG4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A470	CAP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A480	LEBCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A490	LEBDLY4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A4A0	AUXCON4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A4B0	PTMR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A4C0	PWMCON5	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A4D0	IOCON5	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A4E0	PDC5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A4F0	SDC5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A500	PHASE5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A510	DTR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
A520	ALTDTR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
A530	DTCOMP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A540	TRIG5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A550	TRGCON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000

Legend: '—' = unimplemented; read as '0'.

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A560	STRIG5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A570	CAP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A580	LEBCON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A590	LEBDLY5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A5A0	AUXCON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A5B0	PTMR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A5C0	PWMCON6	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A5D0	IOCON6	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A5E0	PDC6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A5F0	SDC6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A600	PHASE6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A610	DTR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
A620	ALTDTR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
A630	DTCOMP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A640	TRIG6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A650	TRGCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A660	STRIG6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000

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A670	CAP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A680	LEBCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A690	LEBDLY6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A6A0	AUXCON6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A6B0	PTMR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A6C0	PWMCON7	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A6D0	IOCON7	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A6E0	PDC7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A6F0	SDC7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A700	PHASE7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A710	DTR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
A720	ALTDTR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
A730	DTCOMP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A740	TRIG7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A750	TRGCON7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A760	STRIG7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A770	CAP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000

Legend: '—' = unimplemented; read as '0'.

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TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A780	LEBCON7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A790	LEBDLY7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A7A0	AUXCON7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A7B0	PTMR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A7C0	PWMCON8	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A7D0	IOCON8	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A7E0	PDC8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A7F0	SDC8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A800	PHASE8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A810	DTR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
A820	ALTDTR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
A830	DTCOMP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A840	TRIG8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A850	TRGCON8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A860	STRIG8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A870	CAP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A880	LEBCON8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000

Legend: '—' = unimplemented; read as '0'.

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TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A890	LEBDLY8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
A8A0	AUXCON8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A8B0	PTMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A8C0	PWMCON9	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A8D0	IOCON9	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A8E0	PDC9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A8F0	SDC9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
A900	PHASE9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
A910	DTR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
A920	ALTDTR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
A930	DTCOMP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
A940	TRIG9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
A950	TRGCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
A960	STRIG9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
A970	CAP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
A980	LEBCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
A990	LEBDLY9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000

Legend: '—' = unimplemented; read as '0'.

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TABLE 31-1: MCPWM REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A9A0	AUXCON9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
A9B0	PTMR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
A9C0	PWMCON10	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
A9D0	IOCON10	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
A9E0	PDC10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
A9F0	SDC10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
AA00	PHASE10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
AA10	DTR10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
AA20	ALTDTR10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
AA30	DTCOMP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
AA40	TRIG10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
AA50	TRGCON10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
AA60	STRIG10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
AA70	CAP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
AA80	LEBCON10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
AA90	LEBDLY10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
AAA0	AUXCON10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000

Legend: '—' = unimplemented; read as '0'.

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AAB0	PTMR10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000
AAC0	PWMCON11	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
AAD0	IOCON11	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
AAE0	PDC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
AAF0	SDC11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
AB00	PHASE11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
AB10	DTR11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
AB20	ALTDTR11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
AB30	DTCOMP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
AB40	TRIG11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
AB50	TRGCON11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
AB60	STRIG11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
AB70	CAP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
AB80	LEBCON11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
AB90	LEBDLY11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
ABA0	AUXCON11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
ABB0	PTMR11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000

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ABC0	PWMCON12	31:16	FLTIF	CLIF	TRGIF	PWMLIF	PWMHIF	—	—	—	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—	0000
		15:0	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>		ITB	—	DTC<1:0>		DTCP	PTDIR	MTBS	—	XPRES	—	0000
ABD0	IOCON12	31:16	—	—	CLSRC<3:0>				CLPOL	CLMOD	—	FLTSRC<3:0>				FLTPOL	FLTMOD<1:0>		0078
		15:0	PENH	PENL	POLH	POLL	PMOD<1:0>		OVRENH	OVRENL	OVRDAT<1:0>		FLTDAT<1:0>		CLDAT<1:0>		SWAP	OSYNC	0000
ABE0	PDC12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PDC<15:0>																0000
ABF0	SDC12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SDC<15:0>																0000
AC00	PHASE12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHASE<15:0>																0000
AC10	DTR12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	DTR<13:0>														0000
AC20	ALTDTR12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ALTDTR<13:0>														0000
AC30	DTCOMP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	COMP<13:0>														0000
AC40	TRIG12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGCMP<15:0>																0000
AC50	TRGCON12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRGDIV<3:0>				TRGSEL<1:0>		STRGSEL<1:0>		DTM	STRGIS	—	—	—	—	—	—	0000
AC60	STRIG12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STRGCMP<15:0>																0000
AC70	CAP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CAP<15:0>																0000
AC80	LEBCON12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	—	—	—	—	—	—	0000
AC90	LEBDLY12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	LEB<11:0>												0000
ACA0	AUXCON12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	CHOPSEL<3:0>				CHOPHEN	CHOPLEN	0000
ACB0	PTMR12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR<15:0>																0000

Legend: '—' = unimplemented; read as '0'.

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REGISTER 31-1: PTCON: PWM PRIMARY TIME BASE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	HS/HC-0	U-0	U-0
	PTEN	—	PTSIDL	SESTAT(1)	SEIEN(3)	PWMRDY	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PCLKDIV<2:0>(2)			SEVTPS<3:0>(2)			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **PTEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

Note: Many of the PWM registers and/or bits as designated, do not allow updates once a PWM module is enabled. Therefore, it is recommended that the user application initialize all required PWM registers before setting the PTEN bit equal to '1'.

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit
1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit(1)
1 = Special Event Interrupt is pending
0 = Special Event Interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special Event Interrupt is enabled
0 = Special Event Interrupt is disabled

bit 10 **PWMRDY:** PWM Module Status bit
1 = PWM module is ready and operation has begun
0 = PWM module is not ready

bit 9-7 **Unimplemented:** Read as '0'

Note 1: The SESTAT bit is cleared by clearing the SEIEN bit and the corresponding bit in the IFSx register.

2: The SEVTPS<3:0> and PCLKDIV<2:0> bits should be changed only when the PTEN bit (PTCON<15>) = 0.

3: To clear the Primary Special Event Interrupt the user application must do the following:
1) Clear the SEIEN bit by setting it to '0'.
2) Clear the Primary Special Event Interrupt flag by setting IFS5<11> = 0.
3) Re-enabling the PTCON register by setting the SEIEN equal to '1' if desired.
The user application will not be able to clear the Primary Special Event Interrupt flag as long as the SEIEN bit is equal to '1'.

REGISTER 31-1: PTCON: PWM PRIMARY TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4 **PCLKDIV<2:0>:** Primary PWM Input Clock Prescaler bits(2)
111 = Divide by 128, PWM resolution = 128/FSYSCLK
110 = Divide by 64, PWM resolution = 64/FSYSCLK
•
•
•
000 = Divide by 1, PWM resolution = 1/FSYSCLK (power-on default)

bit 3-0 **SEVTPS<3:0>:** PWM Special Event Trigger Output Postscaler Select bits(2)
1111 = 1:16 postscaler generates Special Event trigger at every 16th compare match event
•
•
•
0001 = 1:2 postscaler generates Special Event trigger at every second compare match event
0000 = 1:1 postscaler generates Special Event trigger at every compare match event

Note 1: The SESTAT bit is cleared by clearing the SEIEN bit and the corresponding bit in the IFSx register.

2: The SEVTPS<3:0> and PCLKDIV<2:0> bits should be changed only when the PTEN bit (PTCON<15>) = 0.

3: To clear the Primary Special Event Interrupt the user application must do the following:
1) Clear the SEIEN bit by setting it to '0'.
2) Clear the Primary Special Event Interrupt flag by setting IFS5<11> = 0.
3) Re-enabling the PTCON register by setting the SEIEN equal to '1' if desired.
The user application will not be able to clear the Primary Special Event Interrupt flag as long as the SEIEN bit is equal to '1'.

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REGISTER 31-2: PTPER: PRIMARY MASTER TIME BASE PERIOD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PTPER<15:8>(1,2)							
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0(3)	R/W-0(3)	R/W-0(3)
	PTPER<7:0>(1,2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PTPER<15:0>:** Primary Master Time Base Period Value bits(1,2,4)

Note 1: Minimum LSb = 1 / FSYSCLK.

2: Minimum value is 0x0008.

3: If a period value is lesser than 0x0008 is chosen, the internal hardware forcefully sets the period to a minimum value of 0x0008.

4: PTPER = (FSYSCLK / (FPWM * PCLKDIV<2:0> bits (PTCON<6:4>)).
FPWM = User-desired PWM Frequency.

REGISTER 31-3: SEVTCMP: PWM PRIMARY SPECIAL EVENT COMPARE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEVTCMP<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEVTCMP<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **SEVTCMP<15:0>:** Special Event Compare Count Value bits(1)

The special event trigger allows analog-to-digital conversions to be synchronized to the master PWM time base. The analog-to-digital sampling and conversion time may be programmed to occur at any point within the PWM period.

Note 1: Minimum LSb = 1 / FSYSCLK.

REGISTER 31-4: PMTMR: PRIMARY MASTER TIME BASE TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PMTMR<15:8>(1)							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PMTMR<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PMTMR<15:0>:** Primary Master Time Base Timer Value bits(1)

This timer increments with each PWM clock until the PTPER value is reached.

Note 1: LSb = 1 / FSYSCLK.

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REGISTER 31-5: STCON: SECONDARY MASTER TIME BASE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	HS/HC-0	R/W-0	U-0	U-0	U-0
	—	—	—	SSESTAT(1)	SSEIEN(3)	—	—	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	SCLKDIV<2:0>(2)			SEVTPS<3:0>(2)			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12 **SSESTAT:** Secondary Special Event Interrupt Status bit(1)
- 1 = Secondary Special Event Interrupt is pending
- 0 = Secondary Special Event Interrupt is not pending

bit 11 **SSEIEN:** Secondary Special Event Interrupt Enable bit(3)
- 1 = Secondary Special Event Interrupt is enabled
- 0 = Secondary Special Event Interrupt is disabled

bit 10-7 **Unimplemented:** Read as '0'

bit 6-4 **SCLKDIV<2:0>:** Secondary PWM Input Clock Prescaler(2)
- 111 = Divide by 128, PWM resolution = (128/FSYSCLK)
- 110 = Divide by 64, PWM resolution = (64/FSYSCLK)
- •
- •
- •
- 000 = Divide by 1, PWM resolution = 1/FSYSCLK (power-on default)

bit 3-0 **SEVTPS<3:0>:** PWM Secondary Special Event Trigger Output Postscaler Select bits(2)
- 1111 = 1:16 Postscale
- •
- •
- •
- 0001 = 1:2 Postscale
- 0000 = 1:1 Postscale

Note 1: The SSESTAT bit is cleared by clearing the SSEIEN bit and corresponding bit in the IFSx register.

2: These bits should be changed only when the PTEN bit (PTCON<15>) = 0.

3: To clear the Secondary Special Event Interrupt, the user application must do the following:
1) First, clear the SSEIEN bit by setting it to '0'.
2) Next, clear the Secondary Special Event Interrupt flag, IFS5<12>, by setting it to '0'.
3) Finally, re-enable the STCON register by setting the SSEIEN bit equal to '1', if desired.
The user application will not be able to clear the Secondary Special Event Interrupt flag as long as the SSEIEN bit is equal to '1'.

REGISTER 31-6: STPER: SECONDARY MASTER TIME BASE PERIOD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STPER<15:8>(1,2,4)							
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0(3)	R/W-0(3)	R/W-0(3)
	STPER<7:0>(1,2,4)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **STPER<15:0>:** Secondary Master Time Base Period Value bits(1,2,4)

Note 1: Minimum LSb = 1/FSYSCLK.

2: Minimum value is 0x0008.

3: If a period value lesser than 0x0008 is chosen, the internal hardware forcefully sets the period to a minimum value of 0x0008.

4: STPER = (FSYSCLK/(FPWM * PCLKDIV<2:0> bits (PTCON<6:4>)).
FPWM = User-desired PWM Frequency.

REGISTER 31-7: SSEVTCMP: PWM SECONDARY SPECIAL EVENT COMPARE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEVTCMP<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEVTCMP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **SSEVTCMP<15:0>:** Secondary Special Event Compare Value bits

The secondary special event trigger allows analog-to-digital conversions to be synchronized to the secondary master PWM time base. The analog-to-digital sampling and conversion time may be programmed to occur at any point within the PWM period.

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REGISTER 31-8: SMTMR: SECONDARY MASTER TIME BASE TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SMTMR<15:8>(1)							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SMTMR<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **SMTMR<15:0>:** Secondary Master Time Base Timer Value bits(1)
This timer increments with each PWM FSYSCLK until the STPER value is reached.

Note 1: Min LSb = 1/FSYSCLK.

REGISTER 31-9: CHOP: PWM CHOP CLOCK GENERATOR REGISTER

Bit Range	Bit 31/2 /15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	CHPCLKEN	—	—	—	—	—	CHOPCLK<9:8>(2,3)	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHOPCLK<7:0>(2,3)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CHPCLKEN:** Enable Chop Clock Generator bit
1 = Chop clock generator is enabled(1)
0 = Chop clock generator is disabled

bit 14-10 **Unimplemented:** Read as '0'

bit 9-0 **CHOPCLK<9:0>:** Chop Clock Divider bits(2,3)
Chop Frequency = (FSYSCLK/PCLKDIV) / (CHOPCLK<9:0>)

Note 1: The chop clock generator operates with the PCLKDIV<2:0> bits (PTCON<6:4>).
2: Minimum values is 0x0002. A value of 0x0000 or 0x0001 will produce no chop clock.
3: These bits should only be changed when the PTEN bit (PTCON<15>) is clear.

Note: The Chop Clock is a continuous high frequency signal (relative to PWM cycles) that is optionally gated with the PWM output signals to allow the PWM signals to pass through an external isolation barrier such as a pulse transformer or capacitor. The value of [CHOP<9:0> * PWM clock duration] defines the high, and the low times of the Chop Clock. A value of '8' in the CHOP register yields a Chop Clock signal with a period of 16 PWM clock cycles as defined by the primary PWM clock prescaler PCLKDIV<2:0.> A Value of 0x0000 or 0x0001 will produce no Chop Clock

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REGISTER 31-10: PWMKEY: PWM UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	PWMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	PWMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PWMKEY<15:0>:** PWM Unlock bits

If the PWMLOCK Configuration bit is asserted (PWMLOCK = 0), the IOCONx registers are writable only after the proper sequence is written to the PWMKEY register. If the PWMLOCK Configuration bit is deasserted (PWMLOCK = 1), the IOCONx registers are writable at all times. For more information on the unlock sequence, refer to the **44.9 "Write Protection"** in **Section 44. Motor Control PWM (MCPWM)** (DS60001393) of the *"PIC32 Family Reference Manual*" for more information.

This register is implemented only in devices where the PWMLOCK Configuration bit is present in the DEVCFG3 Configuration register.

Note: The user must write two consecutive values of 0xABCD and 0x4321 to the PWMKEY register to perform an unlock operation if PWMLOCK = 0. Write access to any subsequent secure register must be the very next access following the unlock process. This is not an atomic operation and any CPU interrupts that occur during or immediately after an unlock sequence may cause writes to any PWM secure register to fail.

REGISTER 31-11: PWMCONx: PWM CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FLTIF(1)	CLIF(1)	TRGIF(1)	PWMLIF(1)	PWM-HIF(1)	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FLTIEN	CLIEN	TRGIEN	PWMLIEN	PWMHIEN	—	—	—
15:8	HS/HC-0	HS/HC-0	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0
	FLTSTAT	CLTSTAT	—	—	ECAM<1:0>(1)		ITB(2)	—
7:0	R/W-0	R/W-0	R/W-0	HS/HC/R-0	R/W-0	U-0	R/W-0	U-0
	DTC<1:0>		DTCP(4)	PTDIR(6)	MTBS(7)	—	XPRES(3)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTIF:** Fault Interrupt Flag bit(1)
1 = Fault interrupt has occurred
0 = Fault interrupt has not occurred

bit 30 **CLIF:** Current-Limit Status bit(1)
1 = Current limit has occurred
0 = Current limit has not occurred

bit 29 **TRGIF:** Trigger Interrupt Status bit(1)
1 = Trigger interrupt is pending
0 = Trigger interrupt is not pending

bit 28 **PWMLIF:** PWML Interrupt Status bit(1)
1 = PWM Timer equal to 0x0 interrupt has occurred
0 = PWM Interrupt has not occurred

bit 27 **PWMHIF:** PWMH Interrupt Status bit
1 = PWM period match interrupt has occurred
0 = PWM period match interrupt has not occurred

bit 26-24 **Unimplemented:** Read as '0'

bit 23 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled. If FLTIF = 1, an interrupt event will be generated.
0 = Fault interrupt is disabled

bit 22 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled. If CLIF = 1, an interrupt event will be generated.
0 = Current-limit interrupt is disabled

Note 1: If PWM interrupts are enabled, software must clear the PWMCONx interrupt flags here first, followed second by the corresponding IFSx bit in the Interrupt controller. The corresponding PWM IFSx interrupt flag cannot be cleared if any of these local PWMCON interrupt bits are not cleared first. Failure to do so will result in an infinite interrupt loop.

2: This bit should not be changed after the PWM is enabled (PTEN bit (PTCON<15>) = 1).

3: To operate in External Period Reset mode, the ITB bit must be set to '1' and the CLMOD bit in the IOCONx register must be set to '0'.

4: For Dead Time Compensation (DTCP) to be effective, DTC<1:0> must be set to '11'; otherwise, DTCP is ignored.

5: Negative dead time is only implemented for Edge-Aligned mode.

6: XPRES mode should only be used in Edge-Aligned mode with or without complimentary outputs. It does not support dead time compensation (i.e., duty cycle adjustment), which is selected when DTC<1:0> = 11.

7: The clock source is one of the master time bases even if ITB = 1 is selected.

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REGISTER 31-11: PWMCONx: PWM CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 21 **TRIGIEN:** Primary Trigger Interrupt Enable bit
1 = A primary trigger event generates an interrupt request
0 = A primary trigger event interrupts request is disabled

bit 20 **PWMLIEN:** PWM Low Phase Interrupt Enable bit
1 = When the PWM Timer is equal to 0x4, the PWMLIF flag = 1 and generates an interrupt request
0 = PWM Period event interrupt request is disabled

bit 19 **PWMHIEN:** PWM High Phase Interrupt Enable bit
1 = When the PWM Period matches the value in the PWM timer, an interrupt request is generated
0 = PWM Period event interrupt request is disabled, and the PWMHIF bit is cleared

bit 18-16 **Unimplemented:** Read as '0'

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = No fault interrupt is pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLTSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = No current-limit interrupt is pending
This bit is cleared by setting CLIEN = 0.

bit 13-12 **Unimplemented:** Read as '0'

bit 11-10 **ECAM<1:0>:** Edge/Center-Aligned Mode Enable bits(1)
11 = Asymmetric Center-Aligned mode with simultaneous update (PWM(min) Duty Cycle Resolution = (1/FSYSCLK))
10 = Asymmetric Center-Aligned mode double update (PWM(min) Duty Cycle Resolution = (1/FSYSCLK))
01 = Symmetric Center-Aligned mode (PWM(min) Duty Cycle Resolution = (2/FSYSCLK))
00 = Edge-Aligned mode (PWM(min) Duty Cycle Resolution = (1/FSYSCLK))

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx registers provide time base period for this PWM generator
0 = PTPER/STPER register provides timing for this PWM generator based on the MTBS bit

bit 8 **Unimplemented:** Read as '0'

bit 7-6 **DTC<1:0>:** Dead Time Control bits
11 = Dead Time Compensation mode enabled
10 = Dead time function is disabled
01 = Negative dead time actively applied for Complementary Output mode(5)
00 = Positive dead time actively applied for all output modes

Note 1: If PWM interrupts are enabled, software must clear the PWMCONx interrupt flags here first, followed second by the corresponding IFSx bit in the Interrupt controller. The corresponding PWM IFSx interrupt flag cannot be cleared if any of these local PWMCON interrupt bits are not cleared first. Failure to do so will result in an infinite interrupt loop.

2: This bit should not be changed after the PWM is enabled (PTEN bit (PTCON<15>) = 1).

3: To operate in External Period Reset mode, the ITB bit must be set to '1' and the CLMOD bit in the IOCONx register must be set to '0'.

4: For Dead Time Compensation (DTCP) to be effective, DTC<1:0> must be set to '11'; otherwise, DTCP is ignored.

5: Negative dead time is only implemented for Edge-Aligned mode.

6: XPRES mode should only be used in Edge-Aligned mode with or without complimentary outputs. It does not support dead time compensation (i.e., duty cycle adjustment), which is selected when DTC<1:0> = 11.

7: The clock source is one of the master time bases even if ITB = 1 is selected.

REGISTER 31-11: PWMCONx: PWM CONTROL REGISTER 'x' ('x' = 1 THROUGH 12) (CONTINUED)

bit 5 **DTCP:** Dead Time Compensation Polarity bit(5)
- 1 = If the DTCMPx pin = 0, PWMxL is shortened, and PWMxH is lengthened
  If the DTCMPx pin = 1, PWMxH is shortened, and PWMxL is lengthened
- 0 = If the DTCMPx pin = 0, PWMxH is shortened, and PWMxL is lengthened
  If the DTCMPx pin = 1, PWMxL is shortened, and PWMxH is lengthened

bit 4 **PTDIR:** PWM Timer Direction bit(6)
- 1 = PWM timer is decrementing
- 0 = PWM timer is incrementing

bit 3 **MTBS:** Master Time Base Select bit(7)
- 1 = Secondary master time base is the clock source for the MCPWM module
- 0 = Primary master time base is the clock source for the MCPWM module

bit 2 **Unimplemented:** Read as '0'

bit 1 **XPRES:** External PWM Reset Control bit(3)
- 1 = Current-limit source resets primary local time base for this PWM generator if it is in Independent Time Base mode and the PWM module enters the deassertion portion of the duty cycle
- 0 = External pins do not affect PWM time base

Note: If the Current-Limit Reset signal is asserted during the active assertion time of the duty cycle, the time base will not Reset until two PWM clock cycles after the duty cycle transition from assertion to deassertion phase of the duty cycle.

bit 0 **Unimplemented:** Read as '0'

Note 1: If PWM interrupts are enabled, software must clear the PWMCONx interrupt flags here first, followed second by the corresponding IFSx bit in the Interrupt controller. The corresponding PWM IFSx interrupt flag cannot be cleared if any of these local PWMCON interrupt bits are not cleared first. Failure to do so will result in an infinite interrupt loop.

2: This bit should not be changed after the PWM is enabled (PTEN bit (PTCON<15>) = 1).

3: To operate in External Period Reset mode, the ITB bit must be set to '1' and the CLMOD bit in the IOCONx register must be set to '0'.

4: For Dead Time Compensation (DTCP) to be effective, DTC<1:0> must be set to '11'; otherwise, DTCP is ignored.

5: Negative dead time is only implemented for Edge-Aligned mode.

6: XPRES mode should only be used in Edge-Aligned mode with or without complimentary outputs. It does not support dead time compensation (i.e., duty cycle adjustment), which is selected when DTC<1:0> = 11.

7: The clock source is one of the master time bases even if ITB = 1 is selected.

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REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLSRC<3:0>(2,4)				CLPOL(2,4)	CLMOD(2,4)
23:16	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
	—	FLTSRC<3:0>(2,4)				FLTPOL(2)	FLTMOD<1:0>(4)	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PENH(1)	PENL(1)	POLH(2)	POLL(2)	PMOD<1:0>(2)		OVRENH	OVRENL
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	OVRDAT<1:0>(3)		FLTDAT<1:0>(2,3)		CLDAT<1:0>		SWAP	OSYNC

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

bit 29-26 **CLSRC<3:0>:** Current-Limit Control Signal Source select bit for PWM Generator 'x'(2,4)

These bits specify the current-limit control signal source.

1111 = FLT15
1110 = Reserved
1101 = Reserved
1100 = Comparator 5
1011 = Comparator 4
1010 = Comparator 3
1001 = Comparator 2
1000 = Comparator 1
0111 = FLT8
0110 = FLT7
0101 = FLT6
0100 = FLT5
0011 = FLT4
0010 = FLT3
0001 = FLT2
0000 = FLT1

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```


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REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

bit 25 **CLPOL:** Current-Limit Polarity bits for PWM Generator 'x'(2,4)
1 = The selected current-limit source is active-low
0 = The selected current-limit source is active-high

bit 24 **CLMOD:** Current-Limit Mode Enable bit for PWM Generator 'x'(2,4)
1 = Current-limit function is enabled
0 = Current-limit function is disabled, current-limit overrides disabled (current-limit interrupts can still be generated). If Faults are enabled, FLTMOD will override the CLMOD bit.
Changes take effect on the next PWM cycle boundary following PWM being enabled, and subsequently on each PWM cycle boundary. When updating CLMOD from '1' to '0', if the current-limit input is still active, the current-limit override condition will not be removed.

bit 23 **Unimplemented:** Read as '0'

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

bit 22-19 **FLTSRC<3:0>:** Fault Control Signal Source Select bits for PWM Generator 'x'(2,4)
These bits specify the Fault control source.
1111 = FLT15
1110 = Reserved
1101 = Reserved
1100 = Comparator 5
1011 = Comparator 4
1010 = Comparator 3
1001 = Comparator 2
1000 = Comparator 1
0111 = FLT8
0110 = FLT7
0101 = FLT6
0100 = FLT5
0011 = FLT4
0010 = FLT3
0001 = FLT2
0000 = FLT1

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```


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REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

bit 18 **FLTPOL:** Fault Polarity bits for PWM Generator 'x'(2)
1 = The selected fault source is active-low
0 = The selected fault source is active-high

bit 17-16 **FLTMOD<1:0>:** Fault Mode bits for PWM Generator 'x'(4)
11 = Fault input is disabled, no fault overrides possible. (fault interrupts can still be generated)
10 = Reserved
01 = Selected fault source forces PWMxH, PWMxL pins to FLTDAT<1:0> values (cycle by cycle)
00 = Selected fault source forces PWMxH, PWMxL pins to FLTDAT<1:0> values (Latched condition)
Changes take effect on the next PWM cycle boundary following PWM being enabled, and subsequently on each PWM cycle boundary. When updating FLTMOD<1:0> from '00' or '01' to '11' (disabled), if the fault input is still active the fault override condition will not be removed. If enabled, Faults will override the CLMOD bit setting.

bit 15 **PENH:** PWMxH Output Pin Ownership bit(1)
1 = PWM module controls PWMxH pin
0 = GPIO module controls PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit(1)
1 = PWM module controls PWMxL pin
0 = GPIO module controls PWMxL pin

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

bit 13 **POLH:** PWMxH Output Pin Polarity bit(2)
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit(2)
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD<1:0>:** PWM 'x' I/O Pin Mode bits(2)
11 = PWMxL output is held at logic '0' (adjusted by the POLL bit)
10 = PWM I/O pin pair is in Push-Pull Output mode
01 = PWM I/O pin pair is in Redundant Output mode
00 = PWM I/O pin pair is in Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT<1> provides data for output on PWMxH pin
0 = PWM generator provides data for PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT<0> provides data for output on PWMxL pin
0 = PWM generator provides data for PWMxL pin

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```


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REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

bit 7-6 **OVRDAT<1:0>:** State(3) for PWMxH, PWMxL Pins if Override is Enabled bits
If OVRENH = 1, OVRDAT<1> provides data for PWMxH
If OVRENL = 1, OVRDAT<0> provides data for PWMxL

bit 5-4 **FLTDAT<1:0>:** State(3) for PWMxH and PWMxL Pins if FLTMOD is Enabled bits(2)
If FLTMOD<1:0> (IOCONx<17:16>) = 00 or 01, one of the following Fault modes is enabled:
If fault is active, FLTDAT<1> provides the state for PWMxH
If fault is active, FLTDAT<0> provides the state for PWMxL
If fault is inactive, FLTDAT<1:0> bits are ignored

bit 3-2 **CLDAT<1:0>:** State for PWMxH and PWMxL Pins if CLMOD is Enabled bits(3)
If CLMOD (IOCONx<24>) = 1, Current-Limit mode is enabled, as follows:
If current limit is active, CLTDAT<1> provides the state for PWMxH
If current limit is active, CLTDAT<0> provides the state for PWMxL
If current limit is inactive, CLTDAT<1:0> bits are ignored

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to PWMxL pin; PWMxL output signal is connected to PWMxH pin
0 = PWMxH and PWMxL output signals pins are mapped to their respective pins

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```

REGISTER 31-12: IOCONx: PWMX I/O CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

bit 0 **OSYNC:** Output Override Synchronization bit
1 = Output overrides through the OVRDAT<1:0> bits are synchronized to the PWM time base
0 = Output overrides through the OVRDAT<1:0> bits occur on next CPU clock boundary

Note 1: During PWM initialization, if the PWMLOCK fuse bit is 'enabled' (logic '0'), the control on the state of the PWMxL/PWMxH output pins rests solely with the PENH and PENL bits. However, these bits are at '0', which leaves the pin control with the I/O module. Care must be taken to not inadvertently set the TRIS bits to output, which could impose an incorrect output on the PWMxH/PWMxL pins even if there are external pull-up and pull-down resistors. The data direction for the pins must be set to input if tri-state behavior is desired or be driven to the appropriate logic states. The PENH and PENL bits must always be initialized prior to enabling the MCPWM module (PTEN bit = 1).

2: These bits must not be changed after the MCPWM module is enabled (PTEN bit = 1).

3: State represents Active/Inactive state of the PWM, depending on the POLH and POLL bits. For example, if FLTDAT<1> is set to '1' and POLH is set to '1', the PWMxH pin will be at logic level 0 (active level) when a Fault occurs.

4: If (PWMLOCK = 0), these bits are writable only after the proper sequence is written to the PWMKEY register. If (PWMLOCK = 1), these bits are writable at all times. The user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation for the IOCONx register if PWMLOCK = 1. Write access to a IOCONx register must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. This is not an atomic operation, and therefore, any CPU interrupts that occur during or immediately after an unlock sequence may cause the IOCONx SFR write access to fail.

Note: Dead Time Compensation, Current-Limit, and Faults share common inputs on the FLTx inputs ('x' = 1-8, and 15). Therefore, it is not recommended that a user application assign these multiple functions on the same Fault FLTx pin. In addition, DTCMP functions are fixed to specific FLTx inputs, where Current-Limit, (CLSRC<3:0> bits) and Faults (FLTSRC<3:0> bits) can be assigned to any one of 15 unique and separate inputs. For example, if a user application was required to assign multiple simultaneous Fault, Current-Limit, DTCMP to a single PWM1. Refer to the following examples for both desirable and undesirable practices.

Desirable Example PWM1: (DTCMP1 = FLT3 pin, Current Limit = FLT7 pin, Fault = FLT8 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0110;    //Enable current limit for PWM1 on FLT7 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0111;   //Enable Fault for PWM1 on FLT8 pin
```

Undesirable Example: PWM1: (DTCMP1 = Current Limit = Fault = FLT3 pin)

```
PWMCON1bits.DTC = 0b11;       //Enable DTCMP1 input on FLT3 function pin
IOCON1bits.CLMOD = 1;         //Enable PWM1 Current-Limit mode
IOCON1bits.CLSRC = 0b0010;    //Enable current limit for PWM1 on FLT3 pin
IOCON1bits.FLTMOD = 1;        //Enable PWM1 Fault mode
IOCON1bits.FLTSRC = 0b0010;   //Enable Fault for PWM1 on FLT3 pin
```


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REGISTER 31-13: PDCx: PWM GENERATOR DUTY CYCLE REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PDC<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PDC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PDC<15:0>:** Primary PWM Generator 'x' Duty Cycle Value bits(2)

If Edge-Aligned mode is enabled (ECAM<1:0> bits (PWMCONx<11:10>) = 00), these bits specify the trailing edge instance of the ON time and controls the duty cycle directly (PWM Resolution = (1/ FSYCLK)).

If one of the Center-Aligned mode is enabled (ECAM<1:0> (PWMCONx<11:10>) = 01, 10, or 11), these bits specify the compare instance for 'leading edge' level transition (PWM Resolution = (2 / FSYCLK)).

Note 1: In Independent PWM mode, PMOD<1:0> (IOCONx<11:10>) = 11, the PDCx register controls the PWMxH duty cycle only. In Complementary, Redundant and Push-Pull PWM modes (PMOD<1:0> = 00, 01, or 10), the PDCx register controls the duty cycle of both the PWMxH and PWMxL.

2: PDCx = ((FSYSCLK / (FPWM * PCLKDIV<2:0> bits (PTCON<6:4>)) * Desired Duty Cycle)
FPWM = User-desired PWM Frequency.

REGISTER 31-14: SDCx: PWM SECONDARY DUTY CYCLE REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SDC<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SDC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **SDC<15:0>:** Secondary Duty Cycle bits for PWMx output pin

If Edge-Aligned mode is enabled (ECAM<1:0> (PWMCONx<11:10>) = 00) these bits are unused.

If Symmetric Center-Aligned mode is enabled (ECAM<1:0> (PWMCONx<11:10>) = 01), these bits are updated transparently to the user. Loads to the PDCx register automatically copy over to the SDCx register.

If Asymmetric Center-Aligned mode is enabled (ECAM<1:0> (PWMCONx<11:10>) = 10 or 11), these bits specify the compare instance for 'trailing edge' level transition (PWM Resolution = (2 / FSYCLK)).

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REGISTER 31-15: PHASEx: PWM PRIMARY PHASE SHIFT REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PHASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PHASE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PHASE<15:0>:** PWM Phase Shift Value or Independent Time Base Period bits for the PWM Generator bits(6)

Phase shifting is used to offset the start of a PWM Generator's time base period, relative to a master time base, as well as the generated duty cycle. Also, the effects on the operation of the PWM signals through any external control signals, such as current-limit, Fault, and dead time compensation, are also shifted in time.

Note 1: If the ITB bit (PWMCONx<9>) = 0, the following applies based on the mode of operation:

Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01, or 10) PHASE<15:0> = Phase shift value for PWMxH and PWMxL outputs

2: If the ITB bit = 1, the following applies based on the mode of operation:

Complementary, Redundant, and Push-Pull Output modes (PMOD<1:0> = 00, 01, or 10) PHASE<15:0> = local time base period value for TMRx

3: A Phase offset that exceeds the PWM period will lead to unpredictable results.

4: The minimum period value is 0x0008.

5: The SDCx register is used in Independent PWM mode only (PMOD<1:0> = 11). When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle.

6: PHASEx = (FSYSCLK / (FPWM * PCLKDIV<2:0> bits (PTCON<6:4>))
FPWM = User-desired PWM Frequency.

REGISTER 31-16: DTRx: PWM DEAD TIME REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DTR<13:8>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DTR<13:0>:** Unsigned 14-bit Dead Time Value for PWMxH Dead Time Unit bits

These bits specify the leading edge dead time count between the PWMxH and PWMxL. The time base for the count is the same as for the PWM generator.

The dead time period is typically set equal to the switching times of the power transistors in the application circuits. It is specifically intended for use in Complementary Output mode. The use of dead time in any other mode may generate unexpected or unpredictable results. If the duty cycle value in the DC register equals '0', or is greater than or equal to the Period, dead time compensation is ignored. The values for Duty Cycle + Dead Time + Dead Time Compensation must not exceed the value for the Period register minus 1. If the sum exceeds the Period Register minus 1, unexpected results may occur. The values for Duty Cycle + Dead Time - Dead Time Compensation must be greater than '0', or unexpected results may occur.

Note: DTR<13:0> and ALTDTR<13:0> should be $\geq$ 6 while using Leading Edge Blanking.

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REGISTER 31-17: ALTDTRx: PWM ALTERNATE DEAD TIME REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	ALTDTR<13:8>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALTDTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 ALTDTR**<13:0>:** Unsigned 14-bit Dead Time Value for PWMxL Dead Time Unit bits

These bits specify the trailing edge dead time count between the PWMxH and PWMxL. The time base for the count is the same as for the PWM generator.

The alternate dead time period is typically set equal to the switching times of the power transistors in the application circuits. It is specifically intended for use in Complementary Output mode. The use of dead time in any other mode may generate unexpected or unpredictable results. If the duty cycle value in the DC register equals '0', or is greater than or equal to the Period, alternate dead time compensation is ignored. The values for Duty Cycle + Dead Time + ALT Dead Time Compensation must not exceed the value for the Period Register minus 1. If the sum exceeds the Period Register -minus1, unexpected results may occur. The values for Duty Cycle + Dead Time minus Alternate Dead Time Compensation must be greater than '0', or unexpected results may occur.

Note: DTR<13:0> and ALTDTR<13:0> should be $\geq$ 6 while using Leading Edge Blanking.

REGISTER 31-18: DTCOMPx: DEAD TIME COMPENSATION REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	COMP<13:8>(1,2)					
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COMP<7:0>(1,2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **COMP<13:0>:** Dead Time Compensation Value bits(1,2)

Dead time compensation value if Dead Time compensation mode is enabled.

Note 1: COMP<13:0> Min LSb = 1 / FSYSCLK for ECAM<1:0> bits (PWMCONx<11:10>) = '0b00 Edge-Aligned mode; COMP<13:0> Min LSb = 2 / FSYSCLK for ECAM<1:0> bits (PWMCONx<11:10>)> '0b00 Center-Aligned mode.

2: When Dead Time compensation mode is selected through the DTC<1:0> bits in the PWMCONx register, an external pin, CMPx (i.e., FLTx) connected to the Dead Time Compensation module input signals, cause the value in the COMPx register to be added to or subtracted from the PWMx duty cycle. The dead time compensation input signals are sampled at the end of a PWM cycle for use in the next PWM cycle. The modification of the duty cycle duration through the CMPx registers occurs during the end (trailing edge) of the duty cycle. Dead time compensation is available only for Positive Dead Time mode. The CMPx value must be less than one-half the value of the duty cycle register, PDCx; otherwise, unpredictable behavior will result. Dead time compensation will not apply for a duty cycle of zero. In this case, the PWM output will remain zero regardless of the state of the CMPx input pin.

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REGISTER 31-19: TRIGx: PWM PRIMARY TRIGGER COMPARE VALUE REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRGCMP<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRGCMP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **TRGCMP<15:0>:** Trigger Compare Value bits

These bits specify the value to match against the local time base register PTMRx to generate a trigger to the ADC module, and an interrupt if the TRGIEN bit (PWMCONx<21>) is set.

Note: To generate a trigger at the PWM period boundary, set the compare value = 0.

REGISTER 31-20: TRGCONx: PWM TRIGGER CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRGDIV<3:0>				TRGSEL<1:0>(1)		STRGSEL<1:0>(1)	
7:0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	DTM(1,2)	STRGIS(1)	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-12 **TRGDIV<3:0>:** Trigger 'x' Output Divider bits

1111 = Trigger output for every sixteenth trigger event

•

•

•

0010 = Trigger output for every third trigger event

0001 = Trigger output for every second trigger event

0000 = Trigger output for every trigger event

bit 11-10 **TRGSEL<1:0>:** Trigger Cycle Selection for Dual Cycle PWM Cycles (Center-Aligned and Push-Pull)(1)

This bit field has no effect on the raw trigger generation for single cycle PWM modes such as edge-aligned PWM. Each time a raw comparison event occurs, the raw event is processed by the trigger divider.

11 = Reserved, default to same behavior as TRGSEL<1:0> = 00.

10 = When a trigger comparison match event occurs in the incrementing phase in the dual cycle PWM mode (PTDIR = 0), a trigger event output is generated if the trigger divider has counted the appropriate number of trigger events.

01 = When a trigger comparison match event occurs in the decrementing phase in the dual cycle PWM mode (PTDIR = 1), a trigger event output is generated if the trigger divider has counted the appropriate number of trigger events.

00 = When a trigger comparison match event occurs, generate a trigger event output if the trigger divider has counted the appropriate number of raw trigger events. For dual cycle PWM modes such as Center-Aligned mode and Push-Pull mode, the raw trigger event is generated twice every cycle. However, TRIGx/STRIGx compare values of '0' or equal to the PERIOD match register will only generate one interrupt even in the dual cycle modes.

Note 1: These bits must not be changed after the MCPWM module is enabled (PTEN bit (PTCON<15>) = 1).

2: The secondary trigger event is generated regardless of the setting of the DTM bit.

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REGISTER 31-20: TRGCONx: PWM TRIGGER CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

bit 9-8 **STRGSEL<1:0>:** Secondary Trigger Cycle Selection bits for Dual Cycle PWM Cycles (Center-Aligned and Push-Pull)(1)

These bits have no effect on the raw secondary PWM trigger generation for single cycle PWM modes such as edge aligned PWM. Each time a raw comparison event occurs, the raw event is processed by the secondary PWM trigger divider.

11 = Reserved, default to same behavior as STRGSEL<1:0> = 00

10 = When a secondary PWM trigger comparison match event occurs in the second half of a dual cycle PWM mode (PTDIR = 0), generate a secondary PWM trigger event output if the secondary PWM trigger divider has counted the appropriate number of secondary PWM trigger events.

01 = When a secondary PWM trigger comparison match event occurs in the first half of a dual cycle PWM mode (PTDIR = 1), generate a trigger event output if the secondary PWM trigger divider has counted the appropriate number of secondary PWM trigger events.

00 = When a secondary PWM trigger comparison match event occurs, generate a secondary PWM trigger event output if the trigger divider has counted the appropriate number of raw secondary PWM trigger events. For two cycle PWM modes such as Center-Aligned mode and Push-Pull mode, the raw secondary PWM trigger event is generated twice.

bit 7 **DTM:** Dual ADC Trigger Mode(1, 2)

1 = Secondary trigger event is combined with the primary trigger event for purposes of creating a combined ADC trigger

0 = Secondary trigger event is not combined with the primary trigger event for purposes of creating a combined ADC trigger

bit 6 **STRGIS:** Secondary Trigger Interrupt Select(1)

This bit should be changed by the user only when PTEN = 0.

1 = Selects the Secondary Trigger Register (STRIGx) based events for interrupts

0 = When the DTM bit (TRGCONx<7>) is clear (= 0), TRIGx-based events for interrupts are selected. When the DTM bit is set (= 1), the logical OR of both STRIGx and TRIGx based triggers for interrupts are selected.

bit 5-0 **Unimplemented:** Read as '0'

Note 1: These bits must not be changed after the MCPWM module is enabled (PTEN bit (PTCON<15>) = 1).

2: The secondary trigger event is generated regardless of the setting of the DTM bit.

REGISTER 31-21: STRIGx: SECONDARY PWM TRIGGER COMPARE REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STRGCMP<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STRGCMP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **STRGCMP<15:0>:** Secondary Trigger Value Bits

These bits store the 16-bit value to compare against PTMRx to generate a trigger to the ADC module to initiate conversion, and an interrupt if the TRGIEN bit (PWMCONx<21>) and the DTM bit (TRIGCONx<7>) are enabled.

Note: To generate a trigger at the PWM period boundary, set the compare value = 0.

Note: Min LSb = 1 / FSYSCLK.

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REGISTER 31-22: CAPx: PWM TIMER CAPTURE REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CAP<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAP<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CAP<15:0>:** Captured Local PWM Timer Value bits(1)

The value in this register represents the captured local PWM timer (TMRx) value when a leading edge is detected on the current-limit input.

Note 1: The feature is only active after LEB processing on the current-limit input signal is complete.

REGISTER 31-23: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger/retrigger the Leading-Edge Blanking counter
0 = Rising edge of PWMxH will not trigger/retrigger the Leading-Edge Blanking counter

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger/retrigger the Leading-Edge Blanking counter
0 = Falling edge of PWMxH will not trigger/retrigger the Leading-Edge Blanking counter

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger/retrigger the Leading-Edge Blanking counter
0 = Rising edge of PWMxL will not trigger/retrigger the Leading-Edge Blanking counter

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger/retrigger the Leading-Edge Blanking counter
0 = Falling edge of PWMxL will not trigger/retrigger the Leading-Edge Blanking counter

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected fault input
0 = Leading-Edge Blanking is not applied to selected fault input

bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected current-limit input
0 = Leading-Edge Blanking is not applied to selected current-limit input

bit 9-0 **Unimplemented:** Read as '0'

Note: DTR<13:0> and ALTDTR<13:0> should be $\geq$ 6 while using Leading Edge Blanking.

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REGISTER 31-24: LEBDLYx: LEADING-EDGE BLANKING DELAY REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	LEB<11:8>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LEB<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-0 **LEB<11:0>:** Leading-Edge Blanking Delay bits for Current-Limit and Fault Inputs bits

These bits specify the time period for which the selected current limit and fault signals are blanked or delayed following the selected edge transition of the PWM signals. This retriggerable counter has the PWM module clock source (SYSCLK) as the time base.

REGISTER 31-25: AUXCONx: PWM AUXILIARY CONTROL REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CHOPSEL<3:0>(1)				CHOPHEN	CHOPLEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL<3:0>:** PWM Chop Clock Source Select bits(1)

The selected signal will enable and disable (CHOP) the selected PWM outputs.

1111 = Reserved. Do not use
1110 = Reserved. Do not use
1101 = Reserved. Do not use
1100 = PWM12H selected as CHOP clock source
•
•
•
0111 = PWM7H selected as CHOP clock source
•
•
•
0001 = PWM1H selected as CHOP clock source
0000 = Chop clock generator selected as CHOP clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

Note 1: This bit should be changed only when the PTEN bit (PTCON<15>) = 0.

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PTMRx: PWM TIMER REGISTER 'x' ('x' = 1 THROUGH 12)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TMR<15:8>							
7:0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **TMR<15:0>:** PWM Timer bits

When the ECAM<1:0> bits (PWMCONx<11:10>) = 00, the counter counts upwards until a period match forces rollover.

When the ECAM<1:0> bits (PWMCONx<11:10>) ≠ 00, the counter counts downwards starting with a master time base synchronization signal to 0 and then counts upwards until the next synchronization.

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32.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MK GP/MC Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This section describes the power-saving features on the PIC32MK GP devices. These devices have multiple power domains and offer various methods and modes that allow the user to balance the power consumption with device performance.

32.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the speed of PBCLK7, or selecting a lower power clock source (i.e., LPRC or SOSC).

In addition, the Peripheral Bus Scaling mode is available for each peripheral bus where peripherals are clocked at reduced speed by selecting a higher divider for the associated PBCLKx, or by disabling the clock completely.

32.2 Power-Saving with CPU Halted

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

32.2.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted and the associated clocks are disabled. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep mode.

Sleep mode includes the following characteristics:

- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the peripheral bus clocks will start running and the device will enter into Idle mode.

32.2.2 IDLE MODE

In Idle mode, the CPU is Halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

32.2.3 DEEP SLEEP MODE

Deep Sleep mode brings the device into its lowest power consumption state without requiring the use of external switches to remove power from the device.

- **Deep Sleep**
  In this mode, the CPU, RAM and most peripherals are powered down. Power is maintained to the DSGPR0 register and one or more of the RTCC, DSWDT and DSGPR1 through DSGPR32 registers.

Which of these peripherals is active depends on the state of the following register bits when Deep Sleep mode is entered:

- **RTCDIS (DSCON<12>)**
  This bit must be set to disable the RTCC in Deep Sleep mode (Register 32-1).
- **DSWDTEN (DEVCFG2<27>)**
  This Configuration bit must be set to enable the DSWDT register in Deep Sleep mode (Register 41-5)
- **DSGPREN (DSCON<13>)**
  This bit must be set to enable the DSGPR1 through DSGPR32 registers in Deep Sleep mode, and will only maintain their value through Deep Sleep mode if enabled. (Register 32-1).

Note:	The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, the Deep Sleep Control registers and DSGPR1-32 must be written twice as part of a silicon anti-corruption check in case of a write during a power fail.

In addition to the conditionally enabled peripherals described above, $\overline{\text{MCLR}}$ and INT0 pin are enabled in Deep Sleep mode.

32.2.4 VBAT MODE

VBAT mode is similar to Deep Sleep mode, except that the device is powered from the V_{BAT} pin. VBAT mode is controlled strictly by hardware, without any software intervention. VBAT mode is initiated when V_{DD} falls below V_{POR} (refer to the **36.0 "Electrical Characteristics"** chapter for definitions of V_{DD} and V_{POR}). An external power source must be connected to the V_{BAT} pin before power is removed from V_{DD} to enter VBAT mode. VBAT is the lowest battery-powered mode that can maintain an RTCC. Wake-up from VBAT mode can only occur when V_{DD} is reapplied. The wake-up will appear to be a POR to the rest of the device.

In VBAT mode, the Deep Sleep Watchdog Timer is disabled. The RTCC and DSGPR1 through DSGPR32 registers may be enabled or disabled depending on the state of the RTCDIS bit (DSCON<12>) and the DSGPREN bit (DSCON<13>), respectively. Deep Sleep Persistent General Purpose Register 0 (DSGPR0) is always enabled in VBAT mode.

32.2.5 POWER-SAVING MODES

Figure 32-1 shows a block diagram and the related power-saving features. The various blocks are controlled by the following Configuration bit settings and SFRs:

- DSBOREN (DEVCFG2<20>)
- DSEN (DSCON<15>)
- DSGPREN (DSCON<13>)
- DSWDTEN (DEVCFG2<27>)
- DSWDTOSC (DEVCFG2<26>)
- RELEASE (DSCON<0>)
- RTCCLKSEL (RTCCON <9:8>)
- RTCDIS (DSCON<12>)
- SLPEN (OSCCON<4>)
- VREGS (PWRCON<0>)

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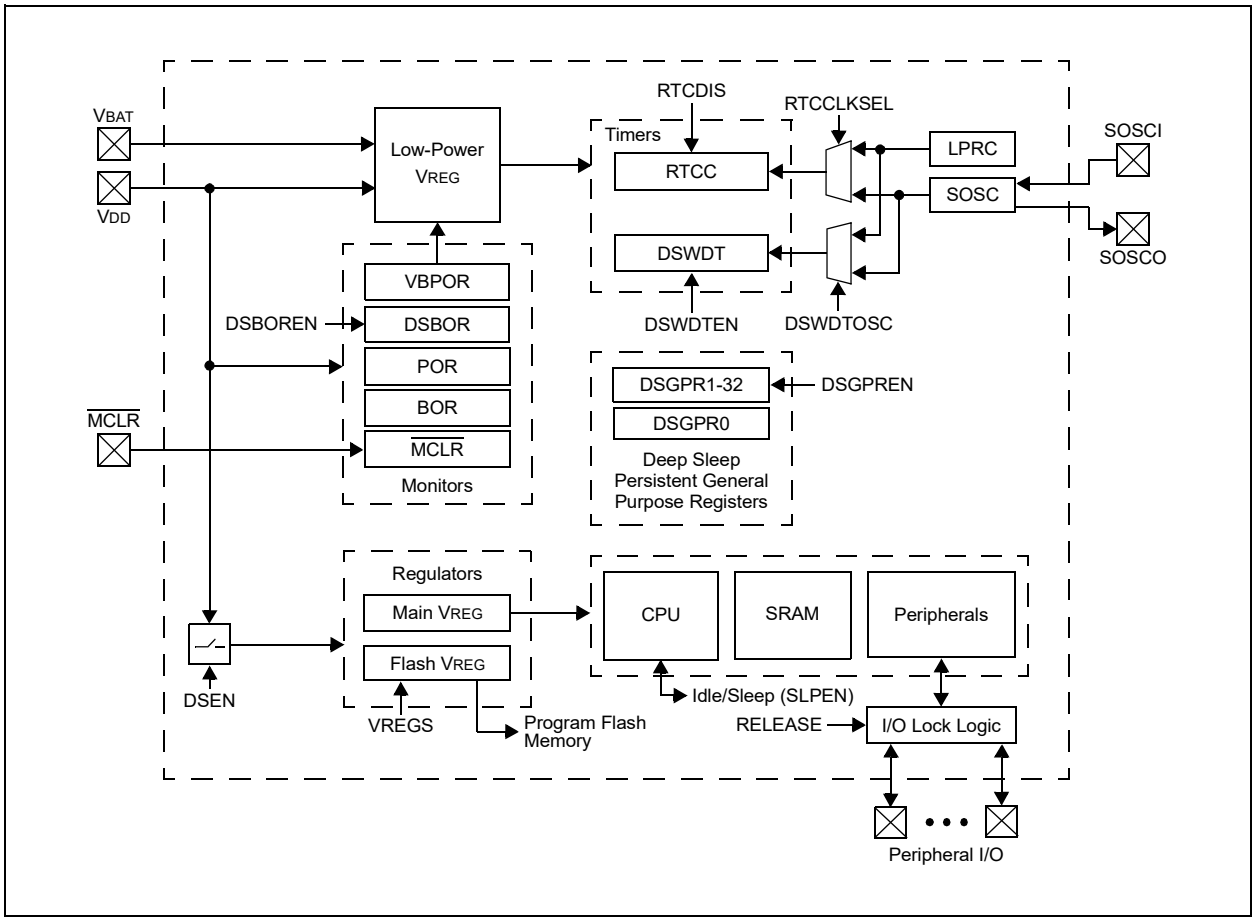
FIGURE 32-1: LOW-POWER DEVICE BLOCK DIAGRAM



32.3 Deep Sleep (DSCTRL) Control Registers

TABLE 32-1: POWER-SAVING MODES REGISTER SUMMARY

Virtual Address (BF8C_#)	Register Name(2)	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	DSCON(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DSEN	—	DSGPREN	RTCDIS	—	—	—	RTCCWDIS	—	—	—	—	—	WAKEDIS	DSBOR	RELEASE	0000
0204	DSWAKE(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	DSINT0	DSFLT	—	—	DSWDT	DSRTC	DSMCLR	—	—	0000
0208	DSGPR0(1)	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0210	DSGPR1	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0214	DSGPR2	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0218	DSGPR3	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
021C	DSGPR4	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0220	DSGPR5	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0224	DSGPR6	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0228	DSGPR7	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
022C	DSGPR8	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0230	DSGPR9	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0234	DSGPR10	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0238	DSGPR11	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
023C	DSGPR12	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice. In addition, to ensure the write is successful, these registers must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

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TABLE 32-1: POWER-SAVING MODES REGISTER SUMMARY

Virtual Address (BF8C_#)	Register Name(2)	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0240	DSGPR13	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0244	DSGPR14	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0248	DSGPR15	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
024C	DSGPR16	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0250	DSGPR17	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0254	DSGPR18	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0258	DSGPR19	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
025C	DSGPR20	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0260	DSGPR21	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0264	DSGPR22	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0268	DSGPR23	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
026C	DSGPR24	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0270	DSGPR25	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0274	DSGPR26	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0278	DSGPR27	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
027C	DSGPR28	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice. In addition, to ensure the write is successful, these registers must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

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TABLE 32-1: POWER-SAVING MODES REGISTER SUMMARY

Virtual Address (BF8C_#)	Register Name(2)	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0280	DSGPR29	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0284	DSGPR30	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
0288	DSGPR31	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000
028C	DSGPR32	31:16	Deep Sleep Persistent General Purpose bits <31:16>																0000
		15:0	Deep Sleep Persistent General Purpose bits <15:0>																0000

Legend: — = unimplemented, read as '0'.

Note 1: The DSGPR0 register is persistent in all device modes of operation.

2: The Deep Sleep Control registers can only be accessed after the system unlock sequence has been performed. In addition, these registers must be written twice. In addition, to ensure the write is successful, these registers must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

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REGISTER 32-1: DSCON: DEEP SLEEP CONTROL REGISTER(3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	HC, R/W-y	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	DSEN(1)	—	DSGPREN	RTCDIS	—	—	—	RTCCWDIS
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DSBOR(2)	RELEASE

Legend:	HC = Hardware Cleared	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **DSEN:** Deep Sleep Enable bit(1)
- 1 = Deep Sleep mode is entered on a WAIT command
- 0 = Sleep mode is entered on a WAIT command

bit 14 **Unimplemented:** Read as '0'

bit 13 **DSGPREN:** General Purpose Registers Enable bit
- 1 = General purpose register retention is enabled in Deep Sleep mode
- 0 = No general purpose register retention in Deep Sleep mode

bit 12 **RTCDIS:** RTCC Module Disable bit
- 1 = RTCC module is not enabled
- 0 = RTCC module is enabled

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **RTCCWDIS:** RTCC Wake-up Disable bit
- 1 = Wake-up from RTCC is disabled
- 0 = Wake-up from RTCC is enabled

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **DSBOR:** Deep Sleep BOR Event Status bit(2)
- 1 = DSBOREN was enabled and VDD dropped below the DSBOR threshold during Deep Sleep(2)
- 0 = DSBOREN was disabled, or VDD did not drop below the DSBOR threshold during Deep Sleep

bit 0 **RELEASE:** I/O Pin State Release bit
- 1 = Upon waking from Deep Sleep, the I/O pins maintain their previous states
- 0 = Release I/O pins and allow their respective TRIS and LAT bits to control their states

Note 1: To enter Deep Sleep mode, Sleep mode must be executed after setting the DSEN bit.

2: Unlike all other events, a Deep Sleep Brown-out Reset (BOR) event will not cause a wake-up from Deep Sleep mode; this bit is present only as a status bit.

3: The DSCON<RELEASE> must be cleared after waking from deep sleep to write to the DSWAKE register.

Note: To ensure a successful write, this register must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

REGISTER 32-2: DSWAKE: DEEP SLEEP WAKE-UP SOURCE REGISTER(3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS
	—	—	—	—	—	—	—	DSINT0
7:0	R/W-0, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0
	DSFLT	—	—	DSWDT	DSRTC	DSMCLR	—	—

Legend:		HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8 **DSINT0:** Interrupt-on-Change bit
1 = Interrupt-on-change was asserted during Deep Sleep
0 = Interrupt-on-change was not asserted during Deep Sleep

bit 7 **DSFLT:** Deep Sleep Fault Detected bit
1 = A Fault occurred during Deep Sleep and some Deep Sleep configuration settings may have been corrupted
0 = No Fault was detected during Deep Sleep

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **DSWDT:** Deep Sleep Watchdog Timer Time-out bit
1 = The Deep Sleep Watchdog Timer timed out during Deep Sleep
0 = The Deep Sleep Watchdog Timer did not time-out during Deep Sleep

bit 3 **DSRTC:** Real-Time Clock and Calendar Alarm bit
1 = The Real-Time Clock and Calendar triggered an alarm during Deep Sleep
0 = The Real-Time Clock and Calendar did not trigger an alarm during Deep Sleep

bit 2 **DSMCLR:** $\overline{\text{MCLR}}$ Event bit
1 = The $\overline{\text{MCLR}}$ pin was active and was asserted during Deep Sleep
0 = The $\overline{\text{MCLR}}$ pin was not active, or was active, but not asserted during Deep Sleep

bit 1-0 **Unimplemented:** Read as '0'

Note 1: All bits in this register are cleared when the DSEN bit (DSCON<15>) is set.

2: To ensure a successful write, this register must be written twice consecutively, back-to-back with the same value, and no interrupts in between the writes.

3: After waking from deep sleep, writes to the DSWAKE register are ignored until the RELEASE bit (DSCON<0>) is cleared.

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REGISTER 32-3: DSGPRX: DEEP SLEEP PERSISTENT GENERAL PURPOSE REGISTER 'x' (x = 0 THROUGH 32)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	Deep Sleep Persistent General Purpose bits							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **Deep Sleep Persistent General Purpose bits**

Note: The contents of the DSGPR0 register are retained, even in Deep Sleep and VBAT modes. The DSPGR1 through DSPGR32 registers are disabled by default in Deep Sleep and VBAT modes, but can be enabled with the DSGPREN bit (DSCON<13>). All register bits are reset only in the case of a V_{DD} Power-on Reset (POR) event outside of Deep Sleep mode.

32.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 32-2 for more information.

Note:	Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module through the PMDx bits.

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TABLE 32-2: PERIPHERAL MODULE DISABLE REGISTER SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0040	PMD1(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	EEMD	CTMUMD	—	DAC3MD	DAC2MD	DAC1MD	—	—	—	ADCMD	0000
0050	PMD2(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	OPA5MD	—	OPA3MD	OPA2MD	OPA1MD	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	CMP5MD	C4MPMD	C3MPMD	CMP2MD	CMP1MD	0000
0060	PMD3(2)	31:16	OC16MD	OC15MD	OC14MD	OC13MD	OC12MD	OC11MD	OC10MD	OC9MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
		15:0	IC16MD	IC15MD	IC14MD	IC13MD	IC12MD	IC11MD	IC10MD	IC9MD	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
0070	PMD4(2)	31:16	—	—	—	—	PWM12MD	PWM11MD	PWM10MD	PWM9MD	PWM8MD	PWM7MD	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD	0000
		15:0	—	—	—	—	—	—		T9MD	T8MD	T7MD	T6MD	T5MD	T4MD	T3MD	T2MD	T1MD	0000
0080	PMD5(1,2)	31:16	CAN4MD	CAN3MD	CAN2MD	CAN1MD	—	—	USB2MD	USB1MD	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SPI6MD	SPI5MD	SPI4MD	SPI3MD	SPI2MD	SPI1MD	—	—	U6MD	U5MD	U4MD	U3MD	U2MD	U1MD	0000
0090	PMD6(2)	31:16	—	—	—	—	QEI4MD	QEI3MD	QEI2MD	QEI1MD	—	—	—	—	QEI6MD	QEI5MD	—	PMPMD	0000
		15:0	—	—	—	—	REFO4MD	REFO3MD	REFO2MD	REFO1MD	—	—	—	—	—	—	—	—	0000
00A0	PMD7(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	DMAMD	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

2: For any associated PMDx bit, '0' = clocks enabled to the peripheral; '1' = For associated peripheral, clocks are disabled, SFRs are reset, and CPU read/write is invalid.

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TABLE 32-3: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral	PMDx Bit Name(3)	Register Name and Bit Location
ADC1-ADC7	ADC1MD	PMD1<0>
CDAC1	DAC1MD	PMD1<4>
CDAC2	DAC2MD	PMD1<5>
CDAC3	DAC3MD	PMD1<6>
CTMU	CTMU1MD	PMD1<8>
Data EEPROM	EEMD	PMD1<9>
Comparator 1	C1MD	PMD2<0>
Comparator 2	C2MD	PMD2<1>
Comparator 3	C3MD	PMD2<2>
Comparator 4	C4MD	PMD2<3>
Comparator 5	C5MD	PMD2<4>
Op amp 1	OPA1MD	PMD2<16>
Op amp 2	OPA2MD	PMD2<17>
Op amp 3	OPA3MD	PMD2<18>
Op amp 5	OPA5MD	PMD2<20>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Input Capture 6	IC6MD	PMD3<5>
Input Capture 7	IC7MD	PMD3<6>
Input Capture 8	IC8MD	PMD3<7>
Input Capture 9	IC9MD	PMD3<8>
Input Capture 10	IC10MD	PMD3<9>
Input Capture 11	IC11MD	PMD3<10>
Input Capture 12	IC12MD	PMD3<11>
Input Capture 13	IC13MD	PMD3<12>
Input Capture 14	IC14MD	PMD3<13>
Input Capture 15	IC15MD	PMD3<14>
Input Capture 16	IC16MD	PMD3<15>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Output Compare 6	OC6MD	PMD3<21>
Output Compare 7	OC7MD	PMD3<22>
Output Compare 8	OC8MD	PMD3<23>

Note 1: The USB module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

2: This peripheral is not available on all devices. Refer to the pin feature tables (Table 2 through Table 4) to determine availability.

3: For any associated PMDx bit, `0` = clocks enabled to the peripheral; `1` = For associated peripheral, clocks are disabled, SFRs are reset, and CPU read/write is invalid.

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TABLE 32-3: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS (CONTINUED)

Peripheral	PMDx Bit Name(3)	Register Name and Bit Location
Output Compare 9	OC9MD	PMD3<24>
Output Compare 10	OC10MD	PMD3<25>
Output Compare 11	OC11MD	PMD3<26>
Output Compare 12	OC12MD	PMD3<27>
Output Compare 13	OC13MD	PMD3<28>
Output Compare 14	OC14MD	PMD3<29>
Output Compare 15	OC15MD	PMD3<30>
Output Compare 16	OC16MD	PMD3<31>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
Timer6	T6MD	PMD4<5>
Timer7	T7MD	PMD4<6>
Timer8	T8MD	PMD4<7>
Timer9	T9MD	PMD4<8>
PWM1	PWM1MD	PMD4<16>
PWM2	PWM2MD	PMD4<17>
PWM3	PWM3MD	PMD4<18>
PWM4	PWM4MD	PMD4<19>
PWM5	PWM5MD	PMD4<20>
PWM6	PWM6MD	PMD4<21>
PWM7	PWM7MD	PMD4<22>
PWM8	PWM8MD	PMD4<23>
PWM9	PWM9MD	PMD4<24>
PWM10	PWM10MD	PMD4<25>
PWM11	PWM11MD	PMD4<26>
PWM12	PWM12MD	PMD4<27>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
UART6	U6MD	PMD5<5>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
SPI3	SPI3MD	PMD5<10>
SPI4	SPI4MD	PMD5<11>

Note 1: The USB module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

2: This peripheral is not available on all devices. Refer to the pin feature tables (Table 2 through Table 4) to determine availability.

3: For any associated PMDx bit, `0` = clocks enabled to the peripheral; `1` = For associated peripheral, clocks are disabled, SFRs are reset, and CPU read/write is invalid.

TABLE 32-3: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS (CONTINUED)

Peripheral	PMDx Bit Name(3)	Register Name and Bit Location
SPI5	SPI5MD	PMD5<12>
SPI6	SPI6MD	PMD5<13>
USB1	USB1MD	PMD5<24>
USB2	USB2MD	PMD5<25>
CAN1	CAN1MD	PMD5<28>
CAN2	CAN2MD	PMD5<29>
CAN3	CAN3MD	PMD5<30>
CAN4	CAN4MD	PMD5<31>
Reference Clock 1	REFO1MD	PMD6<8>
Reference Clock 2	REFO2MD	PMD6<9>
Reference Clock 3	REFO3MD	PMD6<10>
Reference Clock 4	REFO4MD	PMD6<11>
Parallel Master Port	PMP1MD	PMD6<16>
QEI5	QEI5MD	PMD6<18>
QEI6	QEI6MD	PMD6<19>
QEI1	QEI1MD	PMD6<24>
QEI2	QEI2MD	PMD6<25>
QEI3	QEI3MD	PMD6<26>
QEI4	QEI4MD	PMD6<27>
DMA	DMAMD	PMD7<4>

Note 1: The USB module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

2: This peripheral is not available on all devices. Refer to the pin feature tables (Table 2 through Table 4) to determine availability.

3: For any associated PMDx bit, 0 = clocks enabled to the peripheral; 1 = For associated peripheral, clocks are disabled, SFRs are reset, and CPU read/write is invalid.

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32.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32MK GP/MC devices include two features to prevent alterations to enabled or disabled peripherals:

- Control Register Lock Sequence
- Configuration Bit Select Lock

32.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting the PMDLOCK bit prevents writes to the control registers and clearing the PMDLOCK bit allows writes.

To set or clear the PMDLOCK bit, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

32.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If the PMDLOCK bit remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

NOTES:

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33.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MK GP/MC family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 32. "Configuration"** (DS60001124) and **Section 33. "Programming and Diagnostics"** (DS60001129), which are available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MK GP/MC devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. These are:

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)
- Internal temperature sensor

33.1 Configuration Bits

PIC32MK GP/MC devices contain two Boot Flash memories (Boot Flash 1 and Boot Flash 2), each with an associated configuration space. These configuration spaces can be programmed to contain various device configurations. Configuration space that is aliased by the Lower Boot Alias memory region is used to provide values for Configuration registers listed below. See **4.1.1 "Boot Flash Sequence and Configuration Spaces"** for more information.

- DEVSIGN0: Device Signature Word 0 Register
- DEVCP0: Device Code-Protect 0 Register
- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3

The following run-time programmable Configuration registers provide additional configuration control:

- CFGCON: Configuration Control Register
- CFGPG: Permission Group Configuration Register
- CFGCON2: EE Data and Op amp Configuration Register

In addition, the DEVID register (Register 33-10) provides device and revision information, the DEVADC1 through DEVADC5 registers (Register 33-11) provide ADC module calibration data, and the DEVSN0 and DEVSN3 registers contain a unique serial number of the device (Register 33-12).

Note: Do not use Word program operation (NVMOP<3:0> = `0001`) when programming the device Words that are described in this section.

33.2 Registers

TABLE 33-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3FC0	DEVCFG3	31:16	FVBUSIO1	FUSBIDIO1	IOL1WAY	PMDL1WAY	PGL1WAY	—	—	—	FVBUSIO2	FUSBIDIO2	—	PWMLOCK	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
3FC4	DEVCFG2	31:16	UPLLEN	—	BORSEL	FDSEN	DSWDTEN	DSWDT OSC	DSWDTPS<4:0>					DSBOREN	VBAT BOREN	FPLLODIV<2:0>			xxxx
		15:0	—	FPLLMULT<6:0>							FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>			xxxx
3FC8	DEVCFG1	31:16	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>		FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>		IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>			xxxx
3FCC	DEVCFG0	31:16	—	EJTAGBEN	—	—	—	—	—	—	—	—	POSC BOOST	POSCGAIN<1:0>		SOSC BOOST	SOSCGAIN<1:0>		xxxx
		15:0	SMCLR	DBGPER<2:0>			—	FSLEEP	—	—	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN	DEBUG<1:0>		xxxx
3FDC	DEVCP	31:16	—	—	—	CP	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
3FEC	DEVSIGN	31:16	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx

Legend: x = unknown value on Reset; See register description detail for more information.

TABLE 33-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(2)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	CFGCON	31:16	—	—	—	—	—	ADCPRI	—	—	PWMAPIN6	PWMAPIN5	PWMAPIN4	PWMAPIN3	PWMAPIN2	PWMAPIN1	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	—	IOANCPEN	—	—	—	JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0000
00E0	CFGPG	31:16	—	—	—	—	—	—	ADCPG<1:0>		FCPG<1:0>		—	—	CAN4PG<1:0>		CAN3PG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		USB2PG<1:0>		USB1PG<1:0>		—	—	DMAPG<1:0>		—	—	CPUPG<1:0>		0000
0110	CFGCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	ENPGA5	—	ENPGA3	ENPGA2	ENPGA1	0000
		15:0	—	—	—	—	—	—	—	—	EEWS<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET, and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **13.2 "CLR, SET, and INV Registers"** for more information.

2: Reset values are dependent on the specific device.

3: This register is not available on 64-pin devices.

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TABLE 33-3: DEVICE ADC CALIBRATION SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits															All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	DEVADC0(2)	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
5004	DEVADC1(2)	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
5008	DEVADC2(2)	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
500C	DEVADC3(2)	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
5010	DEVADC4(2)	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
5014	DEVADC5(2)	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx
5018	DEVADC7(2)	31:16	ADC Calibration Data <31:16>																xxxx
		15:0	ADC Calibration Data <15:0>																xxxx

Legend: x = unknown value on Reset.
Note 1: Reset values are dependent on the specific device.
2: Before enabling the ADC, the user application must initialize the ADC calibration codes by copying them from the factory programmed DEVADCx Flash locations into the ADCxCFG special function registers, respectively.

TABLE 33-4: DEVICE EE DATA CALIBRATION SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits															All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5030	DEVEE0	31:16	EE Data Calibration Data <31:16>																xxxx
		15:0	EE Data Calibration Data <15:0>																xxxx
5034	DEVEE1	31:16	EE Data Calibration Data <31:16>																xxxx
		15:0	EE Data Calibration Data <15:0>																xxxx
5038	DEVEE2	31:16	EE Data Calibration Data <31:16>																xxxx
		15:0	EE Data Calibration Data <15:0>																xxxx
503C	DEVEE3	31:16	EE Data Calibration Data <31:16>																xxxx
		15:0	EE Data Calibration Data <15:0>																xxxx

Legend: x = unknown value on Reset.
Note 1: Reset values are dependent on the specific device.

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TABLE 33-5: DEVICE SERIAL NUMBER SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5020	DEVSN0	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx
5024	DEVSN1	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx
5028	DEVSN2	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx
502C	DEVSN3	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx

Legend: x = unknown value on Reset.
Note 1: Reset values are dependent on the specific device.

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REGISTER 33-1: DEVSIGN0: DEVICE SIGNATURE WORD 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '0'

bit 30-0 **Reserved:** Write as '1'

REGISTER 33-2: DEVCP0: DEVICE CODE-PROTECT 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	R/P	r-1	r-1	r-1	r-1
	—	—	—	CP	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Reserved:** Write as '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.

1 = Protection is disabled

0 = Protection is enabled

bit 27-0 **Reserved:** Write as '1'

REGISTER 33-3: DEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-x	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	—	EJTAGBEN	—	—	—	—	—	—
23:16	r-1	r-1	R/P	R/P	R/P	R/P	R/P	R/P
	—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>	
15:8	R/P	R/P	R/P	R/P	r-y	R/P	r-1	r-1
	SMCLR	DBGPER<2:0>			—	FSLEEP	—	—
7:0	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN(1)	DEBUG<1:0>	

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** The reset value of this bit is the same as DEVSIGN0<31>.

bit 30 **EJTAGBEN:** EJTAG Boot Enable bit
1 = Normal EJTAG functionality
0 = Reduced EJTAG functionality

bit 29-22 **Reserved:** Write as '1'

bit 21 **POSCBOOST:** Primary Oscillator Boost Kick Start Enable bit
1 = Boost the kick start of the oscillator
0 = Normal start of the oscillator

Note: For Revision A1 silicon, the POSBOOST bit should be set and do not use an external gain resistor (i.e., RSHUNT).

bit 20-19 **POSCGAIN<1:0>:** Primary Oscillator Gain Control bits
11 = Gain Level 3 (highest)
10 = Gain Level 2
01 = Gain Level 1
00 = Gain Level 0 (lowest)

bit 18 **SOSCBOOST:** Secondary Oscillator Boost Kick Start Enable bit
1 = Boost the kick start of the oscillator
0 = Normal start of the oscillator

bit 17-16 **SOSCGAIN<1:0>:** Secondary Oscillator Gain Control bits
11 = Gain Level 3 (highest)
10 = Gain Level 2
01 = Gain Level 1
00 = Gain Level 0 (lowest)

bit 15 **SMCLR:** Soft Master Clear Enable bit
1 = $\overline{\text{MCLR}}$ pin generates a normal system Reset
0 = MCLR pin generates a POR Reset

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

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REGISTER 33-3: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 14-12 **DBGPER<2:0>:** Debug Mode CPU Access Permission bits
1xx = Allow CPU access to Permission Group 2 permission regions
x1x = Allow CPU access to Permission Group 1 permission regions
xx1 = Allow CPU access to Permission Group 0 permission regions
0xx = Deny CPU access to Permission Group 2 permission regions
x0x = Deny CPU access to Permission Group 1 permission regions
xx0 = Deny CPU access to Permission Group 0 permission regions

Note: When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** This bit is controlled by debugger/emulator development tools and should not be modified by the user.

bit 10 **FSLEEP:** Flash Sleep Mode bit
1 = Flash is powered down when the device is in Sleep mode
0 = Flash power down is controlled by the VREGS bit (PWRCON<0>)

bit 9-7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit
1 = Boot code and Exception code is MIPS32
(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
0 = Boot code and Exception code is microMIPS
(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit
1 = Trace features in the CPU are enabled
0 = Trace features in the CPU are disabled

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits
11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = PGEC3/PGED3 pair is used
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit(1)
1 = JTAG is enabled
0 = JTAG is disabled

Note: On Reset, this Configuration bit is copied into JTAGEN (CFGCON<3>). If JTAGEN (DEVCFG0<2>) = 0, the JTAGEN bit cannot be set to '1' by the user application at run-time, as JTAG is always disabled. However, if JTAGEN (DEVCFG0<2>) = 1, the user application may enable/disable JTAG at run-time as by simply writing JTAGEN (CFGCON<3> as required.

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
11 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Disabled
10 = 4-wire JTAG Enabled - PGECx/PGEDx Disabled - ICD module Enabled
01 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Disabled
00 = PGECx/PGEDx Enabled - 4-wire JTAG I/F Disabled - ICD module Enabled

Note: When the FJTAGEN or JTAGEN bits are equal to '0', this prevents 4-wire JTAG debugging, but not PGECx/PGEDx debugging.

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

REGISTER 33-4: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>				
15:8	R/P	R/P	r-1	r-1	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	IESO	FSOSCEN(1)	DMTINV<2:0>			FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FDMTEN:** Deadman Timer enable bit
1 = Deadman Timer is enabled and *cannot* be disabled by software
0 = Deadman Timer is disabled and *can* be enabled by software

bit 30-26 **DMTCNT<4:0>:** Deadman Timer Count Select bits
11111 = Reserved
.
.
.
11000 = Reserved
10111 = 2^{31} (2147483648)
10110 = 2^{30} (1073741824)
10101 = 2^{29} (536870912)
10100 = 2^{28} (268435456)
.
.
.
00001 = 2^{9} (512)
00000 = 2^{8} (256)

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **WDTSPGM:** Watchdog Timer Stop During Flash Programming bit
1 = Watchdog Timer stops during Flash programming
0 = Watchdog Timer runs during Flash programming (for read/execute while programming Flash applications)

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REGISTER 33-4: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits

10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitoring Selection Configuration bits

11 = Clock switching is enabled and clock monitoring is enabled
10 = Clock switching is disabled and clock monitoring is enabled
01 = Clock switching is enabled and clock monitoring is disabled
00 = Clock switching is disabled and clock monitoring is disabled

bit 13-11 **Reserved:** Write as '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit

1 = CLKO output is disabled
0 = CLKO output signal is active on the OSC2 pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits

11 = POSC is disabled
10 = HS Oscillator mode is selected
01 = Reserved
00 = EC mode is selected

bit 7 **IESO:** Internal External Switchover bit

1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **FSOSCEN:** Secondary Oscillator Enable bit

1 = Enable SOSC
0 = Disable SOSC
NOTE: If using external clock oscillator for SOSC instead of crystal, FSOSCEN bit must be "0" with clock oscillator input connected to SOSCO, SOSC output pin not the SOSCI input pin. This will free up SOSCI pin for use as an extra I/O pin.

bit 5-3 **DMTINV<2:0>:** Deadman Timer Count Window Interval bits

111 = Window/Interval value is 127/128 counter value
110 = Window/Interval value is 63/64 counter value
101 = Window/Interval value is 31/32 counter value
100 = Window/Interval value is 15/16 counter value
011 = Window/Interval value is 7/8 counter value
010 = Window/Interval value is 3/4 counter value
001 = Window/Interval value is 1/2 counter value
000 = Window/Interval value is zero

REGISTER 33-4: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits

111 = Reserved
110 = Reserved
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = USB PLL (UPLL Module) (input clock and divider set by UPLLCON)
010 = Primary Oscillator (POSC) (HS, EC)
001 = System PLL (SPLL Module) (input clock and divider set by SPLLCON)
000 = Fast RC Oscillator (FRC) divided by the FRCDIV<2:0> bits (OSCCON<26:24>)
(supports FRC / n, where n = 1, 2, 4, 8, 16, 32, 64, 256

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REGISTER 33-5: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	r-1	R/P	R/P	R/P	R/P	R/P	R/P
	UPLLEN	—	BORSEL	FDSEN	DSWDTEN	DSWDTOSC	DSWDTPS<4:3>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	DSWDTPS<2:0>			DSBOREN	VBAT-BOREN	FPLLODIV<2:0>		
15:8	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	FPLLMULT<6:0>						
7:0	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FPLLICLK	FPLLRNG<2:0>			—	FPLLIDIV<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **UPLLEN:** USB PLL Enable bit
1 = USB PLL is disabled
0 = USB PLL is enabled

bit 30 **Reserved:** Write as '1'

bit 29 **BORSEL:** Brown-out Reset Select Trip Voltage bit
1 = BOR trip voltage 2.1V (non-Op amp device operation)
0 = BOR trip voltage 2.8V (Op amp device operation)

Note: The user application should select the greatest BORSEL voltage to enable the highest trip voltage possible that is still less than VDD application operating voltage.

bit 28 **FDSEN:** Deep Sleep Bit Enable bit
1 = DS bit (DSCON<15>) is enabled on a WAIT command
0 = DS bit (DSCON<15>) is disabled

bit 27 **DSWDTEN:** Deep Sleep Watchdog Timer Enable bit
1 = Enable DSWDT during Deep Sleep
0 = Disable DSWDT during Deep Sleep

bit 26 **DSWDTOSC:** Deep Sleep Watchdog Timer Reference Clock Select bit
1 = Select LPRC as DSWDT reference clock
0 = Select SOSC as DSWDT reference clock

REGISTER 33-5: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 25-21 **DSWDTPS<4:0>:** Deep Sleep Watchdog Timer Postscale Select bits
The DS WDT prescaler is 32; this creates an approximate base time unit of 1 ms.
11111 = 1:236 (25.7 days)
11110 = 1:235 (12.8 days)
11101 = 1:234 (6.4 days)
11100 = 1:233 (77.0 hours)
11011 = 1:232 (38.5 hours)
11010 = 1:231 (19.2 hours)
11001 = 1:230 (9.6 hours)
11000 = 1:229 (4.8 hours)
10111 = 1:228 (2.4 hours)
10110 = 1:227 (72.2 minutes)
10101 = 1:226 (36.1 minutes)
10100 = 1:225 (18.0 minutes)
10011 = 1:224 (9.0 minutes)
10010 = 1:223 (4.5 minutes)
10001 = 1:222 (135.3 s)
10000 = 1:221 (67.7 s)
01111 = 1:220 (33.825 s)
01110 = 1:219 (16.912 s)
01101 = 1:218 (8.456 s)
01100 = 1:217 (4.228 s)
01011 = 1:65536 (2.114 s)
01010 = 1:32768 (1.057 s)
01001 = 1:16384 (528.5 ms)
01000 = 1:8192 (264.3 ms)
00111 = 1:4096 (132.1 ms)
00110 = 1:2048 (66.1 ms)
00101 = 1:1024 (33 ms)
00100 = 1:512 (16.5 ms)
00011 = 1:256 (8.3 ms)
00010 = 1:128 (4.1 ms)
00001 = 1:64 (2.1 ms)
00000 = 1:32 (1 ms)

bit 20 **DSBOREN:** Deep Sleep Zero-Power BOR Enable bit
1 = Enable ZPBOR during deep sleep
0 = Disable ZPBOR during deep sleep

bit 19 **VBATBOREN:** VBAT Zero-Power BOR Enable bit
1 = Enable ZPBOR during VBAT mode
0 = Disable ZPBOR during VBAT mode

bit 18-16 **FPLLODIV<2:0>:** Default System PLL Output Divisor bits
111 = PLL output divided by 32
110 = PLL output divided by 32
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 2

bit 15 **Reserved:** Write as ‘1’

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REGISTER 33-5: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 14-8 **FPLLMULT<6:0>:** System PLL Feedback Divider bits
1111111 = Multiply by 128
1111110 = Multiply by 127
1111101 = Multiply by 126
1111100 = Multiply by 125
•
•
•
0000000 = Multiply by 1

bit 7 **FPLLICLK:** System PLL Input Clock Select bit
1 = FRC is selected as input to the System PLL
0 = POSC is selected as input to the System PLL

bit 6-4 **FPLLRNG<2:0>:** System PLL Divided Input Clock Frequency Range bits
111 = Reserved
110 = Reserved
101 = 34-64 MHz
100 = 21-42 MHz
011 = 13-26 MHz
010 = 8-16 MHz
001 = 5-10 MHz
000 = Bypass

bit 3 **Reserved:** Write as '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
111 = Divide by 8
110 = Divide by 7
101 = Divide by 6
100 = Divide by 5
011 = Divide by 4
010 = Divide by 3
001 = Divide by 2
000 = Divide by 1

REGISTER 33-6: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	r-1	r-1	r-1
	FVBUSIO1	FUSBIDIO1	IOL1WAY	PMDL1WAY	PGL1WAY	—	—	—
23:16	R/P	R/P	r-1	R/P	r-1	r-1	r-1	r-1
	FVBUSIO2	FUSBIDIO2	—	PWMLOCK	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FVBUSIO1:** USB1 VBUSON Selection bit
1 = VBUSON pin is controlled by the USB1 module
0 = VBUSON pin is controlled by the port function

bit 30 **FUSBIDIO1:** USB1 USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27 **PGL1WAY:** Permission Group Lock One Way Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 26-24 **Reserved:** Write as '1'

bit 23 **FVBUSIO2:** USB2 VBUSON Selection bit
1 = VBUSON pin is controlled by the USB2 module
0 = VBUSON pin is controlled by the port function

bit 22 **FUSBIDIO2:** USB2 USBID Selection bit
1 = USBID pin is controlled by the USB2 module
0 = USBID pin is controlled by the port function

bit 21 **Reserved:** Write as '1'

bit 20 **PWMLOCK:** PWM Write Access Select bit
1 = Write accesses to the PWM IOCONx register are not locked or protected
0 = Write accesses to the PWM IOCONx register must use the PWMKEY unlock procedure

bit 19-16 **Reserved:** Write as '1'

bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

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REGISTER 33-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	r-0	U-0
	—	—	—	—	—	ADCPRI(1)	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWMAPIN6	PWMAPIN5	PWMAPIN4	PWMAPIN3	PWMAPIN2	PWMAPIN1	ICACLK(1)	OCACLK(1)
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	r-0	r-0	U-0
	—	—	IOLOCK(1)	PMDLOCK(1)	PGLOCK(1)	—	—	—
7:0	R/W-0	U-0	U-0	U-0	R/W-1	R/W-0	U-0	R/W-1
	IOANCPEN(1)	—	—	—	JTAGEN	TROEN	—	TDOEN

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **ADCPRI:** ADC Arbitration Priority to SRAM bit(1)
- 1 = ADC gets High Priority access to SRAM
- 0 = ADC uses Least Recently Serviced Arbitration (same as other initiators)

bit 25 **Reserved:** Write as '0'

bit 24 **Unimplemented:** Read as '0'

bit 23-18 **PWMAPIN6:PWMAPIN1:** PWM Alternate I/O Pin Selection bit
- 1 = PWMxL ('x' = 1-6) functionality is replaced by PWMxH(x+6) functionality. Provides independent PWMH and PWML functionality. If PWMAPING5 or PWMAPING6 = 1, the dedicated PWM output pin functions, PWMH11 and PWMH12, respectively, will be disabled and rerouted to PWML5 and PWML6.
- 0 = PWMxL functionality remains on pins. Provides complimentary PWMH and PWML functionality.

bit 17 **ICACLK:** Input Capture Alternate Clock Selection bit(1)
- 1 = Input Capture modules use an alternative Timer pair as their timebase clock
- 0 = All Input Capture modules use Timer2/3 as their timebase clock

bit 16 **OCACLK:** Output Compare Alternate Clock Selection bit(1)
- 1 = Output Compare modules use an alternative Timer pair as their timebase clock
- 0 = All Output Compare modules use Timer2/3 as their timebase clock

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit(1)
- 1 = Peripheral Pin Select is locked. Writes to PPS registers are not allowed
- 0 = Peripheral Pin Select is not locked. Writes to PPS registers are allowed

bit 12 **PMDLOCK:** Peripheral Module Disable bit(1)
- 1 = Peripheral module is locked. Writes to PMD registers are not allowed
- 0 = Peripheral module is not locked. Writes to PMD registers are allowed

bit 11 **PGLOCK:** Permission Group Lock bit(1)
- 1 = Permission Group registers are locked. Writes to PG registers are not allowed
- 0 = Permission Group registers are not locked. Writes to PG registers are allowed

bit 10-9 **Reserved:** Write as '0'

bit 8 **Unimplemented:** Read as '0'

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

REGISTER 33-7: CFGCON: CONFIGURATION CONTROL REGISTER (CONTINUED)

bit 7 **IOANCPEN:** I/O Analog Charge Pump Enable bit(1)

1 = Charge pump is enabled
0 = Charge pump is disabled (default)

Note 1: For proper analog operation if VDD is less than 2.5V, the AICPMPEN bit (ADCCON1<12>) must be = 1 and the IOANCPEN bit must be set to '1'; however, the charge pumps will consume additional current. These bits should never be set if the VDD operating voltage is greater than 2.5V.

2: ADC throughput rate performance is reduced, as defined in the following table, if AICPMPEN = 1 or IOANCPEN (CFGCON<7) = 1.

ADC0	ADC1	ADC2	ADC3	ADC4	ADC5	ADC7	Maximum Sum of Total ADC Throughputs
ON	OFF	OFF	OFF	OFF	OFF	OFF	2 Msps
ON	ON	OFF	OFF	OFF	OFF	OFF	4 Msps
ON	ON	ON	OFF	OFF	OFF	OFF	5 Msps
OFF	OFF	OFF	ON	OFF	OFF	OFF	2 Msps
OFF	OFF	OFF	ON	ON	OFF	OFF	4 Msps
OFF	OFF	OFF	ON	ON	ON	OFF	5 Msps
OFF	OFF	OFF	ON	ON	ON	ON	5 Msps
ON	ON	ON	ON	OFF	OFF	OFF	7 Msps
ON	ON	ON	ON	ON	OFF	OFF	9 Msps
ON	ON	ON	ON	ON	ON	OFF	10 Msps
ON	OFF	OFF	ON	ON	ON	ON	7 Msps
ON	ON	OFF	ON	ON	ON	ON	9 Msps
ON	ON	ON	ON	ON	ON	ON	10 Msps

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Port Enable bit

1 = Enable the JTAG port
0 = Disable the JTAG port

Note: The reset value of this bit is the value of the JTAGEN Configuration Word setting in the DEVCFG0 register. If JTAGEN (DEVCFG0<2>) = 0, this bit cannot be set to '1' by the user application at run-time. If JTAGEN (DEVCFG0<2>) = 1, the user application may enable/disable JTAG at run-time by writing this bit to the desired value.

bit 2 **TROEN:** Trace Output Enable bit

1 = Enable trace outputs and start trace clock (trace probe must be present)
0 = Disable trace outputs and stop trace clock

Note: When the user Configuration Word, TRCEN in the DEVCFG0 register is equal to '0', the value of this bit is ignored, but has the effect of being '0'.

bit 1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG

1 = 2-wire JTAG protocol uses TDO
0 = 2-wire JTAG protocol does not use TDO

Note: Implementing the JTAG protocol over the 2-wire interface requires four 2-wire clocks for each TCK if TDO is required. However, if the values shifted out TDO are predetermined, TDO can be disabled.

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

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REGISTER 33-8: CFGPG: PERMISSION GROUP CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	ADCPG<1:0>	
23:16	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	FCPG<1:0>		—	—	CAN4PG<1:0>		CAN3PG<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAN2PG<1:0>		CAN1PG<1:0>		USB2PG<1:0>		USB1PG<1:0>	
7:0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	DMAPG<1:0>		—	—	CPUPG<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-26 **Unimplemented:** Read as '0'

bit 25-24 **ADCPG<1:0>:** ADC Permission bits
The Bus Initiator has access to access controlled memory regions as defined by the bus structure's permission group SFRs for RDPER and WRPER.
11 = Read access if RDPER<3> = 1; write access if WRPER<3> = 1
10 = Read access if RDPER<2> = 1; write access if WRPER<2> = 1
01 = Read access if RDPER<1> = 1; write access if WRPER<1> = 1
00 = Read access if RDPER<0> = 1; write access if WRPER<0> = 1

bit 23-22 **FCPG<1:0>:** Flash Control Permission Group bits
Same definition as bits 25-24.

bit 21-20 **Unimplemented:** Read as '0'

bit 19-18 **CAN4G<1:0>:** CAN4 Module Permission Group bits
Same definition as bits 25-24.

bit 17-16 **CAN3PG<1:0>:** CAN3 Module Permission Group bits
Same definition as bits 25-24.

bit 15-14 **CAN2PG<1:0>:** CAN2 Module Permission Group bits
Same definition as bits 25-24.

bit 13-12 **CAN1PG<1:0>:** CAN1 Module Permission Group bits
Same definition as bits 25-24.

bit 11-10 **USB2PG<1:0>:** USB2 Module Permission Group bits
Same definition as bits 25-24.

bit 9-8 **USB1PG<1:0>:** USB1 Module Permission Group bits
Same definition as bits 25-24.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DMAPG<1:0>:** DMA Module Permission Group bits
Same definition as bits 25-24.

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CPUPG<1:0>:** CPU Permission Group bits
Same definition as bits 25-24.

REGISTER 33-9: CFGCON2: EE DATA AND OP AMP CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	ENPGA5	—	ENPGA3	ENPAG2	ENPGA1
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EEWS<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **ENPGA5:** Enable Op amp 5 to PGA Mode bit
1 = Op amp enable 1x gain mode, 2-terminal buffer mode operation
0 = Op amp 3-terminal standard operation (default)

bit 19 **Unimplemented:** Read as '0'

bit 18 **ENPGA3:** Enable Op amp 3 to PGA Mode bit
1 = Op amp enable 1x gain mode, 2-terminal buffer mode operation
0 = Op amp 3-terminal standard operation (default)

bit 17 **ENPGA2:** Enable Op amp 2 to PGA Mode bit
1 = Op amp enable 1x gain mode, 2-terminal buffer mode operation
0 = Op amp 3-terminal standard operation (default)

bit 16 **ENPGA1:** Enable Op amp 1 to PGA Mode bit
1 = Op amp enable 1x gain mode, 2-terminal buffer mode operation
0 = Op amp 3-terminal standard operation (default)

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **EEWS<7:0>:** Read Access Count bits

These bits indicate the number of clock cycles for a read access.

Note: The EEWS<7:0> bits must be initialized before any user application EEDATA accesses are attempted. Refer to the following table.

DATA EE Wait States EEWS<7:0> bits are equal to:	PBCLK2 = (FSYSCLK / PBDIV<6:0> (PB2DIV<6:0>))
0	0-39 MHz
1	40-59 MHz
2	60-79 MHz
3	80-97 MHz
4	98-117 MHz
5	118-120 MHz

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REGISTER 33-10: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0>(1)				DEVID<27:24>(1)			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16>(1)							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8>(1)							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID(1)

Note 1: See the *"PIC32 Flash Programming Specification"* (DS60001145) for a list of Revision and Device ID values.

REGISTER 33-11: DEVADCx: DEVICE ADC CALIBRATION REGISTER 'x' ('x' = 0-5, 7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	ADCAL<31:24>							
23:16	R	R	R	R	R	R	R	R
	ADCAL<23:16>							
15:8	R	R	R	R	R	R	R	R
	ADCAL<15:8>							
7:0	R	R	R	R	R	R	R	R
	ADCAL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **ADCAL<31:0>:** Calibration Data for the ADC Module bits

Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory programmed DEVADCx Flash locations starting at 0xBFC45000 into the ADCxCFG registers starting at 0xBF887D00, respectively. Refer to **25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** for more information.

REGISTER 33-12: DEVSNx: DEVICE SERIAL NUMBER REGISTER 'x' ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	SN<31:24>							
23:16	R	R	R	R	R	R	R	R
	SN<23:16>							
15:8	R	R	R	R	R	R	R	R
	SN<15:8>							
7:0	R	R	R	R	R	R	R	R
	SN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **SN<31:0>:** Device Unique Serial Number bits

These registers contain a value, programmed during factory production test, that is unique to each unit and are user read only. These values are persistent and not erased even when a new application code is programmed into the device. These values can be used if desired as an encryption key in combination with the Microchip encryption library.

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33.3 On-Chip Voltage Regulator

The core and digital logic for all PIC32MK GP/MC devices is designed to operate at a nominal 1.2V. To simplify system designs, devices in the PIC32MK GP/MC family incorporate an on-chip regulator providing the required core logic voltage from VDD.

33.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

33.3.2 ON-CHIP REGULATOR AND BOR

PIC32MK GP/MC devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **36.1 "DC Characteristics"**.

33.4 On-chip Temperature Sensor

PIC32MK GP/MC devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **36.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** for more information).

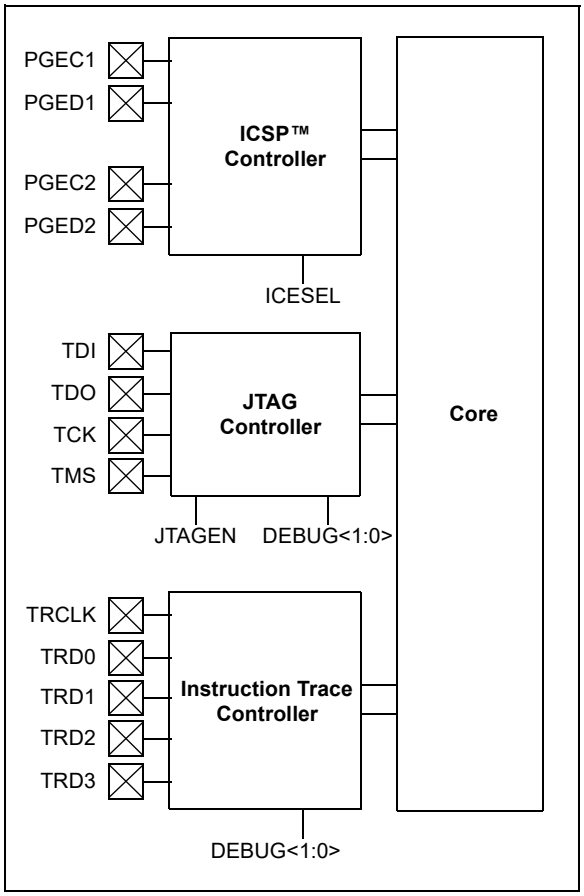
33.5 Programming and Diagnostics

PIC32MK GP/MC devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32MK devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 33-1: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS



NOTES:

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34.0 INSTRUCTION SET

The PIC32MK GP/MC family instruction set complies with the MIPS32® Release 5 instruction set architecture. The PIC32MK GP/MC device family *does not* support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note: Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

NOTES:

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35.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

35.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

35.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

35.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

35.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

35.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

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35.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

35.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

35.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

35.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

35.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

35.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

35.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

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36.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MK GP/MC electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MK GP/MC devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on V_{BAT} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on V_{DD} with respect to V_{USB3V3} ..... V_{USB3V3} -0.3V to V_{USB3V3} +0.3V
Voltage on any pin that is not 5V tolerant, with respect to V_{SS} **(Note 3)** ..... -0.3V to (V_{DD} +0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on D+ or D- pin with respect to V_{USB3V3} ..... Vss -0.3V to V_{USB3V3} +0.3V
Voltage on V_{BUS} with respect to V_{SS} ..... -0.3V to +5.5V
Maximum current out of V_{SS} pin(s) ..... 200 mA
Maximum current into V_{DD} pin(s) **(Note 2)** ..... 200 mA
Maximum current sunk/sourced by any 4x I/O pin **(Note 4)** ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin **(Note 4)** ..... 25 mA
Maximum current sunk by all ports ..... 150 mA
Maximum current sourced by all ports **(Note 2)** ..... 150 mA

Note 1: Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 36-2).

3: See the pin name tables (Table 3 and Table 5) for the 5V tolerant pins.

4: Characterized, but not tested. Refer to parameters DO10, DO20, and DO20a for the 4x and 8x I/O pin lists.

36.1 DC Characteristics

TABLE 36-1: OPERATING MIPS VERSUS VOLTAGE

Characteristic	VDD Range (in Volts) (Note 1)	Temp. Range (in °C)	Max. Frequency	Comment
			PIC32MK GP/MC Devices	
DC5	2.2V-3.6V	-40°C to +85°C	120 MHz	Industrial
DC5b	2.2V-3.6V	-40°C to +125°C	80 MHz	Extended

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is guaranteed, but not characterized. All device analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 36-5 for BOR values. Depending on the selected VBORMAX, the minimum VDD operating voltage will be either 2.2V or 2.9V based on the user application VBOR selection.

TABLE 36-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH) I/O Pin Power Dissipation: PI/O = S (({VDD – VOH} x IOH) + S (VOL x IOL))	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 36-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-pin QFN (9x9x0.9 mm)	θJA	28	—	°C/W	**1**
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θJA	55	—	°C/W	**1**
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θJA	54	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

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TABLE 36-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage (Note 1)**	2.2	—	3.6	V	—
DC12	VDR	**RAM Data Retention Voltage (Note 2)**	1.75	—	—	V	—
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal **(Note 3)**	—	—	Vss + 0.3V	V	—
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.000011	—	1.1	V/µs	300 ms to 3µs
DC18	VBAT	**Battery Supply Voltage**	2.3	—	3.6	V	—
DC19	VBATSW	**Vdd to Vbat Switch Voltage**	—	1.4	—	V	—

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 36-5 for BOR values.

2: This is the limit to which VDD can be lowered without losing RAM data.

3: This is the limit to which VDD must be lowered to ensure Power-on Reset.

TABLE 36-5: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
BO10a	VBOR	BOR Event on VDD transition high-to-low **(Note 2)**	2.735	—	2.880	V	If any OPAxMD bit (PMD2) = 0 (OPAMPx Enb)
			2.010	—	2.129	V	If all OPAxMD bits (PMD2) = 1 (by default, all Op amps are disabled on any reset)
BO10b	VBAT	BOR Event on VBAT	1.35	—	2.0	V	—

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

TABLE 36-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD RUN CURRENT WITH PERIPHERAL CLOCKS ENABLED)(1,2)

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended	
Parameter No.	**Typical(3)**	**Maximum**	**Units**	**Conditions**
Operating Current (IDD Run Current With Peripheral Clocks Enabled) (Note 1,2)				
DC20	4	24	mA	4 MHz **(Note 2,4)**
DC21	6	25	mA	10 MHz **(Note 2,4)**
DC22	20	40	mA	60 MHz **(Note 2,4)**
DC23	25	45	mA	80 MHz **(Note 2,4)**
DC25	37	55	mA	120 MHz **(Note 2,4)**
Operating Current (IDD CPU Only Run Current With Peripheral Clocks Disabled) (Note 1,2)				
DC20A	3	13	mA	4 MHz **(Note 4,5)**
DC21A	5	15	mA	10 MHz **(Note 4,5)**
DC22A	16	26	mA	60 MHz **(Note 4,5)**
DC23A	20	31	mA	80 MHz **(Note 4,5)**
DC25A	30	41	mA	120 MHz **(Note 4,5)**

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled, VUSB3V3 is connected to VDD
- PBCLKx divisor = 1:2 ('x' =/= 1,6,7), PBCLK6 = 1:4, PBCLK1 and PBCLK7 = 1:1
- CPU, Program Flash, and SRAM data memory are operational, Program Flash memory Wait states are equal to seven (default)
- Prefetch module is enabled
- No peripheral modules are operating, (ON bit = `0`), and the associated PMD bit is '`0`' (clocks enabled)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled
- IOANCPEN (CFGCON<7>) = `0`, I/O Analog Charge Pump disabled
- AICPMPEN (ADCCON1><12>) = `0`, ADC Input Charge Pump disabled

3: Data in the "Typical" column is at 3.3V, +25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: This parameter is characterized, but not tested in manufacturing.

5: **Note 2** applies with the following exceptions:

- Prefetch disabled
- Prefetch cache disabled
- PMDx = 1 (all bits set)
- PB2, 3, 4, 5, 6 = OFF
- PB1 = 1:128

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TABLE 36-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended	
Parameter No.	**Typical(2)**	**Maximum**	**Units**	**Conditions**
Idle Current (IIDLE): Core Off, Clock on Base Current (Note 1)				
DC30a	3	13	mA	4 MHz **(Note 3)**
DC31a	4	15	mA	10 MHz
DC32a	13	23	mA	60 MHz **(Note 3)**
DC33a	25	35	mA	120 MHz **(Note 3)**

Note 1: The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled, VUSB3V3 is connected to VDD
- PBCLKx divisor = 1:2 ('x' =/= 1,6,7), PBCLK6 = 1:4, PBCLK1 and PBCLK7 = 1:1
- CPU is in Idle mode (CPU core Halted)
- Prefetch module is disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is '0' (i.e., clocks enabled)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled
- IOANCPEN (CFGCON<7>) = 0, I/O Analog Charge Pump disabled
- AICPMPEN (ADCCON1><12>) = 0, ADC Input Charge Pump disabled

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

TABLE 36-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Param. No.	**Typical(2)**	**Maximum**	**Units**	**Conditions**	
Power-Down Current (IPD) (Note 1)					
DC40k	400	1200	µA	-40°C	Base Power-Down Sleep
DC40l	600	1200	µA	+25°C	
DC40m	1.8	6	mA	+85°C	
DC40o	4.5	10	mA	+125ºC	
DC41	6	40	µA	-40°C to 125ºC	Deep Sleep
DC42	6	40	µA	-40°C to 125ºC	VBAT
Module Differential Current					
DC41e	5	—	µA	3.6V	Watchdog Timer Current: ΔIWDT **(Note 3)**
DC42e	25	—	µA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)**
DC43d	3	—	mA	3.6V	ADC: ΔIADC **(Note 3, 4)**

Note 1: The test conditions for IPD current measurements are as follows:

Sleep:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled, VUSB3V3 is connected to VDD
- PBCLKx divisor = 1:2 ('x' =/= 1,6,7), PBCLK6 = 1:4, PBCLK1 and PBCLK7 = 1:1
- CPU is in Sleep mode
- Prefetch module is disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is '0' (i.e., clocks enabled)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0)
- IOANCPEN (CFGCON<7>) = 0, I/O Analog Charge Pump disabled
- AICPMPEN (ADCCON1><12>) = 0, ADC Input Charge Pump disabled

Deep Sleep Base plus Sleep:

- DSCON = POR state
- UPLLEN (DEVCFG2<31>) = 1 (PLL disabled)
- FSDEN (DEVCFG2<28>) = 1 (Deep Sleep enabled)
- DSWDTEN (DEVCFG2<27>) = 0 (Deep Sleep Watchdog disabled)
- DSBOREN (DEVCFG2<20>) = 0 (Deep Sleep BOR disabled)
- VBATBOREN (DEVCFG2<19>) = 0 (VBAT BOR disabled)

Deep Sleep with DSWDT:

- Deep Sleep Base plus DSWDTEN (DEVCFG2<27>) = 1 (Deep Sleep Watchdog enabled)

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

4: Voltage regulator is operational (VREGS = 1)

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TABLE 36-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
DI10		I/O Pins with PMP	VSS	—	0.15 VDD	V	
		I/O Pins	VSS	—	0.2 VDD	V	
	VIH	**Input High Voltage**					
DI20		I/O Pins not 5V-tolerant(5)	0.65 VDD	—	VDD	V	**(Note 4,6)**
		I/O Pins 5V-tolerant with PMP(5)	0.25 VDD + 0.8V	—	5.5	V	**(Note 4,6)**
		I/O Pins 5V-tolerant(5)	0.65* VDD	—	5.5	V	
DI30	ICNPU	**Change Notification Pull-up Current**	-450	—	-50	µA	VDD = 3.3V, VPIN = VSS **(Note 3,6)**
DI31	ICNPD	**Change Notification Pull-down Current(4)**	50	—	450	µA	VDD = 3.3V, VPIN = VDD
	IIL	**Input Leakage Current (Note 3)**					
DI50		I/O Ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
DI55		$\overline{\text{MCLR}}$(2)	—	—	±1	µA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, HS mode

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the pin name tables (Table 3 and Table 5) for the 5V-tolerant pins.

6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

TABLE 36-10: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(2,5)	mA	This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA.
DI60b	IICH	**Input High Injection Current**	0	—	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, SOSCI, SOSCO, OSC1, OSC2, D-, D+, RTCC, and RB10. Maximum IICH current for these exceptions is 0 mA.
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20(6)	—	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 3**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

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TABLE 36-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO10	VOL	**Output Low Voltage** I/O Pins 4x Sink Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15 RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5, RF6, RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	—	—	0.4	V	IOL ≤ 10 mA, VDD = 3.3V
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6, RC7, RC8, RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	—	—	0.4	V	IOL ≤ 15 mA, VDD = 3.3V
DO20	VOH	**Output High Voltage** I/O Pins: 4x Source Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15 RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5, RF6, RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6, RC7, RC8, RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V

Note 1: Parameters are characterized, but not tested.

TABLE 36-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions(1)**
DO20a	VOH1	**Output High Voltage** I/O Pins: 4x Source Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15 RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5, RF6, RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	1.5	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -12 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage I/O Pins: 8x Source Driver Pins - 8x Source Driver Pins - RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6, RC7, RC8, RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	1.5	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0	—	—	V	IOH ≥ -18 mA, VDD = 3.3V
			3.0	—	—	V	IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized, but not tested.

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TABLE 36-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS[3]			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.[1]**	**Max.**	**Units**	**Conditions**
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	VDDMIN	—	VDDMAX	V	—
D132	VPEW	VDD for Erase or Write	VDDMIN	—	VDDMAX	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	—
D135	IDDP	Supply Current during Programming	—	—	30	mA	—
D136	TRW	Row Write Cycle Time **(Notes 2, 4)**	—	72000	—	FRC Cycles	—
D137	TQWW	Quad Word Write Cycle Time **(Note 4)**	—	773	—	FRC Cycles	—
D138	TWW	Word Write Cycle Time **(Note 4)**	—	135	—	FRC Cycles	—
D139	TCE	Chip Erase Cycle Time **(Note 4)**	—	403200	—	FRC Cycles	—
D140	TPFE	Combined Upper Plus Lower Flash Panels Erase Cycle Time (both Boot Flash excluded) **(Note 4)**	—	256909	—	FRC Cycles	—
D141	TPBE	Single Panel Flash Erase Cycle Time (either Upper or Lower Panel, excluding both Boot Flash) **(Note 4)**	—	134400	—	FRC Cycles	—
D142	TPGE	Page Erase Cycle Time **(Note 4)**	—	134400	—	FRC Cycles	—
D143	TFLPU	NVM Power-up Delay	—	—	10	µs	—

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: The minimum PBCLK5 for row programming is 4 MHz.

3: Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on FRC accuracy (see Table 36-17) and FRC tuning values (see the OSCTUN register: Register 9-2).

TABLE 36-13: DC CHARACTERISTICS: PROGRAM FLASH MEMORY WAIT STATES

DC CHARACTERISTICS	Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Required Flash Wait States[1]	**FSYSCLK**	**Units**	**Conditions**
1 Wait states 3 Wait states	0 < SYSCLK ≤ 60 60 < SYSCLK ≤ 120	MHz	—

Note 1: To use Wait states, the Prefetch module must be enabled (PREFEN<1:0> ≠ 00) and the PFMWS<2:0> bits must be written with the desired Wait state value.

36.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MK GP/MC device AC characteristics and timing parameters.

FIGURE 36-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

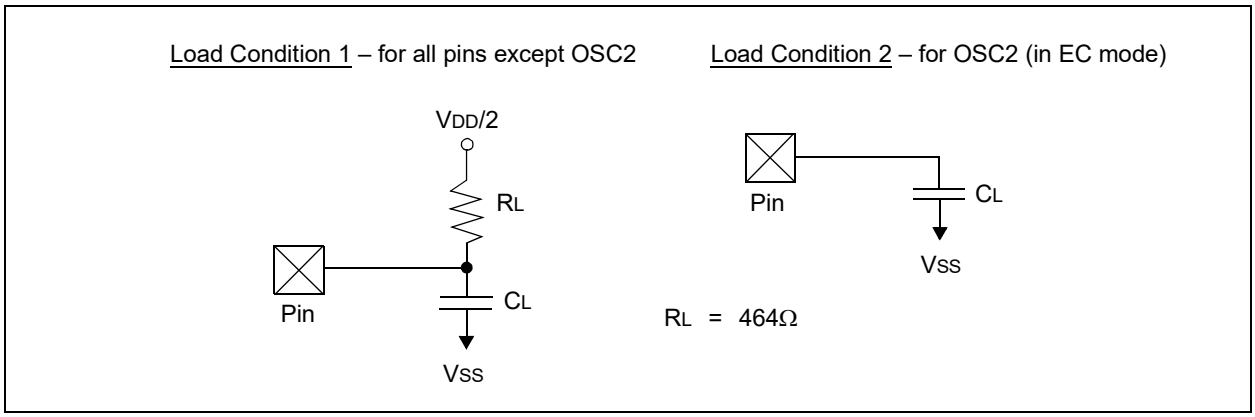

TABLE 36-14: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO56	CL	All I/O pins	—	—	50	pF	—

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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FIGURE 36-2: EXTERNAL CLOCK TIMING

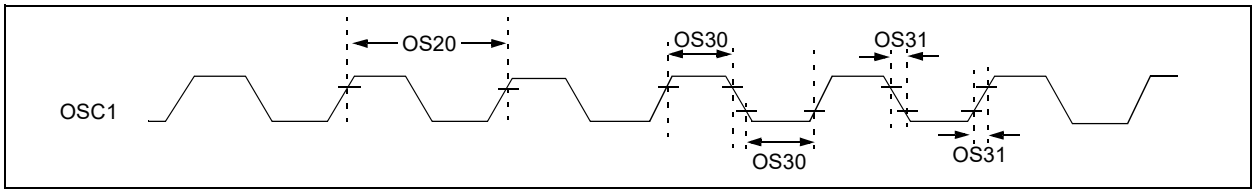

TABLE 36-15: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Minimum**	**Typical(1)**	**Maximum**	**Units**	**Conditions**
OS10	FOSC	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	64	MHz	EC **(Note 2,3)**
OS13		Oscillator Crystal Frequency	4	—	24	MHz	HS **(Note 2,3)**
OS15			32	32.768	100	kHz	SOSC **(Note 2)**
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See parameter OS10 for FOSC value
OS30	TOSL, TOSH	External Clock In (OSC1) High or Low Time	0.375 x TOSC	—	0.675 x TOSC	ns	EC **(Note 2)**
OS31	TOSR, TOSF	External Clock In (OSC1) Rise or Fall Time	—	—	7.5	ns	EC **(Note 2)**
OS40	TOST	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, and SOSC Clock Oscillator modes)	—	1024	—	TOSC	**(Note 2)**
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	**(Note 2)**
OS42	GM	External Oscillator Transconductance	—	16	—	mA/V	VDD = 3.3V, TA = +25°C, HS **(Note 2)**

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are characterized but are not tested.

2: This parameter is characterized, but not tested in manufacturing.

3: See parameter OS50 for PLL input frequency limitations.

TABLE 36-16: SYSTEM PLL TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OS50	FIN	PLL Input Frequency Range	5	—	64	MHz	—
OS51	FSYS	System Frequency	DC	—	120	MHz	USB module disabled
			30	—	120	MHz	USB module enabled
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	100	µs	—
OS53	DCLK	CLKO Stability(2) (Period Jitter or Cumulative)	-0.25	—	+0.25	%	Measured over 100 ms period
OS54	FVCO	PLL VCO Frequency Range	350	—	700	MHz	FVco output frequency to PLLODIV output
OS54a	FPLL	PLL Output Frequency Range	10	—	120	MHz	PLLODIV output frequency range
OS54b	FPLLI	VCO Input Frequency Range	5	—	64	MHz	PLLIDIV output frequency range to FVCO input
OS55a	FPB	Peripheral Bus Frequency	DC	—	120	MHz	For PBCLKx, 'x' ≠ 6
OS55b			DC	—	30	MHz	For PBCLK6

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLKx}{CommunicationClock}}}$$

For example, if PBCLKx = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

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TABLE 36-17: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	-5	—	+5	%	0°C ≤ TA ≤ +70°C
		-10	—	+10	%	-40°C ≤ TA ≤ +125°C

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

TABLE 36-18: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal LPRC @ 32.768 kHz(1)						
F21	LPRC	-8	—	+8	%	0°C ≤ TA ≤ +85°C
		-25	—	+25	%	-40°C ≤ TA ≤ +125°C

Note 1: Change of LPRC frequency as VDD changes.

TABLE 36-19: DATA EEPROM MEMORY

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Sym.**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Comments**
DE10	EP	Effective Write/Erase Cell Endurance	160K	—	Cycles	Specified at TA = +125º C
DE11	TRETD	Characteristic Retention	20	—	Year	—
DE12	TACC	Read Access Time	—	176 / PBCLK2 Frequency	ns	PBCLK2 = (FSYSCLK / PB2DIV<PBDIV>)
DE13	TDPD	Wake-up Time From Deep Power-down to Any Operation	10	—	µs	—
DE14	TPROG	Program Time	20	53	µs	—
DE15	TRCV	Program Recovery Time	5	—	µs	—
		Page Erase Recovery Time	50	—	µs	—
DE16	TERASE	Page Erase Time	—	20	ms	—
DE17	TSCE	Bulk Erase Time	—	20	ms	—
DE18	TRW	Latency to Next Operation After Program/Erase	2	—	µs	—
DE19	TPUWRITE	Power-up to Read/Program/ Erase Operation	12	—	µs	—

Note 1: Timings are for reference only and are not user-configurable. All timing is enforced by hardware.

TABLE 36-20: DATA EEPROM WAIT STATES

DATA EE Wait States EEWS<7:0> (CFGCON2<7:0>) bits are Equal to:	PBCLK2<6:0> = (FSYSCLK / PB2DIV<6:0>)
0	0-39 MHz
1	40-59 MHz
2	60-79 MHz
3	80-97 MHz
4	98-117 MHz
5	118-120 MHz

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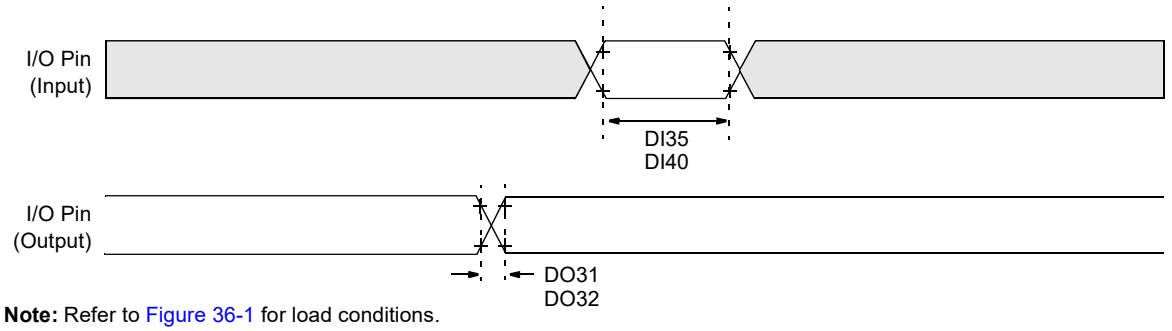
TABLE 36-21: COMPARATOR SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (Note 2): 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
CM30	VIOFF	Input Offset Voltage	-10	—	10	mV	—
CM31	VICM	Input Common Mode Voltage	AVSS +0.9	—	2.5V	V	—
CM33	TRESP	Large Signal Response Time	—	50	—	ns	VCM = VDD/2; 200 mV step
CM36	VHYST	Input Hysteresis Voltage	48	120	192	mV	—
CM37	VGAIN	Open Loop Voltage Gain	—	90	—	dB	—
CM38	TSRESP	Small Signal Response Time	—	100	—	ns	VCM = VDD/2; 100 mV step
CM39	TRISE	Output Rise Time	—	20	—	ns	Refer to parameter DO56.
CM40	TFALL	Output Fall Time	—	20	—	ns	Refer to parameter DO56.
CM41	V I/P	Input Voltage Range	AVSS	—	AVDD	V	—
CM42	ILKG	Input Leakage Control	—	See IIL in Table 36-9	—	nA	—
CM43	TON	Comparator Enabled to Output Valid	—	10	—	µs	Comparator module is configured before setting the Comparator ON bit
CM44	TOFF	Disable to outputs disabled	—	100	—	ns	—

Note 1: These parameters are characterized but not tested.

FIGURE 36-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-22: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	**Port Output Rise Time** I/O Pins: 4x Source Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15, RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5-RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 8x Source Driver Pins - Replace 8x Source Driver pins with: RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6-RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

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TABLE 36-22: I/O TIMING REQUIREMENTS (CONTINUED)

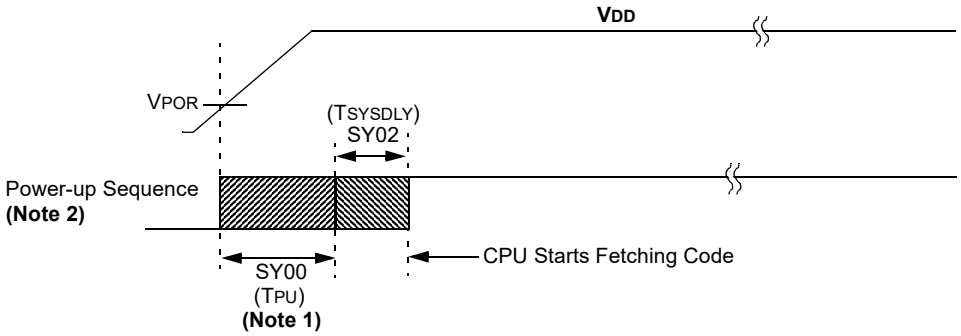
AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO32	TIOF	**Port Output Fall Time** I/O Pins: 4x Source Driver Pins - RA0, RA4, RA11, RA12, RA14, RA15, RB0-RB3, RB8, RB9 RC0, RC1, RC2, RC10, RC12, RC13 RD8, RD12-RD15 RE0, RE1, RE8, RE9 RF5-RF7, RF9, RF10, RF12, RF13 RG0, RG1, RG6-RG15	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Fall Time I/O Pins: 8x Source Driver Pins - RA1, RA7, RA8, RA10 RB4-RB7, RB10-RB15 RC6-RC9, RC11, RC15 RD1-RD6 RE12-RE15 RF0, RF1	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
DI35	TINP	INTx Pin High or Low Time	5	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	5	—	—	ns	—

Note 1: Data in the “Typical” column is at 3.3V, +25°C unless otherwise stated.

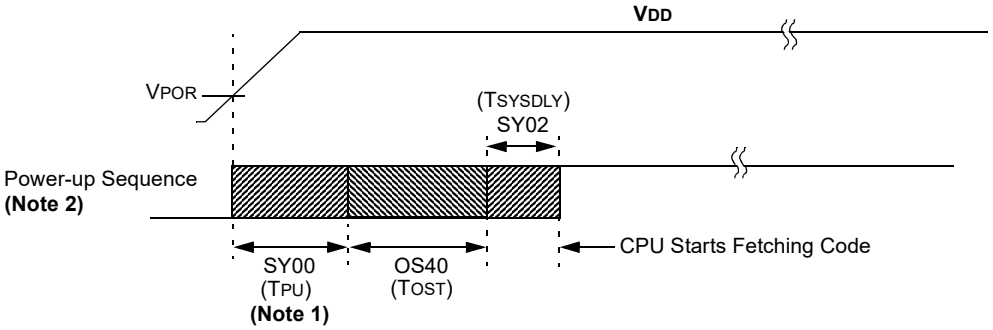
2: This parameter is characterized, but not tested in manufacturing.

FIGURE 36-4: POWER-ON RESET TIMING CHARACTERISTICS

Internal Voltage Regulator Enabled
Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)



Internal Voltage Regulator Enabled
Clock Sources = (HS, HSPLL, and SOSC)



Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{DDMIN}$).

2: Includes interval voltage regulator stabilization delay.

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FIGURE 36-5: EXTERNAL RESET TIMING CHARACTERISTICS

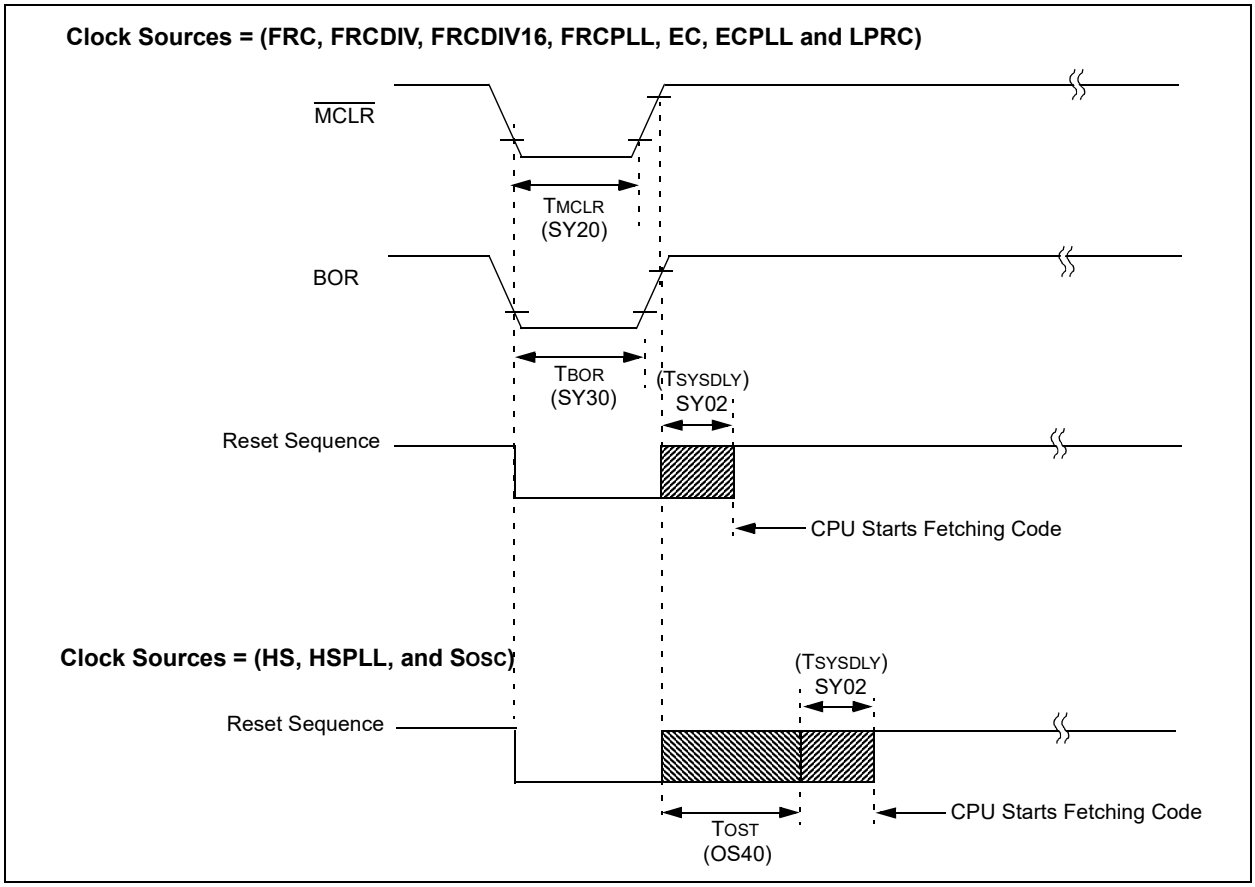


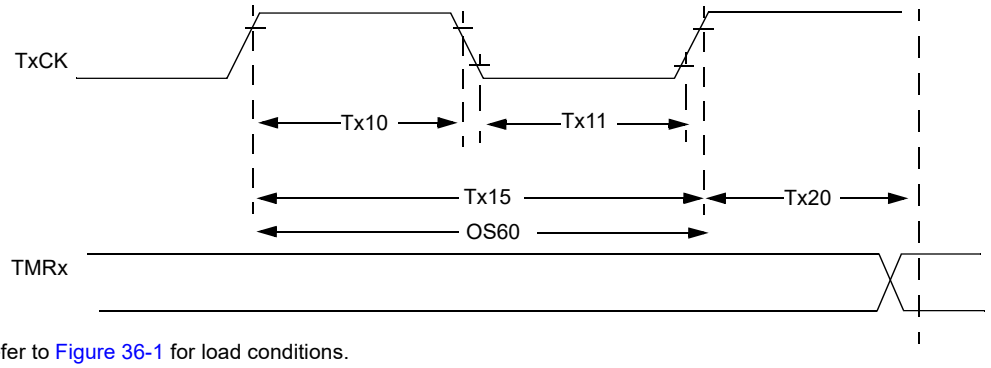
TABLE 36-23: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	—
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	—	1 μs + 8 SYSCLK cycles	—	—	—
SY20	TMCLR	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	μs	—
SY30	TBOR	BOR Pulse Width (low)	—	1	—	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Characterized by design but not tested.

FIGURE 36-6: TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS(1)				Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(2)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 20 ns	—	—	ns	Must also meet parameter TA15 (**Note 3**)
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of 20 ns or 2 TPBCLK3)/N] + 30 ns	—	—	ns	VDD > 2.7V (**Note 3**)
				[(Greater of 20 ns or 2 TPBCLK3)/N] + 50 ns	—	—	ns	VDD < 2.7V (**Note 3**)
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V
				50	—	—	ns	VDD < 2.7V
OS60	FT1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	50	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPBCLK3	—

Note 1: Timer1 is a Type A.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

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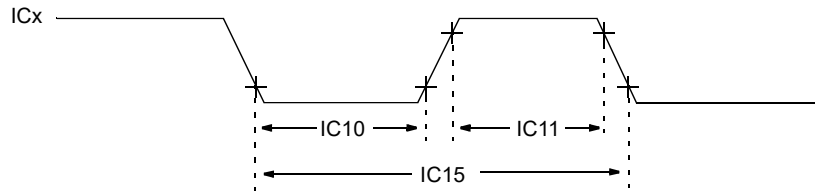
TABLE 36-25: TIMER2-TIMER9 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**		**Min.**	**Max.**	**Units**	**Conditions**	
TB10	TTXH	TxCK High Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 25 ns	—	ns	Must also meet parameter TB15	N = prescale value (1, 2, 4, 8, 16, 32, 64, 256)
TB11	TTXL	TxCK Low Time	Synchronous, with prescaler	[(12.5 ns or 1 TPBCLK3) /N] + 25 ns	—	ns	Must also meet parameter TB15	
TB15	TTXP	TxCK Input Period	Synchronous, with prescaler	[(Greater of [(25 ns or 2 TPBCLK3)/N] + 30 ns	—	ns	VDD > 2.7V	
				[(Greater of [(25 ns or 2 TPBCLK3)/N] + 50 ns	—	ns	VDD < 2.7V	
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TPBCLK3	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 36-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS



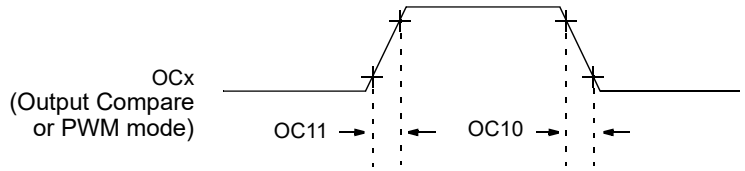
Note: Refer to Figure 36-1 for load conditions.

TABLE 36-26: INPUT CAPTURE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TCCL	ICx Input Low Time	((TPBCLKx/N) + 25 ns)	—	ns	Must also meet parameter IC15.	x = 2 for IC1-IC9 x = 3 for IC10-IC16 N = prescale value (1, 4, 16)
IC11	TCCH	ICx Input High Time	((TPBCLKx/N) + 25 ns)	—	ns	Must also meet parameter IC15.	
IC15	TCCP	ICx Input Period	((TPBCLKx/N) + 50 ns)	—	ns	—	

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 36-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

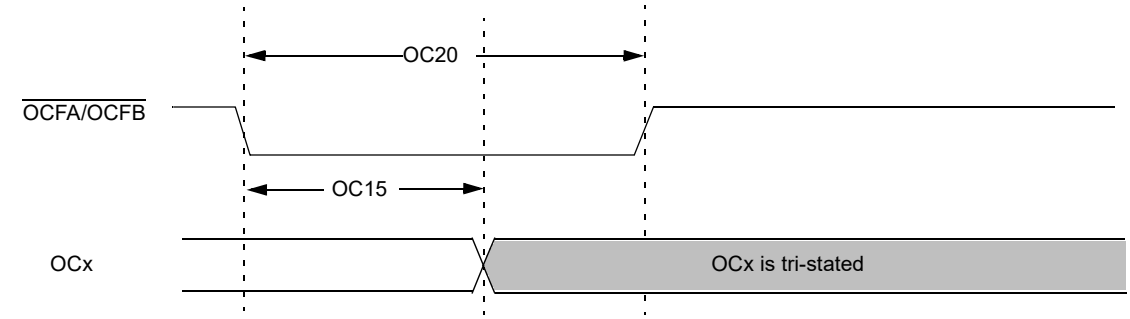
TABLE 36-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 36-9: OCx/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-28: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typ.(2)**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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TABLE 36-29: OP AMP SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Comments**
OA1	VCMR	Common Mode Input Voltage Range	AVSS	—	AVDD	V	—
OA2	CMRR	Common Mode Rejection Ratio	—	70	—	dB	VCM = AVDD/2
OA3	VOFFSET	Op amp Offset Voltage	-5	—	5	mV	—
OA4	VGAINCL	Closed Loop Voltage Gain	8	—	—	V	Non-inverting configuration, RF/RI ≥ 8
OA5	ILKG	Input leakage current	—	—	See IIL in Table 36-9	nA	—
OA6	PSRR	Power Supply Rejection Ratio	—	-75	—	dB	—
OA7	VGAIN	Open Loop Voltage Gain	—	90	—	dB	—
OA8	VOH	Amplifier Output Voltage High	—	AVDD - 0.077	—	V	ISOURCE ≤ 500 µA
			—	AVDD - 0.037	—	V	ISOURCE ≤ 200 µA
			—	AVDD - 0.018	—	V	ISOURCE ≤ 100 µA
OA9	VOL	Amplifier Output Voltage Low	—	AVSS + 0.077	—	V	ISINK ≤ 500 µA
			—	AVSS + 0.037	—	V	ISINK ≤ 200 µA
			—	AVSS + 0.018	—	V	ISINK ≤ 100 µA
OA10	TON	Enable to Valid Output	—	10	—	µs	—
OA11	TOFF	Disable to Outputs Disabled	—	100	—	ns	—
OA11	IOS	Input Offset Current	—	See IIL in Table 36-9	—	—	—
OA13	IB	Input Bias Current	—	See IIL in Table 36-9	—	—	—
OA14	SR	Slew Rate	7.0	9.0	—	V/µs	Measured with a 0.5V to 2.5V step change
OA15	GBW	Gain Bandwidth	10.0	—	—	MHz	—
OA16	AV	Gain	8.0	—	—	V/V	Minimum op-amp stable gain
OA17	PM	Phase Margin	43	65	—	Degrees	—

Note 1: Data in the “Typical” column is at 3.3V, +25°C unless otherwise stated.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, Op amp/Comparator, and Comparator voltage reference, will have degraded performance. Refer to parameter BO10 in Table 36-5 for the minimum and maximum BOR values.

TABLE 36-30: OP AMP UNITY GAIN BUFFER MODE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (Note 3): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
UG10	IDCBIAS	DC Bias Current	-1.25	—	1.25	µA	—
UG20	GBW	Gain Bandwidth	—	7.5	—	MHz	—
UG30	VOUTOFFSET	Output Offset Voltage	-20	—	20	mV	—
UG40	PSRR	Power Supply Rejection Ratio	—	-78	—	dB	Specified at 0 Hz
UG50	PEAK	Peak Gain	—	2	—	dB	Gain in excess of 1 (@ > 6 MHz)

Note 1: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: All other specifications are identical to the regular Op amp mode operation.

3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, Op amp/Comparator, and Comparator voltage reference, will have degraded performance. Refer to parameter BO10 in Table 36-5 for the minimum and maximum BOR values.

TABLE 36-31: UNITY GAIN OP AMP TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
0A10	SR	Slew Rate	7	—	—	V/µs	From 0.5V to 2.5V
OA20	PM	Phase Margin	—	65	—	Degree	RF/RI = 3; Non-inverting gain configuration = 4
OA30	GM	Gain Margin	—	20	—	dB	RF/RI = 3; Non-inverting gain configuration = 4
OA40	GBW	Gain Bandwidth	—	10	—	MHz	—

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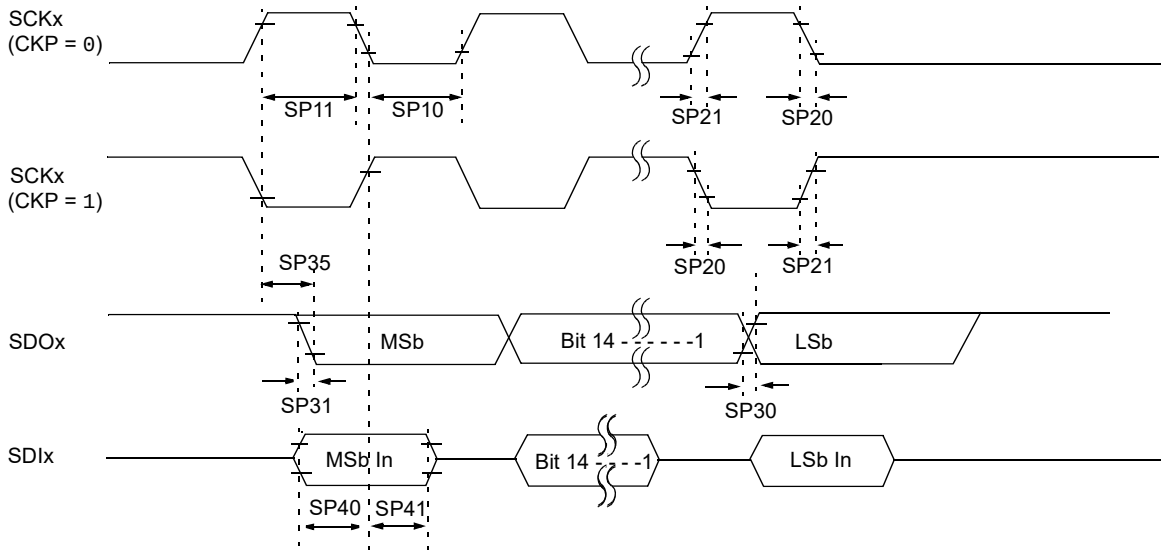
FIGURE 36-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-32: SPIx MASTER MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9a	TSCK	SCKx Period (SPI1-2 only)	28	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			—	35	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			—	41	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			—	47	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 30 pF load on all SPIx pins.

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TABLE 36-32: SPIx MASTER MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9b	TSCK	SCKx Period (SPI3-6 only)	45	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 All other remappable SPI pins not contained in conditions for parameter SP9a. Applies only to SPI3-SPI6.
			—	64	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 All other remappable SPI pins not contained in conditions for parameter SP9a. Applies only to SPI3-SPI6.
			—	82	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1. All other remappable SPI pins not contained in conditions for parameter SP9a. Applies only to SPI3-SPI6.
			—	97	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 All other remappable SPI pins not contained in conditions for parameter SP9a. Applies only to SPI3-SPI6.
SP10	TSCL	SCKx Output Low Time	TSCK/2	—	—	ns	—
SP11	TSCH	SCKx Output High Time	TSCK/2	—	—	ns	—
SP20	TSCF	SCKx Output Fall Time **(Note 3)**	—	—	—	ns	See parameter DO32
SP21	TSCR	SCKx Output Rise Time **(Note 3)**	—	—	—	ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time **(Note 3)**	—	—	—	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time **(Note 3)**	—	—	—	ns	See parameter DO31
SP35	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 3.0V
			—	—	10	ns	VDD < 3.0V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 30 pF load on all SPIx pins.

TABLE 36-32: SPIx MASTER MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS (CONTINUED)

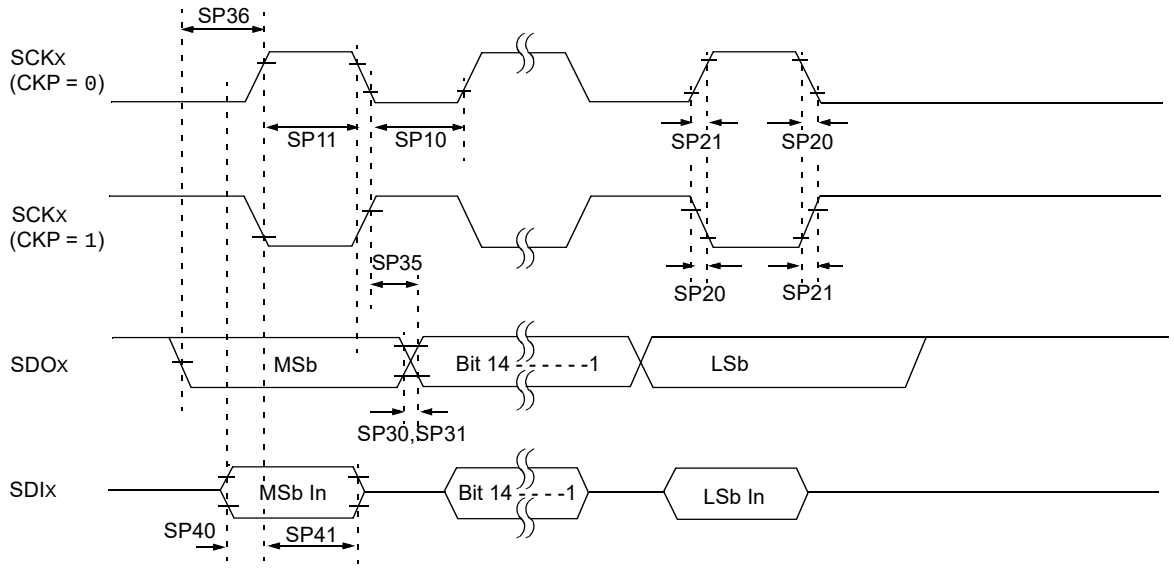
AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 30 pF load on all SPIx pins.

FIGURE 36-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

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TABLE 36-33: SPIx MODULE MASTER MODE (CKE = 1, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

TABLE 36-33: SPIx MODULE MASTER MODE (CKE = 1, SMP = 1) TIMING REQUIREMENTS (CONTINUED) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9b	TSCK	SCKx Period	22	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0. All other remappable SPI pins not contained in conditions for parameter SP9a.
			41	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0. All other remappable SPI pins not contained in conditions for parameter SP9a.
			59	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1. All other remappable SPI pins not contained in conditions for parameter SP9a.
			74	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1. All other remappable SPI pins not contained in conditions for parameter SP9a.
SP10	TSCL	SCKx Output Low Time	TSCK/2	—	—	ns	—
SP11	TSCH	SCKx Output High Time	TSCK/2	—	—	ns	—
SP20	TSCF	SCKx Output Fall Time **(Note 3)**	—	—	—	ns	See parameter DO32
SP21	TSCR	SCKx Output Rise Time **(Note 3)**	—	—	—	ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time **(Note 3)**	—	—	—	ns	See parameter DO32
SP30a	TSCK	SCKx Period	20	—	—	ns	Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
SP30b			40	—	—	ns	All other remappable SPI pins not contained in conditions for parameter SP9a.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

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TABLE 36-33: SPIx MODULE MASTER MODE (CKE = 1, SMP = 1) TIMING REQUIREMENTS (CONTINUED) (CONTINUED)

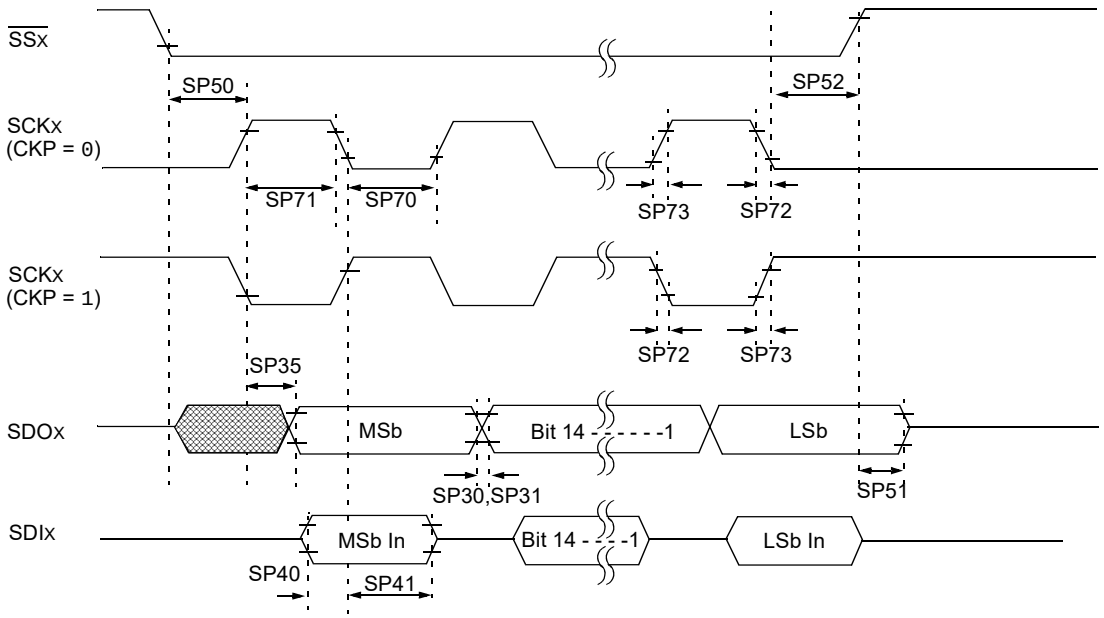
AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP31	TDOR	SDOx Data Output Rise Time **(Note 3)**	—	—	—	ns	See parameter DO31
SP35	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.7V
			—		10		VDD < 2.7V
SP36	TDOV2SC, TDOV2SCL	SDOx Data Output Setup to First SCKx Edge	7	—	—	ns	—
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	7	—	—	ns	VDD > 2.7V
			10				VDD < 2.7V
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	VDD > 2.7V
			10	—	—	ns	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

FIGURE 36-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

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TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS (CONTINUED) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9b	TSCK	SCKx Period	22	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0 All other remappable SPI pins not contained in conditions for parameter SP9a.
			41	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0 All other remappable SPI pins not contained in conditions for parameter SP9a.
			59	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1 All other remappable SPI pins not contained in conditions for parameter SP9a.
			74	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1 All other remappable SPI pins not contained in conditions for parameter SP9a.
SP70	TSCL	SCKx Input Low Time	TSCK/2	—	—	ns	—
SP71	TSCH	SCKx Input High Time	TSCK/2	—	—	ns	—
SP72	TSCF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TSCR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time **(Note 3)**	—	—	—	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time **(Note 3)**	—	—	—	ns	See parameter DO31
SP35	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.7V
			—	—	10	ns	VDD < 2.7V
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

TABLE 36-34: SPIx MODULE SLAVE MODE (CKE = 0, SMP = 1) TIMING REQUIREMENTS (CONTINUED) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

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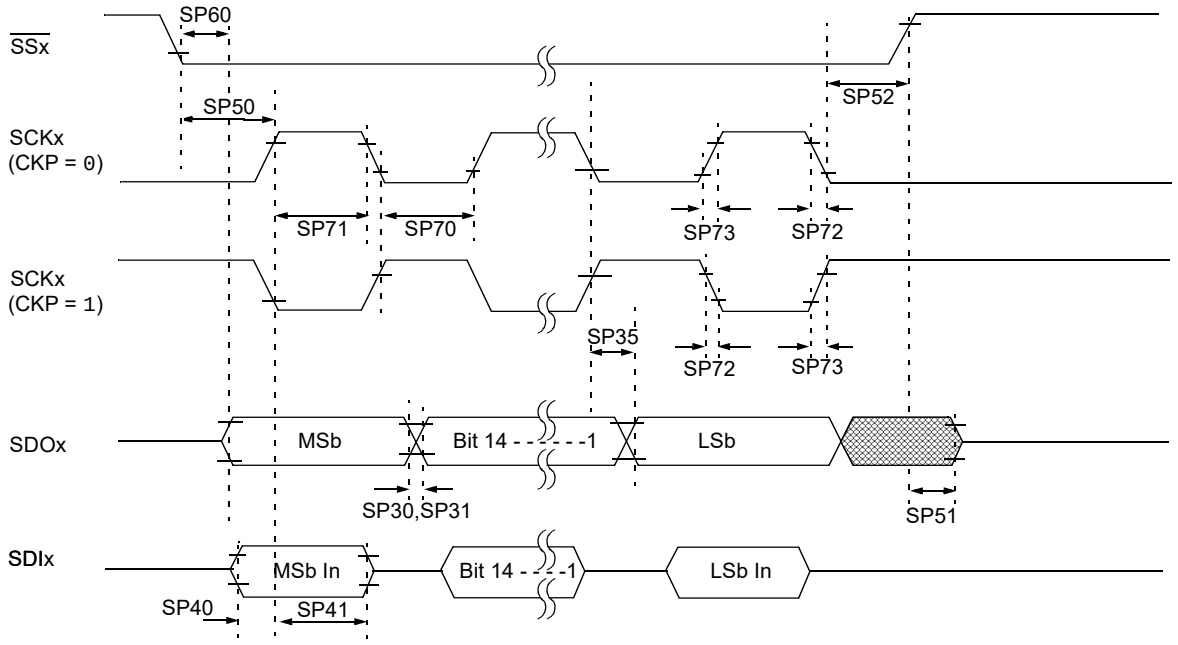
FIGURE 36-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 36-1 for load conditions.

TABLE 36-35: SPIx MODULE SLAVE MODE (CKE = 1, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9a	TSCK	SCKx Period	20	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			27	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			33	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.
			39	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1. Dedicated SCK1 and SCK2 on RB7 and RB6, respectively or PPS remappable SPI onto pins RB5, RA1, and RB15.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

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TABLE 36-35: SPIx MODULE SLAVE MODE (CKE = 1, SMP = 1) TIMING REQUIREMENTS (CONTINUED) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP9b	TSCK	SCKx Period	22	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 0. All other remappable SPI pins not contained in conditions for parameter SP9a.
			41	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 0. All other remappable SPI pins not contained in conditions for parameter SP9a.
			59	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 0, SRCON1x.y = 1. All other remappable SPI pins not contained in conditions for parameter SP9a.
			74	—	—	ns	(VDD ≥ 3.0V and the SMP bit (SPIxCON<9> = 1), I/O Pin Slew Rate Control (x = A-F, y = port pin), SRCON0x.y = 1, SRCON1x.y = 1. All other remappable SPI pins not contained in conditions for parameter SP9a.
SP70	TSCL	SCKx Input Low Time	TSCK/2	—	—	ns	—
SP71	TSCH	SCKx Input High Time	TSCK/2	—	—	ns	—
SP72	TSCF	SCKx Input Fall Time	—	—	10	ns	—
SP73	TSCR	SCKx Input Rise Time	—	—	10	ns	—
SP30	TDOF	SDOx Data Output Fall Time **(Note 3)**	—	—	—	ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time **(Note 3)**	—	—	—	ns	See parameter DO31
SP35	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid after SCKx Edge	—	—	10	ns	VDD > 2.7V
			—	—	15	ns	VDD < 2.7V
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	0	—	—	ns	—
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

TABLE 36-35: SPIx MODULE SLAVE MODE (CKE = 1, SMP = 1) TIMING REQUIREMENTS (CONTINUED) (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 3)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	—
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Assumes 10 pF load on all SPIx pins.

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FIGURE 36-14: QEI MODULE EXTERNAL CLOCK TIMING CHARACTERISTICS

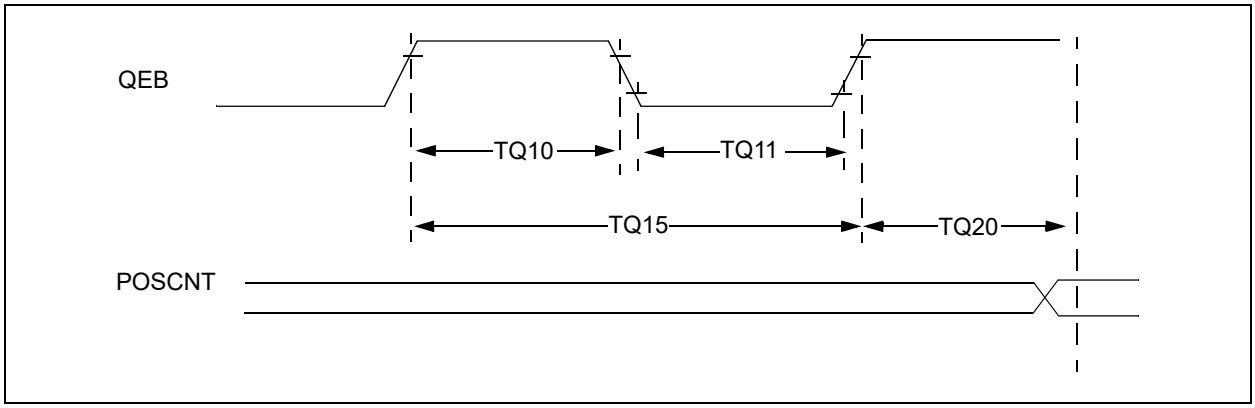

TABLE 36-36: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	[(12.5 or 0.5 TCY) / N] + 25	—	—	ns	Must also meet parameter TQ15. N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	[(12.5 or 0.5 TCY) / N] + 25	—	—	ns	Must also meet parameter TQ15. N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	[(25 or TCY) / N] + 50	—	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)**
TQ20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—	1	TCY	—	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: N = Index Channel Digital Filter Clock Divide Select bits.

FIGURE 36-15: QEA/QEB INPUT CHARACTERISTICS

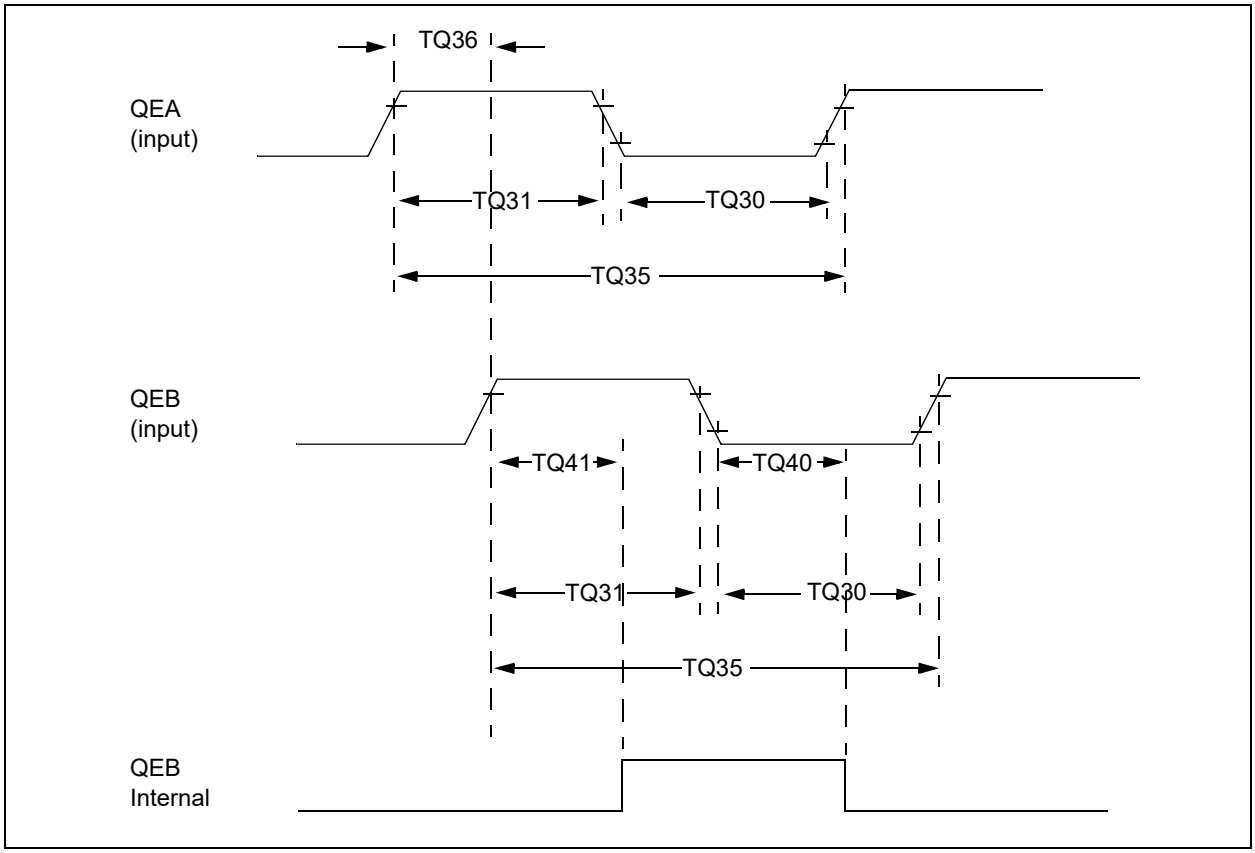

TABLE 36-37: QUADRATURE DECODER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Symbol**	**Characteristic(1)**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
TQ30	TQUL	Quadrature Input Low Time	6 TCY	—	ns	—
TQ31	TQUH	Quadrature Input High Time	6 TCY	—	ns	—
TQ35	TQUIN	Quadrature Input Period	12 TCY	—	ns	—
TQ36	TQUP	Quadrature Phase Period	3 TCY	—	ns	—
TQ40	TQUFL	Filter Time to Recognize Low, with Digital Filter	3 * N * TCY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)**
TQ41	TQUFH	Filter Time to Recognize High, with Digital Filter	3 * N * TCY	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)**

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits.

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FIGURE 36-16: CANx MODULE I/O TIMING CHARACTERISTICS

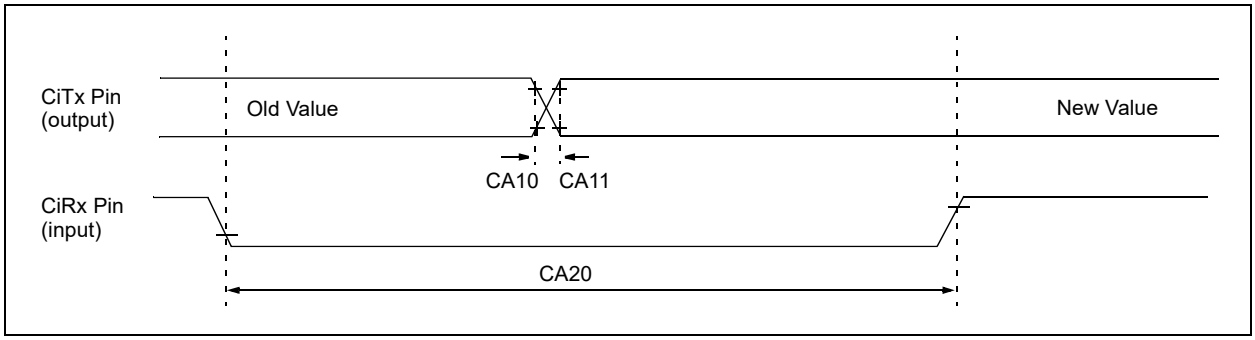

TABLE 36-38: CANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter DO31
CA20	Tcwf	Pulse Width to Trigger CAN Wake-up Filter	700	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 36-39: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.3	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	VREFL + 1.8	—	AVDD	V	**(Note 1)**
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 1.8	V	**(Note 1)**
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	1.8	—	AVDD	V	**(Note 2)**
AD08	IREF	Current Drain	—	102	—	µA	ADC is operating or is in Stand-by.
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS	—	VREFL	V	—
AD14	VINH	Absolute VINH Input Voltage	AVSS	—	VREFH	V	—
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 Resolution Ranges
AD21c	INL	Integral Nonlinearity	—	±3	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	±1	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD23c	GERR	Gain Error	—	±8	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	EOFF	Offset Error	—	±2	—	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed **(Note 2)**
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	—	67	—	dB	Single-ended **(Notes 2,3)**
AD34b	ENOB	Effective Number of bits	—	10.8	—	bits	**(Notes 2,3)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

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TABLE 36-40: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS(2)			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	16.667	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC5 (Class 1 Inputs)	— — — —	— — — —	3.75 4.284 4.992 6	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	— — — —	— — — —	3.53 4.00 4.615 5.45	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC5 (Class 1 Inputs)	3 4 5 13	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	4 5 6 14	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and Class 3 Inputs)	See Table 36-41	—	—	TAD	CVDEN (ADCCON1<11>) = 1
AD62	TCONV	Conversion Time (after sample time is complete)	— — — —	— — — —	13 11 9 7	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
AD65	TWAKE	Wake-up time from Low-Power Mode	— —	500 20	— —	TAD µs	Lesser of 500 TAD or 20 µs

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

TABLE 36-41: ADC SAMPLE TIMES WITH CVD ENABLED

AC CHARACTERISTICS(2)			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
AD60a	TSAMP	Sample Time for ADC7 (Class 2 and Class 3 Inputs) with the CVDEN bit (ADCCON1<11>) = 1	8 9 11 12 14 16 17	—	—	TAD	Source Impedance ≤ 200Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001 CVDCPL<2:0> (ADCCON2<28:26>) = 010 CVDCPL<2:0> (ADCCON2<28:26>) = 011 CVDCPL<2:0> (ADCCON2<28:26>) = 100 CVDCPL<2:0> (ADCCON2<28:26>) = 101 CVDCPL<2:0> (ADCCON2<28:26>) = 110 CVDCPL<2:0> (ADCCON2<28:26>) = 111
			10 12 14 16 18 19 21	—	—	TAD	Source Impedance ≤ 500Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001 CVDCPL<2:0> (ADCCON2<28:26>) = 010 CVDCPL<2:0> (ADCCON2<28:26>) = 011 CVDCPL<2:0> (ADCCON2<28:26>) = 100 CVDCPL<2:0> (ADCCON2<28:26>) = 101 CVDCPL<2:0> (ADCCON2<28:26>) = 110 CVDCPL<2:0> (ADCCON2<28:26>) = 111
			13 16 18 21 23 26 28	—	—	TAD	Source Impedance ≤ 1 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001 CVDCPL<2:0> (ADCCON2<28:26>) = 010 CVDCPL<2:0> (ADCCON2<28:26>) = 011 CVDCPL<2:0> (ADCCON2<28:26>) = 100 CVDCPL<2:0> (ADCCON2<28:26>) = 101 CVDCPL<2:0> (ADCCON2<28:26>) = 110 CVDCPL<2:0> (ADCCON2<28:26>) = 111
			41 48 56 63 70 78 85	—	—	TAD	Source Impedance ≤ 5 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001 CVDCPL<2:0> (ADCCON2<28:26>) = 010 CVDCPL<2:0> (ADCCON2<28:26>) = 011 CVDCPL<2:0> (ADCCON2<28:26>) = 100 CVDCPL<2:0> (ADCCON2<28:26>) = 101 CVDCPL<2:0> (ADCCON2<28:26>) = 110 CVDCPL<2:0> (ADCCON2<28:26>) = 111

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

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TABLE 36-42: CONTROL DAC (CDAC) SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CDAC							
CD10	VOUT	CDAC Output Voltage Range for Guaranteed Settling Time Specifications	0.1 * CDACVREF	—	0.9 * CDACVREF	V	@ ILOAD = IOUT (max)
CD11	N	CDAC Resolution	12	—	—	Bits	Guaranteed Monotonic by architecture
CD12	INL	CDAC Integral Nonlinearity	—	±2	±4	LSB	Guaranteed Monotonic by architecture with CDACVREF = AVDD
CD13	DNL	CDAC Differential Nonlinearity	-1	±1	<+2	LSB	Guaranteed Monotonic by architecture with CDACVREF = AVDD
CD14	OERR	CDAC Offset Error	-5	20	35	mV	CDACVREF = AVDD
CD15	GERR	CDAC Gain Error	-2	0	+2	% of FS	CDACVREF = AVDD
CD16	CDACVREF	CDAC VREF Input Range	0.5	—	AVDD	V	—
CD17	TON	CDAC Module Turn On Time	—	1.0	2	µs	From write of DACON bit
CD18	TOFF	CDAC Module Turn Off Time	—	1.0	2	µs	From write of DACON bit
CD19	TST	Settling Time	—	3	6	µs	Output is within ±4 LSb of desired output step voltage with a 10% to 90% step or 90% to 10% step. With load capacitance of 30 pF.
CD20	FS	Sampling Frequency	—	—	1	Msps	Maximum frequency for a correct CDAC output change for small variations of input codes (from code to code plus 1 LSb).
CD21	CLOAD	Output Load Capacitance	---	—	30	pF	User application loads
DC22	IOUT	Output Current Drive Strength	—	—	1.5	mA	Sink and source

TABLE 36-43: CTMU CURRENT SOURCE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU CURRENT SOURCE							
CTMU0	RES	Resolution	-2	—	+2	ºC	3.3V @ -40ºC to 125ºC
CTMUI1	IOUT1	Base Range(1)	—	0.55	—	µA	CTMUCON<1:0> = 01
CTMUI2	IOUT2	10x Range(1)	—	5.5	—	µA	CTMUCON<1:0> = 10
CTMUI3	IOUT3	100x Range(1)	—	55	—	µA	CTMUCON<1:0> = 11
CTMUI4	IOUT4	1000x Range(1)	—	550	—	µA	CTMUCON<1:0> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage(1,2)	—	0.598	—	V	TA = +25ºC, CTMUCON<1:0> = 01
			—	0.658	—	V	TA = +25ºC, CTMUCON<1:0> = 10
			—	0.721	—	V	TA = +25ºC, CTMUCON<1:0> = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change(1,2)	—	-1.92	—	mV/ºC	CTMUCON<1:0> = 01
			—	-1.74	—	mV/ºC	CTMUCON<1:0> = 10
			—	-1.56	—	mV/ºC	CTMUCON<1:0> = 11

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL

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FIGURE 36-17: PARALLEL SLAVE PORT TIMING

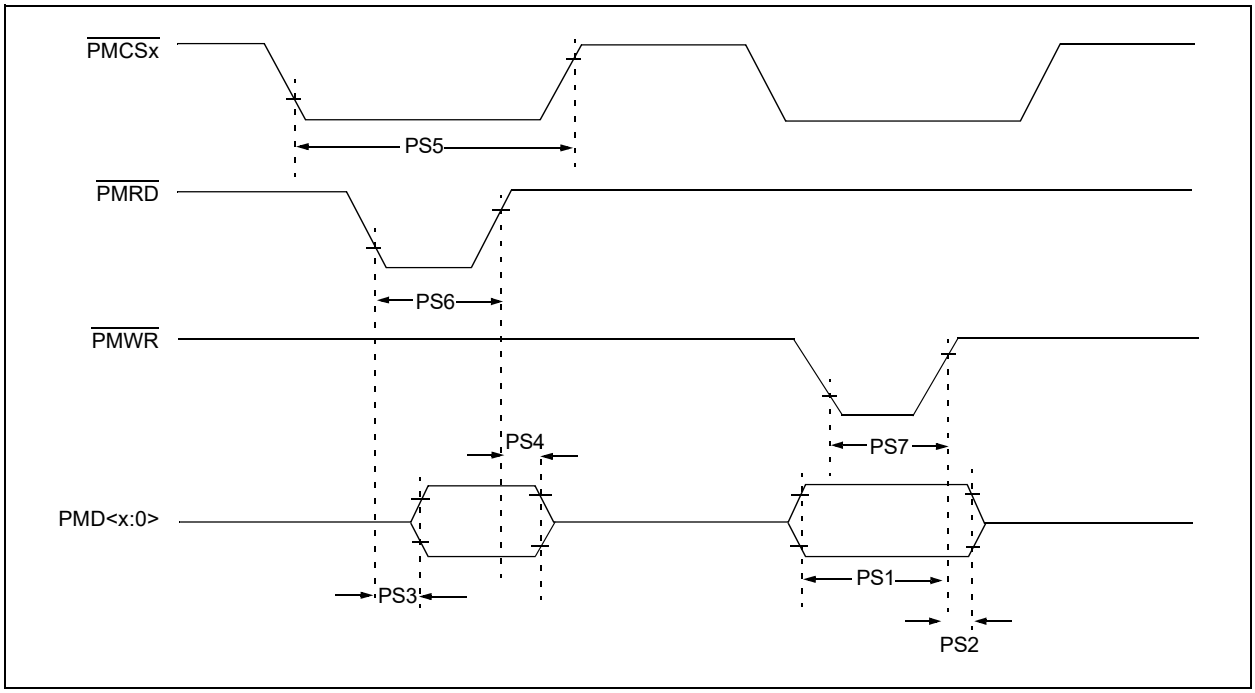

TABLE 36-44: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{\text{PMWR}}$ or $\overline{\text{PMCSx}}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtI	$\overline{\text{PMWR}}$ or $\overline{\text{PMCSx}}$ Inactive to Data-in Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	$\overline{\text{PMRD}}$ and $\overline{\text{PMCSx}}$ Active to Data-out Valid	—	—	60	ns	—
PS4	TrdH2dtI	$\overline{\text{PMRD}}$ Active or $\overline{\text{PMCSx}}$ Inactive to Data-out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{\text{PMCSx}}$ Active Time	TPBCLK2 + 40	—	—	ns	—
PS6	TWR	$\overline{\text{PMWR}}$ Active Time	TPBCLK2 + 25	—	—	ns	—
PS7	TRD	$\overline{\text{PMRD}}$ Active Time	TPBCLK2 + 25	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 36-18: PARALLEL MASTER PORT READ TIMING DIAGRAM

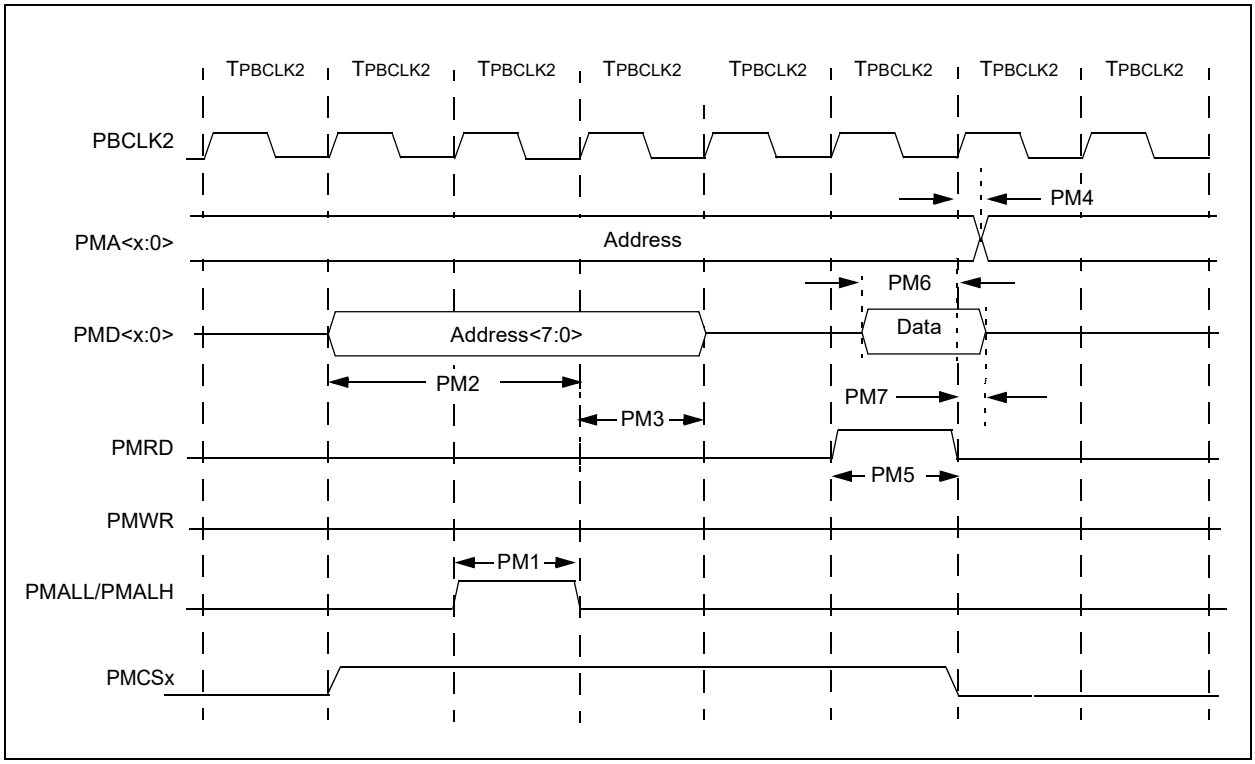

TABLE 36-45: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPBCLK2	—	—	—
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)	—	2 TPBCLK2	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPBCLK2	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPBCLK2	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	5	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

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FIGURE 36-19: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

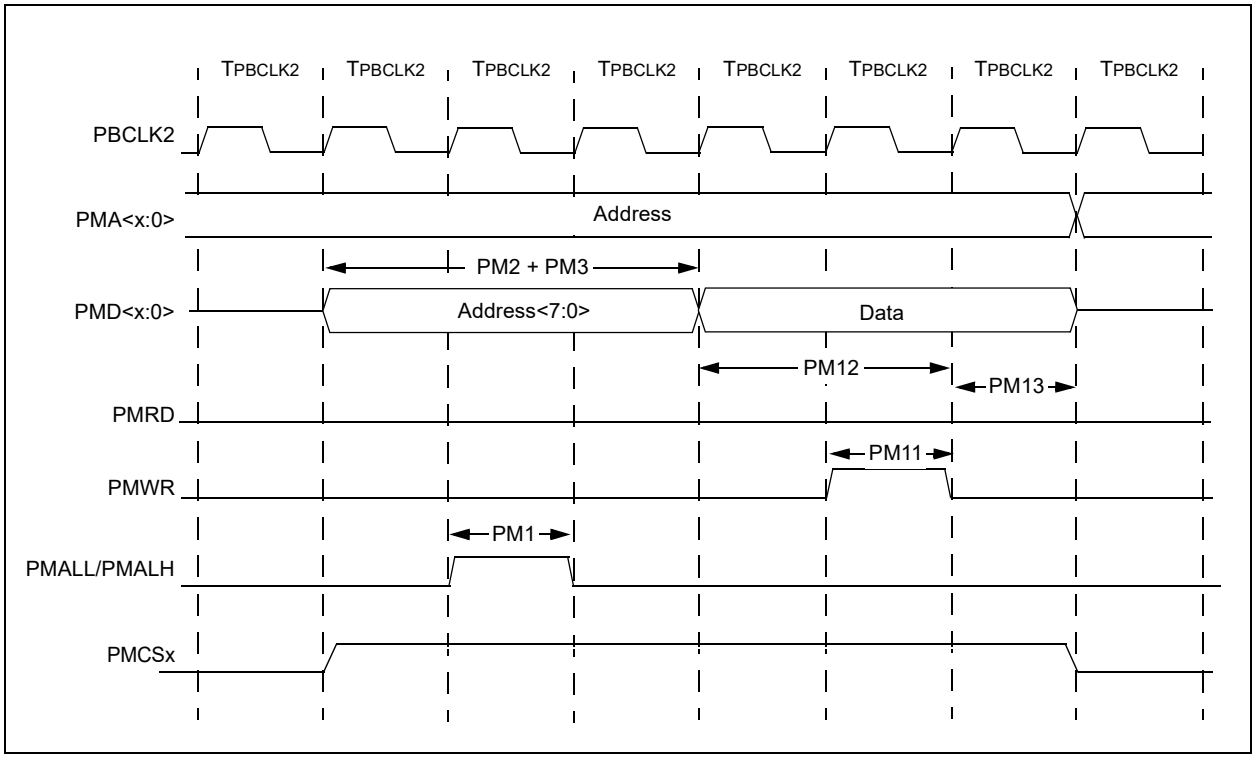

TABLE 36-46: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM11	TWR	PMWR Pulse Width	—	1 TPBCLK2	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPBCLK2	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPBCLK2	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 36-47: USB OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Two requirements for proper USB operation: • 3V ≤ VUSB3V3 ≤ 3.6V • (VUSB3V3 - 0.3V) ≤ VDD ≤ (VUSB3V3 + 0.3V)
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB320	ZOUT	Driver Output Impedance	28.0	—	44.0	Ω	—
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 36-48: UART TIMING CHARACTERISTICS

AC CHARACTERISTICS				Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
UT10	FB	Baud Rate	BRGH = 0	—	—	7.5	Mbps	Baud rate = (FPBy / (16 * (UxBRG + 1)) where: 'x' = 1-6 'y' = FPBCLK2 for UART1 and UART2 'y' = FPBLKC3 for UART3-UART6
UT20			BRGH = 1	—	—	30	Mbps	Baud rate = (FPBy / (4 * (UxBRG + 1)) where: 'x' = 1-6 'y' = FPBCLK2 for UART1 and UART2 'y' = FPBLKC3 for UART3-UART6

Note 1: These parameters are characterized, but not tested in manufacturing.

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FIGURE 36-20: MOTOR CONTROL PWM MODULE FAULT TIMING CHARACTERISTICS

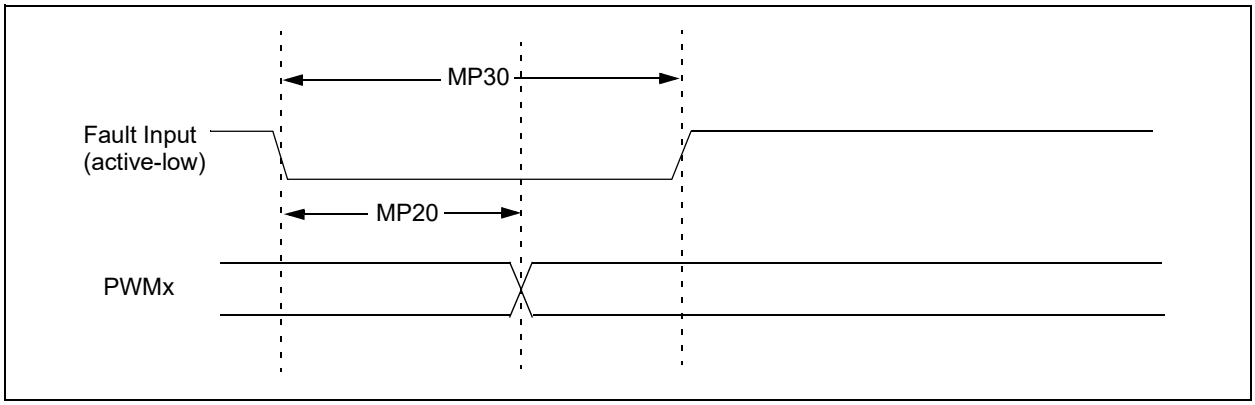

TABLE 36-49: MOTOR CONTROL PWM MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MP10	TFPWM	PWM Output Fall Time	—	—	—	ns	See parameter DO32
MP11	TRPWM	PWM Output Rise Time	—	—	—	ns	See parameter DO31
MP20	TFD	Fault Input ↓ to PWM I/O Change	—	—	50	ns	—
MP30	TFH	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 36-21: EJTAG TIMING CHARACTERISTICS

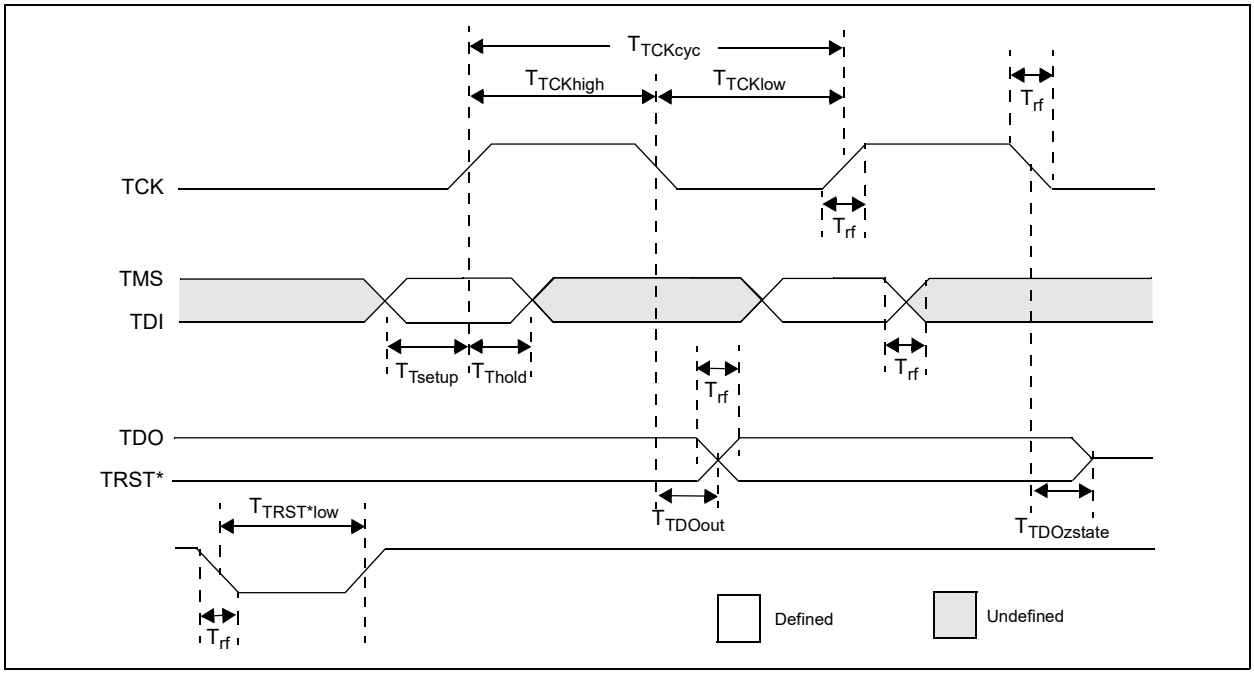

TABLE 36-50: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Description(1)**	**Min.**	**Max.**	**Units**	**Conditions**
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

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37.0 AC AND DC CHARACTERISTICS GRAPHS

Note: The graphs provided are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 37-1: VOH – 4x DRIVER PINS

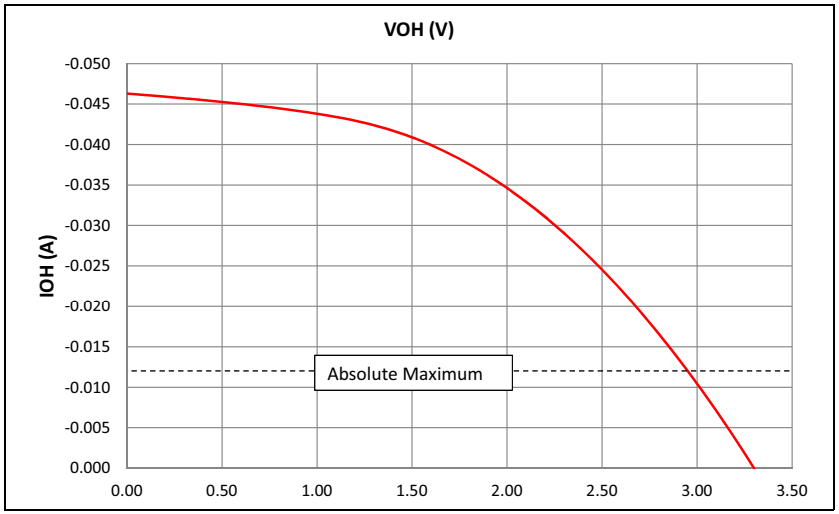


FIGURE 37-2: VOL – 4x DRIVER PINS

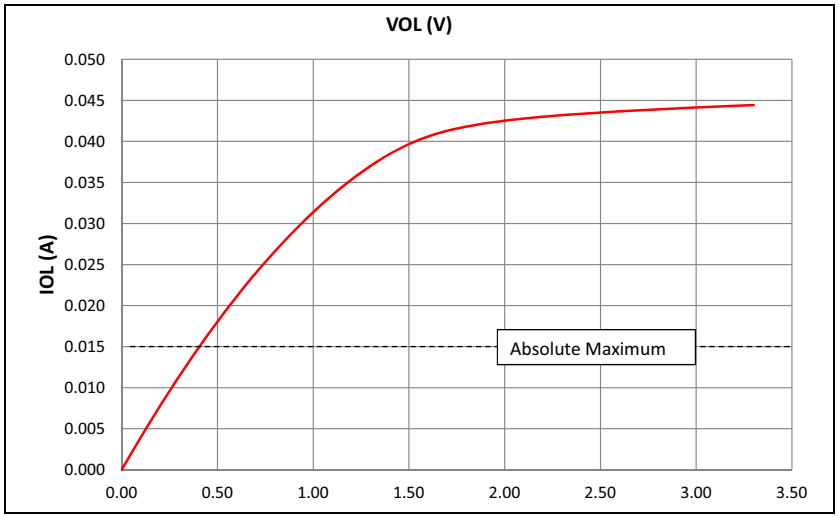


FIGURE 37-3: VOH – 8x DRIVER PINS

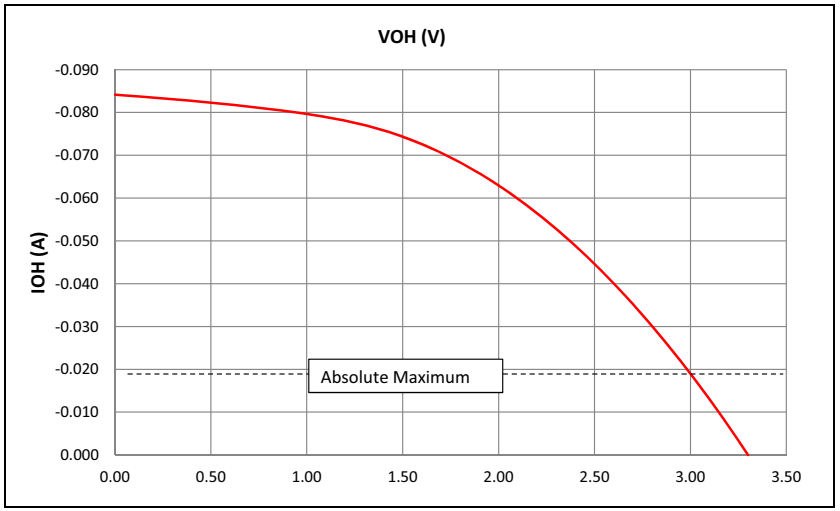
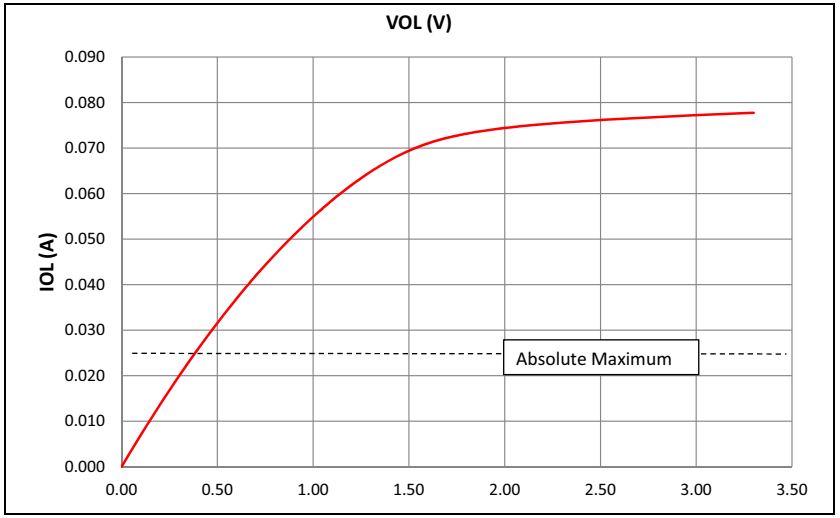


FIGURE 37-4: VOL – 8x DRIVER PINS



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NOTES:

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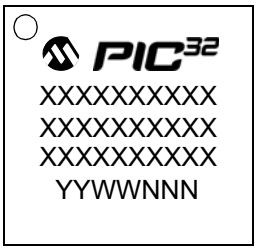
38.0 PACKAGING INFORMATION

38.1 Package Marking Information

64-Lead QFN (9x9x0.9 mm)



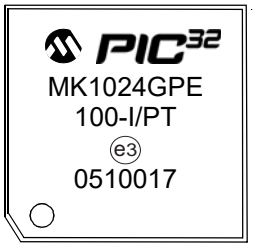
Example

64-Lead TQFP (10x10x1 mm)

Example

100-Lead TQFP (12x12x1 mm)

Example



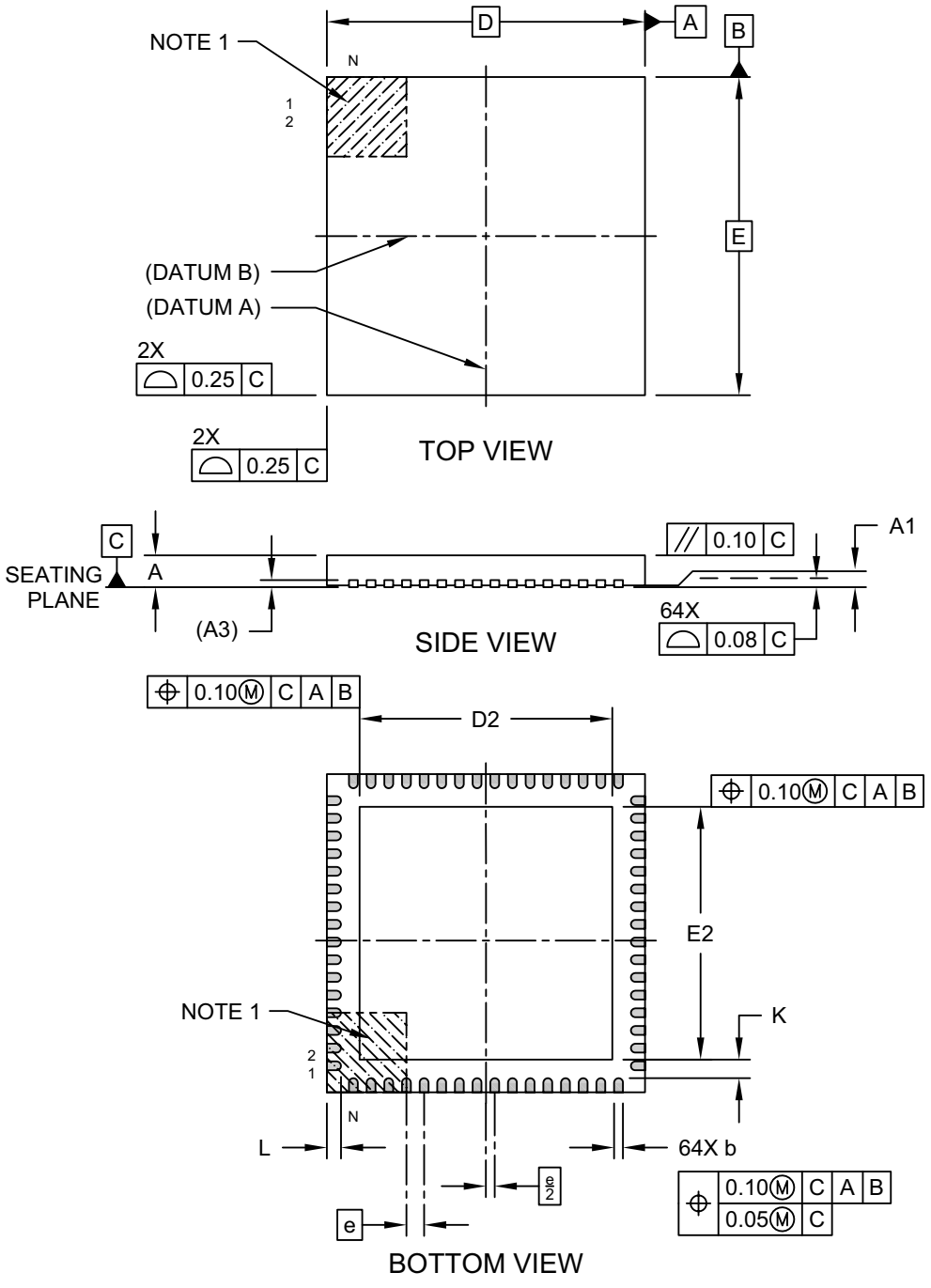
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

38.2 Package Details

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149 [R4X] Rev E Sheet 1 of 2

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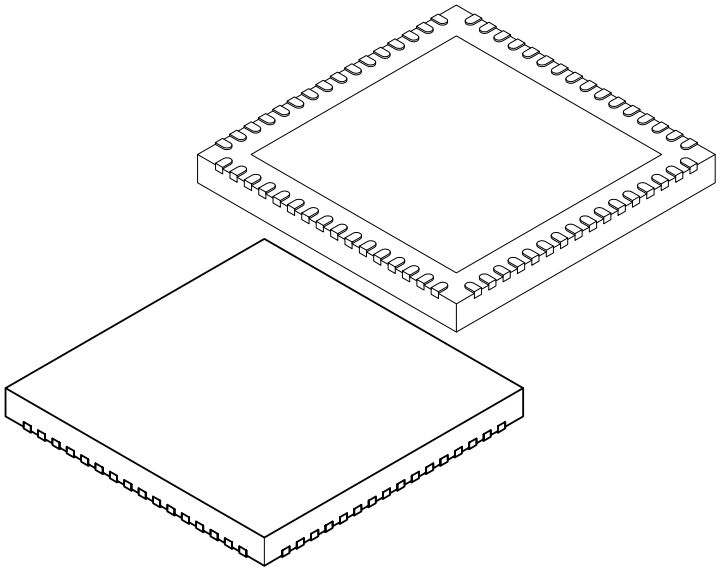
64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.25
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.25
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

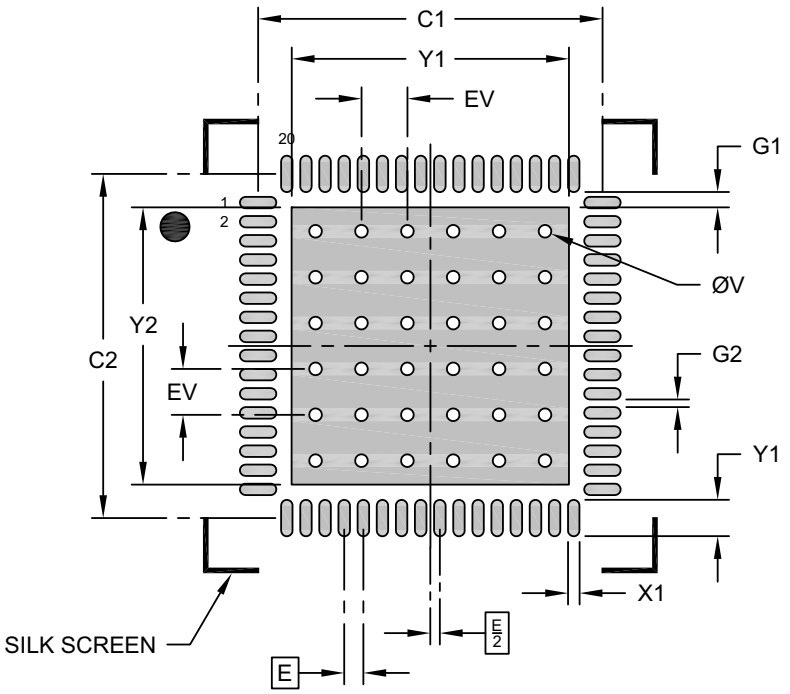
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149 [R4X] Rev E Sheet 2 of 2

64-Lead Very Thin Plastic Quad Flat, No Lead Package (R4X) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			7.25
Optional Center Pad Length	Y2			7.25
Contact Pad Spacing	C1		9.00	
Contact Pad Spacing	C2		9.00	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.95
Contact Pad to Center Pad (X64)	G1	0.40		
Spacing Between Contact Pads (X60)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-149 [R4X] Rev E

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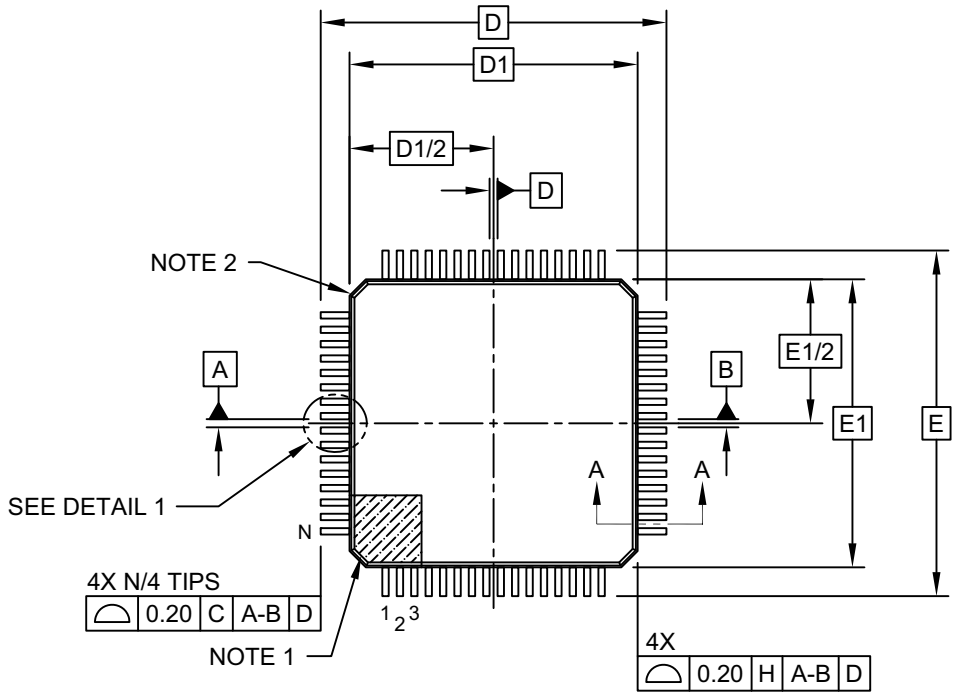
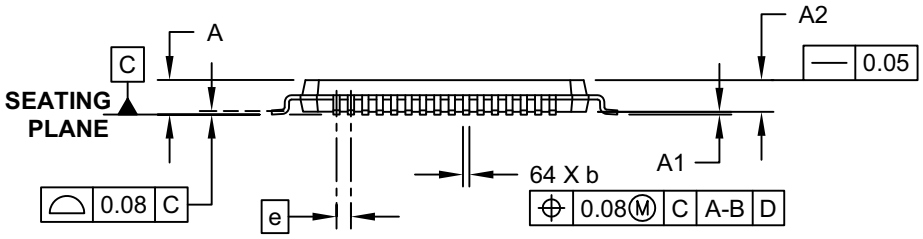
64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

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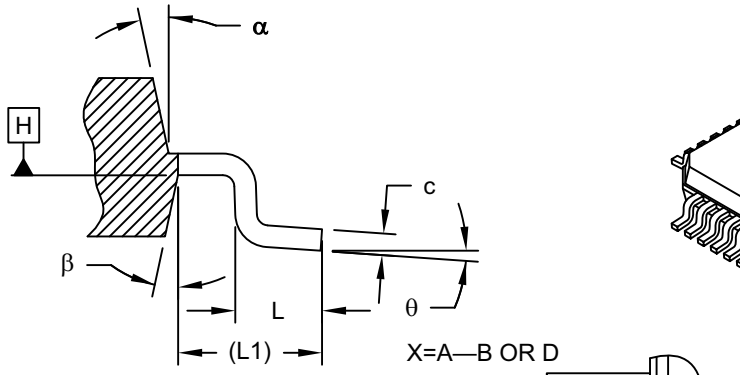
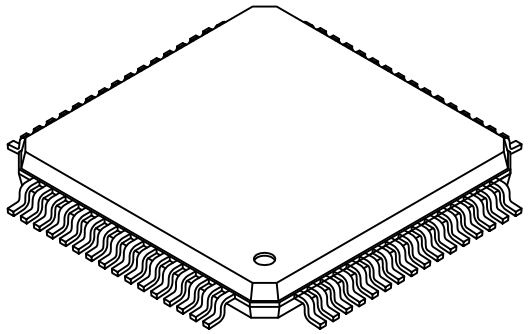
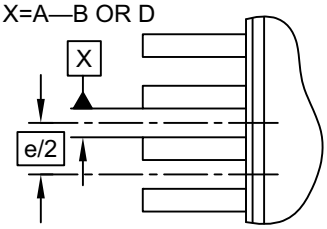
64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A





DETAIL 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

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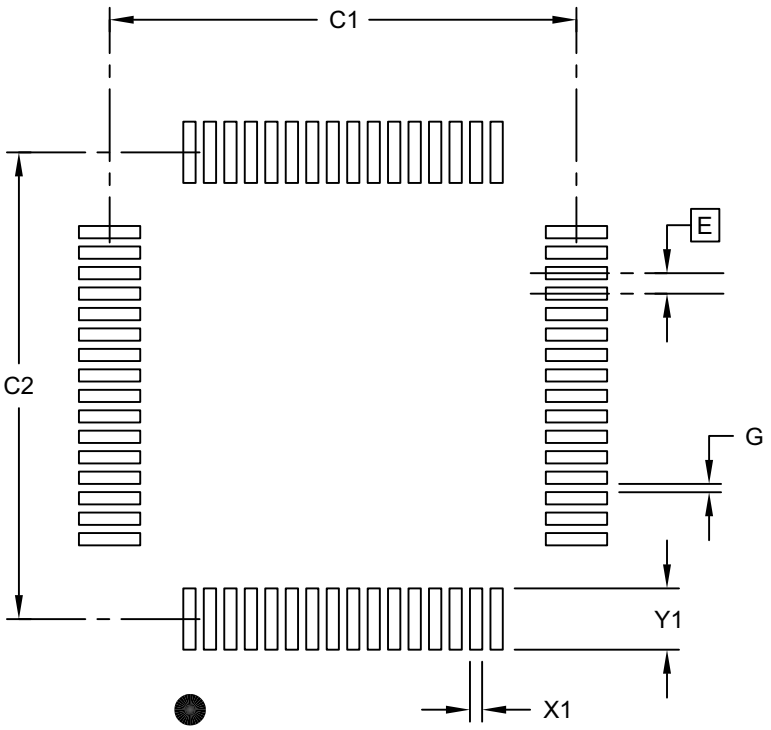
64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

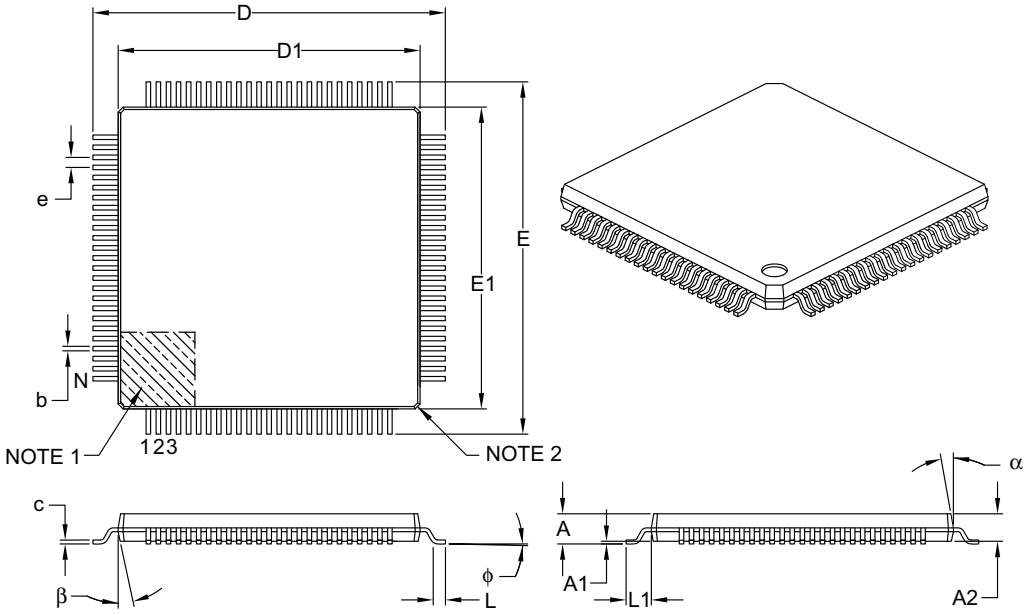
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.40 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.13	0.18	0.23
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

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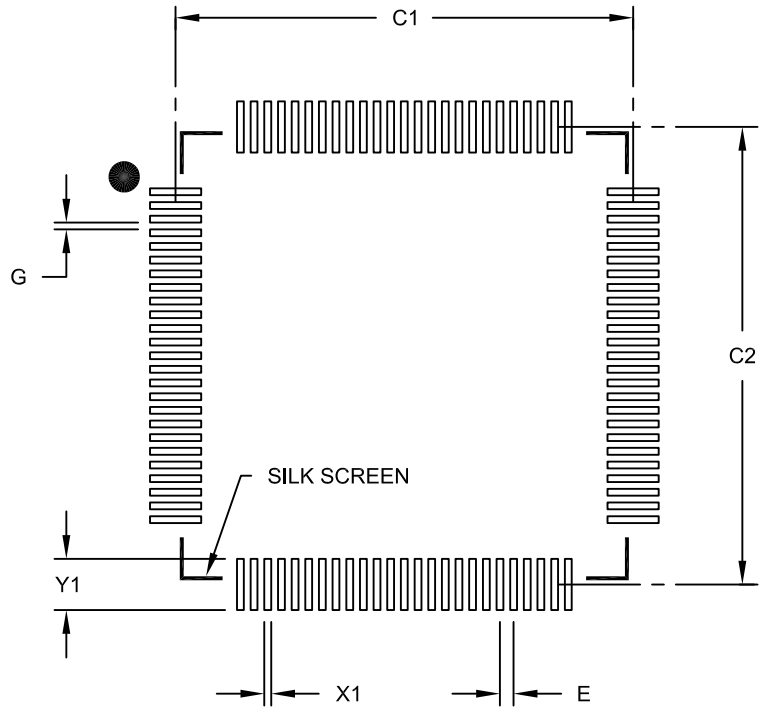
100-Lead Plastic Thin Quad Flatpack (PT)- 12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

NOTES:

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39.0 APPENDIX A: MIGRATION GUIDE

TABLE 39-1: MIGRATION FROM PIC32MKXXGPD/GPE/MCFXX TO PIC32MKXXGPK/GPL/MCMXX

FEATURE	PIC32MKxxGPD/GPE/ MCFxx	PIC32MKxxGPK/GPL/ MCMxx	64/100 pin PIC32MKxxGPD/E/ MCF to 64/100 pin PIC32MKxxGPK/L/ MCM Migration Impact		COMMENTS
			PCB Hardware Non-Compatible	Software Non-Compatible	
#PIN	100/64	100/64	X	X	Pin Differences: LVDIN, T1CLK, VBAT, RD8, PWM7L, PWM7H, PWM8L, PWM8H, PWM9L, PWM9H, PWM10H I2Cx [SCLx, SDAx (x=1-4)] differences. + GP variants have one extra I/O pin.
# I/O	77 (100-pin), 48 (64-pin)	78 (100-pin), 49 (64-pin)	X	X	
CPU	MIPS arch at 120 MHz	MIPS arch at 120 MHz	—	—	—
Configuration Word Registers	4	5/10	—	X	1 new configuration register + new bits + 5 new alternate configuration words.
Flash	1024 Mb/512 Mb No ECC Live Update Dual boot	1024 Mb /512 Mb ECC Live update Dual boot	—	X(1)	Flash ECC added on PIC32MKxxGPK/GPL/ MCMxx. (i.e., Silicon Flash error correction)
SRAM	256 Kb, 128 Kb	256 Kb, 128 Kb	—	—	—
Oscillator	POSC (No AGC) SOSC UPLL (USB PLL) No BFRC	POSC w/AGC and Fine gain SOSC UPLL (USB PLL) BFRC (Back-up FRC)	X(1,2)	X(1,2)	PIC32MKxxGPK/GPL/MCMxx: New BFRC (Back-Up FRC) + OSCCON register clock source selections + AGC (Auto Gain Control) feature/selections in Configuration words.
EE Data Flash Module	4 Kb	4 Kb	—	—	—
DMA	8/13	8/13	—	—	—
USB	(2) Full Speed (100-pin) (1) Full Speed (64 -in)	(2) Full Speed (100-pin) (1) Full Speed (64-pin)	—	—	Note: USB LS non-functional on both product families.
Timer1	1	1	—	—	—
32-bit Timer 2-9 type-B	8	8	—	—	—
Watch Dog Timer (WDT)	1	1	—	—	—

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TABLE 39-1: MIGRATION FROM PIC32MKXXGPD/GPE/MCFXX TO PIC32MKXXGPK/GPL/MCMXX (CONTINUED)

Dead Man Timer (DMT)	1	1	—	—	—
Input Capture	16	16	—	—	—
Output Compare	16	16	—	—	—
SPI	6	6	—	—	—
I^2C	(None)	4	X	X	(4) I^2C peripherals
UART	6	6	—	—	—
PMP	1	1	—	—	—
RTCC	1	1	—	—	—
CAN	CAN (Lite)	CAN FD (New hardware or Software)	—	X	New CAN architecture with all new features register/bit definitions
ADC Modules	7	7	—	—	—
ADC Channels (External)	42 (100 pin), 26 (64 pin)	42 (100-pin), 26 (64-pin)	—	—	—
ADC Channels (V_{BAT} Internal)	Yes (AN52 = $V_{BAT}/2$)	No	—	X(1)	No V_{BAT} on PIC32MKxxGPK/GPLxx
Op amp	4	4 (New features and configurations)	—	X	New op amp features, modes, configurations and register bit additions or deletions + new performance specs.
CFGCON2 Register	Yes	No	—	X	PIC32MKxxGPD/GPE/MCFxx Op-Amp Enable/ Disable register.
COMPARATORS	5	5 (New features and configurations)	—	X	
DAC	3	3	—	—	

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TABLE 39-2: MIGRATION FROM PIC32MKXXGPD/GPE/MCFXX TO PIC32MKXXGPK/GPL/MCMXX

FEATURE	PIC32MKxxGPD/GPE/ MCFxx	PIC32MKxxGPK/GPL/ MCMxx	64/100pin PIC32MKxxGPD/E/ MCF to 64/100pin PIC32MKxxGPK/L/ MCM Migration Impact		COMMENTS
			PCB Hardware Non-Compatible	Software Non-Compatible	
Motor Control PWM (PIC32MKXXMCxXX Only)	8 complimentary pairs (1-6, 11-12)+ 4 single ended (7-10)	12 complimentary pairs + (6) single ended	X	X	**PIC32MKxxMCFxx**: Maximum (8) complimentary pairs or (4) Independent pairs or any combination of complimentary/independent that do not exceed (8) pairs. **PIC32MKxxMCMxx**: Maximum (12) complimentary pairs or (6) Independent pairs or any combination of complimentary/independent that do not exceed (12) pairs.
PWM IOCONx: (x=1-12) FLT and DTCOMP	9	11	X(1)	X(1)	PWM Fault and DTCOMP, Different Fault and Dead Time Compensation features or selections
Low-Voltage Detect	No	1	X	X	—
CTMU	1	1	—	—	—
PMD (Peripheral Module Disable)	Yes	Yes	—	—	—
JTAG	Yes	Yes	—	—	—
TRACE	Yes (100-pin & 64-pin)	Yes (100-pin & 64-pin)	—	—	—
PGCx/PGDx (Debug)	3	3	—	—	—
VBAT (GP variants)	Yes	No	X	X	No VBAT on PIC32MKxxGPK/GPLxx
Deep-sleep modes/ features * DSWDT / DSBOR * DSCON Register * DSWAKE Register * DSGPR[0 - 32] Register	Yes	No	---	X	No Deep-sleep modes/features and registers on PIC32MKxxGPK/GPL/MCMxx

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TABLE 39-2: MIGRATION FROM PIC32MKXXGPD/GPE/MCFXX TO PIC32MKXXGPK/GPL/MCMXX (CONTINUED)

PRISS Register: Priority Shadow Select Registers	2	8	—	X	Interrupt Priority Shadow Register sets added to reduce interrupt latency and interrupt stack memory usage by ~7x
PB5DIV Register	Yes	No	—	X	No PB5 Peripheral bus #5 Clk Pre-scalar or
PB6DIV Register Default	SYSCLK/2	SYSCLK/4	—	X	Peripherals on PB6 only runs at 30 MHz. Changes in default Peripheral Bus #5 Clk Pre-scalar
RD8 I/O pin (GP Variants Only)	No	Yes	X	X(1)	PINx: PIC32MKxxGPD/GPExx = VBAT/VDD PINx: PIC32MKxxGPK/GPLxx = RD8
VDD Ramp Rate	300 ms to 3 µs	300 ms to 10 µs	X	—	Maximum VDD ramp rate is reduced from 3 us to 10 us. Some users design may need to add a 3.3v VDD regulator soft start circuit to meet new specification.
CFGCON2 Register	ENPGAx + EEWS (x=1-3, 5)	EEWS bits Only	—	X	PIC32MKxxGPK/GPL/MCMxx Op-Amp Unity Gain mode enabled removed from CFGCON2 Register. (Unity Gain mode moved to CMxCON Register, x=1-3,5)

Note 1: This is affected only if the user application is using any additional modules, peripheral functions, peripheral pin function, or features on the PIC32MKxxGPD/GPExx that the PIC32MKxxGPH/GPGxx does not possess.

2: POSC Legacy code on PIC32MKxxGPD/GPExx will default in silicon on to PIC32MKxxGPK/GPLxx POSC w/AGC and ignore POSC gain setting. If using an external shunt gain resistor across POSC XTAL on PIC32MKxxGPD/GPExx user MUST ensure that DEVCFG0<POSCBOOST>=0 on PIC32MKxxGPH/GPGxx or remove the resistor for proper operation. Either internal or external gain boost but not both.

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TABLE 39-3: (100) PIN PIC32MKXXMCF100 VERSUS PIC32MKXXMCM100 PIN/FUNCTION MIGRATION DIFFERENCES

PIN	PIC32MKxxMCF100		PIC32MKxxMCM100	FUNCTION PIN MISMATCH
1	AN23/CVD23/PMA23/RG15		AN23/CVD23/PWM7L/PMA23/RG15	PWM7L
2	VDD		VDD	
3	TCK/RPA7/PWMH10/PWML4/PMD5/RA7		TCK/RPA7/PWM10H/PWM4L/PMD5/RA7	
4	RPB14/PWMH1/VBUSON1/PMD6/RB14		RPB14/PWM1H/VBUSON1/PMD6/RB14	
5	RPB15/PWMH7/PWML1/PMD7/RB15		RPB15/PWM7H/PWM1L/PMD7/RB15	
6	PWMH11/PWML5/RD1		PWM11H/PWM5L/RD1	
7	PWMH5/RD2		PWM5H/RD2	
8	RPD3/PWMH12/PWML6/RD3		RPD3/PWM12H/PWM6L/RD3	
9	RPD4/PWMH6/RD4		RPD4/PWM6H/RD4	
10	AN19/CVD19/RPG6/VBUSON2/PMA5/RG6		AN19/CVD19/RPG6/PWM10L/VBUSON2/ PMA5/RG6	
11	AN18/CVD18/RPG7/PMA4/RG7		AN18/CVD18/RPG7/PWM10H/SCL1/PMA4/RG7	SCL1, PWM10H
12	AN17/CVD17/RPG8/PMA3/RG8		AN17/CVD17/RPG8/SDA1/PMA3/RG8	SDA1
13	MCLR#		MCLR#	
14	AN16/CVD16/RPG9/PMA2/RG9		AN16/CVD16/RPG9/PMA2/RG9	
15	VSS		VSS	
16	VDD		VDD	
17	AN22/CVD22/RG10		AN22/CVD22/RG10	
18	AN21/CVD21/RE8		AN21/CVD21/RE8	
19	AN20/CVD20/RE9		AN20/CVD20/RE9	
20	AN10/CVD10/RPA12/RA12		AN10/CVD10/RPA12/RA12	
21	AN9/CVD9/RPA11/RA11		AN9/CVD9/RPA11/RA11	
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0		OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	
23	OA2IN+/AN1/C2IN1+/RPA1/RA1		OA2IN+/AN1/C2IN1+/RPA1/RA1	
24	PGD3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0		PGD3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	
25	PGC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/ CTED1/RB1		PGC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/ CTED1/RB1	
26	PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/ RPB2/RB2		PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/ RPB2/RB2	
27	PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/ RPB3/RB3		PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/ RPB3/RB3	
28	VREF-/AN33/CVD33/PMA7/RF9		VREF-/AN33/CVD33/PMA7/RF9	
29	VREF+/AN34/CVD34/PMA6/RF10		VREF+/AN34/CVD34/PMA6/RF10	

TABLE 39-3: (100) PIN PIC32MKXXMCF100 VERSUS PIC32MKXXMCM100 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

30	AVDD		AVDD	
31	AVSS		AVSS	
32	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0		OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	
33	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/RC1		OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/RC1	
34	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMA13/RC2		OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMA13/RC2	
35	AN11/CVD11/C1IN2-/FLT4/PMA12/RC11		AN11/CVD11/C1IN2-/FLT4/PMA12/RC11	
36	VSS		VSS	
37	VDD		VDD	
38	AN35/CVD35/RG11		AN35/CVD35/RG11	
39	AN36/CVD36/RF13		AN36/CVD36/RF13	
40	AN37/CVD37/RF12		AN37/CVD37/RF12	
41	AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMA11/RE12		AN12/CVD12/C2IN2-/C5IN2-/SDA4/FLT5/PMA11/RE12	SDA4
42	AN13/CVD13/C3IN2-/FLT6/PMA10/RE13		AN13/CVD13/C3IN2-/SCL4/FLT6/PMA10/RE13	SCL4
43	AN14/CVD14/RPE14/FLT7/PMA1/RE14		AN14/CVD14/RPE14/FLT7/PMA1/RE14	
44	AN15/CVD15/RPE15/FLT8/PMA0/RE15		AN15/CVD15/RPE15/FLT8/PMA0/RE15	
45	VSS		VSS	
46	VDD		VDD	
47	AN38/CVD38/RD14		AN38/CVD38/RD14	
48	AN39/CVD39/RD15		AN39/CVD39/RD15	
49	TDI/DAC3/AN26/CVD26/RPA8/PMA9/RA8		TDI/DAC3/AN26/CVD26/RPA8/SDA2/PMA9/RA8	SDA2
50	FLT15/RPB4/PMA8/RB4		FLT15/RPB4/SCL2/PMA8/RB4	SCL2
51	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/RA4		OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/RA4	T1CLK
52	AN40/CVD40/RPE0/RE0		AN40/CVD40/RPE0/RE0	
53	AN41/CVD41/RPE1/RE1		AN41/CVD41/RPE1/RE1	
54	VBUS1		VBUS1	
55	VUSB3V3		VUSB3V3	
56	D1-		D1-	
57	D1+		D1+	
58	VBUS2		VBUS2	
59	D2-		D2-	
60	D2+		D2+	
61	AN45/CVD45/RF5		AN45/CVD45/RF5	

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TABLE 39-3: (100) PIN PIC32MKXXMCF100 VERSUS PIC32MKXXMCM100 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

62	VDD		VDD	
63	OSCI/CLKI/AN49/CVD49/RPC12/RC12		OSCI/CLKI/AN49/CVD49/RPC12/RC12	
64	OSCO/CLKO/RPC15/RC15		OSCO/CLKO/RPC15/RC15	
65	VSS		VSS	
66	AN46/CVD46/RPA14/RA14		AN46/CVD46/RPA14/RA14	
67	AN47/CVD47/RPA15/RA15		AN47/CVD47/RPA15/RA15	
68	RD8		RD8	
69	PGD2/RPB5/USBID1/RB5		PGD2/RPB5/SDA3/USBID1/RB5	SDA3
70	PGC2/RPB6/SCK2/PMA15/RB6		PGC2/RPB6/SCL3/SCK2/PMA15/RB6	SCL3
71	DAC2/AN48/CVD48/RPC10/PMA14/RC10		DAC2/AN48/CVD48/RPC10/PMA14/RC10	
72	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/ INT0/RB7		OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/ INT0/RB7	
73	SOSCI/RPC13/RC13		SOSCI/RPC13/RC13	
74	SOSCO/RPB8/RB8		SOSCO/RPB8/T1CK/RB8	T1CLK
75	VSS		VSS	
76	TMS/OA5IN-/AN27/CVD27/LVDIN/C5IN1-/ RPB9/RB9		TMS/OA5IN-/AN27/CVD27/LVDIN/C5IN1-/ RPB9/RB9	
77	RPC6/USBID2/PMA16/RC6		RPC6/USBID2/PMA16/RC6	
78	RPC7/PMA17/RC7		RPC7/PMA17/RC7	
79	PMD12/RD12		PMD12/RD12	
80	PMD13/RD13		PMD13/RD13	
81	RPC8/PMWR/RC8		RPC8/PMWR/RC8	
82	RPD5/PWMH12/PMRD/RD5		RPD5/PWM12H/PMRD/RD5	
83	RPD6/PWML12/PMD14/RD6		RPD6/PWM12L/PMD14/RD6	
84	RPC9/PMD15/RC9		RPC9/PMD15/RC9	
85	VSS		VSS	
86	VDD		VDD	
87	RPF0/PWMH11/PMD11/RF0		RPF0/PWM11H/PMD11/RF0	
88	RPF1/PWML11/PMD10/RF1		RPF1/PWM11L/PMD10/RF1	
89	RPG1/PMD9/RG1		RPG1/PMD9/RG1	
90	RPG0/PMD8/RG0		RPG0/PMD8/RG0	
91	TRCLK/PMA18/RF6		TRCLK/PWM9H/PMA18/RF6	PWM9H
92	TRD3/PMA19/RF7		TRD3/PWM9L/PMA19/RF7	PWM9L
93	RPB10/PWMH3/PMD0/RB10		RPB10/PWM3H/PMD0/RB10	
94	RPB11/PWMH9/PWML3/PMD1/RB11		RPB11/PWM9H/PWM3L/PMD1/RB11	
95	TRD2/PMA20/RG14		TRD2/PWM8H/PMA20/RG14	PWM8H

TABLE 39-3: (100) PIN PIC32MKXXMCF100 VERSUS PIC32MKXXMCM100 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

96	TRD1/RPG12/PMA21/RG12		TRD1/RPG12/PWM8L/PMA21/RG12	PWM8L
97	TRD0/PMA22/RG13		TRD0/PWM7H/PMA22/RG13	PWM7H
98	RPB12/PWMH2/PMD2/RB12		RPB12/PWM2H/PMD2/RB12	
99	RPB13/PWMH8/PWML2/CTPLS/PMD3/RB13		RPB13/PWM8H/PWM2L/CTPLS/PMD3/RB13	
100	TDO/PWMH4/PMD4/RA10		TDO/PWM4H/PMD4/RA10	

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TABLE 39-4: (100) PIN PIC32MKXXGPD/E100 VERSUS PIC32MKXXGPK/L100 PIN/FUNCTION MIGRATION DIFFERENCES

PIN	PIC32MKxxGPD/GPE100		PIC32MKxxGPK/GPL100	FUNCTION PIN MISMATCH
1	AN23/CVD23/PMA23/RG15		AN23/CVD23/PMA23/RG15	
2	VDD		VDD	
3	TCK/RPA7/PMD5/RA7		TCK/RPA7/PMD5/RA7	
4	RPB14/VBUSON1/PMD6/RB14		RPB14/VBUSON1/PMD6/RB14	
5	RPB15/PMD7/RB15		RPB15/PMD7/RB15	
6	RD1		RD1	
7	RD2		RD2	
8	RPD3/RD3		RPD3/RD3	
9	RPD4/RD4		RPD4/RD4	
10	AN19/CVD19/RPG6/VBUSON2/PMA5/RG6		AN19/CVD19/RPG6/VBUSON2/PMA5/RG6	
11	AN18/CVD18/RPG7/PMA4/RG7		AN18/CVD18/RPG7/SCL1/PMA4/RG7	SCL1
12	AN17/CVD17/RPG8/PMA3/RG8		AN17/CVD17/RPG8/SDA1/PMA3/RG8	SDA1
13	MCLR#		MCLR#	
14	AN16/CVD16/RPG9/PMA2/RG9		AN16/CVD16/RPG9/PMA2/RG9	
15	VSS		VSS	
16	VDD		VDD	
17	AN22/CVD22/RG10		AN22/CVD22/RG10	
18	AN21/CVD21/RE8		AN21/CVD21/RE8	
19	AN20/CVD20/RE9		AN20/CVD20/RE9	
20	AN10/CVD10/RPA12/RA12		AN10/CVD10/RPA12/RA12	
21	AN9/CVD9/RPA11/RA11		AN9/CVD9/RPA11/RA11	
22	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0		OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	
23	OA2IN+/AN1/C2IN1+/RPA1/RA1		OA2IN+/AN1/C2IN1+/RPA1/RA1	
24	PGD3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0		PGD3/OA2IN-/AN2/C2IN1-/RPB0/CTED2/RB0	
25	PGC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1		PGC3/OA1OUT/AN3/C1IN4-/C4IN2-/RPB1/CTED1/RB1	
26	PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2		PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/RPB2/RB2	
27	PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3		PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/RPB3/RB3	
28	VREF-/AN33/CVD33/PMA7/RF9		VREF-/AN33/CVD33/PMA7/RF9	
29	VREF+/AN34/CVD34/PMA6/RF10		VREF+/AN34/CVD34/PMA6/RF10	
30	AVDD		AVDD	

TABLE 39-4: (100) PIN PIC32MKXXGPD/E100 VERSUS PIC32MKXXGPK/L100 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

31	AVSS		AVSS	
32	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0		OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/RPC0/RC0	
33	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/RC1		OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/RC1	
34	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMA13/RC2		OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/PMA13/RC2	
35	AN11/CVD11/C1IN2-/FLT4/PMA12/RC11		AN11/CVD11/C1IN2-/FLT4/PMA12/RC11	
36	VSS		VSS	
37	VDD		VDD	
38	AN35/CVD35/RG11		AN35/CVD35/RG11	
39	AN36/CVD36/RF13		AN36/CVD36/RF13	
40	AN37/CVD37/RF12		AN37/CVD37/RF12	
41	AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMA11/RE12		AN12/CVD12/C2IN2-/C5IN2-/SDA4/FLT5/PMA11/RE12	SDA4
42	AN13/CVD13/C3IN2-/FLT6/PMA10/RE13		AN13/CVD13/C3IN2-/SCL4/FLT6/PMA10/RE13	SCL4
43	AN14/CVD14/RPE14/FLT7/PMA1/RE14		AN14/CVD14/RPE14/FLT7/PMA1/RE14	
44	AN15/CVD15/RPE15/FLT8/PMA0/RE15		AN15/CVD15/RPE15/FLT8/PMA0/RE15	
45	VSS		VSS	
46	VDD		VDD	
47	AN38/CVD38/RD14		AN38/CVD38/RD14	
48	AN39/CVD39/RD15		AN39/CVD39/RD15	
49	TDI/DAC3/AN26/CVD26/RPA8/PMA9/RA8		TDI/DAC3/AN26/CVD26/RPA8/SDA2/PMA9/RA8	SDA2
50	FLT15/RPB4/PMA8/RB4		FLT15/RPB4/SCL2/PMA8/RB4	SCL2
51	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/T1CK/RA4		OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/RPA4/RA4	T1CLK
52	AN40/CVD40/RPE0/RE0		AN40/CVD40/RPE0/RE0	
53	AN41/CVD41/RPE1/RE1		AN41/CVD41/RPE1/RE1	
54	VBUS1		VBUS1	
55	VUSB3V3		VUSB3V3	
56	D1-		D1-	
57	D1+		D1+	
58	VBUS2		VBUS2	
59	D2-		D2-	
60	D2+		D2+	
61	AN45/CVD45/RF5		AN45/CVD45/RF5	
62	VDD		VDD	

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TABLE 39-4: (100) PIN PIC32MKXXGPD/E100 VERSUS PIC32MKXXGPK/L100 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

63	OSCI/CLKI/AN49/CVD49/RPC12/RC12		OSCI/CLKI/AN49/CVD49/RPC12/RC12	
64	OSCO/CLKO/RPC15/RC15		OSCO/CLKO/RPC15/RC15	
65	VSS		VSS	
66	AN46/CVD46/RPA14/RA14		AN46/CVD46/RPA14/RA14	
67	AN47/CVD47/RPA15/RA15		AN47/CVD47/RPA15/RA15	
68	VBAT / VDD (i.e. Non-5v Tolerant)		RD8 (i.e. 5v Tolerant)	VBAT/VDD, RD8
69	PGD2/RPB5/USBID1/RB5		PGD2/RPB5/SDA3/USBID1/RB5	SDA3
70	PGC2/RPB6/SCK2/PMA15/RB6		PGC2/RPB6/SCL3/SCK2/PMA15/RB6	SCL3
71	DAC2/AN48/CVD48/RPC10/PMA14/RC10		DAC2/AN48/CVD48/RPC10/PMA14/RC10	
72	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/ INT0/RB7		OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/ INT0/RB7	
73	SOSCI/RPC13/RC13		SOSCI/RPC13/RC13	
74	SOSCO/RPB8/RB8		SOSCO/RPB8/T1CK/RB8	T1CLK
75	VSS		VSS	
76	TMS/OA5IN-/AN27/CVD27/LVDIN/C5IN1-/ RPB9/RB9		TMS/OA5IN-/AN27/CVD27/LVDIN/C5IN1-/ RPB9/RB9	
77	RPC6/USBID2/PMA16/RC6		RPC6/USBID2/PMA16/RC6	
78	RPC7/PMA17/RC7		RPC7/PMA17/RC7	
79	PMD12/RD12		PMD12/RD12	
80	PMD13/RD13		PMD13/RD13	
81	RPC8/PMWR/RC8		RPC8/PMWR/RC8	
82	RPD5/PMRD/RD5		RPD5/PMRD/RD5	
83	RPD6/PMD14/RD6		RPD6/PMD14/RD6	
84	RPC9/PMD15/RC9		RPC9/PMD15/RC9	
85	VSS		VSS	
86	VDD		VDD	
87	RPF0/PMD11/RF0		RPF0/PMD11/RF0	
88	RPF1/PMD10/RF1		RPF1/PMD10/RF1	
89	RPG1/PMD9/RG1		RPG1/PMD9/RG1	
90	RPG0/PMD8/RG0		RPG0/PMD8/RG0	
91	TRCLK/PMA18/RF6		TRCLK/PMA18/RF6	
92	TRD3/PMA19/RF7		TRD3/PMA19/RF7	
93	RPB10/PMD0/RB10		RPB10/PMD0/RB10	
94	RPB11/PMD1/RB11		RPB11/PMD1/RB11	
95	TRD2/PMA20/RG14		TRD2/PMA20/RG14	
96	TRD1/RPG12/PMA21/RG12		TRD1/RPG12/PMA21/RG12	

TABLE 39-4: (100) PIN PIC32MKXXGPD/E100 VERSUS PIC32MKXXGPK/L100 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

97	TRD0/PMA22/RG13		TRD0/PMA22/RG13	
98	RPB12/PMD2/RB12		RPB12/PMD2/RB12	
99	RPB13/CTPLS/PMD3/RB13		RPB13/CTPLS/PMD3/RB13	
100	TDO/PMD4/RA10		TDO/PMD4/RA10	

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TABLE 39-5: (64) PIN PIC32MKXXMCF64 VERSUS PIC32MKXXMCM64 PIN/FUNCTION MIGRATION DIFFERENCES

PIN	PIC32MKxxMCF64		PIC32MKxxMCM64	FUNCTION PIN MISMATCH
1	TCK/RPA7/PWM10H/PWM4L/PMD5/RA7		TCK/RPA7/PWM10H/PWM4L/PMD5/RA7	
2	RPB14/PWM1H/VBUSON1/PMD6/RB14		RPB14/PWM1H/VBUSON1/PMD6/RB14	
3	RPB15/PWM7H/PWM1L/PMD7/RB15		RPB15/PWM7H/PWM1L/PMD7/RB15	
4	AN19/CVD19/RPG6/PMA5/RG6		AN19/CVD19/RPG6/PWM10L/PMA5/RG6	PWM10L
5	AN18/CVD18/RPG7/PMA4/RG7(6)		AN18/CVD18/RPG7/PWM10H/SCL1/PMA4/RG7	PWM10H, SCL1
6	AN17/CVD17/RPG8/PMA3/RG8(7)		AN17/CVD17/RPG8/SDA1/PMA3/RG8	SDA1
7	MCLR#		MCLR#	
8	AN16/CVD16/RPG9/PMA2/RG9		AN16/CVD16/RPG9/PMA2/RG9	
9	VSS		VSS	
10	VDD		VDD	
11	AN10/CVD10/RPA12/RA12		AN10/CVD10/RPA12/RA12	
12	AN9/CVD9/RPA11/USBOEN1/RA11		AN9/CVD9/RPA11/USBOEN1/RA11	
13	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0		OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	
14	OA2IN+/AN1/C2IN1+/RPA1/RA1		OA2IN+/AN1/C2IN1+/RPA1/RA1	
15	PGD3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/ CTED2/RB0		PGD3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/ CTED2/RB0	
16	PGC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/ RPB1/CTED1/PMA6/RB1		PGC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/ RPB1/CTED1/PMA6/RB1	
17	PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/ RPB2/RB2		PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/ RPB2/RB2	
18	PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/ RPB3/RB3		PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/ RPB3/RB3	
19	AVDD		AVDD	
20	AVSS		AVSS	
21	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/ RPC0/RC0		OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/ RPC0/RC0	
22	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/ PMA7/RC1		OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/PMA7/ RC1	
23	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/ FLT3/PMA13/RC2		OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/FLT3/ PMA13/RC2	
24	AN11/CVD11/C1IN2-/FLT4/PMA12/RC11		AN11/CVD11/C1IN2-/FLT4/PMA12/RC11	
25	VSS		VSS	
26	VDD		VDD	
27	AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMA11/ RE12(7)		AN12/CVD12/C2IN2-/C5IN2-/SDA4/FLT5/ PMA11/RE12	SDA4
28	AN13/CVD13/C3IN2-/FLT6/PMA10/RE13(6)		AN13/CVD13/C3IN2-/FLT6/SCL4/PMA10/RE13	SCL4

TABLE 39-5: (64) PIN PIC32MKXXMCF64 VERSUS PIC32MKXXMCM64 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

29	AN14/CVD14/RPE14/FLT7/PMA1/RE14		AN14/CVD14/RPE14/FLT7/PMA1/RE14	
30	AN15/CVD15/RPE15/FLT8/PMA0/RE15		AN15/CVD15/RPE15/FLT8/PMA0/RE15	
31	TDI/DAC3/AN26/CVD26/RPA8/PMA9/RA8(7)		TDI/DAC3/AN26/CVD26/RPA8/SDA2/PMA9/RA8	SDA2
32	FLT15/RPB4/PMA8/RB4(6)		FLT15/RPB4/SCL2/PMA8/RB4	SCL2
33	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/ RPA4/T1CK/RA4		OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/ RPA4/RA4	T1CLK
34	VBUS		VBUS	
35	VUSB3V3		VUSB3V3	
36	D-		D-	
37	D+		D+	
38	VDD		VDD	
39	OSCI/CLKI/AN49/CVD49/RPC12/RC12		OSCI/CLKI/AN49/CVD49/RPC12/RC12	
40	OSCO/CLKO/RPC15/RC15		OSCO/CLKO/RPC15/RC15	
41	VSS		VSS	
42	RD8		RD8	
43	PGED2/RPB5/USBID1/RB5		PGD2/RPB5/SDA3/USBID1/RB5	SDA3
44	PGEC2/RPB6/SCK2/PMA15/RB6		PGC2/RPB6/SCL3/SCK2/PMA15/RB6	SCL3
45	DAC2/AN48/CVD48/RPC10/PMA14/PMCS/ RC10		DAC2/AN48/CVD48/RPC10/PMA14/PMCS/ RC10	
46	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/ INT0/RB7		OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/ INT0/RB7	
47	SOSCI/RPC13/RC13		SOSCI/RPC13/RC13	
48	SOSCO/RPB8/RB8		SOSCO/T1CK/RPB8/RB8	T1CLK
49	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9		TMS/OA5IN-/AN27/CVD27/LVDIN/C5IN1-/RPB9/ RB9	LVDIN
50	TRCLK/RPC6/PWM6H/RC6		TRCLK/RPC6/PWM6H/RC6	
51	TRD0/RPC7/PWM12H/PWM6L/RC7		TRD0/RPC7/PWM12H/PWM6L/RC7	
52	TRD1/RPC8/PWM5H/PMWR/RC8		TRD1/RPC8/PWM5H/PMWR/RC8	
53	TRD2/RPD5/PWM12H/PMRD/RD5		TRD2/RPD5/PWM12H/PMRD/RD5	
54	TRD3/RPD6/PWM12L/RD6		TRD3/RPD6/PWM12L/RD6	
55	RPC9/PWM11H/PWM5L/RC9		RPC9/PWM11H/PWM5L/RC9	
56	VSS		VSS	
57	VDD		VDD	
58	RPF0/PWM11H/RF0		RPF0/PWM11H/RF0	
59	RPF1/PWM11L/RF1		RPF1/PWM11L/RF1	
60	RPB10/PWM3H/PMD0/RB10		RPB10/PWM3H/PMD0/RB10	
61	RPB11/PWM9H/PWM3L/PMD1/RB11		RPB11/PWM9H/PWM3L/PMD1/RB11	

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TABLE 39-5: (64) PIN PIC32MKXXMCF64 VERSUS PIC32MKXXMCM64 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

62	RPB12/PWM2H/PMD2/RB12		RPB12/PWM2H/PMD2/RB12	
63	RPB13/PWM8H/PWM2L/CTPLS/PMD3/RB13		RPB13/PWM8H/PWM2L/CTPLS/PMD3/RB13	
64	TDO/PWM4H/PMD4/RA10		TDO/PWM4H/PMD4/RA10	

TABLE 39-6: (64) PIN PIC32MKXXGPD/E64 VERSUS PIC32MKXXGPK/L64 PIN/FUNCTION MIGRATION DIFFERENCES

PIN	PIC32MKxxGPD/E64		PIC32MKxxGPK/L64	FUNCTION PIN MISMATCH
1	TCK/RPA7/PMD5/RA7		TCK/RPA7/PMD5/RA7	
2	RPB14/VBUSON1/PMD6/RB14		RPB14/VBUSON1/PMD6/RB14	
3	RPB15/PMD7/RB15		RPB15/PMD7/RB15	
4	AN19/CVD19/RPG6/PMA5/RG6		AN19/CVD19/RPG6/PMA5/RG6	
5	AN18/CVD18/RPG7/PMA4/RG7(6)		AN18/CVD18/RPG7/SCL1/PMA4/RG7	SCL1
6	AN17/CVD17/RPG8/PMA3/RG8(7)		AN17/CVD17/RPG8/SDA1/PMA3/RG8	SDA1
7	MCLR#		MCLR#	
8	AN16/CVD16/RPG9/PMA2/RG9		AN16/CVD16/RPG9/PMA2/RG9	
9	VSS		VSS	
10	VDD		VDD	
11	AN10/CVD10/RPA12/RA12		AN10/CVD10/RPA12/RA12	
12	AN9/CVD9/RPA11/USBOEN1/RA11		AN9/CVD9/RPA11/USBOEN1/RA11	
13	OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0		OA2OUT/AN0/C2IN4-/C4IN3-/RPA0/RA0	
14	OA2IN+/AN1/C2IN1+/RPA1/RA1		OA2IN+/AN1/C2IN1+/RPA1/RA1	
15	PGD3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/ CTED2/RB0		PGD3/VREF-/OA2IN-/AN2/C2IN1-/RPB0/ CTED2/RB0	
16	PGC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/ RPB1/CTED1/PMA6/RB1		PGC3/OA1OUT/VREF+/AN3/C1IN4-/C4IN2-/ RPB1/CTED1/PMA6/RB1	
17	PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/ RPB2/RB2		PGC1/OA1IN+/AN4/C1IN1+/C1IN3-/C2IN3-/ RPB2/RB2	
18	PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/ RPB3/RB3		PGD1/OA1IN-/AN5/CTCMP/C1IN1-/RTCC/ RPB3/RB3	
19	AVDD		AVDD	
20	AVSS		AVSS	
21	OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/ RPC0/RC0		OA3OUT/AN6/CVD6/C3IN4-/C4IN1+/C4IN4-/ RPC0/RC0	
22	OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/ PMA7/RC1		OA3IN-/AN7/CVD7/C3IN1-/C4IN1-/RPC1/PMA7/ RC1	
23	OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/ FLT3/PMA13/RC2		OA3IN+/AN8/CVD8/C3IN1+/C3IN3-/RPC2/ FLT3/PMA13/RC2	
24	AN11/CVD11/C1IN2-/FLT4/PMA12/RC11		AN11/CVD11/C1IN2-/FLT4/PMA12/RC11	
25	VSS		VSS	
26	VDD		VDD	
27	AN12/CVD12/C2IN2-/C5IN2-/FLT5/PMA11/ RE12(7)		AN12/CVD12/C2IN2-/C5IN2-/SDA4/FLT5/ PMA11/RE12	SDA4
28	AN13/CVD13/C3IN2-/FLT6/PMA10/RE13(6)		AN13/CVD13/C3IN2-/FLT6/SCL4/PMA10/RE13	SCL4

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TABLE 39-6: (64) PIN PIC32MKXXGPD/E64 VERSUS PIC32MKXXGPK/L64 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

29	AN14/CVD14/RPE14/FLT7/PMA1/RE14		AN14/CVD14/RPE14/FLT7/PMA1/RE14	
30	AN15/CVD15/RPE15/FLT8/PMA0/RE15		AN15/CVD15/RPE15/FLT8/PMA0/RE15	
31	TDI/DAC3/AN26/CVD26/RPA8/PMA9/RA8(7)		TDI/DAC3/AN26/CVD26/RPA8/SDA2/PMA9/ RA8	SDA2
32	FLT15/RPB4/PMA8/RB4(6)		FLT15/RPB4/SCL2/PMA8/RB4	SCL2
33	OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/ RPA4/T1CK/RA4		OA5IN+/DAC1/AN24/CVD24/C5IN1+/C5IN3-/ RPA4/RA4	T1CLK
34	VBUS		VBUS	
35	VUSB3V3		VUSB3V3	
36	D-		D-	
37	D+		D+	
38	VDD		VDD	
39	OSCI/CLKI/AN49/CVD49/RPC12/RC12		OSCI/CLKI/AN49/CVD49/RPC12/RC12	
40	OSCO/CLKO/RPC15/RC15		OSCO/CLKO/RPC15/RC15	
41	VSS		VSS	
42	VBAT, (VDD)		RD8	VBAT, RD8
43	PGED2/RPB5/USBID1/RB5		PGD2/RPB5/SDA3/USBID1/RB5	SDA3
44	PGEC2/RPB6/SCK2/PMA15/RB6		PGC2/RPB6/SCL3/SCK2/PMA15/RB6	SCL3
45	DAC2/AN48/CVD48/RPC10/PMA14/PMCS/ RC10		DAC2/AN48/CVD48/RPC10/PMA14/PMCS/ RC10	
46	OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/ INT0/RB7		OA5OUT/AN25/CVD25/C5IN4-/RPB7/SCK1/ INT0/RB7	
47	SOSCI/RPC13/RC13		SOSCI/RPC13/RC13	
48	SOSCO/RPB8/RB8		SOSCO/T1CK/RPB8/RB8	T1CLK
49	TMS/OA5IN-/AN27/CVD27/C5IN1-/RPB9/RB9		TMS/OA5IN-/AN27/CVD27/LVDIN/C5IN1-/ RPB9/RB9	LVDIN
50	TRCLK/RPC6/RC6		TRCLK/RPC6/RC6	
51	TRD0/RPC7/RC7		TRD0/RPC7/RC7	
52	TRD1/RPC8/PMWR/RC8		TRD1/RPC8/PMWR/RC8	
53	TRD2/RPD5/PMRD/RD5		TRD2/RPD5/PMRD/RD5	
54	TRD3/RPD6/RD6		TRD3/RPD6/RD6	
55	RPC9/RC9		RPC9/RC9	
56	VSS		VSS	
57	VDD		VDD	
58	RPF0/RF0		RPF0/RF0	
59	RPF1/RF1		RPF1/RF1	
60	RPB10/PMD0/RB10		RPB10/PMD0/RB10	

TABLE 39-6: (64) PIN PIC32MKXXGPD/E64 VERSUS PIC32MKXXGPK/L64 PIN/FUNCTION MIGRATION DIFFERENCES (CONTINUED)

61	RPB11/PMD1/RB11		RPB11/PMD1/RB11	
62	RPB12/PMD2/RB12		RPB12/PMD2/RB12	
63	RPB13/CTPLS/PMD3/RB13		RPB13/CTPLS/PMD3/RB13	
64	TDO/PMD4/RA10		TDO/PMD4/RA10	

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40.0 APPENDIX B: REVISION HISTORY

Revision A (April 2016)

This is the initial released version of the document.

Revision B (September 2016)

This revision of the document was updated to include information for PIC32MK Motor Control (MC) devices.

Revision C (December 2016)

This revision includes the following major changes, which are referenced by their respective chapter in Table 40-1.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE 40-1: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB Live-Update Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps	Removed I^2C and HLVD references (see Table 1 and Table 2). Updated pin names to remove references to I^2C and HLVD, added Notes 6 and 7 for 64-pin devices, and Notes 5 and 6 for 100-pin devices (see Table 3, Table 4, Table 5, and Table 6). Removed references to FRM Section 24 and Section 38 (see Referenced Sources).
1.0 "Device Overview"	Removed original Table 1-9. Removed HLVD reference and added a new Note 1 (see Table 1-20).
2.0 "Guidelines for Getting Started with 32-bit MCUs"	**2.1 "Basic Connection Requirements"** - removed bullet point discussing V_{CAP}. In Figure 2-4, reversed direction OSC1 and OSC2 arrows.
6.0 "Data EEPROM"	**6.0 "Data EEPROM"** - updated Note 2. Updated table under Note 2.
7.0 "Resets"	Removed HLVD references (see Table 7-1 and Register 7-3).
8.0 "CPU Exceptions and Interrupt Controller"	Added Note 2 (see Table 8-1). Removed I^2C references (see Table 8-3). Added Note 7 (see Table 8-4).
9.0 "Oscillator Configuration"	Corrected typo to "POSCMOD", added PWM block to connect to SYSCLK (see Figure 9-1). Removed I^2C and HLVD references (see Table 9-1).
21.0 "Inter-Integrated Circuit (I^2C)"	**21.0 "Inter-Integrated Circuit (I^2C)"** - Removed original chapter contents and added an intro that points to MPLAB Harmony, Notes 5 and 6 for 100-pin devices, and Notes 6 and 7 for 64-pin devices.
22.0 "Universal Asynchronous Receiver Transmitter (UART)"	Corrected the label for bit 19-0 (see Register 22-5).
25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	Updated the definition list for bit 20-16 (see Register 25-17). Added Note 1 to Register 25-4.
27.0 "Op Amp/Comparator Module"	Removed I^2C reference (see Figure 27-2). Removed I^2C and HLVD references (see Figure 27-5). Updated CDAC1 to CDAC3, and added Note 3 (see Figure 27-1, Figure 27-2, Figure 27-3, Figure 27-4, and Figure 27-5). Removed CEVT labels from bit 9. Changed bit 9 definition to "unimplemented" (see Table 27-2). Removed CEVT references, changed bit 9 definition to "unimplemented", and added two notes (see Register 27-2).

TABLE 40-1: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
31.0 "Motor Control PWM Module"	Updated first page bulleted list to "Nine Fault input pins are available for Faults and current limits."
	Updated pin table in Figure 31-1; updated **31.1.2 "WRITE-PROTECTED REGISTERS"**
	Updated label TMRx to PTMRx in Figure 31-2.
	Updated "All Resets" value from 0000 to 0078 for IOCONx<31:16> registers in Table 31-1.
	Updated bit 15-0 descriptions in Register 31-6.and Register 31-10
	Updated note in Register 31-10.
	Updated bit 11-10 description in Register 31-11.
	Updated Notes 1 and 4 in Register 31-12.
	Added Note 2 and added Note 2 markers in COMP<13:8> and DTCOMP<7:0> in Register 31-18.
	Updated major features list Table 31-1, Register 31-5, Register 31-13, Register 31-15, Register 31-21, replaced SCLKSEL with SCLKDIV. Register 31-1 through Register 31-9, Register 31-18, Table 36-13, replaced SYSCLK with FSYSCLK and LSB = 1/SYSCLK with Min LSB = 1/FSYSCLK. Register 31-11, replaced PWM Resolution with PWM(min) Resolution. Register 31-16, replaced PWMxL with PWMxH,
32.0 "High/Low Voltage Detect (HLVD)"	Removed this entire section.
32.0 "Power-Saving Features"	Removed I^2C and HLVD references (see Table 32-3).
33.0 "Special Features"	Updated bit 7-0 definition and added appropriate table (see Register 33-9). replaced SYSCLK with FSYSCLK and updated table under note.
36.0 "Electrical Characteristics"	Removed original Figure 37-16, Figure 37-17, Figure 37-18, Figure 37-19, Table 37-6, Table 37-38, and Table 37-39. Removed I^2C references (see Table 36-9). Removed I^2C references (see Table 36-14). Updated Read Access Time and Program Time values (see Table 36-19). Updated typical ENOB value (see Table 36-38). Removed references to "AC CHARACTERISTICS" in table titles, and so on. Table 36-13, replaced SYSCLK with FSYSCLK. Table 36-19, added table under Note 1. Table 36-20, updated CM36 typical value from 30 to 140 mV.
	Updated DI20 Min. V_{DD} value in Table 36-9 and OS13 Max. MHz value in Table 36-15.
	Updated Note 2 equation value from PBCLK2 to PBCLKx in Table 36-16.
	Updated Table 36-28 to include parameters OA14 through OA17.
	Updated Table 36-30 title to "Unity Gain Op amp Timing Requirements".
	Updated Min. ADC Clock Period for parameter AD50 in Table 36-39.
	Updated Max. Sample Throughput Rates for parameter AD51 in Table 36-39.
	Updated Table 36-42 to include parameter CTMU0.

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Revision D (March 2017)

This revision includes the following major changes, which are referenced by their respective chapter in Table 40-2.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE 40-2: MAJOR SECTION UPDATES

Section Name	Update Description
"32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB Live-Update Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps"	page 1 - Updates in **"Power Management" "Motor Control PWM" "Motor Encoder Interface" "Audio/Graphics/Touch Interfaces" "Unique Features" "Advanced Analog Features" "Communication Interfaces" "Qualification and Class B Support"** Removed VBAT column in Table 1. Added Note 8 in Table 3. Added Note 7 in Table 5.
1.0 "Device Overview"	Added Note 1 in Table 1-20.
25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	Added Note 1 to Register 25-4.
31.0 "Motor Control PWM Module"	Updated first page bulleted list to "Nine Fault input pins are available for Faults and current limits." Updated pin table in Figure 31-1. Updated **31.1.2 "WRITE-PROTECTED REGISTERS"** Updated label TMRx to PTMRx in Figure 31-2. Updated "All Resets" value from 0000 to 0078 for IOCONx<31:16> registers in Table 31-1. Updated bit 15-0 descriptions in Register 31-6.and Register 31-10 Updated note in Register 31-10. Updated bit 11-10 description in Register 31-11. Updated Notes 1 and 4 in Register 31-12. Updated Note 1 and added note markers in DTCOMP<13:8> and DTCOMP<7:0> in Register 31-18.
36.0 "Electrical Characteristics"	Updated parameter DI20 Min. VDD value in Table 36-9. Updated parameter OS13 Max. MHz value in Table 36-15. Updated Note 2 equation value from PBCLK2 to PBCLKx in Table 36-16. Updated Table 36-28 to include parameter OA14. Updated Min. ADC Clock Period for parameter AD50 in Table 36-39. Updated Max. Sample Throughput Rates for parameter AD51 in Table 36-39. Updated Table 36-42 to include parameter CTMU0.

Revision F (May 2019)

This revision includes the following major changes, which are referenced by their respective chapter in Table 40-3.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE 40-3: MAJOR SECTION UPDATES

Section Name	Update Description
"32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB Live-Update Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps"	The 120 MHz Operating Conditions were updated. Secure boot was removed from the Security Features. The FRC internal oscillator Clock Management operating conditions were updated. The number of ADC channels for 64-pin TQFP and QFN Motor Control devices was updated (see Table 2).
1.0 “Device Overview”	The I2Cx and PLVD references were removed from the PIC32MK GP/MC Family Block Diagram (see Figure 1-1).
5.0 “Flash Program Memory”	The Wait state bits, LPRDWS<4:0> (NVMCON2), were updated to include a table with low-power Wait state information (see **Register 5-8 NVMCON2: Flash Programming Control Register 2**).
10.0 “Prefetch Module”	The Wait states table in the PFMWS<2:0> bits (CHECON<2:0>) was updated (see **Register 10-1 CHECON: Cache Module Control Register**).
11.0 “Direct Memory Access (DMA) Controller”	A note was added to the CHSIRQ<7:0> bits (DCHxECON<15:8>) (see **Register 11-8 DCHxecon: dma channel x event control register**).
14.0 “Timer1”	The Timer1 Block Diagram was updated (see Figure 14-1).
15.0 “Timer2 Through Timer9”	The Timer2-Timer9 Block Diagram was updated (see Figure 15-1).

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Section Name	Update Description
25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"	The Step 7 was updated (see **25.1 "Activation Sequence"**). **Table 25-1: "PIC32MKXXX Based on a 60 MHz tAD CLOCK (16.667 ns)"** was updated. IVTEMP references were removed from the: • ADC Block Diagram (see Figure 25-1) • S&H Block Diagram (see Figure 25-2) • ADC Register Map (see Table 25-2) The ADCDATA51 register was removed (see Table 25-2). The ADCCON2 register was updated (see **Register 25-12 ADCCSS2: ADC Common Scan Select Register 2**). The following bits were removed: • CSS51 (see Table 25-2 and **Register 25-12 ADCCSS2: ADC Common Scan Select Register 2**) • ARDY51 (see Table 25-2 and **Register 25-14 ADCDSTAT2: ADC Data Ready Status Register 2**) • EIRDY51 (see Table 25-2 and **Register 25-37 ADCEISTAT2: ADC Early Interrupt Status Register 2**) • AN51 (see Table 25-2 and **Register 25-41 ADCSYSCFG1: ADC System Configuration Register 1**) The definition for bit value '110011' in the ADINSEL<5:0> bits in the ADC Control Register 3 was updated to Reserved (see **Register 25-3 ADCCON3: ADC Control Register 3**). A Note was added to the TRGSRC3<4:0> bits in the ADC Trigger Source x Registers (see **Register 25-18 ADCTRG1: ADC Trigger Source 1 Register** through **Register 25-24 ADCTRG7: ADC Trigger Source 7 Register**). The definition for bit value '110101' in the AINID<5:0> bits in the ADC Digital Comparator 1 Control Register 3 was updated to Reserved (see **Register 25-25 ADCCMPCON1: ADC Digital Comparator 1 Control Register**). The definition for the LVL27:LVL0 bits in the ADC Trigger Level/Edge Sensitivity Register was updated (see **Register 25-32 ADCTRGSNS: ADC Trigger Level/Edge Sensitivity Register**).
27.0 "Op Amp/Comparator Module"	The Digital Filter Interconnect Block Diagram was updated (see Figure 27-7). The PSIDL bit was renamed SIDL, and the C5EVT-C1EVT bits were removed in the register summary (see Table 27-2). The bit value '010' definition was updated to from Reserved to PWM Secondary Special Event in the CFSEL<2:0> bits of the Op amp/Comparator 'x' Control Register (see **Register 27-2 CMxcon: op amp/comparator 'x' control register ('x' = 1-5)**).
28.0 "Charge Time Measurement Unit (CTMU)"	The bit value definitions were updated in the IRNG<1:0> bits of the CTMU Control Register and Notes 5 and 6 were added (see **Register 28-1 CTMUCON: CTMU Control Register**).
32.0 "Power-Saving Features"	The All Resets value in the register summary for bits 15:0 of the PMD2 register was changed to '0000' (see Table 32-2).

Section Name	Update Description
36.0 “Electrical Characteristics”	The Maximum value of the Power-Down Current DC Characteristics parameter DC41 was updated (see Table 36-8). The Minimum value of the Internal LPRC Accuracy for parameter F21 was updated (see Table 36-18). The Temperature Sensor Specifications were removed (was Table 36-43). Parameter AD51 in the Analog-to-Digital Conversion Timing Requirements was updated (see Table 36-40). The CTMU Current Source Specification conditions were updated (see Table 36-43).
37.0 “AC and DC Characteristics Graphs”	The Typical CTMU Temperature Sensor Voltage graph was removed (was Figure 37-5).

Revision G (December 2019)

This revision includes the following major changes, which are referenced by their respective chapter in Table 40-4.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE 40-4: MAJOR SECTION UPDATES

Section Name	Update Description
“Device Pin Tables”	Updated the following tables with new pin descriptions to include CVD pin designations: • **TABLE 3: “Pin Names for 64-pin General Purpose (GPD/GPE) Devices”** • **TABLE 4: “Pin Names for 64-pin Motor Control (MCF) Devices”** • **TABLE 5: “Pin Names for 100-pin General Purpose (GPD/GPE) Devices”** • **TABLE 6: “Pin Names for 100-pin Motor Control (MCF) Devices”**
1.0 “Device Overview”	Added a new table: **TABLE 1-3: “CVD, CAPACITIVE TOUCH ASSIST PINOUT I/O DESCRIPTIONS”**
39.0 “Appendix A: Migration Guide”	Added new **Appendix A: Migration Guide**.
Register 30-3 QEIxSTAT: QEIx Status Register	Updated bit definitions for the PCHEQIRO and PCLEQIRQ bits.
Updated	**Section 38.2 “Package Details”**

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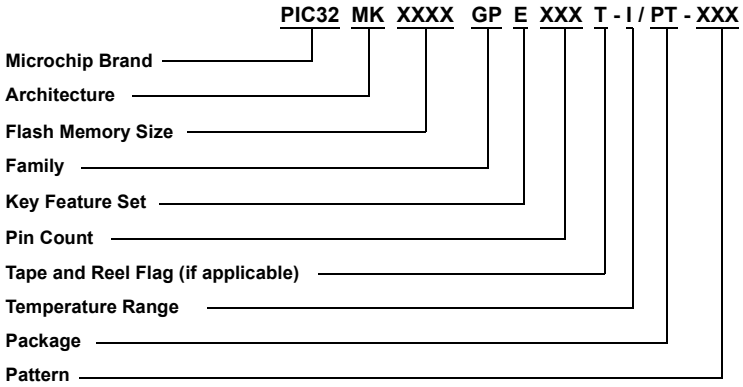

Example:

PIC32MK1024GPE100-I/PT:
General Purpose PIC32MK with CAN,
MIPS32® microAptiv MCU core,
1024 KB program memory,
100-pin, Industrial temperature,
TQFP package.

Flash Memory Family

Architecture	MK	= MIPS32® microAptiv MCU Core with Floating Point Unit (FPU)
Flash Memory Size	0512	= 512 KB
	1024	= 1024 KB
Family	GP	= General Purpose Microcontroller Family
	MC	= Motor Control Microcontroller Family
Key Feature	D	= PIC32 GP Family Features (without CAN)
	E	= PIC32 GP Family Features (with CAN)
	F	= PIC32 MC Family Features (with CAN, PWM, and QEI)
Pin Count	064	= 64-pin
	100	= 100-pin
Temperature Range	I	= -40°C to +85°C (Industrial)
	I	= -40°C to +105°C (V-Temp)
	E	= -40°C to +125°C (Extended)
Package	MR	= 64-Lead (9x9x0.9 mm) VQFN (Plastic Quad Flatpack)
	PT	= 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack)
	PT	= 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack)
Pattern		Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)
	ES	= Engineering Sample

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