PD70210/PD70210A/ PD70210AL

Front-End PD Interface Controller

Product Overview

The PD70210, PD70210A, and PD70210AL devices are advanced PD interface controllers (front-end IC) for powered devices in PoE applications. They support IEEE® 802.3af, IEEE 802at, HDBaseT, and general 2-pair or 4-pair configurations.

The PD70210, PD70210A, and PD70210AL devices have an advanced classification block that supports 2, 3, 4, and 6 event classification. These devices also identify the four pairs of cable that receives power and generates appropriate flags by using the SUPP_Sx pins. The IC features an internal bleeder for rapidly discharging the input capacitor of the DC–DC converter to ensure fast re-detection and port power-up on sudden removal and re-insertion of the Ethernet cable into RJ45.

Features

The following are the features of PD70210, PD70210A, and PD70210AL devices.

- Supports IEEE 802.3af/at, HDBaseT, and other 2-pair or 4-pair configurations
- PD detection and programmable classification
- 2, 3, 4, and 6 event classification
- Integrated 0.3 Ω isolating (series-pass) FET
- In-rush current limiting
- Wall adapter priority support (PD70210A and PD70210AL only)
- Less than 5 µA offset current during detection
- DFN-16/QFN-38 package
- Power Good Flag (PD70210 only)

The following table lists the Microchip PD products offerings.

Table 1. Microchip Powered Device Products Offerings

Part	Type	Package	IEEE 802.3af	IEEE 802.3at	HDBaseT (PoH)	UPoE
PD70100	Front-end	3 mm × 4 mm 12L DFN	x	—	—	—
PD70101	Front-end + PWM	5 mm × 5 mm 32L QFN	x	—	—	—
PD70200	Front-end	3 mm × 4 mm 12L DFN	x	x	—	—
PD70201	Front-end + PWM	5 mm × 5 mm 32L QFN	x	x	—	—
PD70210	Front-end	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210A	Front-end	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210AL	Front-end	5 mm × 7 mm 38L QFN	x	x	x	x
PD70211	Front-end + PWM	6 mm × 6 mm 36L QFN	x	x	x	x
PD70224	Ideal diode bridge	6 mm × 8 mm 40L QFN	x	x	x	x

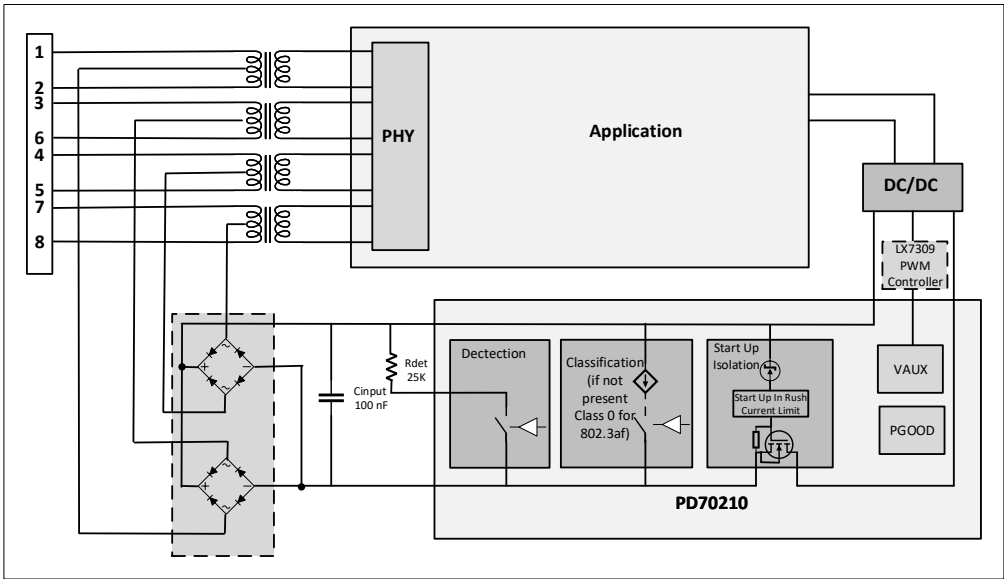
Applications

The following are the applications of PD70210, PD70210A, and PD70210AL devices.

- Single HDBaseT or double up to 95 W
- IEEE 802.3af and IEEE 802.3at
- Indoor and outdoor PoE

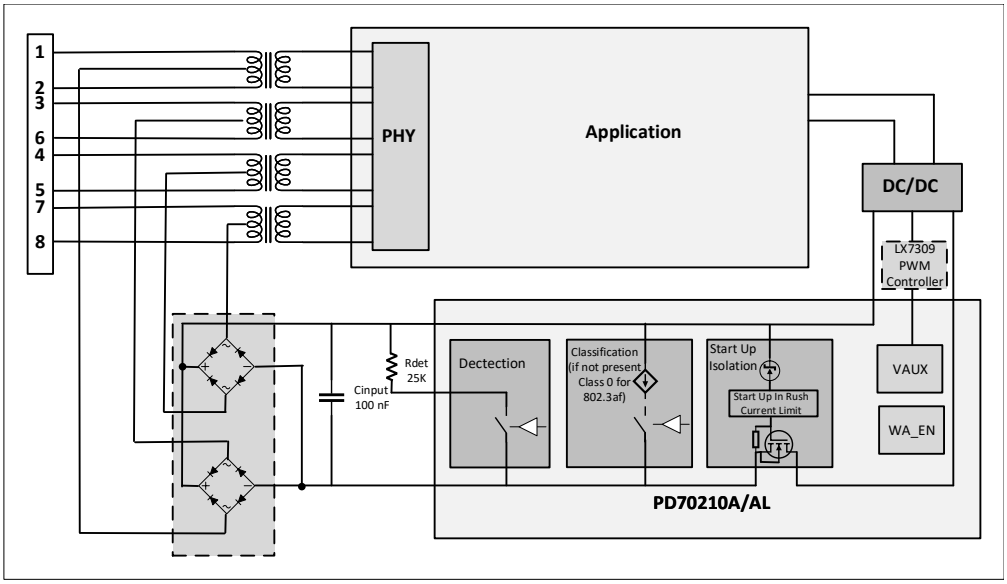
The following figure shows a typical PD70210 application.

Figure 1. Basic PD70210 Block Diagram



The following figure shows a typical PD70210A/AL application.

Figure 2. Basic PD70210A/AL Block Diagram



Microchip offers complete reference design packages and Evaluation Boards (EVBs). For access to these design packages, device datasheets, or application notes, consult local Microchip Client Engagement Manager or visit Microchip website. For technical support, consult local Embedded Solutions Engineers or go to www.microchip.com/support. For help in designing the DC-DC portion of circuit try MPLAB Analog Designer (MAD) tool.

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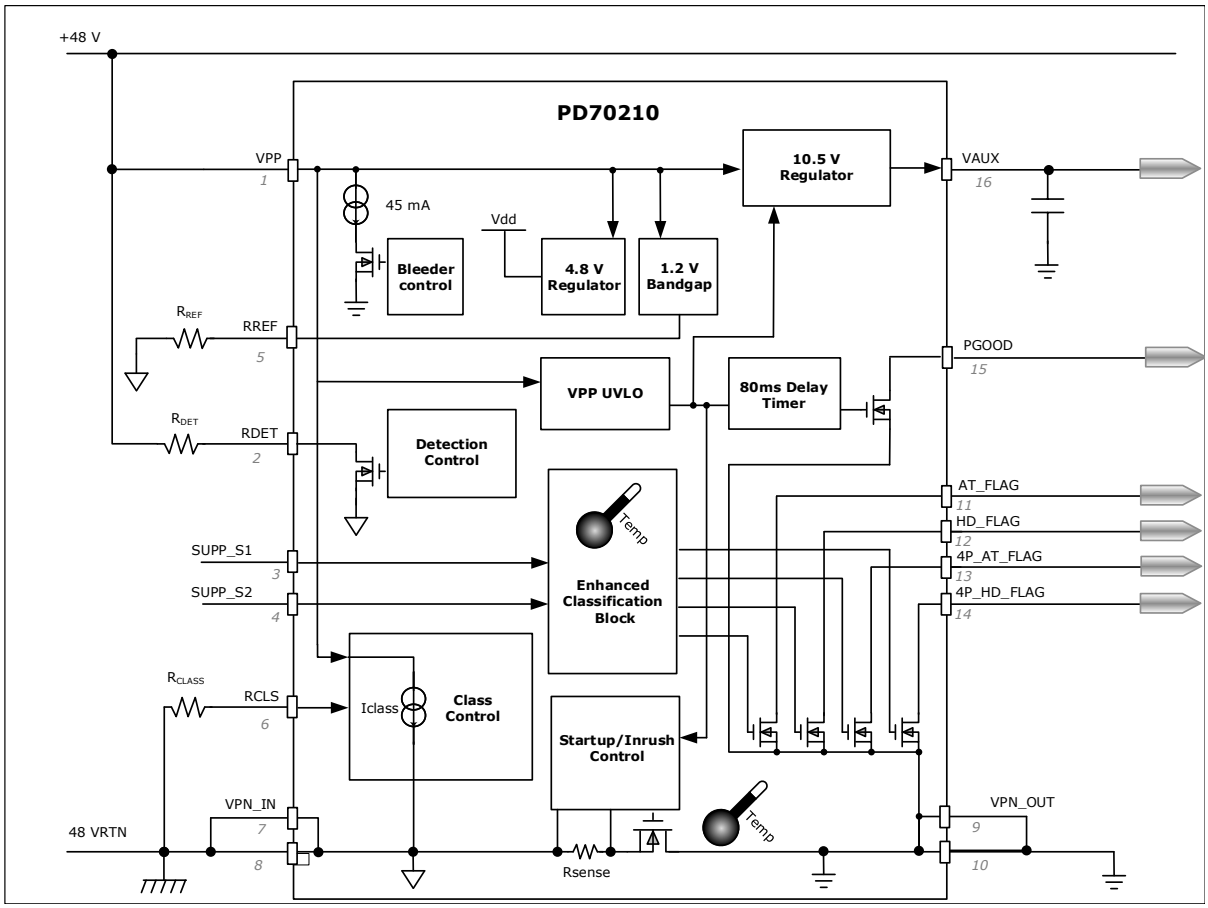
1. Functional Descriptions

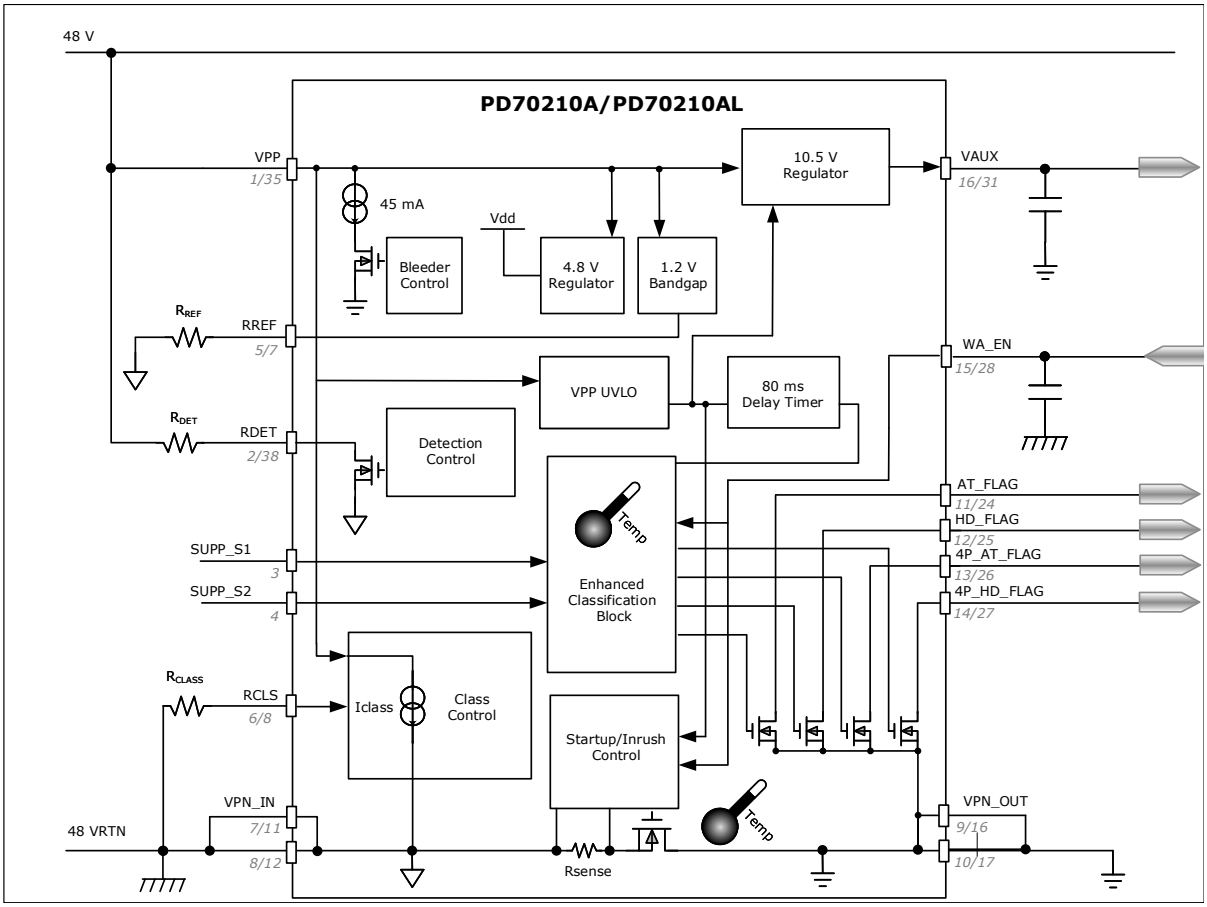
The following figure shows the functional blocks of the PD70210 device.

Figure 1-1. PD70210 Functional Block Diagram



The following figure shows the functional blocks of the PD70210A/PD70210AL devices.

Figure 1-2. PD70210A/PD70210AL Functional Block Diagram



1.1 Application Information

This section describes the PD70210/A/AL application.

For latest recommendations, contact Microchip and/or see *AN3468 Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Front-End Using PD702x0 and PD701x0 ICs*.

1.2 Wall Adapter Mode (PD70210A/AL)

PD70210A and PD70210AL supports wall adapter functionality. By setting the WA_EN pin high, it gives priority to the wall adapter jack to supply the load.

The WA_EN pin is used while connecting a wall-adapter voltage between VPP and VPN_OUT by OR-ing diode. When WA_EN (the wall adapter enable pin) is held low (referenced to VPN_IN), the front-end works as a normal PD. When WA_EN is raised high (referenced to VPN_IN), the following three internal operations are forced.

- The isolation FET is turned off.
- All output flags (AT_FLAG, HD_FLAG, 4P_AT_FLAG, and 4P_HD_FLAG) are activated (low state).
- Vaux output voltage is turned on.

While activating the WA_EN pin, the wall adapter supplies input voltage for the DC–DC converter. The WA_EN at a high state disables the detection and classification modes.

1.2.1 Peripheral Devices

The following is the list of PD70210/A/AL peripheral devices.

- Place 47 nF to 100 nF/100 V capacitor between the device's VPP and VPNI pins and close to the device.
- Place a 58 V TVS between device VPP and VPN_IN pins for protection against voltage transients. For complete surge protection, see *AN3410 Design for PD System Surge Immunity PD701xx and PD702xx Application Note*.
- If 4-pair flags are used, place a 10 kΩ resistor on SUPP_S1 and SUPP_S2 lines between the diode bridge and PD70210/A device.
- When WA_EN is used, place 100 nF to 1 µF/10 V capacitor between WA_EN and the VPN_IN pin, close to the PD70210/A device.
- When it is not used, connect the WA_EN to the VPN_IN pin.
- Place 4.7 µF/25 V capacitor between Vaux pin and VPN_OUT.

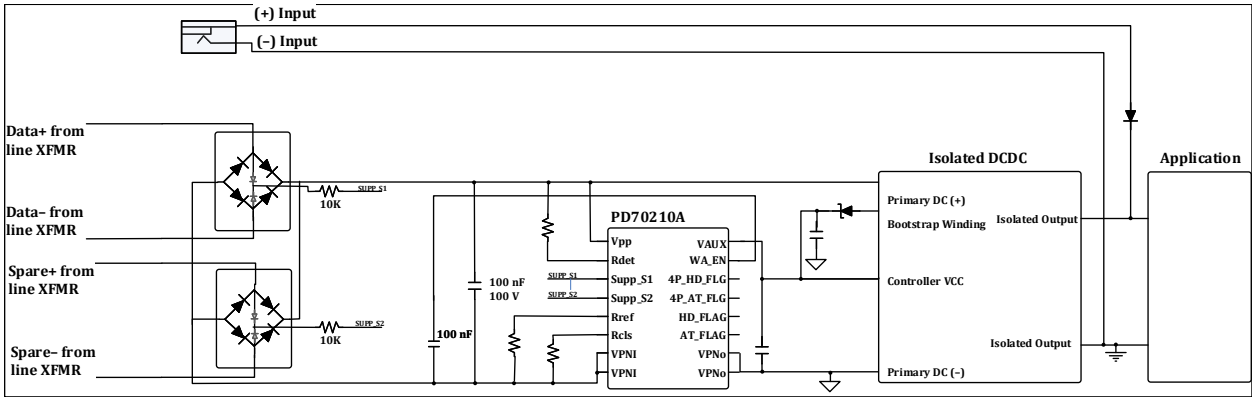
1.2.2 Operation with an External DC Source

PD applications using PD70210A IC operates with an external power source (DC wall adapter). The two cases of providing power with an external source is detailed in the following sections.

1.2.2.1 External Power Input Connected to Application Supply Rails

In this application, the external source is connected to the application's low-voltage supply rails. The external source voltage level depends on DC–DC output characteristics.

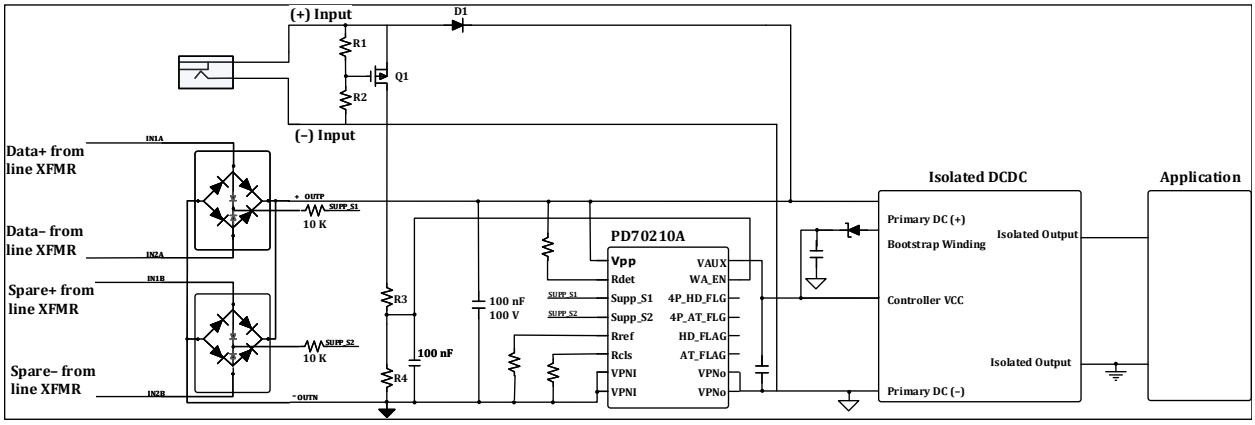
Figure 1-3. External Power Input to Supply Rails



1.2.2.2 External Power Input Connected to PD70210A Output

In this application, the external source is connected to the PD device's output connection for the application (VPP to VPN_{OUT}). The external source voltage level depends on the DC–DC input requirements.

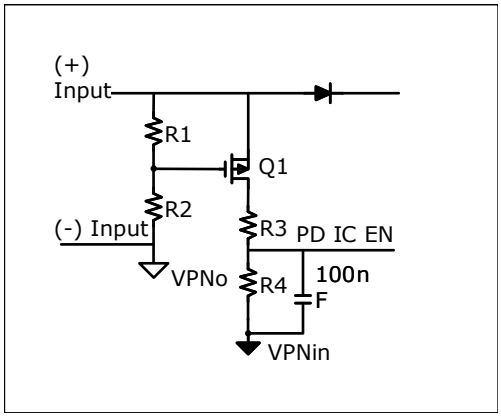
Figure 1-4. External Power Input to PD70210A Output



When an external adapter is connected, the PD70210A WA_EN pin is used for disabling the isolation switch and PSE input power. The WA_EN pin resistors divider depends on the WA_EN threshold of the PD70210A.

The following figure shows a detailed view of the resistors to be selected in an external adapter connection.

Figure 1-5. External Power Input Resistors Dividers



R1 and R2 sets a threshold for Pfet Q1 enable to detect an external adapter. It must be set to a lower threshold than PD70210A disable levels. R3 and R4 sets the PD70210A disable threshold. Therefore, in 36 V–57 V external adapter, the disable settings are selected as follows:

- Pfet enable threshold = 30 V.
- R1 and R2 setting must be the value of Q1 VGS < 20 V at the maximum voltage condition of the external adapter.
- When the external adapter voltage is more than 30 V, Q1 is more than its VGS_{TH} value.

$$VGS = Vext\_adapter \times \frac{R1}{R1 + R2}$$

- R1 is selected as 2 kΩ.

$$R2 = R1 \times \frac{Vext\_adapter - VGS}{VGS}$$

- Using R1 = 2 kΩ, Vext_adapter = 30 V, and VGS = maximum VGS_{TH} = 3.5 V, provides the R2 value as 15 kΩ.
- R3 and R4 are set to the range of few kΩ to tens of kΩ using the following equation.

$$PD70210A\_Wa\_en = Vext\_adapter\_PD70210A \text{ x } \frac{R4}{(R3+R4)}$$

- Using R3 = 15 kΩ, Vext_adapter = 33.7 V, and PD70210A_WA_EN = 2.4 V as turn-off minimum threshold from the datasheet, solving the equation gives the valid resistor values for an adapter of 36 V and above. The values are: R3 = 15 kΩ and R4 = 1.15 kΩ.

  For more information and various adapter connection methods, see *AN3472 Implementing AUX Power in PoE Application Note*.

1.3 Flags

The following truth table lists the flags status.

Table 1-1. Truth Table for Status of Flags

Number of Fingers "N" (N-Event Classification)	SUPP_S1	SUPP_S2	AT_FLAG	HD_FLAG	4P_AT_FLAG	4P_HD_FLAG
1	X	X	Hi Z	Hi Z	Hi Z	Hi Z
2	H	L	0 V	Hi Z	Hi Z	Hi Z
2	L	H	0 V	Hi Z	Hi Z	Hi Z
2	H	H	0 V	Hi Z	0 V	Hi Z
3	L	H	0 V	0 V	Hi Z	Hi Z
3	H	L	0 V	0 V	Hi Z	Hi Z
3	H	H	0 V	0 V	0 V	Hi Z
4	X	X	0 V	0 V	0 V	Hi Z
5	Reserved for future					
6	X	X	0 V	0 V	0 V	Hi Z

Note: A flag's state is set only once at port turn on, while VPP-VPNin voltage crosses $UVLO_{ON}$. If SUPP_S1 and SUPP_S2 pins are changing after port turn on, the flags do not change accordingly.

2. Electrical Specifications

Unless otherwise specified under conditions, the minimum and maximum ratings stated apply over the entire specified operating rating of the device. Typical values are obtained either by design or by production testing at 25 °C ambient. Voltages are with respect to IC ground (VPN_IN).

Table 2-1. Input Voltage

Symbol	Parameter	Conditions	Typical	Maximum	Unit
I_{IN}	IC input current with I_{CLASS} off	VPP = 55 V	1	3	mA

Table 2-2. Detection Phase

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{DET}	Detection range	—	1.1	—	10.1	V
R_{DET_TH}	R_{DET} disconnect threshold	—	10.1	—	12.8	V
$R_{DS\_DET\_ON}$	On-resistance of internal FET during detection	—	—	—	50	Ω
$R_{DS\_DET\_OFF}$	Off-resistance of internal FET after detection	—	2	—	—	MΩ
I_{OFFSET_DET}	Input offset current	1.1 V ≤ VPP ≤ 10.1 V T_J ≤ 85 °C	—	—	5	µA
$V_{R\_DET\_ON}$	R_{DET} reconnection threshold when VPP goes low	—	2.8	3.0	4.85	V

Table 2-3. Classification Phase

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CLS_ON}	Classification sink turn-on threshold	—	11.4	—	13.7	V
V_{CLS_OFF}	Classification sink turn-off threshold	—	20.9	—	23.9	V
$V_{HYS\_CLS\_ON}$	Hysteresis of V_{CLS_ON} threshold	—	—	1	—	V
V_{MARK_TH}	Mark detection threshold (VPP falling)	—	10.1	—	11.4	V
I_{MARK}	Current sink in mark event region	—	0.25	—	4	mA

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Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{CLASS_CLIM}	Current limit of class current	—	50	68	80	mA
I_{CLASS}	Classification current sink	R_{CLASS} = not present (Class 0)	—	—	3	mA
		R_{CLASS} = 133 Ω (Class 1)	9.5	10.5	11.5	
		R_{CLASS} = 69.8 Ω (Class 2)	17.5	18.5	19.5	
		R_{CLASS} = 45.3 Ω (Class 3)	26.5	28.0	29.5	
		R_{CLASS} = 30.9 Ω (Class 4)	38.0	40.0	42.0	

Table 2-4. Isolation FET

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{DSON}	On resistance	Total resistance between VPN_IN to VPN_OUT; I_{LOAD} < 600 mA, –40 °C < T_A < 85 °C	—	0.22	0.3	Ω
I_{CLIM_INRUSH}	Inrush current limit	—	105	240	325	mA
OCP	Overcurrent protection	—	2.2	—	—	A
I_{LOAD}	Continuous operation load[1]	—	—	—	2	A

Note: 1. Actual maximum load is subjected to the application environment conditions, such as ambient temperatures, air flow, mutual heating by other components, and so on.

Table 2-5. Undervoltage Lockout

Symbol	Parameter	Minimum	Maximum	Unit
$UVLO_{ON}$	Threshold that marks start of inrush phase	36	42	V
$UVLO_{OFF}$	Threshold where pass-FET turns off as VPP collapses	30.5	34.5	V

Table 2-6. DC–DC Input Cap Discharger

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
I_{CAP_DIS}	Discharge current (PD70210)	12 V ≤ VPP ≤ 30 V 7 V ≤ VPP ≤ 12 V	22.8 10	60	mA mA
I_{CAP_DIS}	Discharge current (PD70210A)	7 V ≤ VPP ≤ 30 V	22.8	60	mA
$timer_{dis}$	Discharge timer	Time for which discharge circuit is activated	430	—	ms

Table 2-7. References, Rails, and Logic

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{AUX}	Auxiliary voltage	0 mA < I_{AUX} < 4 mA	9.8	10.5	12.0	V
I_{AUX_CLIM}	Auxiliary current limit	—	10	—	32	mA
V_{REF}	Bias current reference voltage	—	1.17	1.2	1.23	V
V_{FLAG_LO}	Low level flag	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG, I_{FLAG} = 3 mA	—	—	0.4	V
V_{PGOOD_LO}	Power good, active low voltage	I_{PGOOD} = 3 mA PD70210 only	—	—	0.4	V
t_{FLAG}	Delay timer between start of inrush and flags declared	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	80	—	—	ms
t_{PGOOD}	Delay timer between start of inrush and power good declared	PD70210 only	80	—	—	ms
I_{FLAG_max}	Flag current driving capability	For AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG	5	—	—	mA
I_{PGOOD_max}	Power good current capability	PD70210 only	5	—	—	mA

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Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{SUPP_HI}	SUPP_Sx high voltage threshold	For SUPP_S1 and SUPP_S2	25	—	35	V

Table 2-8. Wall Adapter Enable Pin

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{IH}	Input high logic	PD70210A, PD70210AL only	2.4	—	V
V_{IL}	Input low logic	PD70210A, PD70210AL only	—	0.8	V

2.1 Absolute Maximum Ratings

Performance is not guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings cause immediate damage or negatively impact long-term operating reliability. Voltages are with respect to IC ground (VPN_IN), unless otherwise specified.

Table 2-9. Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
VPP, RDET		–0.3	74	V
PGOOD, AT_FLAG, HD_FLAG, 4P_AT_FLAG, 4P_HD_FLAG referenced to VPN_OUT		–0.3	20	V
SUPP_S1, SUPP_S2		0	V_{VPP} + 1.5	V
RREF, RCLS, WA_EN		–0.3	5	V
Junction temperature		–40	150	°C
Lead soldering temperature (40 s, reflow)			260	°C
Storage temperature, MSL3		–65	150	°C
ESD rating	HBM (PD70210)	—	±1.5	kV
	HBM (PD70210A/ PD70210AL)	—	±1.25	kV
	MM	—	±100	V
	CDM	—	±500	V

2.2 Operating Conditions

Performance is guaranteed over this range as described in other electrical characteristics tables. Voltages are with respect to IC ground (VPN_IN).

Table 2-10. Operating Conditions

Conditions	Minimum	Maximum	Units
VPP	0	57	V
Ambient temperature[1]	–40	85	°C
Detection range	1.1	10.1	V
Mark event range	4.9	10.1	V
Class event range	13.7	20.9	V

Note: 1. Corresponding maximum operating junction temperature is 125 °C.

2.3 Thermal Properties

The following table shows the thermal properties of the device.

Table 2-11. Thermal Properties

Thermal Resistance	Typical	Units
θ_{JA}	31	°C/W
θ_{JP}	3	°C/W
θ_{JC}	4	°C/W

Note: θ_{JX} numbers assume no forced airflow. Junction temperature is calculated using $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} is a function of the PCB construction. The stated number is for a four-layer board in accordance with JESD-51 (JEDEC®).

3. Pin Descriptions

This section provides the pin information for the PD70210/PD70210A/PD7021AL devices.

The following figures show the device pin diagrams (top and bottom views).

Figure 3-1. PD70210 Pinout

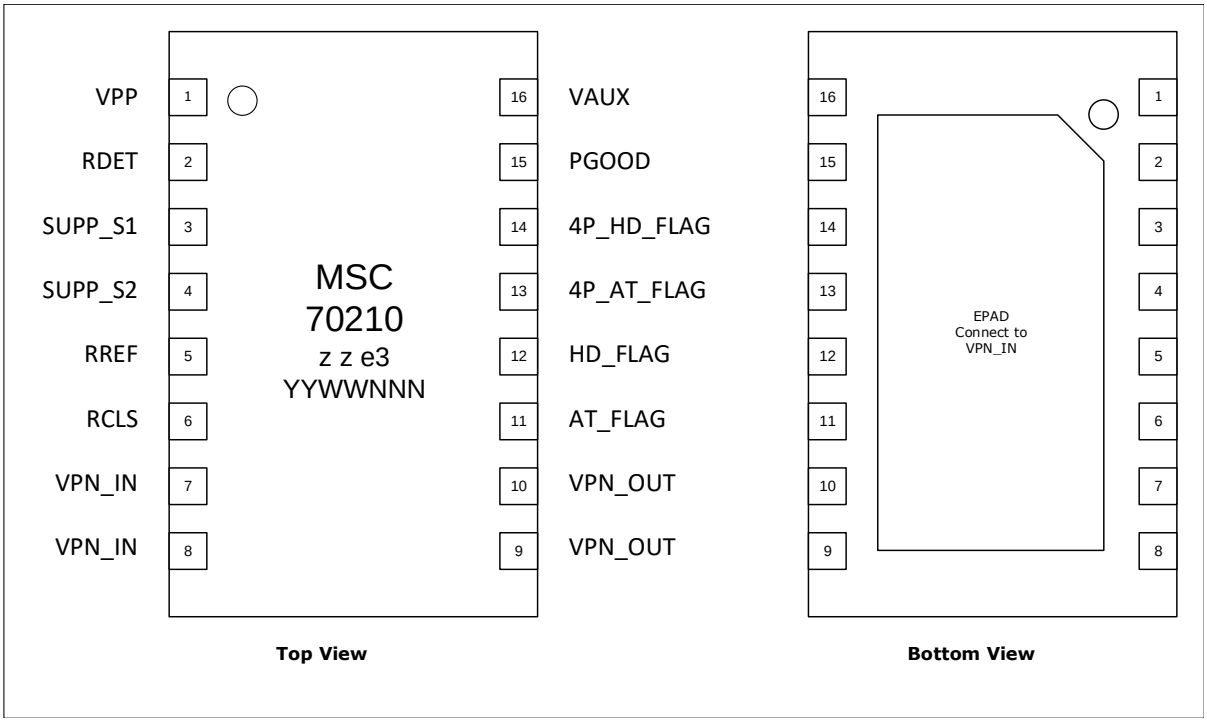


Figure 3-2. PD70210A Pinout

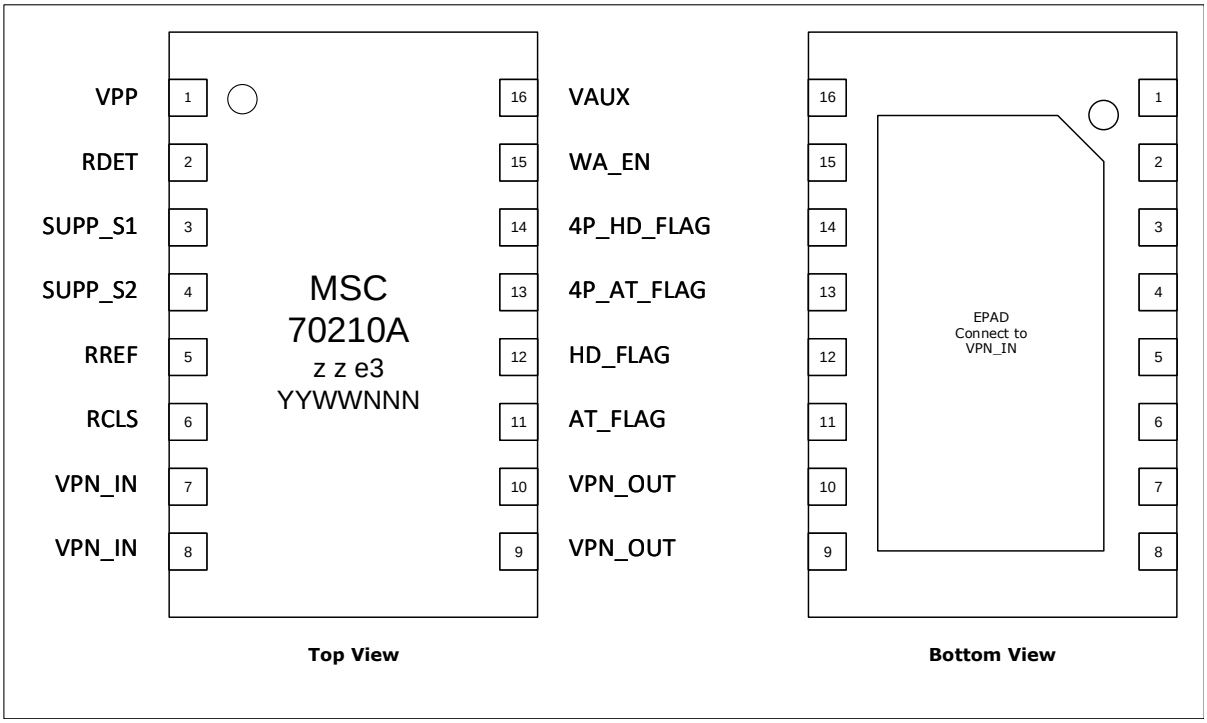
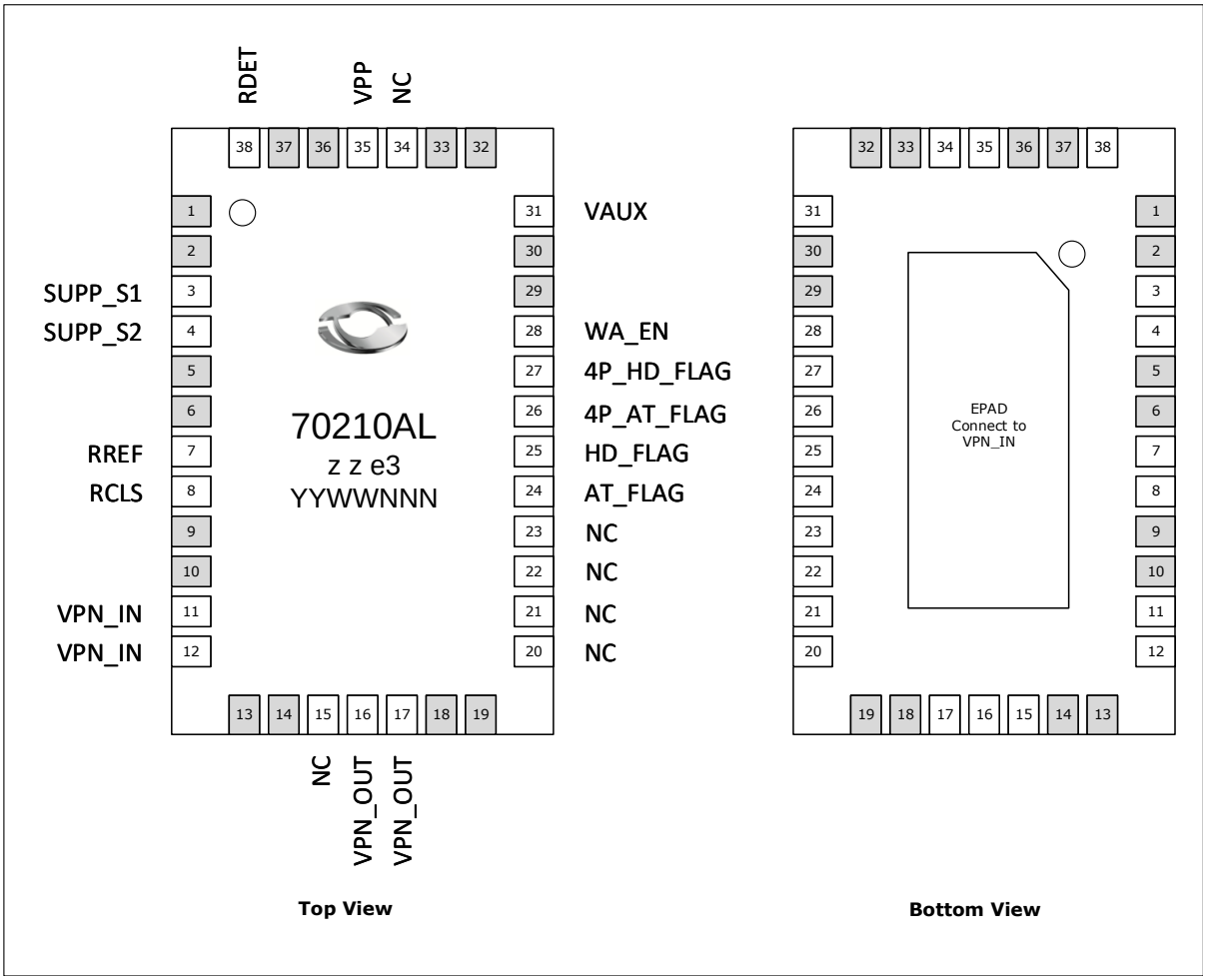


Figure 3-3. PD70210AL Pinout



Note: Shaded pins do not exist.

The following table lists the pin descriptions for the PD70210/PD70210A devices.

Table 3-1. PD70210/PD70210A Pin Descriptions

Pin Number	Pin Name (PD70210A)	Pin Name (PD70210)	Description
1	VPP	VPP	Upper rail of the incoming PSE voltage rail from the positive terminal of the two OR-ed bridge rectifiers. The corresponding lower PoE rail is VPN_IN.
2	RDET	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25 kΩ (or 24.9 kΩ) 1 % resistor is connected between this pin and VPP.
3	SUPP_S1	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin, along with the SUPP_S2 pin, can be used to distinguish between 2-pair and 4-pair operation for PSEs that operate in 4-pairs but do not generate the classification procedure on both pairs, but one pair only. Signal is referenced to VPN_IN. Place a 10 kΩ resistor in the input of this pin.

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Pin Number	Pin Name (PD70210A)	Pin Name (PD70210)	Description
4	SUPP_S2	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin, along with the SUPP_S1 pin, can be used to distinguish between 2-pair and 4-pair operation for PSEs that operate in 4-pairs but do not generate the classification procedure on both pairs, but one pair only. Signal is referenced to VPN_IN. Place a 10 kΩ resistor in the input of this pin.
5	RREF	RREF	Bias current resistor. A 60.4 kΩ 1 % resistor is connected between RREF and IC ground (VPN_IN).
6	RCLS	RCLS	Sets the class of the PD. Connect R_{CLASS} (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4, respectively. If RCLASS is not present, the PD will draw up to 3 mA during classification, indicating Class 0 (default type 1) to the PSE. Signal is referenced to VPN_IN.
7,8	VPN_IN	VPN_IN	Lower rail of the incoming PSE voltage rail, from the negative terminal of the two OR-ed bridge rectifiers. The corresponding upper PoE rail is VPP.
9,10	VPN_OUT	VPN_OUT	In effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and power-up. It is connected to the power ground and PWM controller IC's ground plane of the DC–DC converter section.
11	AT_FLAG	AT_FLAG	Open drain output. This pin gets actively pulled low when a type 2 PD-PSE mutually identifies each other through classification. In PD70210A, there is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. In PD70210, this flag asserts once inrush current is ended. Signal is referenced to VPN_OUT.
12	HD_FLAG	HD_FLAG	Open drain output. This pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identifies each other through classification. In PD70210A, there is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. In PD70210, this flag asserts once inrush current is ended. Signal is referenced to VPN_OUT.
13	4P_AT_FLAG	4P_AT_FLAG	Open drain output. This pin gets actively pulled low when a 4-pair version of a (non-standard) type 2 PD-PSE mutually identifies each other through classification. In PD70210A, there is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. In PD70210, this flag asserts once inrush current is ended. Signal is referenced to VPN_OUT.

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Pin Number	Pin Name (PD70210A)	Pin Name (PD70210)	Description
14	4P_HD_FLAG	4P_HD_FLAG	Open drain output. This pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identifies each other through classification. In PD70210A, there is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. In PD70210, this flag asserts once inrush current is ended. Signal is referenced to VPN_OUT.
15	WA_EN		While this input is low (referenced to VPN_IN), the chip works according to internal flow diagram. When this input is high, it enables the wall adapter feature. Place from 100 nF/10 V to 1 µF/10 V capacitor from WA_EN to VPN_IN pins, close to the device. When WA_EN is not used, connect it to VPN_IN. For more information, see Figure 1-3.
		PGOOD	Open drain output. Power good output signal from the front-end stage. This pin gets actively pulled low when power-on occurs. There is a minimum 80 ms delay from the moment VPort exceeds UVLO (~36 V) to this PGOOD signal being driven low as per the IEEE standard, to allow the PSE to increase its current limit after power-up is completed. Signal is referenced to VPN_OUT.
16	VAUX	VAUX	Auxiliary voltage rail. This can be used to provide a few mA of startup current for the PWM controller (typically, 10.5 V). Signal is referenced to VPN_OUT and is activated once the front-end power-up sequence ends. DC-DC must not start up until Vaux is active.
	EPAD	EPAD	Connected on PCB plane to VPN_IN.

The following table lists the pin descriptions for the PD70210AL device.

Table 3-2. PD70210AL Pin Descriptions

Pin Number	Pin Name	Description
1, 2	NA	
3	SUPP_S1	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin, along with the SUPP_S2 pin, can be used to distinguish between 2-pair and 4-pair operation for PSEs that operate in 4-pairs but do not generate the classification procedure on both pairs, but one pair only. Signal is referenced to VPN_IN. Place a 10 kΩ resistor in the input of this pin.
4	SUPP_S2	Input pin for sensing the voltage on the diode bridge connected to the data pairs. This pin, along with the SUPP_S1 pin, can be used to distinguish between 2-pair and 4-pair operation for PSEs that operate in 4-pairs but do not generate the classification procedure on both pairs, but one pair only. Signal is referenced to VPN_IN. Place a 10 kΩ resistor in the input of this pin.
5,6	NA	

.....continued

Pin Number	Pin Name	Description
7	RREF	Bias current resistor. A 60.4 kΩ 1% resistor is connected between RREF and IC ground (VPN_IN).
8	RCLS	Sets the class of the PD. Connect R_{CLASS} (programming resistor) between this pin and IC ground (VPN_IN). Allowed values are 133 Ω, 69.8 Ω, 45.3 Ω, and 30.9 Ω for Class 1, 2, 3, and 4, respectively. If RCLASS is not present, the PD will draw up to 3 mA during classification, indicating Class 0 (default type 1) to the PSE. Signal is referenced to VPN_IN.
9, 10	NA	
11, 12	VPN_IN	Lower rail of the incoming PSE voltage rail, from the negative terminal of the two OR-ed bridge rectifiers. The corresponding upper PoE rail is VPP.
13, 14	NA	
15	NC	No connect.
16, 17	VPN_OUT	In effect, the switched ground for establishing continuity to the PWM section after successful detection, classification, and power-up. It is connected to the power ground and PWM controller IC's ground plane of the DC–DC converter section.
18, 19	NA	
20, 21, 22, 23	NC	No connect.
24	AT_FLAG	Open drain output. This pin gets actively pulled low when a type 2 PD-PSE mutually identifies each other through classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
25	HD_FLAG	Open drain output. This pin gets actively pulled low when a 2-pair HDBaseT PD-PSE mutually identifies each other through classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
26	4P_AT_FLAG	Open drain output. This pin gets actively pulled low when a 4-pair version of a (non-standard) type 2 PD-PSE mutually identifies each other through classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
27	4P_HD_FLAG	Open drain output. This pin gets actively pulled low when a 4-pair HDBaseT PD-PSE mutually identifies each other through classification. There is a minimum 80 ms delay from the moment that the input capacitor is fully charged to this signal activity. Signal is referenced to VPN_OUT.
28	WA_EN	While this input is low (referenced to VPN_IN), the chip works according to internal flow diagram. When this input is high, it enables the wall adapter feature. Place from 100 nF/10 V to 1 µF/10 V capacitor from WA_EN to VPN_IN pins, close to the device. When WA_EN is not used, connect it to VPN_IN. For more information, see Figure 1-3.
29,30	NA	
31	VAUX	Auxiliary voltage rail. This is used to provide a few mA of startup current for the PWM controller (typically, 10.5 V). Signal is referenced to VPN_OUT and is activated once the front-end power-up sequence ends. DC–DC should not start up until Vaux is active.
32, 33	NA	

.....continued

Pin Number	Pin Name	Description
34	NC	No connect.
35	VPP	Upper rail of the incoming PSE voltage rail, from the positive terminal of the two OR-ed bridge rectifiers. The corresponding lower PoE rail is VPN_IN.
36, 37	NA	
38	RDET	Internally connects to VPN_IN during detection phase and disengages after it is over. A 25 kΩ (or 24.9 kΩ) 1% resistor is connected between this pin and VPP.
	EPAD	Connected on PCB plane to VPN_IN.

4. Package Information

This section provides information about the two available packages.

Note: Dimensions do not include protrusions. These shall not exceed 0.155 mm (0.006 in.) on any side. Lead dimension shall not include solder coverage. Dimensions are in millimeters, inches for reference only.

4.1 16-Pin Plastic DFN, 5 mm × 4 mm

This section shows the 16-pin plastic DFN, 5 mm × 4 mm package and package dimensions.

Figure 4-1. DFN Package

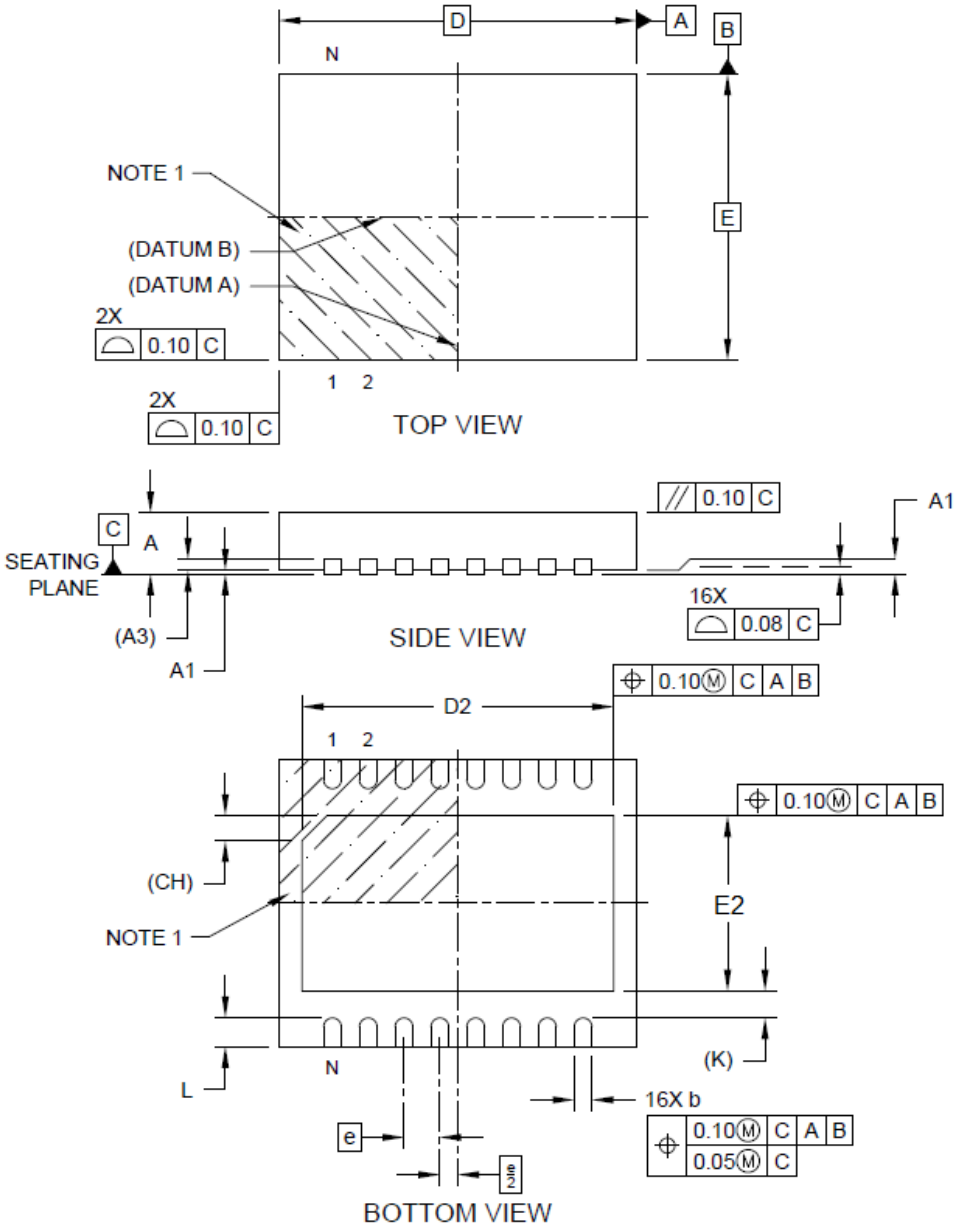


Table 4-1. Package Dimensions: DFN

Units		Millimeters		
Dimension Limit		**Min**	**Nom**	**Max**
Number of terminals	N		16	
Pitch	e	0.50 BSC		
Overall height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.03
Terminal thickness	A3	0.20 REF		
Overall length	D	5.00 BSC		
Exposed pad length	D2	4.25	4.35	4.45
Overall width	E	4.00 BSC		
Exposed pad width	E2	2.35	2.45	2.55
Index corner chamfer	CH	0.35 REF		
Terminal width	b	0.20	0.25	0.30
Terminal length	L	0.30	0.40	0.50
Terminal to exposed pad	K	0.35 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
4. For the most current package drawings, see the Microchip Packaging Specification located at www.microchip.com/packaging.

4.2 38-Pin Plastic QFN, 5 mm × 7 mm

This section shows the 38-pin plastic DFN, 5 mm × 7 mm package and package dimensions.

Figure 4-2. QFN Package

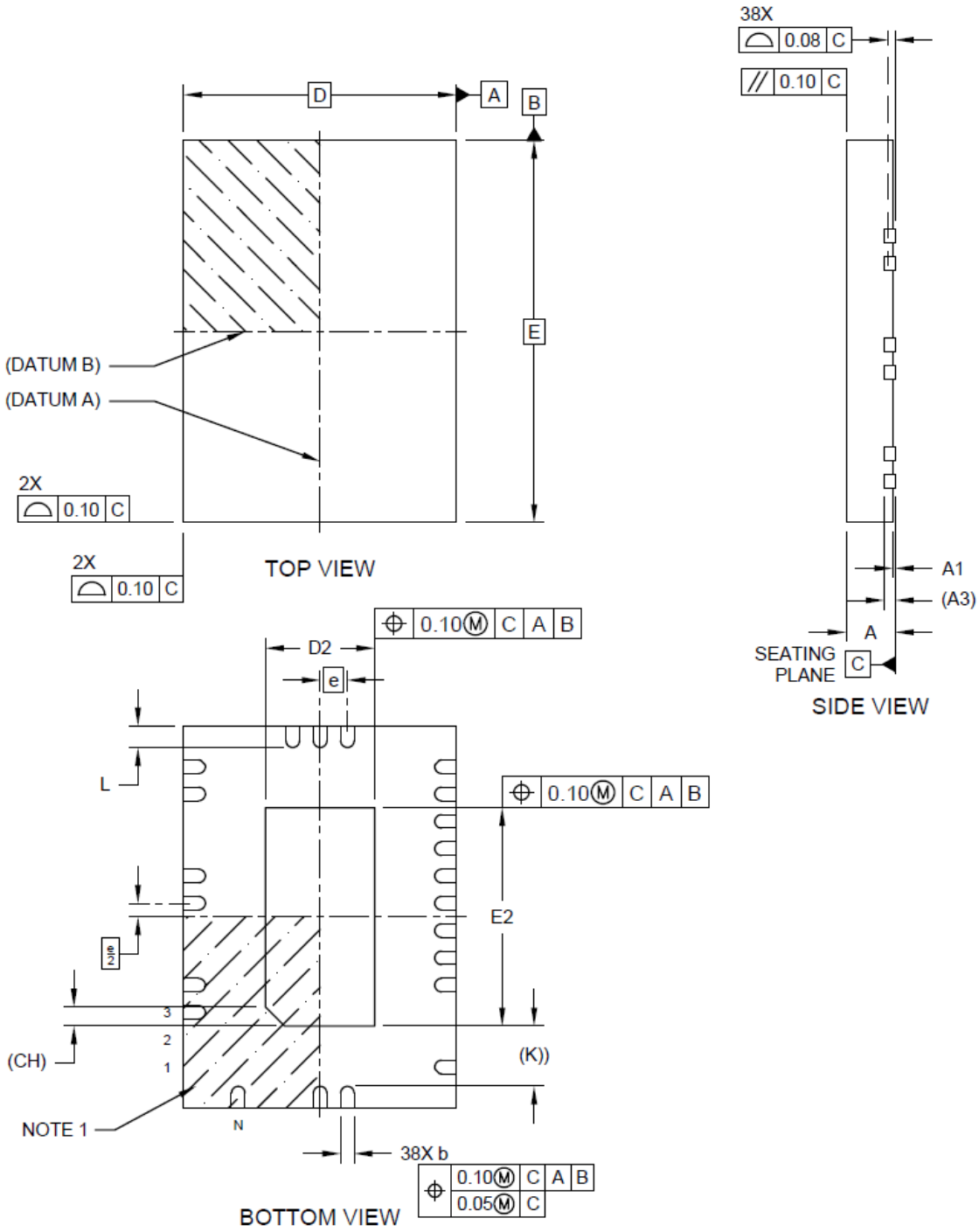


Table 4-2. Package Dimensions: QFN

Units		Millimeters		
Dimension Limist		**Min**	**Nom**	**Max**
Number of terminals	N	38		
Pitch	e	0.50 BSC		
Overall height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal thickness	A3	0.20 REF		
Overall length	D	5.00 BSC		
Exposed pad length	D2	1.90	2.00	2.10
Overall width	E	7.00 BSC		
Exposed pad width	E2	3.90	4.00	4.10
Terminal width	b	0.20	0.25	0.30
Terminal length	L	0.30	0.40	0.50
Terminal-to-exposedp-ad	K	1.016 REF		
Index corner chamfer	CH	0.35 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
4. For the most current package drawings, see the Microchip Packaging Specification located at www.microchip.com/packaging.

4.3 Thermal Protection

PD70210, PD70210A, and PD70210AL are protected from excessive internal temperatures that might occur during various operating procedures. Two temperature sensors are located on the chip, monitoring the temperatures of the isolating switch (pass-FET) and classification current sink.

Each over-temperature sensors activates a protection mechanism that disconnects the isolation (pass) FET or the classification circuit. This protects the device from being permanently damaged and from long-term degradation.

4.4 Recommended PCB Layout

The following figures show the PD70210-PD70210A and PD70210AL PCB layout based on the IPC7093A October 2020 standard. All previously published footprints are still supported.

Figure 4-3. PD70210 and PD70210A Solder Mask (Top View)

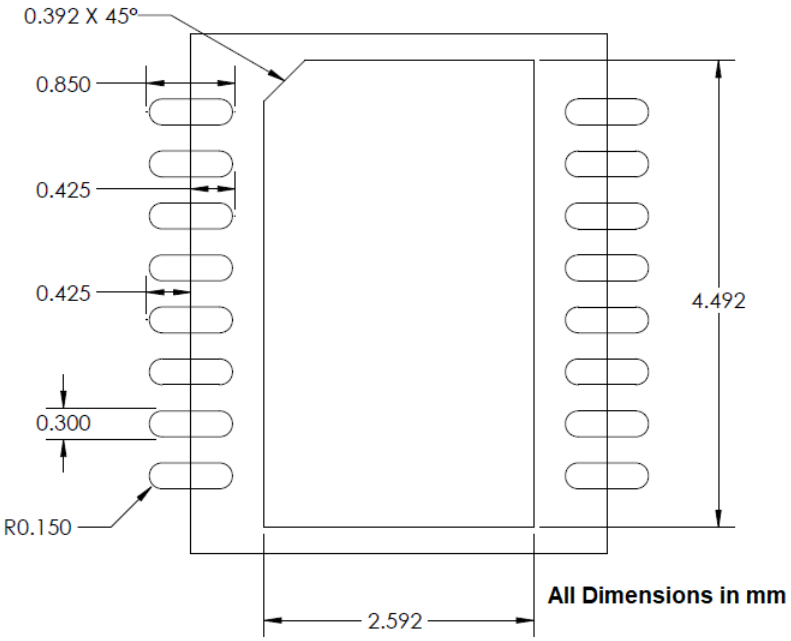


Figure 4-4. PD70210 and PD70210A Copper Layer (Top View)

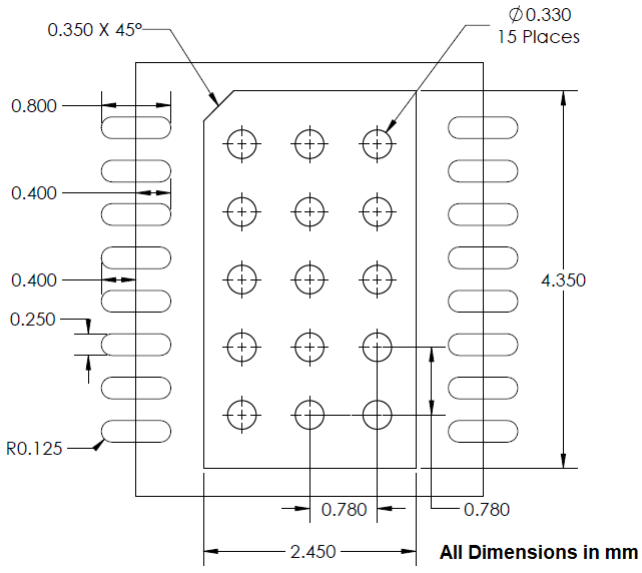
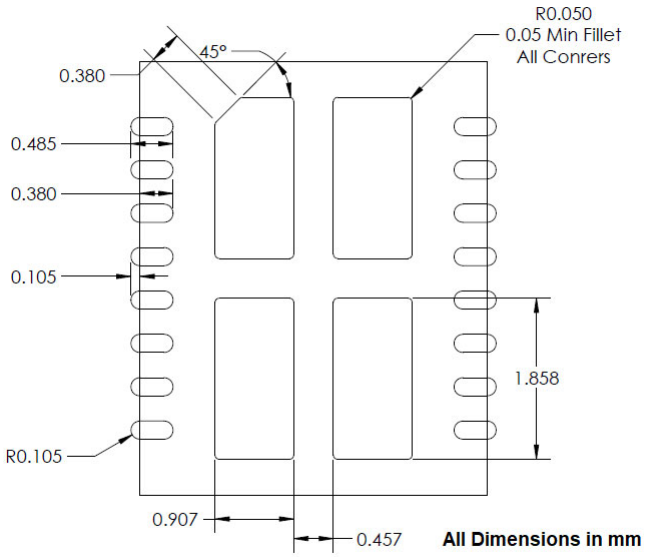


Figure 4-5. PD70210 and PD70210A Paste Mask (Top View



Note: Paste mask stencil is 5 mm thick. All paste mask openings have a radius of 0.05 mm.

Figure 4-6. D70210 and PD70210A Pin Geometry

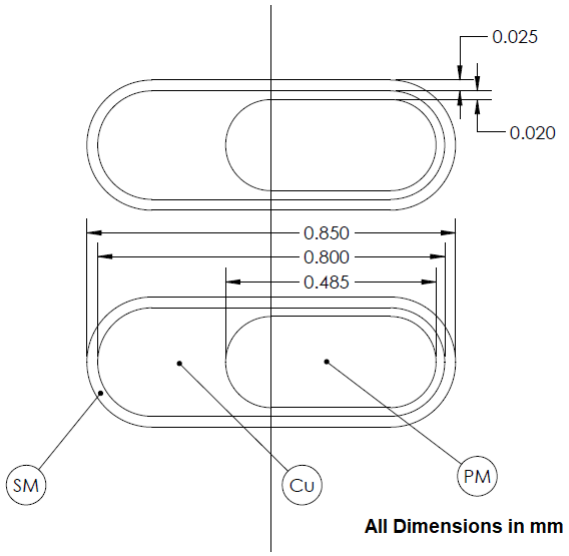


Figure 4-7. PD70210AL Solder Mask (Top View)

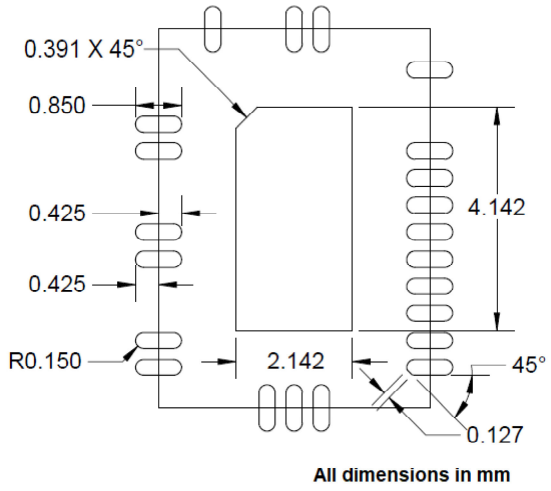


Figure 4-8. PD70210AL Copper Layer (Top View)

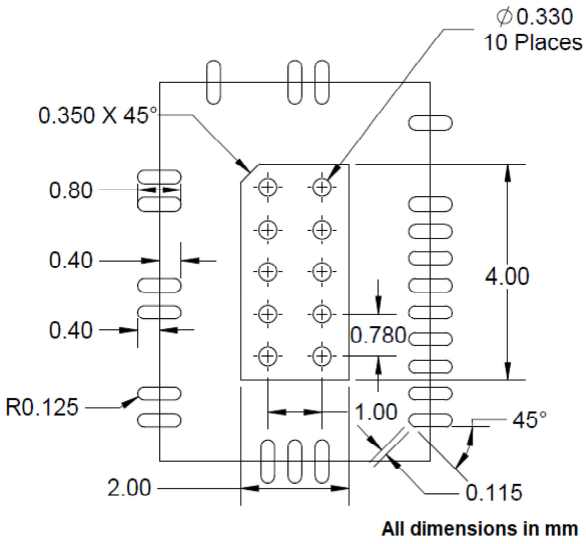
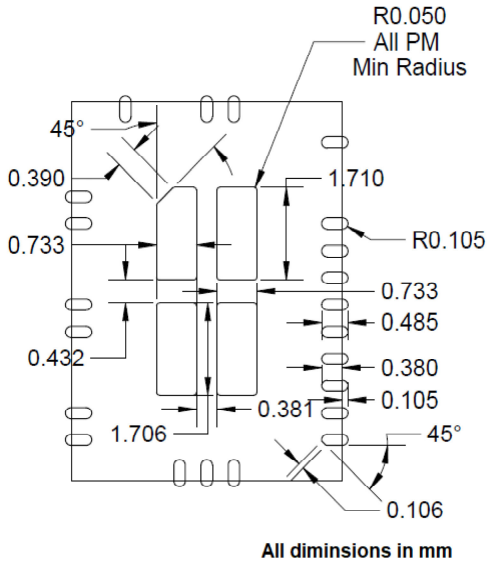
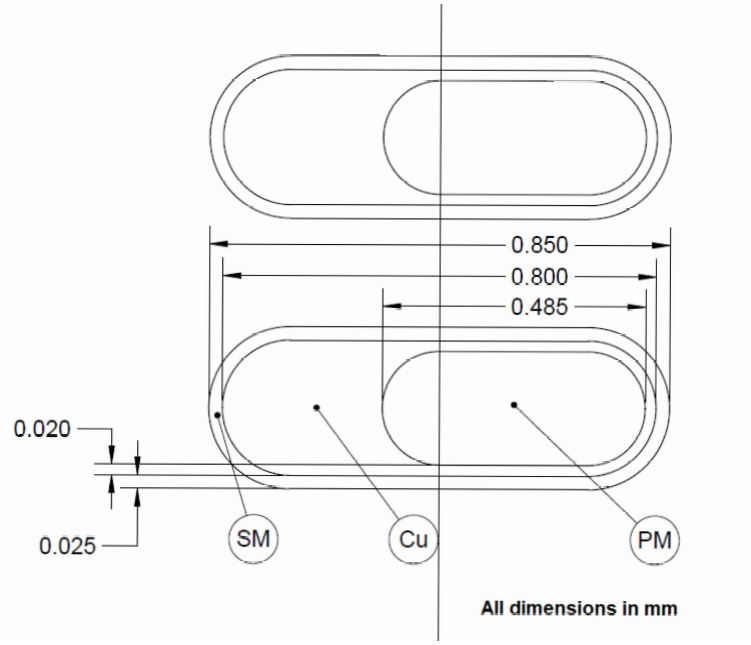


Figure 4-9. PD70210AL Paste Mask (Top View)



Note: Paste mask stencil is 5 mm thick. All paste mask openings have a radius of 0.05 mm.

Figure 4-10. PD70210AL Pin Geometry



5. Ordering Information

The following table lists the detailed part ordering information for the PD70210/PD70210A/PD70210AL devices. All part numbers are RoHS-compliant, Pb-free, and have an ambient temperature range of –40 °C to 85 °C. All parts also have 2-pair/4-pair HDBaseT support.

Table 5-1. Ordering Information

Part Number	Packaging Type	Package	Part Marketing	Wall Adapter Support	Clearance Between HV Pins
PD70210ILD-TR	Tape and reel	DFN 5 mm × 4 mm, 0.5 mm pitch 16 pins	MSC 70210 Z Z e3[1] YYWWNNN[2]	—	0.2 mm
PD70210AILD-TR	Tape and reel	DFN 5 mm × 4 mm, 0.5 mm pitch 16 pins	MSC 70210A Z Z e3[1] YYWWNNN[2]	Available	0.2 mm
PD70210ALILQ-TR	Tape and reel	QFN 5 mm × 7 mm, 0.5 mm pitch 38 pins	MSC logo 70210AL Z Z e3[1,3] YYWWNNN[2]	Available	1 mm

Notes:

1. ZZ e3: ZZ = Random character with no meaning and e3 = Second level interconnect.
2. YY = Year; WW = Week; NNN = Trace code.
3. This is a primary option. Other options are also available.

6. Reference Documents

- AN3533 PD70210/A/AL and PD70211 System Layout Guidelines
- AN3468 Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Front End Using PD702x0 and PD701x0 ICs
- AN3472 Implementing Auxiliary Power in PoE.

7. Revision History

Revision	Date	Description
B	08/2021	Revision B is the latest publication of this document. The following is the summary of changes: • Updated the figure and the table in the 4.1 16-Pin Plastic DFN, 5 mm × 4 mm section. • Updated the figure and the table in the 4.2 38-Pin Plastic QFN, 5 mm × 7 mm section. • Added the 4.4 Recommended PCB Layout section.
A	10/2020	Revision A is the latest publication of this document. The following is the summary of changes: • The document was updated to Microchip template. • The document number updated to DS00003695.
3.0	10/2019	The following is a summary of the changes in revision 3.0 of this document. • Updated package marking of the following figures. – Figure 3-1 – Figure 3-2 – Figure 3-3 • 1.1 Application Information section was updated. • 5. Ordering Information section was updated.
2.0	03/2020	The following is a summary of changes in revision 2.0 of this document. • Document format was updated. • Capacitor between VAUX and VPN_OUT was updated to 4.7 µF according to AN_209 Application Note. For more information, see Applications. • MSL3 rating was added to the storage temperature information. For more information, see 2.1 Absolute Maximum Ratings.
1.51	10/2015	The following is a summary of changes in revision 1.51 of this document. • The 80 mS delay was removed from the Vaux pin description. • Missing UVLO_ON information was added.
1.50	10/2014	Added flag description details in revision 1.50
1.40	06/2014	Added WA_EN information in revision 1.40.
1.38	04/2014	Added thermal properties were in revision 1.38.
1.37	01/2014	Corrected package information in revision 1.37.
1.36	01/2014	Added IC marking information in revision 1.36.

.....continued		
Revision	**Date**	**Description**
1.34		The following is a summary of changes in revision 1.34 of this document. • A new 38-pin, 5 × 7 QFN package option was added (PD70210AL). • The package drawing was updated and an application diagram for the new package added. • The flag table was updated.
1.2	11/2013	In revision 1.2 of this document, the PD70210 application diagram was updated.
1.1	10/2013	In revision 1.1 of this document, the Vaux description and cap GND symbol were fixed.
1.0	06/2013	Revision 1.0 was the first publication of this document.

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