AN1824
Application Note
MSCSICMDD/REF1 Dual SiC MOSFET Driver Reference Design

Final

February 2018

Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

Revision 1.1 was published in February 2018. The following is a summary of changes in revision 1.1 of this document.

- The configuration switch settings were updated. For more information about the configuration switch settings, see Configuration Switch Settings (see page 5).
- The J7 control connector pinout was updated. For more information about the control connector pinout, see J7 Control Connector Pinout (see page 8).
- The High-Voltage Plane Top and High-Voltage Plane Bottom schematics were updated. For more information, see Schematics (see page 20).
- Added explanatory text about desaturation protection. For more information, see Desaturation Protection (see page 11).

1.2 Revision 1.0

Revision 1.0 was published in October 2016. It was the first publication of this document.

2 Overview

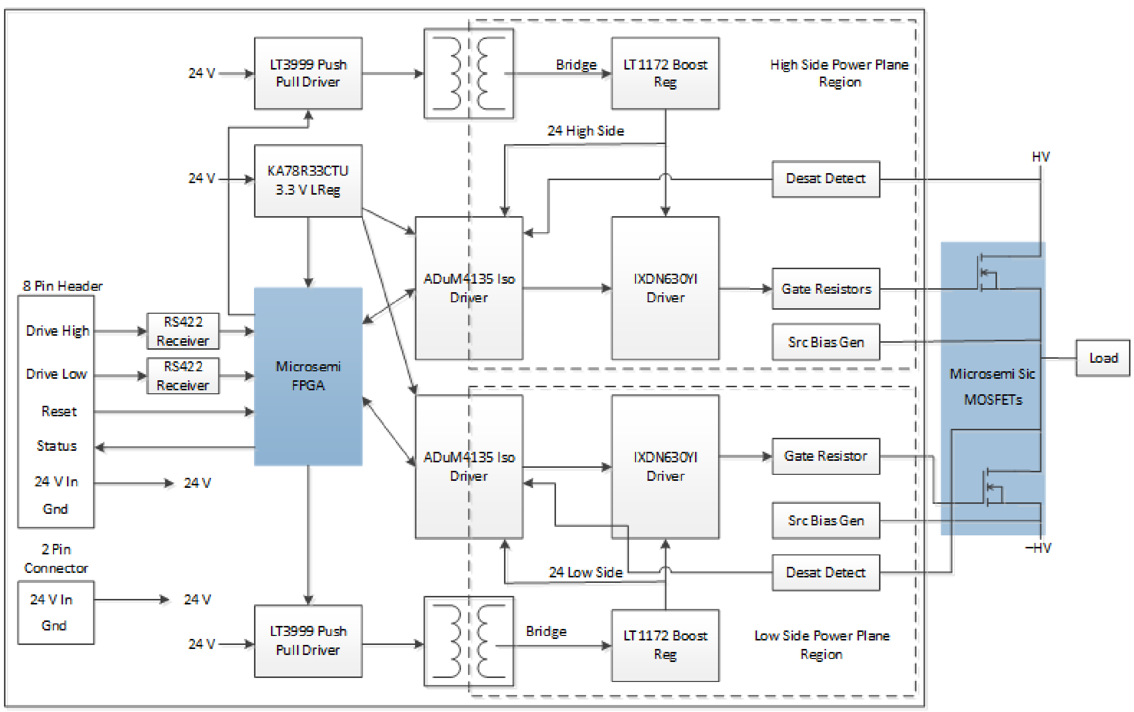
This document provides an example of a highly-isolated SiC MOSFET dual-gate driver. It can be configured by switches to drive as a half-bridge configuration with one side on and dead time protection. It can also be configured to provide concurrent drive with the requirement to study UIS or double-pulse testing. This design can be used with most Microsemi SiC MOSFET discrete and module devices. The dead time and gate drive resistance are adjusted by the user to match the requirements of the application. Dead time protection and desaturation protection makes device evaluation easier while lowering the risk of damaging parts.

Note: The Gerber files, Verilog code, and the Libero project are available on Microsemi's website through http://www.microsemi.com/salescontacts.

This design is offered as a reference design for the evaluation of SiC devices in a laboratory environment. It has not been tested at voltage across the insulation boundaries. It is the responsibility of the engineer to use the proper safety equipment and procedures. For more information, see the appropriate UL or IEC standards for guidance on insulation and creepage requirements.

The following illustration shows a block diagram with half bridge.

Figure 1 • Block Diagram with Half Bridge



The following are two important differences to consider when comparing the drives of Si devices to those of SiC devices.

- The slew rate at the output of a SiC half bridge can be much higher than with silicon. The SiC power stages can easily achieve a dV/dt of 35 kV/µs or more. This affects the design of the gate-drive signal isolation and EMI mitigation. It creates potential issues with the implementation method of system parts, such as the gate power DC-to-DC function. The intention of this board is to provide an off-the-shelf test solution that addresses these issues.

- The SiC MOSFETs are normally driven at higher asymmetrical gate voltages when compared to silicon MOSFETs. Typically, they are driven at –5 V to 20 V. Lower positive voltages can be used if the resulting higher R_{ON} is acceptable. Lower negative drive voltages can be used, possibly down to zero. For gate drive recommendations, see Application Note AN1826.

3 Reference Design Description

The reference design is optimized to drive SiC MOSFET devices at high-speeds with desaturation protection. It is a base design that can be simplified depending upon the individual system requirements. The following is a list of features:

- Requires only a 24 V power input
- Adjustable –5 V, +20 V output gate drive
- Galvanic isolation of more than 2000 V on both gate drivers
- Capable of 6 W of gate-drive power/side (8 W with modification)
- Peak output current up to 30 A
- Maximum switching frequency greater than 400 kHz
- Single-ended or RS485/RS422 differential input gate control
- Shot-through (short-circuit) protection
- ±100 kV/µs capability
- Programmable dead time protection
- Fault signaling
- Under voltage lockout protection

Note: The board has been tested to 400 kHz. Any calculation of gate-power drive must include the frequency dependent portion of the driver IXDN630 and the ADuM4135.

This design uses an analog device (ADuM4135) to pass signals across the isolation boundary. The device is a good fit for the application, with the exception that the under voltage lockout on the gate side is nominally 11 V, which is rather low for SiC MOSFETs. The ADuM4135 has a 4 A driver. To work around the low UVLO and to increase the output current, the output is buffered through an IXDN630 driver. A zener diode is added in the positive leg of the ADuM4135 to increase the UVLO trip point to approximately 18 V.

With any gate driver, there is a need to transfer energy across the isolation interface to drive the gates. Most standard isolation supplies are not designed with adequate insulation, a low-capacitance interface, or tolerance to the high dV/dt associated with SiC MOSFETs in a half bridge. Consider that 10 pF of capacitance across the barrier translates to a 350 mA current spike back into the gate supply and its associated grounding. It is desirable to keep the capacitance across the gate supply transformer to a minimum.

Power is transferred across the isolation boundary with an LTC3999 switching IC followed by a custom transformer. Power is transferred unregulated over the boundary and then regulated on the gate side. This decouples the isolation transformer design from the regulator design.

Microsemi's FPGA controls power sequencing. In the first 0.5 second, the FPGA reduces the power available from the LTC3999. During this time, switching is blocked, hence there will be little demand for power and the LTC3999 can only deliver about 1 W. After the timeout, if there is no fault condition, power capability is increased to approximately 6 W. If at any time a fault is flagged by one of the ADuM4135s, then switching is cut off to both drivers and power is reduced. This protects the LTC3999 against a shorted load as this board is used for product development and generally should survive output device failures.

The gate power transformer is constructed from an RM8 core by Fair-rite, part number 6278230121, a bobbin by Loadstone, part number B-RM8-2-PH. The wire is by Belden, part number 8053 double insulated magnet wire. The primary is 26 turns center tapped, 26 Gauge. The secondary is 13 turns, 26 Gauge. The core is electrically conductive so some of the pins closer to the core have been removed to increase clearance. The split bobbin design results in a primary-to-secondary capacitance of only a few picofarads and provides good electrical isolation.

4 Firmware

The default firmware is configured by switches for the following two modes.

- The upper and lower drivers act independently. This allows use in applications like UIS testing, where both switches must be on simultaneously. The drive signal propagates through immediately. There is no dead time protection.
- Only one ON (half-bridge mode). With this mode, there is a switch-programmable dead time. Dead time is programmable in 100 ns steps up to 3.1 µs.

With either mode, one mode switch selects between a one-input mode and a two-input mode. This is primarily for the half-bridge mode, which makes it unnecessary to program the dead time into an external generator.

Internal logic is all driven by a 10 MHz clock. Inputs are quantized to the 10 MHz clock in half-bridge mode. The quantization to the clock makes the hold-off logic highly immune to input noise. However, it means that there will be timing jitter in the signal propagated through the FPGA.

The following table lists the configuration switch settings.

Table 1 • Configuration Switch Settings

Switch	Function
1	Switch On, signal low—2 input mode, pins 1,2 to high side, 5,6 to low side. Switch Off, signal high—1 input mode, pins 1,2
2	Switch On, signal low—80 kHz mode. Switch Off, signal high—external input mode.
3	Switch Off, signal high—one drive only, synchronous mode with dead time. Switch On, signal low—independent drive, asynchronous mode.
4	Dead time select Switch On, signal low = no delay Switch Off, signal high = 1600 ns
5	Dead time select Switch On, signal low = no delay Switch Off, signal high = 800 ns
6	Dead time select Switch On, signal low = no delay Switch Off, signal high = 400 ns
7	Dead time select Switch On, signal low = no delay Switch Off, signal high = 200 ns
8	Dead time select Switch On, signal low = no delay Switch Off, signal high = 100 ns

The FPGA is a Microsemi Igloo AGL030V2-VQ100. A Microsemi Flashpro5 programmer was used to program it. Flashpro4 should also work. The project is in Verilog using Libero SoC. For more information on IGLOO FPGAs, see http://www.microsemi.com/products/fpga-soc/fpga/igloo-overview.

Switch 1 is closest to the FPGA. The following table lists the common switch settings.

Table 2 • Common Switch Settings

Mode	SW1	SW2	SW3	Dead Time
80 kHz demo	Don’t care	ON	ON	Yes
2 input	ON	OFF	ON	Yes
1 input on high-side input only	OFF	OFF	ON	Yes
Independent	ON	OFF	OFF	N/A

The SiC MOSFETs require very little dead time. Generally, dead time corrects for the effect of gate-driver skew, the time it takes to drive the gate, and the recovery of the power device. With SiC MOSFETs, there is no recovery time. In addition, the ADuM4135 is a very low skew driver. A minimum dead time of 100 ns is possible in some applications. This would be programmed with SW4 through SW7 ON, SW8 OFF.

5 Alternate Design Options

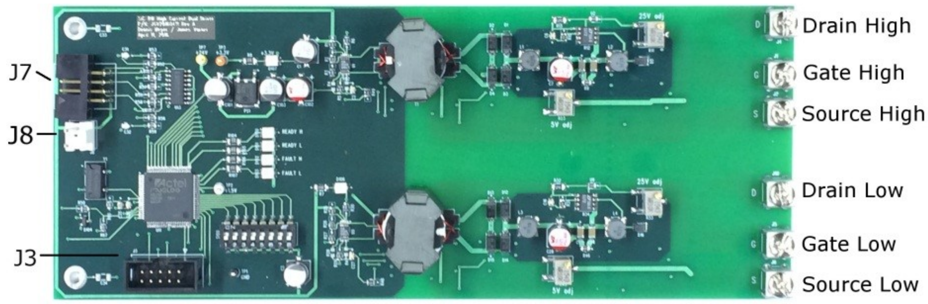
This design has integrated a substantial number of features, listed as follows. There is potential to remove some of these features where they are not needed to reduce the cost.

- The gate-power supply does not need to be adjustable. To modify it, delete D10, D21, and any associated circuitry. Replace D11 and D26 with 5.1 V-or-lower zener diodes. Remember to reduce the voltage input to the board accordingly.
- A lower power option with a lower cost is to replace the whole power supply with a module. Recon makes a series of supplies designed for SiC applications. The part numbers are RxxP22005D.
- The IXDN630 driver provides more current than most applications require. The ADuM4135 has a 4 A drive capability that can be used directly by bypassing the IXDN630. However, if this is done the zener diodes on the power legs of the ADuM4135s must be removed (D23, D24). This will lower the under voltage lockout voltage.
- The ADuM4135 can be replaced with Infineon 1EDIxxI12AF drivers. TI offers an extensive line of drivers, ISO5851, ISO5852, and UCC21520. Silicon Labs has Si8271 through Si8275. At a minimum, the driver and gate-power supply must be tolerant of >35 V/ns with a margin and it must be capable of a negative drive. This excludes most standard gate drivers.
- Multilevel drivers, such as NPC three-level power stages or matrix inverters, normally include sequencing protection within the control source (the FPGA in this case). Likewise a full-bridge driver normally sources all four drivers from one control source. In high-reliability applications, Microsemi FPGAs should be considered for their radiation tolerance and instant-on capability.

6 IO and Settings

The following illustration shows the placement of important connectors on the board.

Figure 2 • Connectors



Connector J7 is an eight-pin male header. The following table lists the J7 control connector pinout.

Table 3 • J7 Control Connector Pinout

Pin	Signal	Description
1	Drive High +	True will turn on the top side FET. Depending upon switch SW1, it can also control the low-side driver.
2	Drive High –	
3	Reset	A high (3.3 V logic) input asserts reset to the ADuM4135. Pulled down through 10K on the board.
4	Ground	Signal ground. Optionally power ground.
5	Drive Low +	Depending upon switch SW0 turns on the low-side FET.
6	Drive Low –	
7	Status	Fault output (3.3 V logic with 1K source resistance).
8	Power	24 V input.

The following table lists the J8 alternate power connector pinout.

Table 4 • J8 Alternate Power Connector Pinout

Pin	Signal
1	24
2	GND

J3 is the programming connector. The connector pinout follows the Microsemi FlashPro programmers.

6.1 LEDs and Gate Voltage Adjustments

Two power LEDs indicate the presence of 24 V and 3.3 V. Two LEDs labeled “READY H” and “READY L” indicate the current status of the ready signal from the two ADuM4135s. Two LEDs labeled “FAULT H” and “FAULT L” indicate the current status of the fault signal from the ADuM4135s.

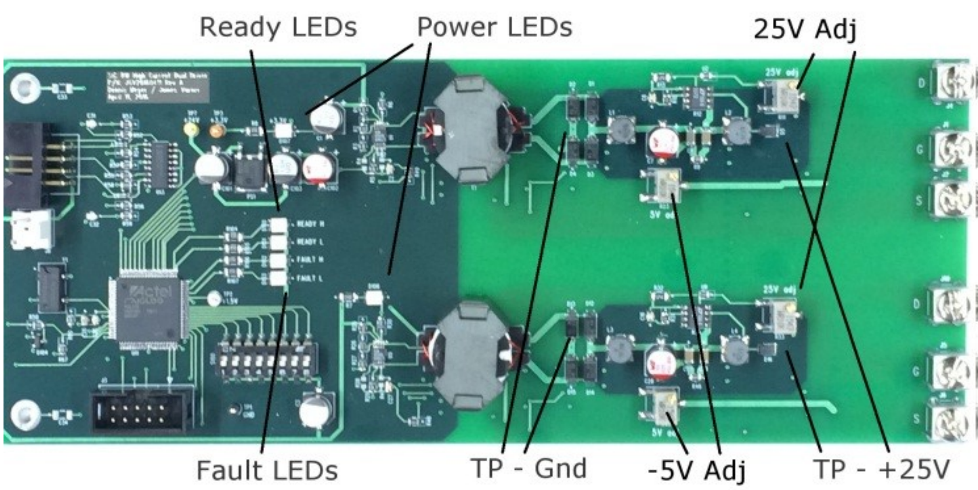
The LEDs respond as described in the following table. The status of the high-side interface and low-side interface are displayed separately.

Table 5 • LED Description

Ready	Fault	Condition
Off	Off	The secondary side is under voltage.
On	Off	Normal operating state.
On	On	Faulted due to a desaturation condition.

The following illustration shows the LEDs and the test points.

Figure 3 • LEDs and Test Points



The four test points are indicated to show the test points for the secondary side power. There is a 25 V regulator that sets the total gate drive, negative plus positive (25 V in this case). A 5 V shunt regulator then sets the negative gate drive relative to the power device source lead.

Relative to the ground reference (the inside of the two diodes on the left), the source screw terminals should measure 5 V. This is adjusted with the 5 V adj pots.

Relative to the ground reference the points labeled TP – 25 V (the right side of the diodes D5, D16) should measure 25 V. This is adjusted with the 25 V adj pots.

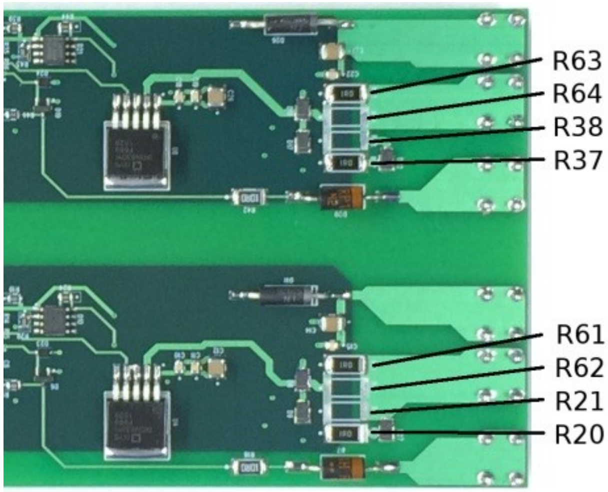
It should be noted that the board input voltage should be less than the total gate drive voltage. This is because the voltage on the secondary side of the bridge is always slightly lower than the 24 V input to the board. Boost regulators, U2 and U9, are used to generate the 25 V total gate swing. The boost regulators require that the input voltage be lower than the output voltage. In the standard configuration, the input voltage is 24 V and the output is 25 V which meets this requirement.

If the board is modified to reduce the total gate voltage, then the input voltage to the board should be reduced accordingly. For example, if the board were modified to drive 20 V/0 V by shorting D11 and D26, then the input voltage should be less than 20 V. The optimal board input voltage is 0 V–3 V below the total gate voltage.

6.2 Gate Resistor Placement

The following illustration shows the placement of the gate resistors on the back of the board. Resistor placement is the same between the rev A and rev B artwork (the rev A artwork is shown). It is expected that these will be replaced as necessary to meet the individual user requirement. For more information about the process for selecting the gate resistors, see the Quick Start (see page 15) section and Application Note AN1826.

Figure 4 • Gate Resistor Placement



The following table lists the rev A resistors grouping.

Table 6 • Rev A Artwork Gate Resistors

Location	Description
R61, R62, R21	High side ON and OFF, only R61 installed, 1 Ω
R20	High side OFF, 1 Ω
R63, R64, R38	Low side ON and OFF, only R63 installed, 1 Ω
R37	Low side OFF, 1 Ω

The following table lists the rev B resistors grouping.

Table 7 • Rev B Artwork Gate Resistors

Location	Description
R61, R62	High side ON and OFF
R21, R20	High side OFF
R63, R64	Low side ON and OFF
R38, R37	Low side OFF

7 Electrical Characteristics

The following table lists the electrical characteristics for the MSCSICMDD/REF1 device.

Table 8 • Electrical Limits

Description	Min	Typ	Max	Unit
Supply voltage, full power	20	24	25	V
Supply current, idle		0.11	0.15	A
Maximum slew rate			100	V/ns

The following table lists the status output for the MSCSICMDD/REF1 device.

Table 9 • Status Output

Description	Min	Typ	Max	Unit
Status output high, status is faulted	3.15	3.3	3.45	V
Status output low, status is OK	0.8			V
Status output impedance high or low	950	1K	1.1K	Ω

The following table lists the reset input for the MSCSICMDD/REF1 device.

Table 10 • Reset Input

Description	Min	Typ	Max	Unit
Reset input low—dis-assert reset	–0.5	0	1.0	V
Reset input high—assert reset	2.5	3.3	3.45	V
Input pull down resistance	10K	11K	12K	Ω

The following table lists the digital RS422 inputs for the MSCSICMDD/REF1 device.

Table 11 • Digital RS422 Inputs

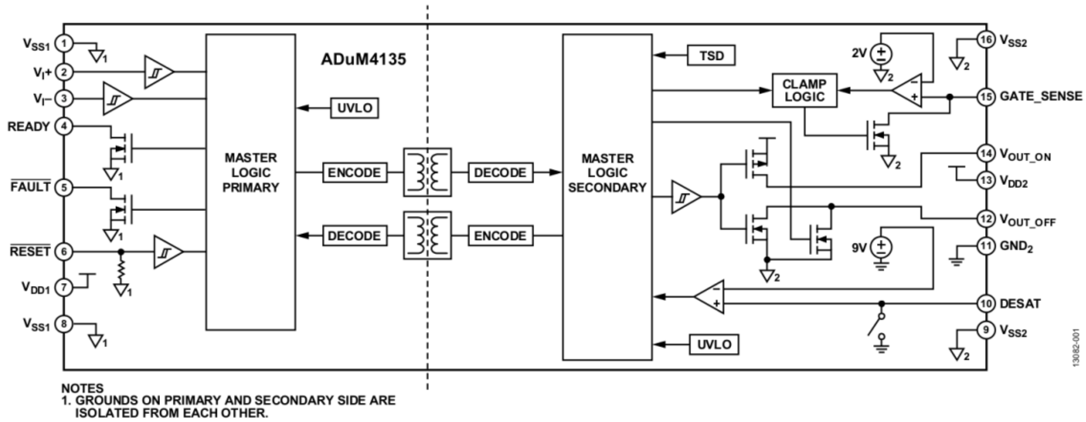
Description	Min	Typ	Max	Unit
Common mode input range	–0.5		5.5	V
Differential voltage threshold		0.050	0.200	V
Differential impedance	84	92	100	Ω
Common mode impedance	240	255	270	Ω
Common mode Thevenin voltage	1.5	1.65	1.8	V

7.1 Desaturation Protection

When a gate high is asserted, it is expected that within a few hundred nanoseconds the source-to-drain voltage across the power FET will be low. Circuitry both internal and external to the ADuM4135 verifies this and shuts off the FET if this is not the case. In many cases, it is desirable to have this function during product development even if it will not be used in the final product.

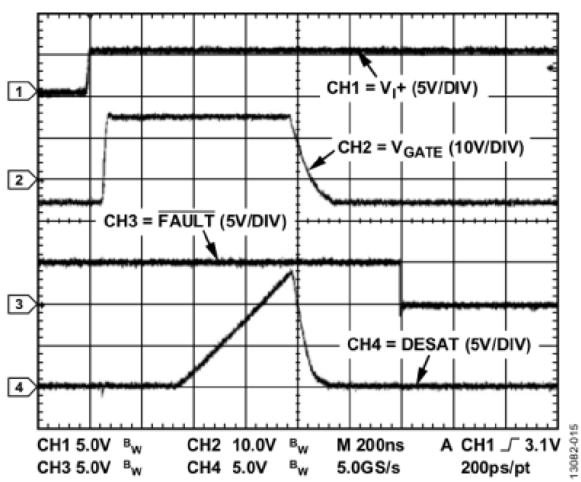
At approximately 300 ns after asserting the high-FET gate voltage, a FET internal to the ADuM4135 releases the DESAT pin. The pin is then free to float up. A 500 µA current source pulls it up. If it crosses 9 V, the ADuM4135 interprets the condition as a fault and shuts off the FET drive. The FET gating the DESAT pin is at the lower right in the following block diagram.

Figure 5 • ADuM4135 Block Diagram



In the following illustration, channel 4 shows the voltage at the DESAT pin if the pin is allowed to float.

Figure 6 • ADuM4135 Specification



The design uses a RP1HV1 diode at the connection to the drain. It is rated a maximum Vf of 7 V at 100 mA. In fact, they run about 1.0 V at 1 mA at 25 °C. This leaves 8 V of the 9 V threshold for the FET. Stated another way, the circuit will trip when the drop across the power FET exceeds approximately 8 V.

There are a number of points to consider in the design of the desat circuit.

- The RP1HV1 diode has a total capacitive charge of approx. 2.8 nC at 1000 V. The reason this matters will become apparent shortly.
- There is a diode internal to the ADuM4135 from the desat pin (10) to GND2(11).
- The fixed dead time of the ADuM4135 is 300 nS typical.
- The bias resistor that generates the 5 V negative gate drive, R19, R39, is set at 10K Ω resulting in 2 mA of Zener current.

For a desat circuit to be effective with SiC MOSFETs it should be able to respond in something on the order of 500 ns. This is not an exact number due to the variability of events leading into desat and the variability of devices to tolerate desat. 500 nS is an achievable number because with the switching speed of SiC the drain should settle within less than 200 nS typically. The 300 nS dead time of the ADuM4135 leaves 200 nS for the circuit to respond.

In the current design most of the capacitive current of the RP1HV1 diode is directed through the MBD7000 diodes to the gate supplies. Note that the low side diode clamps to the V_{EE} rail. During the time that the drain is slewing negative, the low side diode goes into conduction. In the Rev A board, it was left to the user to design the circuit. In the Rev B board, values are used that are more realistic for a functioning desat circuit. In the rev B board, the resistor from the MBD7000 diodes to the ADuM4135 is 100 Ω. This means that roughly 50 mA of current will pull down the desat pin through the GND2 pin during the switching event when the drain slews negative.

If all of the diode currents were directed to the desat pin, then at 500 kHz the desat pin internal diode will be absorbing 2.8 nC * 5e5 = 1.4 mA. This 1.4 mA takes current from the Zener clamp resulting in 2 mA – 1.4 mA = 0.6 mA of Zener current. If the frequency is a little higher, this can result in a collapse of the Zener voltage. The 10K Ω resistors bias for the Zener should be lowered if this is of concern.

A SBD clamp from pin 10 to 11 on the ADuM4135 will prevent internal diode conduction. The ADuM4135 can latch up with excessive diode current. At this time there is not a specification for the maximum diode current.

8 Board Mounting

The board has four #6 mounting screws. There are two screws near the Microsemi FPGA that provide optional grounding of the switching currents to a chassis. They direct switching currents from the isolation interface to the chassis. Without these screws, the currents are directed through the signal input and power cable. This results in much higher emissions and can interfere with control.

There are two #6 screw holes in the high-voltage area. These should be nylon. They do not have sufficient creepage for the voltages involved.

To minimize gate-drive inductance the board should be mounted no more than a few inches from the SiC MOSFETs. To minimize inductance at greater distances use large diameter wire and twist the wire to the source/drain connection. For more information and recommendations, see Application Note AN1826
.

9 Quick Start

The basic functionality of the board can be tested without a connection to power circuitry. To do this, the short circuit protection circuitry must first be disabled.

The following steps are to test the board without power circuitry connected.

1. At the screw terminals jumper Source High to Drain High, see Figure 2 (see page 8).
2. At the screw terminals jumper Source Low to Drain Low.
3. Set switches 2 and 3 to ON, see Table 2 (see page 6). This selects 80 kHz self-clocking mode. The dead time switches (4–8) can be set as required.
4. Apply 14 V–24 V power at J8 (J7–J8 is preferred). The loading should be approximately 0.11 A without FETs. With FETs, there is the additional power required for the gates.

The gate drive can then be observed at the screw terminals.

The following are requirements for normal use.

- Mount the board with metal screws on the control side and nylon on the high-voltage side.
- Select the gate resistors as required. For more information on gate resistors, see Application Note AN1826.

Note: C33 and C34 connect the board SELV side ground to the chassis. These capacitors direct switching currents conducted across the isolation interface to the chassis, thus steering them away from the signal cables. Their use is recommended. Some early board revisions may not have them installed.

Note: R4 and R28 limit the LT3999 power to 6 W to protect the LT3999 in the event of a shorted load. Without them, the LT3999s will deliver 8 W, but it is not as tolerant of overload as a result of power stage failure. Their use is recommended. Some early board revisions did not have these resistors.

The board comes with very low-gate resistors installed. It is best to use the lowest possible gate resistance to get the fastest switching and lowest associated switching loss. However, this is subject to the following conditions.

- The gate resistor should be high enough that there is no excessive ringing and overshoot with the given drive circuit inductance.
  When using an oscilloscope, it is recommended to measure only across the gate/source of the low side transistor. The design is symmetrical and it can be assumed the high side looks the same. The scope probes generally cannot measure the gate/source voltage of the high-side device due to the high-slew rate.
- The gate-drive impedance should be low enough that the Miller effect does not drive a transistor into conduction.
  To measure the effect of Miller capacitance, place a scope to observe the gate/source voltage on the low side power device. Observe at the time of the rising edge of a half-bridge output with no load on the output. When there is no load on a half bridge, the rising edge at the output occurs when the top-side device turns on. At that point, the low-side device has been off for the dead time. The positive induced voltage at the gate should be no more than a few volts.
- Sometimes the gate-drive impedance must be raised to limit the switching speed at the output to limit voltage overshoot at the output.

If a design has excessive gate inductance, these requirements will conflict. In that case, a series RC network is added across the source/gate leads to lower the impedance observed by the FET.

The board has a 1 Ω resistor installed in both the locations to turn on and off assistance. In most cases, this will result in quite a bit of ringing but will not overvoltage the gate. There are locations for an optional second set of resistors for use in the event a very high-gate drive power is used. The following table lists the recommended value to start with.

Table 12 • Recommended Initial Gate Resistors

Part Number	R20, R37, R61, R63
MSC025SMA120	3.3 Ω
MSC040SMA120	5 Ω
MSC080SMA120	7.5 Ω
MSC140SMA120	10 Ω
MSC280SMA120	10 Ω
MSC015SMA070	3.3 Ω
MSC035SMA070	5.0 Ω
MSC060SMA070	7.5 Ω
MSC090SMA070	7.5 Ω

Values in this table are not critical. A few volts of overshoot will have little effect on the reliability of the devices. It is important that the board is close to the devices to avoid losses due to the Miller effect coupling into the gate due to inductance between the gate and the gate driver.

10 Bill of Materials

The following table lists the bill of materials for the MSCSICMDD/REF1 device.

Table 13 • Bill of Materials

Item	Reference	Manufacturer	Part Number	Description	Quantity
1	C33-34	DNP	DNP	Placeholder for 1206 component	2
2	J9, J11	Keystone Electronics	1650-2	ROUND STANDOFF 4-40 BRASS 1 /4"	2
3	D11, D26	ON Semiconductor	1N5342BRLG	DIODE ZENER 6.8 V 5 W AXIAL	2
4	J3	On Shore Technology Inc.	302-S101	CONN HEADER VERT 10POS GOLD	1
5	TP1	Keystone Electronics	5001	TEST POINT PC MINI 0.040" D black	1
6	TP2	Keystone Electronics	5002	TEST POINT PC MINI 0.040" D WHITE	1
7	TP3	Keystone Electronics	5003	TEST POINT PC MINI 0.040" D ORANGE	1
8	TP7	Keystone Electronics	5004	TEST POINT PC MINI 0.040" D YELLOW	1
9	J7	Wurth Electronics Inc.	61200821721	CONN HEADER 8 POS RA 2.54	1
10	T1-2	Far-rite	6278230121	Ferrite core	4
11	T1-2	Loadstone Pacific	B-RM8-2-H	Split bobbin	2
12	T1-2	Belden	8053	26 Ga WIRE	
13	J1-2, J4-6, J10	Keystone Electronics	8191	TERMINAL SCREW VERTICAL PC MNT	6
14	R11, R23, R33, R43	TT Electronics/BI	84WR10KLF	TRIMMER 10K Ω 0.25 W SMD top adj	4
15	C7, C28, C102	Wurth Electronics Inc.	8.6506E+11	CAP 100 µF 20% 25 V	3
16A	J8 (Rev A Assy)	TE Connectivity AMP Connectors	A1971-ND	CONN HEADER VERT 2POS .156 TIN	1
16B	J8 (Rev B Assy)	Phoenix Contact	5442756	CONN 2 POS SCREW	1
17	U3, U6	Analog Devices Inc.	ADUM4135BRWZ	DGTL ISO 4 A GEN PURP SOIC	2
18	U11	Microsemi SoC	AGL030V2-VQG100	IC FPGA 77 I/O 100VQFP	1
19	U13	Texas Instruments	AM26LV32CDR	IC QUAD DIFF LINE RCVR 16-SOIC	1
20	D23-24	NXP Semiconductors	BZX84J-C6V2,115	DIODE ZENER 6.2 V 550 MW SOD323F	2
21	C31-32	Kemet	C0805C101K3GACTU	CAP CER 100 PF 25 V 10% NP0 0805	2
22	C13	Kemet	C0805C103K5RACTU	CAP CER 10000 PF 50 V X7R 0805	1
23	C2, C6, C16, C27	Kemet	C0805C104K3RACTU	CAP CER 0.1 µF 25 V X7R 0805	4
24	C9-11, C15, C17-19, C22	Kemet	C0805C104M5RACTU	CAP CER 0.1 µF 50 V X7R 0805	8
25	C29	Kemet	C0805C105M3RACTU	CAP CER 1 µF 25 V X7R 0805	1
26	C30	Kemet	C0805C225K9RACTU	CAP CER 2.2 µF 6.3 V X7R 0805	1
27	C20	Kemet	C0805C334K5RACTU	CAP CER 0.33 µF 50 V X7R 0805	1

Item	Reference	Manufacturer	Part Number	Description	Quantity
28	C8, C23 (Rev A Assy Only)	Kemet	C1206C101M5GACTU	CAP CER 100 PF 50 V NP0 1206	2
29	D1-4, D12-15	Central Semiconductor Corp	CMSH1-200HE TR13	DIODE SCHOTTKY 200 V 1 A SMA	8
30A	R16, R40 (Rev A Assy)	Vishay Dale	CRCW12061M00JNEAHP	RES SMD 1M Ω 5% 1/2 W 1206	2
30B	R16, R40 (Rev B Assy)	Vishay Dale	CRCW120610K0JNEAHP	RES SMD 10K Ω 5% 1/2 W 1206	2
31	L5-6	Murata North America	DLP11SN201HL2L	CHOKE COIL COMMON MODE 110 MA SMD	2
32	C35	Murata North America	GRM21BR61E106KA73L	CAP CER 10 µF 25 V X5R 0805	1
33	C36	Murata North America	GRM21BR71E104KA01L	CAP CER 0.1 µF 25 V X7R 0805	1
34	U4, U8	IXYS	IXDN630YI	IC GATE DRIVER LOW SIDE 5TO263	2
35	S100	E-Switch	KAE08LGGT	SWITCH DIP 25 MA 8 POS GOLD 24 V	1
36	PS1	STMicroelectronics	LD1086DT33TR	IC REG LDO 3.3 V 1.5 A DPAK	1
37	D100-103	OSRAM Opto Semi Inc.	LG T67K-H2K1-24-Z	LED GREEN CLEAR 2PLCC SMD	4
38	D107	OSRAM Opto Semi Inc.	LO T67K-K1L2-24-Z	LED ORANGE CLEAR 2PLCC SMD	1
39	U2, U9	Linear Technology	LT1172HVCQ#PBF	IC REG MULT CONFG INV ADJ 5DDPAK	2
40	U12	Linear Technology	LT3007ITS8-1.5 #TRMPBF	IC REG LDO 1.5 V 20 MA TSOT23-8	1
41	U1, U5	Linear Technology	LT3999HMSE#PBF	IC REG PSH-PLL ISO ADJ 1 A 10MSOP	2
42	D106	OSRAM Opto Semi Inc.	LY T67K-J2L1-26-Z	LED YELLOW CLEAR 2PLCC SMD	1
43	D6, D19, D104	ON Semiconductor	MMBD7000LT1G	DIODE ARRAY GP 100 V 200 MA SOT23	3
44	L1-4	Bourns Inc.	PM54-101K-RC	FIXED IND 100 µH 520 MA 700 MΩ	4
45	R21, R38, R62, R64		DNP	Place holder for 2512 component	4
46	R4, R28, R47, R82	Stackpole Electronics Inc.	DNP	0605 do not place resistor	4
47	R65-66	Stackpole Electronics Inc.	RMCF0603JT1K00	RES SMD 1K Ω 5% 1/10 W 0603	2
48	R3, R27, R60	Stackpole Electronics Inc.	RMCF0805FT10R0	RES SMD 10 Ω 1% 1/8 W 0805	3
49	R12, R34	Stackpole Electronics Inc.	RMCF0805FT15K8	RES SMD 15.8K Ω 1% 1/8 W 0805	2
50	R48-49	Stackpole Electronics Inc.	RMCF0805FT20K0	Resistor 1/8 W 1% 0805 SMD	2
51	R22, R45	Stackpole Electronics Inc.	RMCF0805FT20R0	RES SMD 20 Ω 1% 1/8 W 0805	2
52	R6, R30	Stackpole Electronics Inc.	RMCF0805FT49K9	RES SMD 49.9K Ω 1% 1/8 W 0805	2
53	R24, R44	Stackpole Electronics Inc.	RMCF0805FT4K99	RES SMD 4.99K Ω 1% 1/8 W 0805	2

Item	Reference	Manufacturer	Part Number	Description	Quantity
54	R52, R54-56	Stackpole Electronics Inc.	RMCF0805FT510R	RES SMD 510 Ω 1% 1/8 W 0805	4
55	R53, R57-59	Stackpole Electronics Inc.	RMCF0805FT51R0	RES SMD 51 Ω 1% 1/8 W 0805	4
56	R1, R25	Stackpole Electronics Inc.	RMCF0805FT68K0	RES SMD 68K Ω 1% 1/8 W 0805	2
57	R5, R29	Stackpole Electronics Inc.	RMCF0805JT100K	RES SMD 100K Ω 5% 1/8 W 0805	2
58	R2, R19, R26, R39, R67	Stackpole Electronics Inc.	RMCF0805JT10K0	RES SMD 10K Ω 5% 1/8 W 0805	5
59	R50-51	Stackpole Electronics Inc.	RMCF0805JT1K00	RES SMD 1K Ω 5% 1/8 W 0805	2
60A	R17, R41 (Rev A Assy)	Stackpole Electronics Inc.	RMCF0805JT1K00	RES SMD 1K Ω 5% 1/8 W 0805	2
60B	R17, R41 (Rev B Assy)	Stackpole Electronics Inc.	RMCF0805JT100R	RES SMD 100 Ω 5% 1/8 W 0805	2
61	R9, R46	Stackpole Electronics Inc.	RMCF0805JT1R00	RES SMD 1 Ω 5% 1/8 W 0805	2
62A	R10, R31 (Rev A Assy)	Stackpole Electronics Inc.	RMCF0805ZT0R00	RES SMD 0.0 Ω JUMPER 1/8 W 0805	2
62B	R10 R31 (Rev B Assy)	Stackpole Electronics Inc.	RMCF0805JT10K0	RES SMD 10K Ω 5% 1/8 W 0805	2
63	R7	Stackpole Electronics Inc.	RMCF1206FT14K3	RES SMD 14.3K Ω 1% 1/4 W 1206	1
64	R13, R32	Stackpole Electronics Inc.	RMCF1206FT1K24	RES SMD 1.24K Ω 1% 1/4 W 1206	2
65	R8, R104-107	Stackpole Electronics Inc.	RMCF1206JT150R	RES SMD 150 Ω 5% 1/4 W 1206	5
66	R20, R37, R61, R63	Stackpole Electronics Inc.	RMCF2512JT1R00	RES SMD 1 Ω 5% 1 W 2512	4
67	R18, R42	Stackpole Electronics Inc.	RMCP2010FT10R0	RES SMD 10 Ω 1% 1 W 2010	2
68	R14-15, R35-36	Stackpole Electronics Inc.	RNCP1206FTD10R0	RES SMD 10 Ω 1% 1/2 W 1206	4
69	D7, D20	Sanken	RP 1HV1	DIODE GEN PURP 2 kV 100 MA AXIAL	2
70	Y1	EPSON	SG-636PCE 10.0000 MC0:ROHS	OSC XO 10.000 MHZ CMOS SMD	1
71	D5, D8-9, D16-18, D22, D27	Vishay Semiconductor Diodes Division	SS3P4-M3/84A	DIODE SCHOTTKY 40 V 3 A DO220AA	8
72	D10, D21	Texas Instruments	TL1431CDR	IC VREF SHUNT ADJ 8SOIC	2
73	C4-5, C24-25	Taiyo Yuden	UMK316BBJ106ML-T	CAP CER 10 µF 50 V X5R 1206	4
74	C12, C26	Taiyo Yuden	UMK325AB7106MM-T	CAP CER 10 µF 50 V X7R 1210	2
75	C21, C14	Taiyo Yuden	UMK325AB7106MM-T	CAP CER 10 µF 50 V X7R 1210	2
76	C1, C3, C101, C103	Nichicon	UUD1H100MCL1GS	CAP ALUM 10 µF 20% 50 V SMD	4
77	Across C12 C26 (Rev B Assy)	Nichicon	TVX1V470MAD1LV	CAP ALUM 47UF 20% 35V RADIAL	2

11 Schematics

The following illustrations show the schematics of the MSCSICMDD/REF1 device.

Figure 7 • Low-Voltage Area

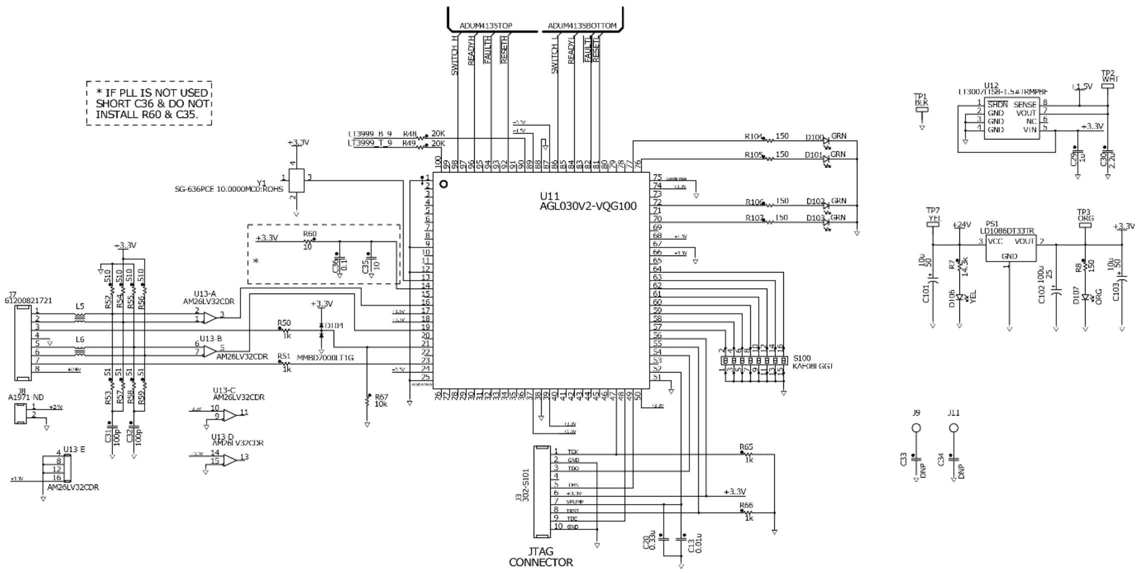
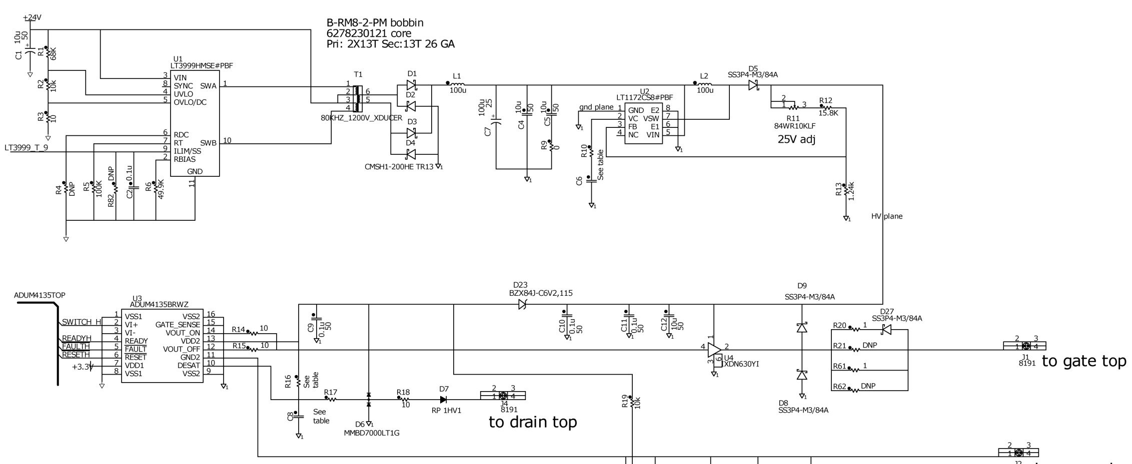
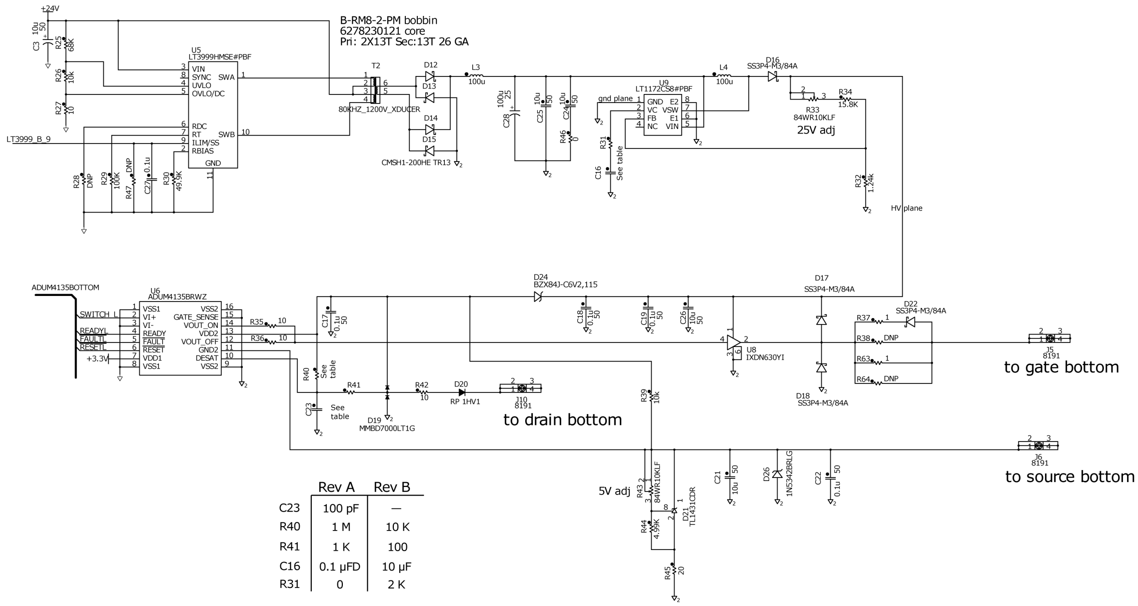


Figure 8 • High-Voltage Plane Top



	Rev A	Rev B
C8	100 pF	—
R16	1 M	10 K
R17	1 K	100
C6	0.1 μFD	10 μF
R10	0	2 K

Figure 9 • High-Voltage Plane Bottom



	Rev A	Rev B
C23	100 pF	—
R40	1 M	10 K
R41	1 K	100
C16	0.1 µFD	10 µF
R31	0	2 K

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