MX77

Ultra-Low Jitter Clock Oscillator with Integrated Quartz Crystal

Features

- Generates Differential or Single-Ended Output
- 85 fs (typ.) Phase Jitter @ 156.25 MHz (12 kHz to 20 MHz)
- 80 fs (typ.) Phase Jitter @ 312.5 MHz (12 kHz to 20 MHz)
- 12 On-Chip Power Supply Regulators for Excellent Power Supply Noise Immunity >-75dB Suppression
- Integrated Quartz Crystal for Superior Reliability, Noise/Jitter Performance
- Excellent Close in Phase Noise
- Independently Programmable Output Logic:
  - Output Logic: LVPECL, LVDS, HCSL, LVCMOS
- 2.5V to 3.3V Operating Power Supply
- Industrial Temperature Range, –40°C to +85°C
- Green, RoHS, and PFOS Compliant QFN
- Industry Standard 6-Pin, 5 mm x 7 mm Package
- Moisture Sensitivity Level (MSL): Level-1

Applications

- 10/40/100/400 Gigabit Ethernet - (GMII)
- SONET/SDH
- PCI-Express Gen 1/2/3/4/5/6 Compliant
- CPRI/OBSAI - Wireless Base Station
- Fibre Channel
- HDMI/HDTV 4K/8k
- DIMM (DDR2-3-4/AMB)
- High Speed ADC/DAC
- Optical Network (OTN, DCI)

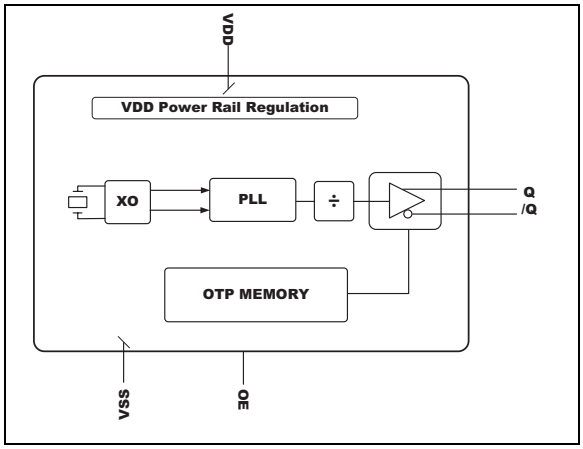
General Description

The MX77XXXX series are a family of PLL clock oscillators plus integrated quartz crystal that achieves ultra-low phase jitter (<90 fs_{RMS} typical, 12.5 MHz up to 875 MHz).

The output can be programmed to LVPECL, LVDS, HCSL, or LVCMOS logic.

The MX77 is packaged in a standard 6-pin LGA.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage, (V_{DD}) .....+4.6V
Input Voltage, (V_{IN}).....–0.50V to V_{DD} +4.6V
ESD Protection (HBM) .....2 kV
ESD Protection (MM) 200V

Operating Ratings ††

Supply Voltage (V_{DD})..... +2.375V to +3.465V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, typical values are for T_A = +25°C. The min. and max. values are for –40°C ≤ T_A ≤ +85°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.375	2.5	2.625	V	2.5V Operation
		3.135	3.3	3.465		3.3V Operation
Current Consumption	I_{DD}	—	135	180	mA	@3.3V

LVPECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±5% to 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO} – 2V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	V_{DDO} – 1.35	V_{DDO} – 1.01	V_{DDO} – 0.8	V	50Ω to V_{DDO} – 2V
Output Low Voltage	V_{OL}	V_{DDO} – 2	V_{DDO} – 1.78	V_{DDO} – 1.6	V	50Ω to V_{DDO} – 2V
Peak-to-Peak Output Voltage	V_{SWING}	0.65	0.77	0.95	V	Figure 5-3, Figure 5-6

LVDS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±5% to 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 100Ω between Q and /Q.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Differential Output Voltage	V_{DD}	2.45	350	454	mV	Figure 5-3, Figure 5-8
Common Mode Voltage	V_{CM}	1.125	1.2	1.375	V	Figure 5-3, Figure 5-8
Output High Voltage	V_{OH}	1.248	1.375	1.602	V	Figure 5-3, Figure 5-8
Output Low Voltage	V_{OL}	0.898	1.025	1.252	V	Figure 5-3, Figure 5-8

HCSL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±5% to 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{SS}.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	660	700	850	mV	Figure 5-3, Figure 5-7
Output Low Voltage	V_{OL}	–150	0	27	mV	Figure 5-3, Figure 5-7
Crossing Point Voltage	V_{CROSS}	—	350	—	V	Figure 5-3, Figure 5-7

LVCMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±5% to 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to $V_{DDO}/2$. Figure 5-3, Figure 5-9

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	V_{DD} – 0.8	—	—	V	Medium Drive (Default)
Output Low Voltage	V_{OL}	—	—	0.5	V	—
Input High Voltage	V_{IH}	V_{DD} – 0.7	—	V_{DD} + 0.3	V	—
Input Low Voltage	V_{IL}	V_{SS} – 0.3	—	0.3 x V_{DD}	V	—
Input High Current	I_{IH}	—	—	5	µA	V_{DD} = V_{IN} = 3.465V
Input Low Current	I_{IL}	–150	—	—	µA	V_{DD} = 3.465V, V_{IN} = 0V

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±5% to 2.5V ±5%, V_{DD} = 3.3V ±5%, $V_{DDO}1/2$ = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output Frequency	F_{OUT}	12.5	—	875	MHz	LVPECL, LVDS, HCSL
		12.5	—	400	MHz	LVCMOS
Output Rise/Fall Time Note 1	t_R/t_F	85	135	350	ps	LVPECL output
		85	140	300		LVDS output
		175	200	400		HCSL output
		100	200	400		LVCMOS output (default drive)
Output Duty Cycle	ODC	45	50	55	%	All output frequencies
		48	50	52	%	< 450 MHz output frequencies
PLL Lock Time	T_{LOCK}	—	5	20	ms	Time from 90% V_{DD}
RMS Phase Jitter Note 2, Figure 5-5	$t_{JIT}(\Phi)$	—	85	—	fs	156.250 MHz, Integration range (12 kHz - 20 MHz)
			85	—		156.250 MHz, Integration range (1.875 MHz - 20 MHz)

Note 1: See Figure 5-4.

2: All phase noise measurements were taken with an Agilent 5052B phase noise system.

3: The CMOS driver can deliver usable waveforms up to ~ 600 MHz under light loading and CL below 5 pf. Careful attention to signal integrity, transmission line design, VIA's and signal termination must be followed. VIA design is very important and has the most effect on the waveform.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	—	—	—	+265	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Case Temperature	—	—	—	+115	°C	—
Package Thermal Resistance						
Junction Thermal Resistance 7 mm x 5 mm LGA	θ_{JA}	—	52.8	55	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Pin Level	Description
1	OE	I, (SE)	LVCMOS	Output Enable, Disable to tri-state (on-chip 75 kΩ pull-up)
2	NC	—	—	No Connect No internal connections to the ASIC are made
3	GND-VSS	PWR	—	Power Supply Ground
4	Q1	O, (DIF/SE)	LVPECL, LVDS HCSL, LVCMOS (Q only	Differential / SE Clock Output (LVCMOS)
5	Q1/			
6	VDD	PWR	—	Power Supply

TABLE 2-2: TRUTH TABLE

Output Enable	OE = Pin 1	OE Default State
Enable Pin option	B	—
Output Logic Type	A= PECL B=LVDS C=CMOS D=HCSL	Active high
	F=PECL G=LVDS H=CMOS J=HCSL	Active low

3.0 PHASE NOISE PERFORMANCE

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

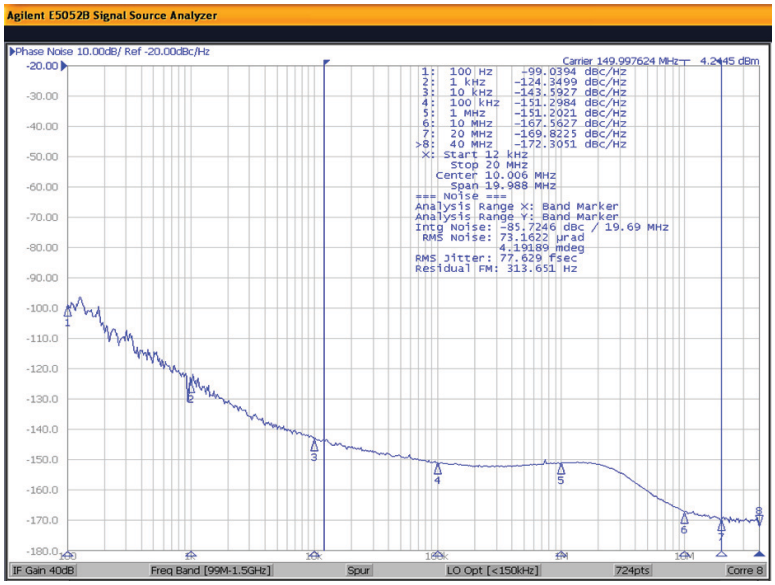


FIGURE 3-1: *150.0000 MHz, HCSL, Integration Range 12 kHz to 20 MHz: 77.6 fs_{RMS}.*

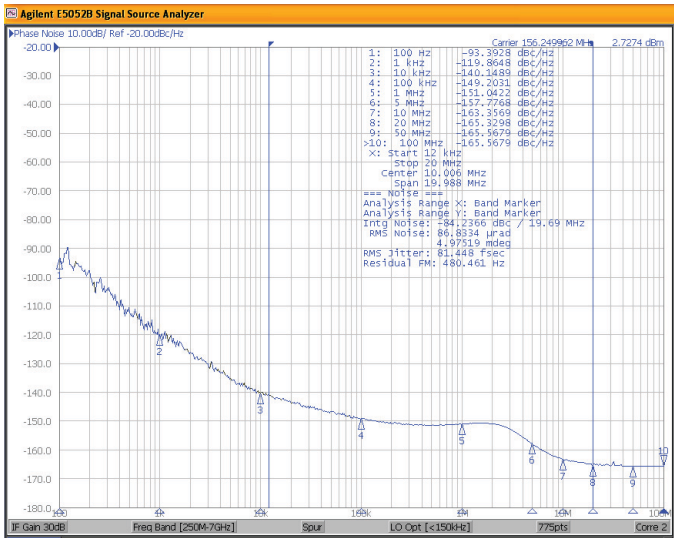


FIGURE 3-2: *156.250 MHz, LVPECL, Integration Range 12 kHz to 20 MHz: 82 fs_{RMS}.*

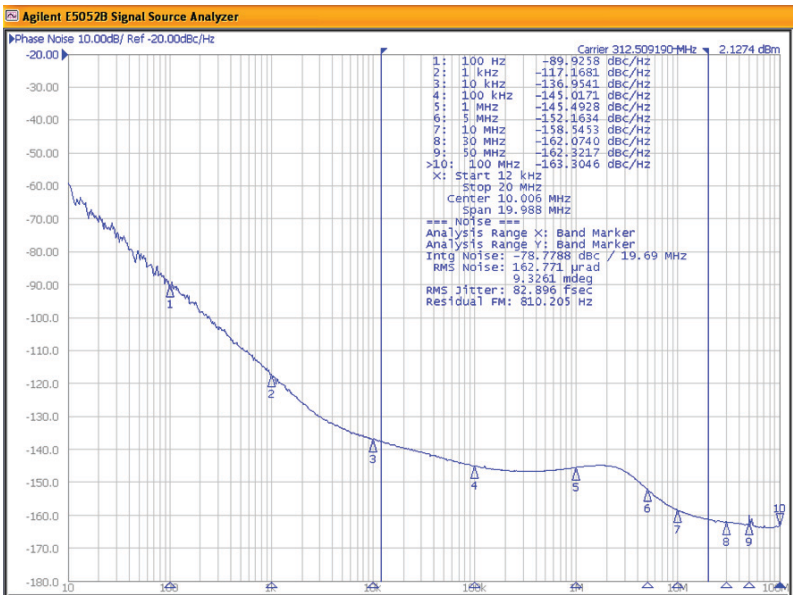


FIGURE 3-3: *312.500 MHz, LvPecl. Integration Range 12 kHz to 20 MHz: 83 fs_{RMS}.*

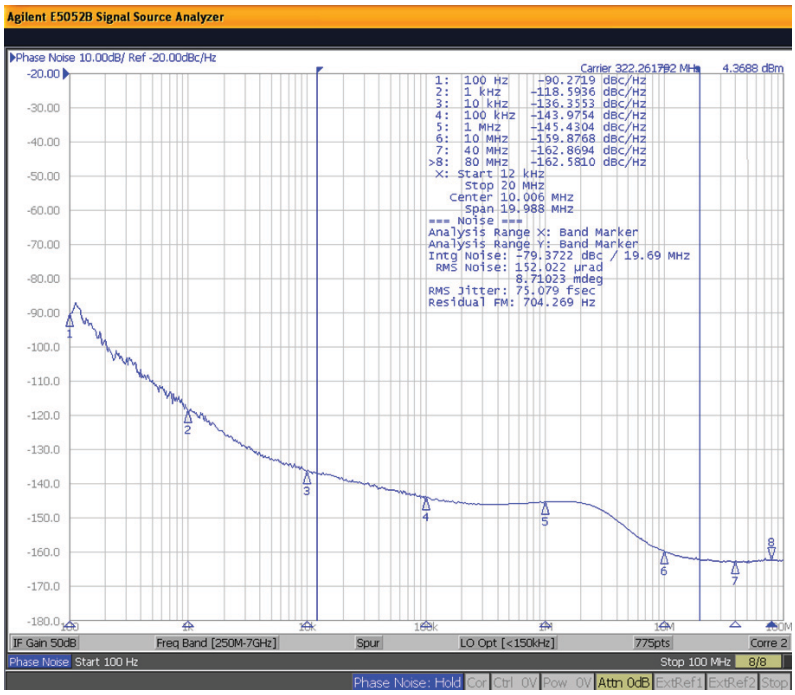


FIGURE 3-4: *322.265625 MHz, LVPECL Integration Range 12 kHz to 20 MHz: 75 fs_{RMS}.*

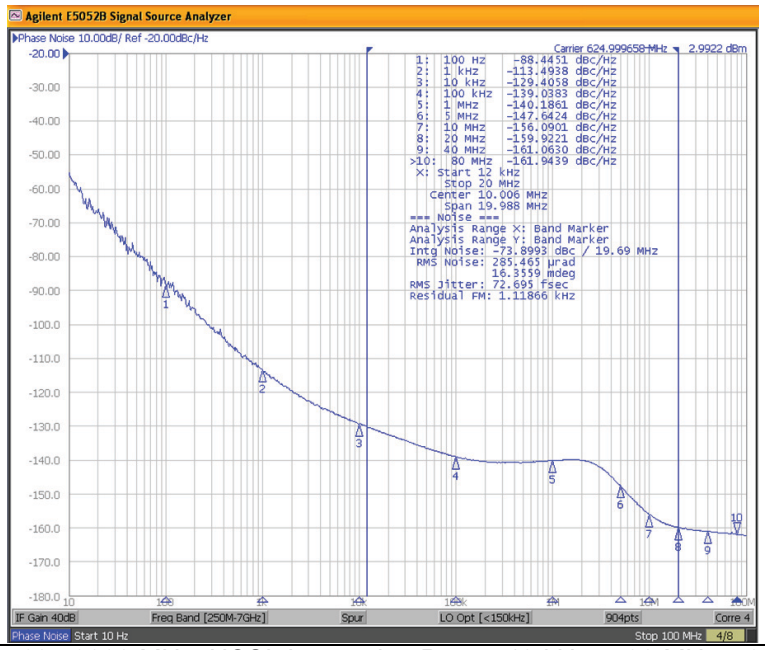


FIGURE 3-5: *625.0000 MHz, HCSL Integration Range 12 kHz to 20 MHz: 72.7 fs_{RMS}.*

4.0 KEY PROGRAMMABLE PARAMETERS

4.1 Frequency Settings for One PLL and One Output Bank

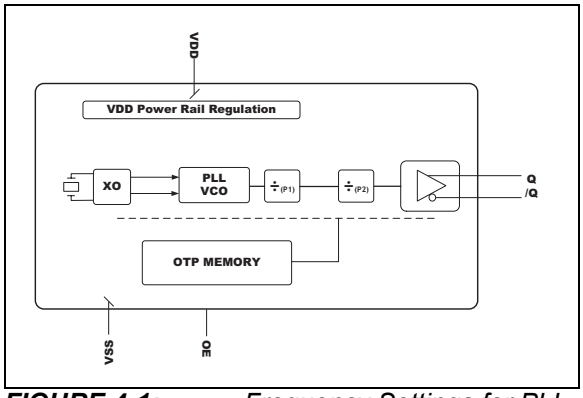


FIGURE 4-1: *Frequency Settings for PLL and Output Bank.*

The crystal reference frequency is integer multiplied to fall within the VCO capture range and the post dividers divide the VCO back down to the required frequency.

The VCO has a range of 2875 MHz to 3540 MHz.

Counters M and P0 have a range of 4 to 259.

Counter P1 has a range of 1 to 16.

EQUATION 4-1:

$$F_{VCO} = REF \times M$$

EQUATION 4-2:

$$Q1 = F_{VCO} \div (P0 \times P1)$$

4.2 Output Logic Programming

The output can be programmed to one of four logic types, LVPECL, LVDS, HCSL, and LVCMOS.

All logic types are differential except LVCMOS. For LVCMOS, only the true channel of the output pair is enabled, and the complementary channel is disabled, HiZ. With LVCMOS there is also an output drive setting, 3 bits, that can be set to adjust edge rate.

These bits are set at the factory and depend on customer application, frequency, loading and EMI.

The default setting is 4.

5.0 APPLICATION INFORMATION

5.1 Output Traces

Design the output signal traces according to the output logic requirements, terminations, etc. These are high edge rate signals so care must be taken in the PCB layout/traces, use best SI practices. If LVCMOS is unterminated at the destination device and the trace length is 1/4 λ or longer add a ~30Ω resistor in series with the oscillator output and as close as possible to the output pin. Then start a 50Ω trace to the clock consumer device.

For differential traces you can either use a differential design or two separate 50Ω traces. For EMI reasons, it is better to use a balanced differential transmission line design.

LVDS can be AC-coupled or DC-coupled to its termination.

5.2 Power Supply Filtering Recommendations

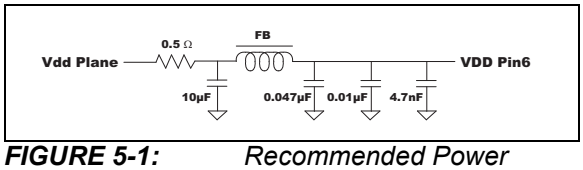


FIGURE 5-1: *Recommended Power Supply Filtering.*

- Use the power supply filtering shown in Figure 5-1 for V_{DD}.
- Connect V_{SS} (GND) pin directly to the ground power plane.
- Recommended ferrite bead properties are 80Ω to 240Ω impedance @100 MHz and >250 mA saturation current.
- To improve power supply filtering beyond what a ferrite bead Pi filter can provide, the Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in Figure 5-2 and can be used along with any of the above V_{DD} sections except V_{DDO}.

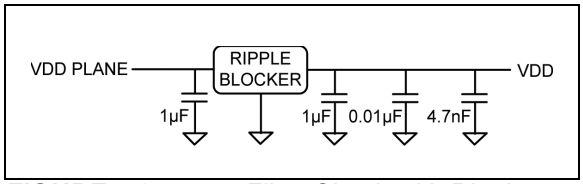


FIGURE 5-2: *Filter Circuit with Ripple Blocker.*

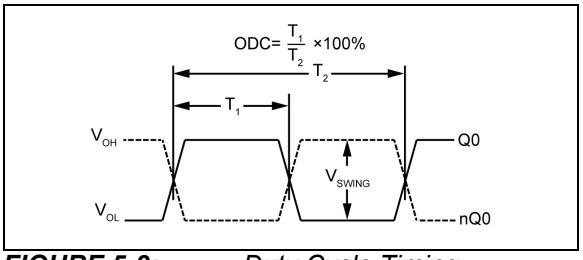


FIGURE 5-3: *Duty Cycle Timing.*

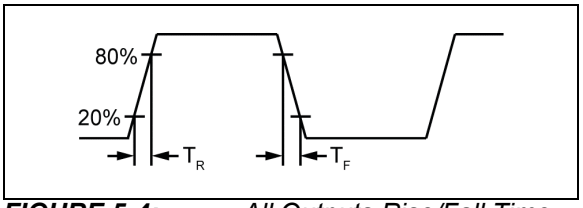


FIGURE 5-4: *All Outputs Rise/Fall Time.*

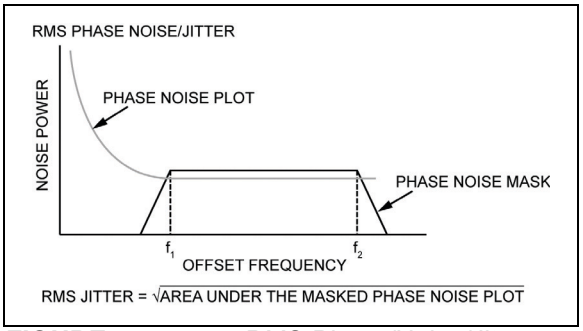


FIGURE 5-5: *RMS Phase/Noise/Jitter.*

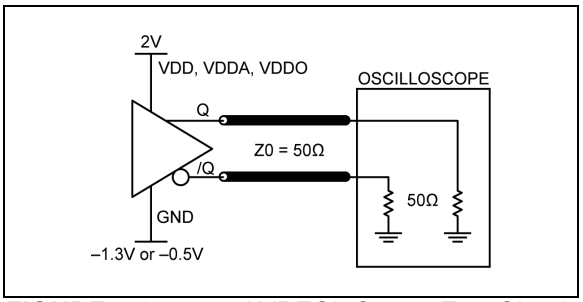


FIGURE 5-6: *LVPECL Output Test Circuit.*

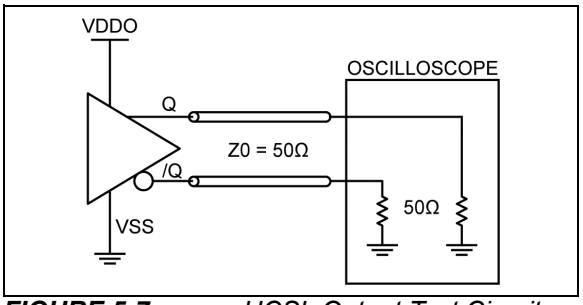


FIGURE 5-7: *HCSL Output Test Circuit.*

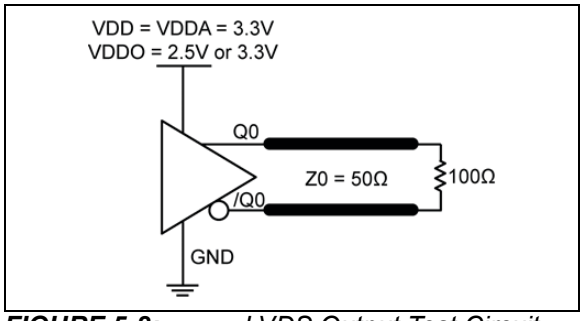


FIGURE 5-8: *LVDS Output Test Circuit.*

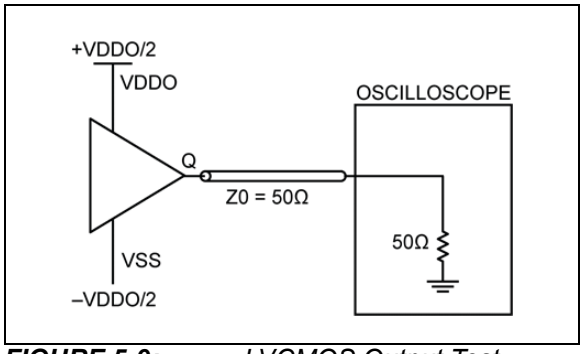


FIGURE 5-9: *LVCMOS Output Test Circuit.*

5.3 HCSL Source Terminated Per JESD8-18A

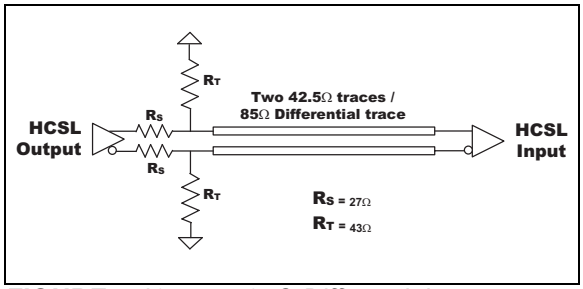


FIGURE 5-10: *85Ω Differential Transmission Line.*

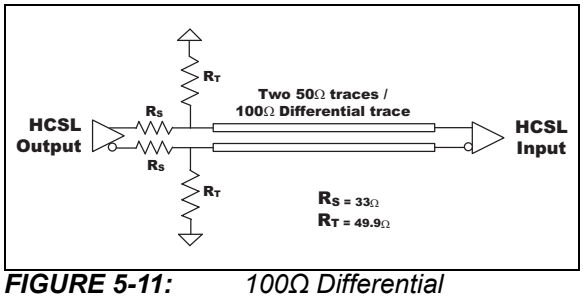


FIGURE 5-11: *100Ω Differential Transmission Line.*

Environmental Specifications

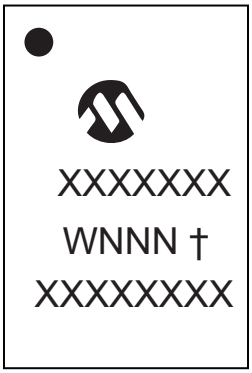
TABLE 5-1: ENVIRONMENTAL SPECIFICATIONS

Parameter	Specification
Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method1004
Mechanical Shock	MIL-STD-883, Method 2022, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition B
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free Devices (Except 2 Cycles Max)
Hazardous Substance	Pb-Free/RoHS/Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1 = $2x10^{-8}$ ATM CC/S
Solvent Resistance	MIL-STD-202, Method 215

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

6-Pin LGA*
5 mm x 7 mm



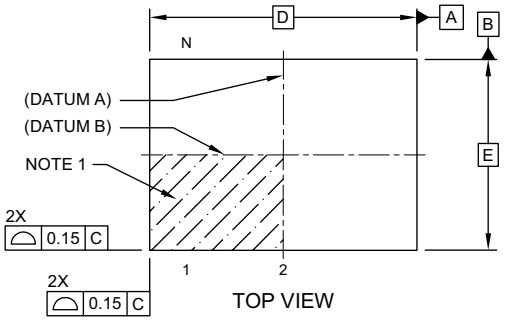
Example

Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

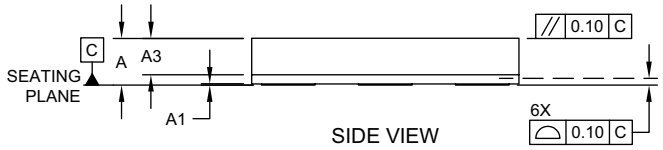
6-Lead Low 7 mm x 5 mm LLGA Package Outline and Recommended Land Pattern

6-Lead Low Profile Land Grid Array (LLX) - 5x7x1.22 mm Body [LLGA]

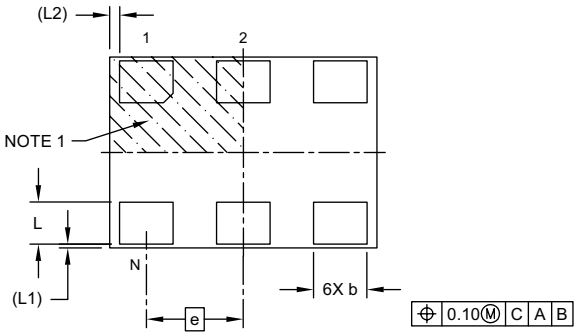
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



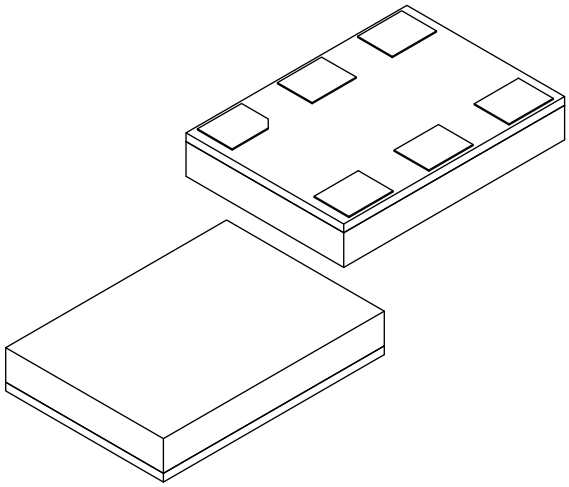
BOTTOM VIEW

Microchip Technology Drawing C04-499 Rev A Sheet 1 of 2

MICROCHIP

6-Lead Low Profile Land Grid Array (LLX) - 5x7x1.22 mm Body [LLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		2.54 BSC	
Overall Height	A	1.08	1.15	1.22
Standoff	A1	–	–	0.03
Mold Cap Thickness	A3	0.85	0.90	0.95
Overall Length	D		7.00 BSC	
Overall Width	E		5.00 BSC	
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.05	1.10	1.15
Terminal Pullback	L1		0.10 REF	
Terminal Offset	L2		0.26 REF	

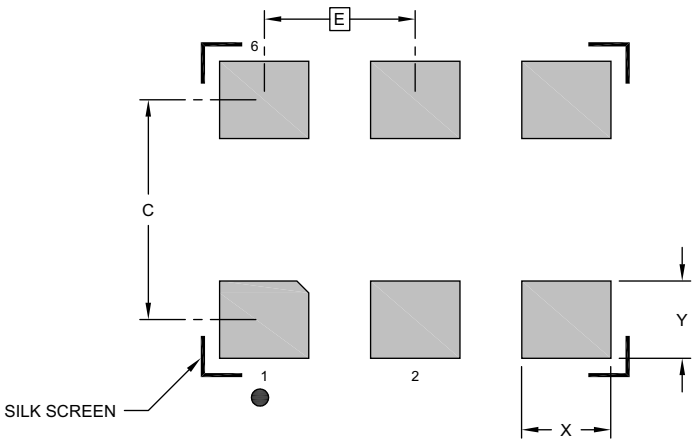
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-499 Rev A Sheet 2 of 2

6-Lead Low Profile Land Grid Array (LLX) - 5x7x1.22 mm Body [LLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		2.54 BSC	
Contact Pad Spacing	C		3.70	
Contact Pad Width (Xnn)	X			1.50
Contact Pad Length (Xnn)	Y			1.30

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2499 Rev A

APPENDIX A: REVISION HISTORY

Revision A (October 2020)

- Initial creation of MX77 Microchip data sheet DS20006425A.

Revision B (December 2020)

- Removed the Frequency Table that was under Standard Base Modules.
- Updated image for package marking under **Section 6.0 "Packaging Information"**.
- Also updated the table for Product Identification System.

Revision C (March 2021)

- Corrected Stability option in the Product Identification System.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	X	X	XXXMXXX	XX
Device	Revision	Stability	Output Logic	Output Frequency	Media Type

Device:	MX77:	Ultra-Low Jitter Clock oscillator with Integrated Quartz Crystal	
Revision (Auto Generated after Selecting Output Frequency)	5A, 5B, 5C, 5D, 5E, 6A, 6B, 6C		
Stability:	B	=	±50 ppm/20 ppm (–40°C to +85°C)
Output Logic	A B C D	= = = =	PECL LVDS CMOS HCSL
Output Frequency:	xxxMxxx	=	Generated by ClockWorks® Configurator
Shipping	T = R =		43/Tube 1,000/Reel

Please visit http://clockworks.microchip.com/timing to select a combination of options to customize your product, print a specific data sheet and order samples.

Examples:

a) MX775ABB 156M250T: 156.250 MHz LVDS Single Output, 6-Lead LGA, –40°C to +85°C Temperature Range, ±50 ppm Stability, 43/Tube

b) MX776ABD 156M250R: 156.250 MHz HCSL Single Output, 6-Lead LGA, –40°C to +85°C Temperature Range, ±50 ppm Stability, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
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