MX55/57

Low Jitter Crystal Oscillator

Features

- Output Frequency 2.5 MHz to 850 MHz
- PCIe Gen 1/2/3/4/5/6 Compliant
- Phase Noise as Low as 150 fs at F0 = 156.25 MHz, Integration Bandwidth 12 kHz–20 MHz, LVPECL Output
- Ultra Low Spurs (–113 dBc Typical)
- ±50 ppm Overvoltage and Temperature
- Supports CMOS, LVPECL, LVDS, and HCSL Outputs
- Supply Voltage (V_{IN}) +2.375V to +3.63V
- Output Enable Option; Can Be Ordered on Pin 1 or Pin 2
- Industry-Standard and Space-Saving 5.0 mm × 3.2 mm 6-lead package (MX55) and 5.0 mm × 7.0 mm (MX57)
- –40°C to +85°C Operating Temperature Range
- Pb-Free and RoHS Compliant
- Short Production Lead Time

Applications

- Ethernet 100/400/800G
- Optical Communications
- PCIe Gen 1/2/3/4/5/6* Compliant
- Fibre Channel/SAS
- CPRI/OBSAI, XAUI and Backplane SERDES

* Common Clock Configuration

General Description

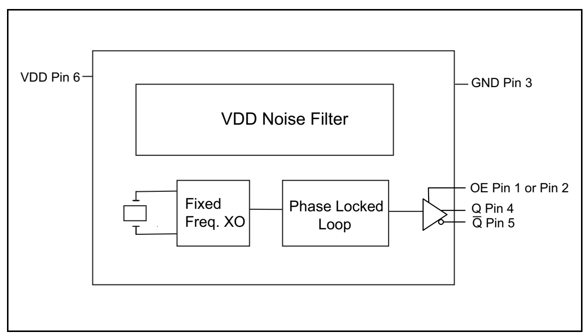
The MX55/MX57 product line is an ultra-low jitter family of industry standard crystal oscillators (XO) designed to maximize performance in networking, storage, server, and telecommunications equipment.

The MX55 employs a space-saving 3.2 mm x 5 mm package, while the MX57 is in a 5 mm x 7 mm package. These devices meet ±50 ppm total stability across –40°C to +85°C operating temperature range, using proven high reliability assembly methods that improve long term reliability and minimize aging drift compared to traditional XO assembly processes.

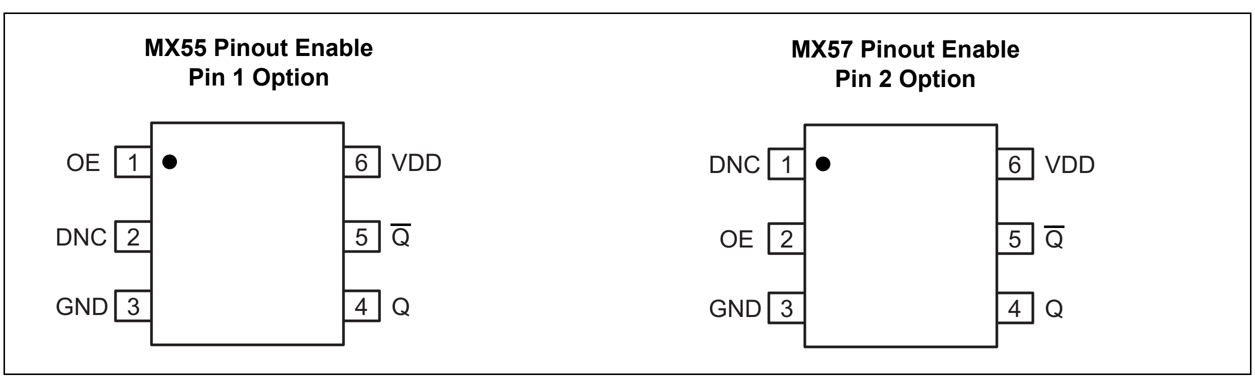
With programmable output format and OE options, these XOs can be configured to be footprint compatible with any standard 6-pin XO available today. Standard options and frequencies are also available.

Please visit http://clockworks.microchip.com/timing to select a combination of options to customize your product, print a specific data sheet, and order samples.

Block Diagram



Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, (V_{IN}).......–0.3V to V_{DD} +0.3V
Supply Voltage .... –0.3V to + 4.0V
ESD Protection (HBM) ....2 kV
ESD Protection (MM) 200V
ESD Protection (CDM) ....1.5 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 2.375V to 3.63V, T_A = –40°C to +85°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage (Note 1)	V_{DD}	2.375	—	3.63	V	—
Supply Current	I_{DD}	—	85	95	mA	Output enabled LVCMOS (no load).
		—	105	120		LVPECL
		—	80	90		LVDS
		—	85	95		HCSL
		—	68	—		Output disabled (Tri-state)
Frequency Stability	Δf	—	—	±50	ppm	Inclusive of initial accuracy, temperature drift, aging, shock and vibration.
Start-up Time	t_{SU}	—	—	20	ms	From 90% VDD to valid clock output, T = +25°C
PCIe Refclk Jitter	$t_{jphPCIe6\text{-}CC}$	—	6	12	fs_{RMS}	Refclk Jitter in Clock Generator Mode
Input Logic Levels	V_{IH}	2	—	V_{DD}+0.3	V	Input logic-high
	V_{IL}	–0.3	—	0.8		Input logic-low
Enable Active High Option (Note 2)	—	—	50	—	kΩ	Pull-up resistor on Pin 1 or 2
Enable Active Low Option (Note 3)	—	—	50	—	kΩ	Pull-down resistor on Pin 1 or 2
LVCMOS						
Frequency	f_0	2.5	—	250	MHz	—
Integrated Phase Noise (Random)	ϕj	—	131	—	fs_{RMS}	12 kHz to 5 MHz @ 25 MHz
		—	77	—		1.875 MHz to 5 MHz @ 25 MHz
Output High Voltage	V_{OH}	V_{DD}–0.8	—	—	V	R_L = 50Ω termination from Q to V_{DD}–2
Output Low Voltage	V_{OL}	—	—	0.6	V	
Output Rise/Fall Time	T_r/T_f	100	—	500	ps	—
Duty Cycle	SYM	45	—	55	%	—
LVPECL						
Frequency	f_0	2.5	—	850	MHz	—
Integrated Phase Noise (Random)	ϕj	—	130	—	fs_{RMS}	12 kHz to 20 MHz @ 200 MHz
		—	96	—		1.875 MHz to 20 MHz @ 200 MHz

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 2.375V to 3.63V, T_A = –40°C to +85°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output High Voltage	V_{OH}	V_{DD}–1.35	V_{DD}–1.01	V_{DD}–0.8	V	R_L = 50Ω termination at Q and $\overline{Q}$, both to V_{DD}–2
Output Low Voltage	V_{OL}	V_{DD}–2.0	V_{DD}–1.78	V_{DD}–1.6	mV	
Output Differential Voltage	V_{OD}	0.65	0.77	0.95	mV	—
Output Rise/Fall Time	T_r/T_f	85	—	350	ps	—
Duty Cycle	SYM	45	—	55	%	—
LVDS						
Frequency	f_0	2.5	—	850	MHz	—
Integrated Phase Noise (Random)	ϕj	—	140	—	fs_{RMS}	12 kHz to 20 MHz @ 200 MHz
		—	94	—		1.875 MHz to 20 MHz @ 200 MHz
Output High Voltage	V_{OH}	1.248	1.375	1.602	V	R_L = 100Ω termination from Q to $\overline{Q}$
Output Low Voltage	V_{OL}	0.898	1.025	1.252	V	
Output Differential Voltage	V_{OD}	247	350	454	mV	—
Common Mode Output Voltage	V_{CM}	1.125	1.2	1.375	V	—
Output Rise/Fall Time	T_r/T_f	100	—	400	ps	—
Duty Cycle	SYM	45	—	55	%	—
HCSL						
Frequency	f_0	2.5	—	850	MHz	—
Integrated Phase Noise (Random)	ϕj	—	166	—	fs_{RMS}	12 kHz to 20 MHz @ 100 MHz
		—	97	—		1.875 MHz to 20 MHz @ 100 MHz
Output High Voltage	V_{OH}	660	700	850	V	R_L = 50Ω termination at Q and $\overline{Q}$ to GND
Output Low Voltage	V_{OL}	–150	0	27	mV	
Output Differential Voltage	V_{OD}	—	200	250	mV	20% to 80%
		—	250	300		—
Common Mode Output Voltage	V_{CM}	48	—	52	mV	Differential
Output Rise/Fall Time	T_r/T_f	150	300	450	ps	—
Duty Cycle	SYM	48	—	52	%	—

Note 1: VDD Pin should be filtered with a 0.1 µF capacitor.
2: Output is enabled if pad floated (not connected) or pulled high; output tri-stated if pulled low.
3: Output is enabled if pad floated (not connected) or pulled low; output tri-stated if pulled high.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–40	—	85	°C	Ordering Option I
Junction Operating Temperature	T_J	—	—	125	°C	—
Storage Temperature Range	T_S	–65	—	150	°C	—
Soldering Temperature	—	—	—	260	°C	10 sec. max.
Package Thermal Resistance						
Thermal Resistance from Junction to Ambient	θ_{JA}		—	53	°C/W	5 mm x 7 mm
			—	58		5 mm x 3.2 mm

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and Table 2-2.

TABLE 2-1: PIN FUNCTION TABLE (ENABLE PIN 1 OPTION)

Pin Number	Pin Name	Pin Type	Description
1	OE	I	Output Enable. Active-High and Active-Low Options.
2	DNC	NC	Do not connect, Leave Floating.
3	GND	Power	Power Supply Ground.
4	Q	O	Clock Output + or Output for CMOS.
5	$\overline{Q}$	O	Clock Output – or Do Not Connect for CMOS.
6	VDD	Power	Power Supply.

TABLE 2-2: PIN FUNCTION TABLE (ENABLE PIN 2 OPTION)

Pin Number	Pin Name	Pin Type	Description
1	DNC	NC	Do not connect, Leave Floating.
2	OE	I	Output Enable. Active-High and Active-Low Options.
3	GND	Power	Power Supply Ground.
4	Q	O	Clock Output + or Output for CMOS.
5	$\overline{Q}$	O	Clock Output – or Do Not Connect for CMOS.
6	VDD	Power	Power Supply.

3.0 PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

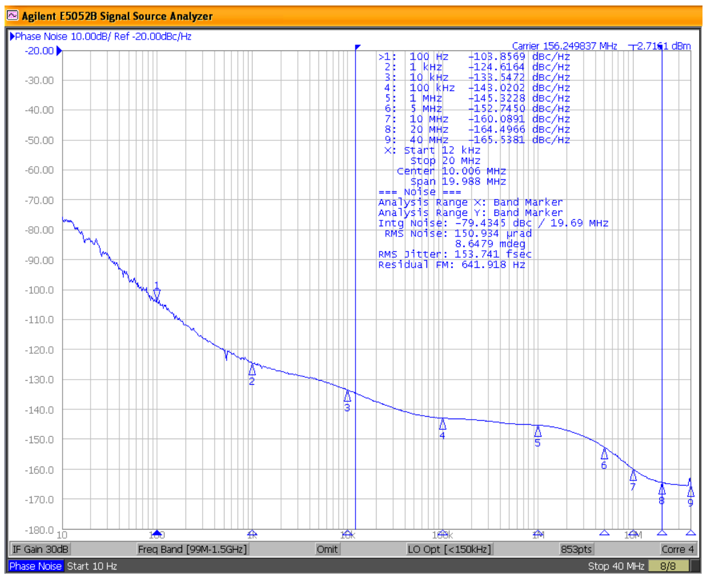


FIGURE 3-1: *LVPECL Output 156.25 MHz 12 kHz - 20 MHz 153 fs.*

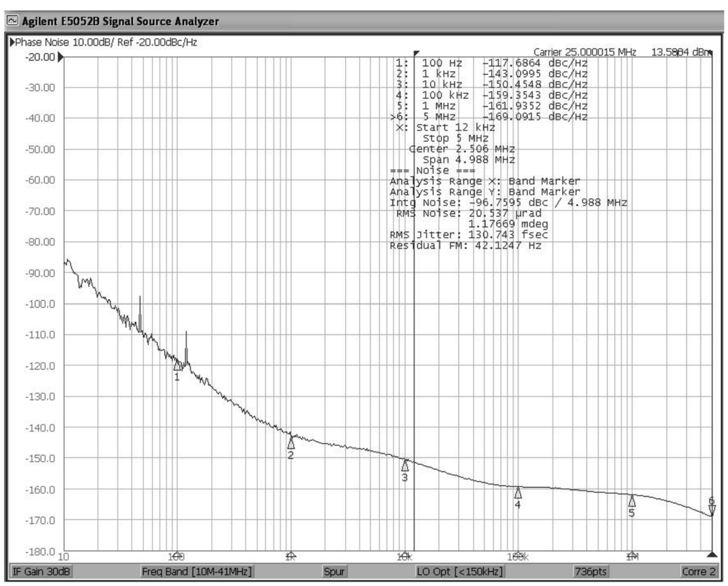


FIGURE 3-2: *LVCMOS Output 25 MHz 12 kHz - 5 MHz 131 fs.*

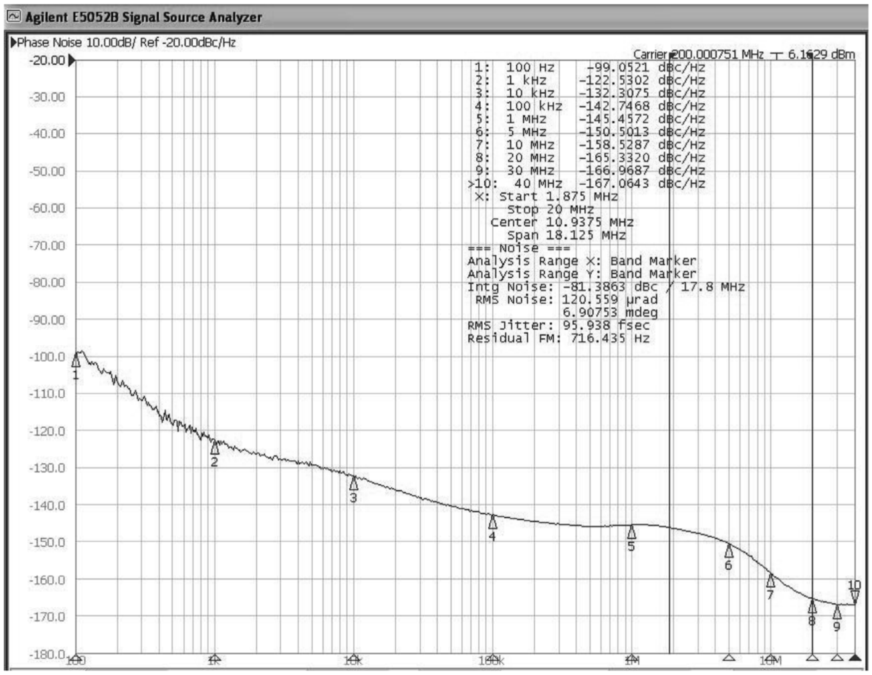


FIGURE 3-3: *LVPECL Output 200 MHz 1.875 MHz - 20 MHz 96 fs.*

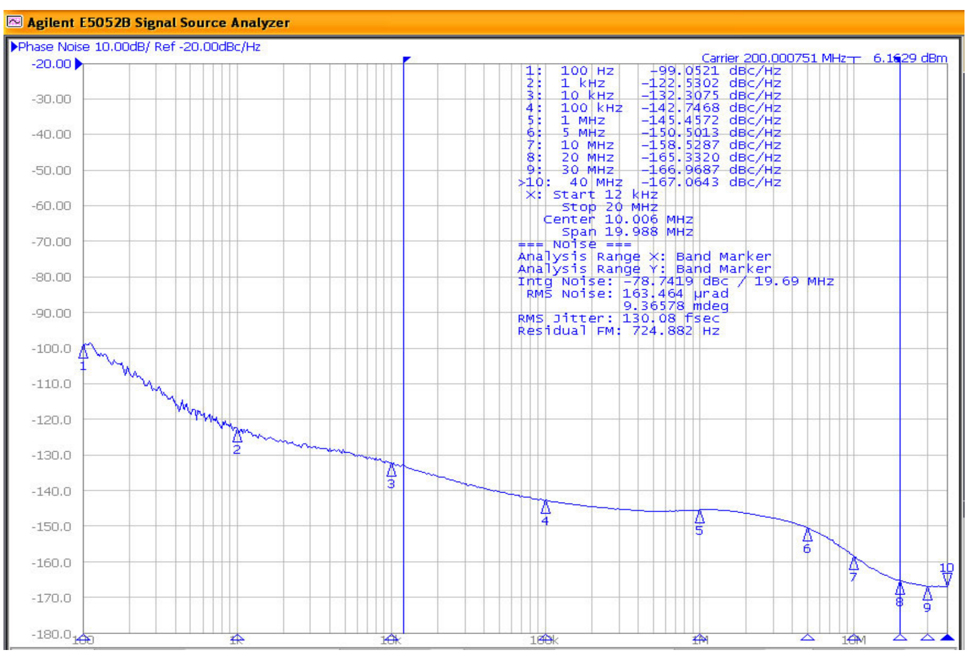


FIGURE 3-4: *LVPECL Output 200 MHz 12 kHz - 20 MHz 130 fs.*

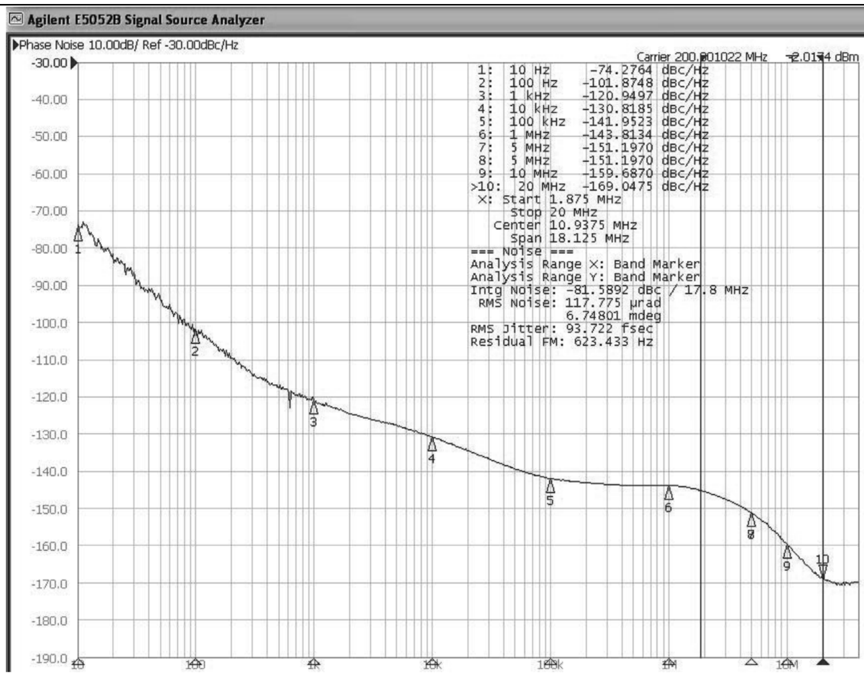


FIGURE 3-5: *LVDS Output 200 MHz 1.875 MHz - 20 MHz 94 fs.*

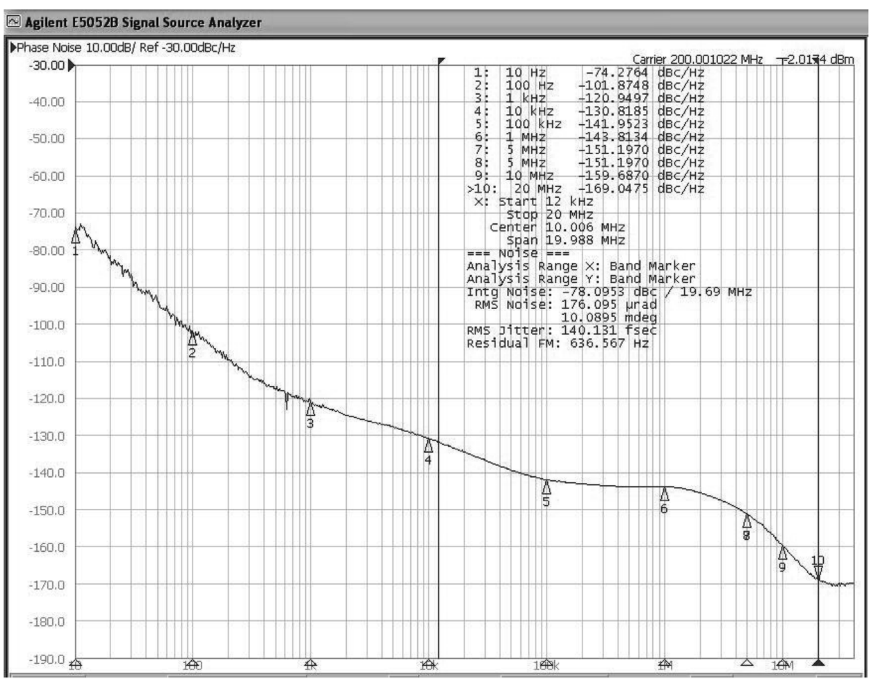


FIGURE 3-6: *LVDS Output 200 MHz 12 kHz - 20 MHz 140 fs.*

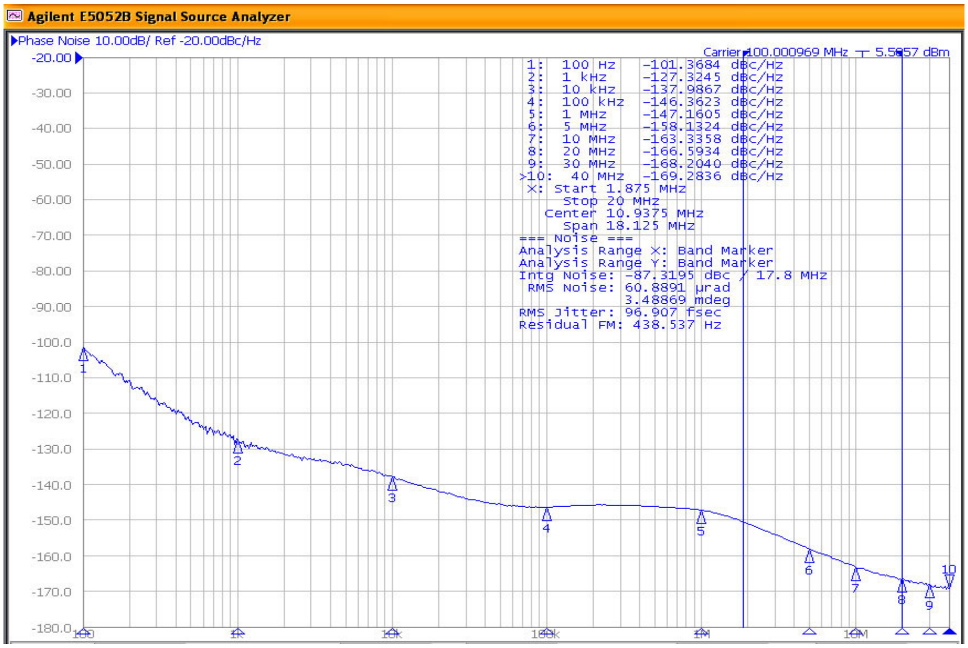


FIGURE 3-7: *HCSL Output 100 MHz 1.875 MHz - 20 MHz 97 fs.*

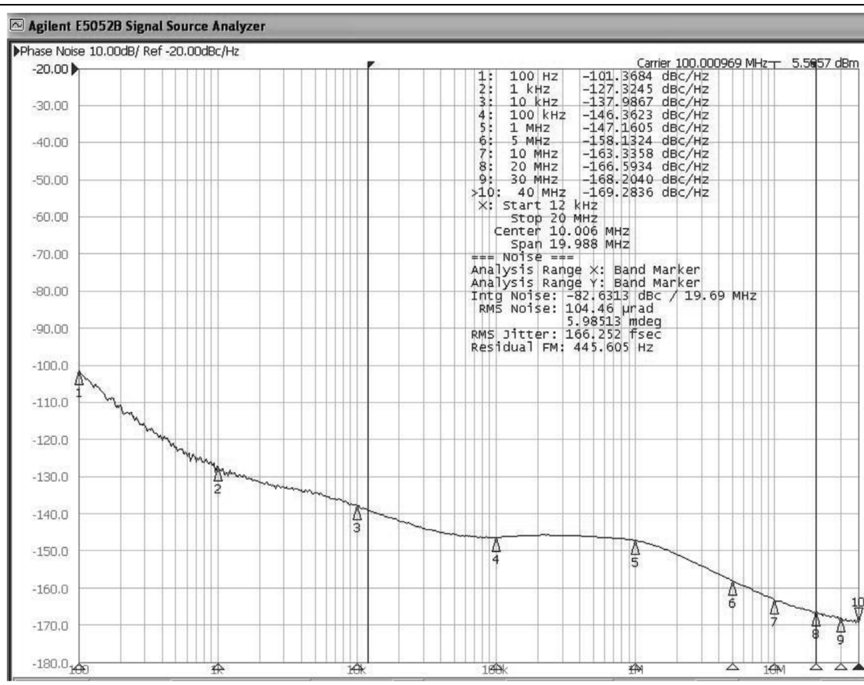


FIGURE 3-8: *HCSL Output 100 MHz 12 kHz - 20 MHz 166 fs.*

4.0 OUTPUT WAVEFORM

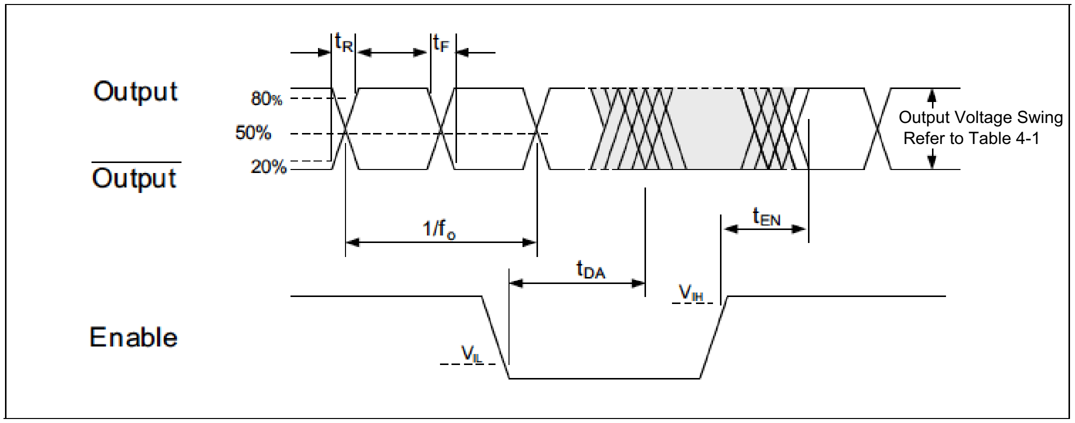


FIGURE 4-1: *Output Waveform: LVPECL, LVDS, HCSL, LVCMOS.*

TABLE 4-1: OUTPUT VOLTAGE SWING

Output Logic Protocol	Output Swing (mV Peak-Peak, Typical)
LVCMOS	V_{OH}, V_{OL}
LVPECL	770 mV
LVDS	350 mV
HCSL	700 mV

5.0 SOLDER REFLOW PROFILE

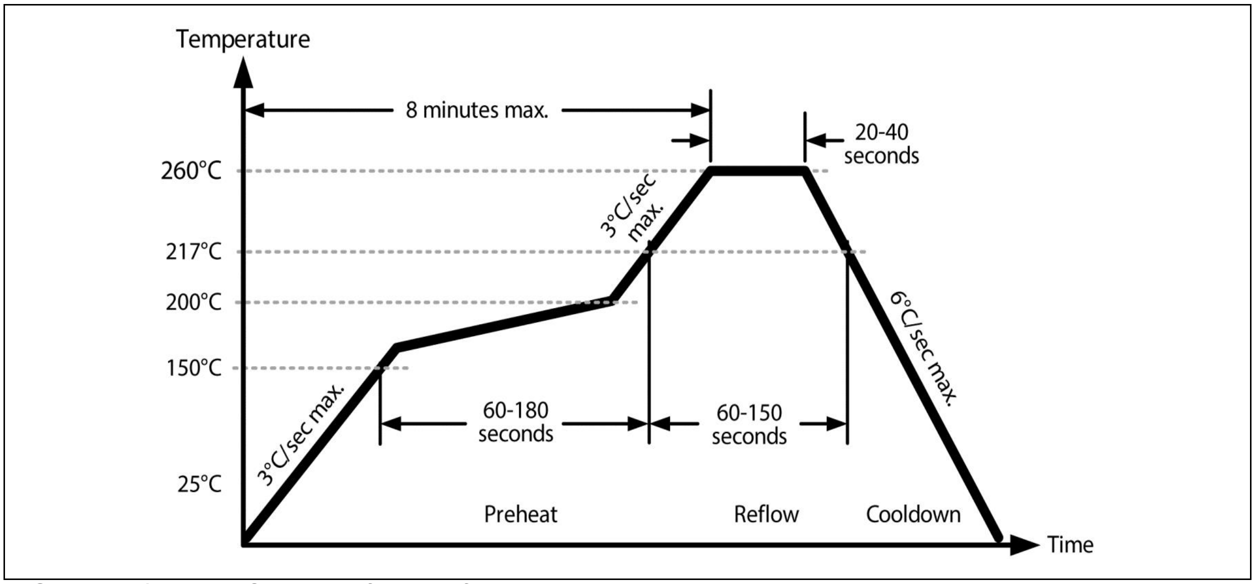


FIGURE 5-1: Solder Reflow Profile.

TABLE 5-1: SOLDER REFLOW

Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

6.0 ENVIRONMENTAL SPECIFICATIONS

TABLE 6-1: ENVIRONMENTAL SPECIFICATIONS

Parameter	Specification
Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method1004
Mechanical Shock	MIL-STD-883, Method 2022, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition B
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free Devices (Except 2 Cycles Max)
Hazardous Substance	Pb-Free/RoHS/Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1 = $2x10^{-8}$ ATM CC/S
Solvent Resistance	MIL-STD-202, Method 215

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

6-Pin LGA*
5 mm x 7 mm

```
XXXXXXX
WNNN
XXXXXXXX
```

Example

```
MX575AB
1958
F100M000
```

6-Pin LGA*
3.2 mm x 5 mm

```
XXXXXX
WNNN
XXXXXX
```

Example

```
MX555A
1817
BF1000
```

Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

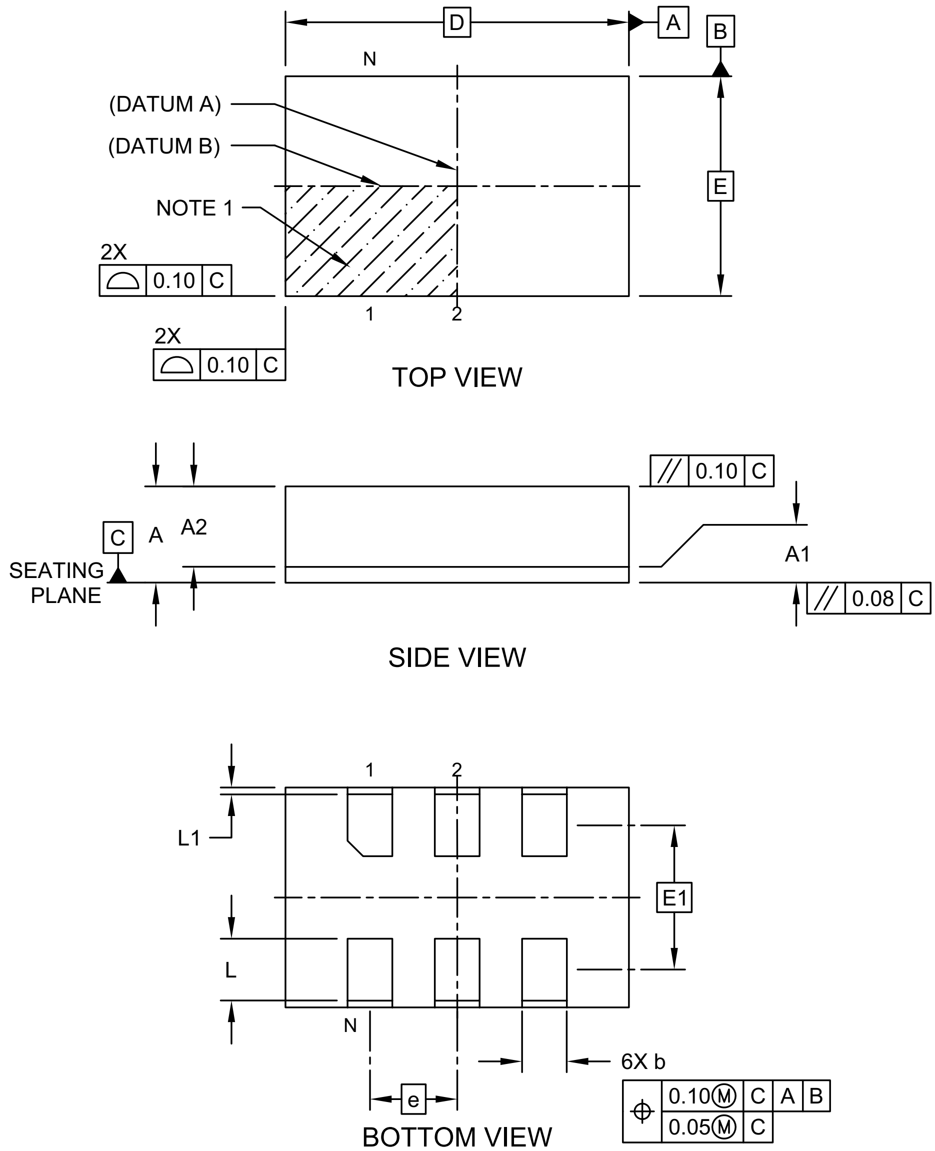
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

6-Lead Low 5.0 mm x 3.2 mm LGA Package Outline and Recommended Land Pattern

6-Lead Low Profile Land Grid Array (ANA) - 5.0x3.2 mm Body [LLGA]

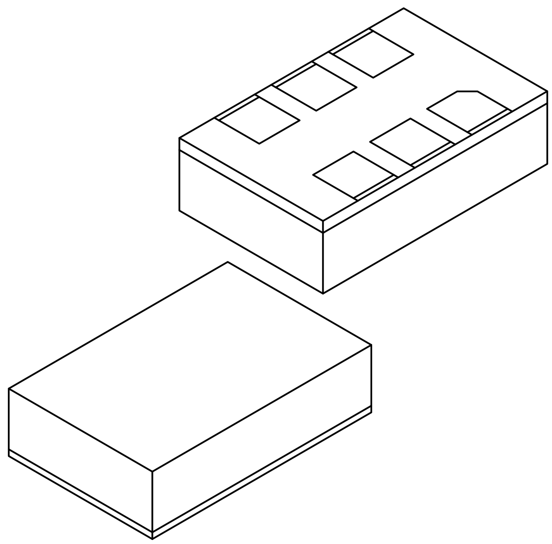
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1068A Sheet 1 of 2

6-Lead Low Profile Land Grid Array (ANA) - 5.0x3.2 mm Body [LLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		1.27 BSC	
Overall Height	A	1.26	1.33	1.40
Substrate Thickness	A1	0.19	0.23	0.27
Mold Cap Height	A2	1.07	1.10	1.13
Overall Length	D		5.00 BSC	
Overall Width	E		3.20 BSC	
Terminal Pitch	E1		2.10 BSC	
Terminal Width	b	0.85	0.90	0.95
Terminal Length	L	0.85	0.90	0.95
Terminal Pullback	L1	0.05	0.10	0.15

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

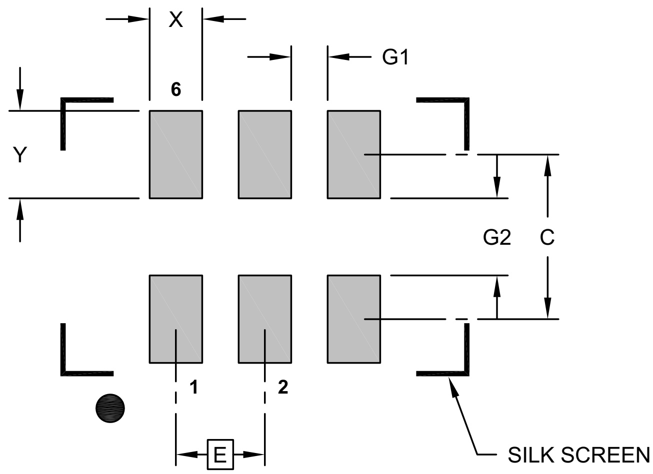
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1068A Sheet 2 of 2

6-Lead Low Profile Land Grid Array (ANA) - 5.0x3.2 mm Body [LLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		1.27 BSC		
Contact Pad Spacing	C			2.35	
Contact Pad Width (X6)	X				0.75
Contact Pad Length (X6)	Y				1.25
Spacing Between Pads (X4)	G1		0.52		
Spacing Between Pads (X3)	G2		1.10		

Notes:

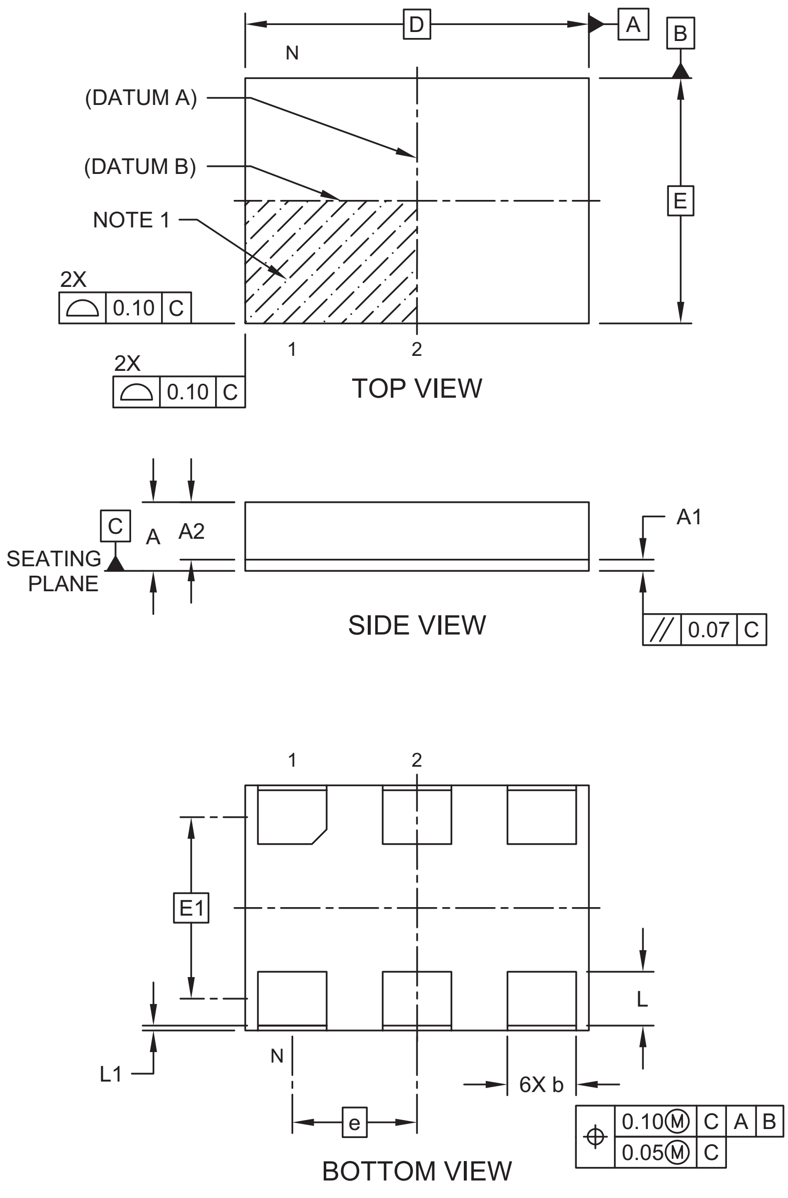
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3068A

6-Lead Low 7 mm x 5 mm LGA Package Outline and Recommended Land Pattern

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

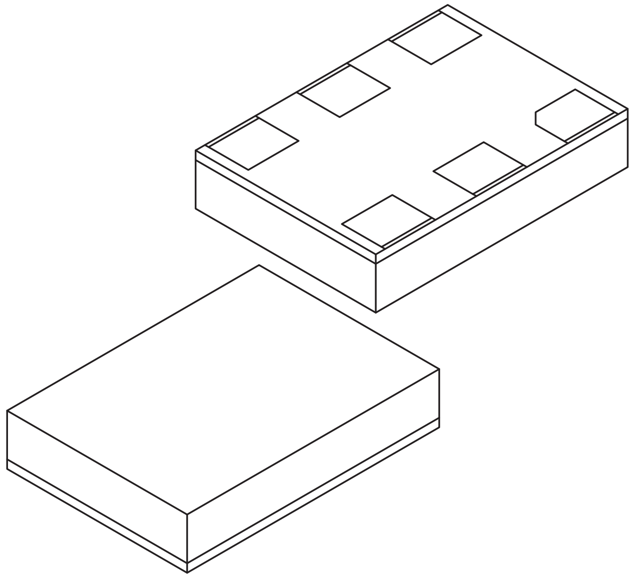
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1071A Sheet 1 of 2

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		2.54 BSC	
Overall Height	A	1.26	1.33	1.40
Substrate Thickness	A1	0.19	0.23	0.27
Mold Cap Thickness	A2	1.07	1.10	1.13
Overall Length	D		7.00 BSC	
Pitch	E1		3.70 BSC	
Overall Width	E		5.00 BSC	
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.05	1.10	1.15
Pullback	L1	0.05	0.10	0.15

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

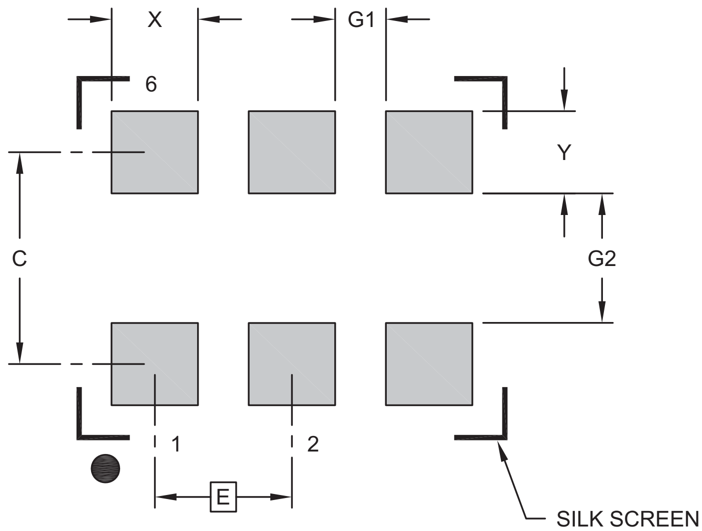
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1071A Sheet 2 of 2

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		2.54 BSC	
Contact Pad Spacing	C		3.93	
Contact Pad Width (X6)	X			1.60
Contact Pad Length (X6)	Y			1.53
Contact to Contact (X4)	G1	0.94		
Contact to Contact (X3)	G2	2.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3071A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2018)

- Initial creation of MX55/57 Microchip data sheet DS20005972A.

Revision B (January 2023)

- Updated Applications to include PCIe Gen 5 and Gen 6.
- Updated Features section to include PCIe compliance statement.

Revision C (July 2024)

- Updated Applications to include PCIe Gen 5 and Gen 6.
- Updated Features section to include PCIe compliance statement.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	X	X	XXXMXXX	XX
Device	Crystal Frequency	Enable Pin Option	Output Logic Type	Output Frequency	Shipping

Device: MX55: Low Jitter Crystal Oscillator in 6-Pin 5 mm × 3.2 mm
MX57: Low Jitter Crystal Oscillator in 6-Pin 7 mm × 5 mm

Crystal Frequency: 5A (Example Only) = Option selected by ClockWorks Configurator for Manufacturing

Enable Pin Option:
B = Pin 1
N = Pin 2

Output Logic Type: (For Enable Pin 1)
A = PECL (Active High)
B = LVDS (Active High)
C = CMOS (Active High)
D = HCSL (Active High)
F = PECL (Active Low)
G = LVDS (Active Low)
H = CMOS (Active Low)
J = HCSL (Active Low)

Output Logic Type: (For Enable Pin 2)
R = PECL (Active High)
S = LVDS (Active High)
T = CMOS (Active High)
U = HCSL (Active High)
L = PECL (Active Low)
M = LVDS (Active Low)
N = CMOS (Active Low)
P = HCSL (Active Low)

Output Frequency: xxxMxxx = 2.5 MHz to 850 MHz

Shipping
TA = Tube
RA = Tape & Reel

Please visit http://clockworks.microchip.com/timing to select a combination of options to customize your product, print a specific data sheet and order samples.

Examples:

a) MX555ABF 100M000TA — Low Jitter Crystal Oscillator in 6-Pin 5 mm × 3.2 mm, Pin 1 PECL Active Low, 100 MHz, Tube

b) MX575ABF 100M000RA — Low Jitter Crystal Oscillator in 6-Pin 5 mm × 7 mm, Pin 1 PECL Active Low, 100 MHz, Reel

c) MX555ANU 100M000TA — Low Jitter Crystal Oscillator in 6-Pin 5 mm × 3.2 mm, Pin 2 PECL Active Low, 250 MHz, Tube

d) MX575ANN 100M000RA — Low Jitter Crystal Oscillator in 6-Pin 5 mm × 7 mm, Pin 2 CMOS Active Low, 150 MHz, Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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