DC – 26 GHz GaAs Distributed MMIC LNA

MMA041AA

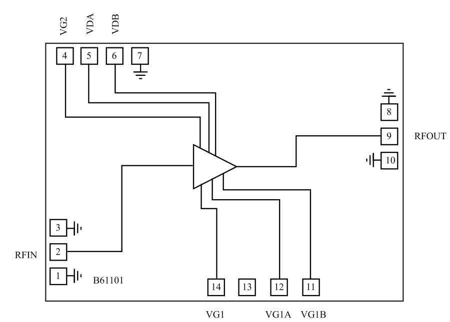
Product Overview

MMA041AA is a Gallium Arsenide (GaAs) monolithic microwave integrated circuit (MMIC) Pseudomorphic High-Electron Mobility Transistor (PHEMT) distributed amplifier die that operates between DC and 26 GHz. It is ideal for test instrumentation, defense, aerospace, and communications infrastructure applications. The amplifier provides a flat gain of 18.5 dB, 2 dB noise figure, and 22 dBm of output power at 1 dB gain compression, and 36 dBm output IP3. The MMA041AA amplifier features RF I/Os that are internally matched to 50Ω, which allows for easy integration into multi-chip modules (MCMs).

Key Features

- Broadband performance: DC to 26 GHz
- High gain: 18.5 dB
- Low noise figure: 2 dB
- High output IP3: + 36 dBm
- High input power: + 22 dBm
- Positive supply : +6V at 150 mA
- 50Ω matched input/output
- Die size: 3.0 mm × 1.35 mm × 0.1 mm

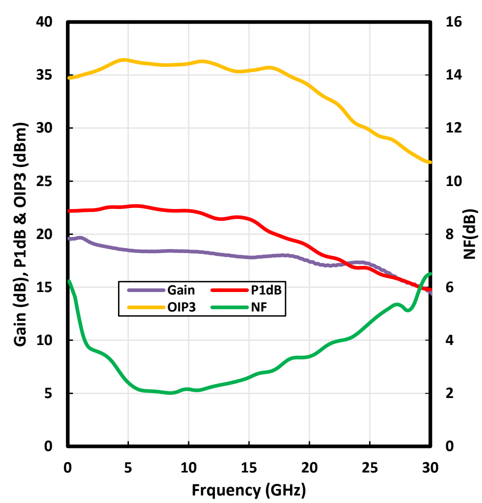
Functional Block Diagram



Applications

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military, A&D, space, SATCOM
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

Gain, NF, OIP3, and P1dB Performances



Performance Overview

Parameter	Typ.	Units
Frequency range	DC – 26	GHz
Gain	18.5	dB
NF	2	dB
Output IP3	+36	dBm
P1dB	+22	dBm

Export Classification: EAR–99

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1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, V_{DD} = 6V, I_{DD} = 150 mA (unless otherwise specified)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		26	GHz
Gain	DC – 6 GHz	18	20		dB
	6 GHz – 12 GHz	17	18.5		
	12 GHz – 20 GHz	17	18		
	20 GHz – 26 GHz		17		
Gain flatness	4 GHz – 12 GHz		± 0.5		dB
	12 GHz – 20 GHz		± 0.25		
Noise figure	2 GHz – 6 GHz		2.2	3	dB
	6 GHz – 12 GHz		1.5	2	
	12 GHz – 20 GHz		2	3	
	20 GHz – 26 GHz		3.5		
P1dB	DC – 6 GHz	21.5	22		dBm
	6 GHz – 12 GHz	21	22		
	12 GHz – 20 GHz	18.5	20		
	20 GHz – 26 GHz		18		
P3dB	DC – 6 GHz		24		dBm
	6 GHz – 12 GHz		24		
	12 GHz – 20 GHz		23		
	20 GHz –26 GHz		20		
OIP3	DC – 6 GHz		37		dBm
	6 GHz – 12 GHz		37		
	12 GHz – 20 GHz		36		
	20 GHz – 26 GHZ		32		
Input return loss	DC – 6 GHz		17		dB
	6 GHz – 12 GHz		20		
	12 GHz – 20 GHz		20		
	20 GHz – 26 GHz		15		
Output return loss	DC – 6 GHz		17		dB
	6 GHz – 12 GHz		17		
	12 GHz – 20 GHz		16		
	20 GHz – 26 GHz		15		
V_{DD} (drain voltage supply)			6		V
I_{DD} (drain current)			150		mA
V_{GG} (gate voltage bias)			–0.4		V

1.2 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA041AA device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_D)	+8V
First gate bias voltage (V_{G1})	–2V to +0.5V
RF input power (Pin)	22 dBm
DC power dissipation (T = +85 °C)	2.4W
Channel temperature	150 °C
Thermal resistance	18 °C/W
Operating temperature	–55 °C to +85 °C
Storage temperature	–65 °C to +150 °C

ESD Sensitive Device

1.3 Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The following graphs show the typical performance curves of the MMA041AA device at specific bias conditions. All measurements were performed using the test circuit shown in Figure 3–2.

Figure 1-1. Gain vs. Temperature at 5V/100 mA

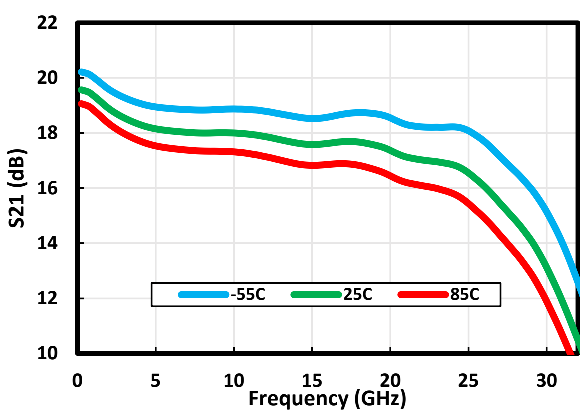


Figure 1-2. Gain vs. Temperature at 6V/150 mA

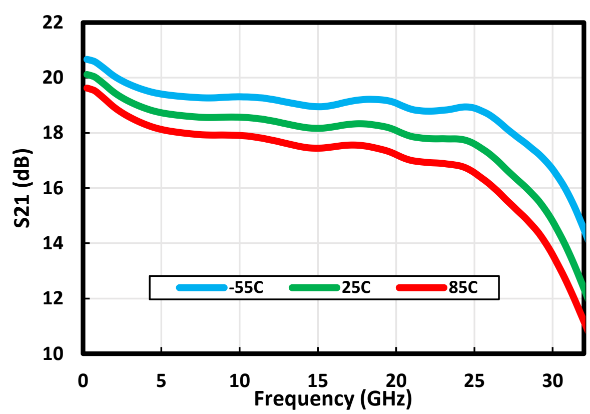


Figure 1-3. Gain vs. Temperature at 7V/180 mA

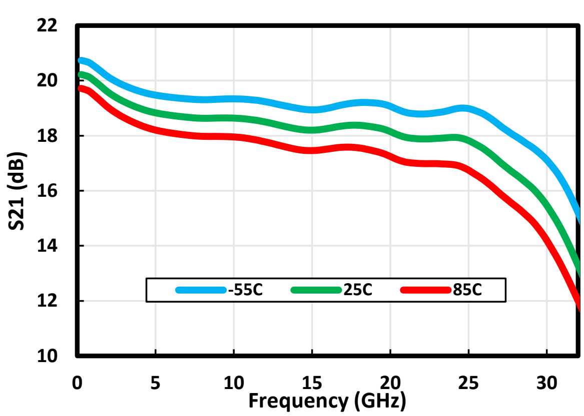


Figure 1-4. S11 vs. Temperature at 5V/100 mA

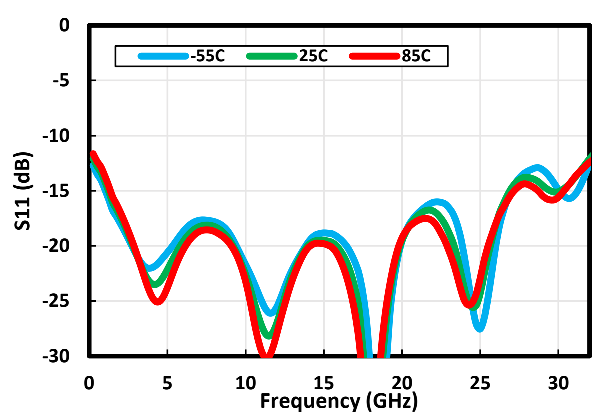


Figure 1-5. S11 vs. Temperature at 6V/150 mA

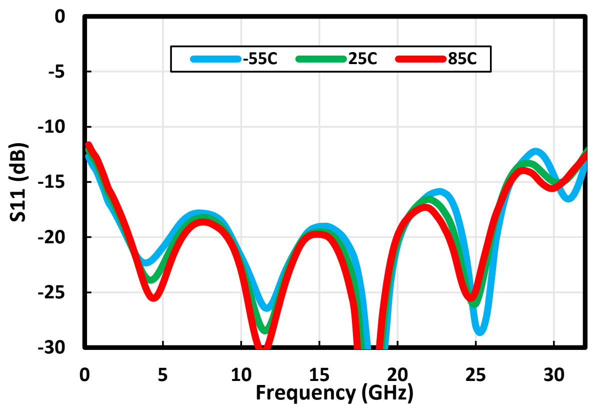


Figure 1-6. S11 vs. Temperature at 7V/180 mA

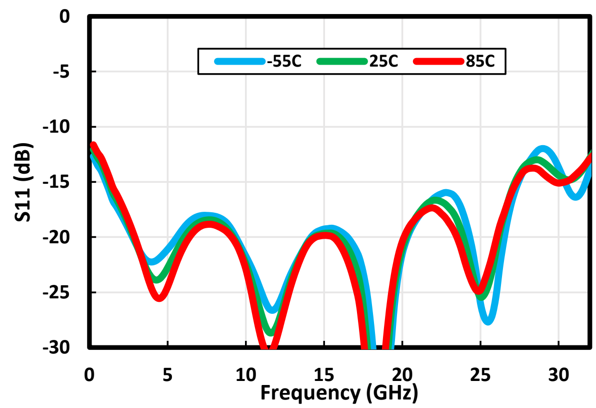


Figure 1-7. S22 vs. Temperature at 5V/100 mA

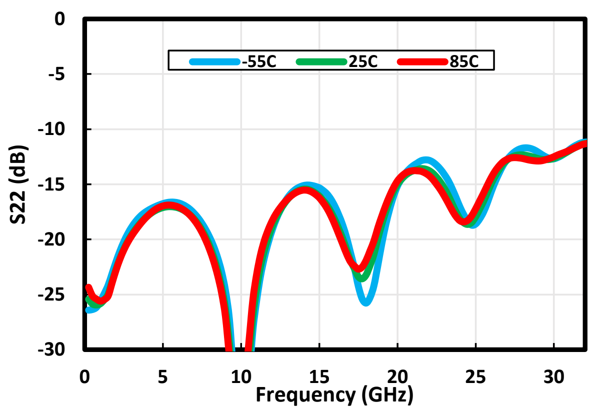


Figure 1-8. S22 vs. Temperature at 6V/150 mA

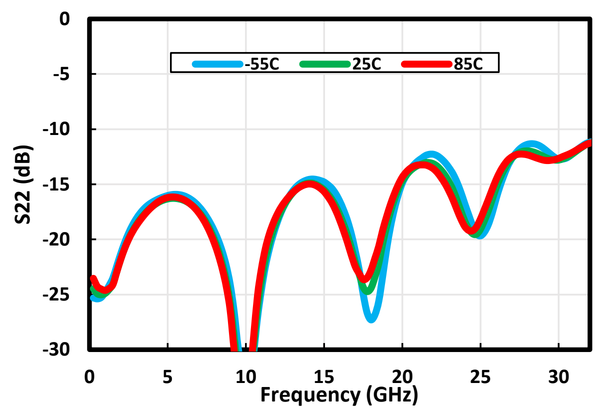


Figure 1-9. S22 vs. Temperature at 7V/180 mA

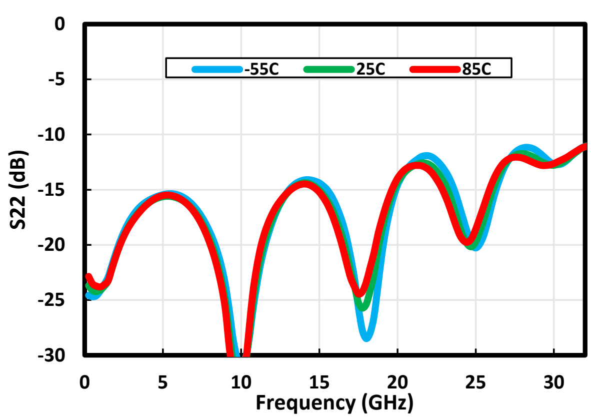


Figure 1-10. S12 vs. Temperature at 5V/100 mA

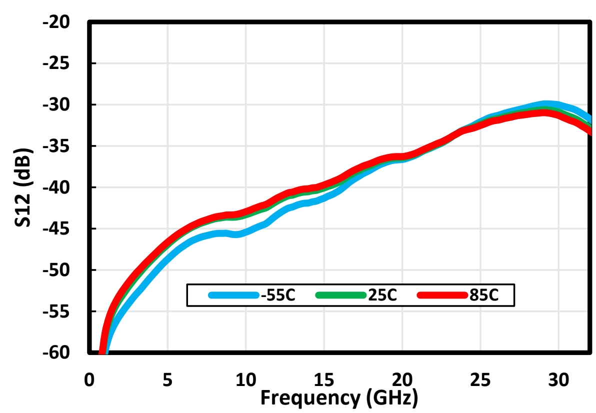


Figure 1-11. S12 vs. Temperature at 6V/150 mA

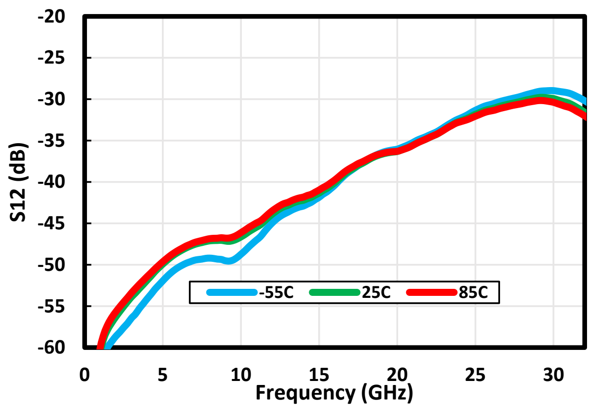


Figure 1-12. S12 vs. Temperature at 7V/180 mA

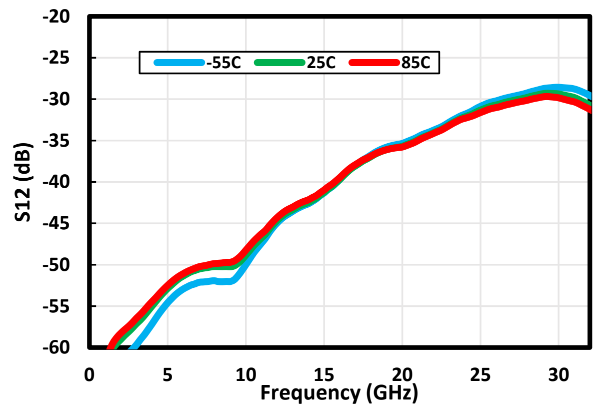


Figure 1-13. NF vs. Temperature at 5V/100 mA

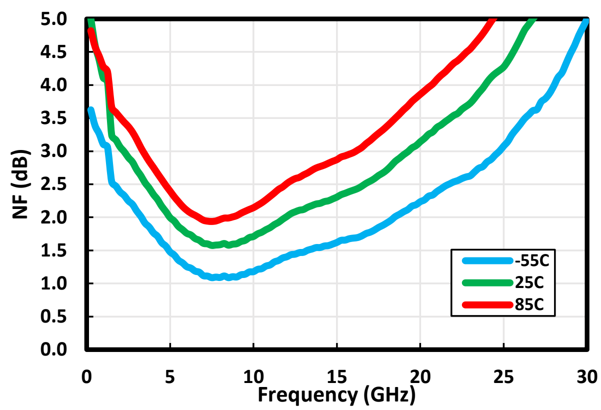


Figure 1-14. NF vs. Temperature at 6V/150 mA

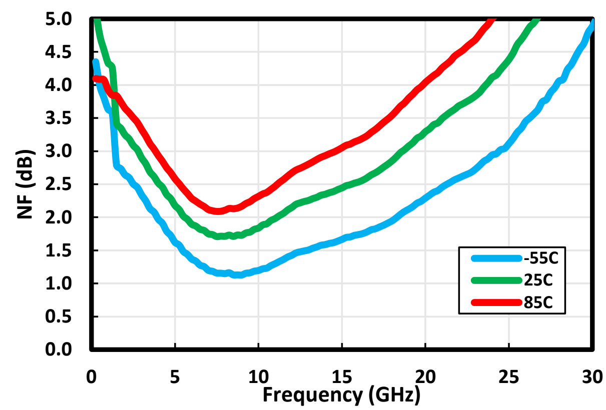


Figure 1-15. NF vs. Temperature at 7V/180 mA

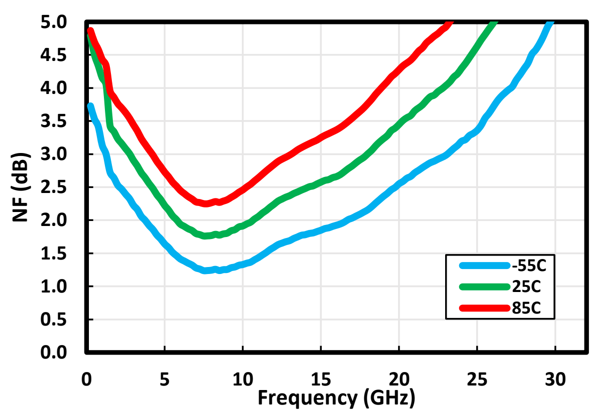


Figure 1-16. P1dB vs. Temperature at 5V/100 mA

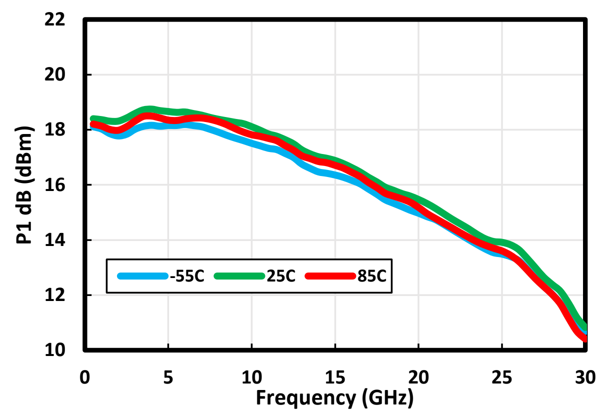


Figure 1-17. P1dB vs. Temperature at 6V/150 mA

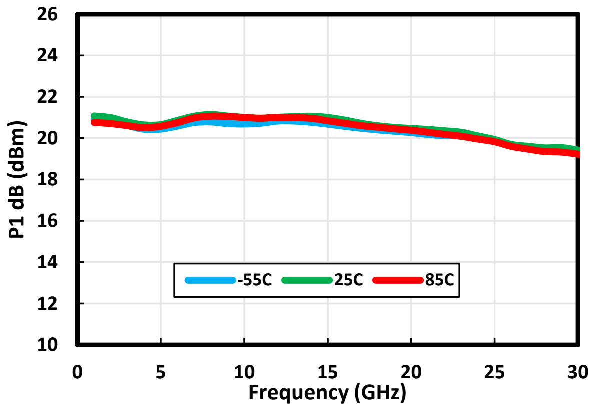


Figure 1-18. P1dB vs. Temperature at 7V/180 mA

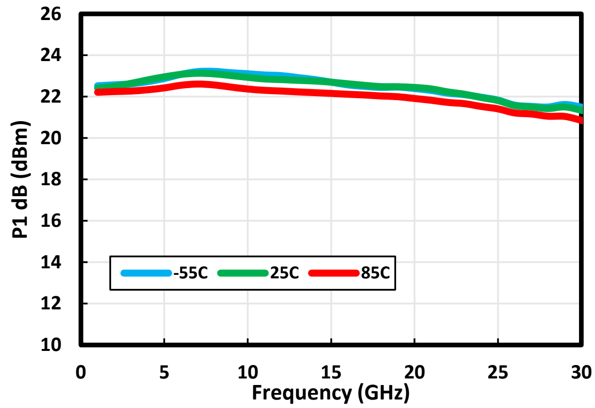


Figure 1-19. Psat vs. Temperature at 5V/100 mA

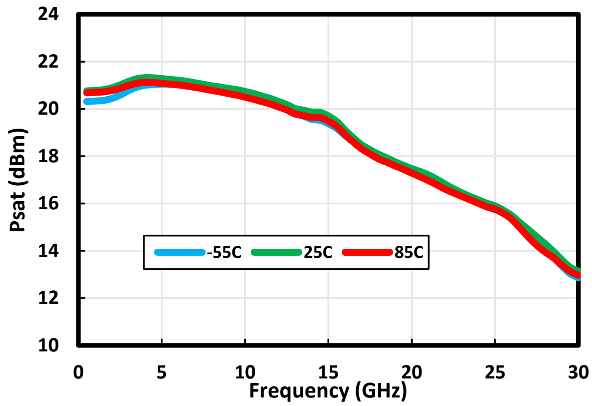


Figure 1-20. Psat vs. Temperature at 6V/150 mA

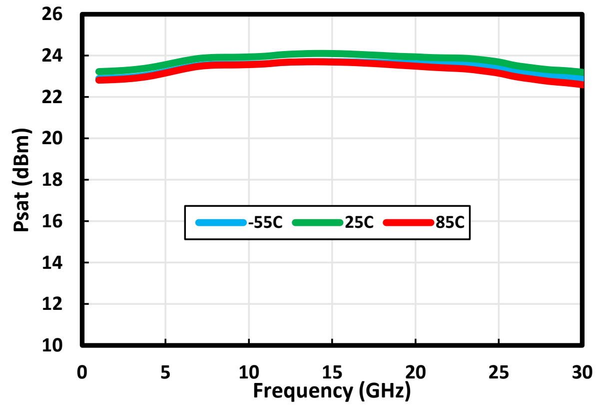


Figure 1-21. Psat vs. Temperature at 7V/180 mA

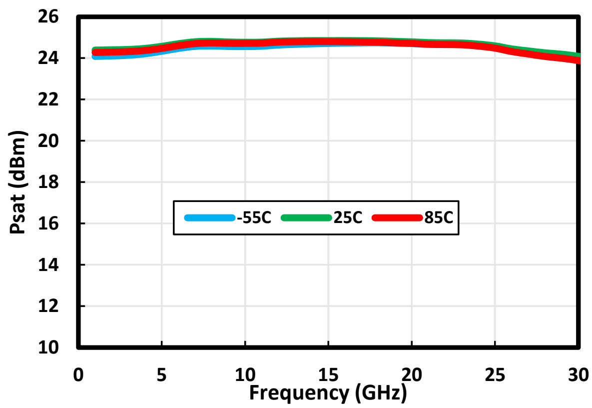


Figure 1-22. OIP3 vs. Temperature at 5V/100 mA

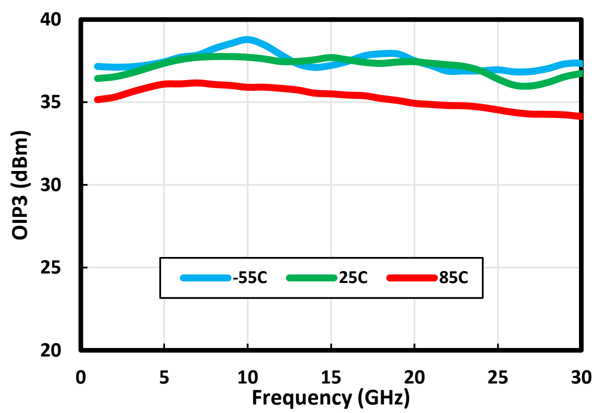


Figure 1-23. OIP3 vs. Temperature at 6V/150 mA

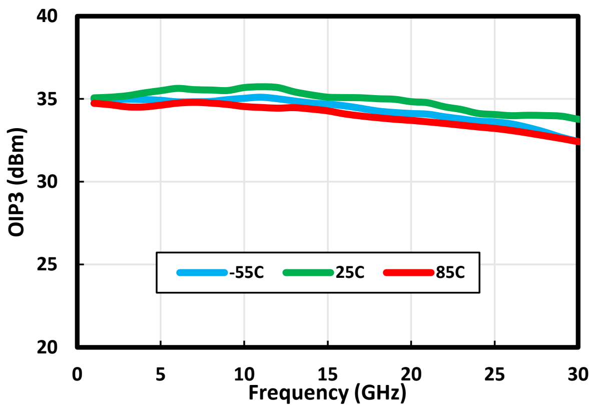


Figure 1-24. OIP3 vs. Temperature at 7V/180 mA

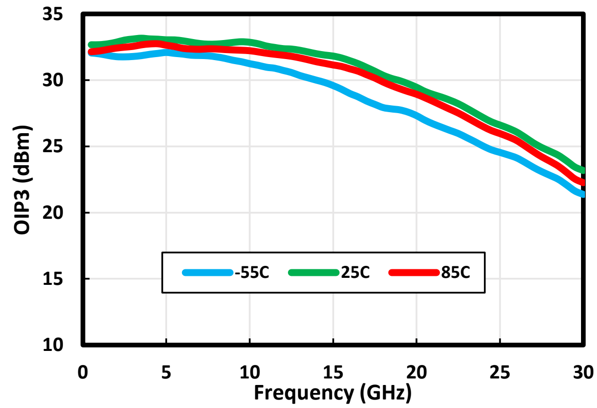


Figure 1-25. OIP2(low) vs. Temperature at 5V/100 mA

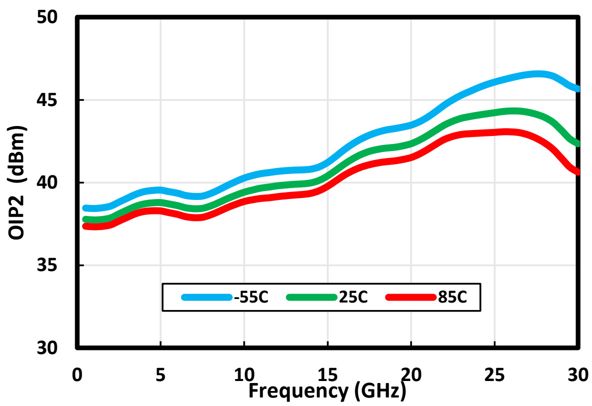


Figure 1-26. OIP2(low) vs. Temperature at 6V/150 mA

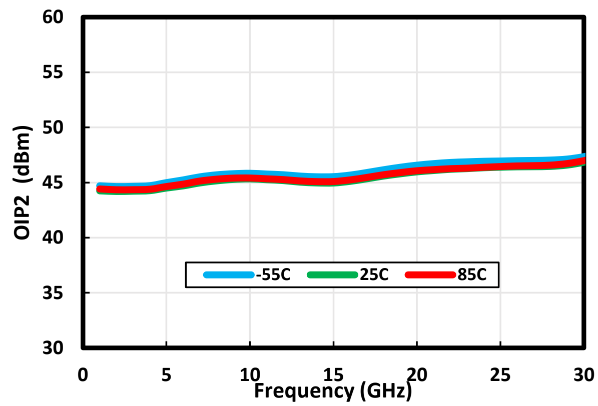


Figure 1-27. OIP2(low) vs. Temperature at 7V/180 mA

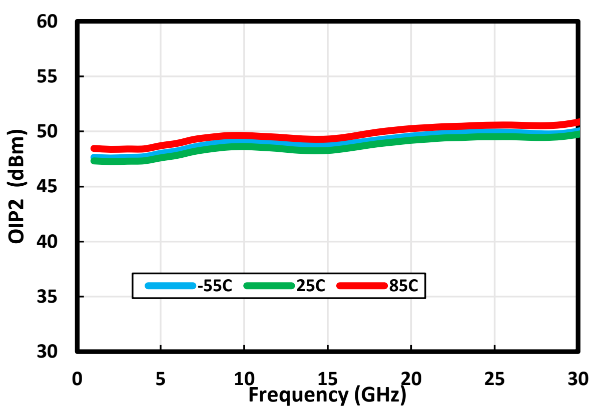


Figure 1-28. IM3 vs. Temperature at 5V/100 mA, 10 dBM (per tone)

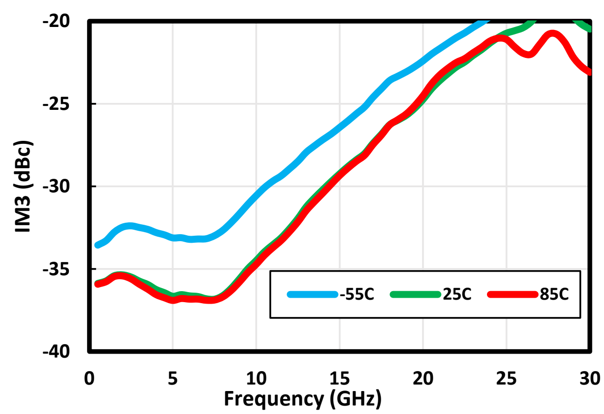


Figure 1-29. IM3 vs. Temperature at 6V/150 mA, 10 dBM (per tone)

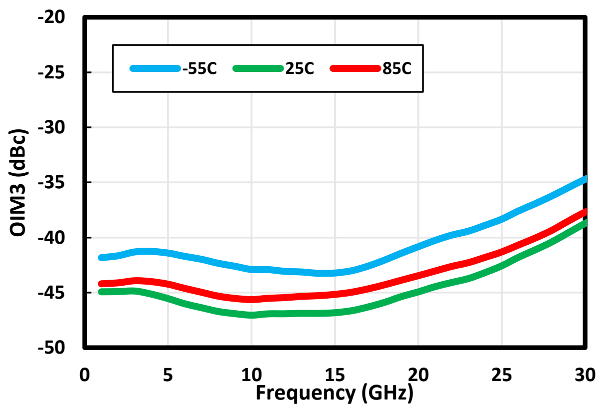
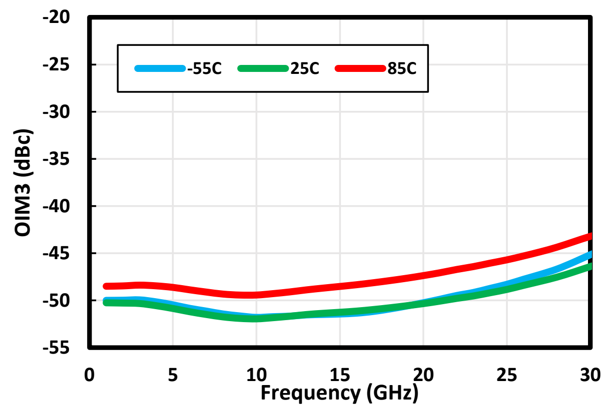


Figure 1-30. IM3 vs. Temperature at 7V/180 mA, 10 dBM (per tone)



1.3.2 Typical Performances vs. Bias

The following graphs show the typical performance curves of the MMA041AA device at 25 °C vs.bias conditions. All measurements were performed using the test circuit shown in Figure 3–2.

Figure 1-31. Gain vs. V_{DD}/I_{DD}

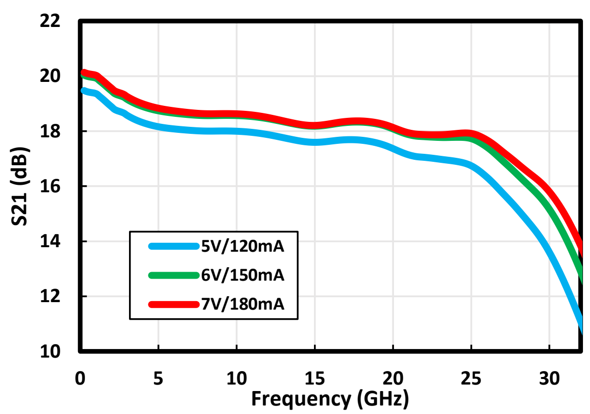


Figure 1-32. NF vs. V_{DD}/I_{DD}

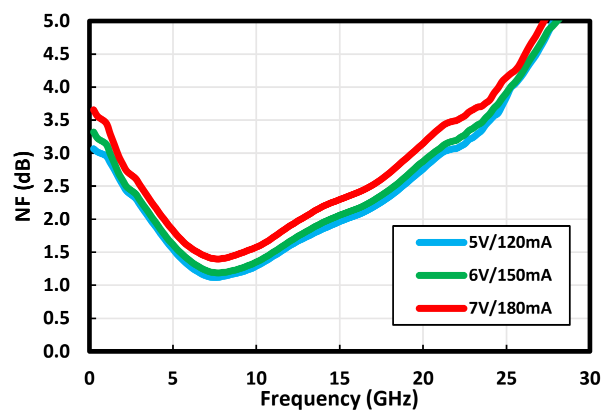


Figure 1-33. S11 vs. V_{DD}/I_{DD}

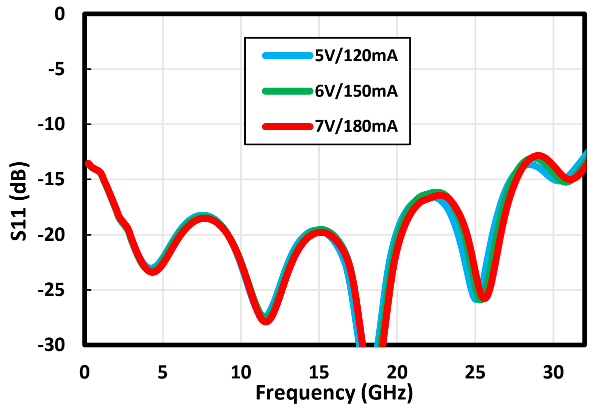


Figure 1-34. S22 vs. V_{DD}/I_{DD}

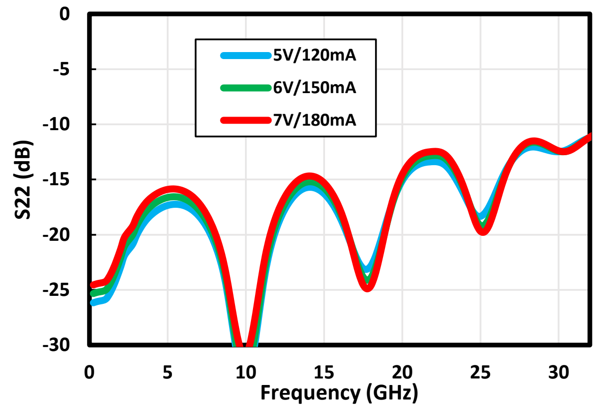


Figure 1-35. S12 vs. V_{DD}/I_{DD}

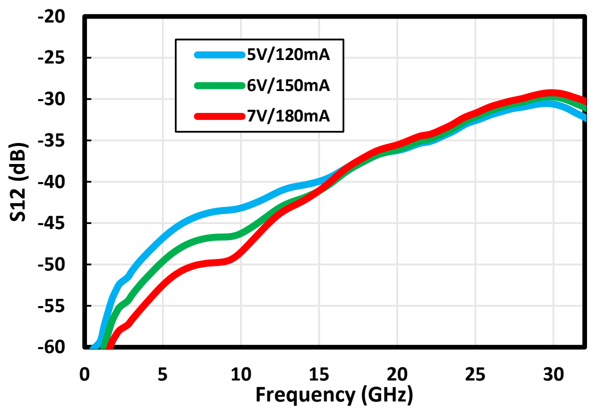


Figure 1-36. P1dB vs. V_{DD}/I_{DD}

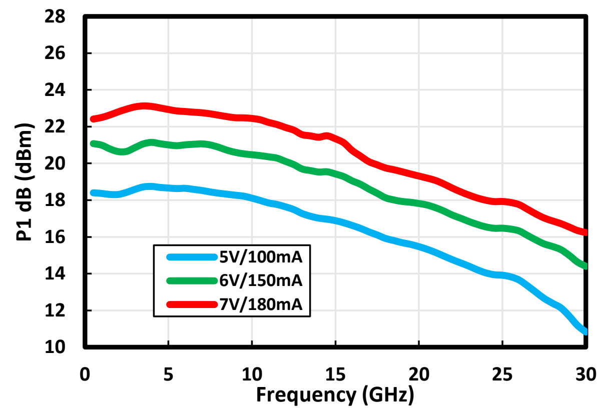


Figure 1-37. Psat vs. V_{DD}/I_{DD}

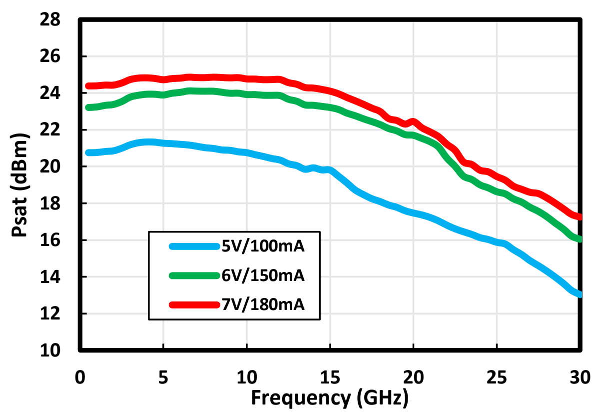


Figure 1-38. OIP3 vs. V_{DD}/I_{DD}

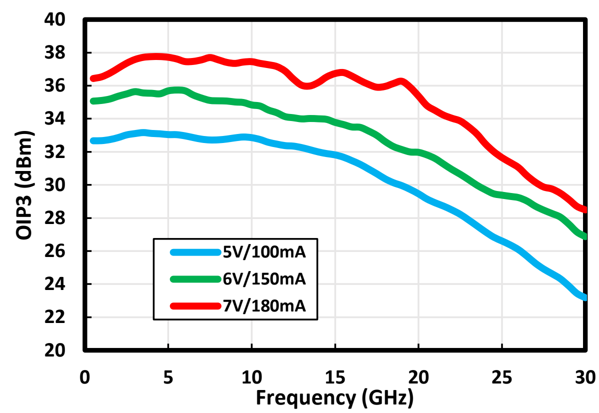


Figure 1-39. OIP2 Low at Δ – 10 MHz vs. V_{DD}/I_{DD}

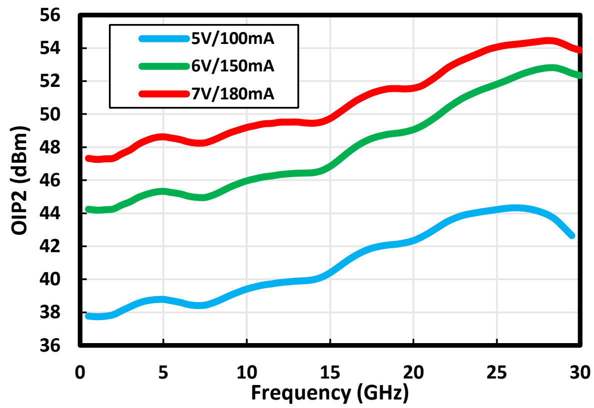
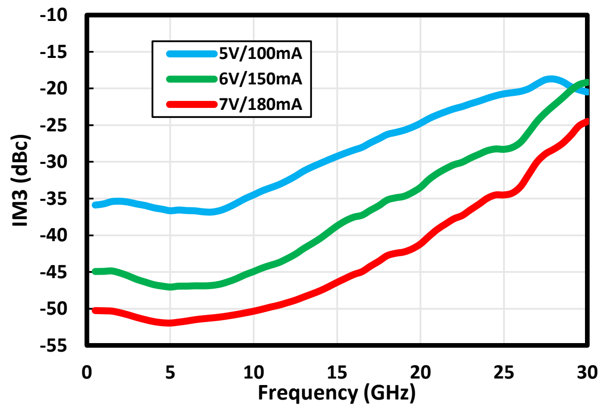


Figure 1-40. IM3 vs. V_{DD}/I_{DD} 10 dBm (per tone)



1.3.3 Typical Performances vs. Output Power

The following graphs show the typical performance curves of the MMA041AA device at 25 °C vs. Output Power conditions. All measurements were performed using the test circuit shown in Figure 3–2.

Figure 1-41. IM2 vs. Power at 5V/100 mA

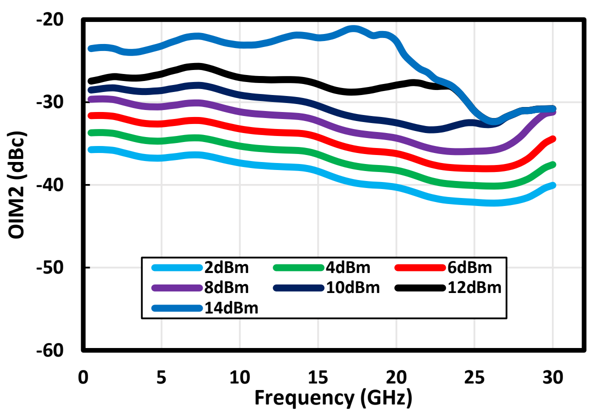


Figure 1-42. IM2 vs. Power at 6V/150 mA

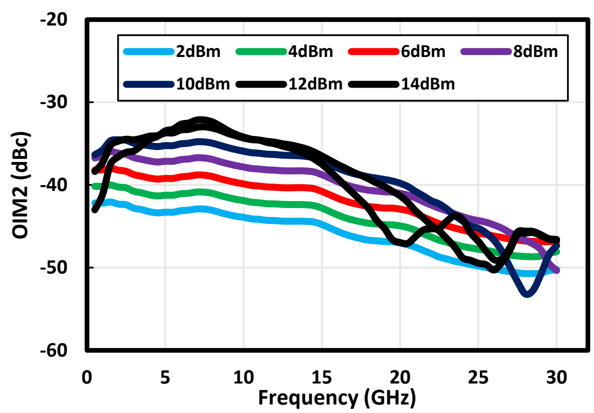


Figure 1-43. IM2 vs. Power at 7V/180 mA

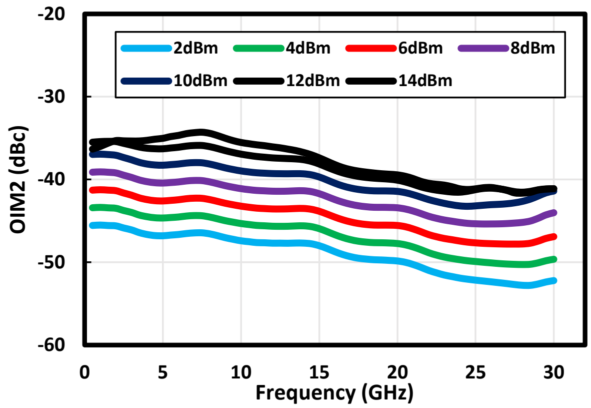


Figure 1-44. IM3 vs. Power at 5V/100 mA

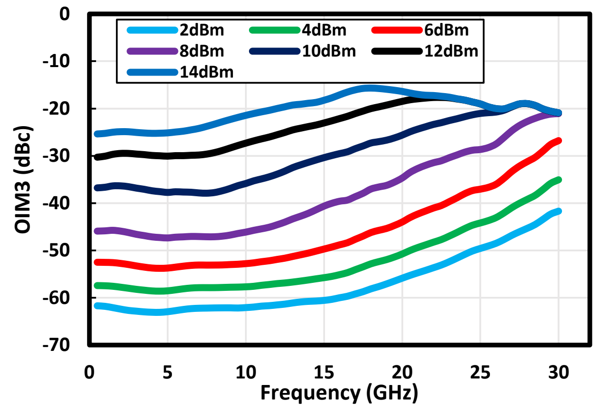


Figure 1-45. IM3 vs. Power at 6V/150 mA

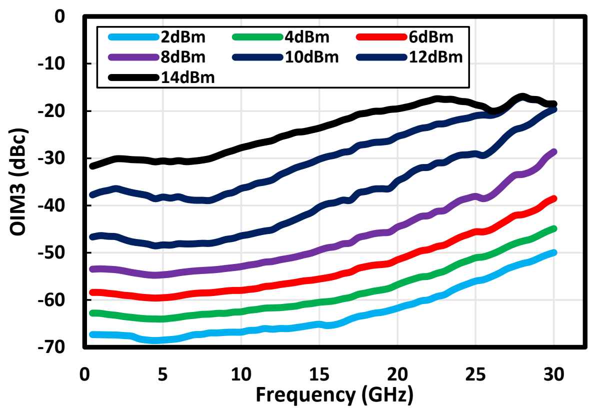


Figure 1-46. IM3 vs. Power at 7V/180 mA

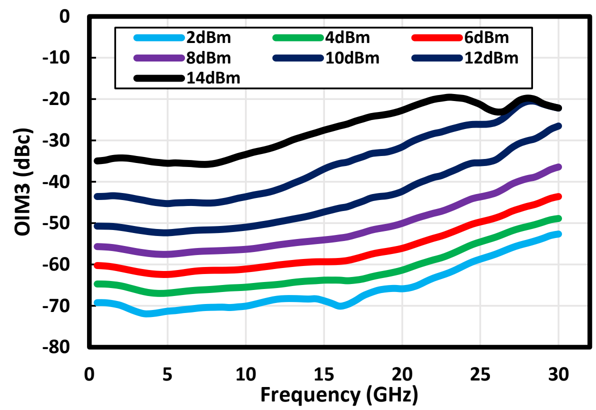


Figure 1-47. 2nd Harmonic vs. Power at 5V/100 mA

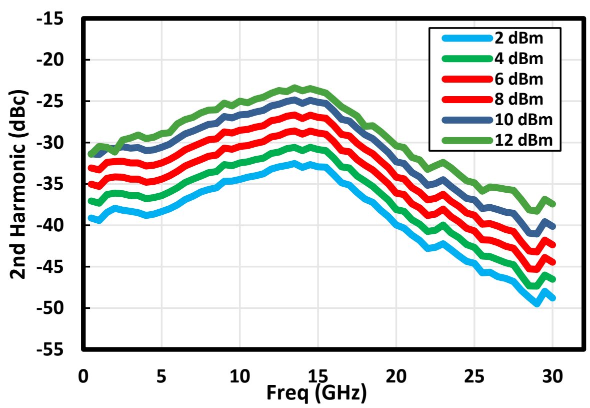


Figure 1-48. 2nd Harmonic vs. Power at 6V/150 mA

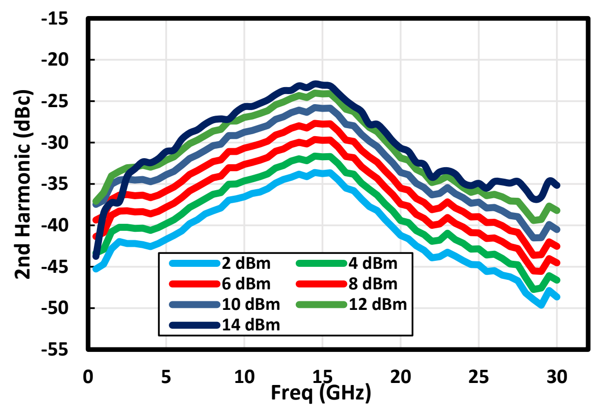
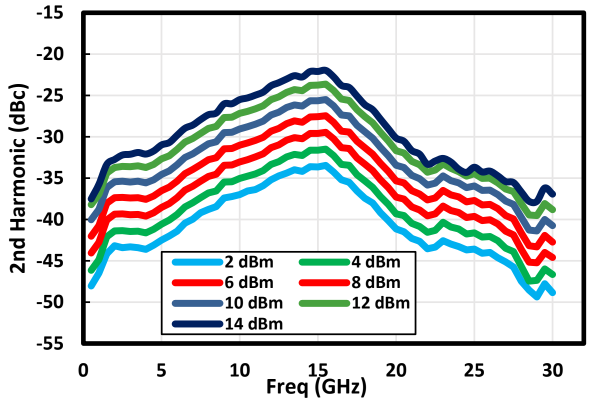


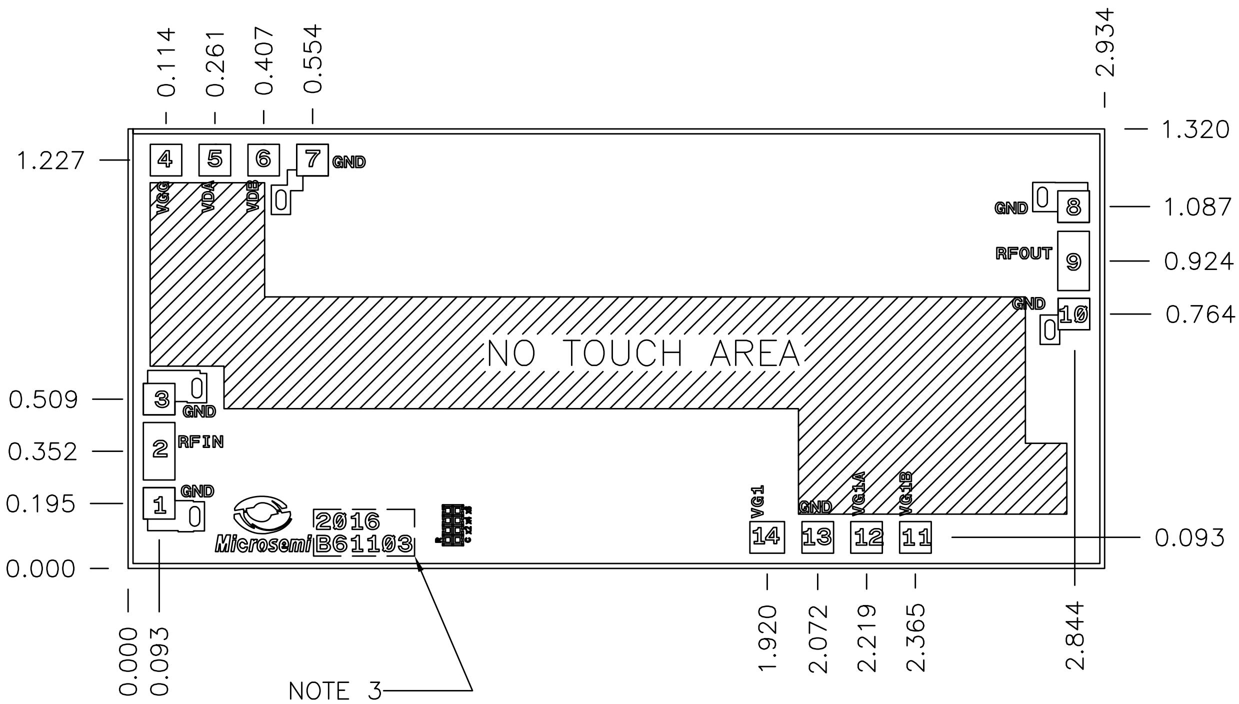
Figure 1-49. 2nd Harmonic vs. Power at 7V/180 mA



2. Die Specifications

The following illustration shows the chip outline of the MMA041AA device. Dimensions are in millimeter and are relative to the zero datum locations shown in the drawing. The minimum bond pad size is 0.1 mm × 0.1 mm. Both the bond pad surface and the backside metal are 3 µm gold. The die thickness is 0.1 mm. The backside is the DC/RF ground. The airbridge keep–out polygon region is shown inside.

Figure 2-1. Die Outline Drawing



PAD No.	Description	PAD Size
1	GND	0.97 × 0.97
2	RFIN	0.97 × 0.177
3	GND	0.97 × 0.97
4	VGG	0.97 × 0.97
5	VDA	0.97 × 0.97
6	VDB	0.97 × 0.97
7	GND	0.97 × 0.97
8	GND	0.97 × 0.97
9	RFOUT	0.97 × 0.177
10	GND	0.97 × 0.97
11	VG1B	0.97 × 0.97
12	VG1A	0.97 × 0.97
13	GND	0.97 × 0.97
14	VG1	0.97 × 0.97

Notes:

1) Dimension are in millimeters.

2) Die thickness: 0.100 millimeters.

3) Making info:
2016 = Design date
B61103 = Die name

For additional packaging information, contact your Microchip sales representative.

Table 2-1. I/O Pad Description

Pad Number	Pad Name	Pad Description
2	RFIN	DC–coupled and matched to 50Ω.
9	RFOUT + VDD	DC–decoupled and matched to 50Ω. Used for VDD bias.
4	VG2	Second Gate Bias. Connect to VD1A (Optional could be used for gain control by applying external bias in the range of VDD +/- 30%)
5, 6	VD1A, VD1B	Low-frequency termination. Connect bypass capacitors per application circuit below. (Do NOT apply VDD bias to this connections)
11, 12	VG1A, VG1B	Low-frequency termination. Connect bypass capacitors per application circuit below at Figure 51
14	VG1	Gate control for amplifier. Adjust to achieve IDD = 150 mA
1, 3, 7,8, 10, 13	Ground	RF/DC Ground pads, not used in typical applications.
Backside paddle	RF/DC GND	Must be connected to RF/DC Ground

3. Application Circuit

Figure 3-1. Application Circuit: Schematic

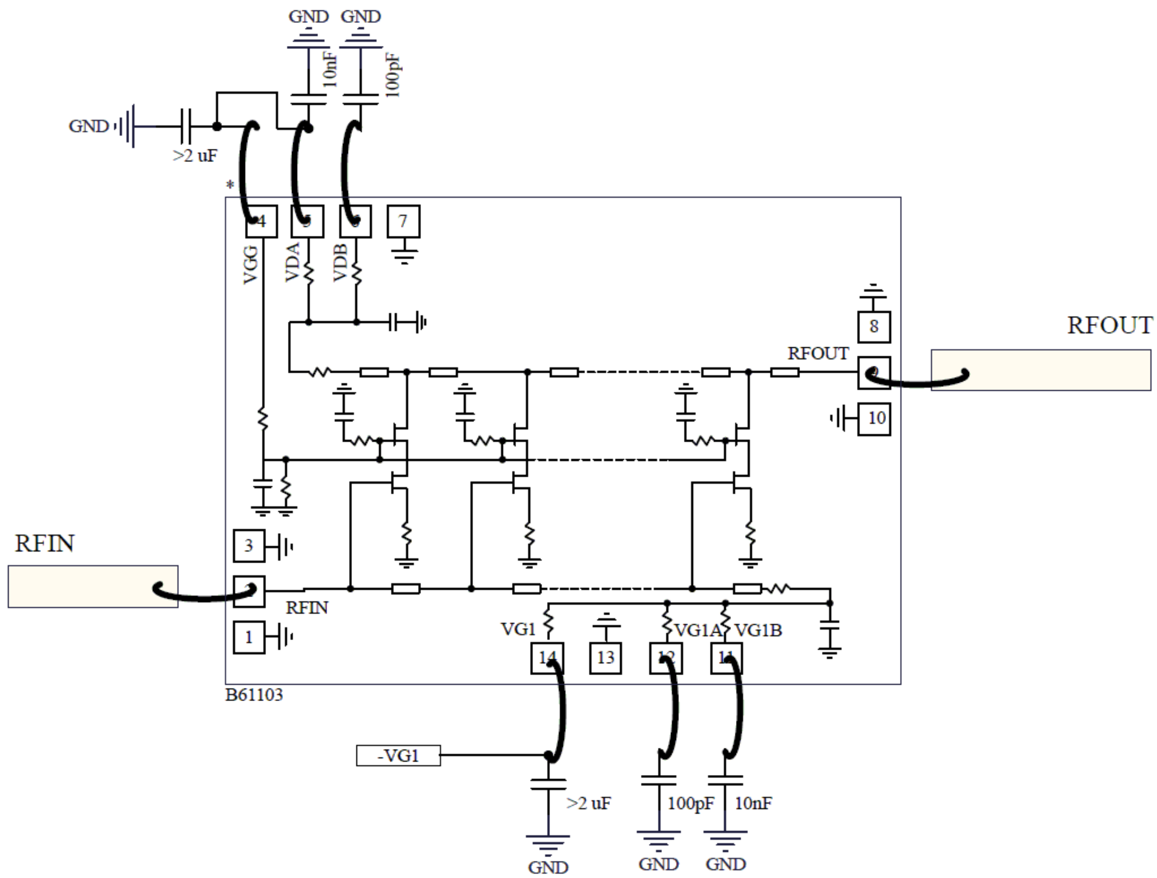


Figure 3-2. Test Circuit DC–26 GHz: Assembly Drawing

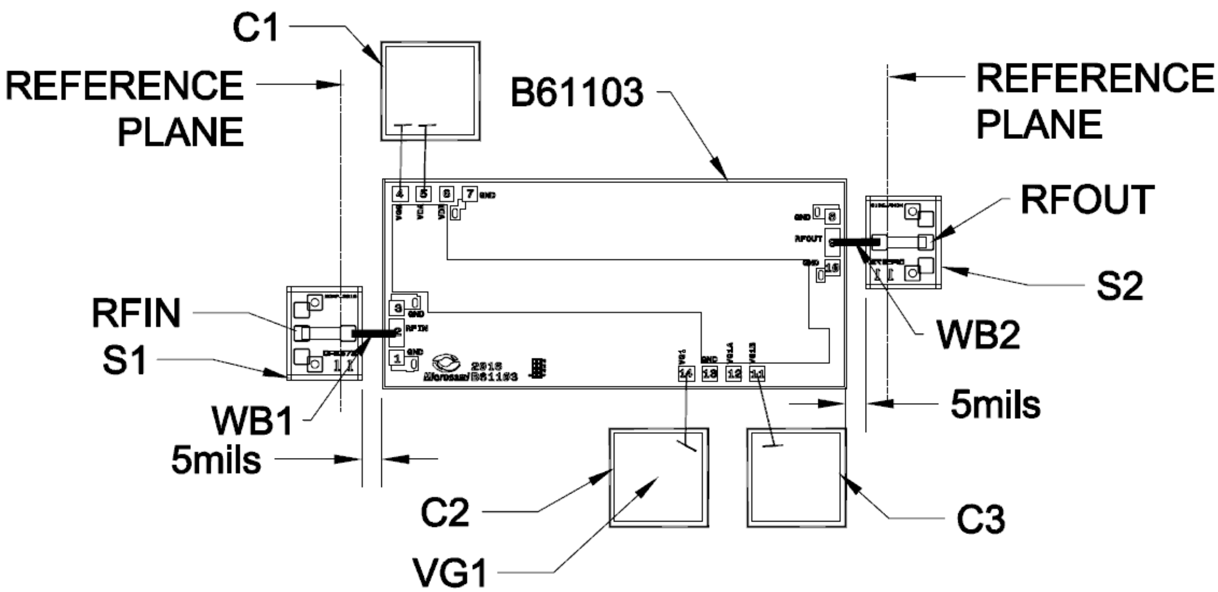


Table 3-1. List of Materials for Assembly Drawing

Reference	Part Number	Description
B61103	MMA041AA	Amplifier Die
C1 ... C3	160U02A102MT4W	Johanson Dielectric SLC 1 nF (Values could be different from the Application Circuit Schematic for ease of Test Circuit Assembly)
S1, S2	E57311	Microchip Probe Launchers, calibrated with the TRL kit to Ref. Planes shown
WB1, WB2	744-903-06	Microchip 2 mils Gold Ribbon, Should be as short as possible
RFIN/RFOUT		Location of the Input/Output GSG (150 µm) probes
VG1		Needle contact location for DC connection to VG1 (should be grounded if not used)

Table 3-2. Bias Sequence

Bias Sequence
1) Set the gate voltage VG1 to –1V
2) Set drain voltage VDD to 6V (or as applications require)
3) Adjust the Gate Voltage by increments <0.01V until current reaches required value

4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Gallium Arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA041AA	Bare die
MMA041PP5	5 mm × 5 mm, 32L SMT
MMA041PP5/TR	Tape and reel
MMA041PP5E	Evaluation board for MMA041PP5

4.3 Packing Information

Standard Format
Gel pack
50 pieces per pack

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
B	06/2024	Electrical data updated and performance curves reformatted.
A	07/2022	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00004636.
Initial release (Microsemi Revision A)	2016	Document created.

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