

2A Sequencing LDO with Tracking and Ramp Control

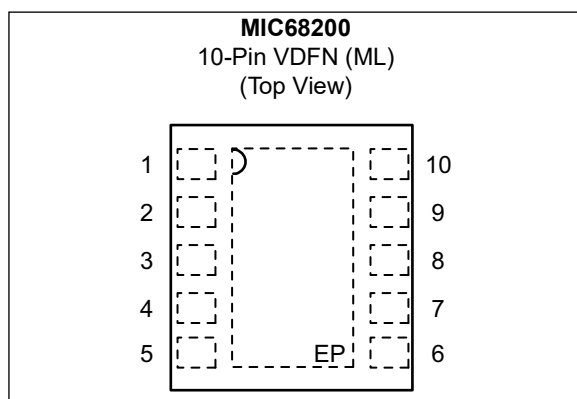
Features

- Stable with 4.7 μF Ceramic Capacitor
- Input Voltage Range: 1.65V to 5.5V
- 0.5V Reference
- $\pm 1.0\%$ Initial Output Tolerance
- 2A Maximum Output Current – Peak Start Up
- 1A Continuous Operating Current
- Tracking on Turn-On and Turn-Off with Pin Strapping
- Timing Controlled Sequencing On/Off
- Programmable Ramp Control for In-Rush Current Limiting and Slew Rate Control of the Output Voltage on Turn-On and Turn-Off
- Power-on Reset (POR) Supervisor with Programmable Delay Time
- Single Host can Control Multiple Client Regulators with Tracking Output Voltages
- Tiny 3 mm x 3 mm VDFN Package
- Maximum Dropout ($V_{\text{IN}} - V_{\text{OUT}}$) of 400 mV over Temperature at 1A Output Current
- Fixed and Adjustable Output Voltages
- Excellent Line and Load Regulation Specifications
- Logic Controlled Shutdown
- Thermal Shutdown and Current Limit Protection

Applications

- FPGA/PLD Power Supply
- Networking/Telecom Equipment
- Microprocessor Core Voltage
- High Efficiency Linear Post Regulator
- Sequenced or Tracked Power Supply

Package Type



General Description

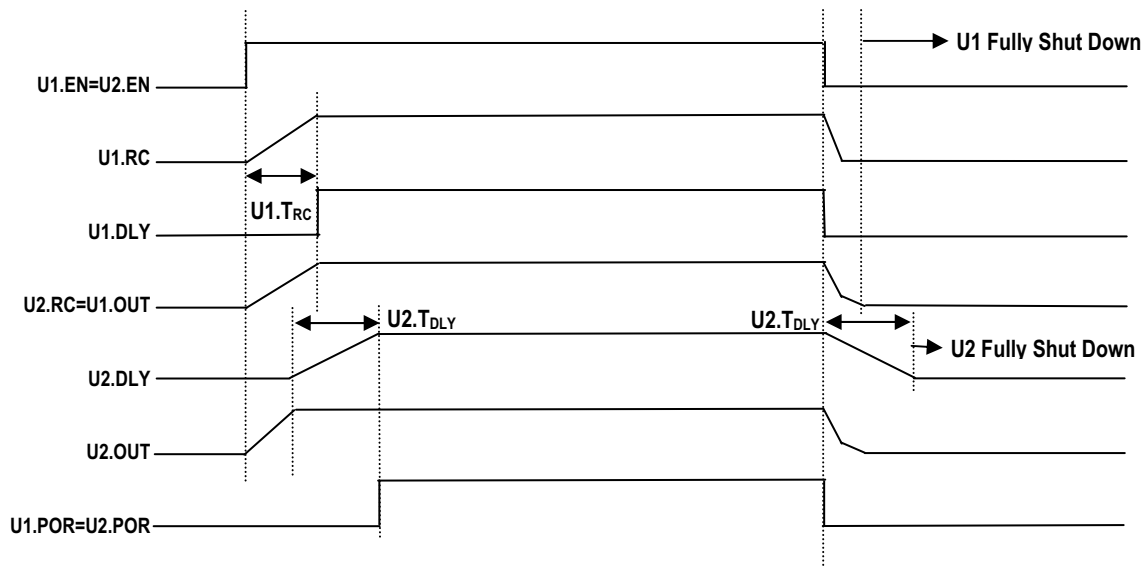
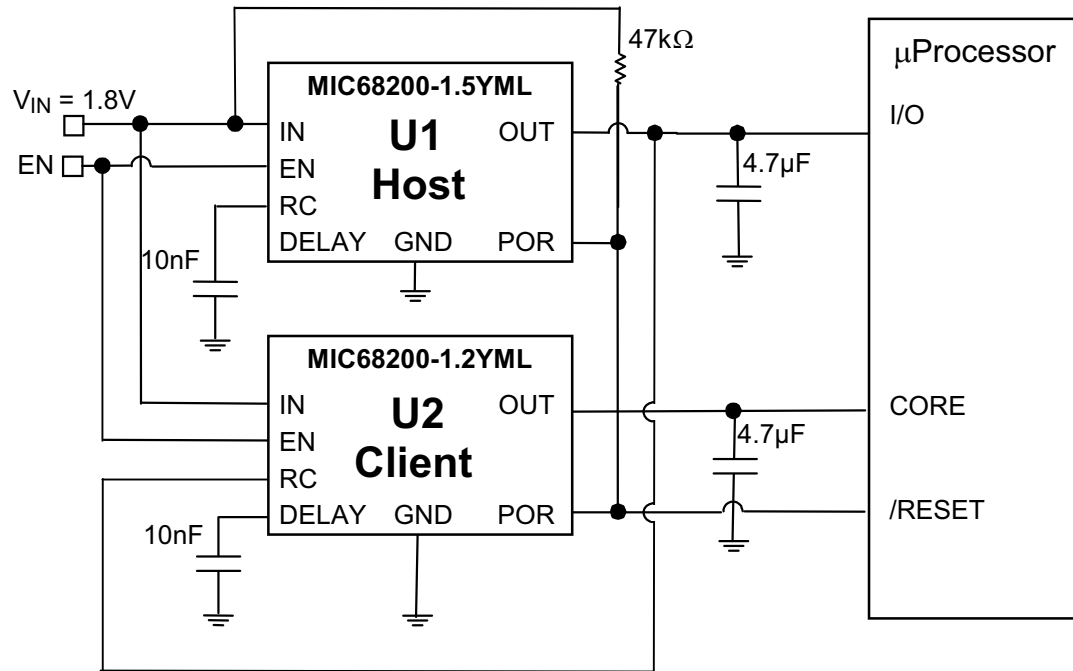
The MIC68200 is a high peak current LDO regulator designed specifically for powering applications such as FPGA core voltages that require high start up current with lower nominal operating current. Capable of sourcing 2A of current for start-up, the MIC68200 provides high power from a small VDFN leadless package. The MIC68200 can also implement a variety of power-up and power-down protocols such as sequencing, tracking, and ratiometric tracking.

The MIC68200 operates from a wide input range of 1.65V to 5.5V, which includes all of the main supply voltages commonly available today. It is designed to drive digital circuits that require low voltage at high currents (i.e. PLDs, DSP, microcontroller, etc.). The MIC68200 incorporates a delay pin (DLY) for control of power-on reset output (POR) at turn-on and power-down delay at turn-off. In addition, there is a ramp control pin (RC) for either tracking applications or output voltage slew rate adjustment at turn-on. This is important in applications where the load is highly capacitive and in-rush currents can cause supply voltages to fail and microprocessors or other complex logic chips to hang up.

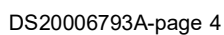
Multiple MIC68200s can be daisy chained in two modes. In tracking mode the output voltage of the Host drives the RC pin of a Client so that the Client tracks the main regulator during turn-on and turn-off. In sequencing mode the POR of the Host drives the enable (EN) of the Client so that it turns on after the Host and turns off before (or after) the Host. This behavior is critical for power-up and power-down control in multi-output power supplies. The MIC68200 is fully protected offering both thermal and current limit protection and reverse current protection.

The MIC68200 has a junction temperature range of -40°C to $+125^{\circ}\text{C}$ and is available in fixed and adjustable voltage options. The MIC68200 is offered in the tiny 10-pin 3 mm x 3 mm VDFN package.

Tracking Dual Power Supply for I/O and Core Voltage of μ Processor



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN})	+6V
Enable Input Voltage (V_{EN})	0V to $V_{IN} + 0.3V$
Power-On Reset (V_{POR})	$V_{IN} + 0.3V$
Ramp Control (V_{RC})	$V_{IN} + 0.3V$
Power Dissipation (P_D , Note 1)	Internally Limited
ESD Rating (Note 2)	2 kV

Operating Ratings ‡

Supply Voltage	+1.65V to +5.5V
Enable Input Voltage (V_{EN})	0V to V_{IN}
Ramp Control (V_{RC})	0V to 5.5V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 k Ω in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $T_A = +25^\circ\text{C}$ with $V_{IN} = V_{OUT} + 1V$; $V_{EN} = V_{IN}$; $I_{OUT} = 10\text{ mA}$; **bold** values valid for $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, unless noted. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy		-2	—	2	%	$10\text{ mA} < I_{OUT} < I_{L(MAX)}$, $V_{OUT} + 1 \leq V_{IN} \leq 5.5V$
Feedback Voltage	V_{FB}	0.49	0.50	0.51	V	Adjustable version only
Feedback Current	I_{FB}	—	10	—	nA	Adjustable version only
Output Voltage Line Regulation	$\Delta V_{OUT}/(V_{OUT}/\Delta V_{IN})$	—	0.06	0.5	V	$V_{IN} = V_{OUT} + 1V$ to 5.0V
Output Voltage Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.3	1	%	$I_L = 0\text{ mA}$ to 2A
Dropout Voltage	V_{DO}	—	140	250	mV	$I_L = 500\text{ mA}$
		—	200	400		$I_L = 1.0A$
		—	300	600		$I_L = 2.0A$
Ground Pin Current	I_{GND}	—	1.5	—	mA	$I_L = 10\text{ mA}$
		—	7	15		$I_L = 500\text{ mA}$
		—	15	30		$I_L = 1.0A$
		—	42	80		$I_L = 2.0A$
Shutdown Current	I_{SD}	—	0.01	10	μA	$V_{EN} = 0V$; $V_{OUT} = 0V$
Current Limit	I_{LIM}	2.0	3.4	6.0	A	$V_{OUT} = 0V$; $V_{IN} = 3.0V$
Start-Up Time	t_{SU}	—	25	150	μs	$V_{EN} = V_{IN}$; $C_{RC} = \text{Open}$

MIC68200

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $T_A = +25^\circ\text{C}$ with $V_{IN} = V_{OUT} + 1\text{V}$; $V_{EN} = V_{IN}$; $I_{OUT} = 10\text{ mA}$; **bold** values valid for $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, unless noted. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Enable Input						
Enable Input Threshold	V _{EN_TH}	1	—	—	V	Regulator enable
		—	—	0.2		Regulator shutdown
Enable Hysteresis	V _{EN_HYS}	50	100	250	mV	—
Enable Input Current	I _{EN}	—	0.8	—	μA	V _{IL} ≤ 0.2V (Regulator shutdown)
		—	2	—		V _{IH} ≤ 1V (Regulator enable)
POR Output						
POR Leakage Current	I _{POR(LEAK)}	—	—	1	μA	V _{POR} = 5.5V; POR = High
		—	—	2		
Output Logic Low Voltage	V _{POR(LO)}	—	60	90	mV	Undervoltage condition, I _{POR} = 1 mA
Power-On Reset Voltage Threshold	V _{POR}	7.5	10	12.5	%	V _{OUT} Ramping Up, % of V _{OUT} below nominal
		10	12.5	15		V _{OUT} Ramping Down, % of V _{OUT} below nominal
Delay Current	I _{DELAY}	0.7	1	1.3	μA	V _{DELAY} = 0.75V
Delay Voltage	V _{DELAY}	1.185	1.235	1.285	V	V _{POR} = High, Note 2
Ramp Control						
Ramp Control Current	I _{RC}	0.7	1	1.3	μA	—
Output Discharge Current	I _{DIS(OUT)}	25	45	70	mA	V _{OUT} = 0.5V _{REF} , V _{RAMP} = 0V, Note 3
Fixed Tracking Accuracy		–50	25	100	mV	200 mV < V _{RC} < V _{TARGET} ; Measure (V _{OUT} – V _{RC}), Note 4
Adjustable Tracking Accuracy		2	15	50	mV	Measure (V _{OUT} – V _{RC} x (V _{TARGET} /500 mV)), Note 4

Note 1: Specification for packaged product only.

2: Timer High Voltage along with Delay pin current (1 μA nominal) determines the delay per μF of capacitance. Typical delay is 1.1 sec/ μF .

3: Discharge current is the current drawn from the output to ground to actively discharge the output capacitor during the shutdown process.

4: V_{TARGET} is the output voltage of an adjustable with customer resistor divider installed between V_{OUT} and the ADJ/SNS pin, or the rated output voltage of a fixed device.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	$^\circ\text{C}$	—
Storage Temperature	T_S	–65	—	+150	$^\circ\text{C}$	—
Package Thermal Resistances						
Thermal Resistance, VDFN 10-Ld	θ_{JA}	—	60	—	$^\circ\text{C/W}$	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

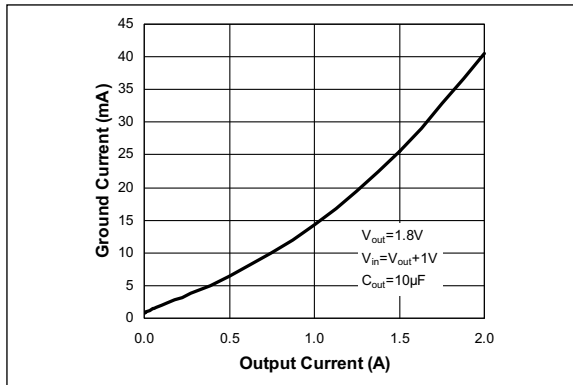


FIGURE 2-1: Ground Current vs. Output Current.

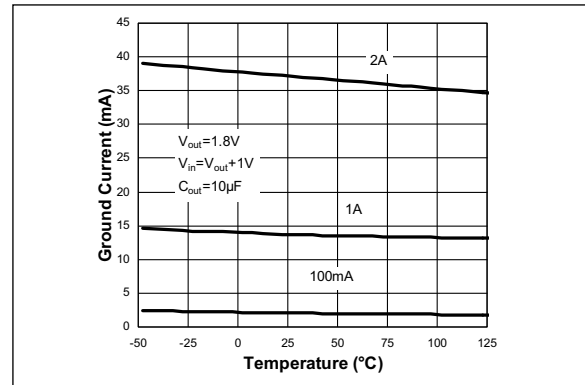


FIGURE 2-4: Ground Current vs. Temperature.

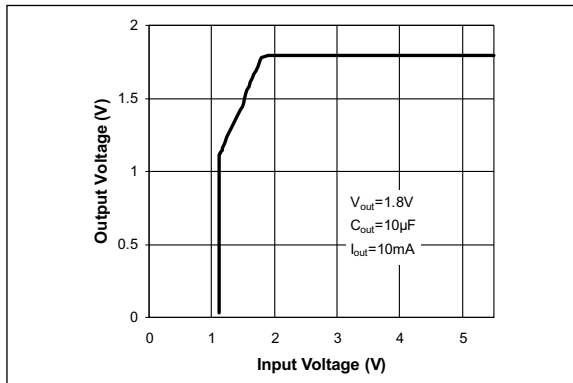


FIGURE 2-2: Output Voltage vs. Input Voltage.

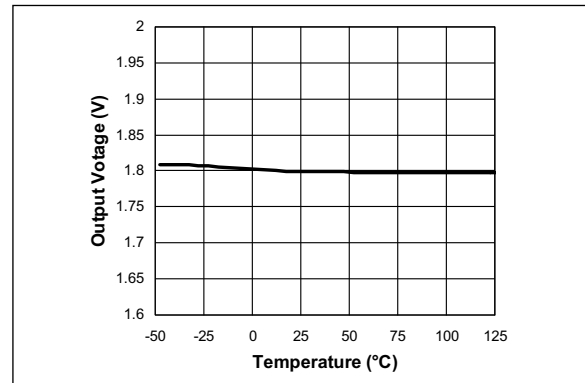


FIGURE 2-5: Output Voltage vs. Temperature.

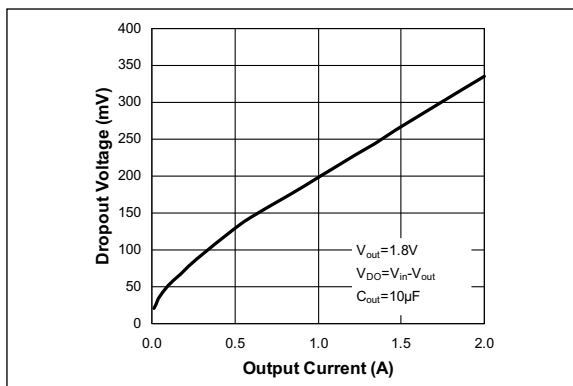


FIGURE 2-3: Dropout Voltage vs. Output Current.

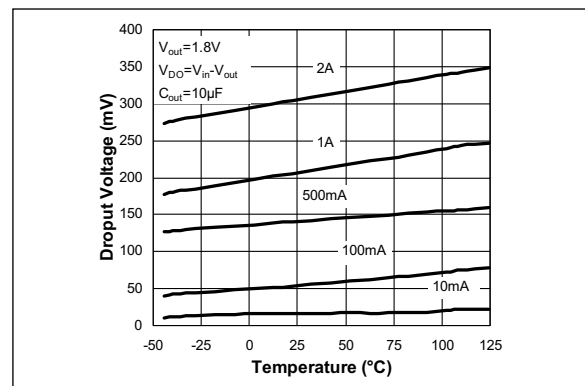


FIGURE 2-6: Dropout Voltage vs. Temperature.

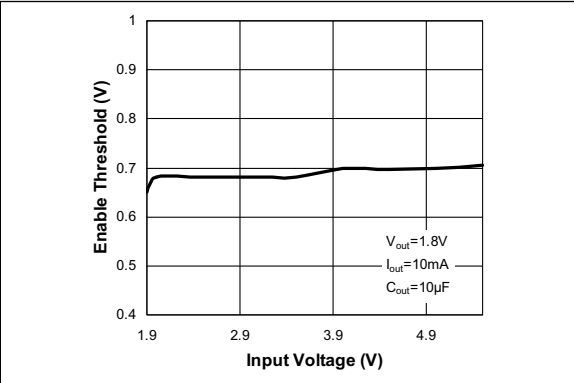


FIGURE 2-7: Enable Threshold vs. Input Voltage.

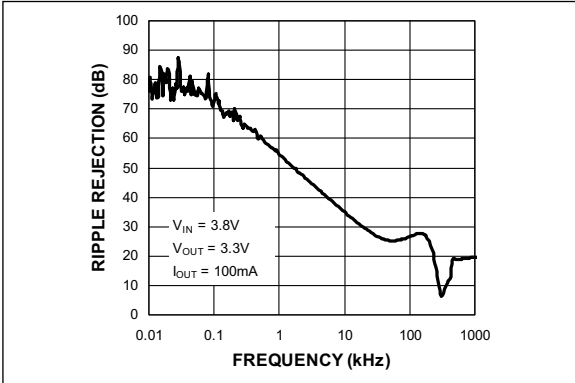


FIGURE 2-10: PSRR ($V_{IN} = 3.8V$, $I_{OUT} = 100\text{ mA}$).

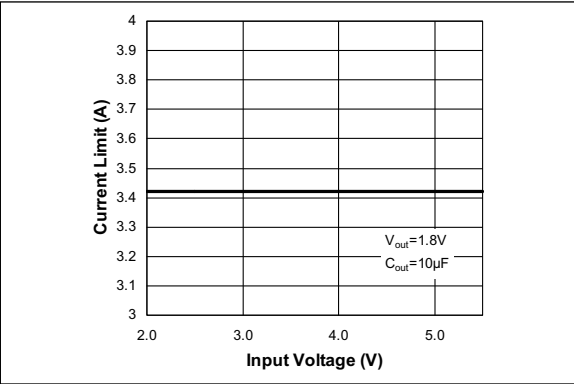


FIGURE 2-8: Current Limit vs. Input Voltage.

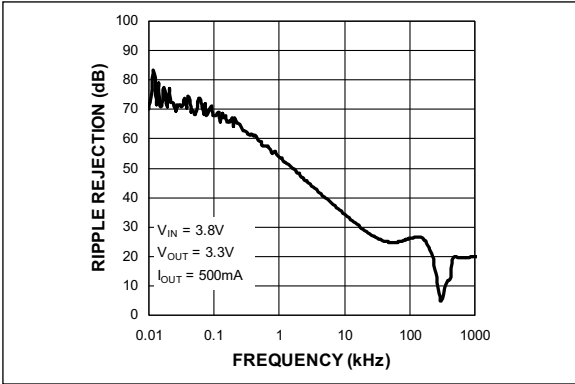


FIGURE 2-11: PSRR ($V_{IN} = 3.8V$, $I_{OUT} = 500\text{ mA}$).

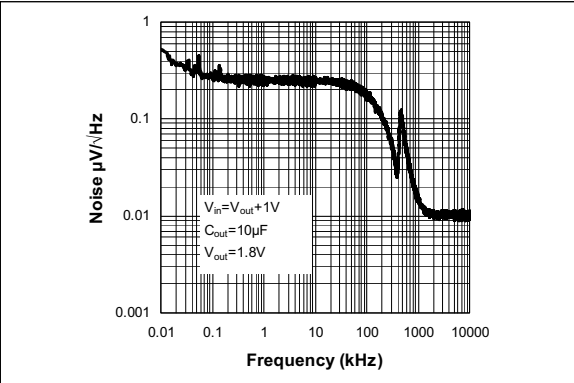


FIGURE 2-9: Output Noise Spectral Density.

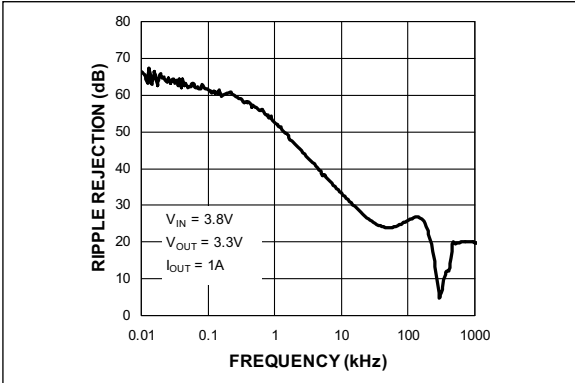


FIGURE 2-12: PSRR ($V_{IN} = 3.8V$, $I_{OUT} = 1A$).

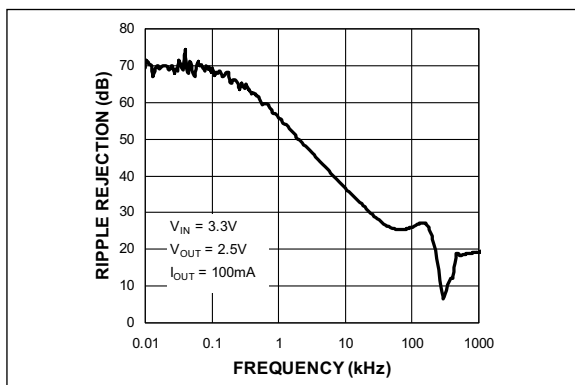


FIGURE 2-13: PSRR ($V_{IN} = 3.3V$, $I_{OUT} = 100\text{ mA}$).

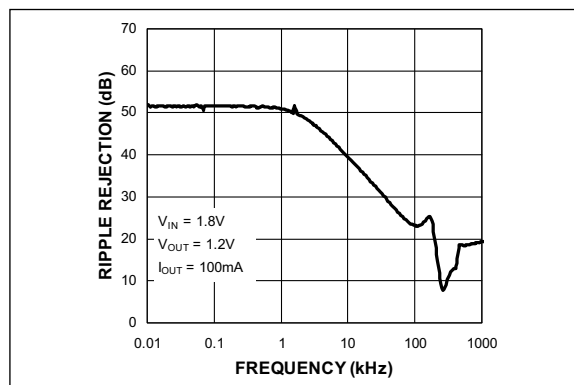


FIGURE 2-16: PSRR ($V_{IN} = 1.8V$, $I_{OUT} = 100\text{ mA}$).

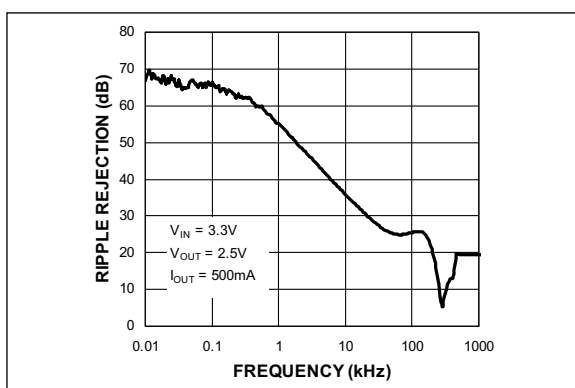


FIGURE 2-14: PSRR ($V_{IN} = 3.3V$, $I_{OUT} = 500\text{ mA}$).

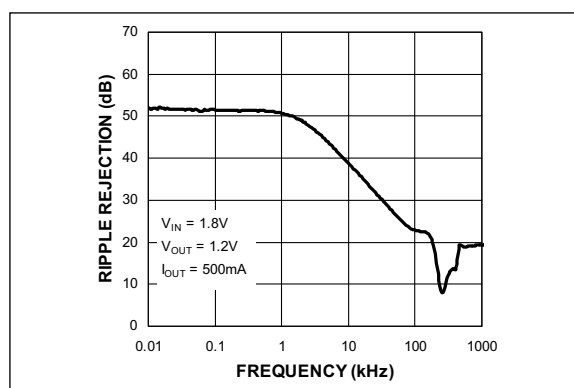


FIGURE 2-17: PSRR ($V_{IN} = 1.8V$, $I_{OUT} = 500\text{ mA}$).

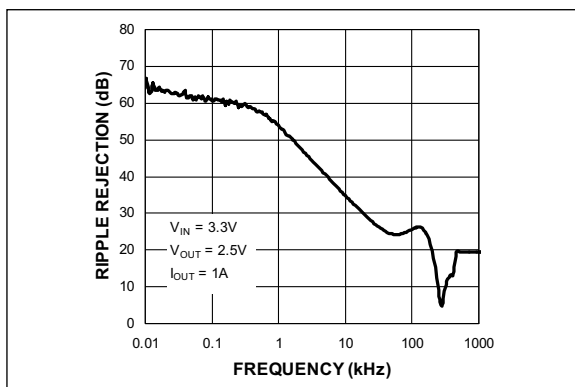


FIGURE 2-15: PSRR ($V_{IN} = 3.3V$, $I_{OUT} = 1A$).

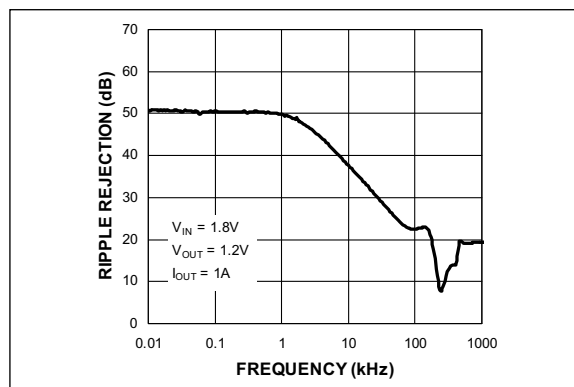


FIGURE 2-18: PSRR ($V_{IN} = 1.8V$, $I_{OUT} = 1A$).

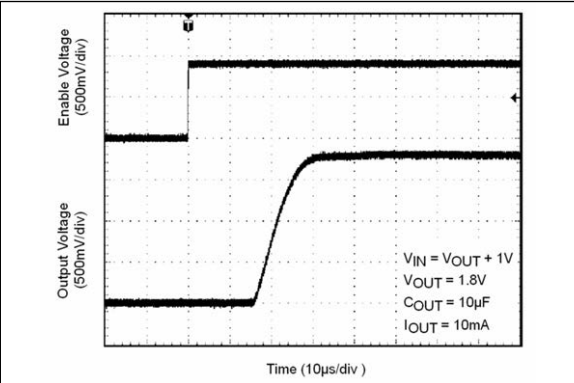


FIGURE 2-19: Enable Turn-On.

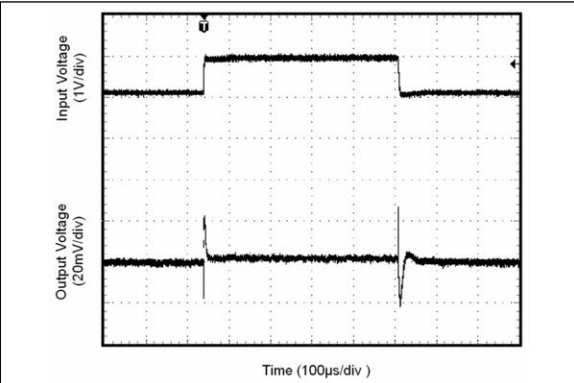


FIGURE 2-20: Line Transient.

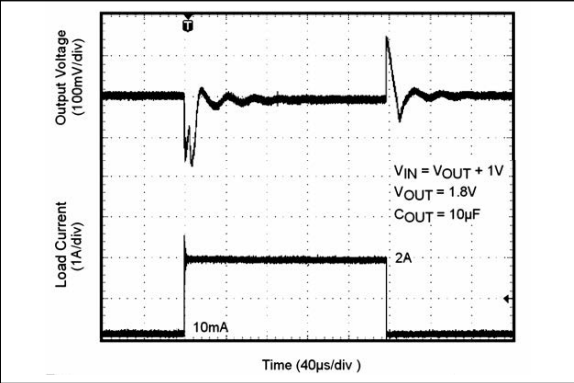


FIGURE 2-21: Load Transient.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#). Pin numbering may change depending on layout considerations.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number Fixed	Pin Number Adjustable	Pin Name	Description
1, 2	1, 2	IN	Input: Input voltage supply pin. Place a capacitor to ground to bypass the input supply
3	3	DLY	Delay: Capacitor to ground sets internal delay timer. Timer delays power-on reset (POR) output at turn-on and ramp down at turn-off.
4	4	RC	Ramp Control: Voltage driven for tracking applications. Capacitor to ground sets slew rate during start-up.
5	5	EN	Enable (Input): CMOS compatible input. Logic high = enable and logic low = shutdown.
6, EP	6, EP	GND	Ground: EP is connected to ground.
7	7	POR	Power-on Reset: Open-drain output device indicates when the output is in regulation. High (open) means device is regulating within 10%. POR onset can be delayed using a single capacitor from Delay to ground.
8	8	SNS	Adjustable regulators: Feedback input. Connect to external resistor voltage divider. Fixed regulators: Sense pin. Connect to output at load for point-of-load regulation.
9, 10	9, 10	OUT	Output Voltage: Output of voltage regulator. Place capacitor to ground to bypass the output voltage. Minimum load current is 100 μ A. Nominal bypass capacitor is 4.7 μ F ceramic.

4.0 APPLICATION INFORMATION

4.1 Enable Input

The MIC68200 features a TTL/CMOS compatible positive logic enable input for on/off control of the device. High ($>1V$) enables the regulator while low ($<0.2V$) disables the regulator. In shutdown the regulator consumes very little current (only a few microamperes of leakage). For simple applications the enable (EN) can be connected to V_{IN} (IN). While MIC68200 only requires a few microamps of enable current to turn on, actual enable pin current will depend on the overdrive (voltage exceeding 1V) in each particular application.

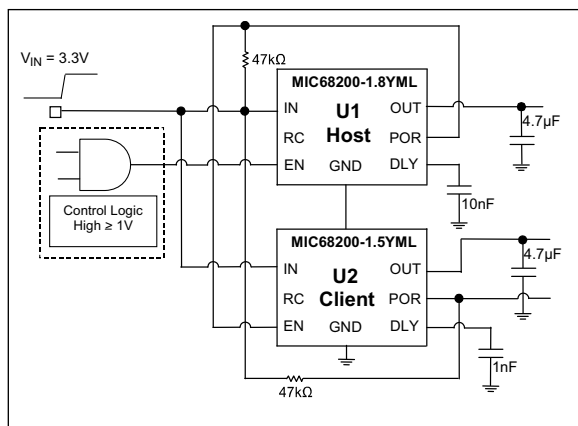


FIGURE 4-1: Enable Connections for Logic Driven Input.

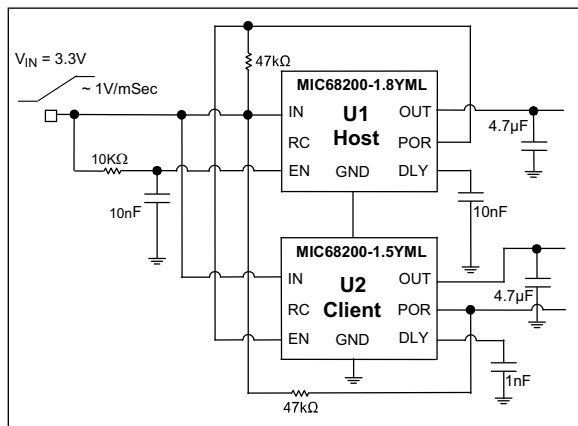


FIGURE 4-2: Enable Connection for V_{IN} -Driven and/or Slow Rise Time Inputs.

4.2 Input Capacitor

An input capacitor of 0.1 μF or greater is recommended when the device is more than 4 inches away from the bulk supply capacitance, or when the supply is a battery. Small, surface mount chip capacitors can be used for the bypassing. The capacitor should be placed within 1 inch of the device for optimal performance. Larger values will help to improve ripple rejection by bypassing the regulator input, further improving the integrity of the output voltage.

4.3 Output Capacitor

The MIC68200 requires an output capacitor for stable operation. As a μCap LDO, the MIC68200 can operate with ceramic output capacitors of 4.7 μF or greater with ESRs ranging from a 3 m Ω to over 300 m Ω . Values of greater than 4.7 μF improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their superior temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Larger output capacitances can be achieved by placing tantalum or aluminum electrolytics in parallel with the ceramic capacitor. For example, a 100 μF electrolytic in parallel with a 4.7 μF ceramic can provide the transient and high frequency noise performance of a 100 μF ceramic at a significantly lower cost. Specific undershoot/overshoot performance will depend on both the values and ESR/ESL of the capacitors.

4.4 Adjustable Regulator Design

The adjustable MIC68200 output voltage can be programmed from 0.5V to 5.5V using a resistor divider from output to the SNS pin. Resistors can be quite large, up to 1 M Ω because of the very high input impedance and low bias current of the sense amplifier. Typical sense input currents are less than 30 nA which causes less than 0.3% error with R1 and R2 less than or equal to 100 k Ω . For large value resistors (>50 k Ω) R1 should be bypassed by a small capacitor ($C_{FF} = 0.1$ μF bypass capacitor) to avoid instability due to phase lag at the ADJ/SNS input.

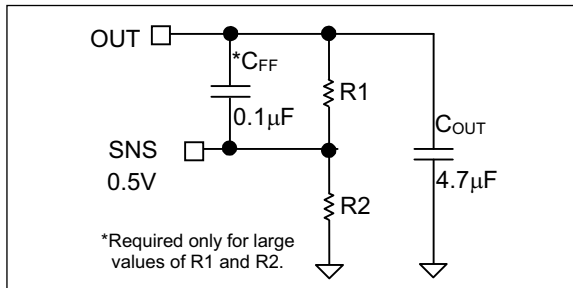


FIGURE 4-3: Adjustable Regulator with Resistors.

The output resistor divider values are calculated by:

EQUATION 4-1:

$$V_{OUT} = 0.5V \times \left(\frac{R1}{R2} + 1 \right)$$

4.5 Power-on Reset (POR) and Delay (DLY)

The power-on reset output (POR) is an open-drain N-Channel device requiring a pull-up resistor to either the input voltage or output voltage for proper voltage levels. POR is driven by the internal timer so that the release of POR at turn-on can be delayed for as much as 1 second. POR is always pulled low when enable (EN) is pulled low or the output goes out of regulation by more than 10% due to loading conditions.

The internal timer is controlled by the DLY pin which has a bidirectional current source and two limiting comparators. A capacitor connected from DLY to GND sets the delay time for two functions. On start up, DLY sets the time from power good to the release of the POR. At shut down, the delay sets the time from disable (EN pin driven low) to actual ramp down of the output voltage. The current source is $\pm 1 \mu A$, which charges the capacitor from ~ 150 mV (nominal disabled DLY voltage) to $\sim 1.25V$. At turn on, the DLY cap begins to charge when the output voltage reaches 90% of the target value. When the capacitor reaches 1.25V, the output of the POR is released to go high. At turn off, the DLY cap begins to discharge when the EN is driven low. When the cap reaches ~ 150 mV the output is ramped down. Both delays are nominally the same, and are calculated by the same formula:

EQUATION 4-2:

$$t_{DLY} = 1.1 \times \left(\frac{C_{DLY}}{1 \mu A} \right)$$

Scale	factor	is:
1.1		seconds/microfarad,
1.1		milliseconds/nanofarad, or
1.1		microseconds/picofarad

t_{DLYOFF} is the time from lowering of EN to the start of ramp down on the off cycle. t_{POR} is the time from raising of EN to the release (low to high edge) of the POR. This behavior means that a microprocessor or other complex logic system is guaranteed that power has been good for a known time before the POR is released, and they are further guaranteed that once POR is pulled low, they have a known time to 'tidy up' memory or other registers for a well controlled shutdown. In Host/Client configurations the timers can be used to assure that the Host is always accurately regulating when the Client is on.

4.6 Ramp Control

The ramp control (RC) has a bidirectional current source and a sense amplifier, which together are used to control the voltage at the output. When RC is below the target voltage (nominal output voltage for fixed voltage parts, 0.5V for adjustable parts) the RC pin controls the output voltage. When RC is at or above the target voltage, the output is controlled by the internal regulator.

4.6.1 TRACKING APPLICATIONS: DRIVING RC FROM A VOLTAGE SOURCE

Fixed Parts: If RC is driven from another (Host) regulator, the two outputs will track each other until the Host exceeds the target voltage of the Client regulator. Typically, the output of the MIC68200 will track above the RC input by 30 mV to 70 mV. This offset is designed to allow Host/Client tracking of same-voltage regulators. Without the offset, same-voltage Host/Client configurations could suffer poor regulation.

Adjustable Parts: The RC pin on adjustable versions operates from 0V to 0.5V. To implement tracking on an adjustable version, an external resistor divider must be used. This divider is the nearly same ratio as the voltage setting divider used to drive the SNS/ADJ pin. It is recommended that the ratio be adjusted to track ~ 50 mV (2% to 3%) above the target voltage if the Host and Client are operating at the same target voltage.

MIC68200

4.6.2 RAMP UP: CAP-CONTROLLED SLEW RATE

If a capacitor is connected to RC, the bidirectional current source will charge the cap during startup and discharge the cap during shutdown. The size of the capacitor and the RC current (1 μ A nom) control the slew rate of the output voltage during startup. For example, to ramp up a 1.8V regulator from zero to full output in 10 ms requires a 5.6 nF capacitor.

For Fixed Versions:

EQUATION 4-3:

$$t_{RC} = V_{OUT} \times \left(\frac{C_{RC}}{1 \mu A} \right)$$

$$SR_{ON} = \frac{1 \mu A}{C_{RC}}$$

Similarly, to slew an adjustable (any output voltage) from 0 to full output in 10 ms requires a 20 nF cap.

For Adjustable Versions:

EQUATION 4-4:

$$t_{RC} = 0.5 V \times \left(\frac{C_{RC}}{1 \mu A} \right)$$

$$SR_{ON} = 2 V_{OUT} \times \left(\frac{1 \mu A}{C_{RC}} \right)$$

4.6.3 RAMP DOWN: TURN-OFF SLEW RATE

When EN is lowered and the DLY pin has discharged, the RC pin and the OUT pin slew toward zero. For fixed voltage devices, the RC pin slew rate is 2 to 3 times the SR_{ON} defined above. For adjustable voltage devices, the RC pin slew is much higher. In both cases, turn-off slew rate may be determined by the RC pin for low values of output capacitor or by the maximum discharge current available at the output for large values of output capacitor. Turn-off slew rate is not a specified characteristic of the MIC68200.

4.7 Sequencing Configurations

Sequencing refers to timing-based Host/Client control between regulators. It allows a Host device to control the start and stop timing of a single or multiple Client devices. In typical sequencing, the Host POR drives the Client EN. The sequence begins with the Host EN driven high. The Host output ramps up and triggers the Host DLY when the Host output reaches 90%. The Host DLY then determines when the POR is released to enable the Client device. When the Host EN is driven low, the Host POR is immediately pulled low causing the Client to ramp down. However, the Host output will

not ramp down until the Host DLY has fully discharged. In this way, the Host power can remain good after the Client has been ramped down.

In sequencing configurations, the Host DLY controls the turn-on time of the Client and the Client DLY controls the turn-off time of the Client.

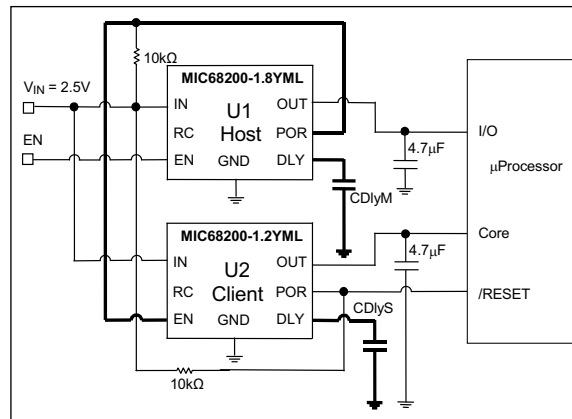


FIGURE 4-4: Sequencing Connections.

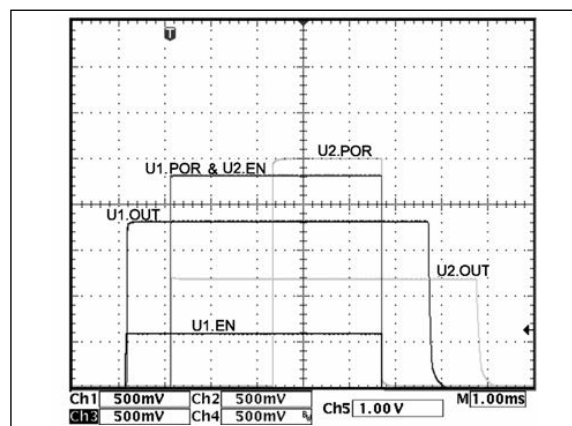


FIGURE 4-5: Delayed Sequencing ($CDLYS > CDLYM$; $CDLYS = 2$ nF, $CDLYM = 1$ nF).

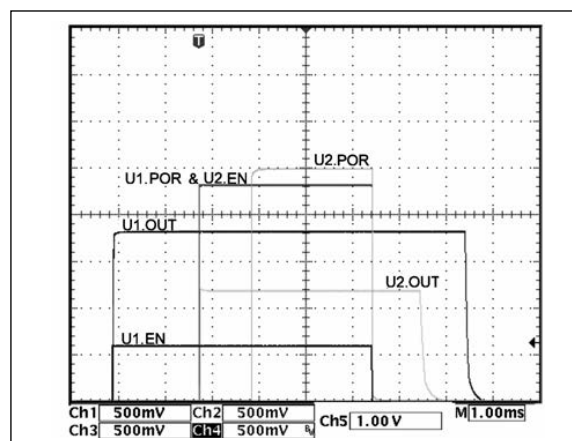


FIGURE 4-6: Windowed Sequencing ($CDLYS > CDLYM$; $CDLYS = 1$ nF, $CDLYM = 2$ nF).

4.8 Tracking Configurations

4.8.1 NORMAL TRACKING

In normal tracking, the Client RC pin is driven from the Host output. The internal control buffering ensures that the output of the Client is always slightly above the Host to further ensure that the Client properly regulates (based on its own internal reference) if the Host and Client are both fixed-voltage devices of the same output voltage. The schematic and plot in [Figure 4-7](#) show a 1.2V device tracking a 1.8V device through the entire turn-on/turn-off sequence. Note that because the RC pin will overdrive the target voltage (to ensure proper regulation) the ramp down delay is longer than the POR delay during turn-on.

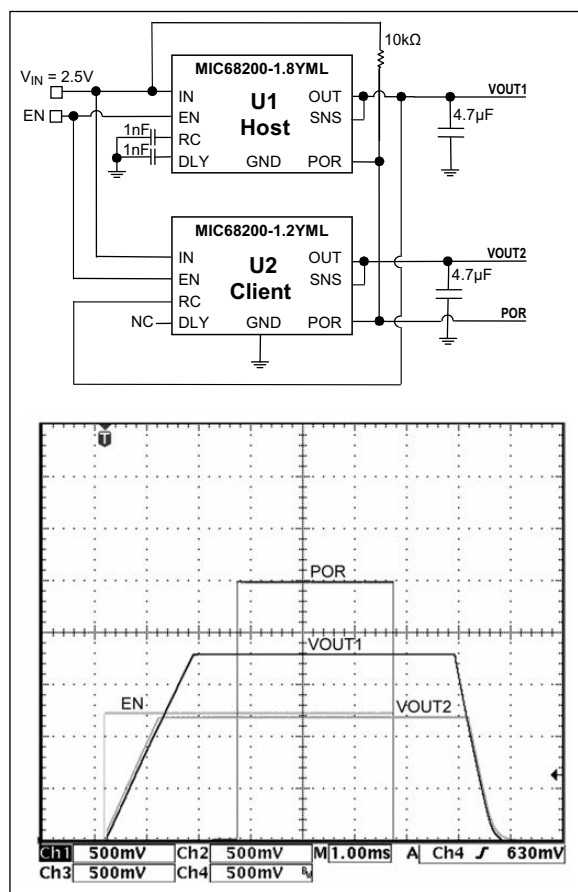


FIGURE 4-7: Fixed-Voltage Devices.

Fixed voltage versions of MIC68200 have two internal voltage dividers: one for setting the output voltage and the other for driving the tracking circuitry. Adjustable parts have up to two external dividers: one from output to SNS (to set the output voltage) and one from the output to the Client RC pin (in tracking configurations). Also, the RC pin in fixed parts operates at the same voltage as the output, whereas the RC pin in adjustable parts operates at the 0.5V reference. To setup a normal tracking configuration, the divider driving the Client RC pin is the same ratio (or nearly the same; if both Host and Client are set to the same output voltage, the Client RC divider should be adjusted 2% to 4% higher) as the divider driving the Client SNS pin. This is shown in [Figure 4-8](#).

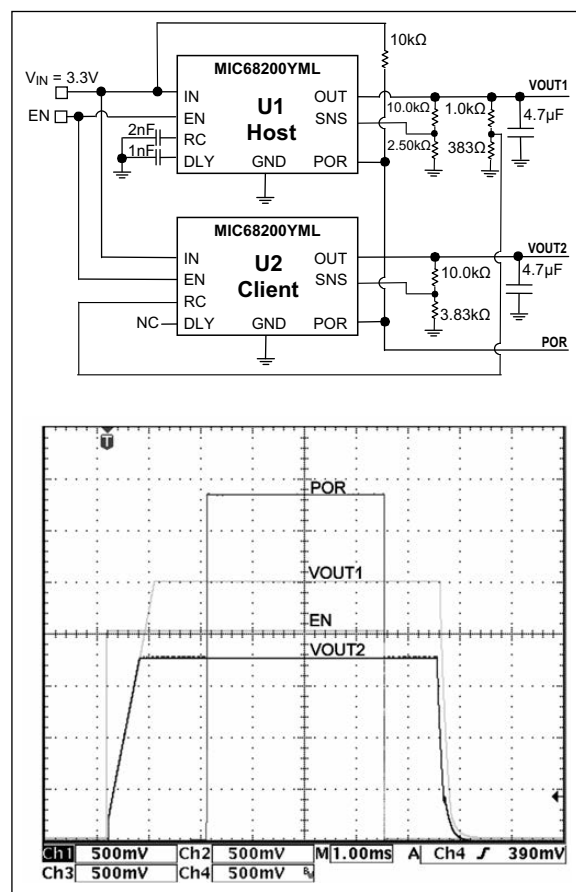


FIGURE 4-8: Adjustable Voltage Devices.

MIC68200

4.8.2 RATIOMETRIC TRACKING

Ratiometric tracking allows independent ramping speeds for both regulators so that the regulation voltage is reached at the same time. This is accomplished by adding a resistor divider between the Host output pin and the Client RC pin. The divider should be scaled such that the Client RC pin reaches or exceeds the target output voltage of the Client as the Host reaches its target voltage.

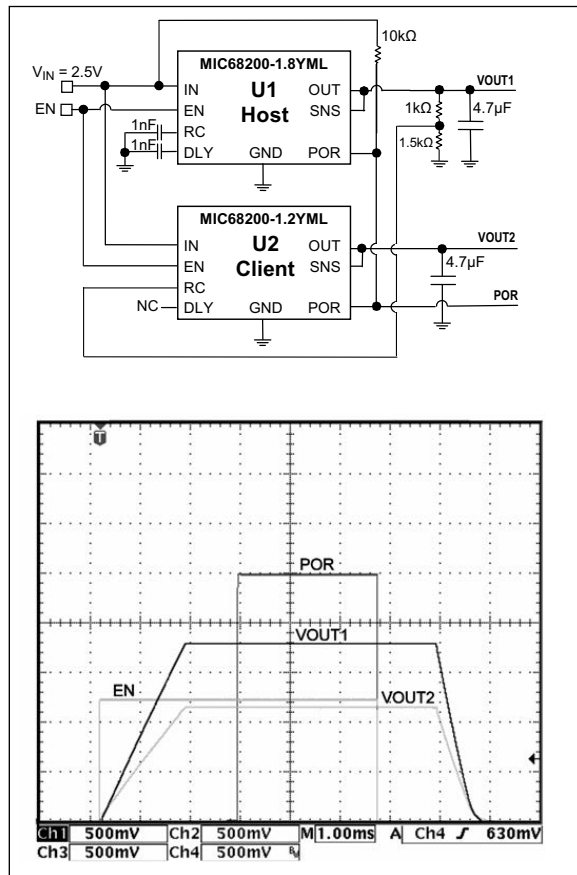


FIGURE 4-9: Fixed Voltage Devices.

Ratiometric tracking may be used with adjustable parts by simply connecting the RC pins of the Host and Client. Use a single RC capacitor of twice the normal value (because twice the current is injected into the single RC cap). Alternatively, adjustable parts may use ratiometric tracking in a manner similar to standard tracking, with the tracking divider changed to the same resistor ratio driving the Master ADJ/SNS pin.

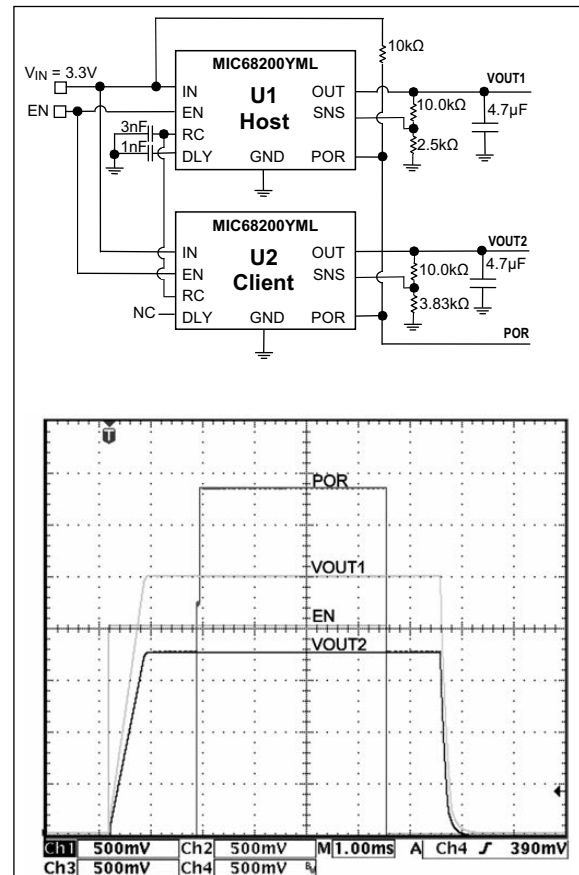


FIGURE 4-10: Adjustable Voltage Devices.

4.8.3 FINAL NOTE ON TRACKING

The MIC68200 does not fully shutdown until the output load is discharged to near zero. If RC is driven from an external source in a tracking configuration and the external source does not go to zero on shutdown, it may prevent complete shutdown of the MIC68200. This will cause no damage, but some Q current will remain and may cause concern in battery operated portable equipment. Also, when RC is driven in tracking mode, pulling EN low will not cause the output to drop. Maintaining low EN in tracking mode simply means that the MIC68200 will shutdown when the tracking voltage gets near zero. In no case can the MIC68200 enter the tracking mode unless EN is pulled high.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

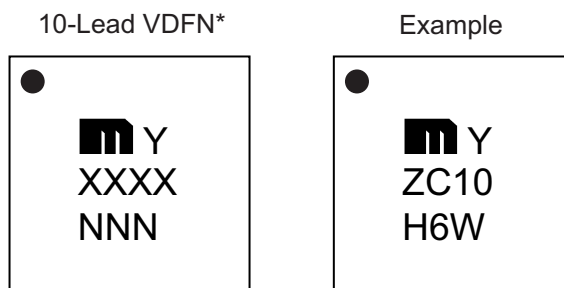


TABLE 5-1: MARKING CODES

Part Number	Marking Code	Voltage
MIC68200-1.0YML	ZC10	1.0V
MIC68200-1.2YML	ZC12	1.2V
MIC68200-1.5YML	ZC15	1.5V
MIC68200-1.8YML	ZC18	1.8V
MIC68200-2.5YML	ZC25	2.5V
MIC68200-3.3YML	ZC33	3.3V
MIC68200YML	ZAAA	Adjustable

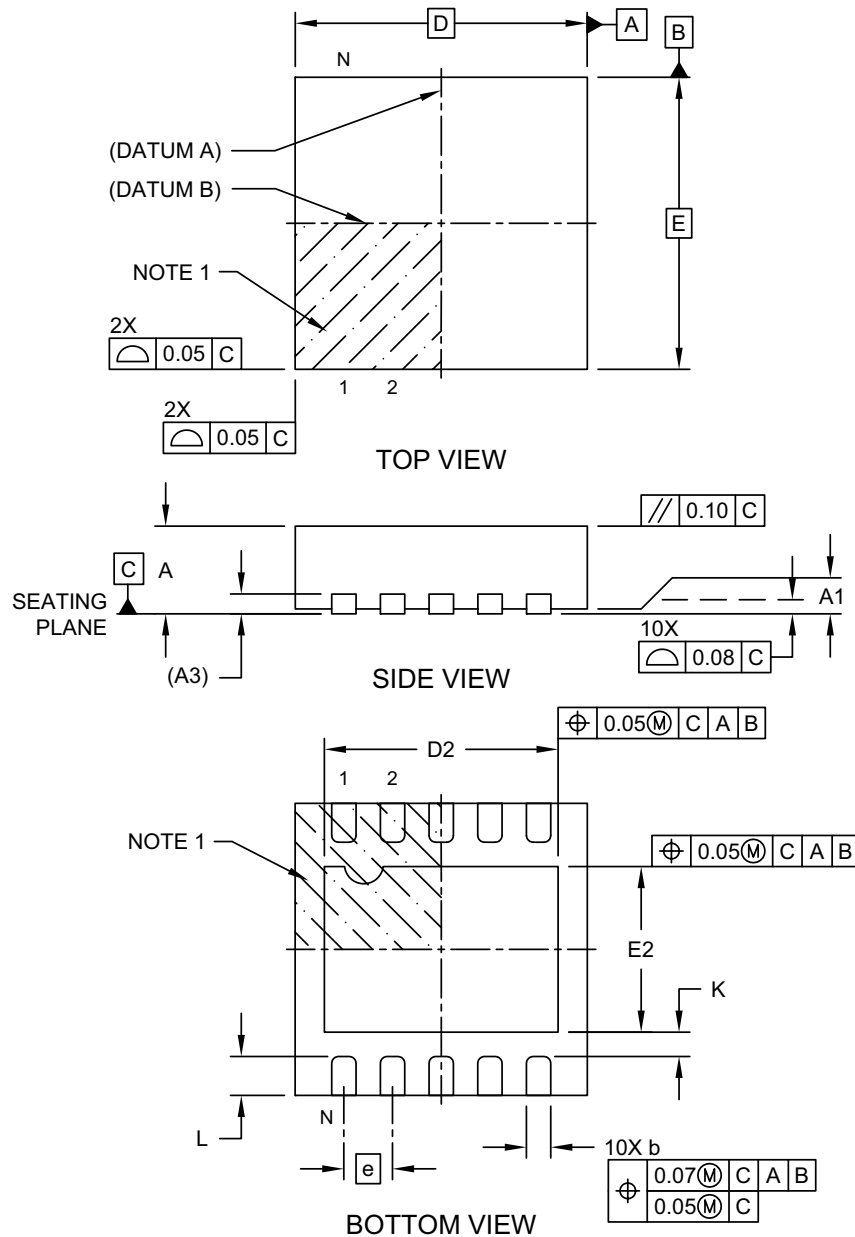
Legend: XX...X Product code or customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code
(e3) Pb-free JEDEC® designator for Matte Tin (Sn)
* This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
Underbar (_) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN] Micrel Legacy Package DFN33-10LD-PL-1

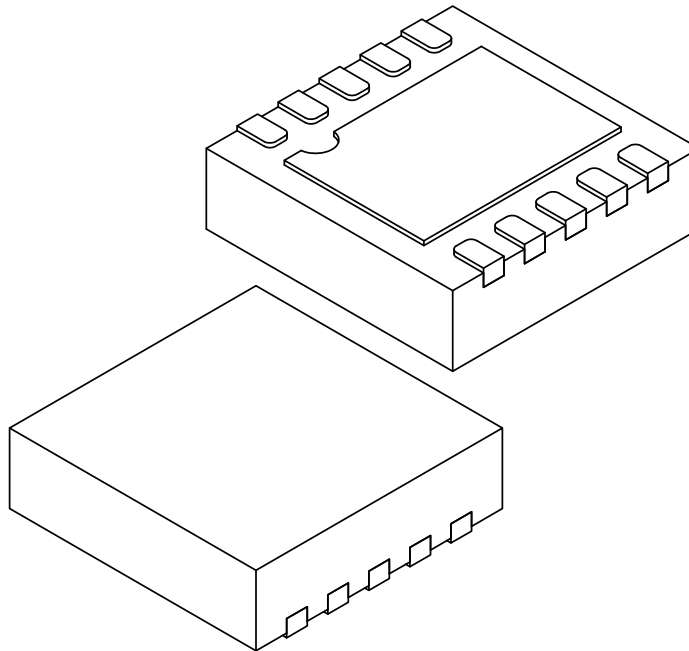
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-1019-JFA Rev A Sheet 1 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN] Micrel Legacy Package DFN33-10LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Terminals	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.35	2.40	2.45
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.65	1.70	1.75
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	—	—

Notes:

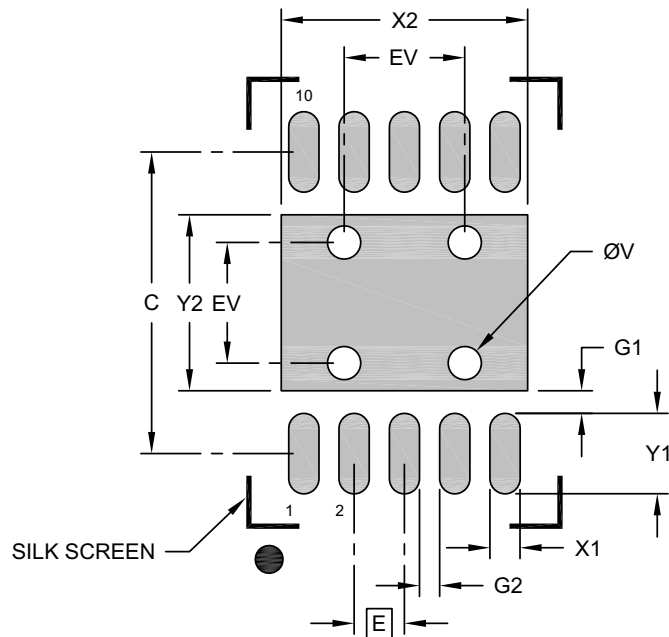
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1019-JFA Rev A Sheet 2 of 2

MIC68200

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN] Micrel Legacy Package DFN33-10LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.45
Optional Center Pad Length	Y2			1.75
Contact Pad Spacing	C		3.00	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.80
Contact Pad to Center Pad (Xnn)	G1	0.23		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3019-JFA Rev A

APPENDIX A: REVISION HISTORY

Revision A (August 2023)

- Converted Micrel document MIC68200 to Microchip data sheet DS20006793A.
- Minor text changes throughout.

MIC68200

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>Part Number</u>	<u>-X.X</u>	<u>X</u>	<u>XX</u>	<u>-XX</u>																					
Device	Output Voltage	Temp. Range	Package	Media Type																					
<div><div>Device: MIC68200: 2A Sequencing LDO with Tracking and Ramp Control</div><div>Output Voltage:<table><tr><td>1.0</td><td>=</td><td>1.0V</td></tr><tr><td>1.2</td><td>=</td><td>1.2V</td></tr><tr><td>1.5</td><td>=</td><td>1.5V</td></tr><tr><td>1.8</td><td>=</td><td>1.8V</td></tr><tr><td>2.5</td><td>=</td><td>2.5V</td></tr><tr><td>3.3</td><td>=</td><td>3.3V</td></tr><tr><td><blank></td><td>=</td><td>Adjustable</td></tr></table></div><div>Temperature Range: Y = -40°C to +125°C</div><div>Package: ML = 10-Lead 3 mm x 3 mm VDFN</div><div>Media Type: TR = 5,000/Reel</div></div>					1.0	=	1.0V	1.2	=	1.2V	1.5	=	1.5V	1.8	=	1.8V	2.5	=	2.5V	3.3	=	3.3V	<blank>	=	Adjustable
1.0	=	1.0V																							
1.2	=	1.2V																							
1.5	=	1.5V																							
1.8	=	1.8V																							
2.5	=	2.5V																							
3.3	=	3.3V																							
<blank>	=	Adjustable																							

Examples:	
a) MIC68200-1.2YML-TR:	MIC68200, 1.2V Output Voltage, -40°C to +125°C Temp. Range, 10-Lead VDFN, 5,000/Reel
b) MIC68200YML-TR:	MIC68200, Adjustable Output Voltage, -40°C to +125°C Temp. Range, 10-Lead VDFN, 5,000/Reel
c) MIC68200-3.3YML-TR:	MIC68200, 3.3V Output Voltage, -40°C to +125°C Temp. Range, 10-Lead VDFN, 5,000/Reel
d) MIC68200-2.5YML-TR:	MIC68200, 2.5V Output Voltage, -40°C to +125°C Temp. Range, 10-Lead VDFN, 5,000/Reel
e) MIC68200-1.8YML-TR:	MIC68200, 1.8V Output Voltage, -40°C to +125°C Temp. Range, 10-Lead VDFN, 5,000/Reel
Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.	

MIC68200

NOTES:

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