MICROCHIP

MIC5305

150 mA µCap Ultra-Low Dropout Regulator

Features

- Ultra-Low Dropout Voltage: 60 mV @ 150 mA
- Input Voltage Range: 2.25 to 5.5V
- Stable with Ceramic Output Capacitors
- 150 mA output Current
- Low Output Noise: 20 μV_{RMS}
- Low Quiescent Current of 90 µA Total
- High PSRR: Up to 85 dB @1 kHz
- Less than 30 µs Turn-On Time w/ C_{BYP} = 0.01 µF
- High Output Accuracy:
  - ±1.0% Initial Accuracy
  - ±2.0% over Temperature
- Thermal Shutdown Protection
- Current Limit Protection
- Tiny 6-Lead 2 mm x 2 mm VDFN Package
- Ultra-Thin 6-Lead 2 mm x 2 mm UDFN Package
- Thin SOT 5-Lead Package

Applications

- Cellular Phones
- PDAs
- Fiber Optic Modules
- Portable Electronics
- Notebook PCs
- Audio Codec Power Supplies

General Description

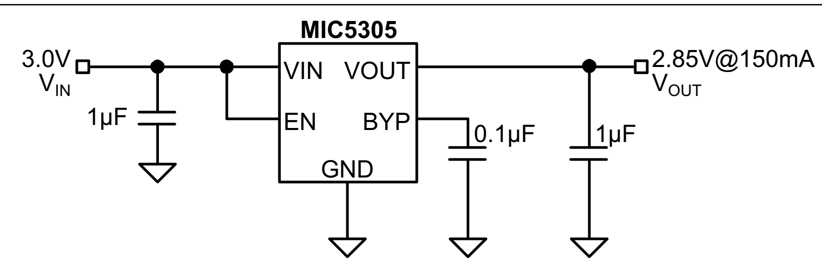
The MIC5305 is a high-performance, 150 mA LDO regulator that offers extremely high PSRR and very low noise while consuming low ground current.

Ideal for battery-operated applications, the MIC5305 features 1% accuracy, extremely low dropout voltage (60 mV @ 150 mA), and low ground current at light load (typically 90 µA). Equipped with a logic-compatible enable pin, the MIC5305 can be put into a zero off-mode current state that draws no current when disabled.

The MIC5305 is a µCap design that operates with very small ceramic output capacitors for stability, thereby reducing required board space and component cost.

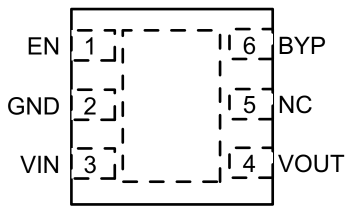
The MIC5305 is available in fixed output voltages and adjustable output voltages in the compact 6-lead 2 mm x 2 mm VDFN leadless package, the ultra-thin 6-lead 2 mm x 2 mm UDFN, and 5-lead Thin SOT package.

Typical Application Circuit

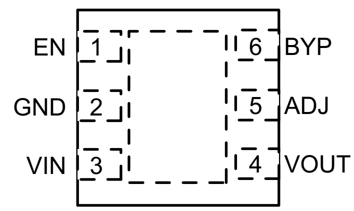


Package Types

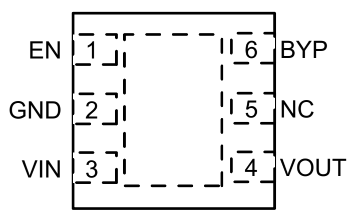
MIC5305-x.xYML (Fixed)
6-Lead 2 mm x 2 mm VDFN (ML)
(Top View)



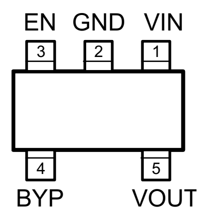
MIC5305YML (Adjustable)
6-Lead 2 mm x 2 mm VDFN (ML)
(Top View)



MIC5305-x.xYMT (Fixed)
6-Lead 2 mm x 2 mm UDFN (MT)
(Top View)

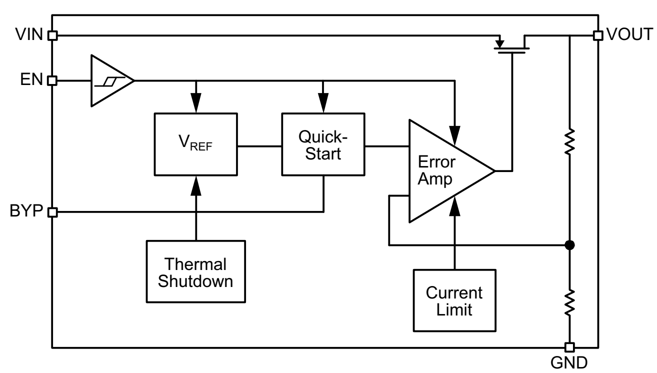


MIC5305-x.xYD5 (Fixed)
5-Lead TSOT (D5)
(Top View)

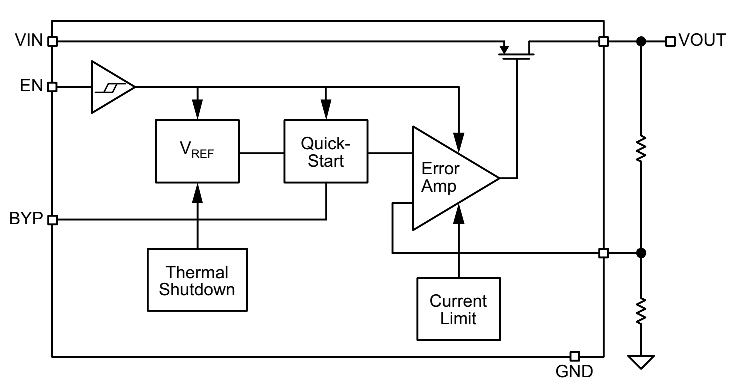


Functional Block Diagrams

Fixed Voltage Version



Adjustable Voltage Version



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) ..... 0V to +6V
Enable Input Voltage (V_{EN}) ..... 0V to +6V
Power Dissipation (P_D, Note 1) ..... Internally Limited
ESD Rating (Note 2) ..... 2 kV

Operating Ratings ‡

Supply Voltage ..... +2.25V to +5.5V
Enable Input Voltage (V_{EN}) ..... 0V to V_{IN}

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(MAX)} = (T_{J(MAX)} – T_A)/θ_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$; C_{OUT} = 1.0 µF; I_{OUT} = 100 µA; T_A = +25°C. **Bold** values valid for –40ºC to +125°C; unless otherwise specified. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy		–1.0	—	1.0	%	Variation from nominal V_{OUT}
		–2.0	—	**2.0**		Variation from nominal V_{OUT}, I_{OUT} = 100 mA to 150 mA
Output Voltage Temperature Coefficient		—	40	—	ppm/°C	—
Line Regulation	$ΔV_{OUT}/(V_{OUT} \times ΔV_{IN})$	—	0.02	**0.3**	%/V	$V_{IN} = V_{OUT}$ + 1V to 5.5V
Load Regulation (Note 2)	$ΔV_{OUT}/V_{OUT}$	—	0.1	**0.5**	%	I_{OUT} = 100 µA to 150 mA
Dropout Voltage (Note 3)	V_{DO}	—	20	**35**	mV	I_{OUT} = 50 mA, V_{OUT} > 2.8V
		—	60	**85**		I_{OUT} = 150 mA, V_{OUT} > 2.8V
		—	27	**45**		I_{OUT} = 50 mA, V_{OUT} ≤ 2.8V
		—	85	**110**		I_{OUT} = 150 mA, V_{OUT} ≤ 2.8V
Ground Pin Current (Note 4)	I_{GND}	—	90	**150**	µA	I_{OUT} = 0 mA to 150 mA
Ground Pin Current in Shutdown	I_{SD}	—	0.5	—	µA	V_{EN} ≤ 0.2V
Ripple Rejection	PSRR	—	85	—	dB	f = up to 1 kHz; C_{OUT} = 1.0 µF ceramic; C_{BYP} = 0.1 µF
		—	65	—		f = 10 kHz; C_{OUT} = 1.0 µF ceramic; C_{BYP} = 0.1 µF
Current Limit	I_{LIM}	**300**	600	**900**	mA	V_{OUT} = 0V

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$; C_{OUT} = 1.0 µF; I_{OUT} = 100 µA; T_A = +25°C. **Bold** values valid for –40ºC to +125°C; unless otherwise specified. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Noise	e_n	—	20	—	μV_{RMS}	C_{OUT} = 1 µF, C_{BYP} = 0.1 µF, 10 Hz to 100 kHz
Turn-On Time	t_{ON}	—	30	**100**	µs	C_{OUT} = 1 µF; C_{BYP} = 0.1 µF; I_{OUT} = 150 mA
Enable Input						
Enable Input Voltage	V_{IL}	—	—	**0.2**	V	Logic Low (Regulator Shutdown)
	V_{IH}	**1.0**	—	—		Logic High (Regulator Enabled)
Enable Input Current	I_{IL}	—	0.01	**1**	µA	$V_{IL} \le 0.2V$ (Regulator Shutdown)
	I_{IH}	—	0.01	**1**		$V_{IH} \ge 1.2V$ (Regulator Enabled)

Note 1: Specification for packaged product only.

2: Regulation is measured at constant junction temperature using low duty cycle pulse testing; changes in output voltage due to heating effects are covered by the thermal regulation specification.

3: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal V_{OUT}. For outputs below 2.25V, the dropout voltage is the input-to-output differential with the minimum input voltage 2.25V.

4: Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 5 sec.
Package Thermal Resistances						
Thermal Resistance, UDFN 6-Ld	θ_{JA}	—	93	—	°C/W	—
Thermal Resistance, VDFN 6-Ld	θ_{JA}	—	93	—	°C/W	—
Thermal Resistance, TSOT 5-Ld	θ_{JA}	—	235	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

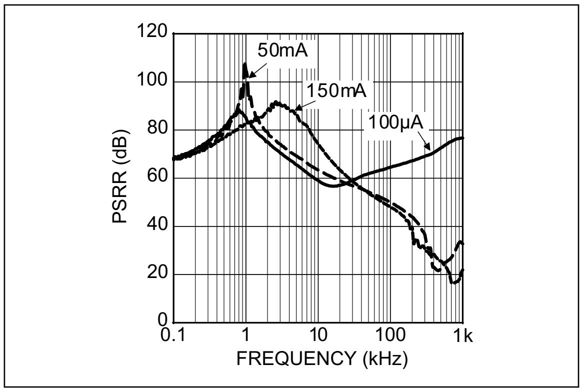


FIGURE 2-1: *PSRR (Bypass Pin Cap = 0.01 µF).*

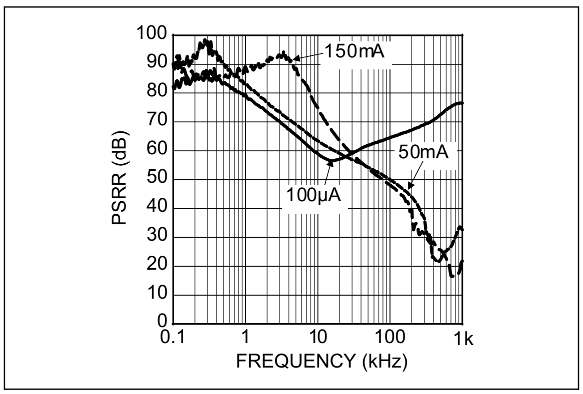


FIGURE 2-2: *PSRR (Bypass Pin Cap = 0.1 µF).*

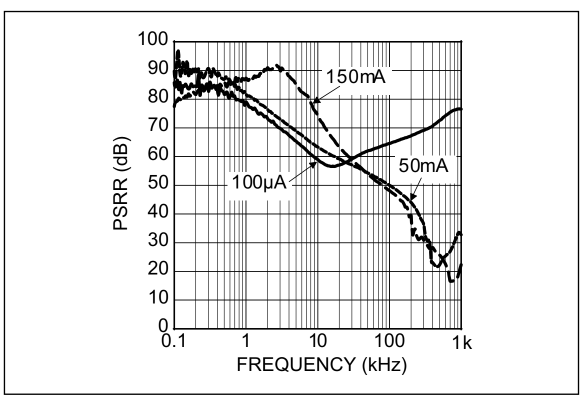


FIGURE 2-3: *PSRR (Bypass Pin Cap = 1 µF).*

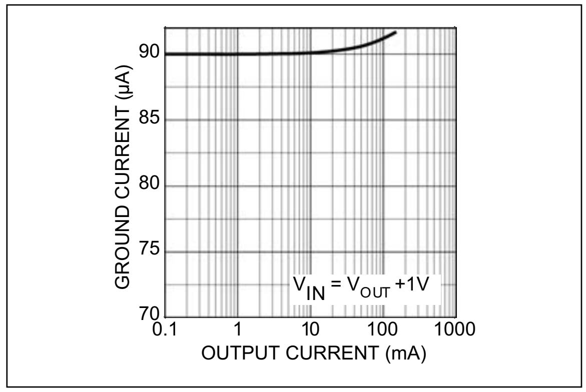


FIGURE 2-4: *Ground Pin Current.*

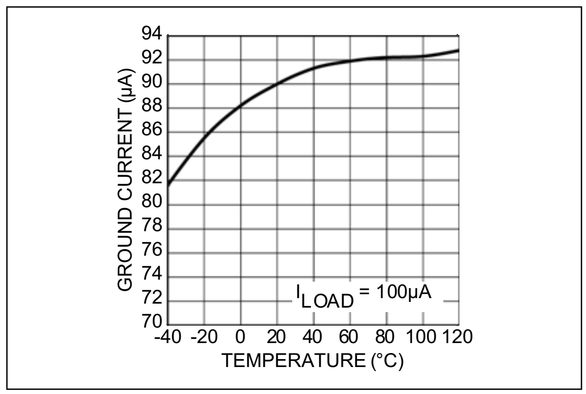


FIGURE 2-5: *Ground Pin Current.*

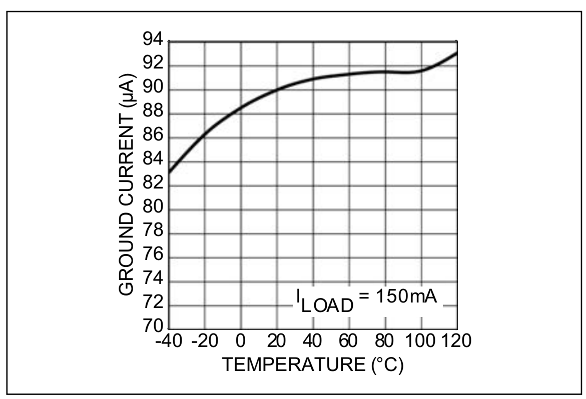


FIGURE 2-6: *Ground Pin Current.*

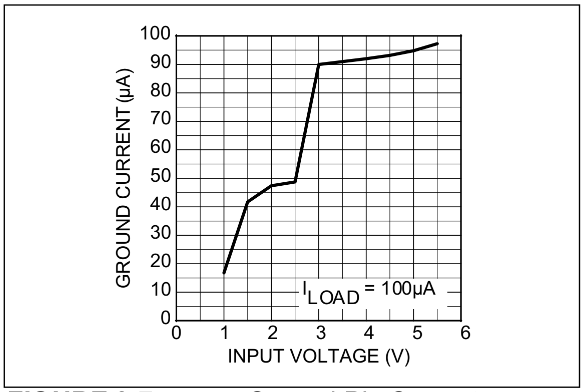


FIGURE 2-7: *Ground Pin Current.*

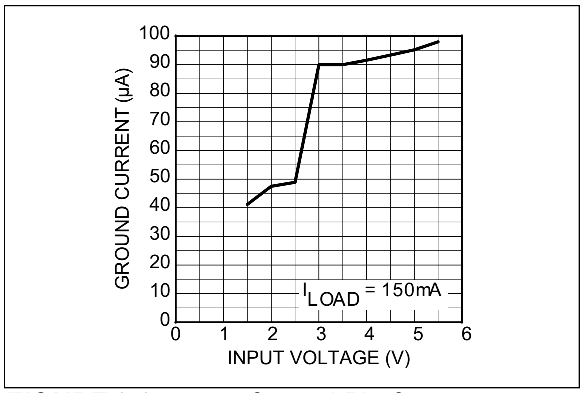


FIGURE 2-8: *Ground Pin Current.*

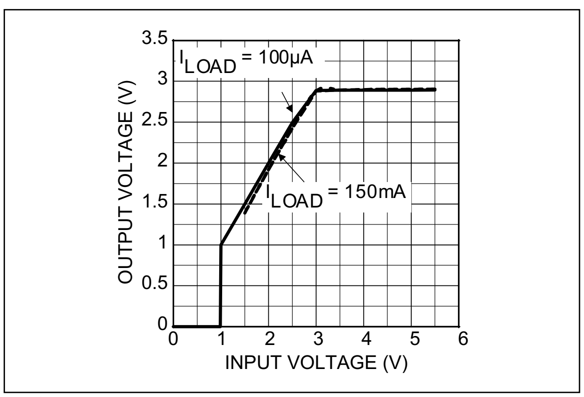


FIGURE 2-9: *Dropout Characteristics.*

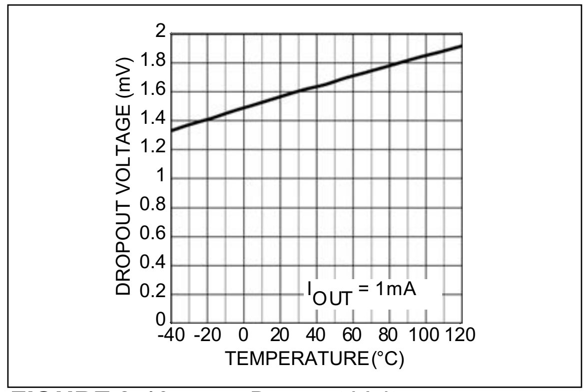


FIGURE 2-10: *Dropout Voltage.*

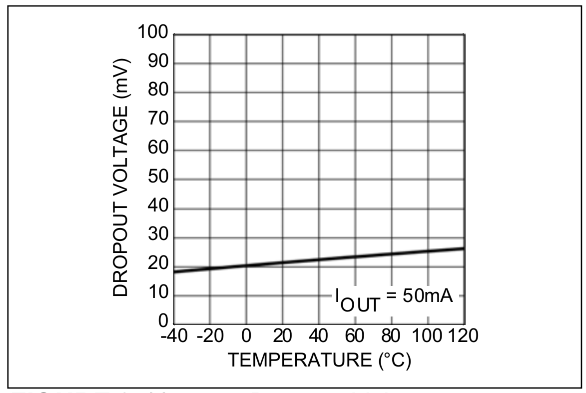


FIGURE 2-11: *Dropout Voltage.*

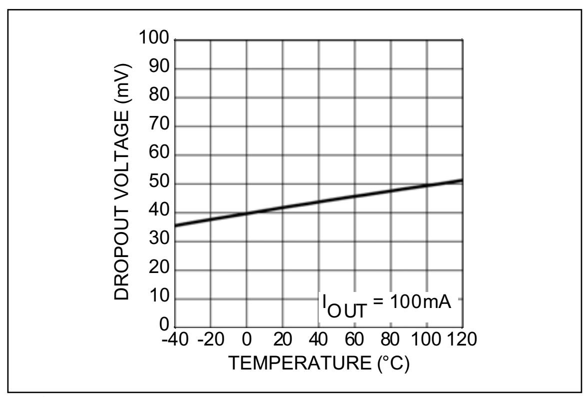


FIGURE 2-12: *Dropout Voltage.*

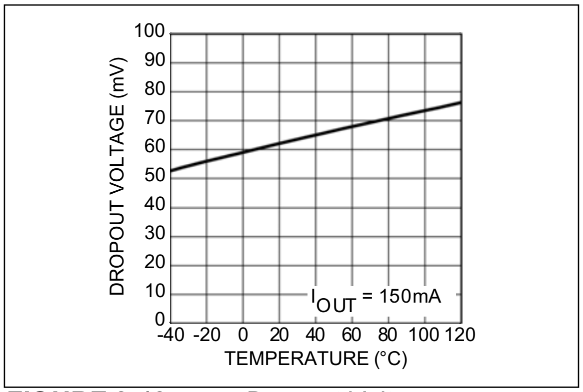


FIGURE 2-13: *Dropout Voltage.*

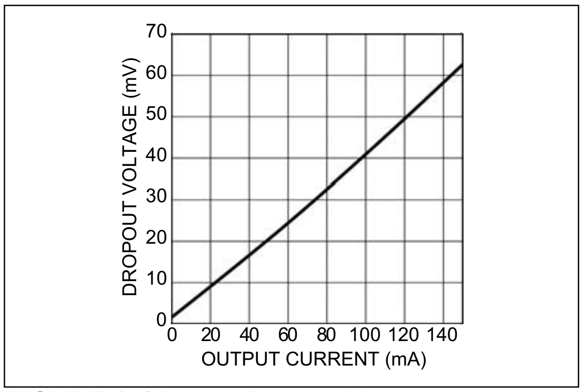


FIGURE 2-14: *Dropout Voltage.*

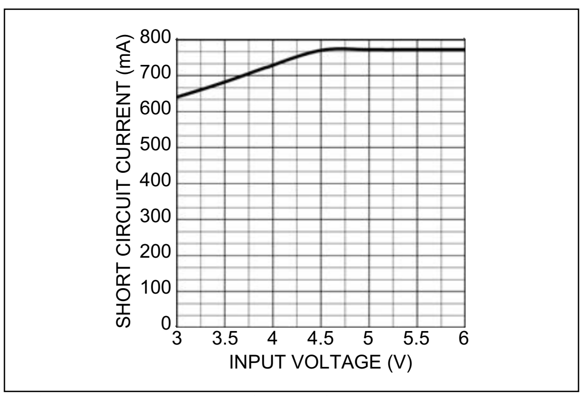


FIGURE 2-15: *Short Circuit Current.*

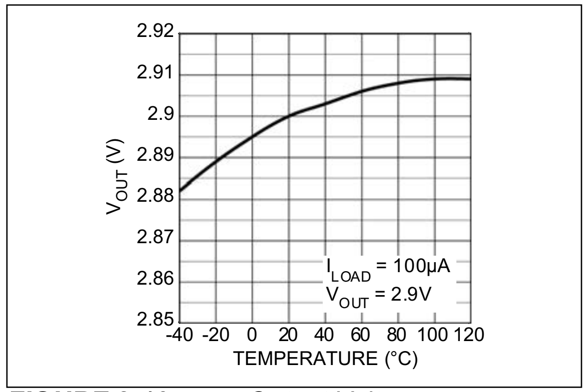


FIGURE 2-16: *Output Voltage vs. Temperature.*

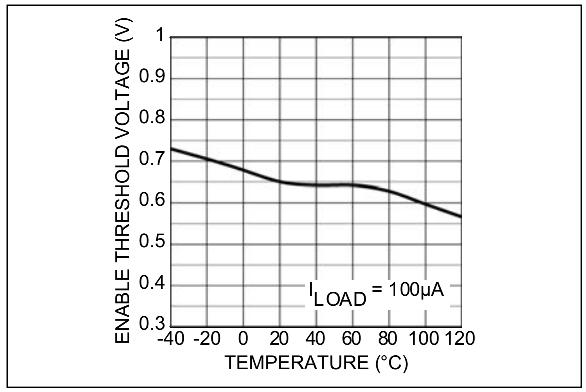


FIGURE 2-17: *Enable Threshold vs. Temperature.*

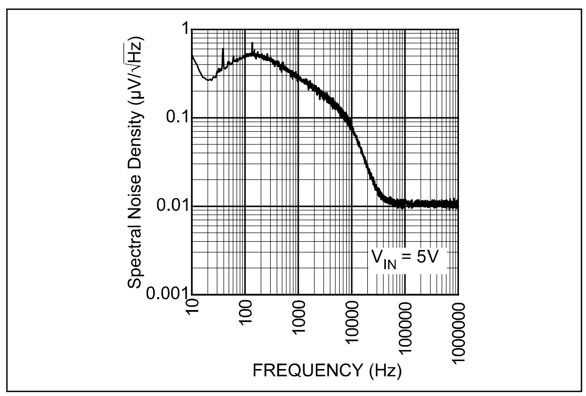


FIGURE 2-18: *Output Noise Spectral Density.*

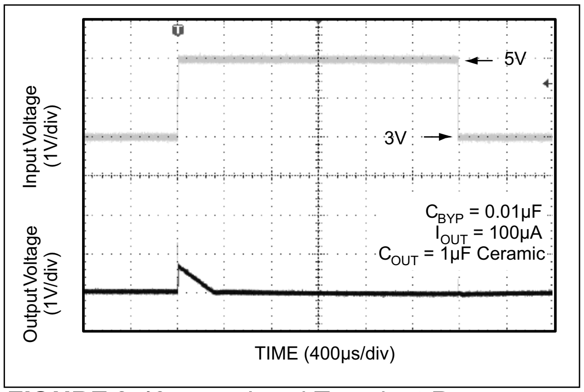


FIGURE 2-19: *Load Transient Response.*

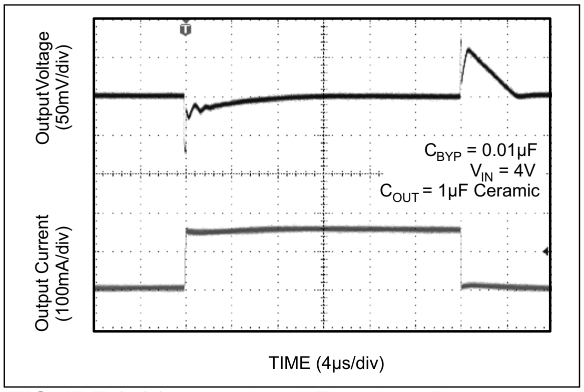


FIGURE 2-20: *Load Transient Response.*

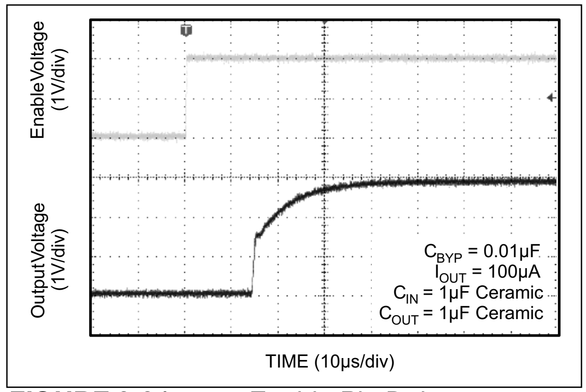


FIGURE 2-21: *Enable Pin Delay.*

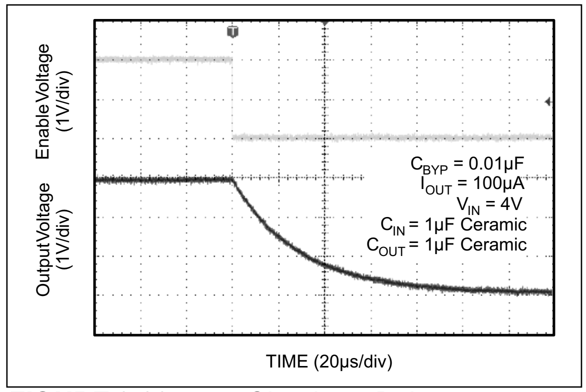


FIGURE 2-22: *Shutdown Delay.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number VDFN-6 Fixed	Pin Number VDFN-6 Adjustable	Pin Number UDFN-6 Fixed	Pin Number TSOT-5 Fixed	Pin Name	Description
1	1	1	3	EN	Enable Input. Active High. High = on, Low = off. Do not leave floating.
2	2	2	2	GND	Ground.
3	3	3	1	VIN	Supply Input.
4	4	4	5	VOUT	Output Voltage.
—	5	—	—	ADJ	Adjust Input: Connect to external resistor voltage divider network.
5	—	5	—	NC	No connection for fixed-voltage parts.
6	6	6	4	BYP	Reference Bypass: Connect external 0.1 µF to GND for reduced output noise. May be left open.
Heatsink Pad	Heatsink Pad	Heatsink Pad	—	EPAD	Exposed Heatsink Pad connected to ground internally.

4.0 APPLICATION INFORMATION

4.1 Enable/Shutdown

The MIC5305 comes with an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a “zero” off-mode current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. The active-high enable pin uses CMOS technology and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

4.2 Input Capacitor

The MIC5305 is a high-performance, high bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1 µF capacitor is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high frequency capacitors, such as small-valued NPO dielectric-type capacitors, help filter out high-frequency noise and are good practice in any RF-based circuit.

4.3 Output Capacitor

The MIC5305 requires an output capacitor of 1 µF or greater to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1 µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

4.4 Bypass Capacitor

A capacitor can be placed from the noise bypass pin to ground to reduce output voltage noise. The capacitor bypasses the internal reference. A 0.1 µF capacitor is recommended for applications that require low-noise outputs. The bypass capacitor can be increased, further reducing noise and improving PSRR. Turn-on time increases slightly with respect to bypass capacitance. A unique, quick-start circuit allows the MIC5305 to drive a large capacitor on the bypass pin without significantly slowing turn-on time. Refer to the Typical Performance Curves section for performance with different bypass capacitors.

4.5 No-Load Stability

Unlike many other voltage regulators, the MIC5305 will remain stable and in regulation with no load. This is especially important in CMOS RAM keep-alive applications.

4.6 Adjustable Regulator Application

Adjustable regulators use the ratio of two resistors to multiply the reference voltage to produce the desired output voltage. The MIC5305 can be adjusted from 1.25V to 5.5V by using two external resistors (Figure 4-1). The resistors set the output voltage based on the following equation:

EQUATION 4-1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{REF} = 1.25V

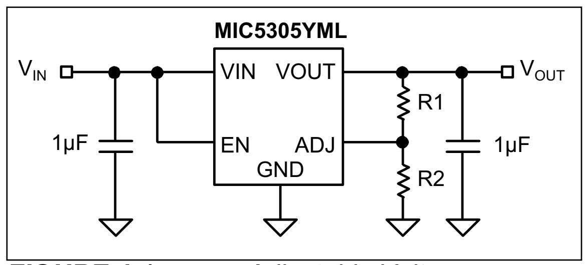


FIGURE 4-1: *Adjustable Voltage Application.*

4.7 Thermal Considerations

The MIC5305 is designed to provide 150 mA of continuous current in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. Given that the input voltage is 5.0V, the output voltage is 2.9V and the output current equals 150 mA.

The actual power dissipation of the regulator circuit can be determined using the following equation:

EQUATION 4-2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

Because this device is CMOS and the ground current is typically <100 µA over the load range, the power dissipation contributed by the ground current is <1% and can be ignored for this calculation.

EQUATION 4-3:

$$P_D = (5.0V - 2.9V) \times 150mA = 0.32W$$

To determine the maximum ambient operating temperature of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

EQUATION 4-4:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where:

$T_{J(MAX)}$ = 125°C, the max. junction temperature of the die.

θ_{JA} = 93°C/W, thermal resistance.

Table 4-1 shows junction-to-ambient thermal resistance for the MIC5305 in the 6-lead 2 mm x 2 mm VDFN package.

TABLE 4-1: THERMAL RESISTANCE

Package	θ_{JA} Rec. Min. Footprint	θ_{JC}
VDFN 6-Ld	93°C/W	2°C/W

Substituting P_D for $P_{D(MAX)}$ and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit. The junction-to-ambient thermal resistance for the minimum footprint (the minimum amount of copper that you can solder the part to) is 93°C/W, from Table 4-1. The maximum power dissipation must not be exceeded for proper operation.

For example, when operating the MIC5305-2.9YML at an input voltage of 5.0V and 150 mA load with a minimum footprint layout, the maximum ambient operating temperature T_A can be determined as follows:

EQUATION 4-5:

$$0.32W = \frac{125°C - T_A}{93°C/W}$$

$$T_A = 95.2°C$$

Therefore, a 2.9V application at 150 mA of output current can accept an ambient operating temperature of 95.2°C in a 6-lead 2 mm x 2 mm VDFN package. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the “Regulator Thermals” section of Microchip’s Designing with Low-Dropout Voltage Regulators handbook.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

6-Lead UDFN*	Example	6-Lead VDFN*	Example
▲ XXX NNN	▲ 828 21R	● XXX NNN	● 820 0PI

5-Lead TSOT* (Front)	Example	5-Lead TSOT* (Back)	Example
XXXX	N815	NNN	BK1

Note: A full list of marking codes for all available part numbers appears in the Product Identification System section.

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

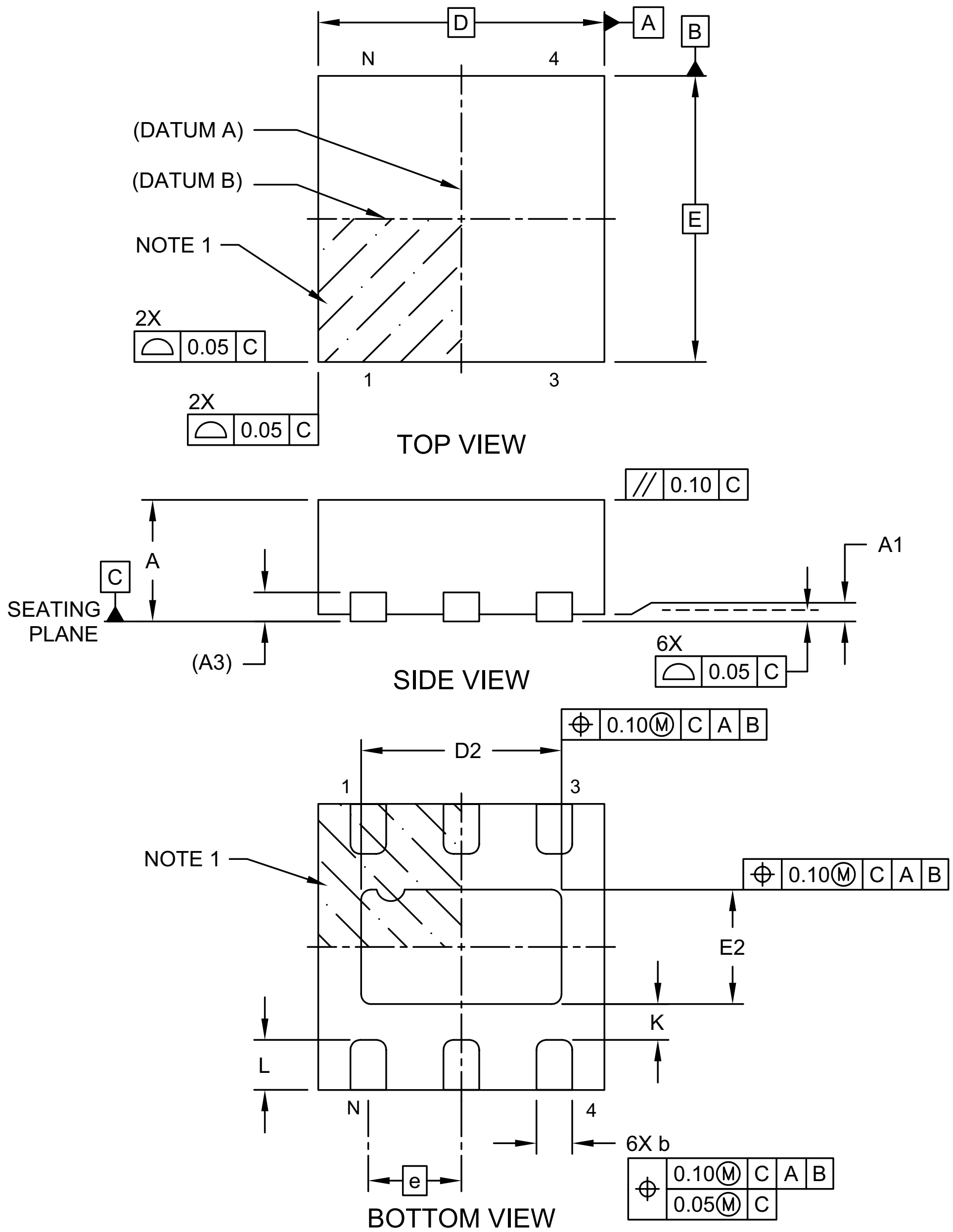
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

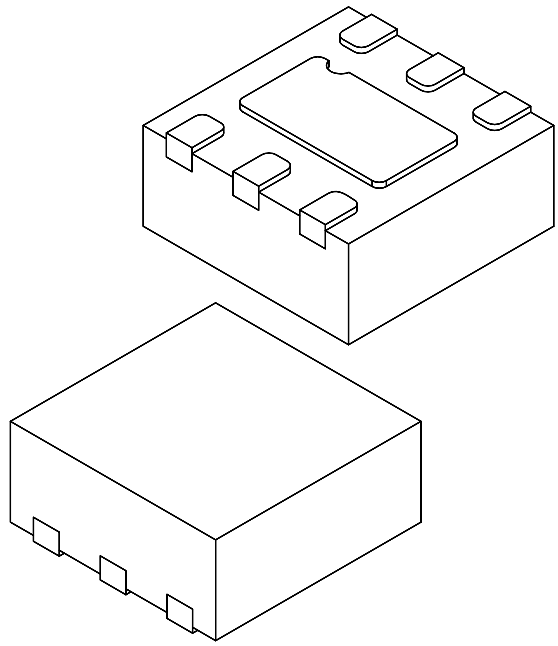
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1016A Sheet 1 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.75	0.80	0.85
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

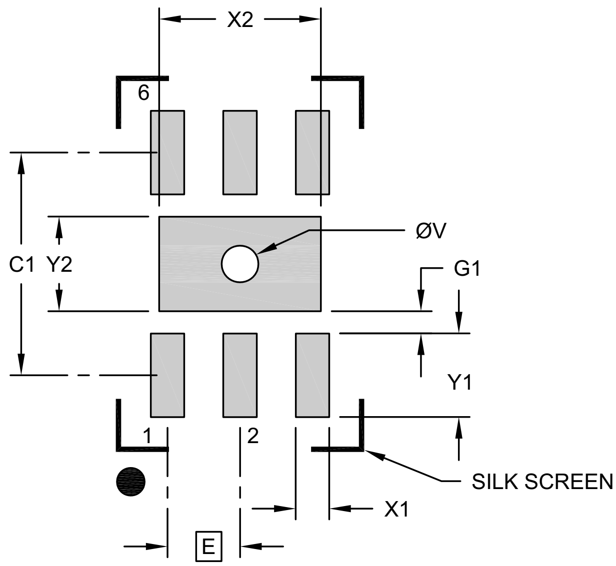
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1016A Sheet 2 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (JDA) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			0.85
Optional Center Pad Length	Y2			1.45
Contact Pad Spacing	C1		2.00	
Contact Pad Width (X6)	X1			0.30
Contact Pad Length (X6)	Y1			0.75
Contact Pad to Center Pad (X6)	G1	0.20		
Thermal Via Diameter	V	0.27	0.30	0.33

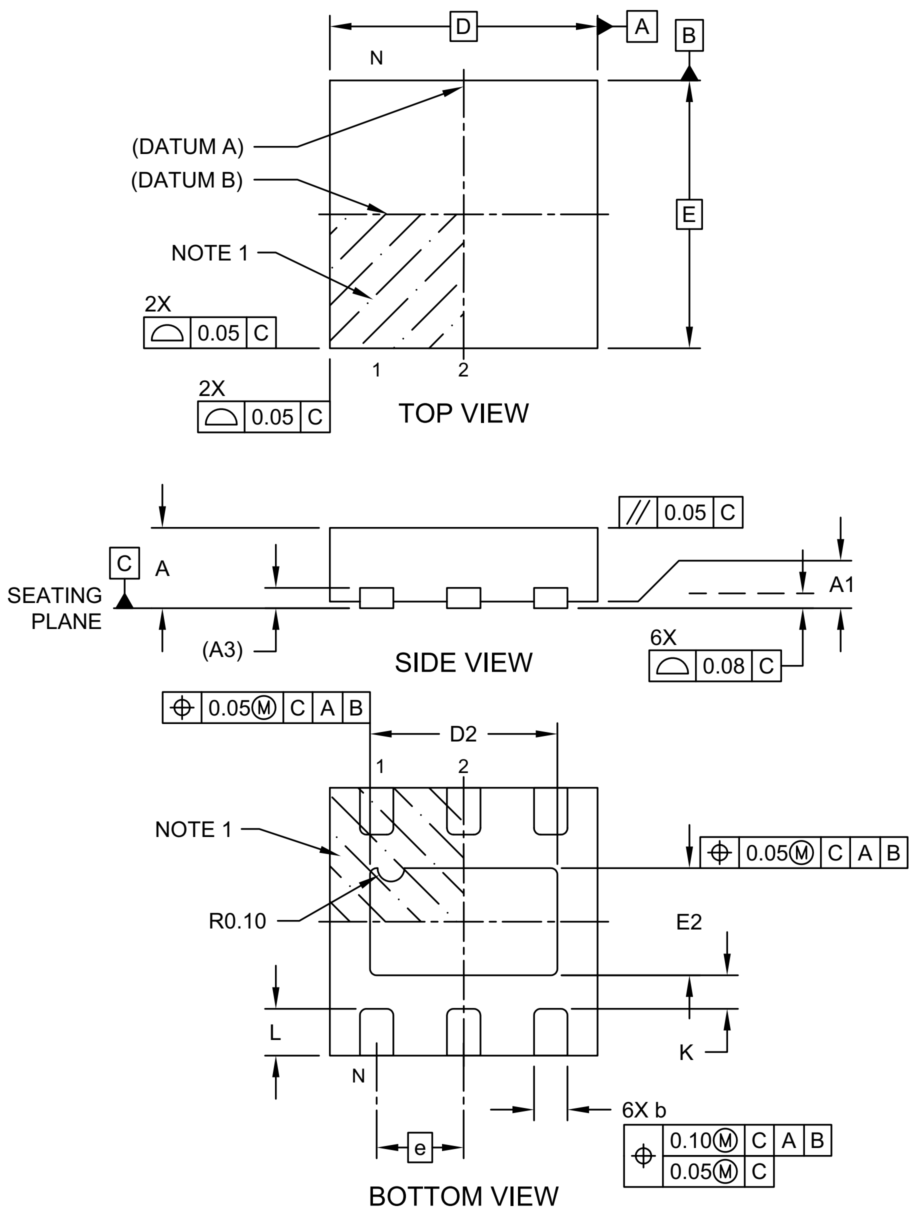
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-21016A

6-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HSA) - 2x2x0.6 mm Body [UDFN]
Micrel Legacy Package TDFN22-6LD-PL-1

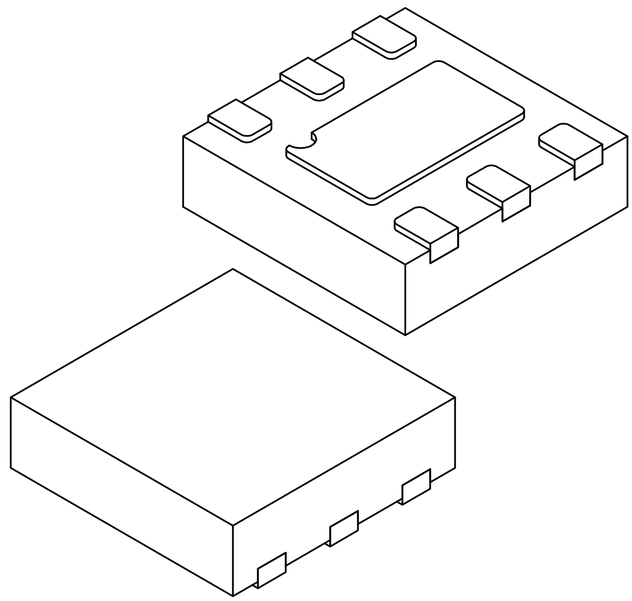
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1156-HSA Rev A Sheet 1 of 2

6-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HSA) - 2x2x0.6 mm Body [UDFN] Micrel Legacy Package TDFN22-6LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.75	0.80	0.85
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	-	-

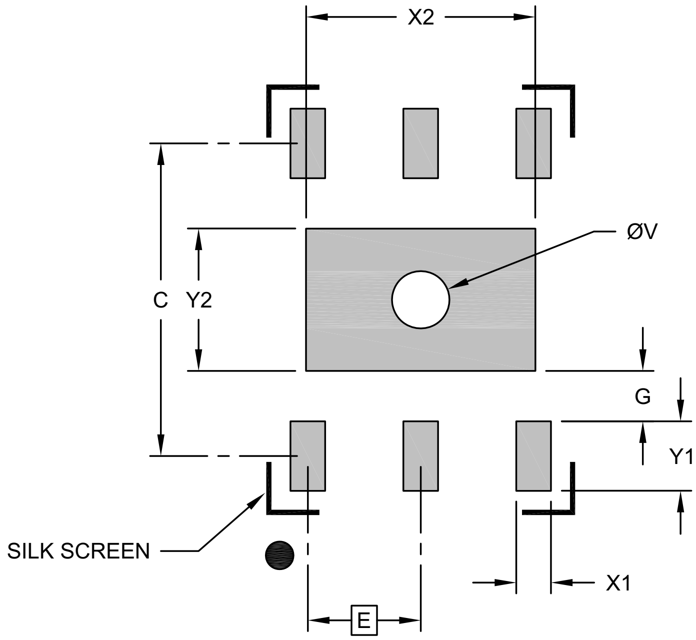
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1156-HSA Rev A Sheet 2 of 2

6-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HSA) - 2x2x0.6 mm Body [UDFN] Micrel Legacy Package TDFN22-6LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Center Pad Width	X2			1.32
Center Pad Length	Y2			0.82
Contact Pad Spacing	C		1.80	
Contact Pad Width (X6)	X1			0.20
Contact Pad Length (X6)	Y1			0.40
Contact Pad to Center Pad (X6)	G	0.29		
Thermal Via Diameter	V		0.33	

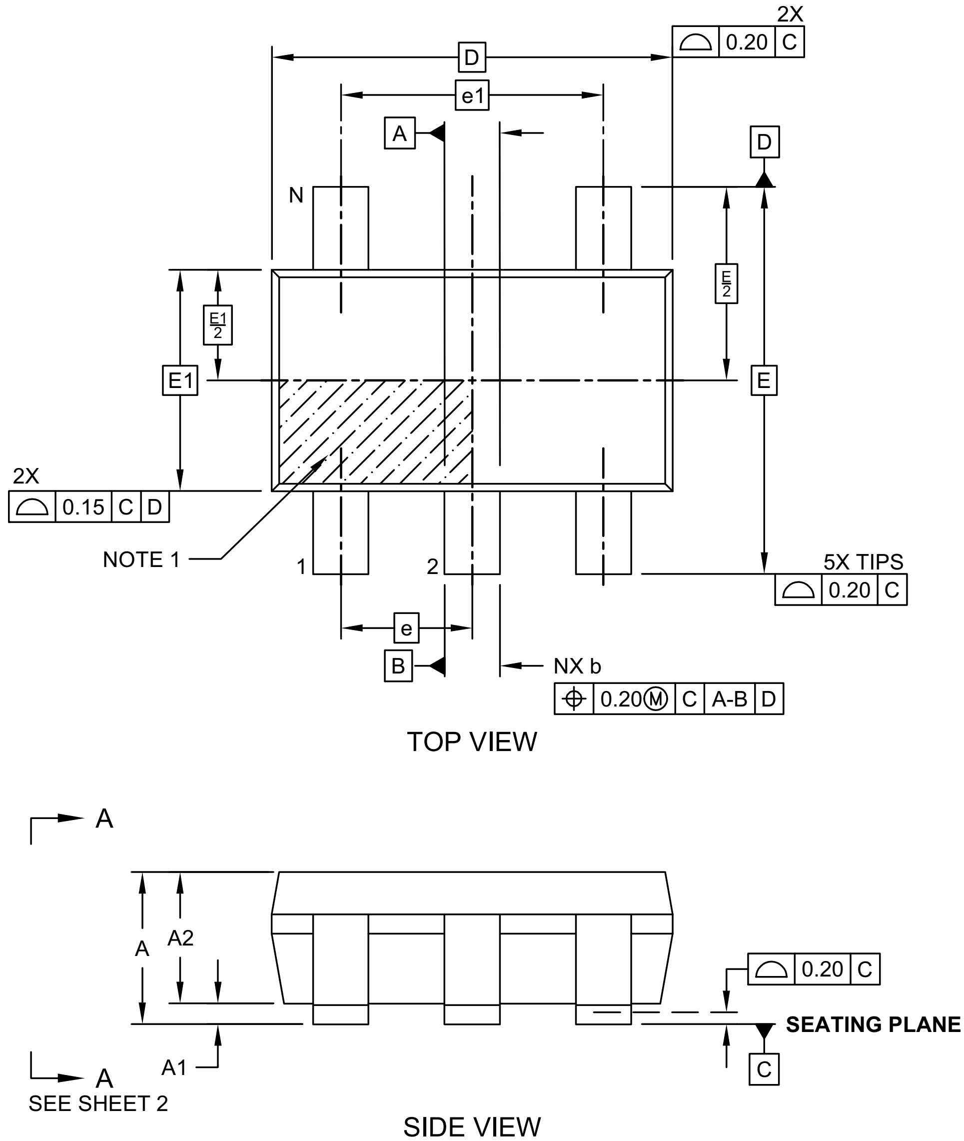
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3156-HSA Rev A

5-Lead Plastic Thin Small Outline Transistor (D5A) [TSOT]
Micrel Legacy Package TSOT-5LD-PL-1

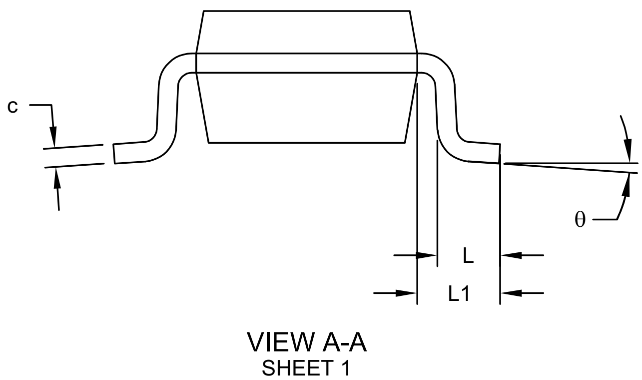
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

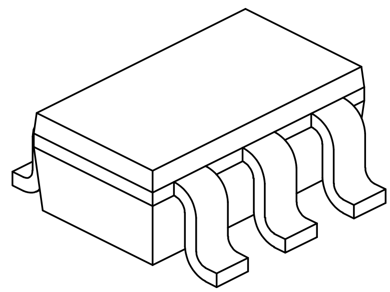


Microchip Technology Drawing C04-1179 Rev A Sheet 1 of 2

5-Lead Plastic Thin Small Outline Transistor (D5A) [TSOT]
Micrel Legacy Package TSOT-5LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	-	-	1.00
Molded Package Thickness	A2	0.84	0.87	0.90
Standoff	A1	0.00	-	0.10
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	0.40	0.50
Footprint	L1	0.60 REF		
Foot Angle	ϕ	0°	-	4°
Lead Thickness	c	0.127 REF		
Lead Width	b	0.30	-	0.50

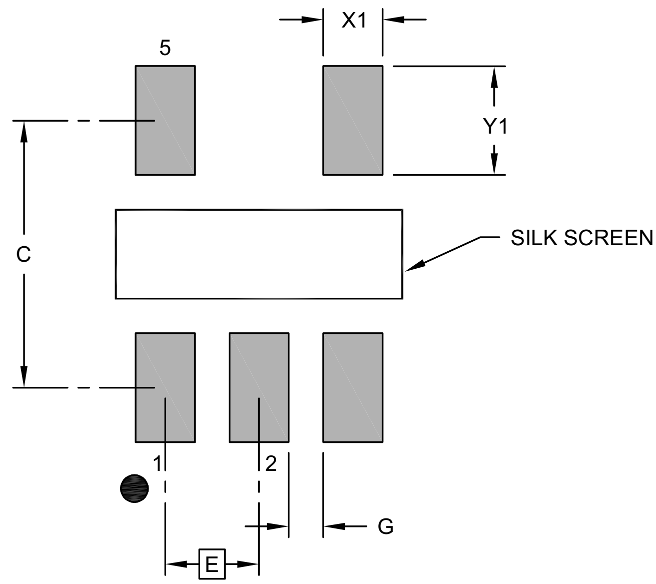
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1179 Rev A Sheet 1 of 2

5-Lead Plastic Thin Small Outline Transistor (D5A) [TSOT]
Micrel Legacy Package TSOT-5LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.60	
Contact Pad Width (X5)	X1			0.60
Contact Pad Length (X5)	Y1			1.10
Contact Pad to Center Pad (X2)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3179 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2024)

- Converted Micrel document MIC5305 to Microchip data sheet DS20006746A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number	-X.X	X	XX	-XX
Device	Output Voltage	Temp. Range	Package	Media Type

Device:	MIC5305:		150 mA µCap Ultra-Low Dropout Regulator
Output Voltage:	<blank>	=	Adjustable (VDFN only)
	1.5	=	1.5V (TSOT and VDFN only)
	1.8	=	1.8V (TSOT and VDFN only)
	2.5	=	2.5V (TSOT and VDFN only)
	2.6	=	2.6V (TSOT and VDFN only)
	2.7	=	2.7V (TSOT and VDFN only)
	2.8	=	2.8V (All package options)
	2.85	=	2.85V (TSOT and VDFN only)
	2.9	=	2.9V (TSOT and VDFN only)
	3.0	=	3.0V (TSOT and VDFN only)
	3.3	=	3.3V (TSOT and VDFN only)
	4.6	=	4.6V (VDFN or UDFN only)
	4.75	=	4.75V (TSOT and VDFN only)
Temperature Range:	Y	=	–40°C to +125°C
Package:	MT	=	6-Lead 2 mm x 2 mm UDFN
	ML	=	6-Lead 2 mm x 2 mm VDFN
	D5	=	5-Lead Thin SOT
Media Type:	TR	=	3,000/Reel (TSOT only)
	TR	=	5,000/Reel (UDFN and VDFN only)
	TX	=	3,000/Reel, Rev. Tape & Reel (TSOT only)

Examples:

a) MIC5305YML-TR: MIC5305, Adj. Output Voltage, –40°C to +125°C Temp. Range, 6-Lead VDFN, 5,000/Reel

b) MIC5305-2.5YD5-TX: MIC5305, 2.5V Output Voltage, –40°C to +125°C Temp. Range, 5-Lead TSOT, 3,000/Reel Reverse

c) MIC5305-2.8YMT-TR: MIC5305, 2.8V Output Voltage, –40°C to +125°C Temp. Range, 6-Lead UDFN, 5,000/Reel

d) MIC5305-3.0YD5-TR: MIC5305, 3.0V Output Voltage, –40°C to +125°C Temp. Range, 5-Lead TSOT, 3,000/Reel

e) MIC5305-2.9YML-TR: MIC5305, 2.9V Output Voltage, –40°C to +125°C Temp. Range, 6-Lead VDFN, 5,000/Reel

f) MIC5305-1.5YD5-TX: MIC5305, 1.5V Output Voltage, –40°C to +125°C Temp. Range, 5-Lead TSOT, 3,000/Reel Reverse

g) MIC5305-4.6YMT-TR: MIC5305, 4.6V Output Voltage, –40°C to +125°C Temp. Range, 6-Lead UDFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

MARKING CODES

Part Number	Marking Code	Output Voltage	Package
MIC5305-1.5YML	815	1.5V	6-Lead 2 mm x 2 mm VDFN
MIC5305-1.8YML	818	1.8V	6-Lead 2 mm x 2 mm VDFN
MIC5305-2.5YML	825	2.5V	6-Lead 2 mm x 2 mm VDFN
MIC5305-2.6YML	826	2.6V	6-Lead 2 mm x 2 mm VDFN
MIC5305-2.7YML	827	2.7V	6-Lead 2 mm x 2 mm VDFN
MIC5305-2.8YML	828	2.8V	6-Lead 2 mm x 2 mm VDFN
MIC5305-2.85YML	82J	2.85V	6-Lead 2 mm x 2 mm VDFN
MIC5305-2.9YML	829	2.9V	6-Lead 2 mm x 2 mm VDFN
MIC5305-3.0YML	830	3.0V	6-Lead 2 mm x 2 mm VDFN
MIC5305-3.3YML	833	3.3V	6-Lead 2 mm x 2 mm VDFN
MIC5305-4.6YML	846	4.6V	6-Lead 2 mm x 2 mm VDFN
MIC5305-4.75YML	84H	4.75V	6-Lead 2 mm x 2 mm VDFN
MIC5305YML	8AA	Adjustable	6-Lead 2 mm x 2 mm VDFN
MIC5305-2.8YMT	828	2.8V	6-Lead 2 mm x 2 mm UDFN
MIC5305-4.6YMT	846	4.6V	6-Lead 2 mm x 2 mm UDFN
MIC5305-1.5YD5	N815	1.5V	5-Lead Thin SOT
MIC5305-1.8YD5	N818	1.8V	5-Lead Thin SOT

MARKING CODES

Part Number	Marking Code	Output Voltage	Package
MIC5305-2.5YD5	N825	2.5V	5-Lead Thin SOT
MIC5305-2.6YD5	N826	2.6V	5-Lead Thin SOT
MIC5305-2.7YD5	N827	2.7V	5-Lead Thin SOT
MIC5305-2.8YD5	N828	2.8V	5-Lead Thin SOT
MIC5305-2.85YD5	N82J	2.85V	5-Lead Thin SOT
MIC5305-2.9YD5	N829	2.9V	5-Lead Thin SOT
MIC5305-3.0YD5	N830	3.0V	5-Lead Thin SOT
MIC5305-3.3YD5	N833	3.3V	5-Lead Thin SOT
MIC5305-4.75YD5	N84H	4.75V	5-Lead Thin SOT

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