MIC47100

1A High-Speed, Low-V_{IN} LDO

Features

- Operating Voltage Range:
  - Input Supply: 1.0V to 3.6V
  - Bias Supply: 2.3V to 5.5V
- 0.8V to 2.0V Output Voltage Range
- High Bandwidth: Very Fast Transient Response
- PSRR >50 dB at 100 kHz
- Stable with a 1 µF Ceramic Output Capacitor
- Low Dropout Voltage of 80 mV at 1A
- High Output Voltage Accuracy:
  - ±1.5% Initial Accuracy
  - ±2% over Temperature
- Logic Level Enable Input
- UVLO on Both Supply Voltages for Easy Turn-On
- ePad MSOP-8: Small Form Factor Power Package
- Thermally Enhanced 2 mm x 2 mm VDFN: Smallest Solution

Applications

- Point-of-Load
- PDAs
- DSP, PLD, and FPGA Power Supply
- Low Voltage Post Regulation

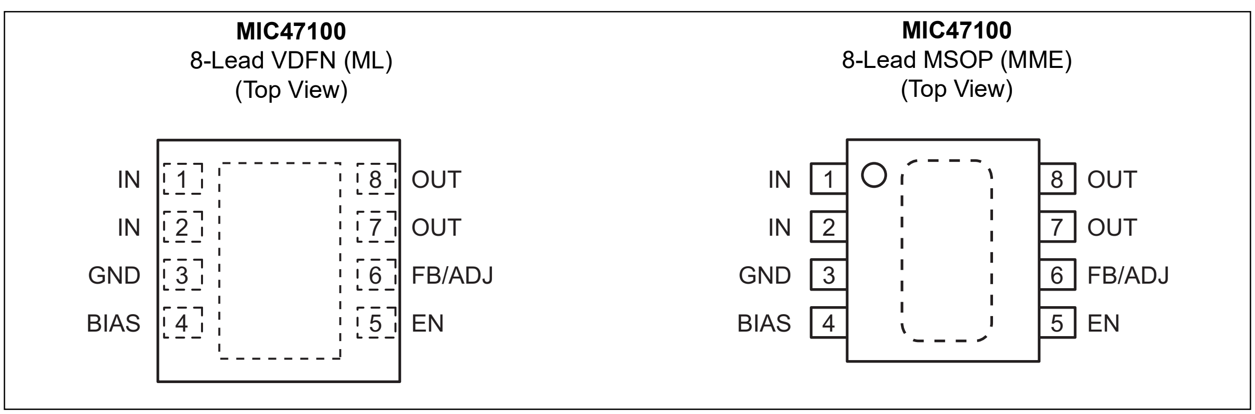
General Description

The MIC47100 is a high-speed, low-V_{IN} LDO capable of delivering up to 1A and designed to take advantage of point-of-load applications that use multiple supply rails to generate a low voltage, high current power supply. The MIC47100 is stable with only a 1 µF ceramic output capacitor and is available in a thermally enhanced 2 mm x 2 mm VDFN package, making it an optimal solution for board-constrained applications.

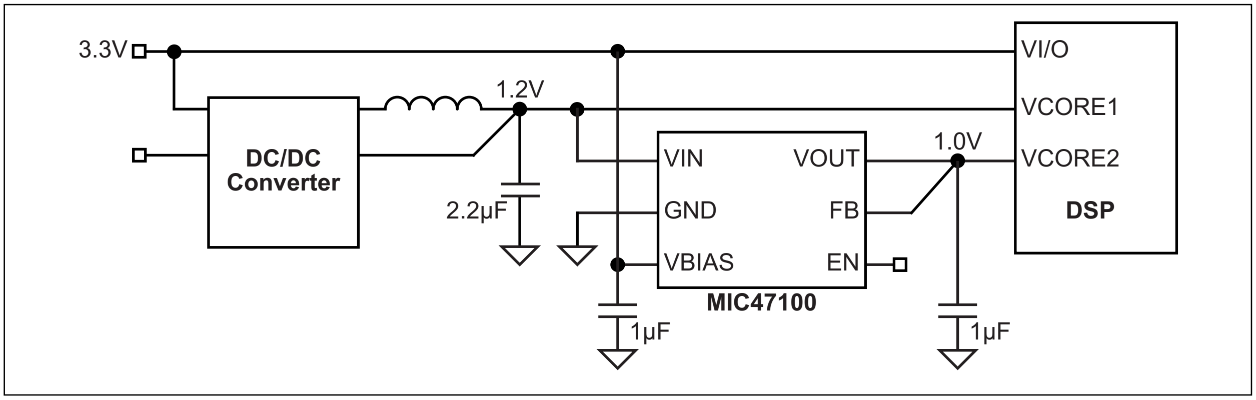
The MIC47100 has an NMOS output stage offering very low output impedance. The NMOS output stage offers a unique ability to respond very quickly to sudden load changes such as that required by a microprocessor, DSP or FPGA. The MIC47100 consumes little quiescent current and therefore can be used for driving the core voltages of mobile processors, post regulating a core DC/DC converter in any portable device.

The MIC47100 is available in fixed and adjustable output voltages in the exposed pad MSOP-8 package and the tiny 2 mm x 2 mm VDFN package with an operating junction temperature range of –40°C to +125°C.

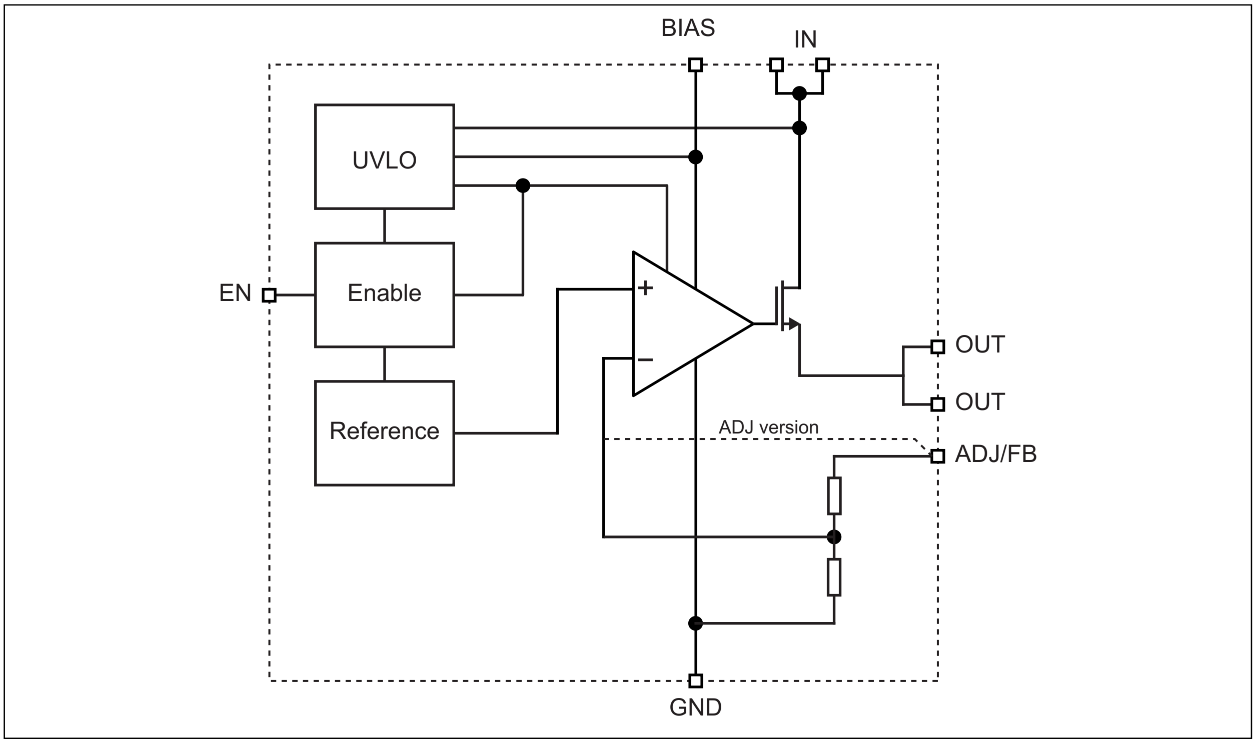
Package Types



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Supply Voltage (V_{IN}) .... 0V to +4V
Bias Supply Voltage (V_{BIAS}) .... 0V to +6V
Enable Voltage (V_{EN}) .... 0V to +6V
Power Dissipation (P_D) .... Note 1, Internally Limited
ESD Rating (Note 2) .... 2 kV

Operating Ratings ‡

Supply Voltage (V_{IN}) .... +1.0V to +3.6V
Bias Supply Voltage (V_{BIAS}) .... +2.3V to +5.5V
Enable Input Voltage (V_{EN}) .... 0V to V_{BIAS}

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(MAX)} = T_{J(MAX)} – T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{IN} = V_{OUT} + 0.5V$; $V_{BIAS} = V_{OUT} + 2.1V$, $I_{OUT} = 100\ \mu A$; $T_A = +25°C$, **bold** values valid for –40°C ≤ T_A ≤ +125°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
UVLO Thresholds, Note 2	$UVLO_{TH}$	**1.9**	2.1	**2.3**	V	Bias Supply
		0.7	0.85	**1.0**		Input Supply
UVLO Hysteresis	$UVLO_{HYS}$	—	70	—	mV	V_{BIAS}
		—	25	—		V_{IN}
Output Voltage Accuracy	V_{OUT}	–1.5	—	1.5	%	Variation from nominal V_{OUT}
		–2.0	—	**2.0**		
Output Voltage Line Regulation (Bias Supply)	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{BIAS})$	–0.1	0.015	0.1	%/V	$V_{BIAS} = V_{OUT} + 2.1V$ to 5.5V
Output Voltage Line Regulation (Input Supply)	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	–0.05	0.005	0.05	%/V	$V_{IN} = V_{OUT} + 0.5V$ to 3.6V
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—	0.2	0.5	%	I_{OUT} = 10 mA to 1A
Input Supply Dropout Voltage	V_{DROP_INPUT}	—	8.5	**50**	mV	I_{OUT} = 100 mA
		—	37	—		I_{OUT} = 500 mA
		—	80	**250**		I_{OUT} = 1A
Bias Supply Dropout Voltage	V_{DROP_BIAS}	—	1.15	—	V	I_{OUT} = 100 mA
		—	1.25	—		I_{OUT} = 500 mA
		—	1.35	**2.1**		I_{OUT} = 1A

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = V_{OUT} + 0.5V; V_{BIAS} = V_{OUT} + 2.1V, I_{OUT} = 100 µA; T_A = +25°C, **bold** values valid for –40°C ≤ T_A ≤ +125°C, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Ground Current from V_{BIAS}	I_{GND_BIAS}	—	350	**500**	µA	I_{OUT} = 1 mA
		—	350	**500**		I_{OUT} = 1A
Shutdown Current from V_{BIAS}	I_{SHDN_BIAS}	—	0.1	1.0	µA	EN ≤ 0.2V
Ground Current from V_{IN}	I_{GND_VIN}	—	6	—	µA	I_{OUT} = 1A
Shutdown Current from V_{IN}	I_{SHDN_VIN}	—	0.1	1.0	µA	EN ≤ 0.2V
Ripple Rejection	PSRR	—	80	—	dB	f = 1 kHz; C_{OUT} = 1.0 µF; I_{OUT} = 100 mA
		—	55	—		f = 100 kHz; C_{OUT} = 1.0 µF; I_{OUT} = 100 mA
		—	45	—		f = 500 kHz; C_{OUT} = 1.0 µF; I_{OUT} = 100 mA
Current Limit	I_{LIM}	1.1	1.6	2.5	A	V_{IN} = 2.7V; V_{OUT} = 0V
Output Voltage Noise	e_N	—	63	—	$µV_{RMS}$	C_{OUT} = 1 µF; 10 Hz to 100 kHz; I_{OUT} = 100 mA
Overtemperature Shutdown	TH_{SHDN}	—	160	—	°C	—
Overtemperature Shutdown Hysteresis	TH_{SHDN_HYS}	—	20	—	°C	—
Enable Inputs						
Enable Voltage	V_{IL}	—	—	**0.2**	V	Logic Low
	V_{IH}	**1.0**	—	—		Logic High
Enable Input Current	I_{IL}	—	1	—	µA	V_{IL} ≤ 0.2V
	I_{IH}	—	6	—		V_{IH} = 1.2V
Turn-On Time	t_{ON}	—	35	**500**	µs	C_{OUT} = 1 µF; 90% of typical V_{OUT}
Reference Voltage (Adjustable Option Only)						
Reference Voltage	V_{REF}	0.69	0.7	0.71	V	—
		0.686	—	**0.714**		
ADJ Pin Input Current	I_{IN_ADJ}	—	20	—	nA	—

Note 1: Specification for packaged product only.

2: Both UVLO thresholds must be met for the output voltage to be allowed to turn-on. If either of the two input voltages are below the UVLO thresholds, the output is kept off.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, ?? sec.
Package Thermal Resistances						
Thermal Resistance, ePad MSOP 8-Ld	θ_{JA}	—	64	—	°C/W	—
Thermal Resistance, VDFN 8-Ld	θ_{JA}	—	90	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

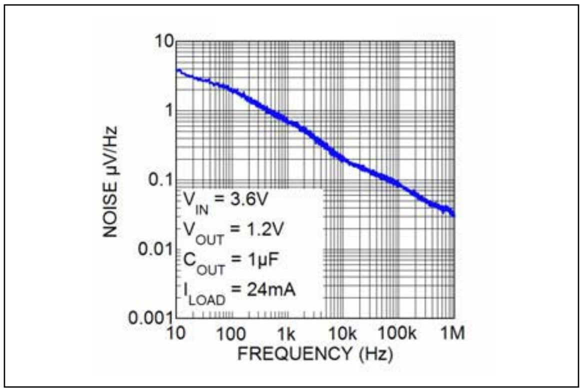


FIGURE 2-1: *Output Noise Spectral Density.*

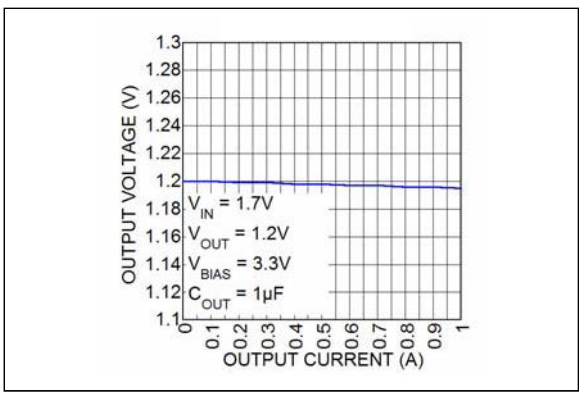


FIGURE 2-2: *Load Regulation.*

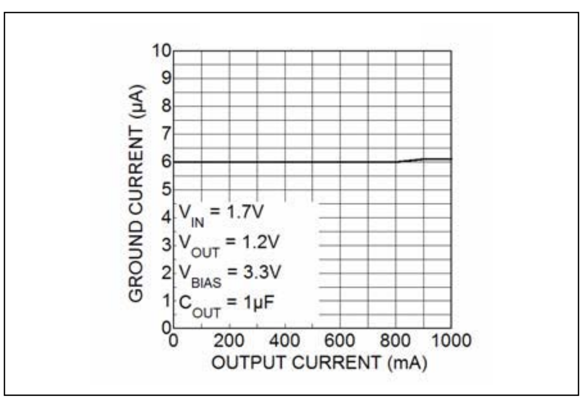


FIGURE 2-3: *Ground Pin Current from V_{IN} vs. Output Current.*

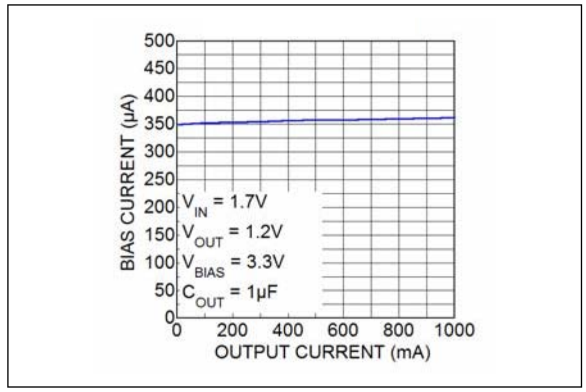


FIGURE 2-4: *Bias Current vs. Output Current.*

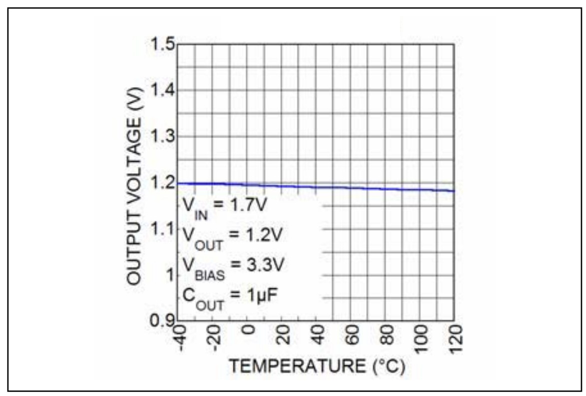


FIGURE 2-5: *Output Voltage vs. Temperature.*

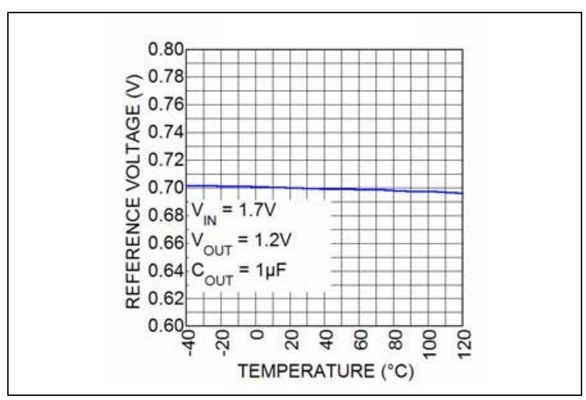


FIGURE 2-6: *Reference Voltage vs. Temperature.*

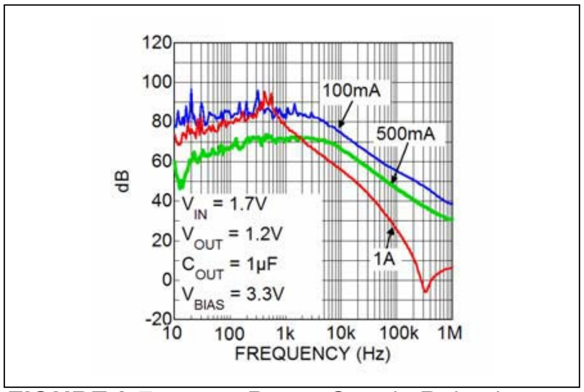


FIGURE 2-7: *Power Supply Rejection Ratio (Input Supply).*

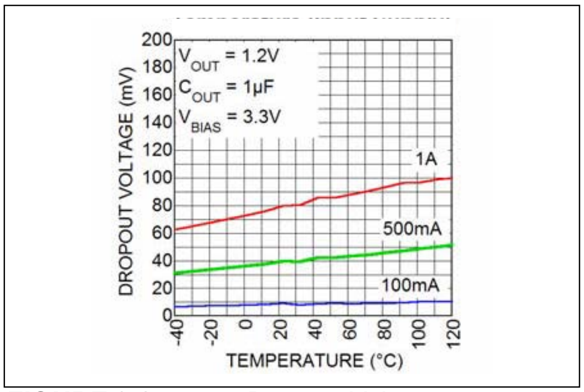


FIGURE 2-8: *Dropout Voltage vs. Temperature (Input Supply).*

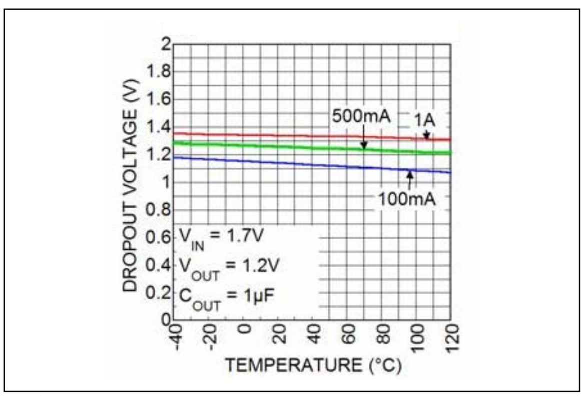


FIGURE 2-9: *Dropout Voltage vs. Temperature (V_{BIAS} Supply).*

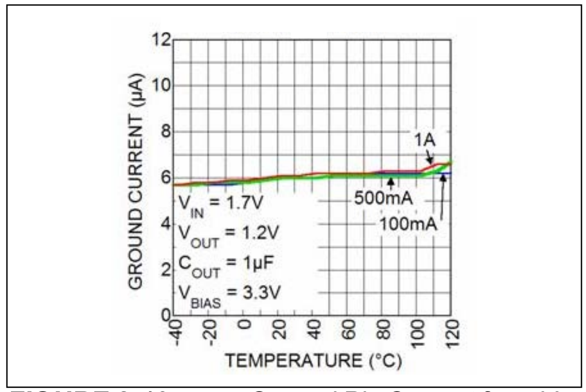


FIGURE 2-10: *Ground Pin Current from V_{IN} vs. Temperature.*

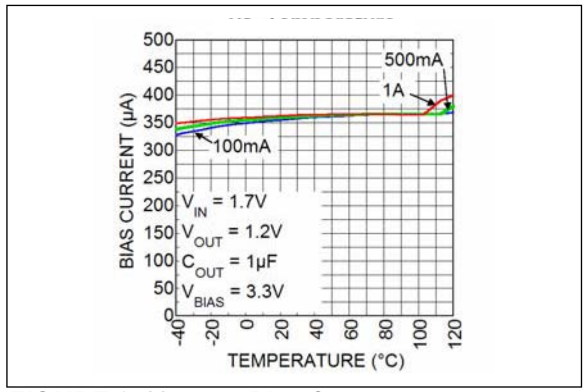


FIGURE 2-11: *Bias Current vs. Temperature.*

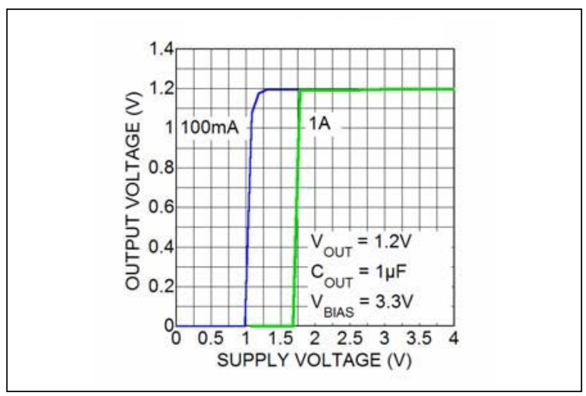


FIGURE 2-12: *Dropout Characteristics (Input Supply).*

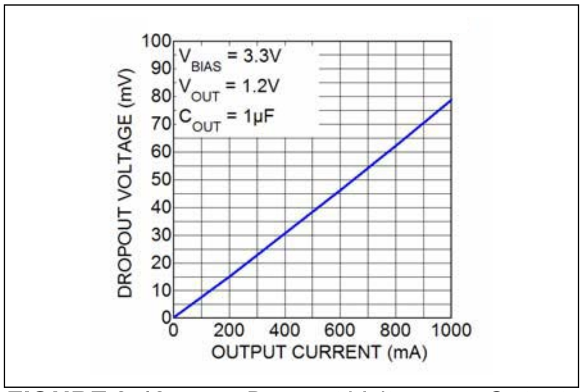


FIGURE 2-13: *Dropout Voltage vs. Output Current (Input Supply).*

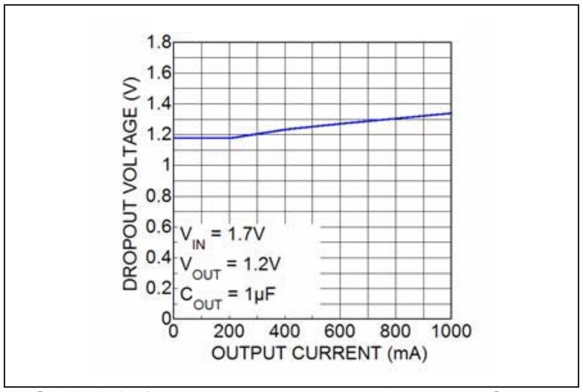


FIGURE 2-14: *Dropout Voltage vs. Output Current (Bias Supply).*

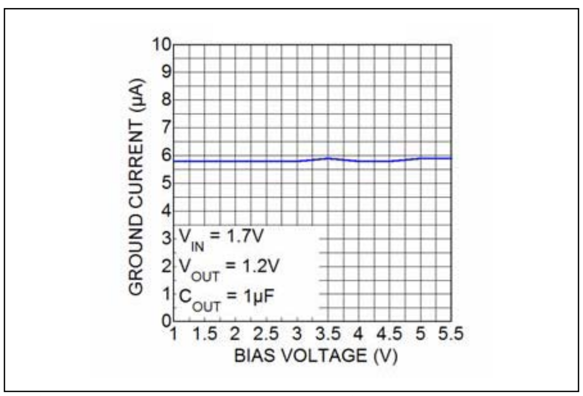


FIGURE 2-15: *Ground Current vs. Bias Voltage.*

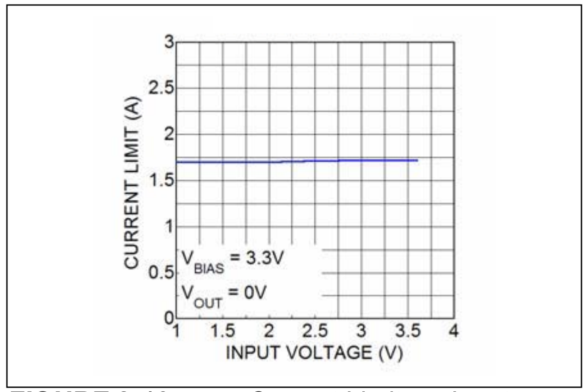


FIGURE 2-16: *Current Limit vs. Input Voltage.*

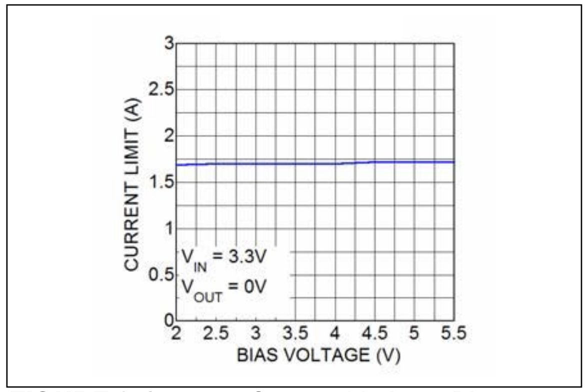


FIGURE 2-17: *Current Limit vs. Bias Voltage.*

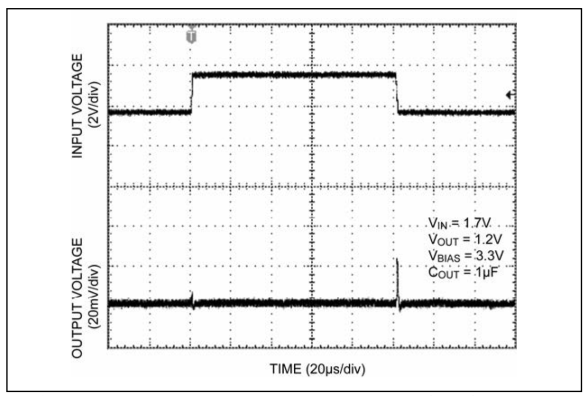


FIGURE 2-18: *Line Transient (V_{IN}).*

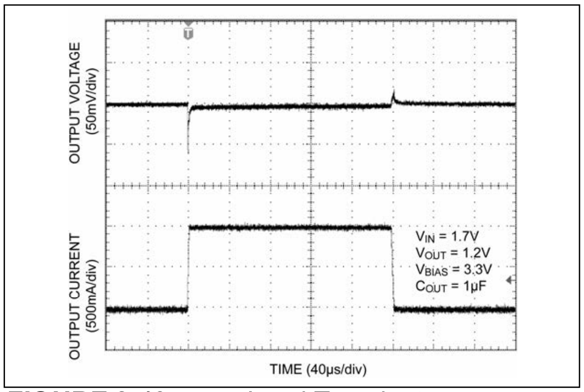


FIGURE 2-19: *Load Transient.*

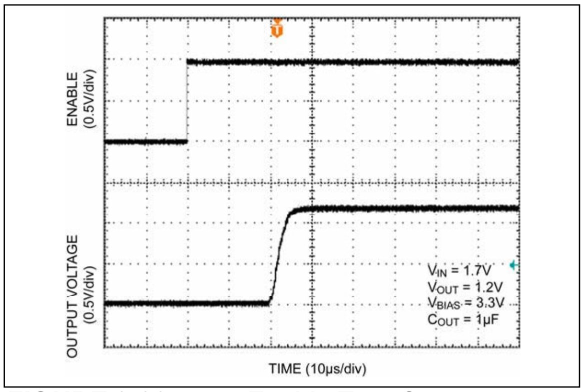


FIGURE 2-20: *Enable Turn-On.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number VDFN	Pin Number MSOP	Pin Name	Description
1, 2	1, 2	IN	Input Supply. Drain of NMOS pass transistor which is the power input voltage for regulator. The NMOS pass transistor steps down this input voltage to create the output voltage.
3	3	GND	Ground. Ground pins and exposed pad must be connected externally.
4	4	BIAS	Bias Supply. The bias supply is the power supply for the internal circuitry of the regulator.
5	5	EN	Enable: TTL/CMOS compatible input. Logic high = enable, logic low or open = shutdown
6 (Fixed)	6 (Fixed)	FB	Feedback Input. Connect to OUT. Optimum load regulation is obtained when feedback is taken from the actual load point.
6 (Adj.)	6 (Adj.)	ADJ	Adjust Input. Connect external resistor divider to program output voltage.
7, 8	7, 8	OUT	Output. Output Voltage of Regulator

4.0 APPLICATION INFORMATION

The MIC47100 is a high-speed, dual-supply NMOS LDO designed to take advantage of point-of-load applications that use multiple supply rails to generate a low voltage, high current power supply. The MIC47100 can source 1A of output current while only requiring a 1 µF ceramic output capacitor for stability.

The MIC47100 regulator is fully protected from damage due to fault conditions, offering linear current limiting and thermal shutdown.

4.1 Bias Supply Voltage

V_{BIAS}, requiring relatively light current, provides power to the control portion of the MIC47100. Bypassing on the bias pin is recommended to improve performance of the regulator during line and load transients. Small ceramic capacitors from V_{BIAS}-to-ground help reduce high frequency noise from being injected into the control circuitry from the bias rail and are good design practice.

4.2 Input Supply Voltage

V_{IN} provides the supply to power the LDO. The minimum input voltage is 1V, allowing conversion from low voltage supplies.

4.3 Output Capacitor

The MIC47100 requires an output capacitor of 1 µF or greater to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1 µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

4.4 Input Capacitor

The MIC47100 is a high-performance, high bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1 µF capacitor is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high-frequency capacitors, such as small-valued NPO dielectric-type capacitors, help filter out high-frequency noise and are good practice in any RF-based circuit.

4.5 Minimum Load Current

The MIC47100, unlike most other regulators, does not require a minimum load to maintain output voltage regulation.

4.6 Adjustable Regulator Design

The MIC47100 adjustable version allows programming the output voltage anywhere between 0.8V and 2.0V. Two resistors are used. The R1 resistor value between V_{OUT} and the adjust pin should not exceed 10 kΩ. Larger values can cause instability. R2 connects between the adjust pin and ground. The resistor values are calculated by:

EQUATION 4-1:

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.7} - 1\right)$$

Where:
V_{OUT} = The desired output voltage.

4.7 Enable/Shutdown

The MIC47100 comes with a single active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a “zero” off-mode current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. The active-high enable pin uses CMOS technology and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

4.8 Thermal Considerations

The MIC47100 is designed to provide 1A of continuous current in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. Given that the input voltage is 1.8V, the output voltage is 1.2V and the output current is 1A. The actual power dissipation of the regulator circuit can be determined using the following equation:

EQUATION 4-2:

$$P_D = (V_{IN} - V_{OUT1}) \times I_{OUT} + V_{BIAS} \times I_{GND}$$

Because this device is CMOS, the ground current is insignificant for power dissipation and can be ignored for this calculation.

EQUATION 4-3:

$$P_D = (1.8V - 1.2V) \times 1A = 0.6W$$

To determine the maximum ambient operating temperature of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

EQUATION 4-4:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where:

$T_{J(MAX)}$ = 125°C, the max. junction temperature of the die.

θ_{JA} = 90°C/W, the thermal resistance of the VDFN-8.

Table 4-1 shows junction-to-ambient thermal resistance for the MIC47100 in the VDFN package.

TABLE 4-1: THERMAL RESISTANCE

Package	θ_{JA} Rec. Min. Footprint	θ_{JC}
8-Lead VDFN	90°C/W	2°C/W

Substituting P_D for $P_{D(MAX)}$ and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit. The junction-to-ambient thermal resistance for the minimum footprint is 90°C/W.

The maximum power dissipation must not be exceeded for proper operation.

For example, when operating the MIC47100-1.2YML at an input voltage of 1.8V and a 1A load with a minimum footprint layout, the maximum ambient operating temperature T_A can be determined as follows:

EQUATION 4-5:

$$0.6W = \frac{125°C - T_A}{90°C/W}$$

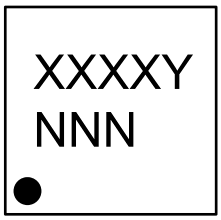
$$T_A = 71°C$$

Therefore, a 1.2V application with 1A of output current can accept an ambient operating temperature of 71°C in a 2 mm x 2 mm VDFN package. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the “Regulator Thermals” section of Microchip’s Designing with Low-Dropout Voltage Regulators handbook.

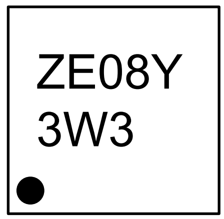
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

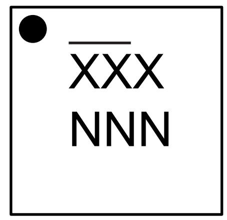
8-Lead VDFN*



Example



8-Lead MSOP*



Example

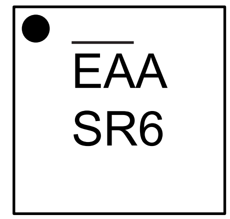


TABLE 5-1: MARKING CODES

Part Number	Marking Code	Nominal Output Voltage	Package
MIC47100YML	EAA	ADJ.	8-Lead 2 mm x 2 mm VDFN
MIC47100-0.8YML	E08	0.8V	8-Lead 2 mm x 2 mm VDFN
MIC47100-1.0YML	E10	1.0V	8-Lead 2 mm x 2 mm VDFN
MIC47100-1.2YML	E12	1.2V	8-Lead 2 mm x 2 mm VDFN
MIC47100YMME	ZEAAY	ADJ.	8-Lead ePad MSOP
MIC47100-08YMME	ZE08Y	0.8V	8-Lead ePad MSOP
MIC47100-10YMME	ZE10Y	1.0V	8-Lead ePad MSOP
MIC47100-12YMME	ZE12Y	1.2V	8-Lead ePad MSOP

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

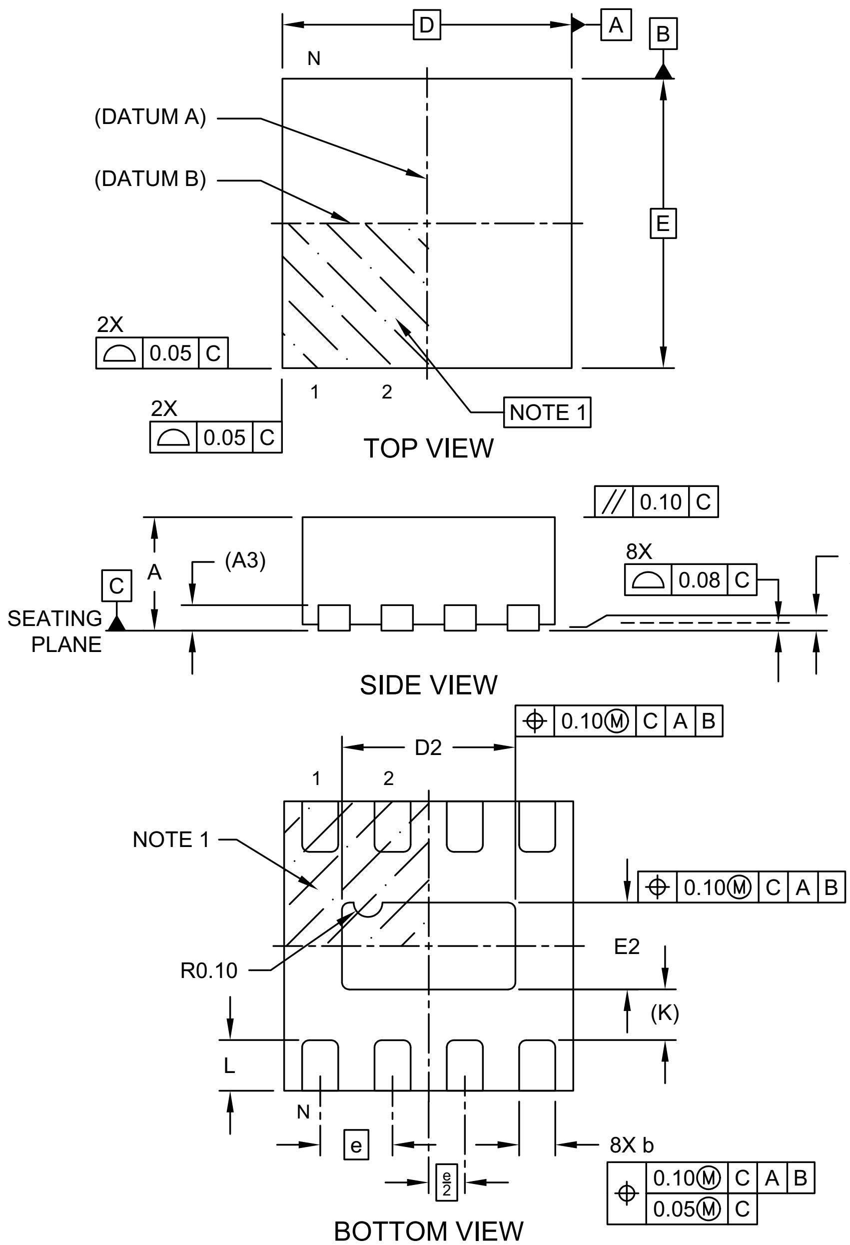
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2x0.9 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

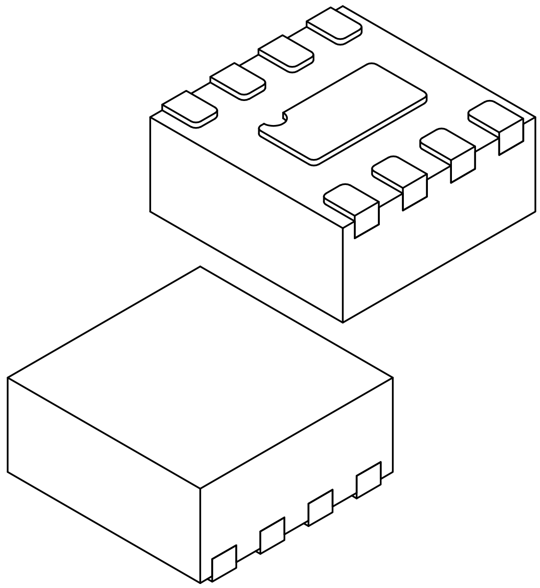
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1247 Rev A Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2x.9 mm Body [VDFN] With 1.20x0.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.50	0.60	0.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K		0.35 REF	

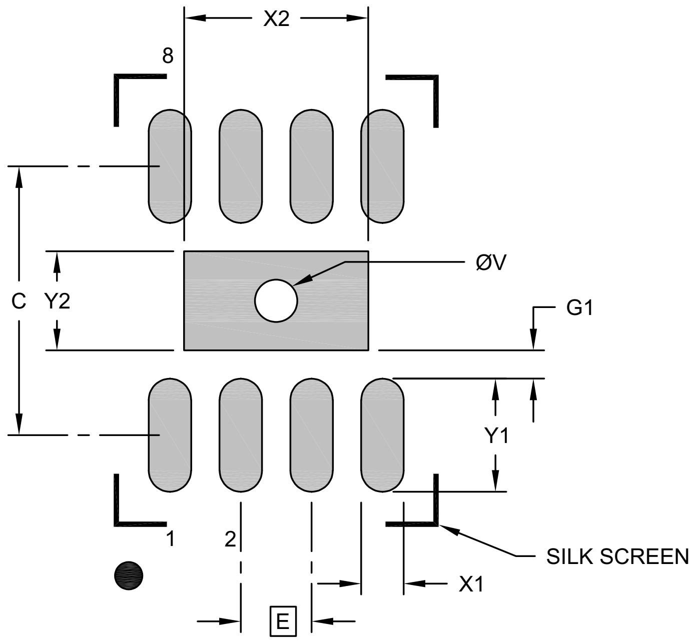
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1247 Rev A Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (H2A) - 2x2 mm Body [VDFN] Micrel Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			0.70
Optional Center Pad Length	Y2			1.30
Contact Pad Spacing	C		1.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.80
Contact Pad to Center Pad (X8)	G1	0.20		
Thermal Via Diameter	V		0.30	

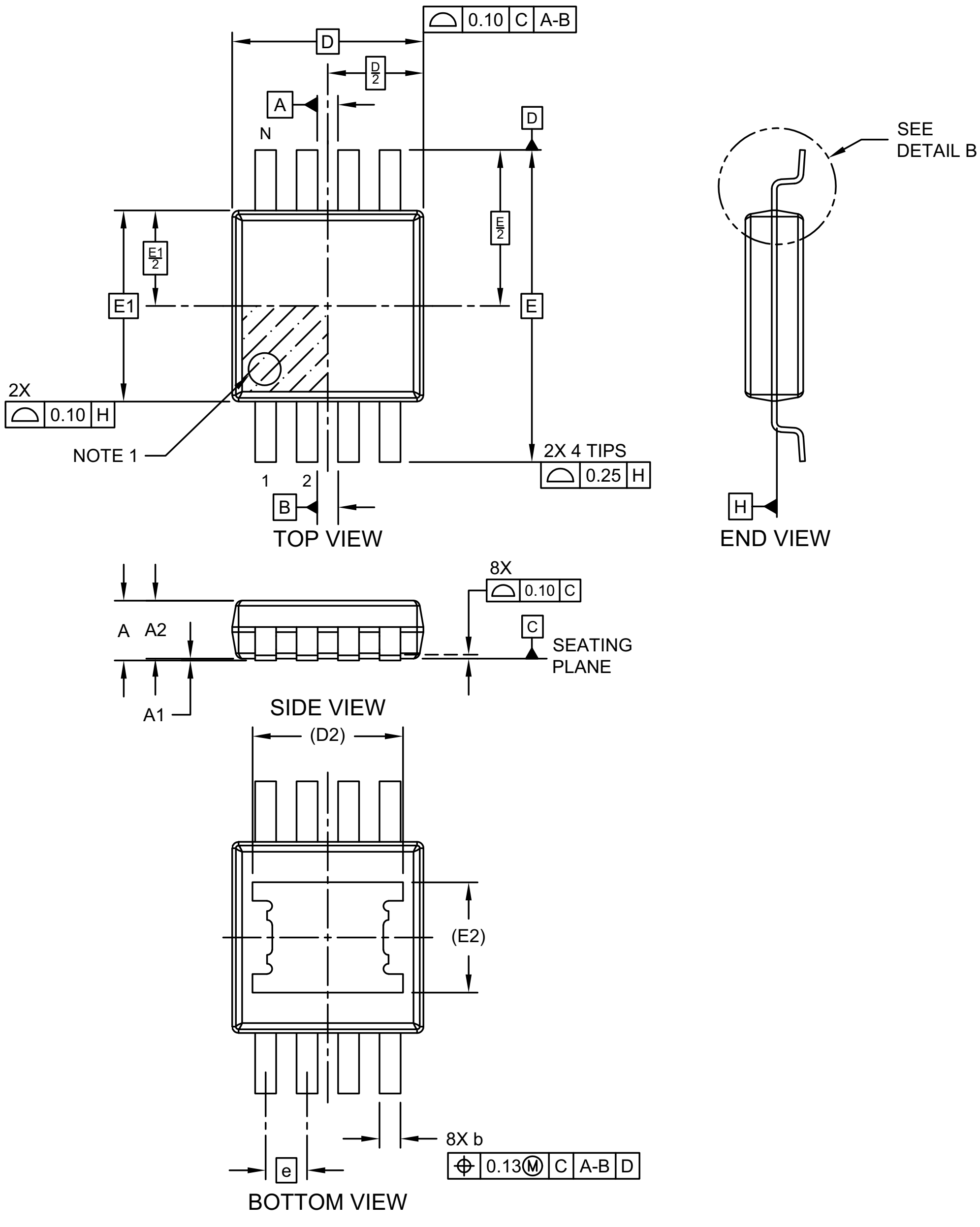
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3247 Rev. A

8-Lead Micro Small Outline Package (DPA) - 3x3 mm Body [MSOP]
With 2.36x1.73 mm Exposed Pad; Micel Legacy Package eP-MSOP-08L

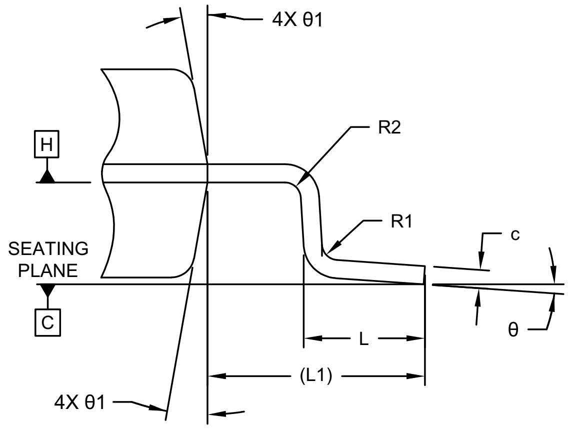
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



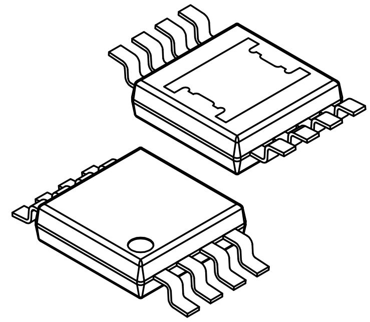
Microchip Technology Drawing C04-1085 Rev A Sheet 1 of 2

8-Lead Micro Small Outline Package (DPA) - 3x3 mm Body [MSOP] With 2.36x1.73 mm Exposed Pad; Micel Legacy Package eP-MSOP-08L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B
ROTATED FOR CLARITY



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.84	0.94	1.04
Standoff	A1	0.03	0.08	0.13
Molded Package Thickness	A2	0.81	0.86	0.91
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Exposed Pad Length	D2		2.36 REF	
Exposed Pad Width	E2		1.73 REF	
Terminal Width	b	0.30	0.33	0.43
Terminal Thickness	c	0.10	0.15	0.20
Terminal Length	L	0.43	0.53	0.63
Footprint	L1		0.95 REF	
Lead Bend Radius	R1	0.07	–	–
Lead Bend Radius	R2	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

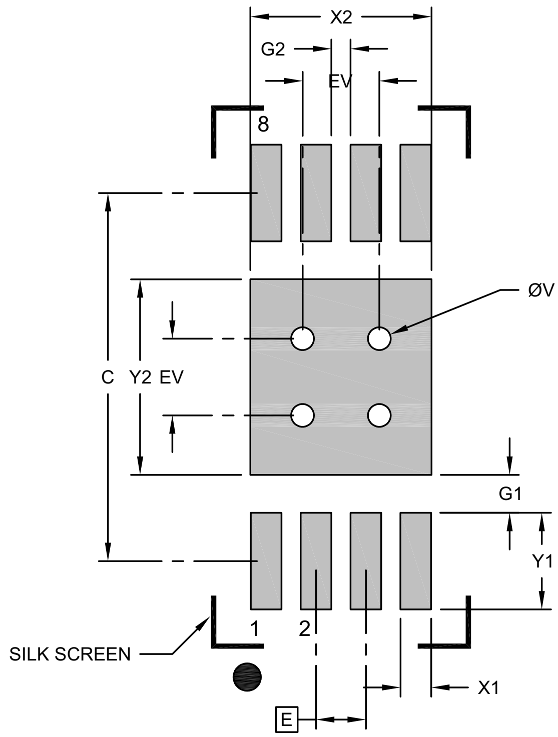
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1085 Rev A Sheet 2 of 2

**8-Lead Micro Small Outline Package (DPA) - 3x3 mm Body [MSOP]
With 2.36x1.73 mm Exposed Pad; Micel Legacy Package eP-MSOP-08L**

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65	
Center Pad Width	X2			2.36
Center Pad Length	Y2			2.55
Contact Pad Spacing	C		4.80	
Contact Pad Width (X8)	X1			0.40
Contact Pad Length (X8)	Y1			1.26
Contact Pad to Center Pad (X8)	G1	0.50		
Contact Pad to Contact Pad (X6)	G2	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3085 Rev A

APPENDIX A: REVISION HISTORY

Revision A (February 2024)

- Converted Micrel document MIC47100 to Microchip data sheet DS20006801A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number	-X.X	X	XXX	-XX
Device	Output Voltage	Temp. Range	Package	Media Type

Device:	MIC47100:		1A High-Speed, Low-V_{IN} LDO
Output Voltage: Note 1	<blank>	=	Adjustable
	0.8	=	0.8V
	1.0	=	1.0V
	1.2	=	1.2V
Temperature Range:	Y	=	–40°C to +125°C
Package:	ML	=	8-Lead 2 mm x 2 mm VDFN
	MME	=	8-Lead ePad MSOP
Media Type:	<blank>	=	100/Tube (MSOP option only)
	TR	=	2,500/Reel (MSOP option)
	TR	=	5,000/Reel (VDFN option)

Note 1: For the MSOP package option, the output voltage element in the part number does not include a decimal point. See the Examples section on this page for instances of how that is represented.

Examples:

a) MIC47100YML-TR: MIC47100, Adj. Output Voltage, –40°C to +125°C Temp. Range, 8-Lead VDFN, 5,000/Reel

b) MIC47100-08YMME: MIC47100, 0.8V Output Voltage, –40°C to +125°C Temp. Range, 8-Lead MSOP, 100/Tube

c) MIC47100-1.0YML-TR: MIC47100, 1.0V Output Voltage, –40°C to +125°C Temp. Range, 8-Lead VDFN, 5,000/Reel

d) MIC47100-12YMME-TR: MIC47100, 1.2V Output Voltage, –40°C to +125°C Temp. Range, 8-Lead MSOP, 2,500/Reel

e) MIC47100YMME: MIC47100, Adj. Output Voltage, –40°C to +125°C Temp. Range, 8-Lead MSOP, 100/Tube

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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