



MIC4414/MIC4415 Evaluation Board

1.5A / 4.5V to 18V
Low-Side MOSFET Driver

General Description

The MIC4414 and MIC4415 are low-side MOSFET drivers designed to switch an N-channel enhancement type MOSFET in low-side switch applications. The MIC4414 is a non-inverting driver and the MIC4415 is an inverting driver. These drivers feature short delays and high peak current to produce precise edges and rapid rise and fall times.

The MIC4414/15 are powered from a 4.5V to 18V supply and can sink and source peak currents up to 1.5A, switching a 1000pF capacitor in 12ns. The on-state gate drive output voltage is approximately equal to the supply voltage (no internal regulators or clamps). High supply voltages, such as 10V, are appropriate for use with standard N-channel MOSFETs. Low supply voltages, such as 5V, are appropriate for use with many logic-level N-channel MOSFETs.

In a low-side configuration, the driver can control a MOSFET that switches any voltage up to the rating of the MOSFET.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Requirements

The MIC4414/MIC4415 evaluation board requires only a single power supply to power the driver and a function generator or logic signal to drive the IN pin.

Precautions

The MIC4414/MIC4415 evaluation board does not have reverse polarity protection. Applying a negative voltage to the VDD and GND terminals may damage the device. The maximum VDD of the board is rated at 20V. Exceeding 20V on the VDD could damage the device.

Getting Started

1. VDD Supply

Connect a supply to the VS and GND terminals, paying careful attention to the polarity and the supply range ($4.5V < VDD < 18V$). Monitor I_{DD} with a current meter and VDD at VS and GND terminals with voltmeter. Do not apply power until Step 4.

2. Connect Function Generator to IN pin

Connect the Function generator output to IN pin and GND.

3. OUT Signal

The voltage on OUT pin can be monitored by either a voltmeter or with scope probe.

4. Turn on the Power

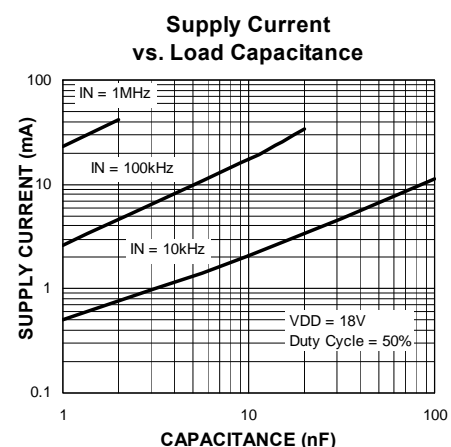
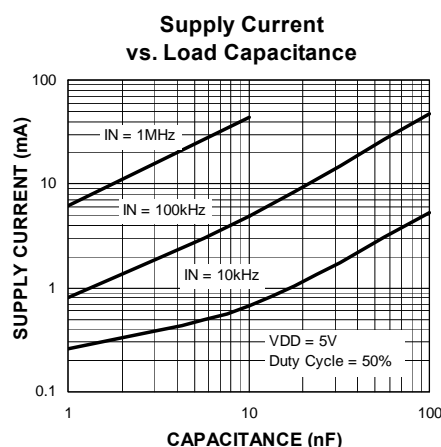
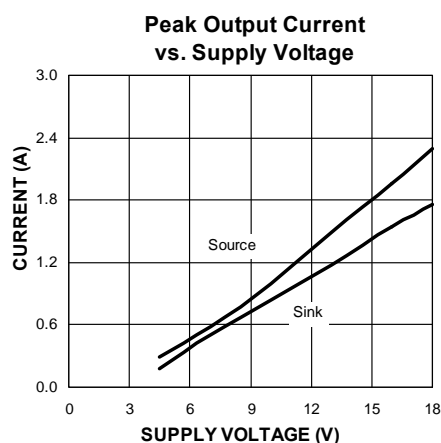
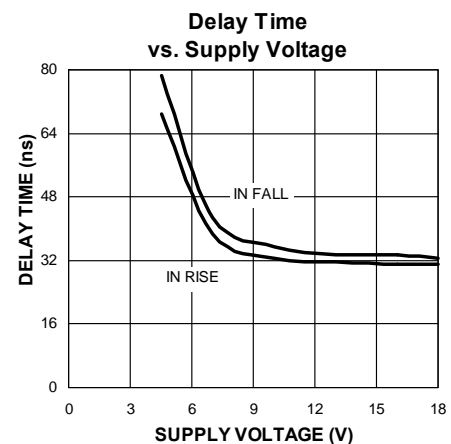
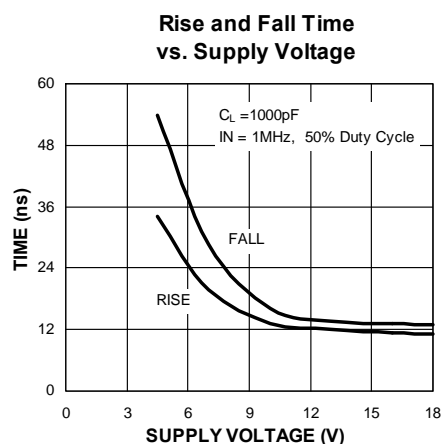
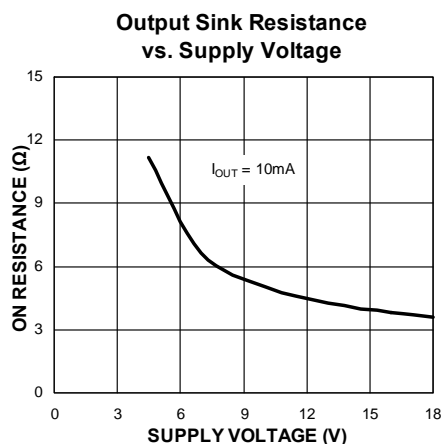
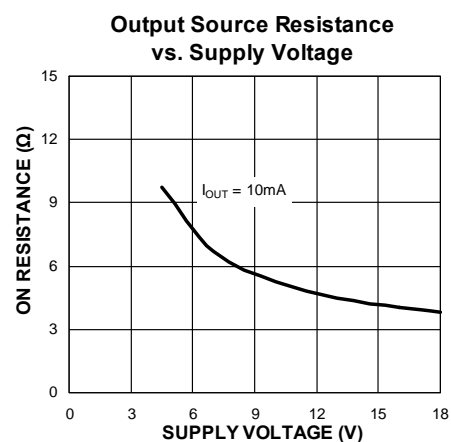
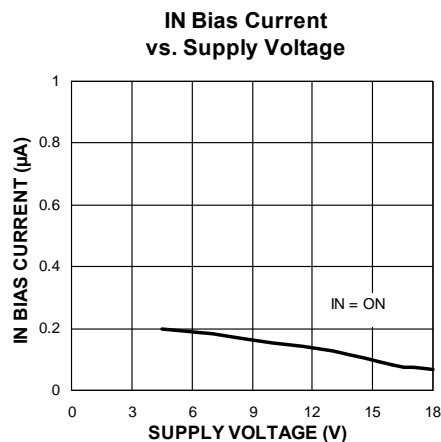
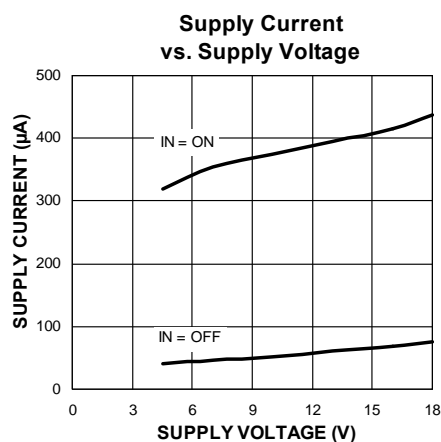
Turn on the VDD supply and apply logic signal to IN pin, and verify OUT signal. The on-state gate drive output voltage is approximately equal to the supply voltage (no internal regulators or clamps). Since the MIC4414 is a non-inverting driver so a logic high signal on the IN pin makes the OUT signal high (typically VDD) and MIC4415 is an inverting driver so logic low signal on the IN pin makes the OUT signal high (typically VDD).

The user has a flexibility of soldering a FET (Q1) or using different values of capacitors to imitate the gate capacitance (C3).

Ordering Information

Part Number	Description
MIC4414YFT EV	MIC4414 Evaluation Board
MIC4415YFT EV	MIC4415 Evaluation Board

MIC4414/MIC4415 Evaluation Board Typical Characteristics

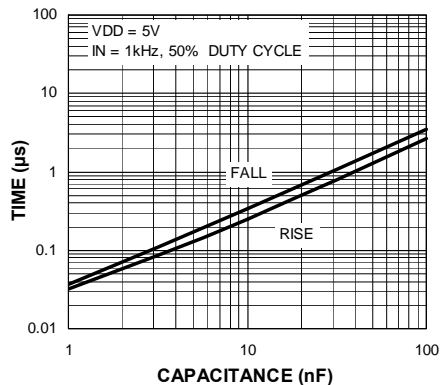


Note:

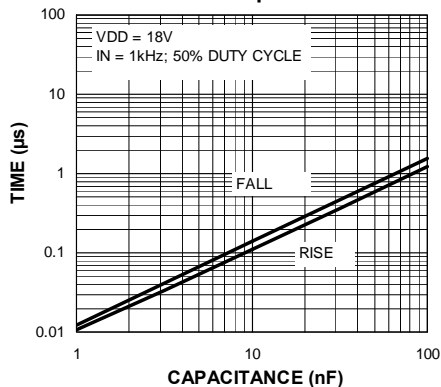
1. MIC4414 ON IN = 5V; OFF IN = 0V.
2. MIC4415 ON IN = 0V; OFF IN = 5V.

Typical Characteristics (Continued)

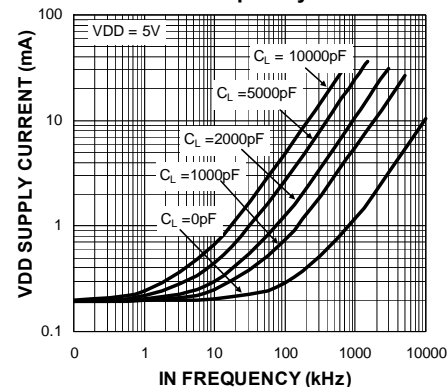
**Output Rise and Fall Time
vs. Load Capacitance**



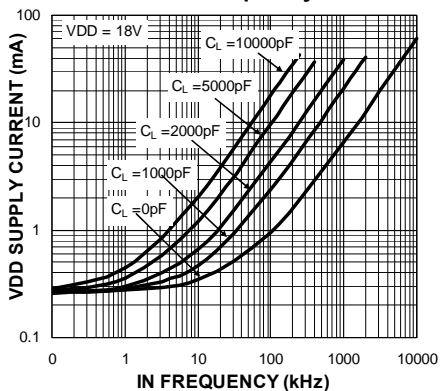
**Output Rise and Fall Time
vs. Load Capacitance**



**VDD Supply Current
vs. Frequency**



**VDD Supply Current
vs. Frequency**



MIC4414/MIC4415 Evaluation Board Schematic

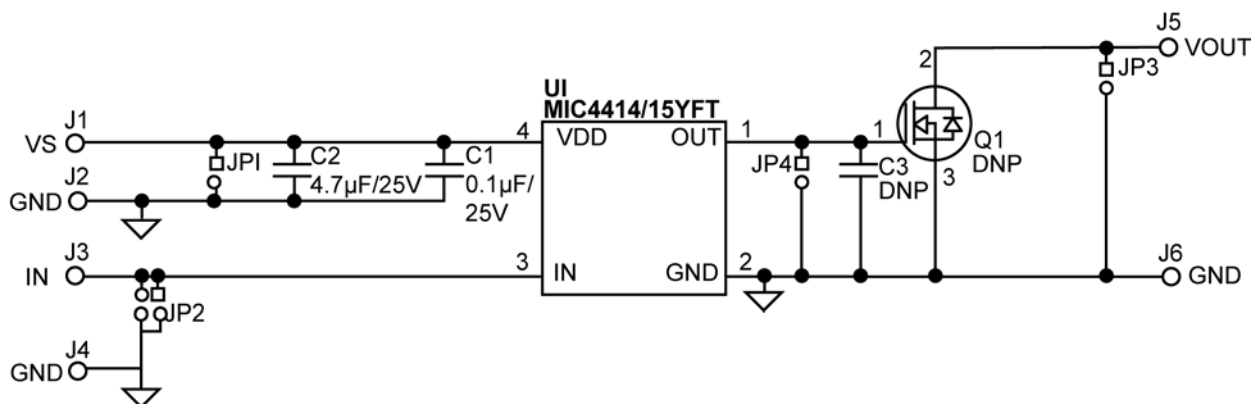


Figure 1. MIC4414/MIC4415 Evaluation board schematic

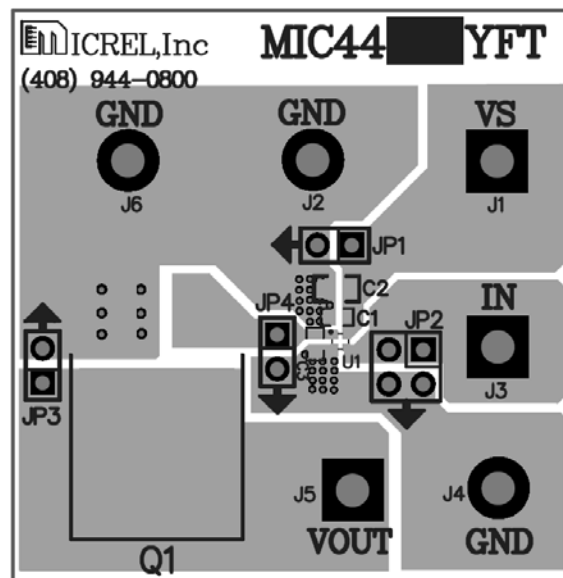
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty
C1	GRM188R71E104KA01D	Murata ⁽¹⁾	0.1µF/25V Ceramic Capacitor, X7R, Size 0603	1
C2	C2012X5R1E475K	TDK ⁽²⁾	4.7µF/25V Ceramic Capacitor, X5R, Size 0805	1
	GRM21BR61E475KA12L	Murata		
	08053D475KAT2A	AVX ⁽³⁾		
C3, Q1			Do not populate (DNP)	
U1	MIC4414YFT MIC4415YFT	Micrel, Inc. ⁽⁴⁾	1.5A/4.5V to 18V Low Side MOSFET Driver	1

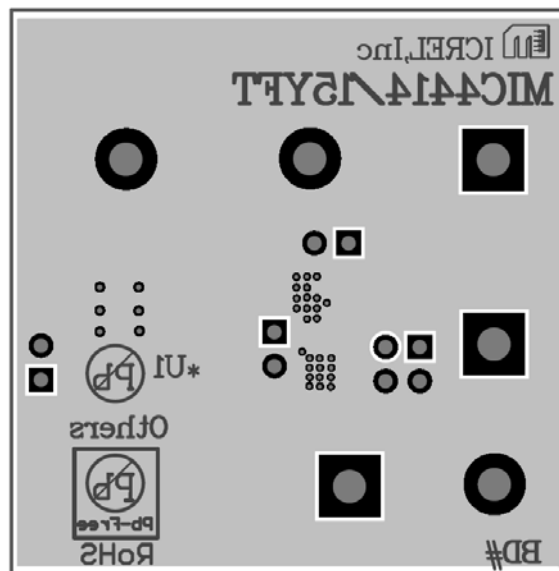
Notes:

1. Murata: www.murata.com.
2. TDK: www.tdk.com.
3. AVX: www.avx.com
4. Micrel, Inc.: www.micrel.com.

Evaluation Board PCB Layout



MIC4414/MIC4415 Evaluation Board – Copper Layer 1 (Top)



MIC4414/MIC4415 Evaluation Board – Copper Layer 2 (Bottom)

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