MIC4126/27/28

Dual 1.5A-Peak Low-Side MOSFET Drivers in Advanced Packaging

Features

- Dual 1.5A-Peak Drivers
- 4.5V to 20V Operating Range
- Exposed Backside Pad Packaging Reduces Heat
  - ePAD SOIC-8L (θ_{JA} = 58°C/W)
  - ePAD MSOP-8L (θ_{JA} = 60°C/W)
  - VDFN ML™-8L (θ_{JA} = 60°C/W)
- Bipolar/CMOS/DMOS Construction
  - 25mV maximum output offset from supply or ground
- Latch-Up Protection to >200mA Reverse Current
- Switches 1000pF in 25ns
- Logic-Input Threshold Independent of Supply Voltage
- Logic-Input Protection to –5V
- 6pF Typical Equivalent Input Capacitance
- Dual Inverting, Dual Noninverting, and Complementary Configurations
  - -40°C to +125°C operating junction temperature range

Applications

- DC/DC Converters
- Motor Drivers
  - Clock Line Driver

General Description

The MIC4126, MIC4127, and MIC4128 family are highly-reliable dual 1.5A low-side MOSFET drivers fabricated on Microchip's BiCMOS/DMOS process. The devices feature low power consumption and high efficiency. The MIC4126/27/28 translate TTL or CMOS input logic levels to output voltage levels that swing within 25mV of the positive supply or ground whereas comparable bipolar devices are capable of swinging only to within 1V of the supply. The MIC4126/7/8 is available in three configurations: dual inverting, dual noninverting, and complimentary output.

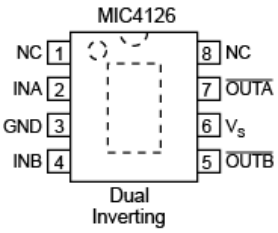
The MIC4126/27/28 offer pin-compatible as well as smaller footprint replacements for the MIC4426/27/28 with improved packaging and electrical performance. The MIC4126/27/28 are available in exposed pad, EPAD, SOIC-8L and MSOP-8L options as well as a small-size VDFN ML™-8L option. The devices have an input operating range of 4.5V to 20V.

Primarily intended for driving power MOSFETs, MIC4426/7/8 drivers are suitable for driving other loads (capacitive, resistive, or inductive) which require low-impedance, high peak current, and fast switching time. The devices can withstand up to 500mA of reverse current (either polarity) without latching and up to 5V noise spikes (either polarity) on ground pins.

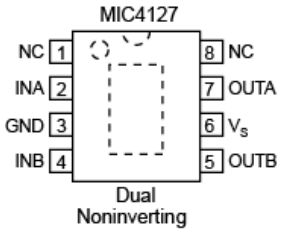
Data sheets and support documentation can be found on Microchip's website at www.microchip.com.

Package Types

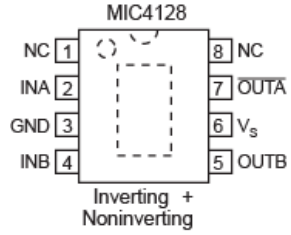
MIC4126
ePad SOIC-8L (ME)
ePad MSOP-8L (MME)
VDFN-8 (ML)
(Top View)



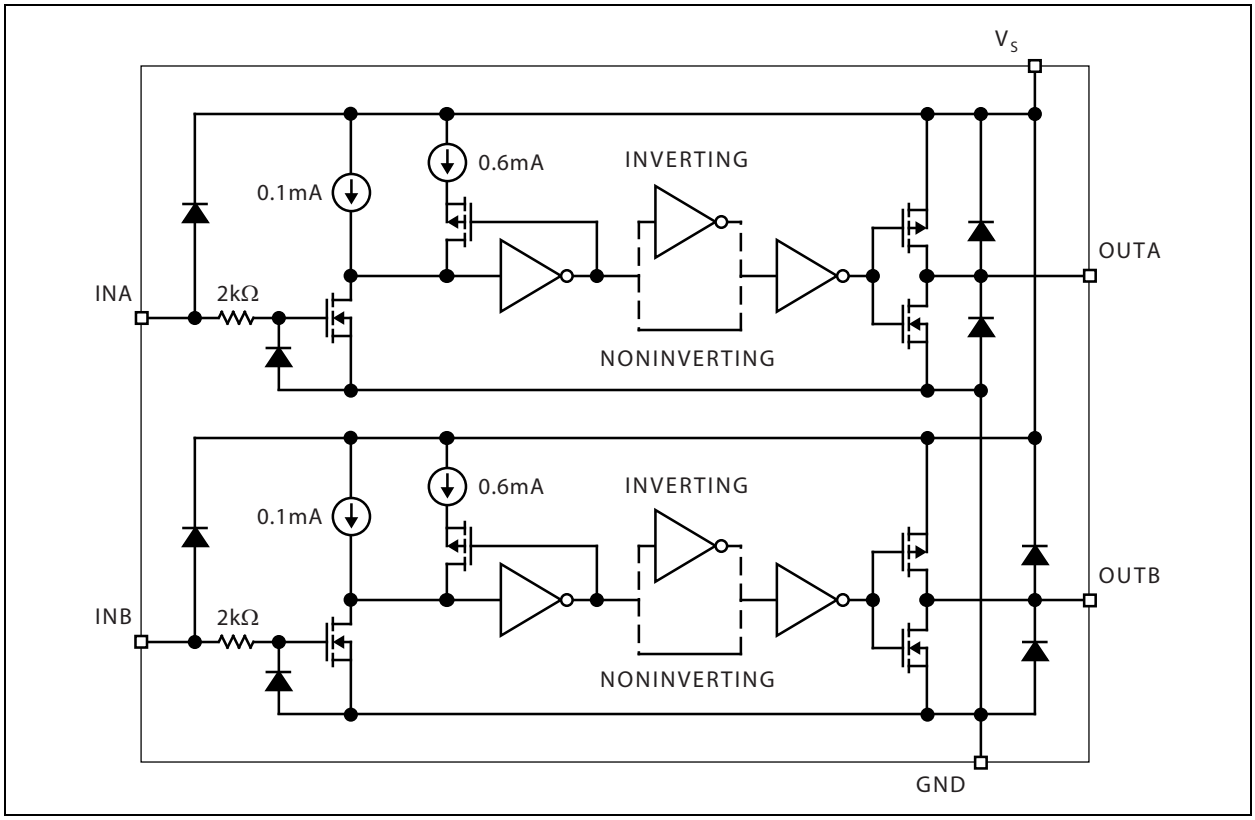
MIC4127
ePad SOIC-8L (ME)
ePad MSOP-8L (MME)
VDFN-8 (ML)
(Top View)



MIC4128
ePad SOIC-8L (ME)
ePad MSOP-8L (MME)
VDFN-8 (ML)
(Top View)



Functional Block Diagram



The function block diagram contains only four resistors, four capacitors, and 52 transistors. Be sure to ground any unused inputs.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... +24V
Input Voltage ..... V_S + 0.3V to GND – 5V
ESD Susceptibility ..... (Note 1)

Operating Ratings ††

Supply Voltage (V_S) ..... +4.5V to +20V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 4.5V ≤ V_S ≤ 20V; T_A = +25°C, **bold** values indicate full specified temperature range; unless noted. Input voltage slew rate >1V/µs; C_{OUT} = 1000pF. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Logic 1 Input Voltage	V_{IH}	2.4	1.4	—	V	—
		2.4	**1.6**	—	V	—
Logic 0 Input Voltage	V_{IL}	—	1.1	0.8	V	—
		—	**1.3**	**0.8**	V	—
Input Current	I_{IN}	**–1**	—	**1**	µA	0V ≤ V_{IN} ≤ V_S
Output						
High Output Voltage	V_{OH}	**V_S – 0.025**	—	—	V	—
Low Output Voltage	V_{OL}	—	—	**0.025**	V	—
Output Resistance	R_O	—	6	10	Ω	I_{OUT} = 10 mA, V_S = 20V
		—	**8**	**12**		
Peak Output Current	I_{PK}	—	**1.5**	—	A	—
Latch-Up Protection	I	**>200**	—	—	mA	Withstand Reverse Current
Switching Time						
Rise Time	t_R	—	13	30	ns	Test Figure 1-1
		—	**20**	**40**		
Fall Time	t_F	—	15	25	ns	Test Figure 1-1
		—	**18**	**40**		
Delay Time	t_{D1}	—	37	50	ns	Test Figure 1-1
		—	**43**	**60**		
Delay Time	t_{D2}	—	40	60	ns	Test Figure 1-1
		—	**45**	**70**		

Note 1: Specification for packaged product only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $4.5V \le V_S \le 20V$; T_A = +25°C, **bold** values indicate full specified temperature range; unless noted. Input voltage slew rate >1V/µs; C_{OUT} = 1000pF. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply						
Power Supply Current	I_S	—	1.4	4.5	mA	$V_{INA} = V_{INB}$ 3.0V
		—	**1.5**	**8**		
Power Supply Current	I_S	—	0.18	0.4	mA	$V_{INA} = V_{INb}$ 0.0V
		—	**0.19**	**0.6**		

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+300	°C	10 sec.
Junction Operating Temperature Range	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance, 3x3 VDFN 8-Ld	θ_{JA}	—	60	—	°C/W	—
Thermal Resistance, EP MSOP 8-Ld	θ_{JA}	—	60	—	°C/W	—
Thermal Resistance, EP SOIC 8-Ld	θ_{JA}	—	58	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

Test Circuits

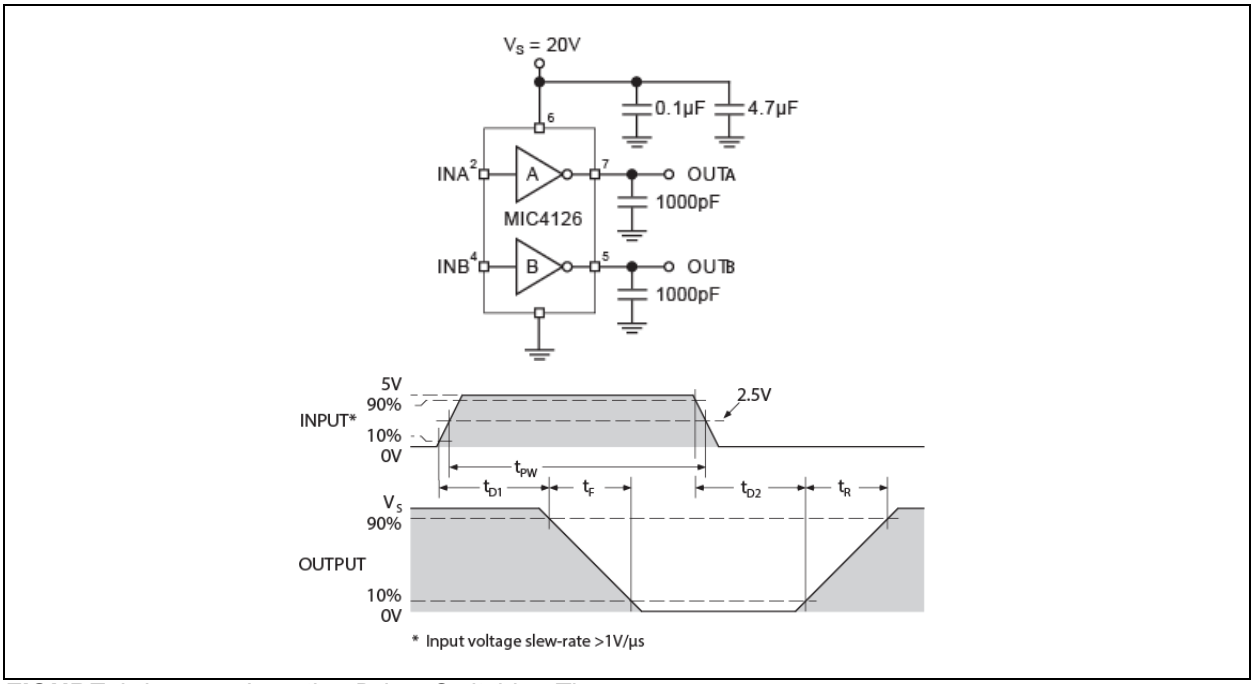


FIGURE 1-1: *Inverting Driver Switching Time.*

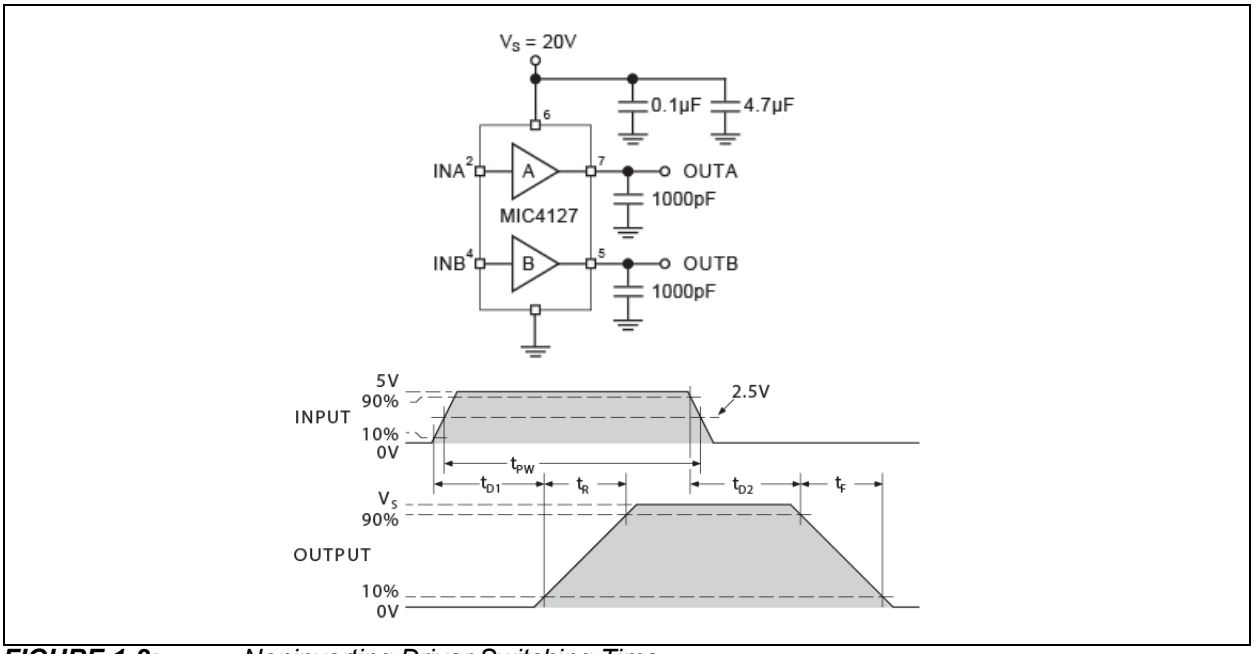


FIGURE 1-2: *Noninverting Driver Switching Time.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

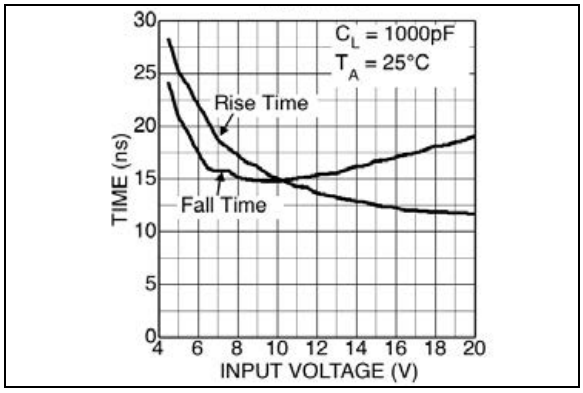


FIGURE 2-1: *Rise and Fall Time.*

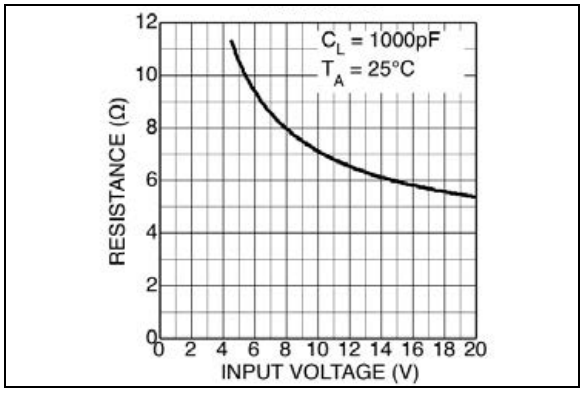


FIGURE 2-4: *MIC4126 Output Resistance.*

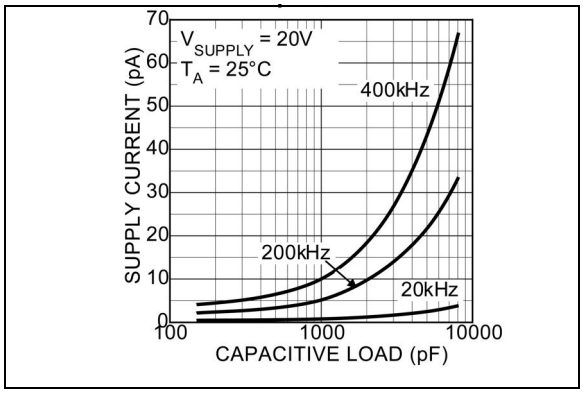


FIGURE 2-2: *MIC4127 Supply Current vs. Capacitive Load.*

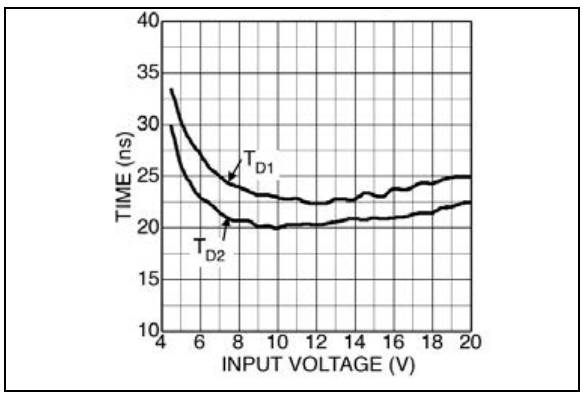


FIGURE 2-5: *Turn On and Turn Off Delay.*

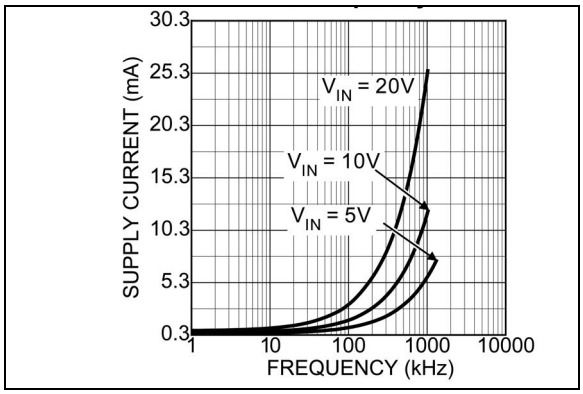


FIGURE 2-3: *Supply Current vs. Frequency.*

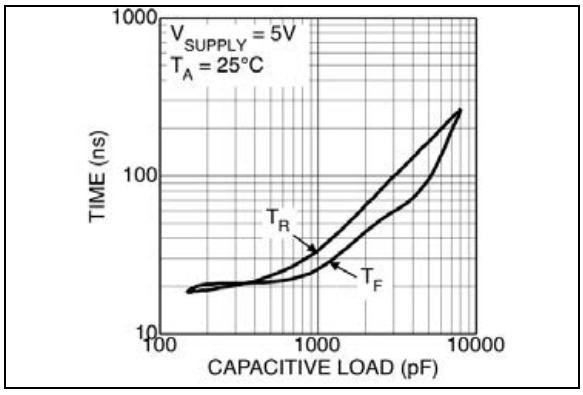


FIGURE 2-6: *Rise and Fall Time vs. Capacitive Load.*

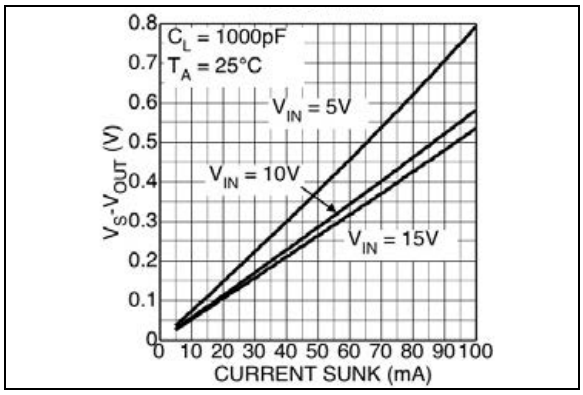


FIGURE 2-7: *Low Output vs. Current.*

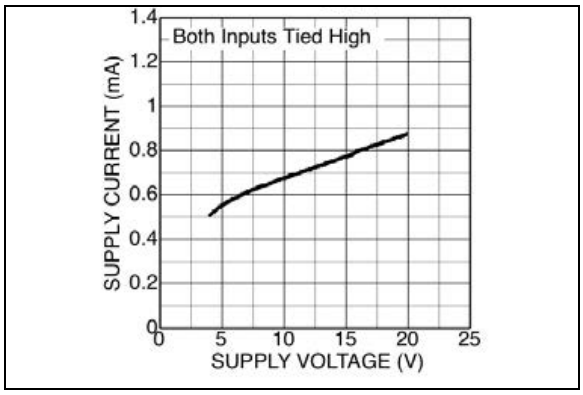


FIGURE 2-10: *Rise and Fall Time vs. Capacitive Load.*

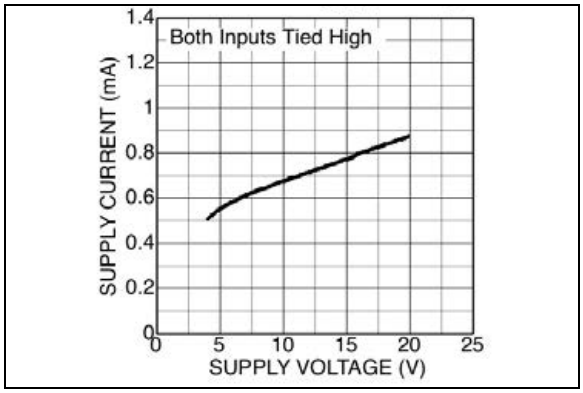


FIGURE 2-8: *Quiescent Power Supply Current vs. Supply Voltage.*

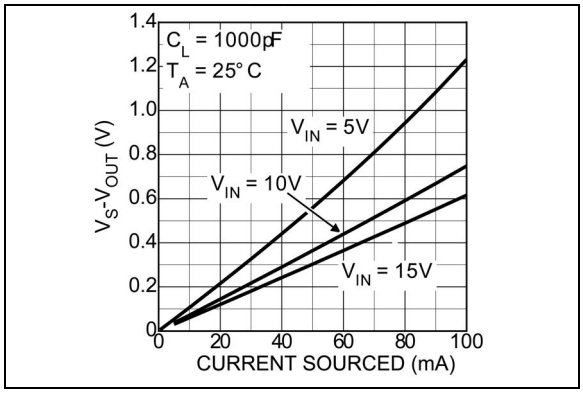


FIGURE 2-11: *High Output vs. Current.*

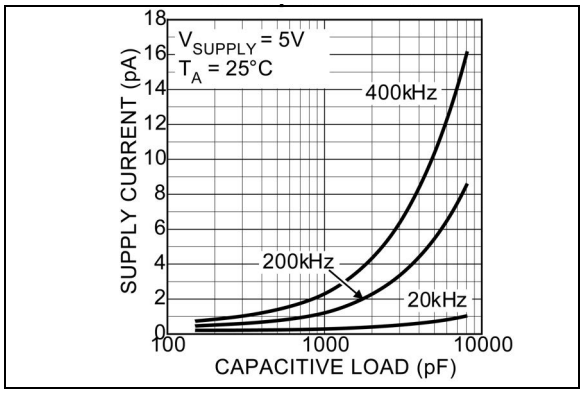


FIGURE 2-9: *MIC4127 Supply Current vs. Capacitive Load.*

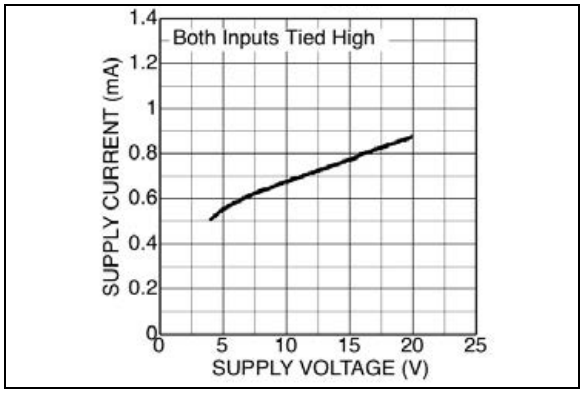


FIGURE 2-12: *Quiescent Power Supply Current vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 8	NC	Not internally connected
2	INA	Control Input A: TTL/CMOS compatible logic input
3	GND	Ground
4	INB	Control Input B: TTL/CMOS compatible logic input
5	OUTB	Output B: CMOS totem-pole output
6	V_S	Supply Input: +4.5V to +20V
7	OUTA	Output A: CMOS totem-pole output
EP	GND	Ground, backside pad

4.0 APPLICATION INFORMATION

Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000pF load by 16V in 25ns requires 0.8A from the supply input.

To ensure low supply impedance over a wide frequency range, parallel capacitors are recommended for power supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (< 0.5") should be used. A 1.0µF film capacitor in parallel with one or two 0.1µF ceramic MLC capacitors normally provides adequate bypassing.

Grounding

When using the inverting drivers in the MIC4126 or MIC4128, individual ground returns for the input and output circuits or a ground plane are recommended for optimum switching speed. The voltage drop that occurs between the driver's ground and the input signal ground, during normal high-current switching, will behave as negative feedback and degrade switching speed.

The E-pad and ML packages have an exposed pad under the package. It is important for good thermal performance that this pad is connected to a ground plane.

Control Input

Unused driver inputs must be connected to logic high (which can be V_S) or ground. For the lowest quiescent current (< 500µA), connect unused inputs-to-ground. A logic-high signal will cause the driver to draw up to 9mA.

The control input voltage threshold is approximately 1.5V. The control input recognizes 1.5V up to V_S as a logic high and draws less than 1µA within this range.

Power Dissipation

Power dissipation should be calculated to make sure that the driver is not operated beyond its thermal ratings. Quiescent power dissipation is negligible. A practical value for total power dissipation is the sum of the dissipation caused by the load and the transition power dissipation ($P_L + P_T$).

Load Dissipation

Power dissipation caused by continuous load current (when driving a resistive load) through the driver's output resistance is:

$P_L = I_{L^2} R_O$

For capacitive loads, the dissipation in the driver is:

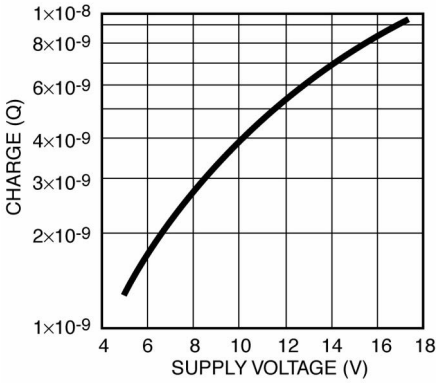
$P_L = f C_L V_{S^2}$

Transition Dissipation

In applications switching at a high frequency, transition power dissipation can be significant. This occurs during switching transitions when the P-channel and N-channel output FETs are both conducting for the brief moment when one is turning on and the other is turning off.

$P_T = 2 f V_S Q$

Charge (Q) is read from the following graph:

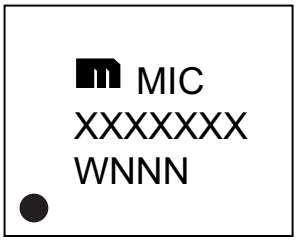


Crossover Energy Loss per Transition

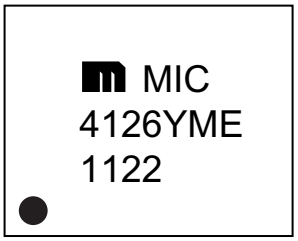
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

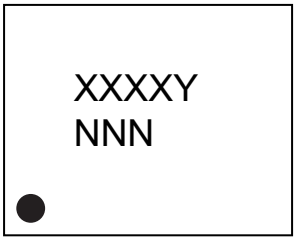
8-Lead SOIC*



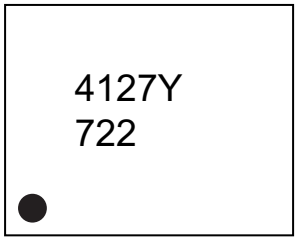
Example



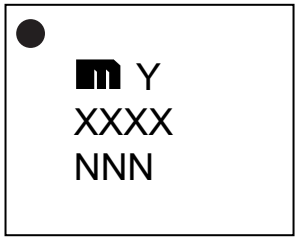
8-Lead MSOP*



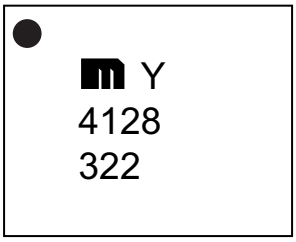
Example



8-Lead VDFN*



Example

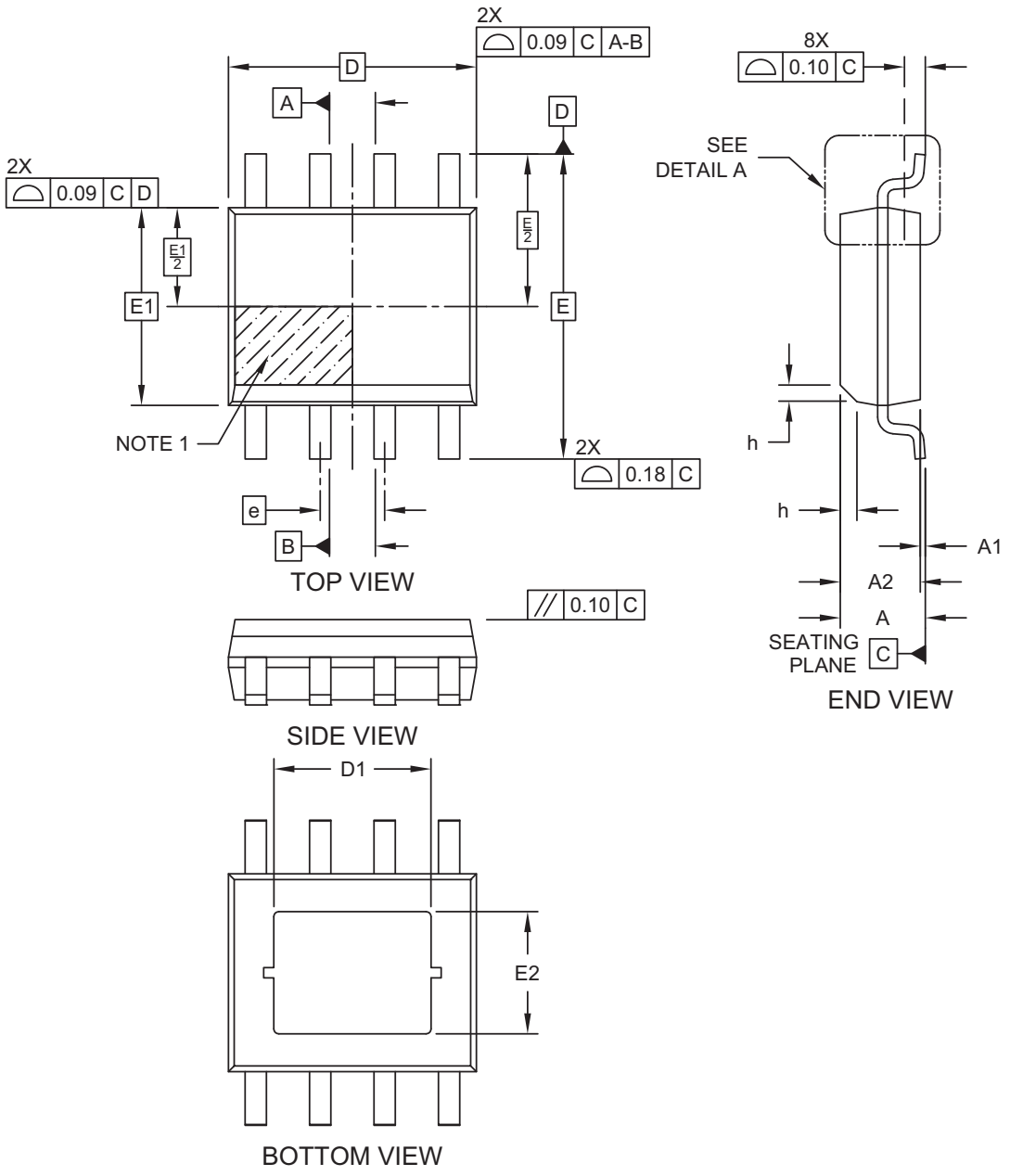


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

8-Lead SOICN ePad Package Outline and Recommended Land Pattern

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

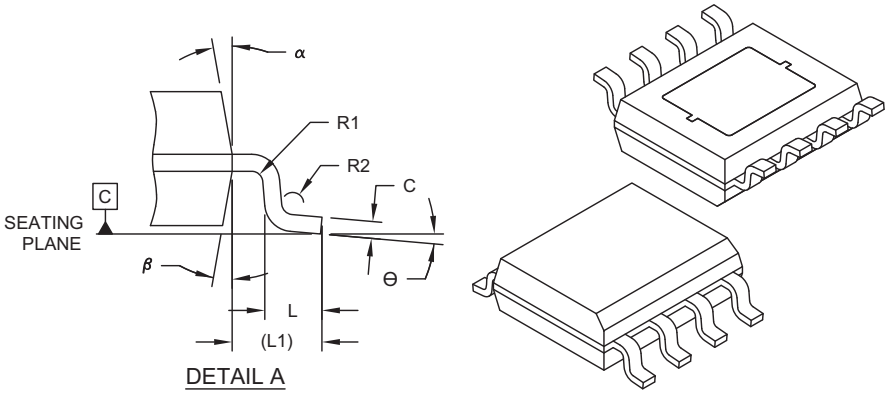
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1136 Rev A Sheet 1 of 2

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.43	1.55	1.68
Standoff	A1	0.00	0.05	0.10
Molded Package Thickness	A2	1.25	-	-
Overall Length	D		4.89 BSC	
Exposed Pad Length	D1	-	3.10	-
Overall Width	E		6.02 BSC	
Molded Package Width	E1		3.90 BSC	
Exposed Pad Width	E2	-	2.41	-
Terminal Width	b	0.35	0.41	0.49
Lead Thickness	c	0.19	0.20	0.25
Terminal Length	L	0.41	0.64	0.89
Terminal-to-Exposed-Pad	L1		1.04 REF	
Foot Angle	Θ	0°	5°	8°
Lead Bend Radius	R1	0.07	-	-
Terminal Length	R2	0.07	-	-
Mold Draft Angle	α	5°	-	15°
Mold Draft Angle	β	5°	-	15°

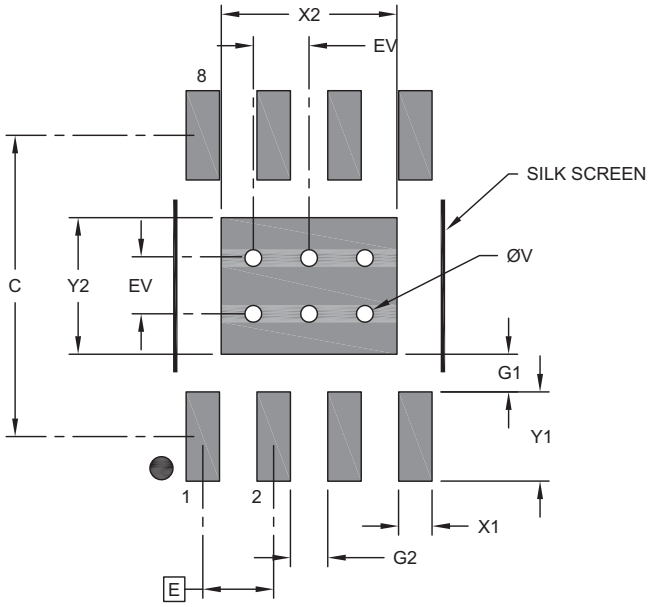
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1136 Rev A Sheet 2 of 2

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			3.15
Optional Center Pad Length	Y2			2.45
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.60
Contact Pad to Center Pad (X8)	G1	0.68		
Contact Pad to Contact Pad (X6)	G2	0.67		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

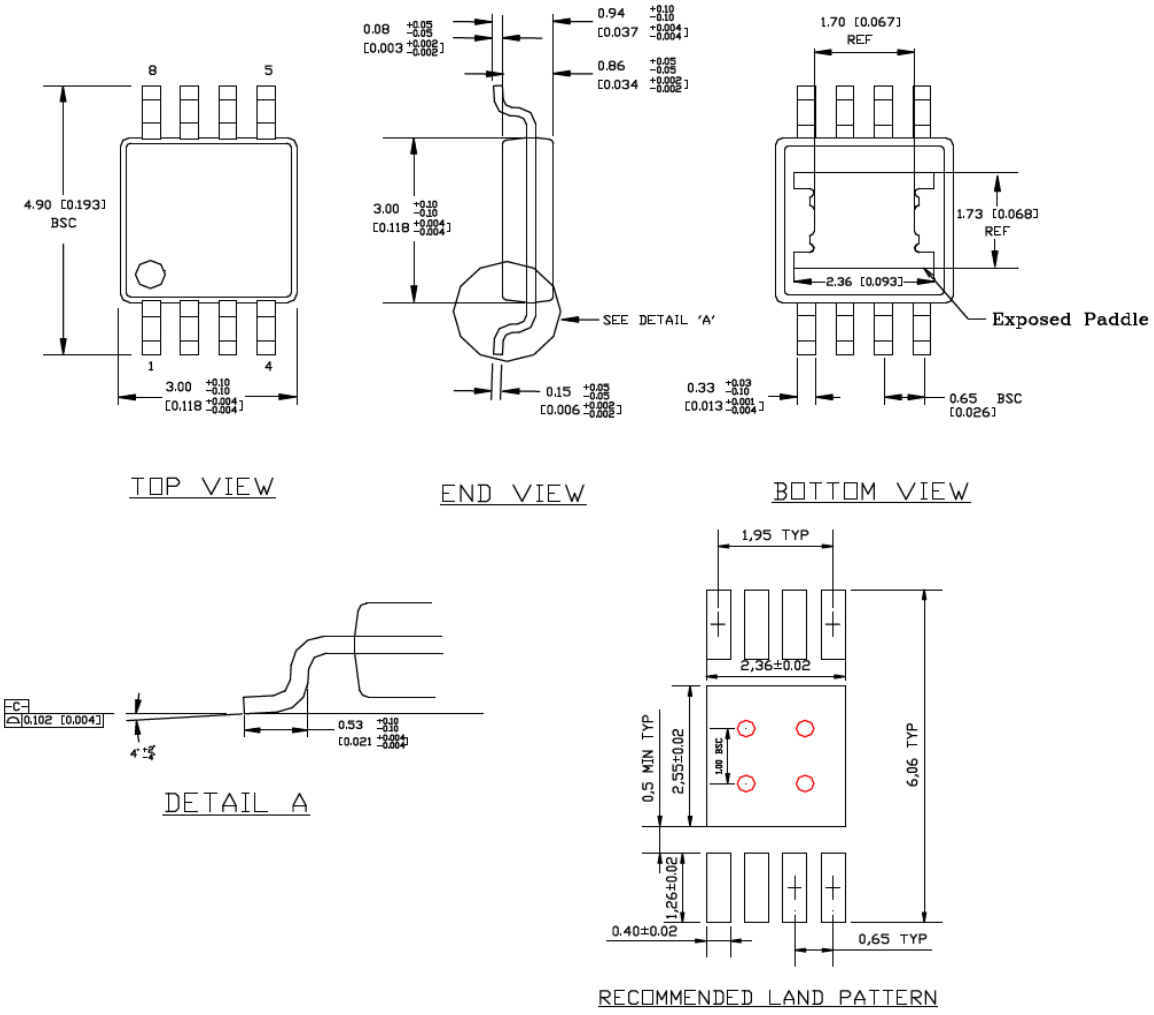
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-1136 Rev A

8-Lead MSOP ePad Package Outline and Recommended Land Pattern

DRAWING #	MSOPEP-8LD-PL-1	UNIT	MM [INCH]



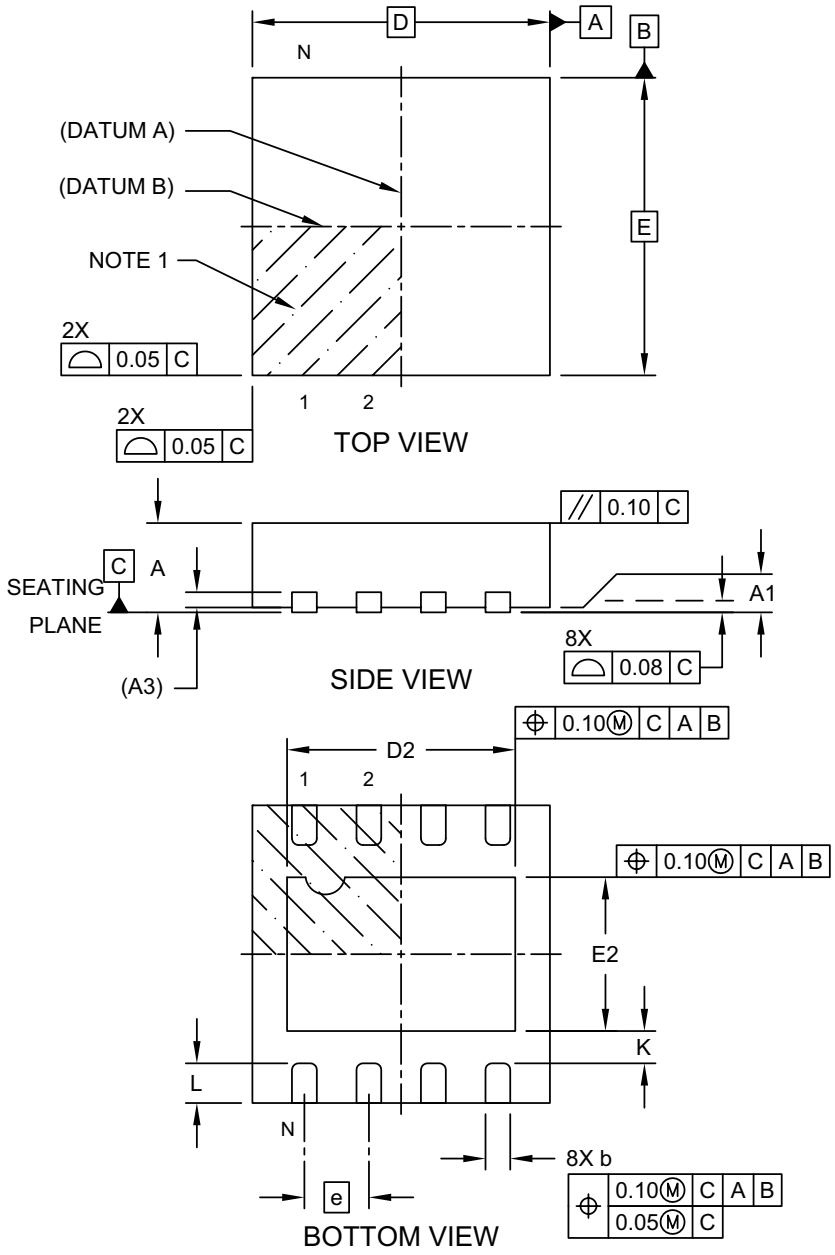
NOTE:
1. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE
2. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30–0.35MM IN DIAMETER, 1.00 PITCH AND SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead VDFN Package Outline and Recommended Land Pattern

8-Lead Very Thin Plastic Dual Flat, No Lead Package (JMA) - 3x3x0.9 mm Body [VDFN] Micrel Legacy Package DFN33-8LD-PL-1

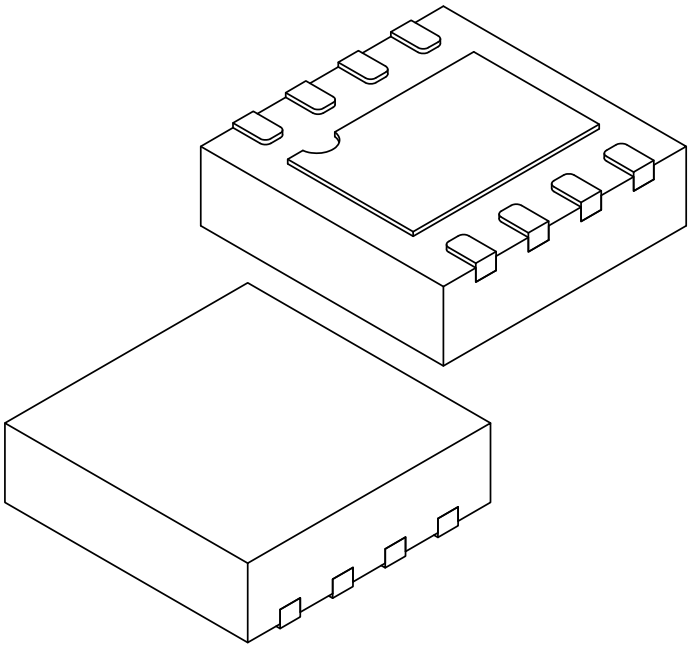
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1021 A Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (JMA) - 3x3x0.9 mm Body [VDFN]
Micrel Legacy Package DFN33-8LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.25	2.30	2.35
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

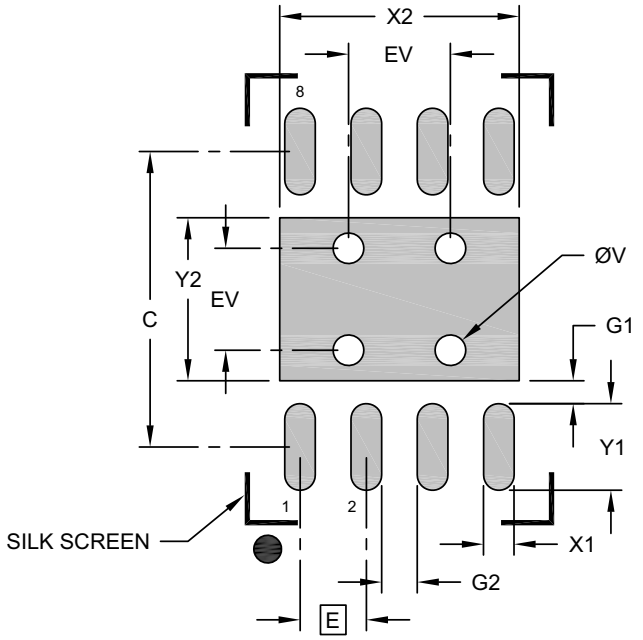
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1021 A Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (JMA) - 3x3x0.9 mm Body [VDFN]
Micrel Legacy Package DFN33-8LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			2.35
Optional Center Pad Length	Y2			1.60
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.23		
Contact Pad to Contact Pad (X6)	G2	0.35		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3021 Rev A

APPENDIX A: REVISION HISTORY

Revision A (June 2019)

- Converted Micrel document MIC4126/27/28 (M9999-072605) to Microchip data sheet template DS20006084A.
- Minor grammatical text changes throughout.
- Updated Packaging Information to MCHP standard versions.

Revision B (May 2022)

- Updated package marking drawing in **Section 5.1 "Package Marking Information"**.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	Dual 1.5A-Peak Low-Side MOSFET Driver in Advance Packaging Bipolar/CMOS/DMOS Process	
	MIC4126:	Dual Inverting
	MIC4127:	Dual Noninverting
	MIC4128:	Inverting and Noninverting
Junction Temperature Range:	Y =	–40°C to +125°C, RoHS Compliant
Package:	ME =	8-Lead ePad SOIC
	MME=	8-Lead ePad MSOP
	ML =	8-Lead VDFN
Media Type:	<blank>=	95/Tube (ME, ePad SOIC)
	<blank>=	100/Tube (MME, ePad MSOP)
	TR =	2,500/Reel (ME & MME, ePad SOIC)
	TR =	5,000/Reel (ML, VDFN)

Examples:

a) MIC4126:1.5A-Peak, Dual Inverting, Low-Side MOSFET Driver in Advanced Packaging, Extended Temperature Range, –40°C to +125°C, RoHS Compliant.

MIC4126YME	8-Lead ePad SOIC Package	95/Tube
MIC4126YME-TR	8-Lead ePad SOIC Package	2500/Reagingel
MIC4126YMME	8-Lead ePad MSOP Package	100/Tube
MIC4126YMME-TR	8-Lead ePad MSOP Package	2500/Reel
MIC4126YML-TR	8-Lead VDFN Package	5000/Reel

b) MIC4127:1.5A-Peak, Dual Noninverting, Low-Side MOSFET Driver in Advanced Packaging, Extended Temperature Range, –40°C to +125°C, RoHS Compliant.

MIC4127YME	8-Lead ePad SOIC Package	95/Tube
MIC4127YME-TR	8-Lead ePad SOIC Package	2500/Reagingel
MIC4127YMME	8-Lead ePad MSOP Package	100/Tube
MIC4127YMME-TR	8-Lead ePad MSOP Package	2500/Reel
MIC4127YML-TR	8-Lead VDFN Package	5000/Reel

c) MIC4128:1.5A-Peak, Inverting and Noninverting, Low-Side MOSFET Driver in Advanced Packaging, Extended Temperature Range, –40°C to +125°C, RoHS Compliant.

MIC4128YME	8-Lead ePad SOIC Package	95/Tube
MIC4128YME-TR	8-Lead ePad SOIC Package	2500/Reagingel
MIC4128YMME	8-Lead ePad MSOP Package	100/Tube
MIC4128YMME-TR	8-Lead ePad MSOP Package	2500/Reel
MIC4128YML-TR	8-Lead VDFN Package	5000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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