MIC33M650

6A, Pin Strapping Power Module with HyperLight Load® Mode and Output Voltage Select

Features

- 2.4V to 5.5V Input Voltage Range
- 6A Output Current
- Pin Strapping Voltage Selection:
  - Tri-state pins (nine voltage options)
  - 0.6V, 0.8V, 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V or 3.3V output voltage
- Reduced Component Count (No Feedback Resistors)
- High Efficiency (up to 95%)
- Output Discharge when Disabled
- Constant-On-Time (COT) Control with High Switching Frequency:
  - 1.2 MHz typical at 1.0V output voltage
- ±1.5% Output Voltage Accuracy Over Line/Load/Temperature Range
- 0.8 ms/V Soft Start Speed
- Supports Safe Start-up with Pre-Biased Output
- Typical 1.5 µA Shutdown Supply Current
- Low Dropout Operation (100% Duty Cycle)
- Ultra-Fast Transient Response
- Latch-Off Thermal Shutdown Protection
- Latch-Off Current Limit Protection
- Power Good (PG) Open-Drain Output
- Meets CISPR32 Class B Emissions
- Package: 53-Lead, 6 mm x 10 mm B1QFN

Applications

- Solid-State Drives (SSD)
- FPGAs, DSP and Low-Voltage ASIC Power

General Description

The MIC33M650 is a pin-selectable output voltage, high-efficiency, low-voltage input, 6A current, synchronous step-down regulator power module with integrated inductor. The COT control architecture with HyperLight Load® mode provides very high efficiency at light loads, while still having an ultra-fast transient response.

The MIC33M650 output voltage is set by two V_{SEL} (Voltage Selection) pins, between nine different values. This method eliminates the need for an external feedback resistor divider and improves the output voltage setting accuracy.

The 2.4V to 5.5V input voltage range, low shutdown and quiescent currents make the MIC33M650 ideal for single-cell Li-Ion battery-powered applications. The 100% duty cycle capability provides low dropout operation, extending operating range in portable systems.

The MIC33M650 pinout is compatible with the MIC33M656 I^2C-based programmable regulator version, such that applications can be easily converted. An open-drain PG output is provided to indicate when the output voltage is within 9% of regulation and facilitates the interface with an MCU or power sequencing. If set in shutdown (EN = GND), the MIC33M650 typically draws 1.5 µA, while the output is discharged through 10Ω pull-down.

The MIC33M650 is available in a thermally efficient, 53-Lead, 6 mm x 10 mm x 3 mm B1QFN package, with an operating junction temperature range from -40°C to +125°C.

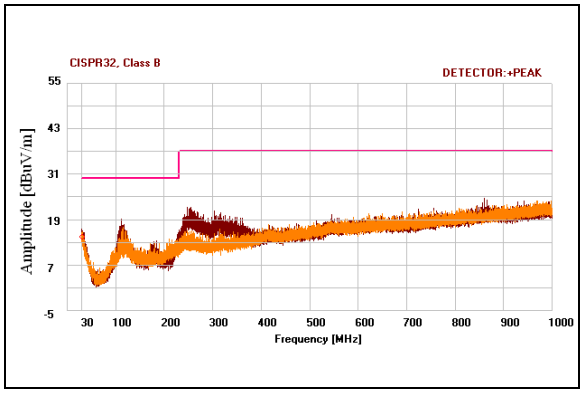

FIGURE 1: *Radiated Emissions, CISPR32, Class B (V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 6A).*

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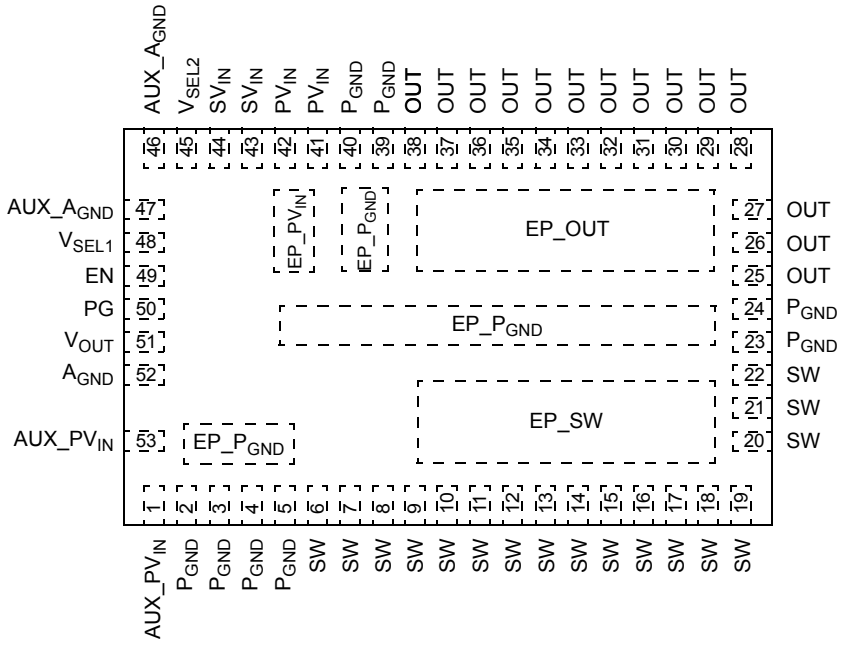
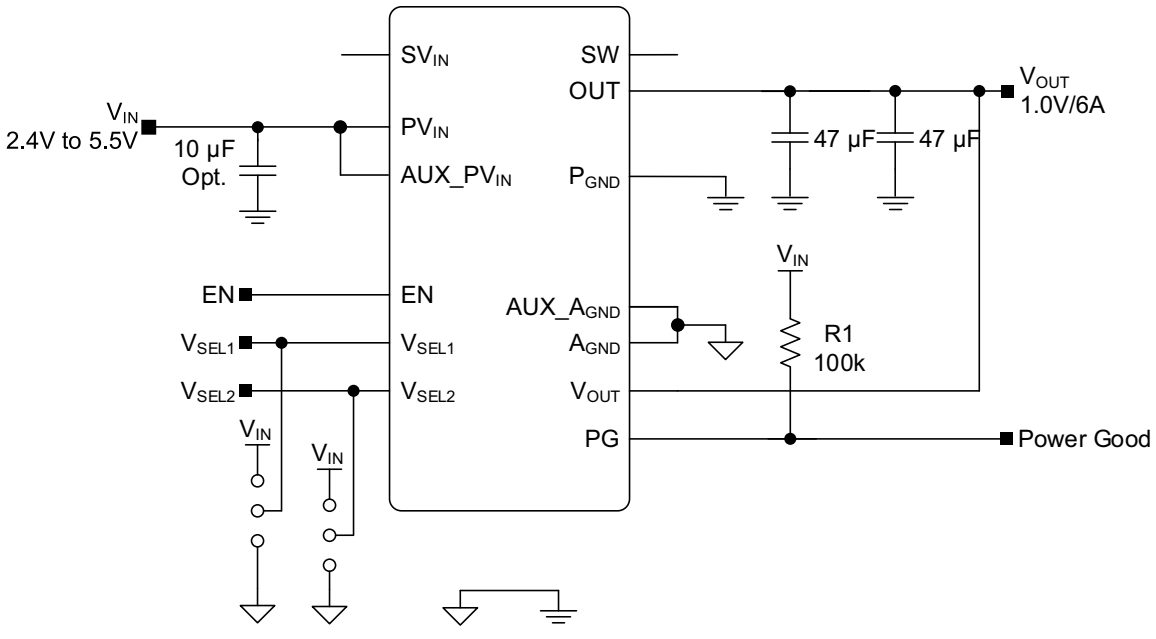
Package Type

MIC33M650
53-pin B1QFN 6 mm x 10 mm
(Top View)



* Includes Exposed Thermal Pads (EP); see Table 3-1.

Typical Application



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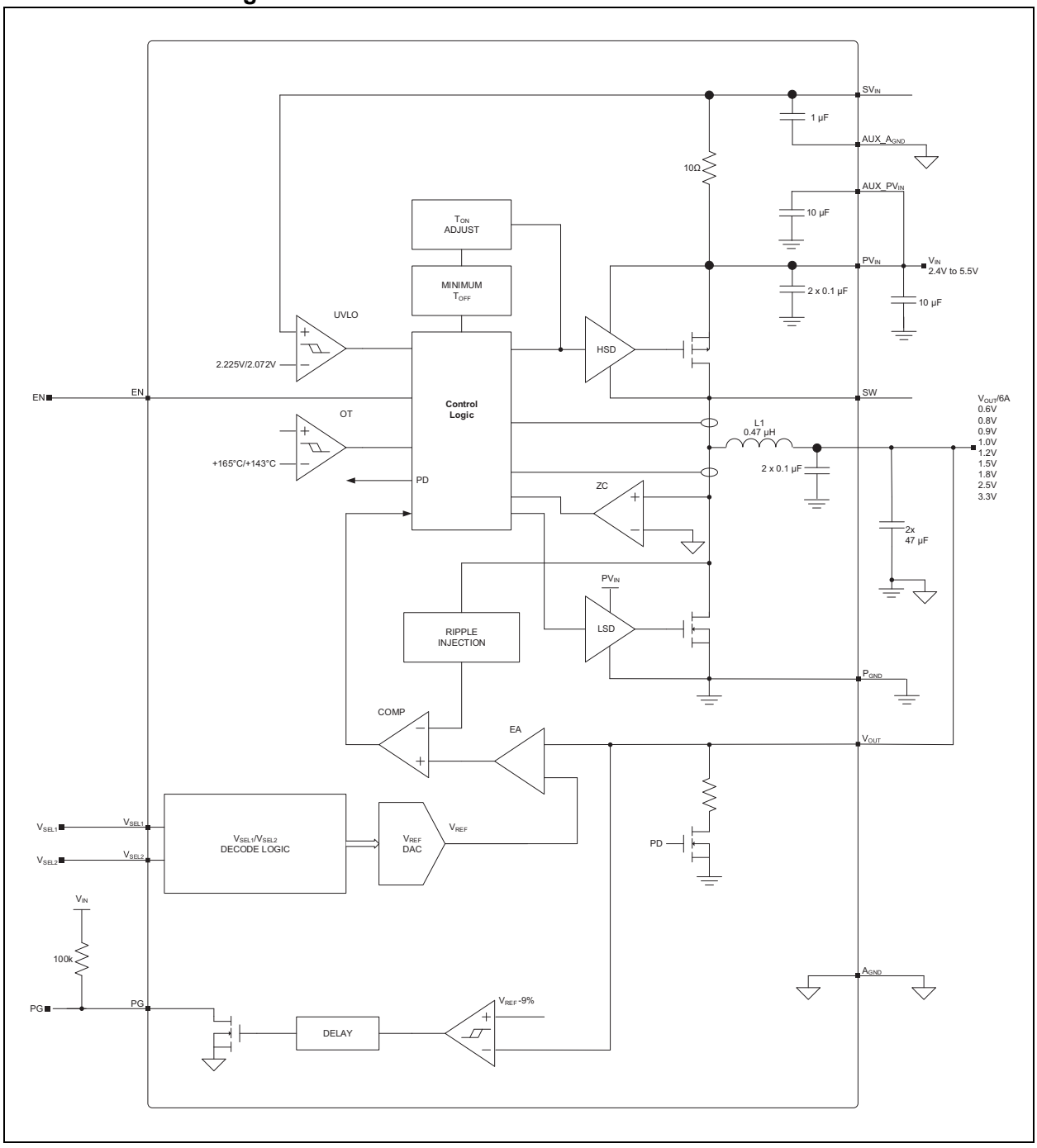
Functional Block Diagram



NOTES:

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

SV_{IN}, PV_{IN} to A_{GND} ..... -0.3V to +6V
V_{SW} to A_{GND} ..... -0.3V to +6V
V_{EN} to A_{GND} ..... -0.3V to PV_{IN}
V_{PG} to A_{GND} ..... -0.3V to PV_{IN}
V_{VSEL1}, V_{VSEL2} to A_{GND} ..... -0.3V to PV_{IN}
PV_{IN} to SV_{IN} ..... -0.3V to +0.3V
A_{GND} to P_{GND} ..... -0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +260°C
ESD Rating **(Note 1)**
HBM 2000V
CDM 1500V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD-sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings(1)

Supply Voltage (PV_{IN}) ..... 2.4V to 5.5V
Enable Voltage (V_{EN}) ..... 0V to PV_{IN}
Power-Good Pull-up Voltage (V_{PU_PG}) ..... 0V to 5.5V
AUX_PV_{IN} to PV_{IN} ..... 0V (shorted in operation)
AUX_A_{GND} to A_{GND} ..... 0V (shorted in operation)
Maximum Output Current 6A
Junction Temperature (T_J) ..... -40°C to +125°C

Note 1: The device is not ensured to function outside the operating range.

ELECTRICAL CHARACTERISTICS[1]

Electrical Specifications: Unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1V; C_{OUT} = 2 x 47 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{IN} Supply						
Input Range	PV_{IN}	**2.4**	—	**5.5**	V	
Undervoltage Lockout Threshold	UVLO	**2.15**	2.225	**2.35**	V	SV_{IN} rising
Undervoltage Lockout Hysteresis	UVLO_H	—	153	—	mV	SV_{IN} falling
Operating Supply Current	I_{IN0}	—	60	**100**	µA	V_{FB} = 1.2V, non-switching
Shutdown Current	I_{SHDN}	—	1.5	10	µA	V_{EN} = 0V, PV_{IN} = SV_{IN} = 5.5V, V_{SW} = V_{SEL1} = V_{SEL2} = 0V, -40°C ≤ T_J ≤ +105°C
		—		**20**	µA	V_{EN} = 0V, PV_{IN} = SV_{IN} = 5.5V, V_{SW} = V_{SEL1} = V_{SEL2} = 0V, -40°C ≤ T_J ≤ +125°C
Output Voltage vs. $V_{SEL1/2}$						
Output Accuracy	V_{OUT_ACC}	**0.5910**	0.6	**0.6090**	V	V_{SEL2} = 0, V_{SEL1} = 0
		0.7880	0.8	**0.8120**	V	V_{SEL2} = 0, V_{SEL1} = Z
		0.8865	0.9	**0.9135**	V	V_{SEL2} = 0, V_{SEL1} = 1
		0.9850	1.0	**1.0150**	V	V_{SEL2} = Z, V_{SEL1} = 0
		1.1820	1.2	**1.2180**	V	V_{SEL2} = Z, V_{SEL1} = Z
		1.4775	1.5	**1.5225**	V	V_{SEL2} = Z, V_{SEL1} = 1
		1.7730	1.8	**1.8270**	V	V_{SEL2} = 1, V_{SEL1} = 0
		2.4625	2.5	**2.5375**	V	V_{SEL2} = 1, V_{SEL1} = Z
		3.2505	3.3	**3.3495**	V	V_{SEL2} = 1, V_{SEL1} = 1
Line Regulation	—	—	0.06	—	%	V_{OUT} = 1.0V, V_{IN} = 2.5V to 5.5V, I_{OUT} = 300 mA
Load Regulation	—	—	0.1	—	%	V_{OUT} = 1.0V, I_{OUT} = 0A to 6A
Enable Control						
EN Logic Level High	V_{EN_H}	**1.2**	—	—	V	V_{EN} rising, regulator enabled
EN Logic Level Low	V_{EN_L}	—	—	**0.4**	V	V_{EN} falling, regulator shutdown
EN Low Input Current	I_{EN_L}	—	0.01	500	nA	V_{EN} = 0V
EN High Input Current	I_{EN_H}	—	0.01	500	nA	V_{EN} = 5.5V
Enable Lockout Delay	—	0.15	0.25	0.4	ms	
V_{SEL} Logic Level Control						
$V_{SEL1,2}$ Logic Level High	V_{SEL_H}	1.2	—	—	V	$V_{SEL1,2}$ rising, regulator enabled
$V_{SEL1,2}$ Logic Level Low	V_{SEL_L}	—	—	0.4	V	$V_{SEL1,2}$ falling, regulator shutdown
$V_{SEL1,2}$ Logic Level Open	V_{SEL_O}	—	0.8	—	V	$V_{SEL1,2}$ falling, regulator shutdown
$V_{SEL1,2}$ Low Input Current	I_{VSEL_L}	-1	0.01	1	µA	$V_{SEL1,2}$ = 0V
$V_{SEL1,2}$ High Input Current	I_{VSEL_H}	-1	0.01	1	µA	$V_{SEL1,2}$ = 5.5V

Note 1: Specification for packaged product only.

2: Tested in open loop. The closed-loop current limit is affected by the inductance value.

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ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Specifications: Unless otherwise specified, PV_{IN} = 5V; V_{OUT} = 1V; C_{OUT} = 2 x 47 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
T_{ON} Control/Switching Frequency						
Switching On Time	T_{ON}	—	180	—	ns	V_{IN} = 5V, V_{OUT} = 1V
Switching Frequency	FREQ	—	1.2	—	MHz	V_{OUT} = 1.0V, I_{OUT} = 3A, L = 0.47 µH
		—	1.1	—		V_{OUT} = 3.3V, I_{OUT} = 3A, L = 0.47 µH
Maximum Duty Cycle	DCMAX		—	**100**	%	
Short-Circuit Protection						
High-Side MOSFET Forward Current Limit	I_{LIM_HS}	8	10	12	A	**Note 2**
Low-Side MOSFET Forward Current Limit	I_{LIM_LS}	—	8	—	A	**Note 2**
Low-Side MOSFET Negative Current Limit	I_{LIM_NEG}	-2	-3	-4	A	**Note 2**
N-Channel Zero-Crossing Threshold	I_{ZC_TH}	—	0.9	—	A	
Current Limit Events before Hiccup	HICCUP	—	8	—	Cycles	
Hiccup Period before Restart	—	—	1	—	ms	
Internal MOSFETs						
High-Side On-Resistance	$R_{DS-ON-HS}$	—	30	60	mΩ	I_{SW} = 1A
Low-Side On-Resistance	$R_{DS-ON-LS}$	—	16	40	mΩ	I_{SW} = -1A
Output Discharge Resistance	$R_{DS-ON-DSC}$	—	10	**50**	Ω	V_{EN} = 0V, V_{SW} = 5.5V, from V_{OUT} to P_{GND}
SW Leakage Current	I_{LEAK_SW}	—	1	**10**	µA	PV_{IN} = 5.5V, V_{SW} = 0V, V_{EN} = 0V
Power Good						
PG Threshold	PG_TH	87	91	95	$\%V_{OUT}$	V_{OUT} Rising (Good)
PG Hysteresis	PG_HYS	—	4	—	$\%V_{OUT}$	V_{FB} = V_{REF}, V_{PG} = 5.5V
PG Blanking Time	PG_BLANK	—	65	—	µs	
PG Output Leakage Current	PG_LEAK	—	30	300	nA	
PG Sink Low Voltage	PG_SINKV	—	—	200	mV	V_{FB} = 0V, V_{PG} = 5.5V, I_{PG} = 10 mA
Thermal Shutdown						
Thermal Shutdown	T_{SHDN}	—	+165	—	°C	T_J rising
Thermal Shutdown Hysteresis	T_{SHDN_HYST}	—	+22	—	°C	T_J falling
Thermal Latch-Off Soft Start Cycles	TH_LATCH	—	4	—	Cycles	

Note 1: Specification for packaged product only.

2: Tested in open loop. The closed-loop current limit is affected by the inductance value.

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TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, SV_{IN} = PV_{IN} = 5V; V_{OUT} = 1V; C_{OUT} = 2 x 47 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 53-Lead, 6 mm x 10 mm x 3 mm B1QFN	θ_{JA}	—	+31	—	°C/W	

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2.0 TYPICAL CHARACTERISTIC CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $SV_{IN} = PV_{IN} = 5V$; $V_{OUT} = 1V$; $C_{OUT} = 2 \times 47\ \mu F$; $T_A = +25°C$.

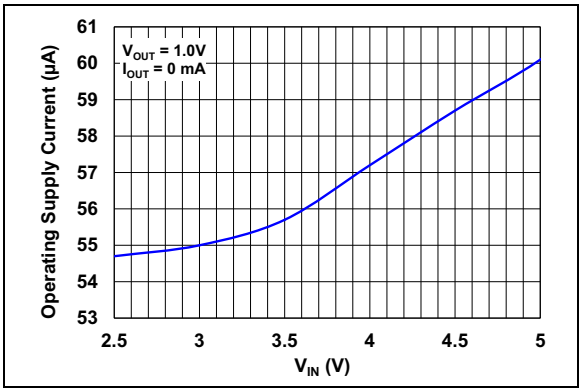

FIGURE 2-1: *Operating Supply Current vs. Input Voltage, Switching.*

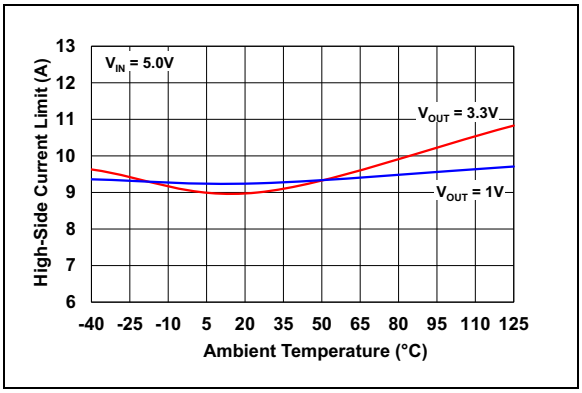

FIGURE 2-2: *High-Side Current Limit vs. Temperature (closed loop).*

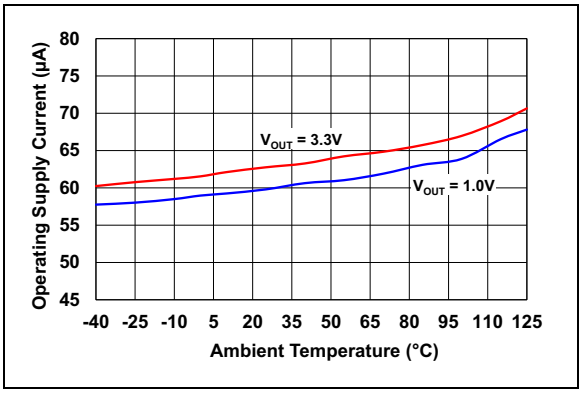

FIGURE 2-3: *Operating Supply Current vs. Temperature, Switching.*

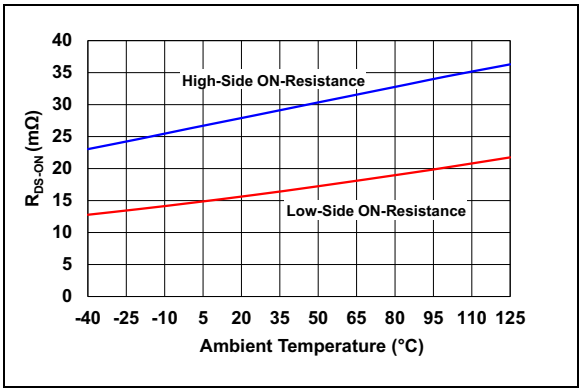

FIGURE 2-4: *R_{DS-ON} vs. Temperature.*

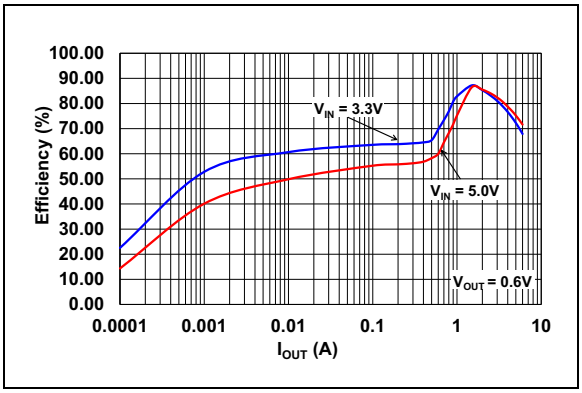

FIGURE 2-5: *Efficiency vs. Load Current.*

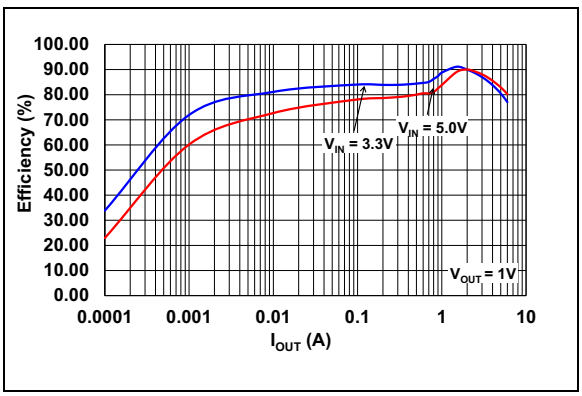

FIGURE 2-6: *Efficiency vs. Load Current.*

Note: Unless otherwise indicated, $SV_{IN} = PV_{IN} = 5V$; $V_{OUT} = 1V$; $C_{OUT} = 2 \times 47\ \mu F$; $T_A = +25°C$.

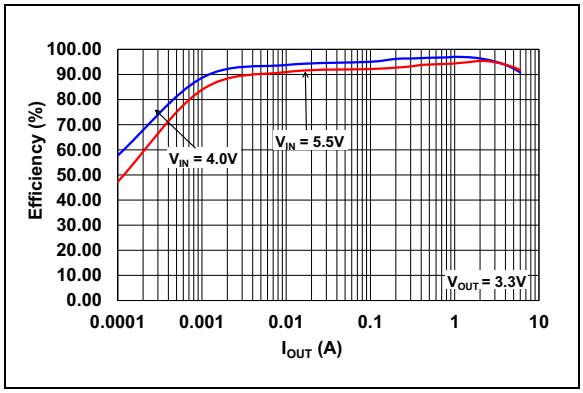

FIGURE 2-7: *Efficiency vs. Load Current.*

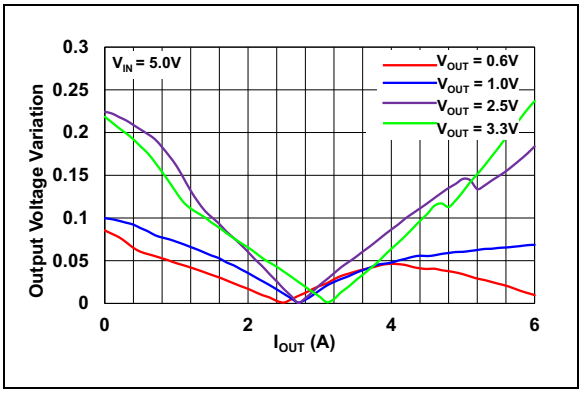

FIGURE 2-10: *Load Regulation: Output Voltage Variation vs. I_{OUT}.*

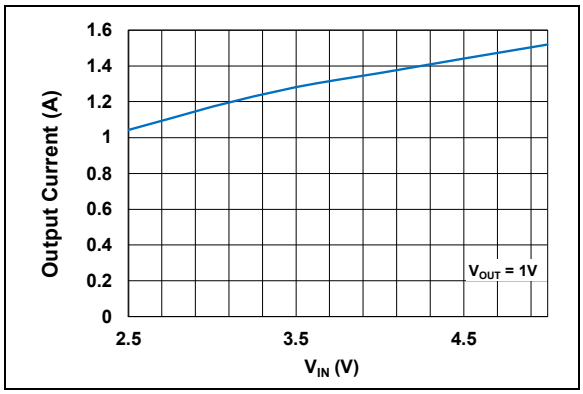

FIGURE 2-8: *DCM/FPWM I_{OUT} Threshold vs. V_{IN}.*

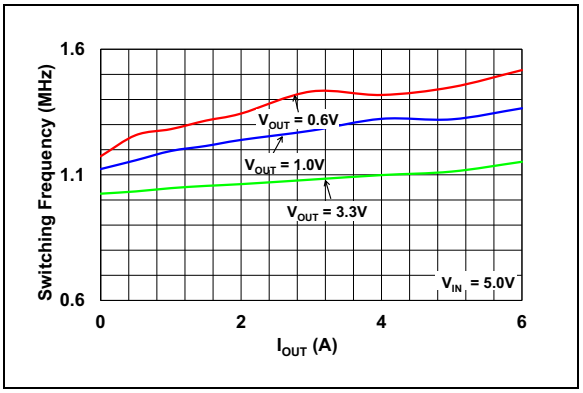

FIGURE 2-11: *Switching Frequency vs. Output Current.*

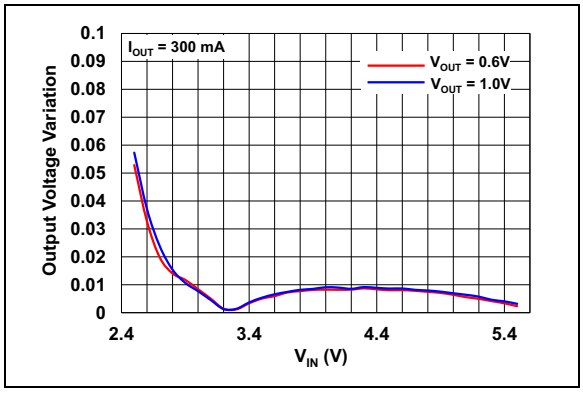

FIGURE 2-9: *Line Regulation: Output Voltage Variation vs. Input Voltage.*

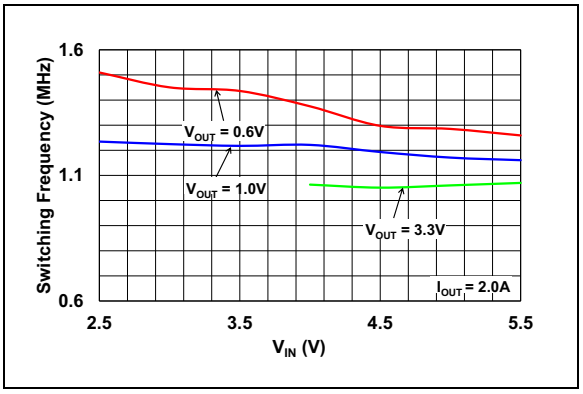

FIGURE 2-12: *Switching Frequency vs. Input Voltage.*

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Note: Unless otherwise indicated, $SV_{IN} = PV_{IN} = 5V$; $V_{OUT} = 1V$; $C_{OUT} = 2 \times 47\ \mu F$; $T_A = +25°C$.

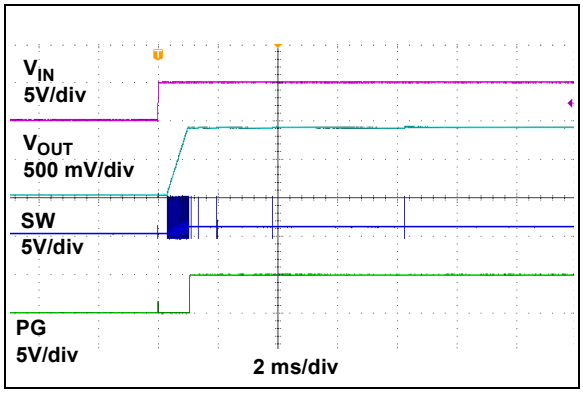

FIGURE 2-13: *V_{IN} Turn-On (EN = PV_{IN}).*

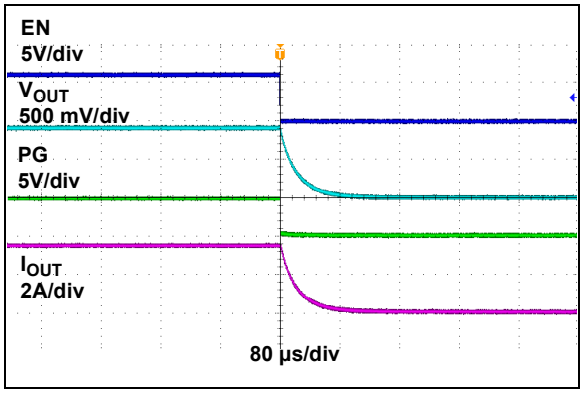

FIGURE 2-16: *EN Turn-Off, $R_{LOAD} = 0.3\Omega$.*

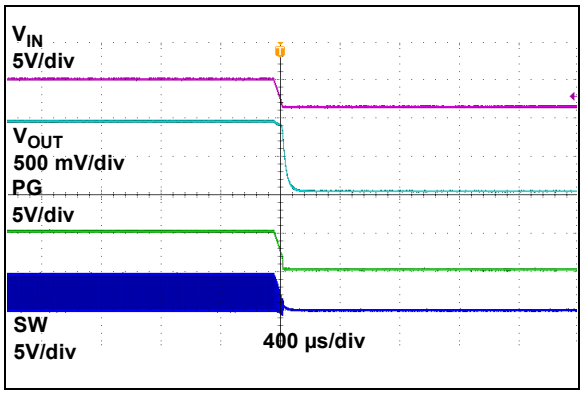

FIGURE 2-14: *V_{IN} Turn-Off (EN = PV_{IN}), $R_{LOAD} = 0.3\Omega$.*

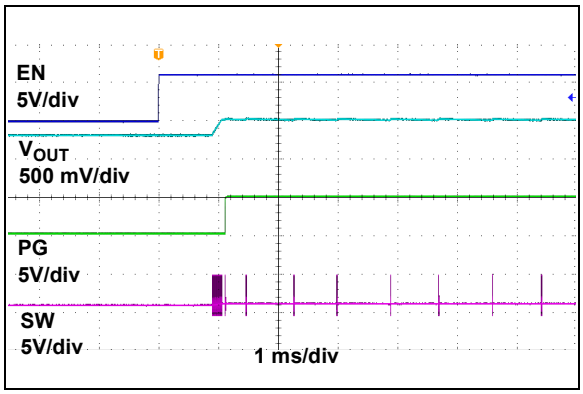

FIGURE 2-17: *EN Turn-On into Pre-Biased Output ($V_{pre\text{-}bias} = 0.8V$).*

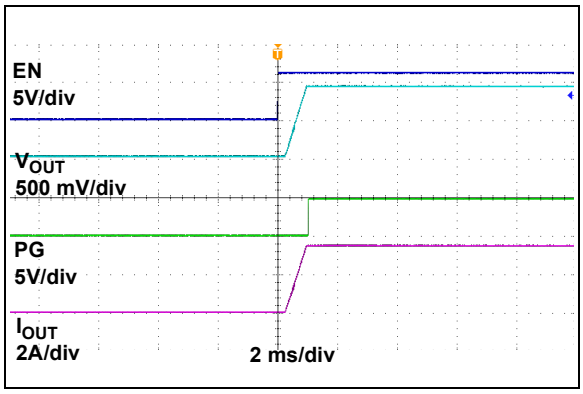

FIGURE 2-15: *EN Turn-On, $R_{LOAD} = 0.3\Omega$.*

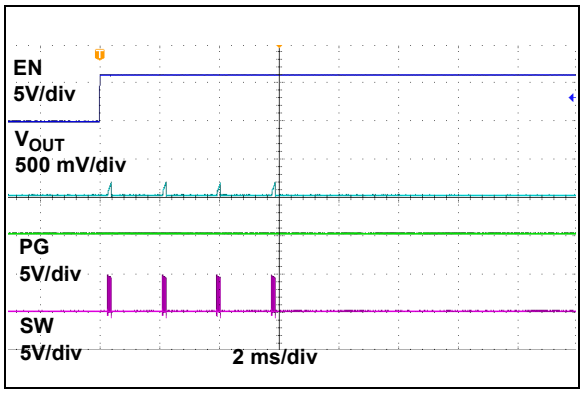

FIGURE 2-18: *Power-up into Short-Circuit.*

Note: Unless otherwise indicated, SV_{IN} = PV_{IN} = 5V; V_{OUT} = 1V; C_{OUT} = 2 x 47 µF; T_A = +25°C.

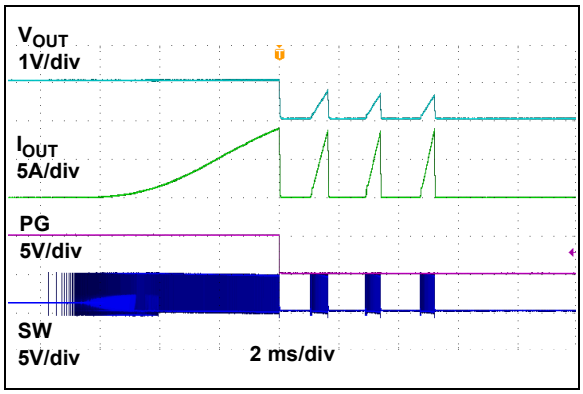

FIGURE 2-19: *Output Current Limit Threshold.*

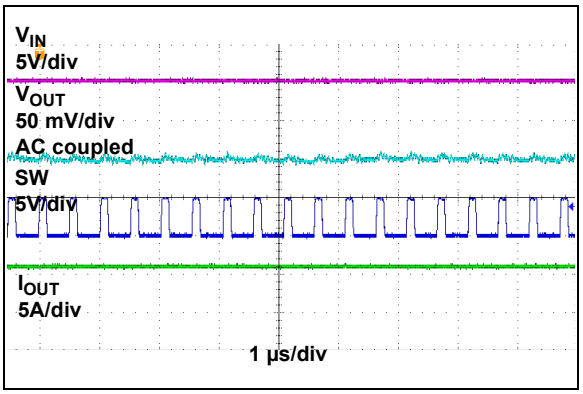

FIGURE 2-22: *Switching Waveforms, I_{OUT} = 6A.*

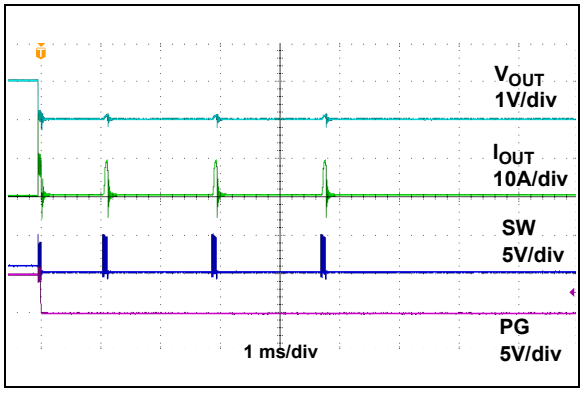

FIGURE 2-20: *Hiccup Mode Short-Circuit Current Limit Response.*

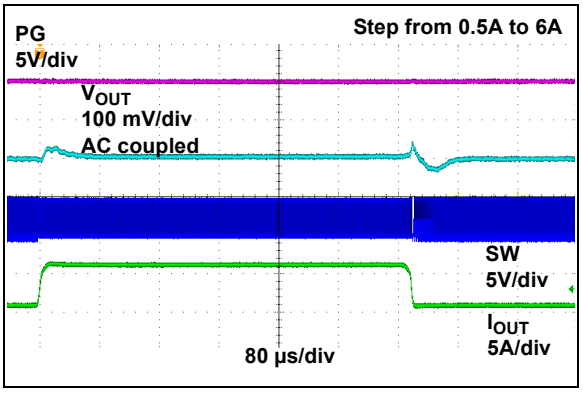

FIGURE 2-23: *Load Transient Response.*

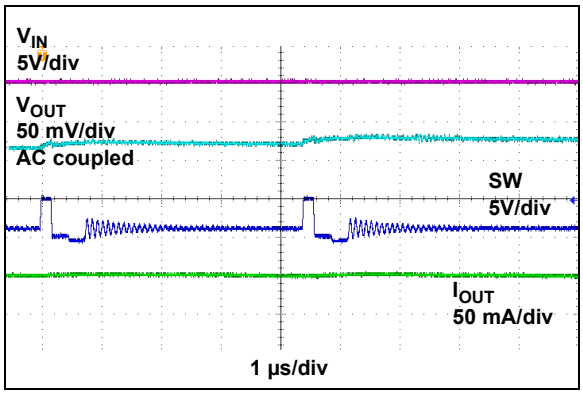

FIGURE 2-21: *Switching Waveforms, I_{OUT} = 50 mA.*

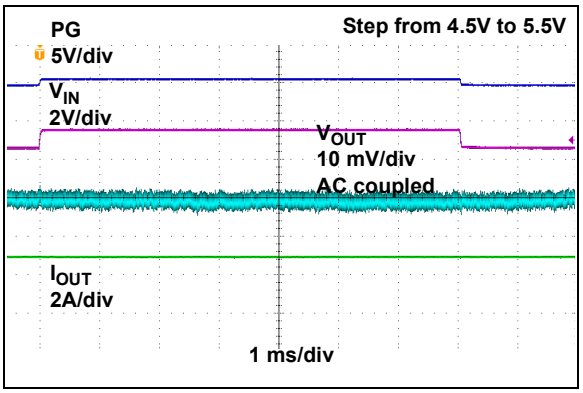

FIGURE 2-24: *Line Transient Response.*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
2, 3, 4, 5, 23, 24, 39, 40	P_{GND}	Power Ground. P_{GND} is the ground path for the MIC33M650 power module.
1, 53	AUX_PV_{IN}	Auxiliary Power Input Voltage Pin. Connect externally to PV_{IN}.
6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22	SW	Switch Node Pin. SW connects to the internal MOSFETs and inductor. Do not connect any external load to this point.
41, 42	PV_{IN}	Power Supply Voltage Pin.
25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38	OUT	Output Side Connection Pin.
43, 44	SV_{IN}	Analog Voltage Input Pin. SV_{IN} is the power to the internal reference and control sections of the MIC33M650. Internally connected to PV_{IN} through a 10W resistor.
46, 47	AUX_A_{GND}	Auxiliary Analog Ground Pin. Connect externally to A_{GND}.
45	V_{SEL2}	Output Voltage Selection Control 2 (Input) Pin. The logic state of V_{SEL1} and V_{SEL2} selects the output voltage. This input has three digital states: High, Low and Floating.
48	V_{SEL1}	Output Voltage Selection Control 1 (Input) Pin. The logic state of V_{SEL1} and V_{SEL2} selects the output voltage. This input has three digital states: High, Low and Floating.
49	EN	Enable (Input) Pin. Logic high enables the operation of the regulator. The EN pin should not be left floating.
50	PG	Power Good (Output) Pin. This is an open-drain output that indicates when the output voltage is higher than the 91% limit.
51	V_{OUT}	Output Voltage Sense (Input) Pin. This pin is used to remote sense the output voltage. Connect V_{OUT} as close to the output capacitor as possible to sense the output voltage.
52	A_{GND}	Analog Ground Pin. A_{GND} is the internal signal ground for all low-power circuits.
54	EP_OUT	Exposed Thermal Pad. Internally connected to OUT.
55	EP_SW	Exposed Thermal Pad. Internally connected to SW.
56	EP_P_{GND}	Exposed Thermal Pad. Internally connected to P_{GND}.
57	EP_PV_{IN}	Exposed Thermal Pad. Internally connected to PV_{IN}.

3.1 Power Ground Pin (P_{GND})

P_{GND} is the ground path for the MIC33M650 buck converter power stage. The P_{GND} pin connects to the sources of the low-side N-Channel MOSFETs, the negative terminals of input capacitors and the negative terminals of output capacitors. The loop for the Power Ground must be as small as possible and separate from the Analog Ground (A_{GND}) loop.

3.2 Switch Node Pin (SW)

Switching node output pin which connects to the internal MOSFETs and inductor. This is a high-frequency connection; therefore, traces should be kept as short and as wide as practical.

3.3 Power Supply Voltage Pin (PV_{IN})

Input supply to the source of the internal high-side P-channel MOSFET. The PV_{IN} operating voltage range is from 2.4V to 5.5V. An input capacitor between PV_{IN} and the P_{GND} pin is required and placed as close to the IC as possible.

3.4 Output Side Connection Pins (OUT)

Output side connection of the internal inductor. The output capacitors must be connected from this pin group to GND, as close to the module as possible.

3.5 Analog Voltage Input Pin (SV_{IN})

This pin is the power to the internal reference and control sections of the MIC33M650. It is internally connected to PV_{IN} through a 10Ω resistor.

3.6 Output Voltage Selection Control Pins (V_{SEL1}, V_{SEL2})

Output Voltage Selection Control (Input). The logic state of V_{SEL1} and V_{SEL2} selects the output voltage. This input has three digital states: High, Low and Floating. See Table 4-1.

3.7 Enable Pin (EN)

Logic high enables the regulator's operation. Logic low shuts down the device. In the OFF state, the supply current of the device is greatly reduced (typically, 1.5 µA). The EN pin should not be left open.

3.8 Power Good Pin (PG)

This is an open-drain output that indicates when the output voltage is higher than the 91% limit. There is a 4% hysteresis; therefore, PG will return low when the output voltage falls below 87% of the target regulation voltage.

3.9 Output Voltage Sense Pin (V_{OUT})

This pin is used to remote sense the output voltage. Connect to V_{OUT} as close to the output capacitor as possible to sense the output voltage. It also provides the path to discharge the output through an internal 10Ω resistor when the device is disabled.

3.10 Analog Ground Pin (A_{GND})

Internal signal ground for all low-power circuits. Connect to ground plane. For best load regulation, the connection path from A_{GND} to the output capacitor ground terminal must be free from parasitic voltage drops.

3.11 Auxiliary Analog Ground Pins (AUX_A_{GND})

Connect these pins to A_{GND} to make use of the internal decoupling capacitor for SV_{IN} pin filtering.

3.12 Auxiliary Input Voltage Pins (AUX_PV_{IN})

Connect these pins to PV_{IN} to make use of the internal 10 µF capacitor for PV_{IN} filtering/decoupling.

3.13 OUT Exposed Pad (EP_OUT)

It is electrically connected to the OUT pins. It must be externally connected to the output power connection.

3.14 SW Exposed Pad (EP_SW)

It is electrically connected to the SW node.

3.15 P_{GND} Exposed Pad (EP_P_{GND})

It is electrically connected to the P_{GND} pins. It must be connected with thermal vias to the ground plane to ensure adequate heat sinking.

3.16 PV_{IN} Exposed Pad (EP_PV_{IN})

It is electrically connected to the PV_{IN} pins. It must be connected to the input power connection.

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4.0 FUNCTIONAL DESCRIPTION

4.1 Device Overview

The MIC33M650 is a high-efficiency, 6A peak current, synchronous buck regulator power module with HyperLight Load mode. The module integrates the inductor, alongside with high-frequency ripple dampening capacitors, on the input and output of the converter and decoupling capacitor for the signal input. The COT control architecture with automatic HyperLight Load mode provides very high efficiency at light loads and ultra-fast transient response.

The MIC33M650 output voltage is set by two V_{SEL} tri-state logic pins that can set the output voltage to nine different values. See Table 4-1.

The 2.4V to 5.5V input voltage operating range makes the device ideal for single-cell Li-Ion battery-powered applications. The 100% duty cycle capability provides low dropout operation, extending battery life in portable systems. The automatic HyperLight Load mode provides very high efficiency at light loads.

This device focuses on high output voltage accuracy. Total output error is less than 1.5% over line, load and temperature.

The MIC33M650 buck regulator uses an adaptive COT control method. The adaptive on-time control scheme is employed to obtain a nearly constant switching frequency in Continuous Conduction mode. Overcurrent protection is implemented by sensing the current on both the low-side and high-side internal power MOSFETs. The device includes an internal soft start function, which reduces the power supply input surge current at start-up, by controlling the output voltage rise time.

4.2 HyperLight Load Mode (HLL)

HLL is a power-saving mode. In HLL, the switching frequency is not constant over the operation current range, but its average value reduces proportionally to the load current. This reduces switching and drive losses and maintains high efficiency as the load current decreases.

4.3 Enable (EN)

When the EN pin is pulled low, the IC is in a Shutdown state, with all internal circuits disabled with the PG output low. During shutdown, the part typically consumes 1.5 µA. When the EN pin is pulled HIGH, the start-up sequence is initiated.

4.4 Power Good (PG)

The PG output is generally used for power sequencing where the Power Good output is tied to the enable output of another regulator. This technique avoids all the regulators powering up at the same time, causing large inrush current.

The PG output is an open-drain output. During start-up, when the output voltage rises, the PG output goes high by means of an external pull-up resistor when the output voltage reaches 91% of its set value. The PG threshold has 4% hysteresis, so the PG output stays high until the output voltage falls below 87% of the set value. A built-in 65 µs blanking time is incorporated to prevent nuisance tripping.

The pull-up resistor can be connected to V_{IN}, V_{OUT} or an external source that is less than or equal to V_{IN}. The PG pin can be connected to another regulator's enable pin for output sequencing. The PG output is deasserted as soon as the enable pin is pulled low, or an input undervoltage condition or any other Fault is detected.

4.5 Resistive Discharge (Soft Discharge)

To ensure a known output condition when the device is turned off and then back on, the output is actively discharged to ground by means of an internal 10Ω resistor. This prevents the load from powering up starting from an undefined condition.

4.6 Output Voltage Setting

The MIC33M650 V_{SEL1} and V_{SEL2} pins are used to choose among nine predefined voltage settings: 0.6V, 0.8V, 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V. These pins can be tied to V_{IN}, GND or left floating. The relationship between V_{SEL1}/V_{SEL2} and the output voltage is shown in Table 4-1.

TABLE 4-1: OUTPUT VOLTAGE SETTINGS

V_{SEL2}	V_{SEL1}	V_{OUT}
GND	GND	0.6V
GND	OPEN	0.8V
GND	V_{IN}	0.9V
OPEN	GND	1.0V
OPEN	OPEN	1.2V
OPEN	V_{IN}	1.5V
V_{IN}	GND	1.8V
V_{IN}	OPEN	2.5V
V_{IN}	V_{IN}	3.3V

The output voltage sensing pin, V_{OUT}, must be connected to the desired Point-of-Load (POL) regulation, avoiding parasitic resistive drops. It is possible to fine-tune the desired output voltage by adding a series resistor on the V_{OUT} pin. This allows slightly higher output value programming, but should not exceed 5% deviation from the V_{SEL} selected value.

EQUATION 4-1:

$$R_{VOUT} = 8.2\ k\Omega \times TRIM$$

Where:

R_{VOUT} = V_{OUT} series resistance needed for a TRIM% output voltage increase

4.7 Converter Stability, Output Capacitor

The MIC33M650 utilizes an internal compensation network and it is designed to provide stable operation with output capacitors from 47 µF to 1000 µF. This greatly simplifies the design, where the user can add supplementary output capacitance without having to worry about stability.

4.8 Soft Start

Excess bulk capacitance on the output can cause excessive input inrush current. The MIC33M650 internal soft start feature forces the output voltage to rise gradually, keeping the inrush current at reasonable levels. This is particularly important in battery-powered applications. When the EN pin goes high, the output voltage starts to rise. Once the soft start period finishes, the PG comparator is enabled, and if the output voltage is above 91% of the nominal regulation voltage, then the PG output goes high.

The output voltage Soft Start Time, t_{SS}, is determined by the soft start equation below. The Soft Start Time can be calculated by:

EQUATION 4-2:

$$t_{SS} = V_{OUT} \times t_{RAMP}$$

$$t_{SS} = 1.0V \times 800\ \mu s/V$$

$$t_{SS} = 800\ \mu s = 0.8\ ms$$

Where:

V_{OUT} = 1.0V

t_{RAMP} = 800 µs/V

4.9 Dropout Operation

As the input voltage approaches the output voltage, the minimum on-time limits the maximum duty cycle. To achieve a 100% duty cycle, the high-side switch is latched on when the duty cycle reaches around 92% and stays latched until the output voltage falls 4% below its regulated value. In dropout, the output voltage is determined by the input voltage minus the voltage drop across the high-side MOSFET.

4.10 Switching Frequency

The switching frequency of the MIC33M650 is determined by the internal On-Time (T_{ON}) calculation. For an input voltage of 5V and an output voltage of 1V, the typical value of T_{ON} is 180 ns.

The resulting switching frequency can be estimated by the following equation:

EQUATION 4-3:

$$f_{SW} = V_{OUT} / (V_{IN} \times T_{ON})$$

The above equation is only valid in Continuous Conduction mode and for a lossless converter. In practice, losses will cause an increase of the switching frequency with respect to the ideal case. As the load current increases, losses increase too and so does the switching frequency.

The on-time calculation is adaptive, in that the T_{ON} value is modulated based on the input voltage and on the target output voltage to stabilize the switching frequency against their variations. Losses are not accounted for.

TABLE 4-2: T_{ON} FOR TYPICAL APPLICATIONS

V_{IN} (V)	V_{OUT} (V)	T_{ON}
5	0.6	110
	1	180
	1.8	340
	2.5	490
	3.3	610
3.3	1	270

4.11 Undervoltage Protection (UVLO)

Undervoltage protection ensures that the IC has enough voltage to bias the internal circuitry properly and provide sufficient gate drive for the power MOSFETs. When the input voltage starts to rise, both power MOSFETs are off and the PG output is pulled low. The IC starts at typically 2.225V and has a typical 153 mV of hysteresis to prevent chattering between the UVLO High and Low states.

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4.12 Overtemperature Fault

The MIC33M650 monitors the die junction temperature to keep the IC operating properly. If the IC junction temperature exceeds +165°C, both power MOSFETs are immediately turned off. The IC is allowed to restart when the die temperature falls below +143°C.

During recovery from a thermal shutdown event, if the regulator hits another thermal shutdown event before PG can be achieved, the controller resets again. If this happens four times in a row, the part will be in a Latch-Off state and the MOSFETs are permanently latched off. The MIC33M650 will not restart unless the input power is cycled or the EN pin is set low and then high again. This latch-off feature eliminates the thermal stress on the MIC33M650 during a persistent Fault event.

4.13 Safe Start-up into a Pre-Biased Output

The MIC33M650 is designed for safe start-up into a pre-biased output. This feature prevents high negative inductor current flow in a pre-bias condition which can damage the IC. This is achieved by not allowing PWM operation until the control loop commands eight switching cycles. After eight cycles, the low-side negative current limit is switched from 0A to -3A. The cycle counter is reset to zero if the EN pin is pulled low, or an input undervoltage condition or any other Fault is detected.

4.14 Current Limiting

The MIC33M650 regulator uses both high-side and low-side current sense for current limiting. When the high-side current sense threshold is reached, the high-side MOSFET is turned off and the low-side MOSFET is turned on. The low-side MOSFET stays on until the current falls to 80% of the high-side current threshold value, then the high side can be turned on again. If the overload condition lasts for more than seven cycles, the MIC33M650 enters hiccup current limiting and both MOSFETs are turned off. There is a cool-off period before the MOSFETs are allowed to be turned on. If the regulator has another hiccup event before it reaches the PG threshold on restart, it will turn off both MOSFETs and wait for the cool-off period. If this happens for more than three times in a row, then the part enters the Latch-Off state, which will permanently turn off both MOSFETs until the part is reset by cycling input power or by toggling the enable input.

4.15 Thermal Considerations

Although the MIC33M650 is capable of delivering up to 6A under load, the package thermal resistance and the device internal power dissipation may dictate some limitations to the continuous output current.

As a reference, for V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 5A, the evaluation board application shows a stable +40°C chip package self-heating (DT100107).

For V_{IN} = 5V, V_{OUT} = 3.3V, the same self-heating is produced at about 4A.

If operated above the rated junction temperature, electrical parameters may drift beyond characterized specifications. The MIC33M650 is protected under all circumstances by thermal shutdown.

NOTES:

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5.0 APPLICATION INFORMATION

5.1 Output Voltage Sensing

To achieve accurate output voltage regulation, the V_{OUT} pin (internal feedback divider top terminal) should be Kelvin connected as close as possible to the point of regulation top terminal. Since both the internal reference and the internal feedback divider's bottom terminal refer to A_{GND}, it is important to minimize voltage drops between A_{GND} and the point of regulation return terminal (typically the ground terminal of the output capacitor which is closest to the load).

EQUATION 5-1:

$$P_{WINDING(HT)} = R_{WINDING(20C)} \times (1 + 0.0042 \times (T_H - T_{20C}))$$

Where:

T_H = Temperature of Wire Under Full Load

T_{20C} = Ambient Temperature

$R_{WINDING(20C)}$ = Room Temperature Winding Resistance (usually specified by the manufacturer)

5.2 Output Capacitor Selection

The type of output capacitor is usually determined by its Equivalent Series Resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, OS-CON and POSCAP. The output capacitor ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated using Equation 5-2.

EQUATION 5-2:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-Peak Output Voltage Ripple

$\Delta I_{L(PP)}$ = Peak-to-Peak Inductor Current Ripple

The peak-to-peak inductor current ripple can be calculated with the following formula:

EQUATION 5-3:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

Where:

L = 0.47 µH

The total output ripple is a combination of the ESR and the output capacitance.The total ripple is calculated in Equation 5-4.

EQUATION 5-4:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{COUT}\right)^2}$$

Where:

C_{OUT} = Output Capacitance Value

f_{SW} = Switching Frequency

The output capacitor RMS current is calculated in Equation 5-5.

EQUATION 5-5:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-6:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

5.3 Input Capacitor

The MIC33M650 integrates high-frequency input bypass capacitors, connected between PV_{IN} and P_{GND}, and an additional 10 µF, low-ESR ceramic capacitor for input ripple smoothing, connected between P_{GND} and AUX_PV_{IN}. Therefore, the connection between PV_{IN} and AUX_PV_{IN} should have very low stray resistance and inductance (i.e., many vias) to take advantage of the internal 10 µF capacitor. While the internal 10 µF capacitor can support the RMS ripple current, additional external input ceramic capacitors can be optionally added to further attenuate the input voltage ripple amplitude. The need for additional external input capacitance also depends on the impedance of the input supply distribution network.

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NOTES:

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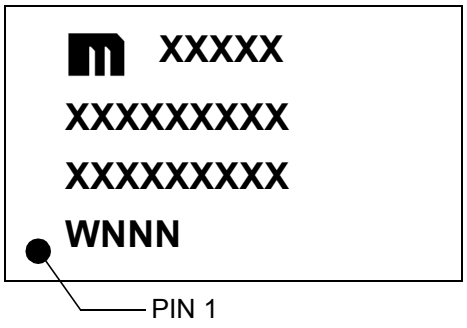
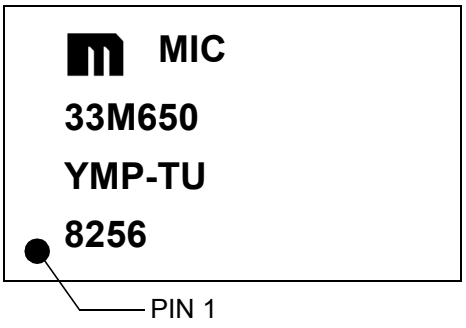
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

53-Lead B1QFN



Example:

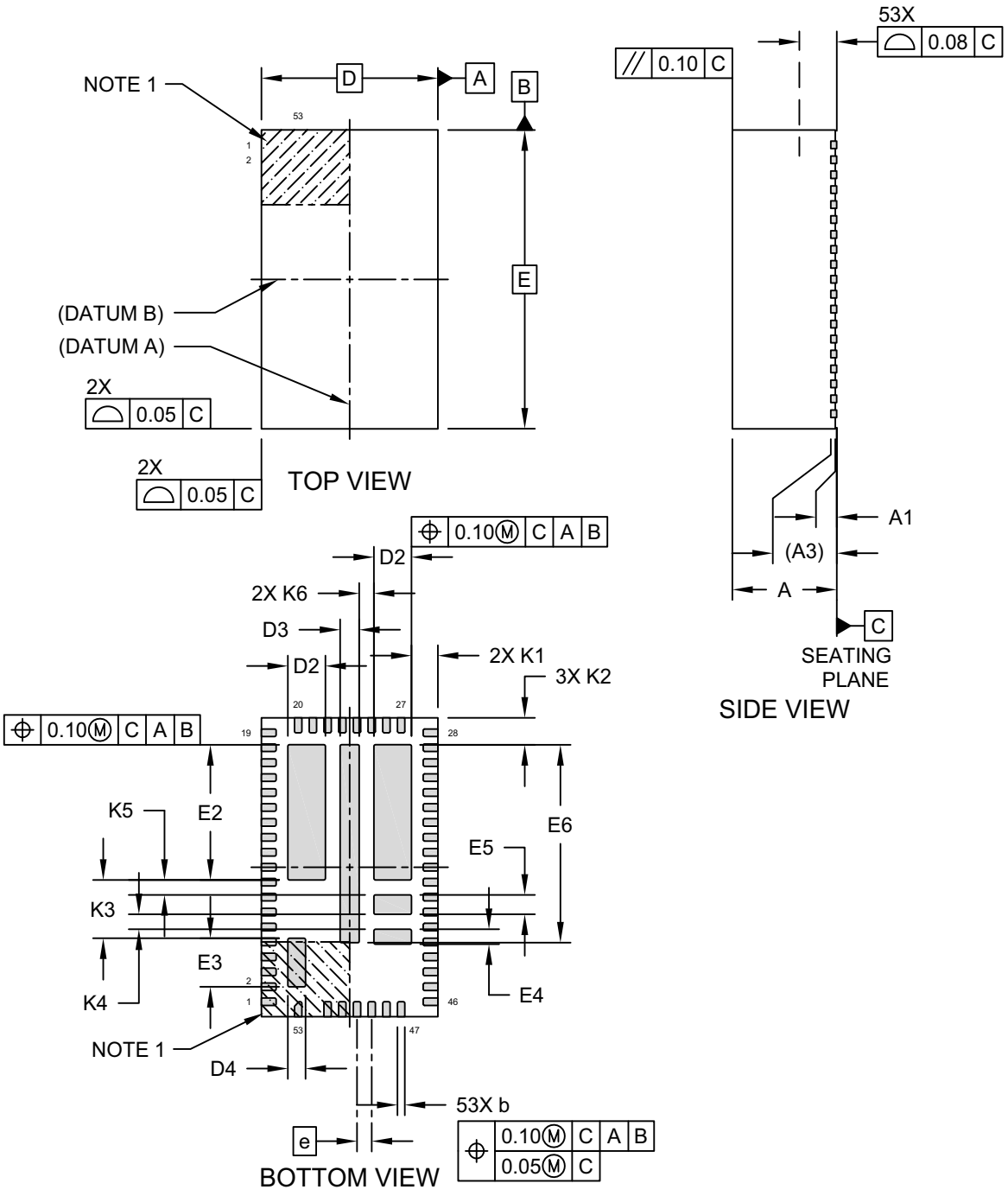


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

53-Lead Very Thick Plastic Quad Flat, No Lead Package (QDA) - 6x10x3.05 mm Body [B1QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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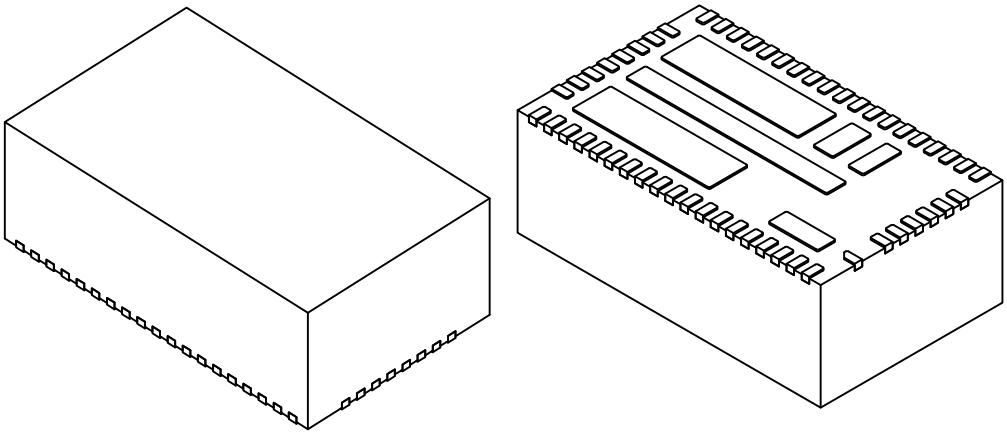

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		53	
Pitch	e		0.50 BSC	
Overall Height	A	2.95	3.00	3.05
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	1.225	1.275	1.325
Exposed Pad Length	D3	0.60	0.65	0.70
Exposed Pad Length	D4	0.55	0.60	0.65
Overall Width	E		10.00 BSC	
Exposed Pad Width	E2	4.475	4.525	4.575
Exposed Pad Width	E3	1.575	1.625	1.675
Exposed Pad Width	E4	0.45	0.50	0.55
Exposed Pad Width	E5	0.60	0.65	0.70
Exposed Pad Width	E6	6.573	6.623	6.673
Package Edge to Exposed Pad	K1	0.85	0.90	0.95
Package Edge to Exposed Pad	K2	0.85	0.90	0.95
Exposed Pad to Exposed Pad	K3	1.90	1.95	2.00
Exposed Pad to Exposed Pad	K4	0.45	0.50	0.55
Exposed Pad to Exposed Pad	K5	0.45	0.50	0.55
Exposed Pad to Exposed Pad	K6	0.45	0.50	0.55
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.45	0.50	0.55

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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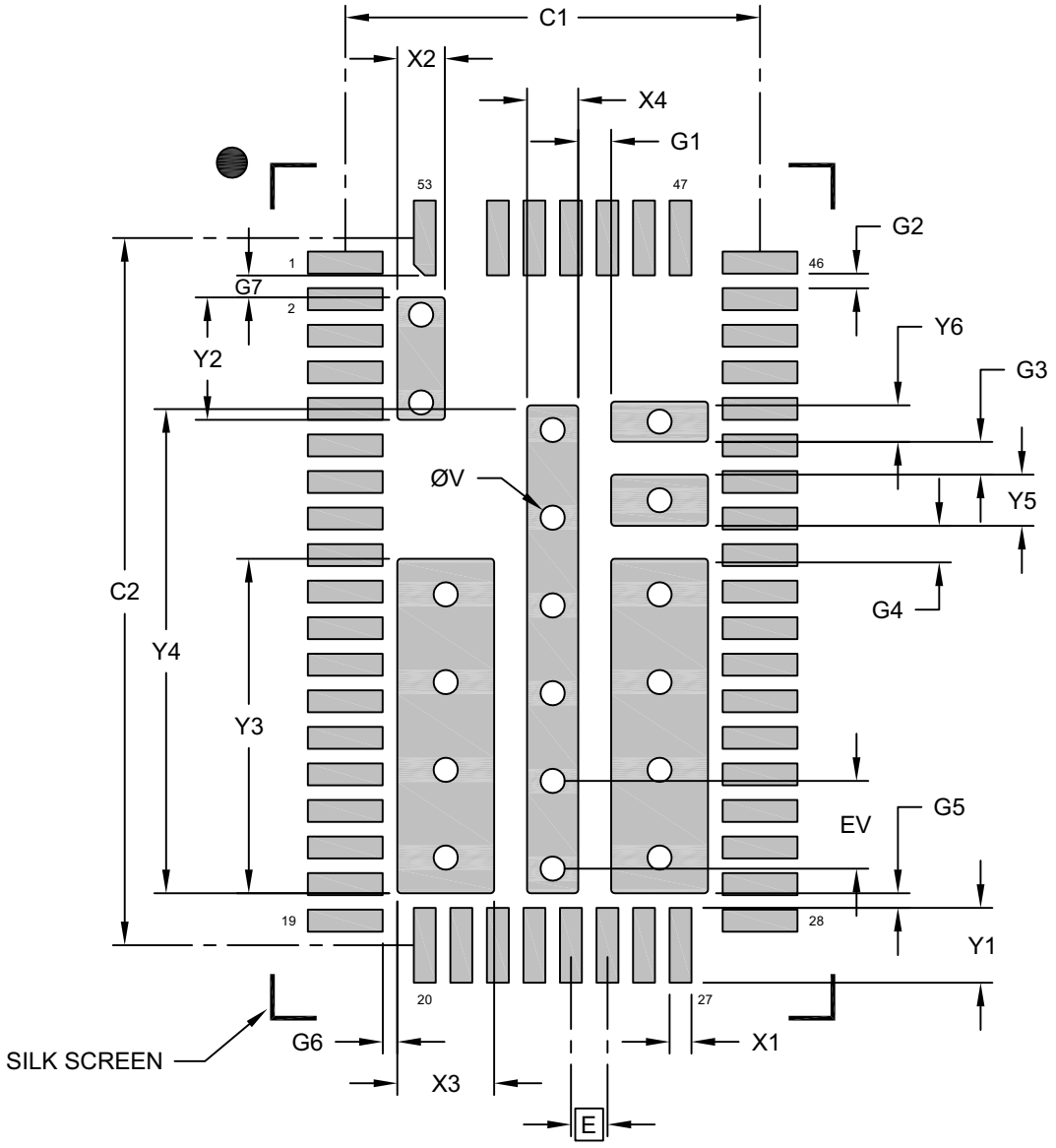

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53-Lead Very Thick Plastic Quad Flat, No Lead Package (QDA) - 6x10x3.05 mm Body [B1QFN]

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RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		5.68	
Contact Pad Spacing	C2		9.68	
Contact Pad Width (X53)	X1			0.30
Contact Pad Length (X53)	Y1			1.02
Center Pad Width	X2			0.65
Center Pad Length	Y2			1.68
Center Pad Width (X4)	X3			1.33
Center Pad Length (X2)	Y3			4.58
Center Pad Width	X4			0.70
Center Pad Length	Y4			6.62
Center Pad Length	Y5			0.70
Center Pad Length	Y6			0.55
Contact Pad to Center Pad (X2)	G1	0.45		
Contact Pad to Contact Pad (X48)	G2	0.20		
Contact Pad to Center Pad	G3	0.45		
Contact Pad to Center Pad	G4	0.45		
Contact Pad to Center Pad	G5	0.20		
Contact Pad to Center Pad	G6	0.20		
Contact Pad to Center Pad	G7	0.30		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch (X12)	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process
3. Thermal vias are centered within each exposed pad.

Microchip Technology Drawing C04-3272 Rev B Sheet 2 of 2

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (September 2019)

- Original release of this document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	–	XX
Device	Temperature Range	Package		Tape and Reel Option

Device:	MIC33M650:	6A, Pin Strapping Power Module with HyperLight Load® Mode and Output Voltage Select
Temperature Range:	Y	= -40°C to +125°C (Extended)
Package:	MP	= 53-Lead Very Thick Plastic Quad Flat B1QFN, 6 mm x 10 mm x 3 mm
Tape and Reel Option:	TR	= Tape and Reel

Examples:

a) MIC33M650YMP: Extended Temperature Range, 53-Lead B1QFN

b) MIC33M650YMP-TR: Extended Temperature Range, 53-Lead B1QFN, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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