



MIC23450

**3MHz, PWM, 2A Triple Buck Regulator
with HyperLight Load® and Power Good**

General Description

The MIC23450 is a high-efficiency, 3MHz, triple 2A, synchronous buck regulator with HyperLight Load® mode. HyperLight Load provides very-high efficiency at light loads and ultra-fast transient response which is perfectly suited for supplying processor core voltages. An additional benefit of this proprietary architecture is very low output ripple voltage throughout the entire load range with the use of small output capacitors. The 5mm x 5mm QFN package saves board space and requires only five external components for each channel.

The MIC23450 is designed for use with a very small inductor, down to 0.47μH, and an output capacitor as small as 2.2μF that enables a total solution size, less than 1mm height.

The MIC23450 has a very-low quiescent current of 23μA each channel and achieves as high as 81% efficiency at 1mA. At higher loads, the MIC23450 provides a constant switching frequency around 3MHz while achieving peak efficiencies up to 93%.

The MIC23450 is available in 32-pin 5mm x 5mm QFN package with an operating junction temperature range from -40°C to +125°C.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

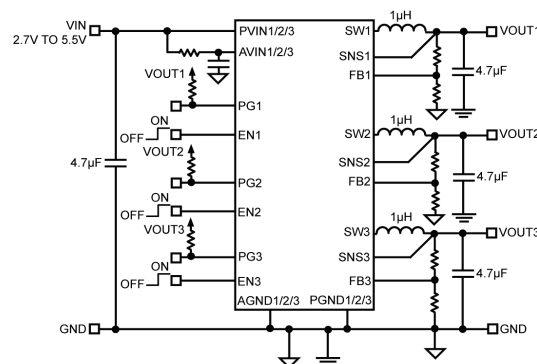
Features

- Input voltage: 2.7V to 5.5V
- 3 independent 2A outputs
- Up to 93% peak efficiency
- 81% typical efficiency at 1mA
- Three independent Power Good Indicators
- 23μA typical quiescent current (per channel)
- 3MHz PWM operation in continuous mode
- Ultra-fast transient response
- Low voltage output ripple
 - 30mV_{PP} ripple in HyperLight Load mode
 - 5mV output voltage ripple in full PWM mode
- Fully integrated MOSFET switches
- 0.01μA shutdown current (per channel)
- Thermal-shutdown and current-limit protection
- Output voltage as low as 1V
- 32-pin 5mm x 5mm QFN
- -40°C to +125°C junction temperature range

Applications

- Solid state drives (SSD)
- μC/μP, FPGA, and DSP power
- Test and measurement systems
- Set-top boxes and DTV
- High-performance servers
- Security/surveillance cameras
- 5V POL applications

Typical Application



HyperLight Load is a registered trademark of Micrel, Inc

Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax +1 (408) 474-1000 • <http://www.micrel.com>

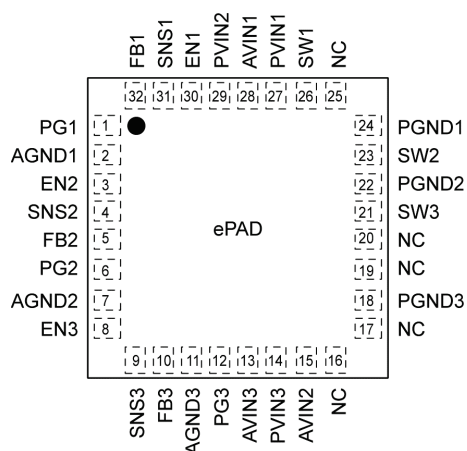
Ordering Information

| Part Number | Marking | Nominal Output Voltage | Junction Temperature Range ⁽¹⁾ | Package ^(2, 3) | Lead Finish |
|-----------------|---------|------------------------|---|---------------------------|-------------|
| MIC23450-AAAYML | AAA | ADJ/ADJ/ADJ | −40°C to +125°C | 32-Pin 5mm × 5mm QFN | Pb-Free |

Notes:

- Other options available. Contact Micrel for details.
- QFN is a Green, RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.
- QFN • = Pin 1 identifier.

Pin Configuration



32-Pin 5mm × 5mm QFN (ML) – Adjustable
Top View

Pin Description

| Pin Number | Pin Name | Pin Function |
|--------------------|-------------|---|
| 26, 23, 21 | SW1, 2, 3 | Switch (Output). Internal power MOSFET output switches for Output 1/2/3. |
| 30, 3, 8 | EN1, 2, 3 | Enable (Input). Logic high enables operation of regulator 1/2/3. Logic low will shut down the device. Do not leave floating. |
| 31, 4, 9 | SNS1, 2, 3 | Sense. Connect to $V_{OUT1,2,3}$ as close to output capacitor as possible to sense output voltage. |
| 32, 5, 10 | FB1, 2, 3 | Feedback. Connect a resistor Divider from output 1/2/3 to ground to set the output voltage. |
| 1, 6, 12 | PG1, 2, 3 | Power Good. Open Drain output for the power good indicator for output 1/2/3. Place a resistor between this pin and a voltage source to detect a power good condition. |
| 2, 7, 11 | AGND1, 2, 3 | Analog Ground. Connect to quiet ground point away from high-current paths, e.g., C_{OUT} for best operation. Must be connected externally to PGND. |
| 27, 29, 14 | PVIN1, 2, 3 | Power Input Voltage. Connect a capacitor to PGND to localize loop currents and decouple switching noise. |
| 28, 15, 13 | AVIN1, 2, 3 | Analog Input Voltage. Connect a capacitor to AGND to decouple noise. |
| 24, 22, 18 | PGND1, 2, 3 | Power Ground. |
| 16, 17, 19, 20, 25 | NC | No Connect. |
| ePAD | ePad | Connect to ground plane to ensure good thermal properties. |

Absolute Maximum Ratings⁽¹⁾

| | |
|---|-------------------|
| Supply Voltage (V_{IN} , AV_{IN}) | –0.3 to 6V |
| Sense (V_{SNS1} , V_{SNS2} , V_{SNS3}) | –0.3 to 6V |
| Power Good (PG1, PG2, PG3) | –0.3 to 6V |
| Output Switch Voltage (V_{SW1} , V_{SW2} , V_{SW3}) | –0.3V to 6V |
| Enable Input Voltage (V_{EN1} , V_{EN2} , V_{EN3}) | –0.3V to V_{IN} |
| Storage Temperature Range | –65°C to +150°C |
| ESD Rating ⁽³⁾ | ESD Sensitive |

Operating Ratings⁽²⁾

| | |
|---|------------------------|
| Supply Voltage (V_{IN}) | +2.7V to +5.5V |
| Enable Input Voltage (V_{EN1} , V_{EN2} , V_{EN3}) | 0V to V_{IN} |
| Output Voltage Range (V_{SNS1} , V_{SNS2} , V_{SNS3}) | +1V to +3.3V |
| Junction Voltage Range (T_J) | –40°C ≤ T_J ≤ +125°C |
| Thermal Resistance | |
| 32-Pin 5mm × 5mm QFN (θ_{JA}) | +30°C/W |
| 32-Pin 5mm × 5mm QFN (θ_{JC}) | +10°C/W |

Electrical Characteristics⁽⁴⁾

$T_A = +25^\circ\text{C}$; $V_{IN} = V_{EN1}$, V_{EN2} , $V_{EN3} = 3.6\text{V}$; $L1 = L2 = L3 = 1\mu\text{H}$; C_{OUT1} , C_{OUT2} , $C_{OUT3} = 4.7\mu\text{F}$, unless otherwise specified.

Bold values indicate –40°C ≤ T_J ≤ +125°C, unless noted.

| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|--|-------------|------|-------------|---------------|
| Supply Voltage Range | | 2.7 | | 5.5 | V |
| Undervoltage Lockout Threshold | Turn-On | 2.45 | 2.55 | 2.65 | V |
| Undervoltage Lockout Hysteresis | | | 75 | | mV |
| Quiescent Current | $I_{OUT} = 0\text{mA}$, $SNS > 1.2 \times V_{OUTNOM}$ | | 69 | 120 | μA |
| Per Channel Shutdown Current | V_{EN1} , V_{EN2} , $V_{EN3} = 0\text{V}$; $V_{IN} = 5.5\text{V}$ | | 0.01 | 5 | μA |
| Output Voltage Accuracy | $V_{IN} = 3.6\text{V}$ if $V_{OUT(NOM)} < 2.5\text{V}$, $I_{LOAD} = 20\text{mA}$ | –2.5 | | +2.5 | % |
| | $V_{IN} = 4.5\text{V}$ if $V_{OUT(NOM)} \geq 2.5\text{V}$, $I_{LOAD} = 20\text{mA}$ | | | | |
| Feedback Voltage (V_{FB1} , V_{FB2} , V_{FB3}) | | .604 | 0.62 | .635 | V |
| Peak Current Limit | I_{OUT1} , I_{OUT2} , I_{OUT3} $SNS1$, $SNS2$, $SNS3 = 0.9 \times V_{OUTNOM}$ | 2 | 4.5 | | A |
| Foldback Current Limit | | | 1.8 | | A |
| Output Voltage Line Regulation (V_{OUT1} , V_{OUT2} , V_{OUT3}) | $V_{IN} = 3.6\text{V}$ to 5.5V if $V_{OUTNOM1, 2, 3} < 2.5\text{V}$, $I_{LOAD} = 20\text{mA}$ | | 0.3 | | %/V |
| | $V_{IN} = 4.5\text{V}$ to 5.5V if $V_{OUTNOM1, 2, 3} \geq 2.5\text{V}$, $I_{LOAD} = 20\text{mA}$ | | | | |
| Output Voltage Load Regulation (V_{OUT1} , V_{OUT2} , V_{OUT3}) | DCM: $20\text{mA} < I_{LOAD} < 130\text{mA}$, $V_{IN} = 3.6\text{V}$ if $V_{OUTNOM} < 2.5\text{V}$ | | 0.2 | | % |
| | DCM: $20\text{mA} < I_{LOAD} < 130\text{mA}$, $V_{IN} = 5.0\text{V}$ if $V_{OUTNOM} > 2.5\text{V}$ | | 0.4 | | |
| | CCM: $200\text{mA} < I_{LOAD} < 500\text{mA}$, $V_{IN} = 3.6\text{V}$ if $V_{OUTNOM} < 2.5\text{V}$ | | 0.6 | | |
| | CCM: $200\text{mA} < I_{LOAD} < 1\text{A}$, $V_{IN} = 5.0\text{V}$ if $V_{OUTNOM} > 2.5\text{V}$ | | 0.3 | | |
| PWM Switch ON-Resistance (R_{SW1} , R_{SW2} , R_{SW3}) | I_{SW1} , I_{SW2} , $I_{SW3} = +100\text{mA}$ (PMOS) | | 0.2 | | Ω |
| | I_{SW1} , I_{SW2} , $I_{SW3} = -100\text{mA}$ (NMOS) | | | | |

Notes:

- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- Devices are ESD sensitive. Handling precautions recommended. Human body model, $1.5\text{k}\Omega$ in series with 100pF .
- Specification for packaged product only.

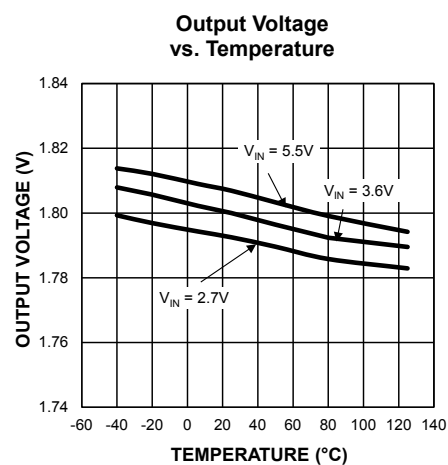
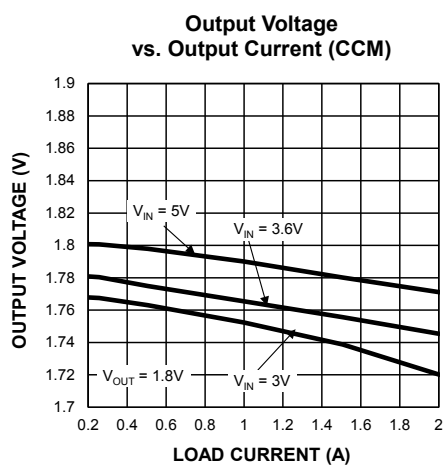
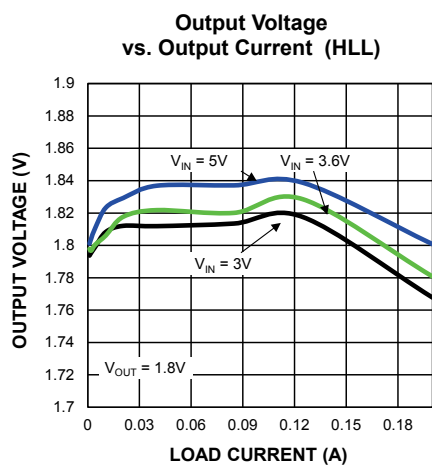
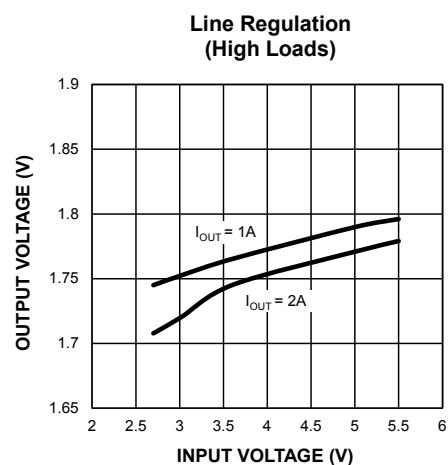
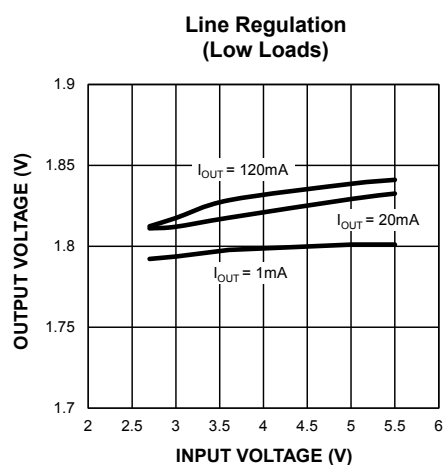
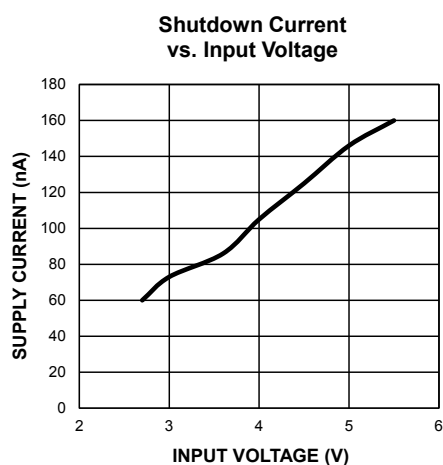
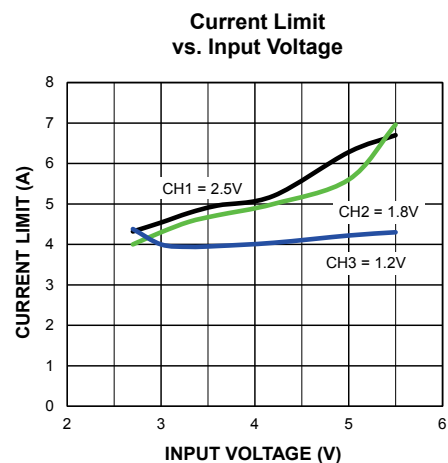
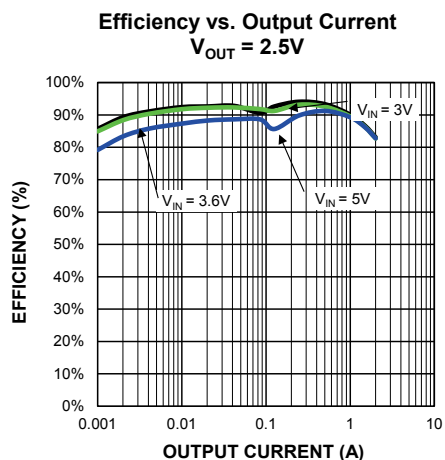
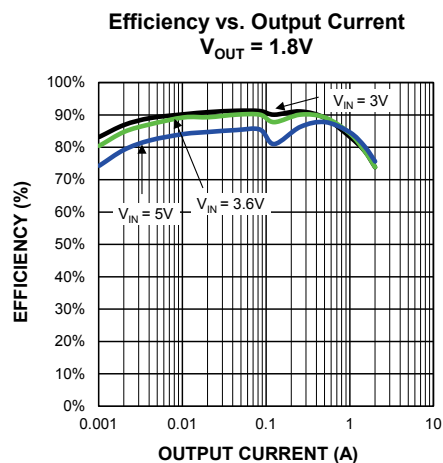
Electrical Characteristics⁽⁴⁾ (Continued)

$T_A = +25^{\circ}\text{C}$; $V_{IN} = V_{EN1}, V_{EN2}, V_{EN3} = 3.6\text{V}$; $L1 = L2 = L3 = 1\mu\text{H}$; $C_{OUT1}, C_{OUT2}, C_{OUT3} = 4.7\mu\text{F}$, unless otherwise specified.

Bold values indicate $-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$, unless noted.

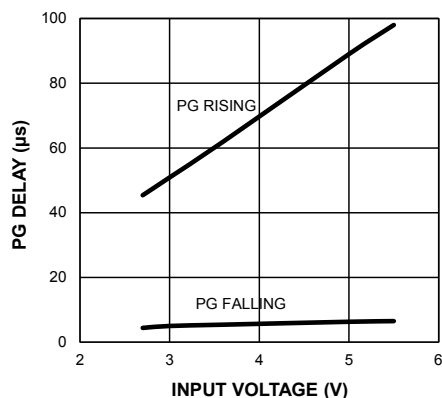
| Parameter | Condition | Min. | Typ. | Max. | Units |
|-------------------------------------|---|------------|------|------------|--------------------|
| Maximum Frequency | $I_{OUT1}, I_{OUT2}, I_{OUT3} = 120\text{mA}$ | | 3 | | MHz |
| Soft-Start Time | $V_{OUT1}, V_{OUT2}, V_{OUT3} = 90\%$ | | 115 | | μs |
| Power Good Threshold | % of V_{NOM} | 83 | 90 | 96 | % |
| Power Good Hysteresis | | | 10 | | % |
| Power Good Pull Down | $V_{SNS} = 90\% V_{NOM}, I_{PG} = 1\text{mA}$ | | | 200 | mV |
| Enable Threshold | Turn-On | 0.5 | 0.8 | 1.2 | V |
| Enable Input Current | | | 0.1 | 1 | μA |
| Overtemperature Shutdown | | | 160 | | $^{\circ}\text{C}$ |
| Overtemperature Shutdown Hysteresis | | | 20 | | $^{\circ}\text{C}$ |

Typical Characteristics

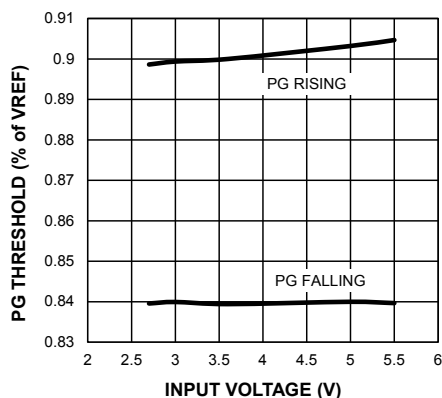


Typical Characteristics (Continued)

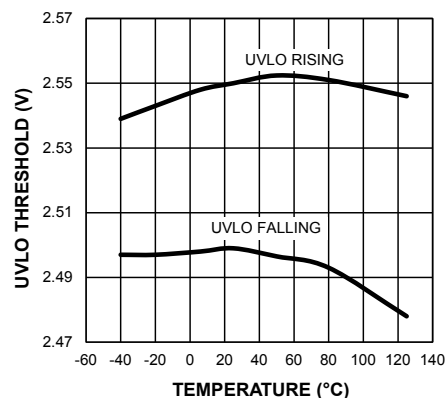
**PG Delay Time
vs. Input Voltage**



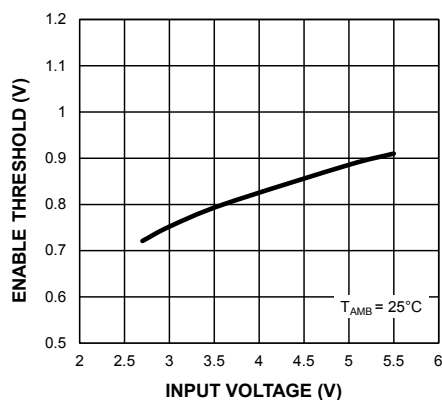
**PG Thresholds
vs. Input Voltage**



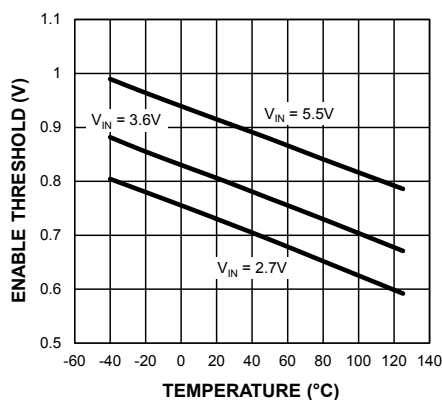
**UVLO Threshold
vs. Temperature**



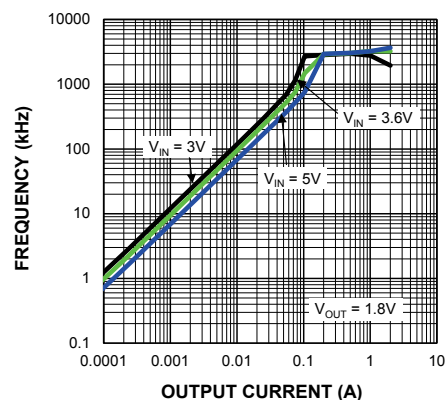
**Enable Threshold
vs. Input Voltage**



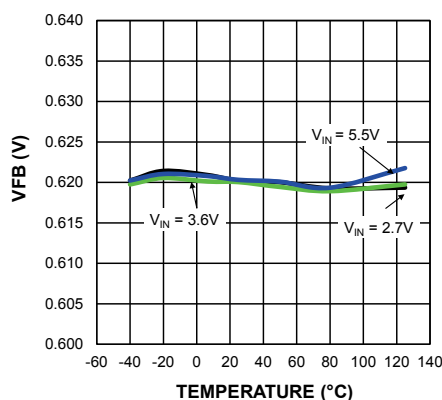
**Enable Threshold
vs. Temperature**



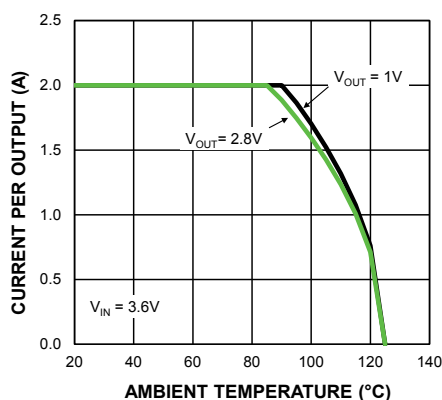
**Switching Frequency
vs. Load Current**



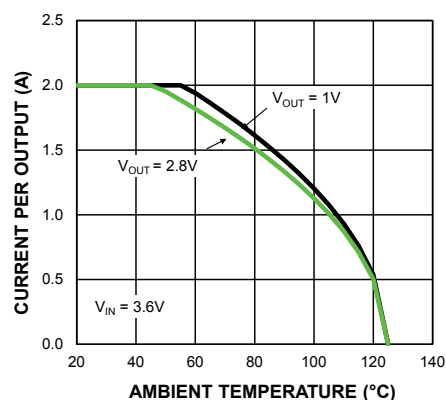
**VFB
vs. Temperature**



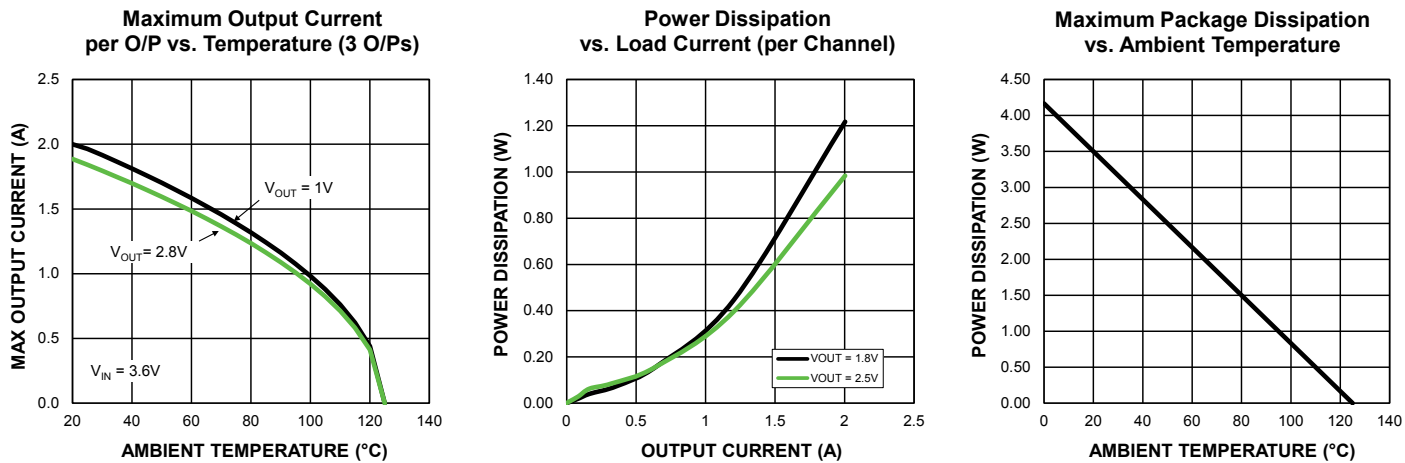
**Maximum Output Current
per O/P vs. Temperature (1 O/P)**



**Maximum Output Current
per O/P vs. Temperature (2 O/Ps)**

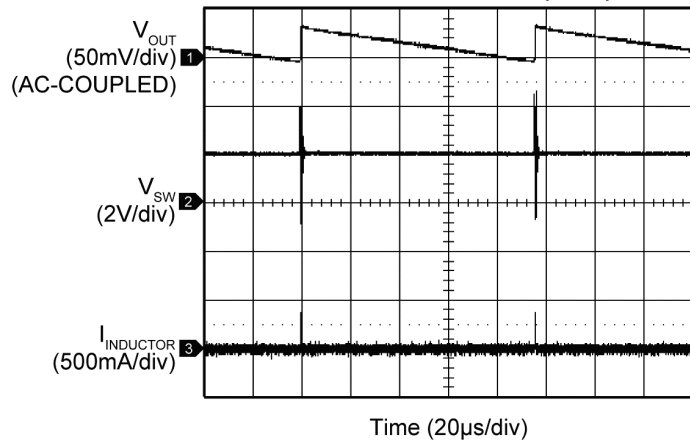


Typical Characteristics (Continued)

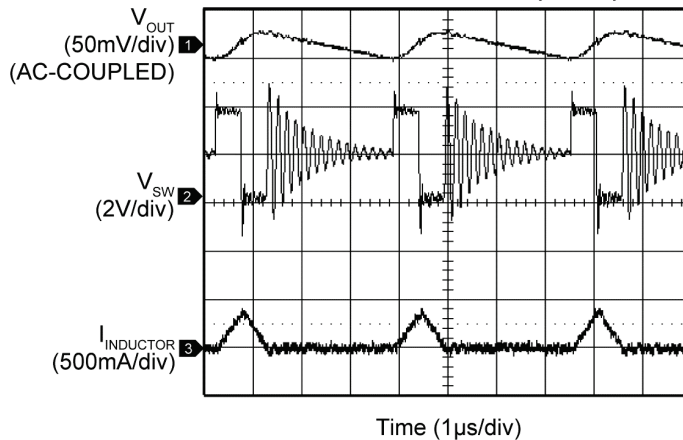


Functional Characteristics

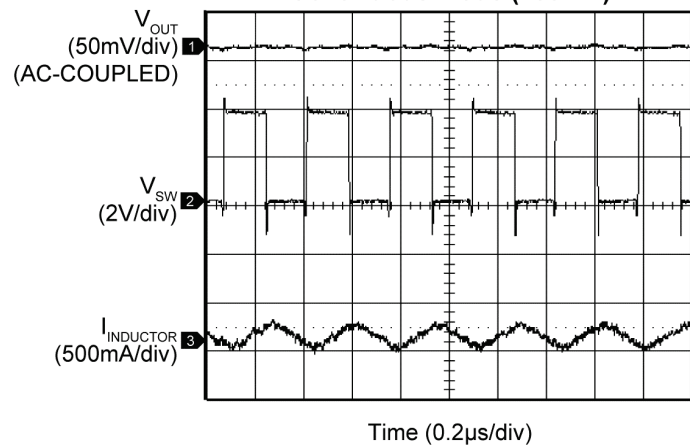
**Switching Waveform
Discontinuous Mode (1mA)**



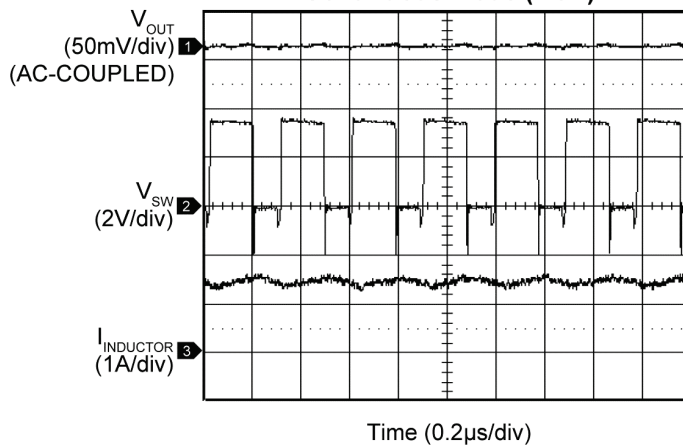
**Switching Waveform
Discontinuous Mode (50mA)**



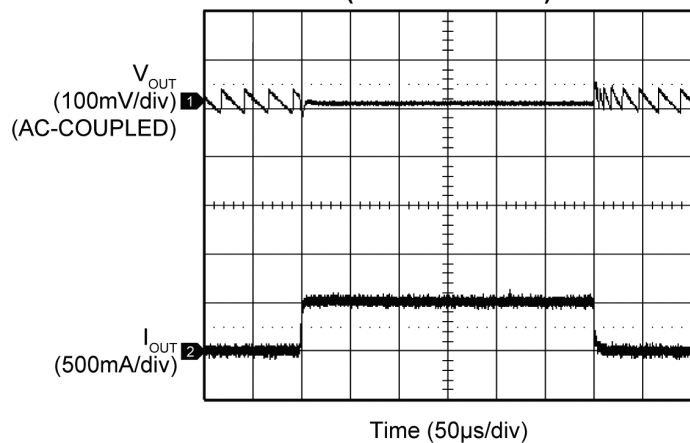
**Switching Waveform
Continuous Mode (150mA)**



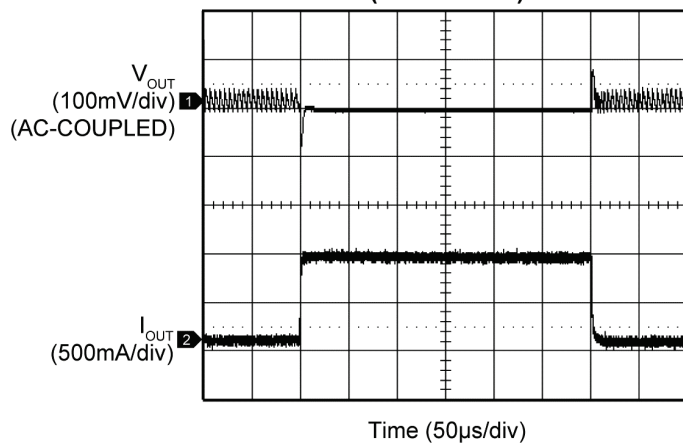
**Switching Waveform
Continuous Mode (1.5A)**



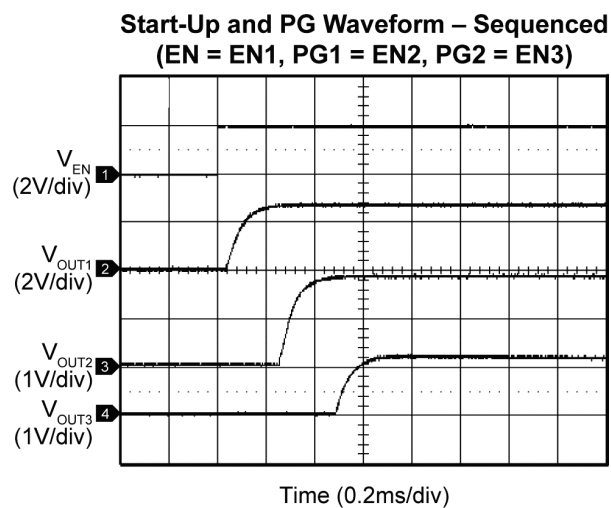
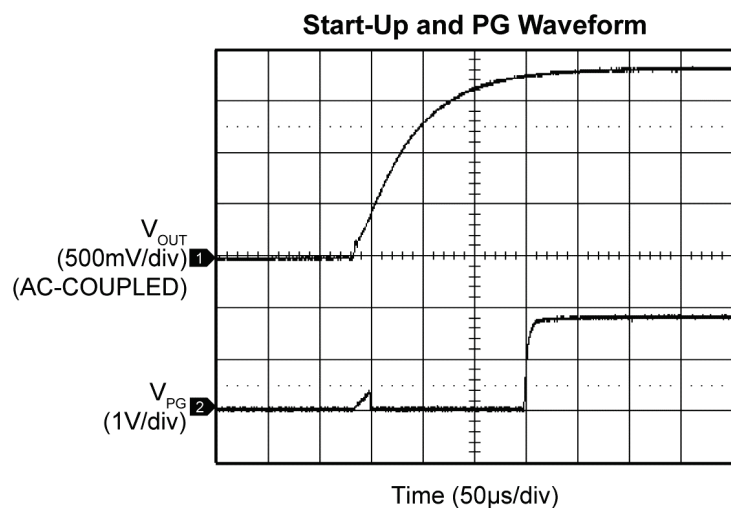
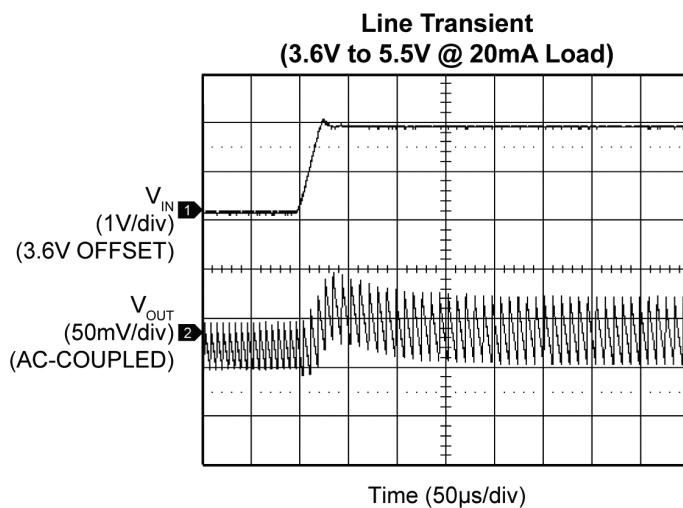
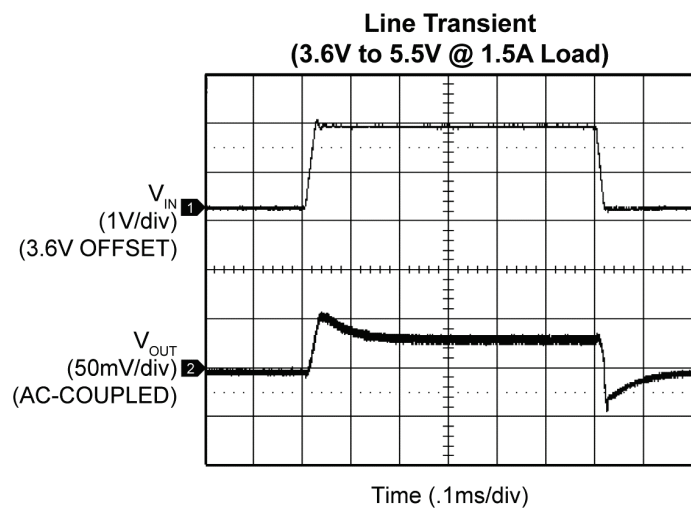
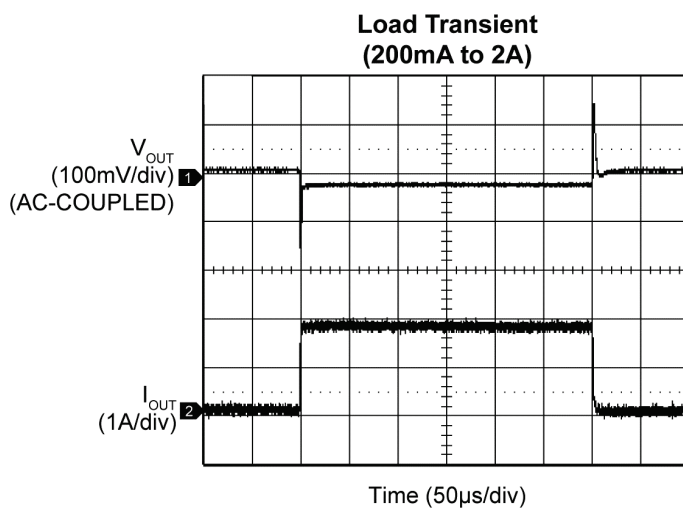
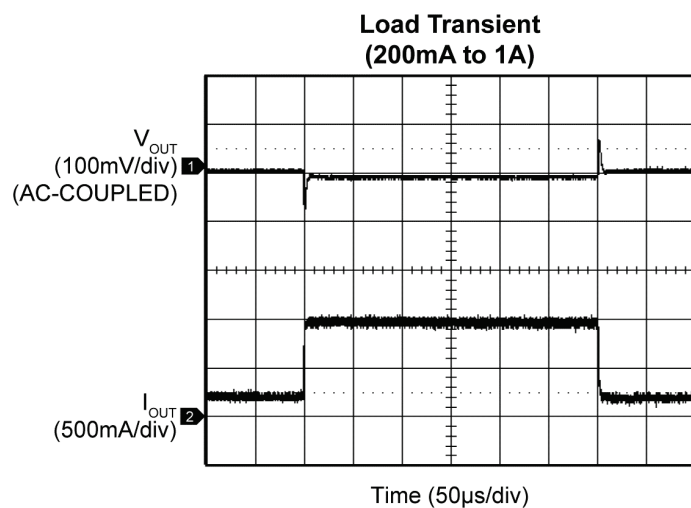
**Load Transient
(10mA to 500mA)**



**Load Transient
(50mA to 1A)**

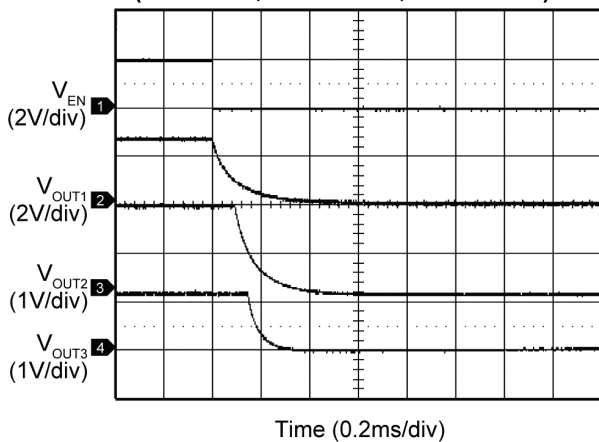


Functional Characteristics (Continued)

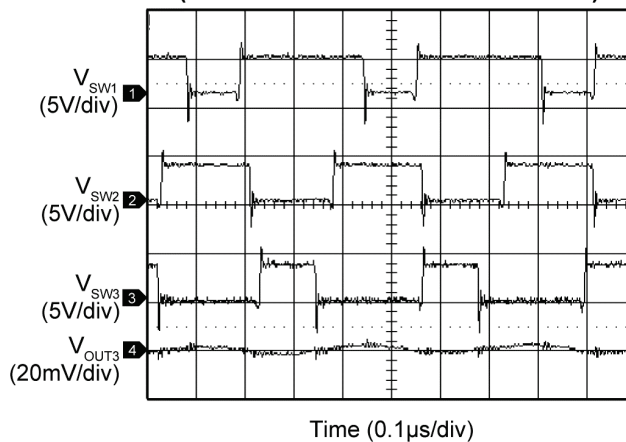


Functional Characteristics (Continued)

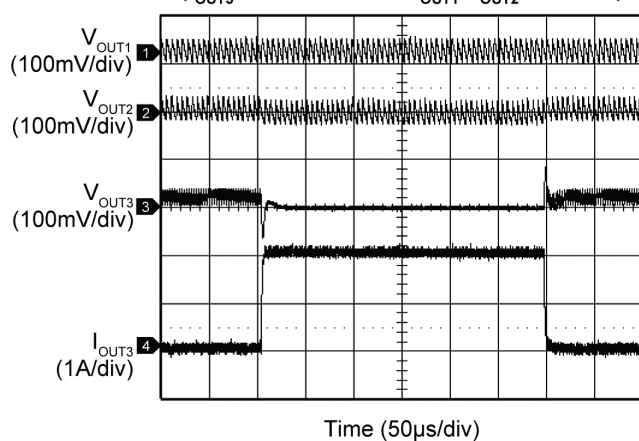
Shut-Down and PG Waveform – Sequenced
(EN = EN1, PG1 = EN2, PG2 = EN3)



Switching Waveform
(All Channels in Continuous Mode)



Transient Cross Regulation
($I_{OUT3} = 50mA$ to $2A$, I_{OUT1} , $I_{OUT2} = 20mA$)



Functional Diagram

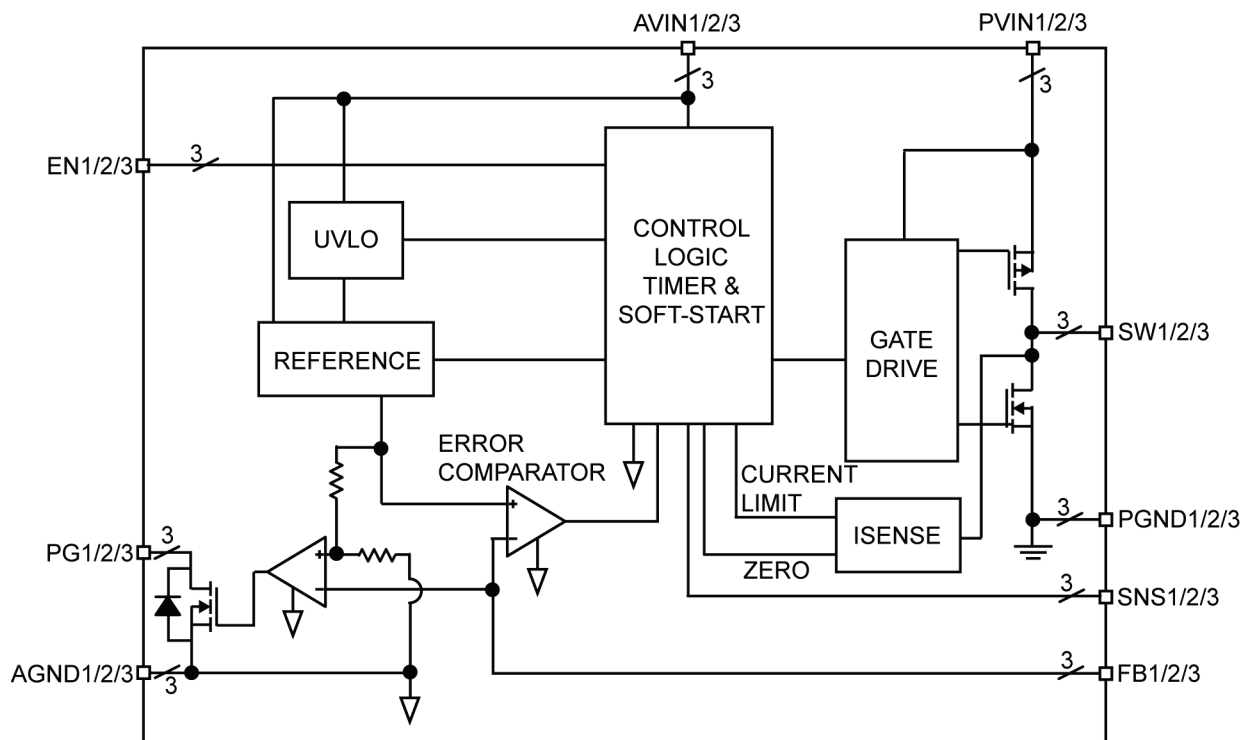


Figure 1. Simplified MIC23450 Adjustable Functional Block Diagram

Functional Description

PVIN

The input supply (PVIN) provides power to the internal MOSFETs for the switch mode regulator. The VIN operating range is 2.7V to 5.5V so an input capacitor, with a minimum voltage rating of 6.3V, is recommended. Due to the high di/dt switching speeds, a minimum 2.2μF or 4.7μF recommended bypass capacitor placed close to PVIN and the power ground (PGND) pin is required. Refer to the layout recommendations for details.

AVIN

The input supply (AVIN) provides power to the internal control circuitry. As the high di/dt switching speeds on PVIN cause small voltage spikes, an RC filter comprising 50Ω and a minimum 100nF decoupling capacitor placed close to the AVIN and signal ground (AGND) pin is required.

EN

A logic high signal on the enable pin activates the output voltage of the device. A logic low signal on the enable pin deactivates the output and reduces supply current to 0.01μA. MIC23450 features internal soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start up. Do not leave the EN pin floating.

SW

The switch (SW) connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load, SNS pin and output capacitor. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

SNS

The sense (SNS) pin is connected to the output of the device to provide feedback to the control circuitry. The SNS connection should be placed close to the output capacitor. Refer to the layout recommendations for more details.

AGND

The analog ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the layout recommendations for more details.

PGND

The power ground pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as short and wide as possible and separate from the analog ground (AGND) loop as applicable. Refer to the layout recommendations for more details.

PG

The power good (PG) pin is an open drain output which indicates logic high when the output voltage is typically above 90% of its steady state voltage. A pull-up resistor of more than 5kΩ should be connected from PG to V_{OUT}.

FB

The feedback (FB) pin is the control input for programming the output voltage. A resistor divider network is connected to this pin from the output and is compared to the internal 0.62V reference within the regulation loop.

The output voltage can be programmed between 1V and 3.3V using Equation 1:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) \quad \text{Eq. 1}$$

Where: R1 is the top, V_{OUT} connected resistor, R2 is the bottom, AGND connected resistor.

Table 1 illustrates example feedback resistor values.

| V _{OUT} | R1 | R2 |
|------------------|------|-------|
| 1.2V | 274k | 294k |
| 1.5V | 316k | 221k |
| 1.8V | 301k | 158k |
| 2.5V | 324k | 107k |
| 3.3V | 309k | 71.5k |

Table 1. Feedback Resistor Values

Application Information

The MIC23450 is a triple high performance DC-to-DC step down regulator offering a small solution size. Supporting 3 outputs with currents up to 2A inside a 5mm x 5mm QFN package, the IC requires only five external components per channel while meeting today's miniature portable electronic device needs. Using the HyperLight Load® switching scheme, the MIC23450 is able to maintain high efficiency throughout the entire load range while providing ultra-fast load transient response. The following sections provide additional device application information.

Input Capacitor

A 2.2μF ceramic capacitor or greater should be placed close to the PVIN pin for each channel and it's corresponding PGND pin for bypassing. For example, Murata GRM188R60J475ME19D, size 0603, 4.7μF ceramic capacitor is ideal, based upon performance, size and cost. A X5R or X7R temperature rating is recommended for the input capacitor. Y5V temperature rating capacitors, aside from losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

Output Capacitor

The MIC23450 is designed for use with a 2.2μF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response but could also increase solution size or cost. A low equivalent series resistance (ESR) ceramic output capacitor such as the Murata GRM188R60J475ME84D, size 0603, 4.7μF ceramic capacitor is recommended based upon performance, size and cost. Both the X7R or X5R temperature rating capacitors are recommended. The Y5V and Z5U temperature rating capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies.

Inductor Selection

When selecting an inductor, it is important to consider the following factors (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23450 is designed for use with a 0.47μH to 2.2μH inductor. For faster transient response, a 0.47μH inductor will yield the best result. On the other hand, a 2.2μH inductor will yield lower output voltage ripple. For the best compromise of these, generally, a 1μH is recommended.

Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current does not cause the inductor to saturate. Peak current can be calculated as shown in Equation 2:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right] \quad \text{Eq. 2}$$

As shown in Equation 2, the peak inductor current is inversely proportional to the switching frequency and the inductance; the lower the switching frequency or the inductance the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Typical Application Circuit and Bill of Materials for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the Efficiency Considerations.

The transition between high loads (CCM) to HyperLight Load (HLL) mode is determined by the inductor ripple current and the load current as illustrated in Figure 2.

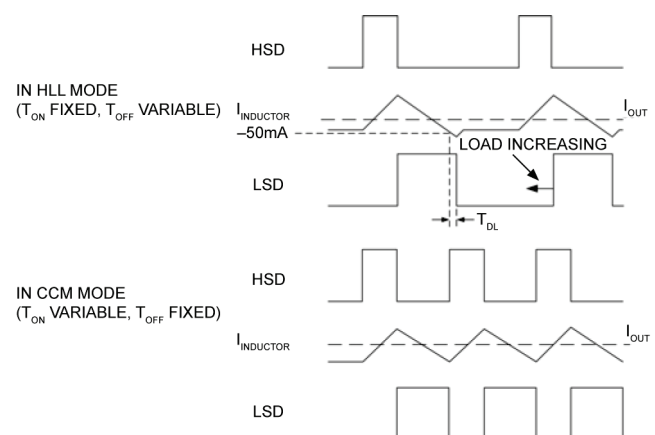


Figure 2. Transition between CCM Mode and HLL Mode

The diagram shows the signals for high side switch drive (HSD) for T_{ON} control, the Inductor current and the low side switch drive (LSD) for T_{OFF} control.

In HLL mode, the inductor is charged with a fixed T_{ON} pulse on the high side switch (HSD). After this, the LSD is switched on and current falls at a rate V_{OUT}/L . The controller remains in HLL mode while the inductor falling current is detected to cross approximately -50mA. When the LSD (or T_{OFF}) time reaches its minimum and the inductor falling current is no longer able to reach this -50mA threshold, the part is in CCM mode and switching at a virtually constant frequency.

Once in CCM mode, the T_{OFF} time will not vary. Therefore, it is important to note that if L is large enough, the HLL transition level will not be triggered.

That inductor is:

$$L_{MAX} = \frac{V_{OUT} \times 135ns}{2 \times 50mA} \quad \text{Eq. 3}$$

Compensation

The MIC23450 is designed to be stable with a $0.47\mu H$ to $2.2\mu H$ inductor with a $4.7\mu F$ ceramic (X5R) output capacitor.

Duty Cycle

The typical maximum duty cycle of the MIC23450 is 80%.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$\text{Efficiency \%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100 \quad \text{Eq. 4}$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery-powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R . Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET $R_{DS(on)}$ multiplied by the Switch Current squared. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at a constant 4MHz frequency and the switching transitions make up the switching losses.

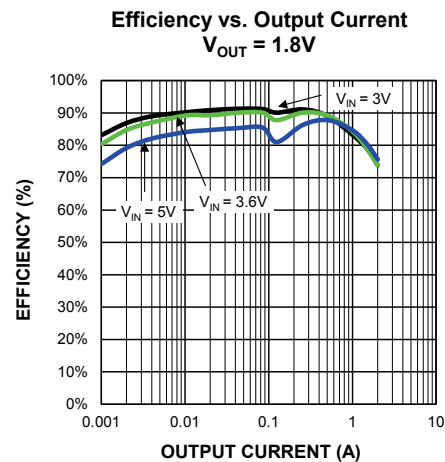


Figure 3. Efficiency under Load

The figure above shows an efficiency curve. From no load to 100mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load mode, the MIC23450 is able to maintain high efficiency at low output currents.

Over 100mA, efficiency loss is dominated by MOSFET $R_{DS(on)}$ and inductor losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, thereby reducing the internal $R_{DS(on)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$P_{DCR} = I_{OUT}^2 \times DCR \quad \text{Eq. 5}$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{\text{OUT}} \times I_{\text{OUT}}}{V_{\text{OUT}} \times I_{\text{OUT}} + P_{\text{DCR}}} \right) \right] \times 100$$

Eq. 6

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Thermal Considerations

As most applications will not require 2A continuous current from all outputs at all times, it is useful to know what the thermal limits will be for various loading profiles.

The allowable overall package dissipation is limited by the intrinsic thermal resistance of the package ($R_{\theta(J-C)}$) and the area of copper used to spread heat from the package case to the ambient surrounding temperature ($R_{\theta(C-A)}$). The composite of these two thermal resistances is $R_{\theta(J-A)}$, which represents the package thermal resistance with at least 1 square inch of copper ground plane. From this figure, which for the MIC23450 is 30°C/W, we can calculate maximum internal power dissipation as shown in Equation 7:

$$PD_{\text{MAX}} = \frac{T_{\text{JMAX}} - T_{\text{AMB}}}{R_{\theta(J-A)}}$$

Eq. 7

where:

T_{JMAX} = Maximum junction temp (125°C)

T_{AMB} = Ambient temperature

$R_{\theta(J-A)}$ = 30°C/W

As can be expected, the allowable dissipation tends towards zero as the ambient temperature increases towards the maximum operating junction temperature.

The graph of PD_{MAX} vs. Ambient temperature could be drawn quite simply using this equation. However, a more useful measure is the maximum output current per regulator vs. ambient temperature. For this, we must first create an 'exchange rate' between power dissipation per regulator (P_{DISS}) and its output current (I_{OUT}).

An accurate measure of this function can utilize the efficiency curve, as illustrated in Equation 8:

$$\eta = \frac{P_{\text{OUT}}}{P_{\text{OUT}} + P_{\text{LOSS}}}$$

$$P_{\text{LOSS}} = \frac{P_{\text{OUT}}(1-\eta)}{\eta}$$

Eq. 8

where:

η = Efficiency

$P_{\text{OUT}} = I_{\text{OUT}} \cdot V_{\text{OUT}}$

To arrive at the internal package dissipation P_{DISS} , one would need to remove the inductor loss P_{DCR} which is not dissipated within the package. This however, does not give a worst case figure, since efficiency is typically measured on a nominal part at nominal temperatures. The I_{OUT} to P_{DISS} function we use therefore is a synthesized P_{DISS} which accounts for worst case values at maximum operating temperature, as shown in Equation 9:

$$P_{\text{DISS}} = I_{\text{OUT}}^2 \left(R_{\text{DS(on)_P}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}} + R_{\text{DS(on)_N}} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right) \right)$$

Eq. 9

where:

$R_{\text{DS(on)_P}}$ = Maximum $R_{\text{DS(on)}}$ of the high side, P-Channel switch at T_{JMAX}

$R_{\text{DS(on)_N}}$ = Maximum $R_{\text{DS(on)}}$ of the low side, N-Channel switch at T_{JMAX}

V_{OUT} = Output Voltage,

V_{IN} = Input Voltage

Since ripple current and switching losses are small with respect to resistive losses at maximum output current, they can be considered negligible for the purpose of this method, but could be included if required.

Now we have a function describing P_{DISS} in terms of I_{OUT} , we can substitute P_{DISS} with Equation 7 to form the function of maximum output current I_{OUTMAX} vs. ambient temperature T_{AMB} (Equation 10):

$$I_{OUTMAX} = \sqrt{\frac{\frac{T_{JMAX} - T_{AMB}}{R\theta_{(J-A)}}}{R_{DS(on)_P} \times \frac{V_{OUT}}{V_{IN}} + R_{DS(on)_N} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}} \quad \text{Eq. 10}$$

The curves shown in the characteristic curves section are plots of this function adjusted to account for 1, 2 or 3 regulators running simultaneously.

HyperLight Load Mode

Each regulator in the MIC23450 uses a minimum on and off time proprietary control loop (patented by Micrel). When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23450 works in pulse-frequency modulation (PFM) to regulate the output. As the output current increases, the off-time decreases, thus provides more energy to the output. This switching scheme improves the efficiency of MIC23450 during light load currents by only switching when it is needed. As the load current increases, the MIC23450 goes into continuous conduction mode (CCM) and switches at a frequency centered at 3MHz. The equation to calculate the load when the MIC23450 goes into continuous conduction mode may be approximated in Equation 11:

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2L \times f} \right) \quad \text{Eq. 11}$$

As shown in Equation 11, the load at which the MIC23450 transitions from HyperLight Load mode to PWM mode is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), duty cycle (D), inductance (L) and frequency (f). As shown in Figure 4, as the Output Current increases, the switching frequency also increases until the MIC23450 goes from HyperLight Load mode to PWM mode at approximately 120mA. The MIC23450 will switch at a relatively constant frequency around 3MHz once the output current is over 120mA.

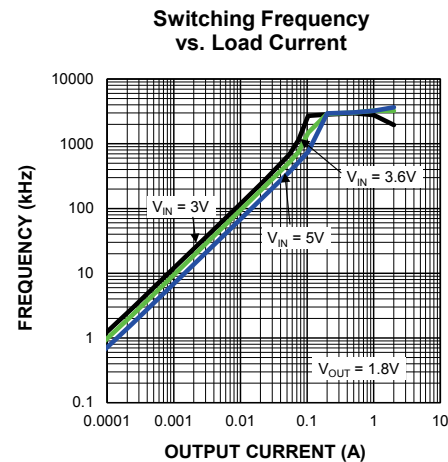


Figure 4. SW Frequency vs. Output Current

Multiple Sources

The MIC23450 provides all the pins necessary to operate the 3 regulators from independent sources. This can be useful in partitioning power within a multi rail system. For example, it is possible that within a system, two supplies are available; 3.3V and 5V. The MIC23450 can be connected to use the 3.3V supply to provide two, low voltage outputs (e.g. 1.2V and 1.8V) and use the 5V rail to provide a higher output (e.g. 2.5V), resulting in the power blocks shown in Figure 5.

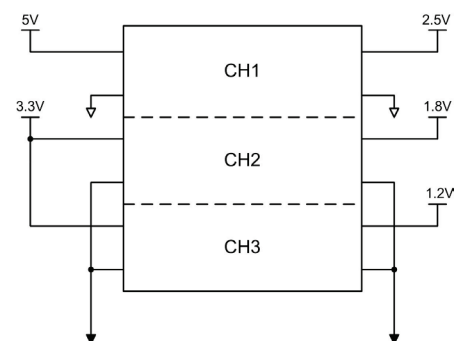
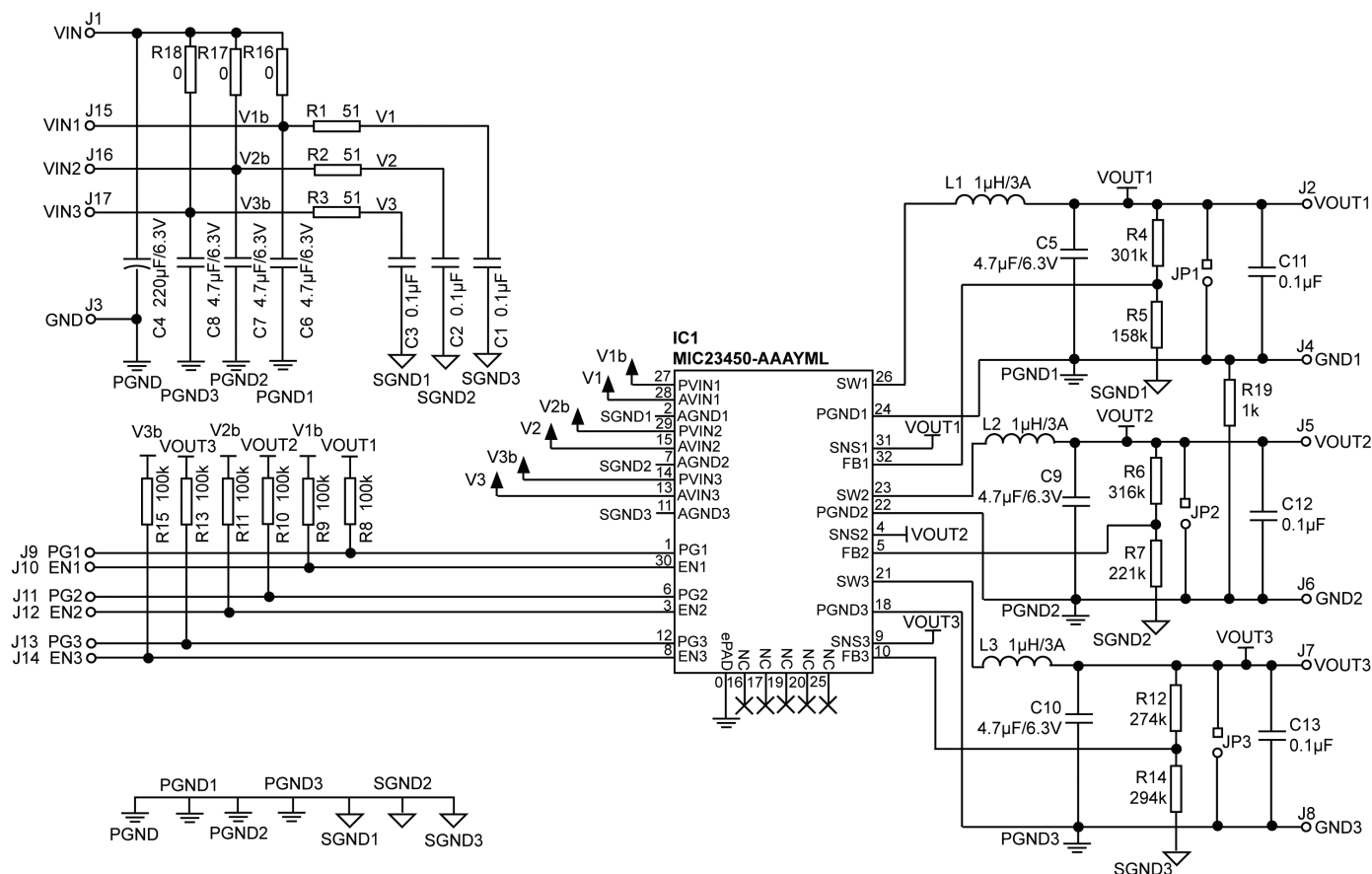


Figure 5. Multi-Source Power Block Diagram

Typical Application Circuit



Bill of Materials

| Item | Part Number | Manufacturer | Description | Qty. |
|---------------------------|--------------------|--------------------------|--|------|
| C1, C2, C3, C11, C12, C13 | C1608X5R1E104K | TDK ⁽¹⁾ | Ceramic Capacitor, 0.1μF, 6.3V, X5R, Size 0603 | 6 |
| | GRM188R60J104KD | Murata ⁽²⁾ | | |
| C4 | EEUFR1A221 | Panasonic ⁽³⁾ | Electrolytic Capacitor, 220μF, 10V, Size 6.3mm | 1 |
| C6, C7, C8, C5, C9, C10 | C1608X5R0J475K | TDK | Ceramic Capacitor, 4.7μF, 6.3V, X5R, Size 0603 | 6 |
| | GRM188R60J475KE19D | Murata | | |
| R1, R2, R3 | CRCW040251R0FKEA | Vishay ⁽⁴⁾ | Resistor, 51Ω, Size 0402 | 3 |
| R4 | CRCW04023013FKEA | Vishay | Resistor, 301kΩ, Size 0402 | 1 |

Notes:

1. TDK: www.tdk.com.
2. Murata Tel: www.murata.com.
3. Panasonic: www.panasonic.com.
4. Vishay Tel: www.vishay.com.

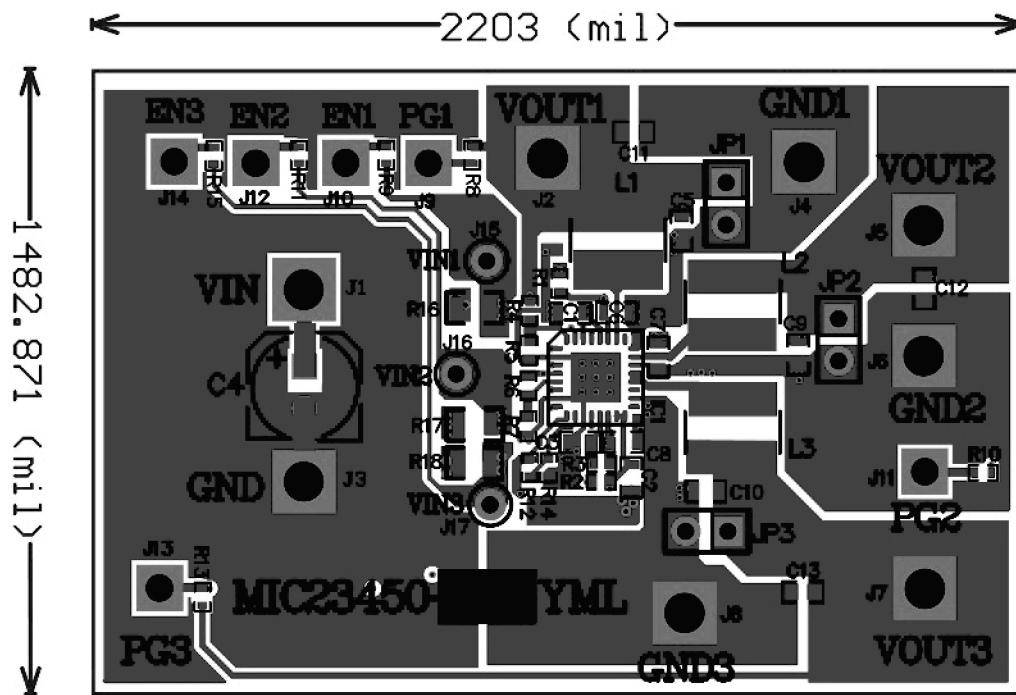
Bill of Materials (Continued)

| Item | Part Number | Manufacturer | Description | Qty. |
|-------------------------------|-------------------|-----------------------------|--|------|
| R5 | CRCW04021583FKEA | Vishay | Resistor, 158k Ω , Size 0402 | 1 |
| R6 | CRCW04023163FKEA | Vishay | Resistor, 316k Ω , Size 0402 | 1 |
| R7 | CRCW04022213FKEA | Vishay | Resistor, 221k Ω , Size 0402 | 1 |
| R12 | CRCW04022743FKEA | Vishay | Resistor, 274k Ω , Size 0402 | 1 |
| R14 | CRCW04022943FKEA | Vishay | Resistor, 294k Ω , Size 0402 | 1 |
| R8, R9, R10, R11, R13, R15 | CRCW04021003FKEA | Vishay | Resistor, 100k Ω , Size 0402 | 6 |
| R16, R17, R18 | CRCW08050000FKEA | Vishay | Resistor, 0 Ω , Size 0805 | 3 |
| L1, L2, L3 | VLS3012ST-1R0N1R9 | TDK | 1 μ H, 2A, 60m Ω , L3.0mm x W3.0mm x H1.0mm | 3 |
| | LQH44PN1R0NJ0 | Murata | 1 μ H, 2.8A, 50m Ω , L4.0mm x W4.0mm x H1.2mm | |
| U1 | MIC23450-AAAYML | Micrel, Inc. ⁽⁵⁾ | 3MHz PWM 2A Buck Regulator with HyperLight Load | 1 |

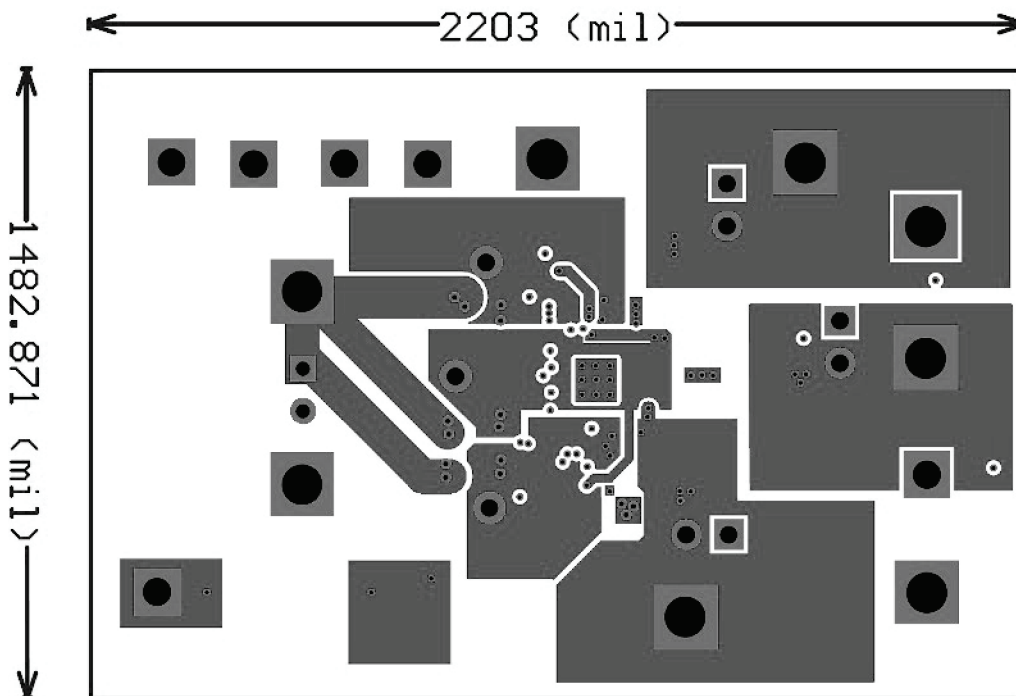
Note:

5. Micrel, Inc.: www.micrel.com.

PCB Layout Recommendations

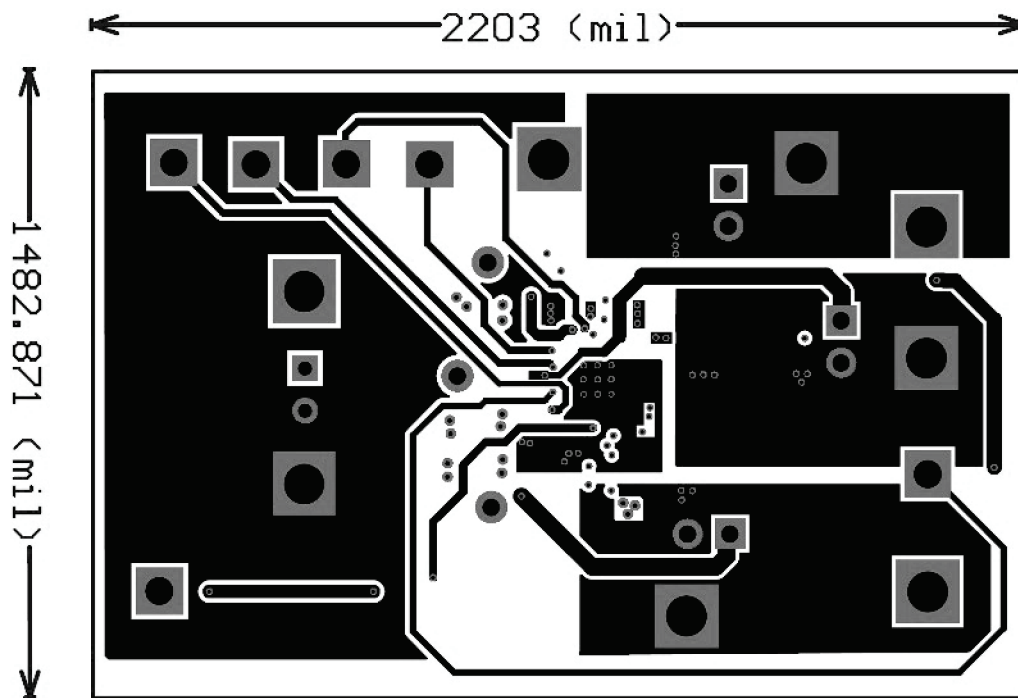


Top Layer

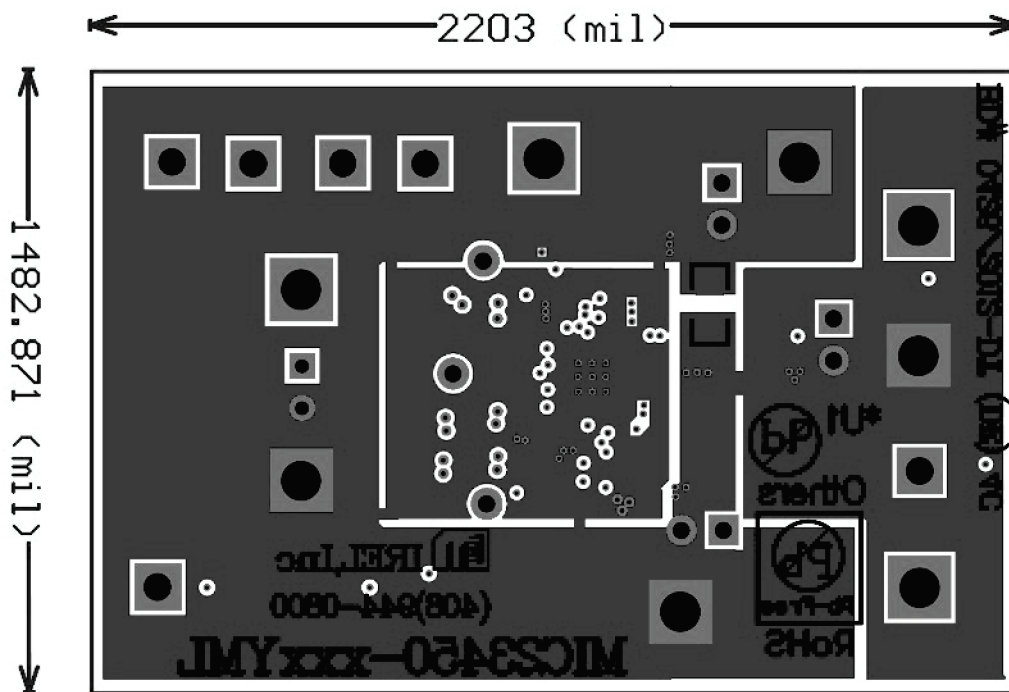


Mid-Layer 1

PCB Layout Recommendations (Continued)

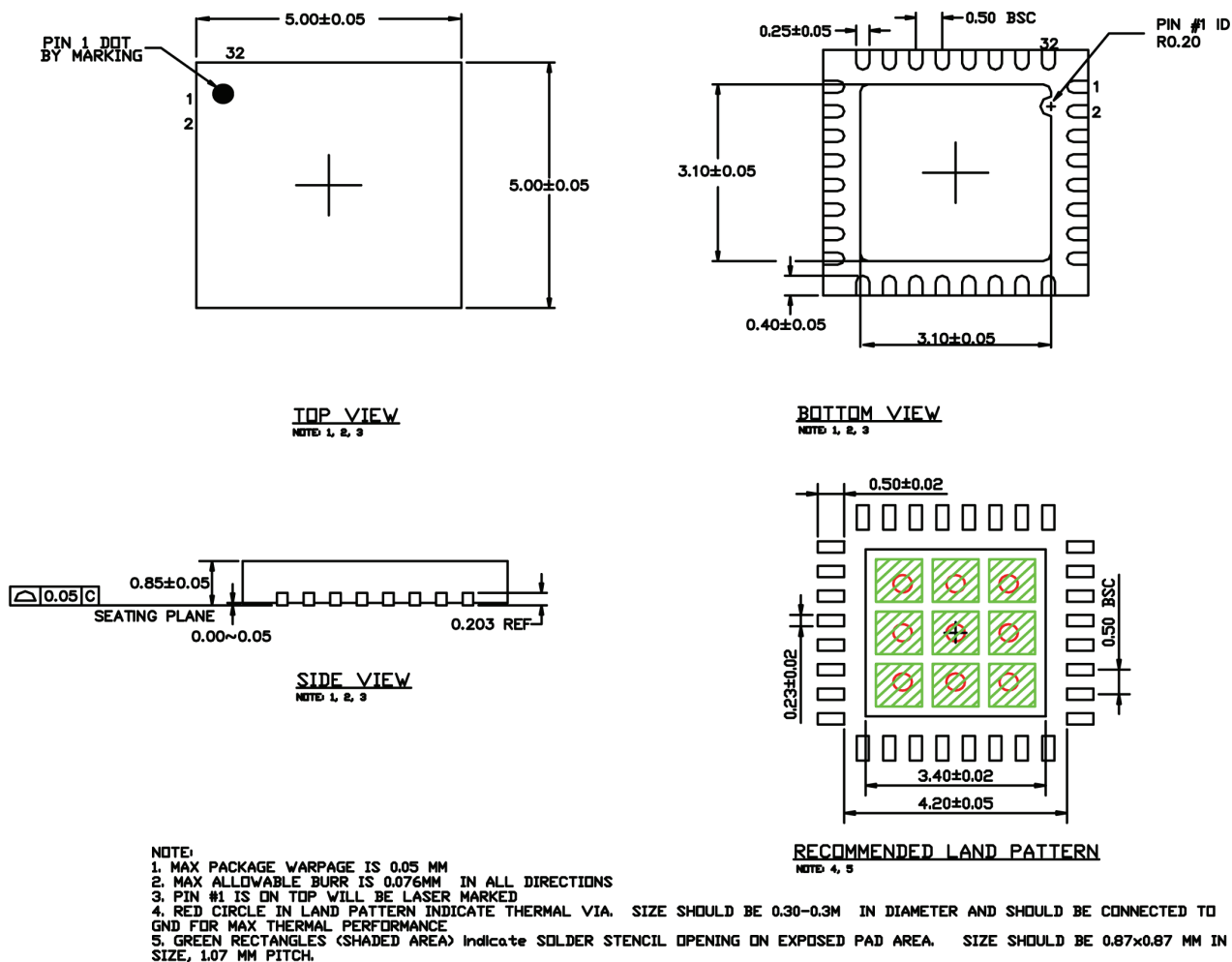


Mid-Layer 2



Bottom Layer

Package Information¹



32-Pin 5mm × 5mm QFN

Note:

- Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USATEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

Micrel makes no representations or warranties with respect to the accuracy or completeness of the information furnished in this data sheet. This information is not intended as a warranty and Micrel does not assume responsibility for its use. Micrel reserves the right to change circuitry, specifications and descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Micrel's terms and conditions of sale for such products, Micrel assumes no liability whatsoever, and Micrel disclaims any express or implied warranty relating to the sale and/or use of Micrel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2013 Micrel, Incorporated.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Microchip:](#)

[MIC23450-AAAYML T5](#) [MIC23450-AAAYML TR](#) [MIC23450-AAAYML-T5](#) [MIC23450-AAAYML-TR](#)