MIC22205

2A, Integrated, Switch, High-Efficiency, Synchronous Buck Regulator with Frequency Programmable up to 4MHz

General Description

The Micrel MIC22205 is a high-efficiency, 2A, integrated switch, synchronous buck (step-down) regulator. The MIC22205 is optimized for highest efficiency, achieving more than 95% efficiency while still switching at 1MHz. The ultra-high speed control loop keeps the output voltage within regulation even under the extreme transient load swings commonly found in FPGAs and low-voltage ASICs. The output voltage is pre-bias safe and can be adjusted down to 0.7V to address all low-voltage power needs.

The MIC22205 offers a full range of sequencing and tracking options. The Enable/Delay (EN/DLY) pin, combined with the Power Good (PG) pin, allows multiple outputs to be sequenced in any way during turn-on and turn-off. The Ramp Control™ (RC) pin allows the device to be connected to another product in the MIC22xxx and/or MIC68xxx family, to keep the output voltages within a certain ΔV on start-up.

The MIC22205 is available in a 12-pin 3mm x 3mm MLF® with a junction operating range from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

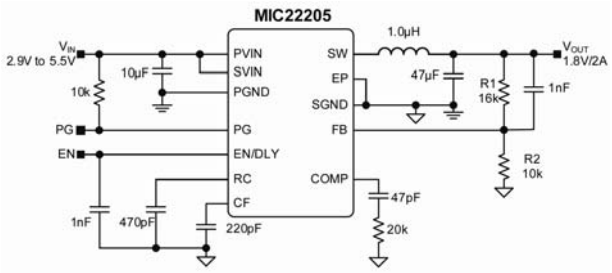
Features

- Input voltage range: 2.9V to 5.5V
- Output voltage adjustable down to 0.7V
- Output load current up to 2A
- Safe start-up into a pre-biased output
- Full sequencing and tracking capability
- Power Good (PG) output
- Efficiency > 95% across a broad load range
- Programmable frequency 300kHz to 4MHz
- Ultra-fast transient response
- Easy RC compensation
- 100% maximum duty cycle
- Fully-integrated MOSFET switches
- Thermal-shutdown and current-limit protection
- 12-pin 3mm x 3mm MLF®
- –40°C to +125°C junction temperature range

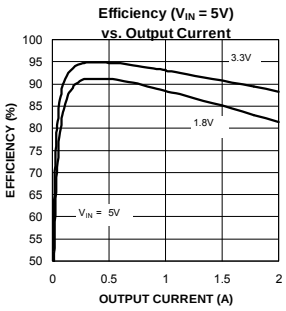
Applications

- High power density point-of-load conversion
- Servers, routers, and base stations
- DVD recorders / Blu-ray players
- Computing peripherals
- FPGAs, DSP, and low-voltage ASIC power

Typical Application



MIC22205 2A 1MHz Synchronous Output Converter



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MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology, Inc.

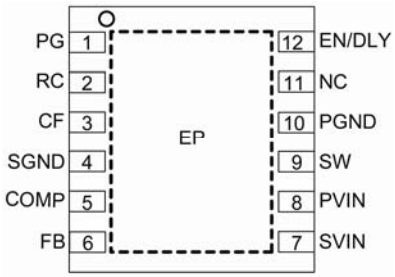
Ordering Information

Part Number	Voltage	Junction Temperature Range	Package[1]	Lead Finish
MIC22205YML	Adjustable	–40° to +125°C	12-Pin 3mm x 3mm MLF®	Pb-Free

Note:

1. MLF® is a GREEN ROHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



12-Pin 3mm x 3mm MLF® (ML)

Pin Description

Pin Number	Pin Name	Description
1	PG	PG (output): This is an open drain output that indicates when the output voltage is below 90% of its nominal voltage. The PG flag is asserted without delay when the enable is set low or when the output goes below the 90% threshold.
2	RC	Ramp Control: A capacitor from the RC pin-to-ground determines slew rate of output voltage during start-up. The RC pin is internally fed with a 1µA current source. The output voltage tracks the RC pin voltage. The slew rate is proportional by the internal 1µA source and the RC pin capacitor. This feature can be used for tracking capability as well as soft start.
3	CF	Adjustable frequency with external capacitor. Refer to Table 2.
4	SGND	Signal Ground: Internal signal ground for all low power circuits.
5	COMP	Compensation Pin (Input): The MIC22205 uses an internal compensation network containing a fixed-frequency zero (phase lead response) and pole (phase lag response) which allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor to the COMP pin will add the necessary pole and zero for voltage mode loop stability using low-value, low-ESR ceramic capacitors.
6	FB	Feedback: Input to the error amplifier. The FB pin is regulated to 0.7V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
7	SVIN	Signal Power Supply Voltage (Input): This pin is connected externally to the PVIN pin. A 2.2µF ceramic capacitor from the SVIN pin to SGND must be placed next to the IC.
8	PVIN	Power Supply Voltage (Input): The PVIN pins are the input supply to the internal P-Channel Power MOSFET. A 10µF ceramic is recommended for bypassing at each PVIN pin. The SVIN pin must be connected to a PVIN pin.
9	SW	Switch (Output): This is the connection to the drain of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high-frequency, high-power connection; therefore traces should be kept as short and as wide as practical.

Pin Description (Continued)

Pin Number	Pin Name	Description
10	PGND	Power Ground: Internal ground connection to the source of the internal N-Channel MOSFETs.
11	NC	No Connect: Leave this pin open. Do not connect to ground or route other signal through this.
12	EN/DLY	Enable/Delay (Input): This pin is internally fed with a 1µA current source from SVIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN/DLY reaches the enable threshold of 1.24V. This pin is pulled low when the input voltage is lower than the UVLO threshold.
EP	GND	Exposed Pad (Power): Must be connected to the GND plane for full output power to be realized.

Absolute Maximum Ratings [1]

PV_{IN} to PGND ..... –0.3V to 6V
SV_{IN} to PGND .....–0.3V to PV_{IN}
V_{SW} to PGND .....–0.3V to PV_{IN}
$V_{EN/DLY}$ to PGND ..... -0.3V to PV_{IN}
V_{PG} to PGND .....–0.3V to PV_{IN}
Junction Temperature ..... 150°C
PGND to SGND ..... –0.3V to 0.3V
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (soldering, 10s)..... 260°C
ESD Rating.....Note 2

Operating Ratings [3]

Supply Voltage (PV_{IN}/SV_{IN}).....2.9V to 5.5V
Power Good Voltage (V_{PG}) ..... 0V to PV_{IN}
Enable Input ($V_{EN/DLY}$) ..... 0V to PV_{IN}
Junction Temperature (T_J).....–40°C ≤ T_J ≤ +125°C
Package Thermal Resistance
3mm x 3mm MLF®-12 (θ_{JC}) ..... 28.7°C/W
3mm x 3mm MLF®-12 (θ_{JA}) ..... 40°C/W

Electrical Characteristics [4]

SV_{IN} = PV_{IN} = $V_{EN/DLY}$ = 3.3V, V_{OUT} = 1.8V, T_A = 25°C, unless noted. Bold values indicate –40°C< T_J < +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Input Supply					
Input Voltage Range (PV_{IN})		**2.9**		**5.5**	V
Under-Voltage Lockout Trip Level	PV_{IN} rising	**2.55**	2.719	**2.9**	V
UVLO Hysteresis			418		mV
Quiescent Supply Current	V_{FB} = 0.9V (not switching)		1.3	**2**	mA
Shutdown Current	$V_{EN/DLY}$ = 0V		5	**10**	µA
Reference					
Feedback Reference Voltage		**0.686**	0.7	**0.714**	V
Load Regulation	I_{OUT} = 100mA to 2A		0.2		%
Line Regulation	V_{IN} = 2.9V to 5.5V; I_{OUT} = 100mA		0.2		%
FB Bias Current	V_{FB} = 0.5V		1		nA
Enable Control					
EN/DLY Threshold Voltage		**1.14**	1.24	**1.34**	V
EN Hysteresis			12		mV
EN/DLY Bias Current	$V_{EN/DLY}$ = 0.5V; V_{IN} = 2.9V and V_{IN} = 5.5V	**0.6**	1.0	**1.8**	µA
RC Ramp Control					
RC Pin Source Current	V_{RC} = 0.35V	0.5	1.0	1.7	µA
Oscillator					
Switching Frequency		**0.8**	1.0	**1.2**	MHz
Maximum Duty Cycle	V_{FB} ≤ 0.5V	100			%
Short Current Protection					
Current Limit	V_{FB} = 0.5V	**2**	5.5	**8**	A
Internal FETs					
Top MOSFET $R_{DS(ON)}$	V_{FB} = 0.5V, I_{SW} = 1A		180		mΩ
Bottom MOSFET $R_{DS(ON)}$	V_{FB} = 0.9V, I_{SW} = -1A		100		mΩ

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended.
3. The device is not guaranteed to function outside its operating rating.
4. Specification for packaged product only.

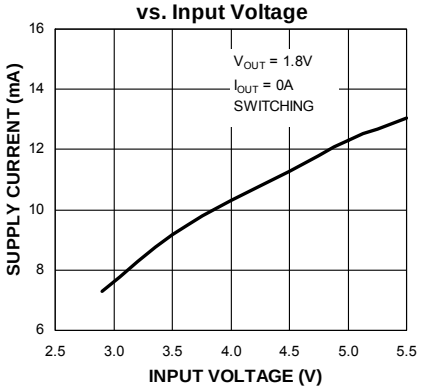
Electrical Characteristics [4] (Continued)

SV_{IN} = PV_{IN} = $V_{EN/DLY}$ = 3.3V, V_{OUT} = 1.8V, T_A = 25°C, unless noted. Bold values indicate –40°C< T_J < +125°C.

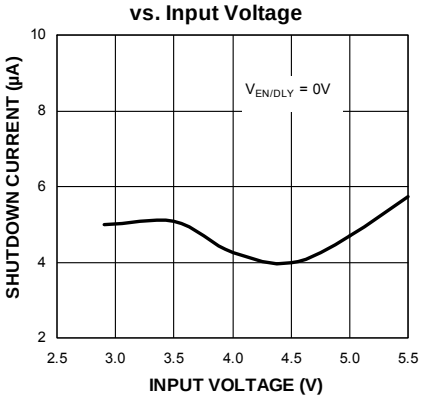
Parameter	Condition	Min.	Typ.	Max.	Units
Power Good (PG)					
PG Threshold	Threshold % of V_{FB} from V_{REF}	**–7.5**	–10	**–12.5**	%
Hysteresis			2.843		%
PG Output Low Voltage	I_{PG} = 5mA (sinking), $V_{EN/DLY}$ = 0V		139		mV
PG Leakage Current	V_{PG} = 5.5V; V_{FB} = 0.9V			1.0 **2.0**	µA
Over-Temperature Shutdown	T_J Rising		151		°C
Over-Temperature Shutdown Hysteresis			16		°C

Typical Characteristics

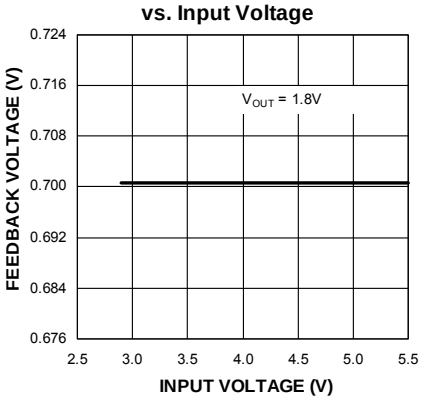
V_{IN} Operating Supply Current vs. Input Voltage



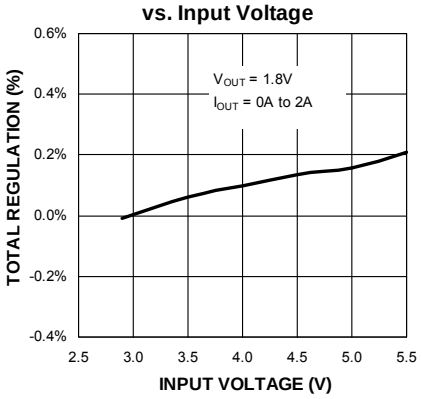
V_{IN} Shutdown Current vs. Input Voltage



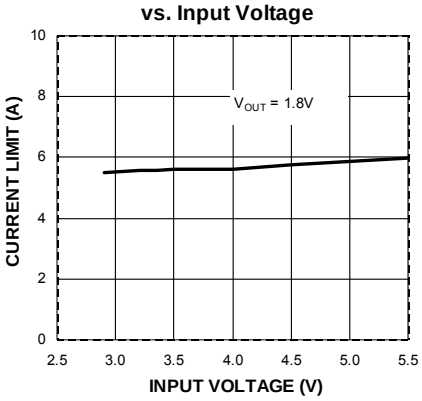
Feedback Voltage vs. Input Voltage



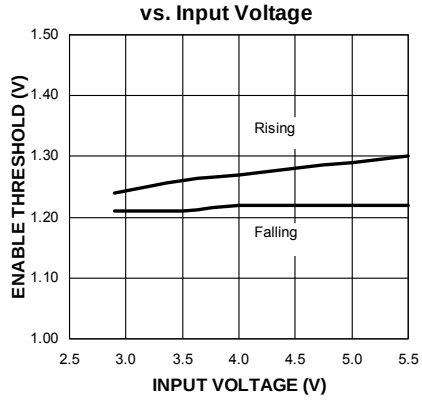
Load Regulation vs. Input Voltage



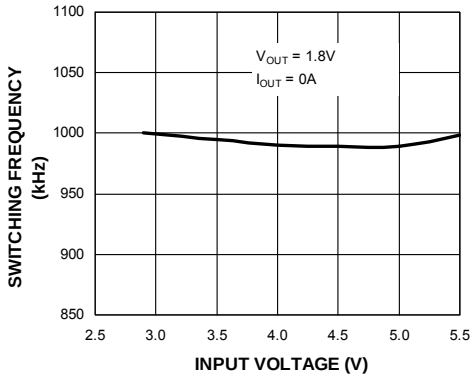
Current Limit vs. Input Voltage



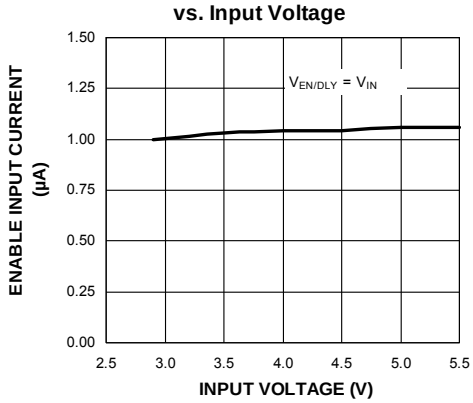
Enable Threshold vs. Input Voltage



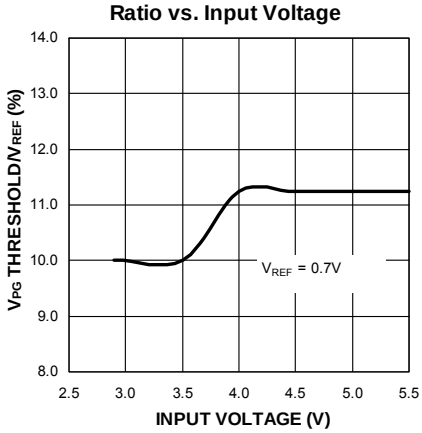
Switching Frequency vs. Input Voltage



Enable Input Current vs. Input Voltage

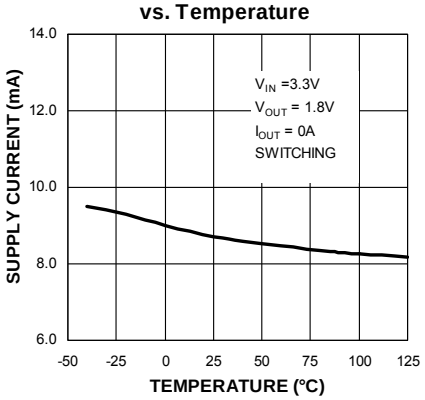


Power Good Threshold/VREF Ratio vs. Input Voltage

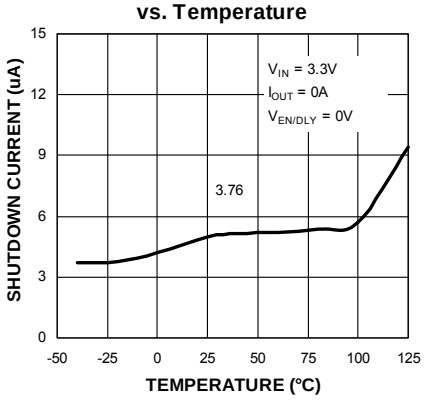


Typical Characteristics (Continued)

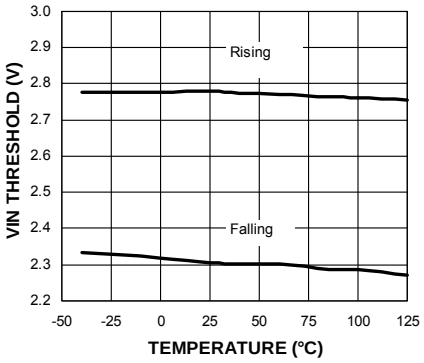
V_{IN} Operating Supply Current vs. Temperature



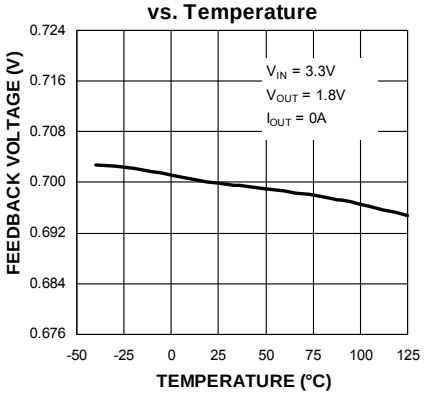
V_{IN} Shutdown Current vs. Temperature



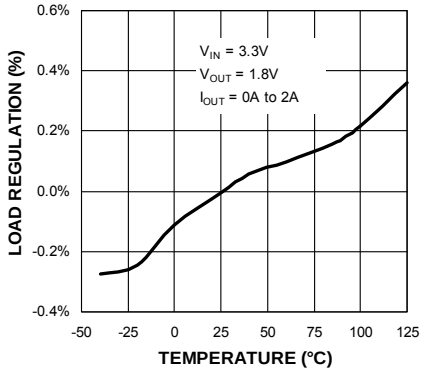
VIN UVLO Threshold vs. Temperature



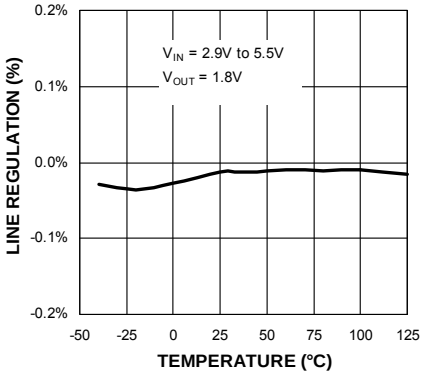
Feedback Voltage vs. Temperature



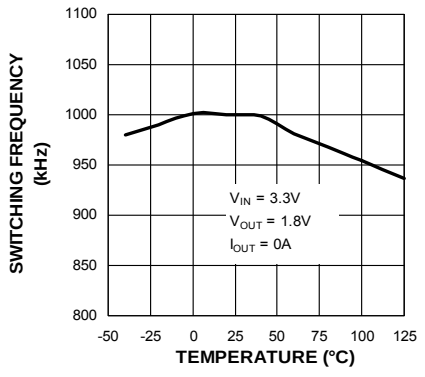
Load Regulation vs. Temperature



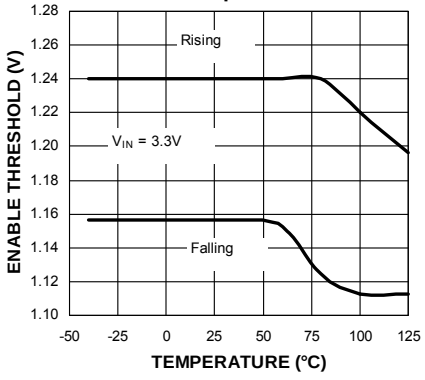
Line Regulation vs. Temperature



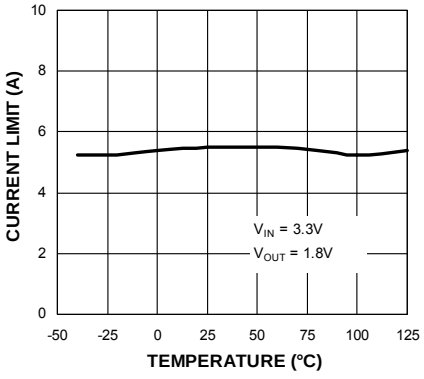
Switching Frequency vs. Temperature



Enable Threshold vs. Temperature

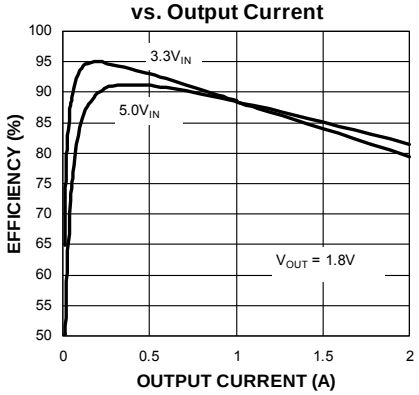


Current Limit vs. Temperature

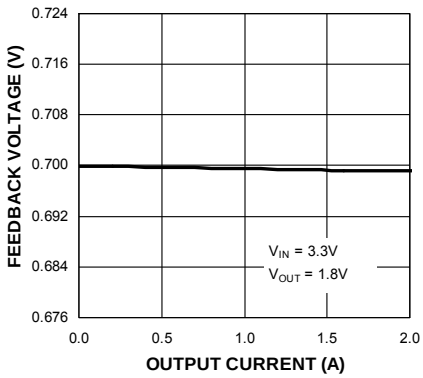


Typical Characteristics (Continued)

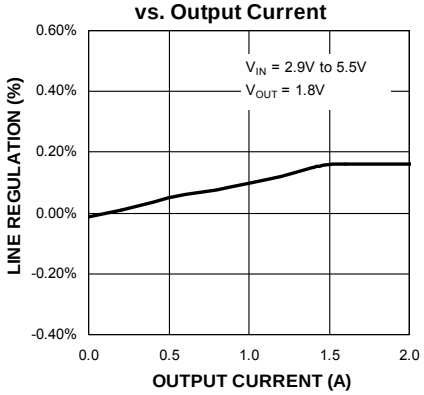
Efficiency vs. Output Current



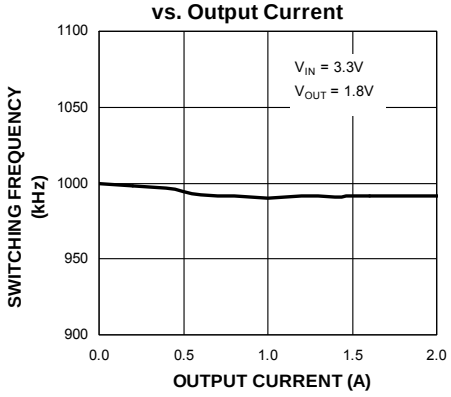
Feedback Voltage vs. Output Current



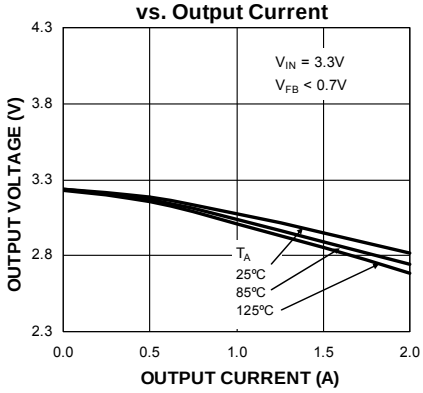
Line Regulation vs. Output Current



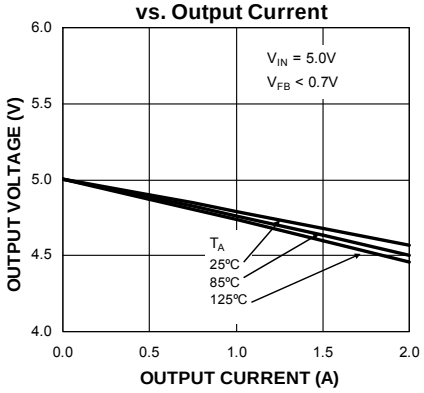
Switching Frequency vs. Output Current



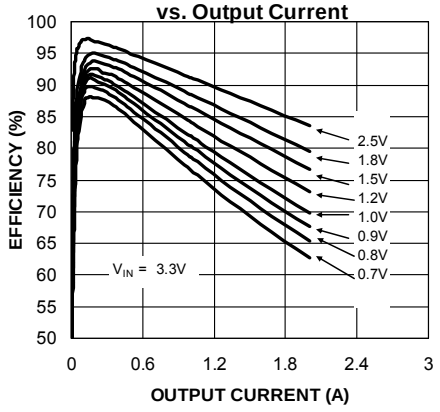
Output Voltage (V_{IN} = 3.3V) vs. Output Current



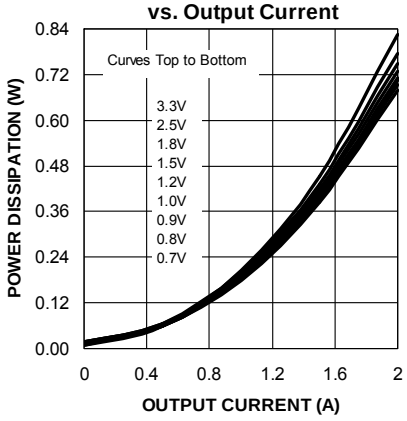
Output Voltage (V_{IN} = 5.0V) vs. Output Current



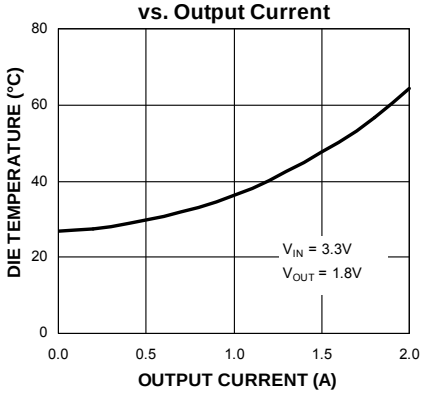
Efficiency (V_{IN} = 3.3V) vs. Output Current



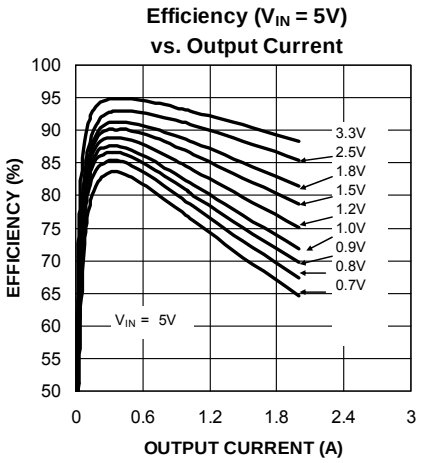
IC Power Dissipation (VIN = 3.3V) vs. Output Current

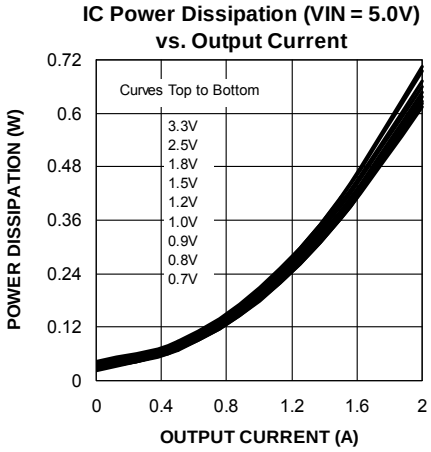


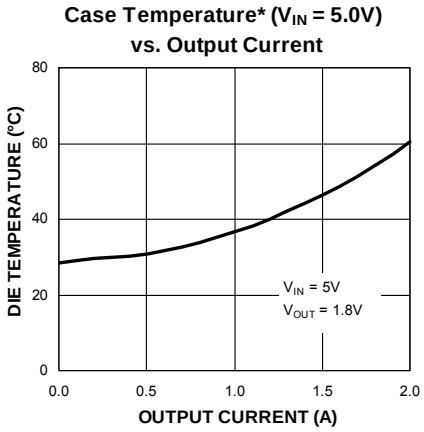
Case Temperature* (V_{IN} = 3.3V) vs. Output Current



Typical Characteristics (Continued)



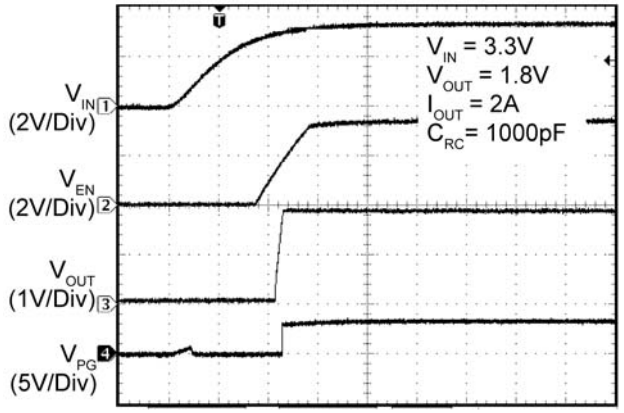




Die Temperature* : The temperature measurement was taken at the hottest point on the MIC22205 case and mounted on a five-square inch PCB (see *Thermal Measurement*s section). Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat-emitting components.

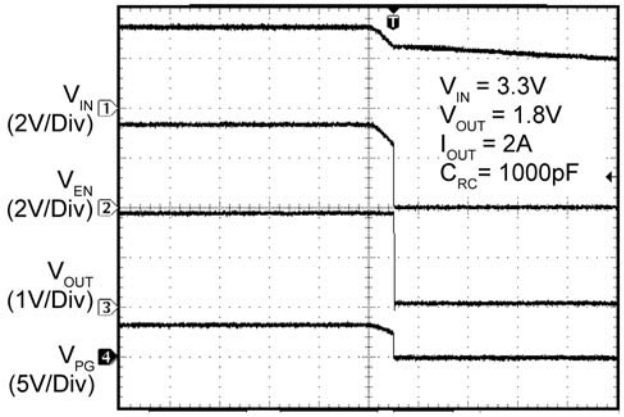
Functional Characteristics

V_{IN} Turn-On



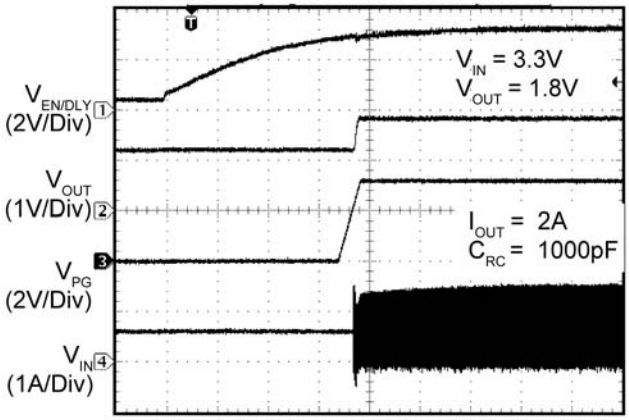
4.0ms/Div

V_{IN} Turn-Off



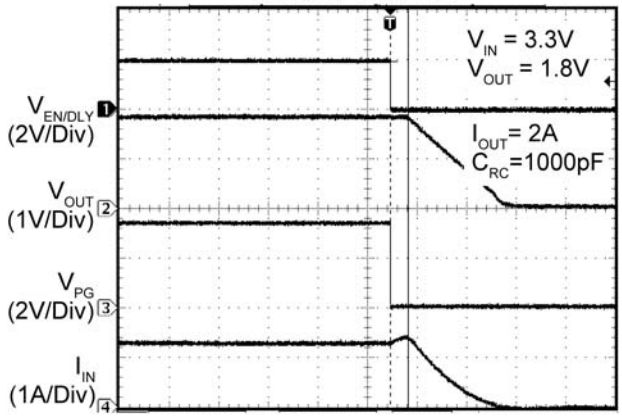
4.0ms/Div

Enable Turn-on Delay and Rise Time



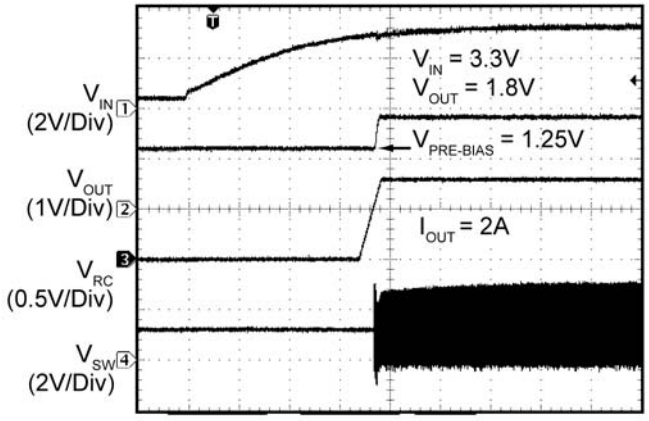
400us/Div

Enable Turn-Off



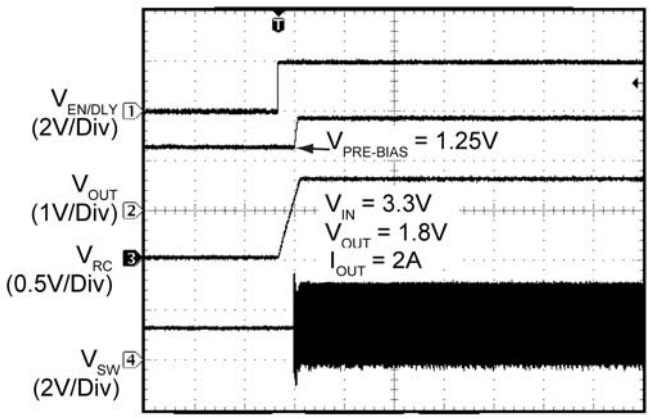
400us/Div

V_{IN} Start-up with Pre-Biased Output



2ms/Div

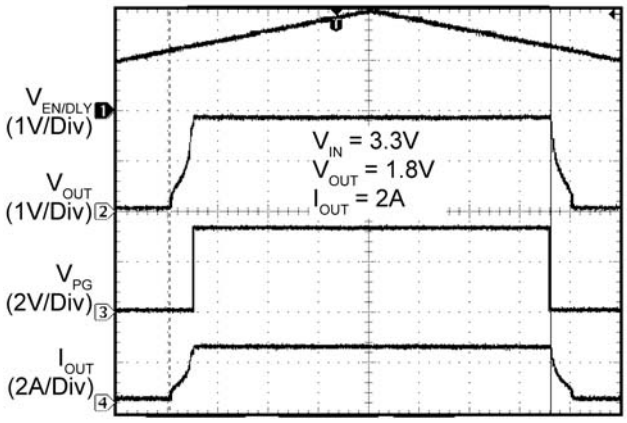
Enable Start-up with Pre-Biased Output



2ms/Div

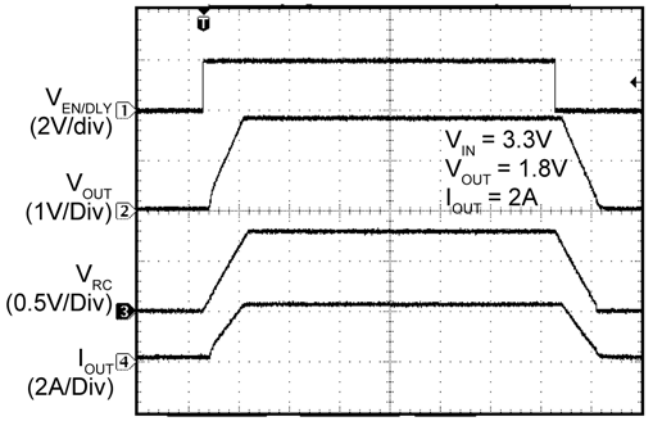
Functional Characteristics (Continued)

Enable Threshold



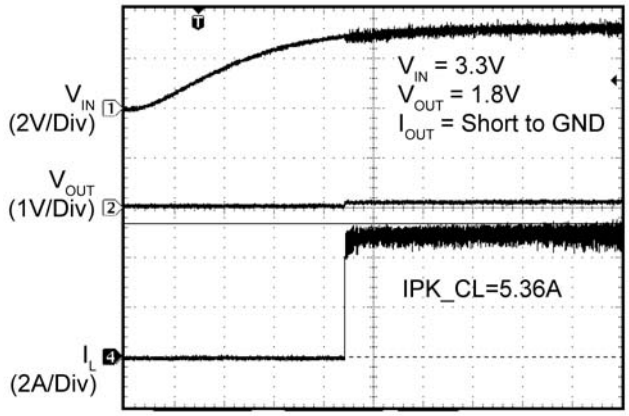
100ms/Div

Enable Turn-On/Off



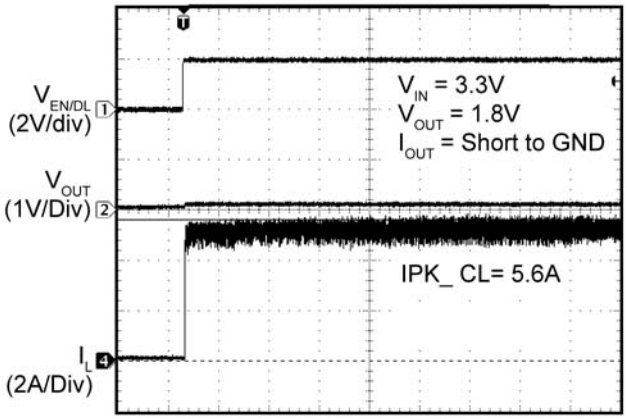
1ms/Div

Power Up into Short Circuit



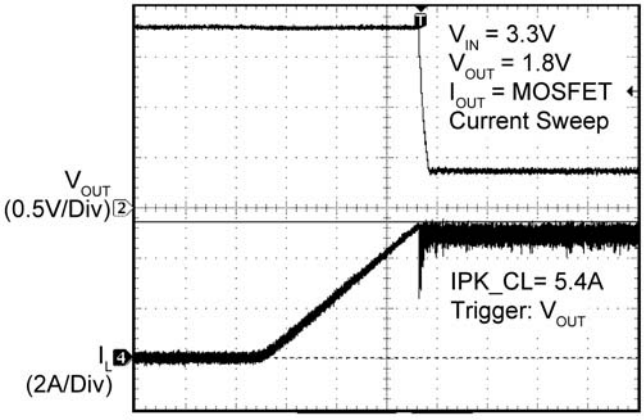
2ms/Div

Enabled into Short Circuit



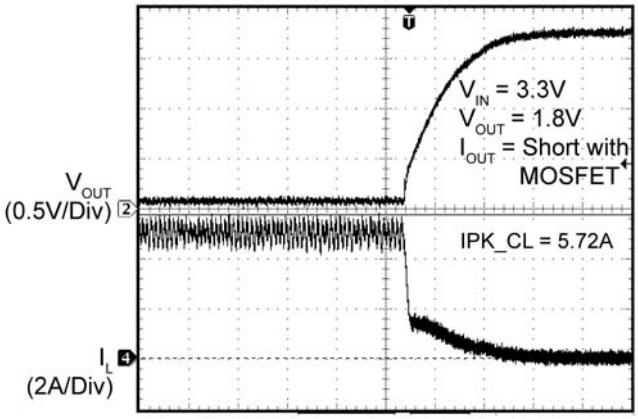
4ms/Div

Output Current Limit Threshold



400us/Div

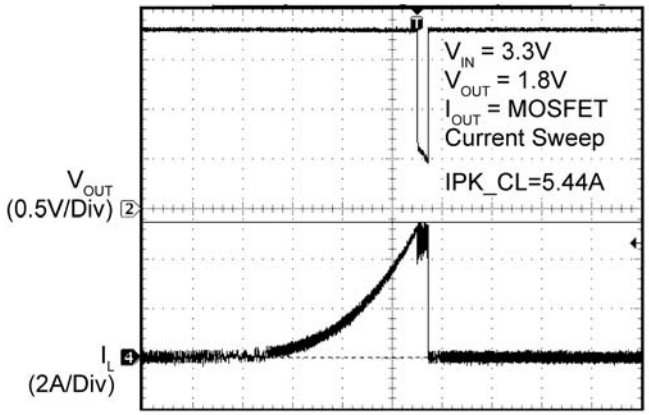
Output Recovery from Short Circuit



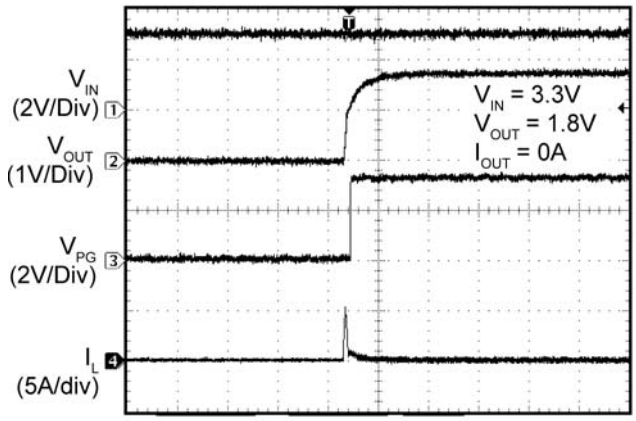
40us/Div

Functional Characteristics (Continued)

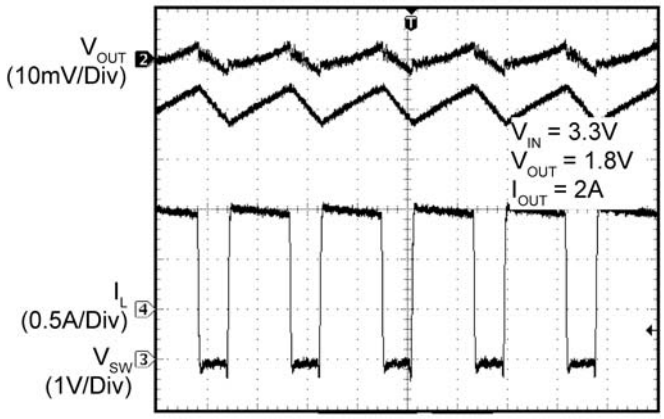
Peak Current Limit Threshold



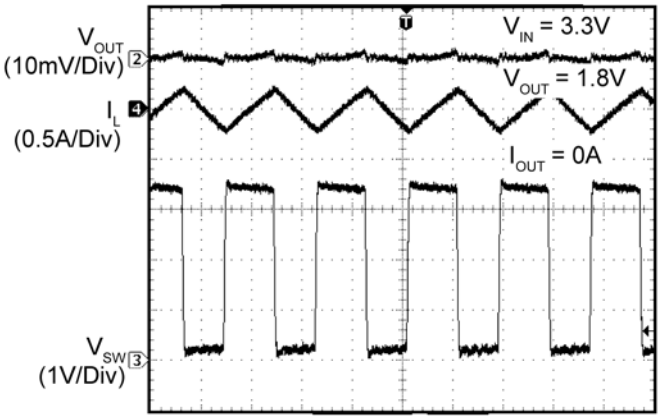
Thermal Shutdown Recovery



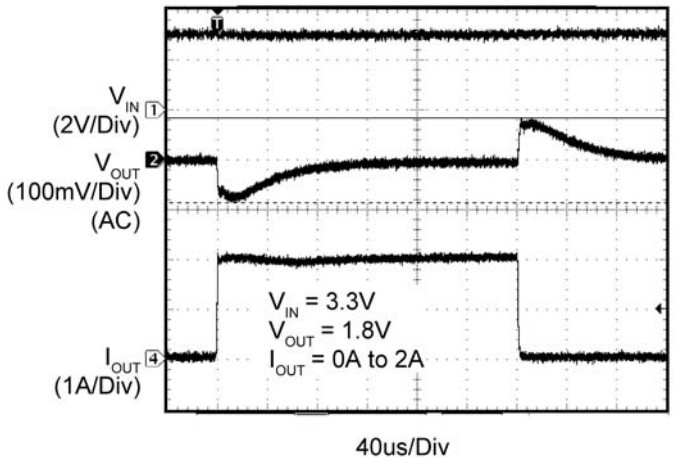
Switching Waveforms, I_{OUT}=2A



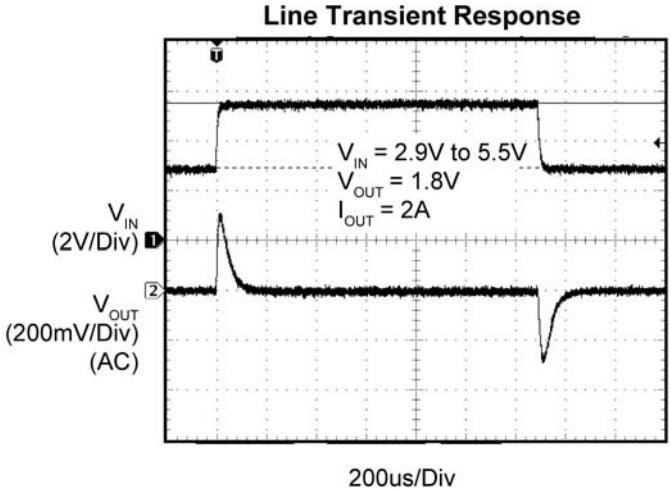
Switching Waveforms, I_{OUT}=0A



Load Transient Response



Line Transient Response



Functional Diagram

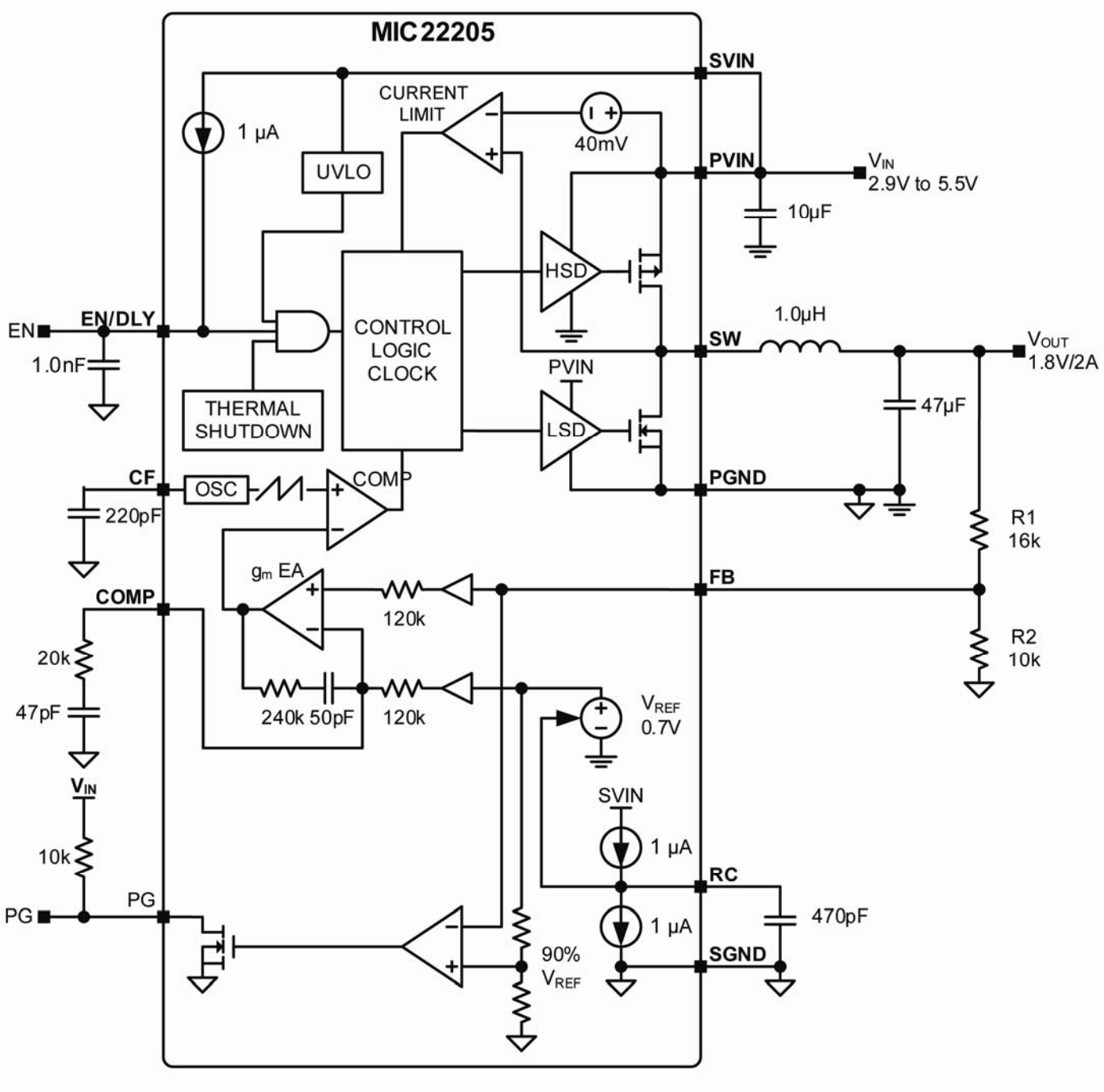


Figure 1. MIC22205 Functional Diagram

Application Information

The MIC22205 is a 2A, synchronous voltage mode, PWM step down regulator IC with a programmable frequency range from 300kHz to 4MHz. Other features include tracking and sequencing control for controlling multiple output power systems and power good (PG).

By controlling the ratio of the on-to-off time, or duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22205 will run at 100% duty cycle.

The internal MOSFETs include a high-side P-channel MOSFET from the input supply to the switch pin, and an N-channel MOSFET from the switch pin to ground. Since the low-side N-channel MOSFET provides the current during the off cycle, a very low amount of power is dissipated during the off period.

The PWM control technique also provides adjustable fixed-frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

Component Selection

Input Capacitor

A 10µF X5R or X7R dielectrics ceramic capacitor is recommended on each of the PVIN pins for bypassing. A Y5V dielectric capacitor should not be used. Aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high-frequency noise.

Output Capacitor

The MIC22205 was designed specifically for use with ceramic output capacitors. The output capacitor can be increased from 47µF to a higher value to improve transient performance. The MIC22205 operates in voltage mode, so the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of a wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22205.

Inductor Selection

Inductor selection will be determined by the following (not in order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC22205 is designed for use with a 0.47µH to 4.7µH inductor.

Maximum current ratings of the inductor are generally given using two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise, or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so the peak current will not saturate the inductor. The ripple current can add as much as 1.2A to the output current level. Choose an RMS rating that is equal to or greater than the current limit of the MIC22205 to prevent overheating in a fault condition. For best electrical performance, place the inductor very close to the SW nodes of the IC. The heat of the inductor is somewhat coupled to the IC, so it offers some level of protection if the inductor gets too hot (**In such cases IC case temperature is not a true indication of IC dissipation**). It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height necessary to fit a particular design. Please refer to the inductor dimensions on the manufacturer's datasheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR increase can represent a significant efficiency loss. Refer to the "Efficiency Considerations" section below for a more detailed description.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed.

$$\text{Efficiency } \% = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. First, it decreases power dissipation in the power supply, which reduces the need for heat sinks and thermal design considerations; also, it decreases the consumption of current for battery-powered applications. Reduced current demand from a battery increases the device's operating time, which is critical in hand-held devices.

There are mainly two loss terms in switching converters: static losses and switching losses. Static losses are the power losses due to VI or I^2R. For example, power is dissipated in the high side switch during the on cycle. Power loss is equal to the high-side MOSFET $RDS_{(ON)}$ multiplied by the RMS switch current squared (I_{SW}^2). During the off-cycle, the low-side N-channel MOSFET conducts, which also dissipates power. Similarly, the inductor's DCR and capacitor's ESR also contribute to I^2R losses. A device's operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The current required to drive the gates on and off at a constant 1MHz frequency, and the switching transitions make up the switching losses.

Figure 2 illustrates a typical efficiency curve. From 0A to 0.2A, efficiency losses are dominated by quiescent current losses, gate drive, transition, and core losses. In this case, lower supply voltages yield greater efficiency because they require less current to drive the MOSFETs, and have reduced input power consumption.

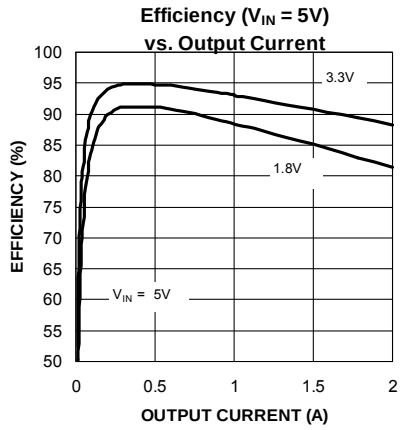


Figure 2. Efficiency Curve

From 0.5A to 2A, efficiency loss is dominated by MOSFET $RDS_{(ON)}$ and inductor DC losses. Higher input supply voltages will increase the gate-to-source voltage on the internal MOSFETs, thereby reducing the internal $RDS_{(ON)}$. This improves efficiency by decreasing DC losses in the device. All but the inductor losses are inherent to the device. In this case, inductor selection is critical for efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L_{PD} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{(V_{OUT} \times I_{OUT}) + L_{PD}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads, and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor in losses. When light load efficiencies become more critical, a larger inductor value may be desired. Larger inductances reduce the peak-to-peak inductor ripple current, which minimize losses.

Compensation

The MIC22205 has a combination of internal and external stability compensation to simplify the circuit for small, high efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal ramp signal, and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100kHz-200kHz, the MIC22205 is capable of extremely fast transient response.

The MIC22205 is designed to be stable with a typical application using a 1µH inductor and a 47µF ceramic (X5R) output capacitor. These values can be varied, depending on the size, cost, and efficiency, and still keep the LC natural frequency $\left(\frac{1}{2\times\pi\times\sqrt{L\times C}}\right)$ less than 26 kHz to ensure stability. The minimum recommended inductor value is 0.47µH and minimum recommended output capacitor value is 22µF. The trade-off with changing these values is that with a larger inductor, there is a reduced peak-to-peak current, which yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold-up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 20k resistor) are shown in Table 1:

C→ / L↓	22µF – 47µF	47µF – 100µF	100µF – 470µF
0.47µH	0* – 10pF	22pF	33pF
1µH	0† – 15pF	15 – 22pF	33pF
2.2µH	15 – 33pF	33 – 47pF	100 – 220pF
* VOUT > 1.2V, † VOUT > 1V			

Note: Compensation values for various output voltages and inductor values refer to Table 3.

Table 1. Compensation Capacitor Selection

Feedback

The MIC22205 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage, and adjusts the output voltage to maintain regulation. The resistor divider network for a desired V_{OUT} is given by:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

where V_{REF} is 0.7V and V_{OUT} is the desired output voltage. A 10kΩ or lower resistor value from the output to the feedback (R1) is recommended, since large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small capacitor (50pF – 100pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

Enable/Delay (EN/DLY) Pin

Enable/Delay (EN/DLY) sources 1µA out of the IC to allow a startup delay to be implemented. The delay time is the time it takes 1µA to charge $C_{EN/DLY}$ to 1.25V. Therefore:

$$t_{EN/DLY} = \frac{1.24\times C_{EN/DLY}}{1\times 10^{-6}}$$

CF Capacitor

Adding a capacitor to this pin can adjust the switching frequency from 800kHz to 4MHz. CF sources 400µA out of the IC to charge the CF capacitor in order to set up the switching frequency. The switch period is the time it takes 400µA to charge CF to 1.0V. Therefore:

CF Capacitor	Frequency
56pF	4.4MHz
68pF	4MHz
82pF	3.4MHz
100pF	2.8MHz
150pF	2.1MHz
180pF	1.7MHz
220pF	1.4MHz
270pF	1.2MHz
330pF	1.1MHz
390pF	1.05MHz
470pF	1MHz

Table 2. CF vs. Frequency

It is necessary to connect the CF capacitor very close between the CF pin and signal ground.

300kHz to 800kHz Operation

The frequency range can be lowered by adding an additional resistor (R_{CF}) in parallel with the CF capacitor. This reduces the amount of current used to charge the capacitor, which reduces the frequency. The following equation can be used to for frequencies between 800kHz to 300kHz:

$$-R_{CF} x C_{CF} x \ln\left(1 + \frac{1.0V}{400\mu A \times R_{CF}}\right) = t$$

$$R_{CF} > 2.9K\Omega$$

RC Pin (Soft-Start)

The RC pin provides a trimmed 1µA current source/sink for accurate ramp-up (soft-start). This allows the MIC22205 to be used in systems that require voltage tracking or ratio-metric voltage tracking at startup.

There are two ways of using the RC pin:

1. Externally driven from a voltage source
2. Externally attached capacitor sets output ramp-up/down rate

In the first case, driving RC with a voltage from 0V to V_{REF} will program the output voltage between 0 and 100% of the nominal set voltage, as shown in Figure 3.

In the second case, the external capacitor sets the ramp-up and ramp-down time of the output voltage. The time is given by:

$$t_{RAMP} = \frac{0.7 \times C_{RC}}{1 \times 10^{-6}}$$

where t_{RAMP} is the time from 0 to 100% nominal output voltage.

During start-up, a light load condition (I_{OUT} < 1.25A) can lead to negative inductor current. Under these conditions, the maximum ramp-up time should not exceed the critical ramp-up time period. This will keep the regulator in continuous mode operation when V_{FB} reaches 90% of reference voltage.

Beyond the critical ramp-up time, the regulator is in discontinuous mode, which leads to prolonged N-channel MOSFET conduction, which in turn causes negative inductor current.

The maximum C_{RC} value is calculated as follows:

$$C_{RC} < \frac{2.86 \bullet C_{OUT} \bullet L \bullet F_{SW} \bullet 10^{-6}}{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

Pre-Bias Start-Up

The MIC22205 is designed for safe start-up into a pre-biased output. This prevents large negative inductor currents and excessive output voltage oscillations. The MIC22205 starts with the low-side MOSFET turned off, preventing reverse inductor current flow. The synchronous MOSFET stays off until the Power Good (PG) goes high after the V_{FB} is above 90 percent of V_{REF}.

A pre-bias condition can occur if the input is turned off, and then immediately turned back on before the output capacitor is discharged to ground. It is also possible that the output of the MIC22205 could be pulled up or pre-biased through parasitic conduction paths from one supply rail to another in multiple voltage (VOUT) level ICs such as a FPGA.

Figure 3 shows a normal start-up waveform. A 1µA current source charges the soft-start capacitor C_{RC}. The C_{RC} capacitor forces the V_{RC} voltage to come up slowly (V_{RC} trace), which provides a soft-start ramp. This ramp is used to control the internal reference (V_{REF}). The error amplifier forces the output voltage to follow the V_{REF} ramp from zero to the final value.

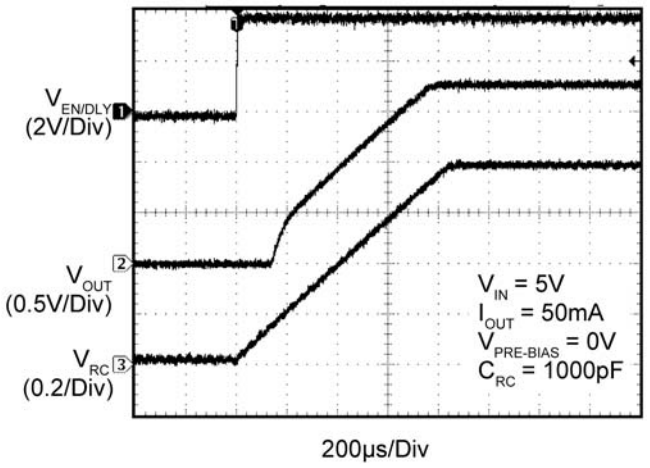


Figure 3. EN Turn-On Time – Normal Start-Up

If the output is pre-biased to a voltage above the expected value, as shown in Figure 4, then neither MOSFET will turn on until the ramp control voltage (V_{RC}) is above the reference voltage (V_{REF}). Then, the high-side MOSFET starts switching, forcing the output to follow the V_{RC} ramp. Once the feedback voltage is above 90 percent of the reference voltage, the low-side MOSFET will begin switching.

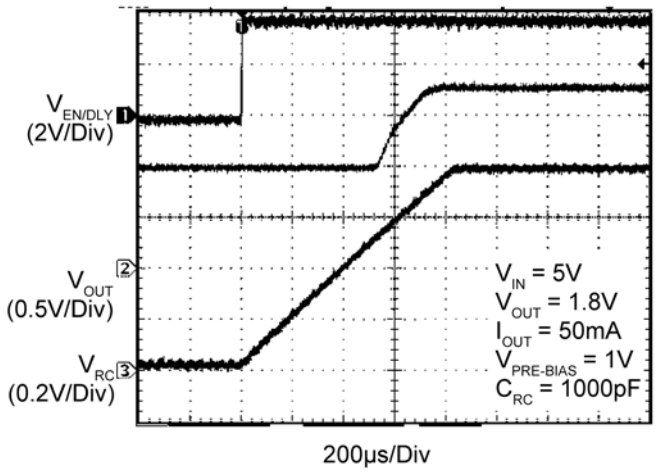


Figure 4. EN Turn-On at 1V Pre-Bias

When the MIC22205 is turned off, the low-side MOSFET will be disabled, and the output voltage will decay to zero. During this time, the ramp control voltage (V_{RC}) will still control the output voltage fall-time with the high-side MOSFET, if the output voltage falls faster than the V_{RC} voltage. Figure 5 shows this operating condition. Here, a 2A load pulls the output down fast enough to force the high-side MOSFET on (V_{SW} trace).

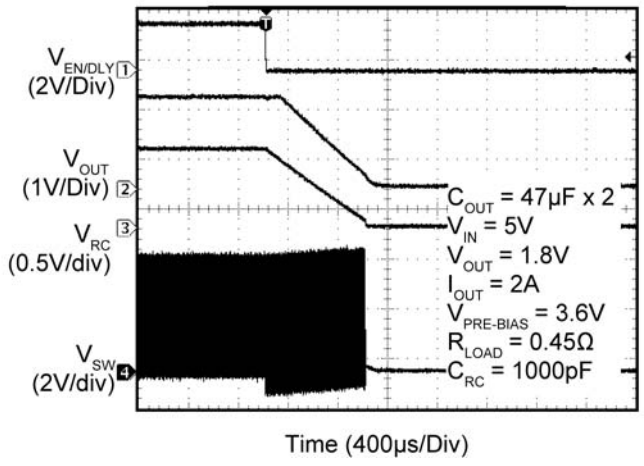


Figure 5. EN Turn-OFF – 2A Load

If the output voltage falls slower than the V_{RC} voltage, then the both MOSFETs will be off and the output will decay to zero as shown in the V_{OUT} trace in Figure 6 with both MOSFETs off, any resistive load connected to the output will help pull down the output voltage. This will occur at a rate determined by the resistance of the load and the output capacitance.

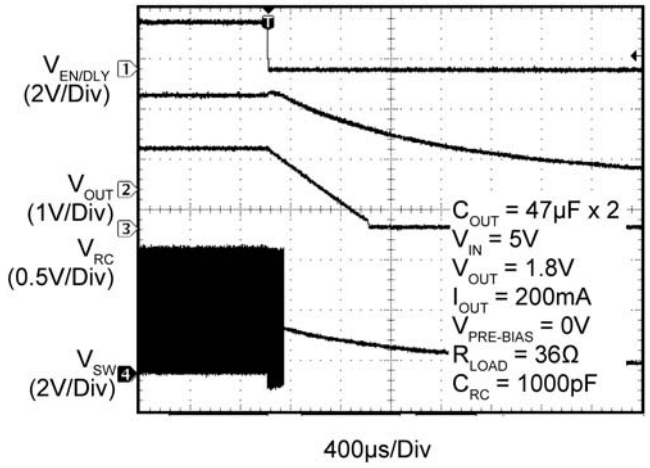


Figure 6. EN Turn-Off – 200mA Load

Current Limit

The MIC22205 uses a two-stage technique to protect against overload. The first stage is to limit the current in the P-channel switch; the second is over temperature shutdown.

Current is limited by measuring the current through the high-side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

The circuit in Figure 7 describes the operation of the current limit circuit. Since the actual RDS_{ON} of the P-channel MOSFET varies from part to part and with changes in temperature and input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current which is a directly proportional to the factory set current limit. This sets the current limit as a current ratio and thus, is not dependant upon the RDS_{ON} value. Current limit is set to nominal value. Variations in the scale factor K between the power PFET and the reference PFET used to generate the limit threshold account for a relatively small inaccuracy.

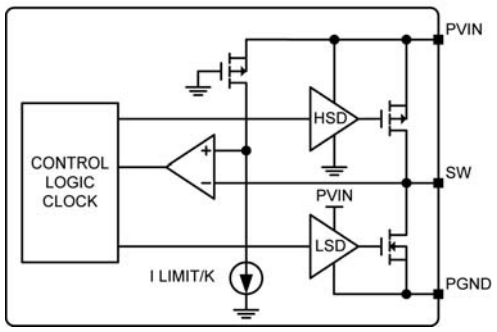


Figure 7. Current-Limit Detail

Thermal Considerations

The MIC22205 is packaged in a MLF® 3mm x 3mm – a package that has excellent thermal-performance equaling that of larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePad), which connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

$$T_J = T_{AMB} + P_{DISS} \times R\theta_{JA}$$

where:

- P_{DISS} is the power dissipated within the MLF® package and is at 2A load. $R\theta_{JA}$ is a combination of junction-to-case thermal resistance ($R\theta_{JC}$) and Case-to-Ambient thermal resistance ($R\theta_{CA}$), since thermal resistance of the solder connection from the ePAD to the PCB is negligible; $R\theta_{CA}$ is the thermal resistance of the ground plane-to-ambient, so $R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$.
- T_{AMB} is the operating ambient temperature.

Example:

The Evaluation board has two copper planes contributing to an $R\theta_{JA}$ of approximately 40ºC/W. The worst case $R\theta_{JC}$ of the MLF 3mm x 3mm is 28.7ºC/W.

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$$
$$R\theta_{JA} = 28.7 + 11.3 = 40^{\circ}C/W$$

To calculate the junction temperature for a 50°C ambient:

$$T_J = T_{AMB} + P_{DISS} \cdot R\theta_{JA}$$
$$T_J = 50 + (0.72 \times 40)$$
$$T_J = 78.8°C$$

This is below the maximum of 125°C.

Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. The most common mistake made is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22-gauge, and behaves like a heat-sink, resulting in a lower case measurement.

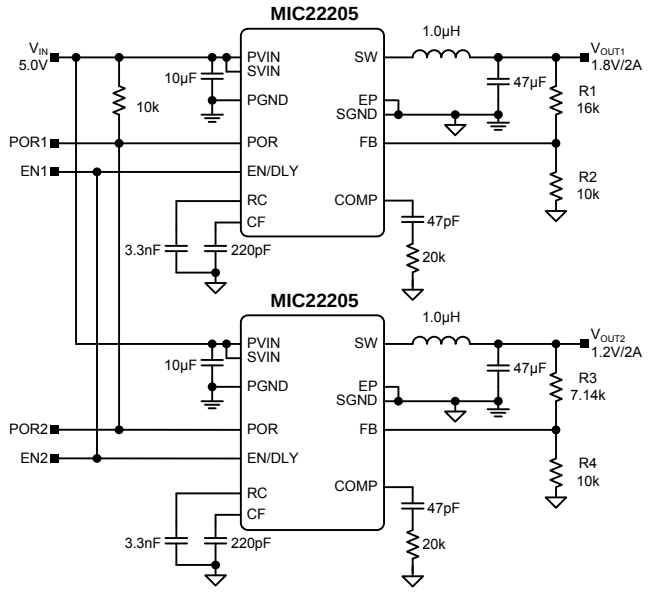
Two better methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36-gauge wire or higher (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to ensure the thermal couple junction makes good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

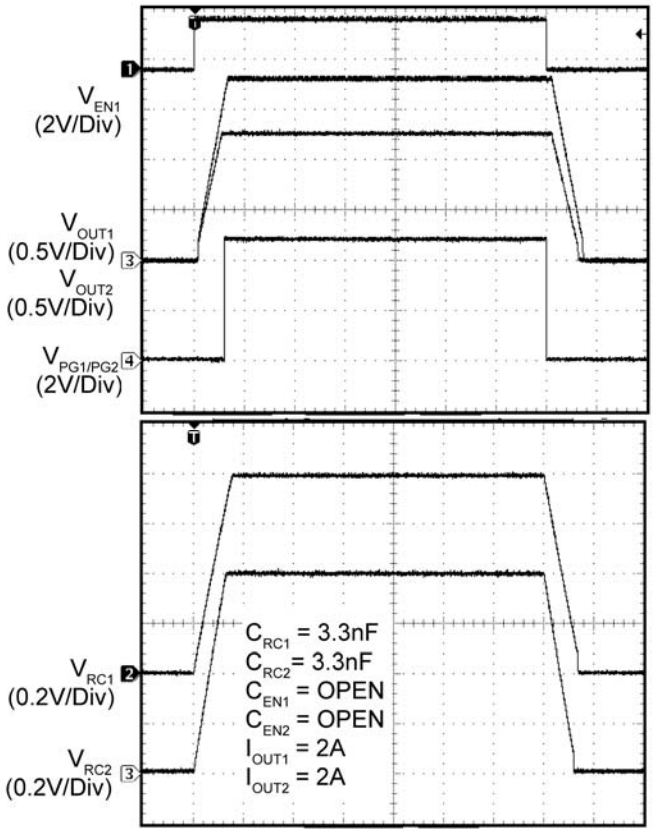
Whenever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, an IR thermometer from Optris has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. Using a stand makes it easier to hold the beam on the IC for long periods of time.

Sequencing and Tracking

There are four variations of sequencing and tracking that are easily implemented using the MIC22205. The two sequencing variations are Delayed and Windowed. The two tracking variants are Normal and Ratio Metric. The following diagrams illustrate methods for connecting two MIC22205's to achieve these requirements.

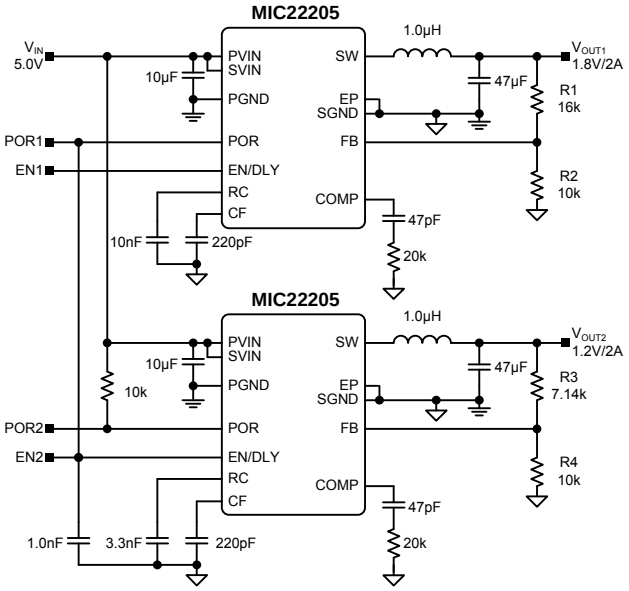
Window Sequencing:

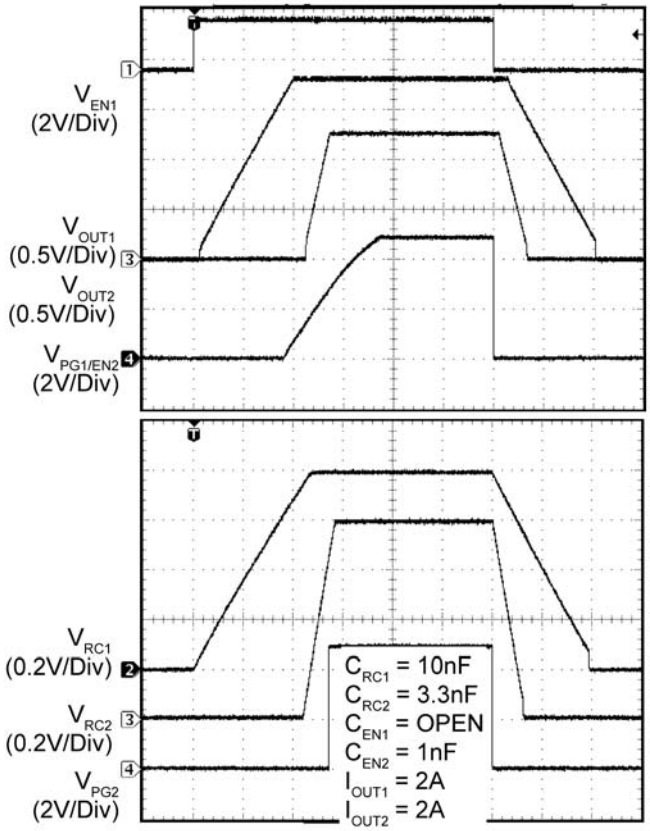




4.0ms/Div

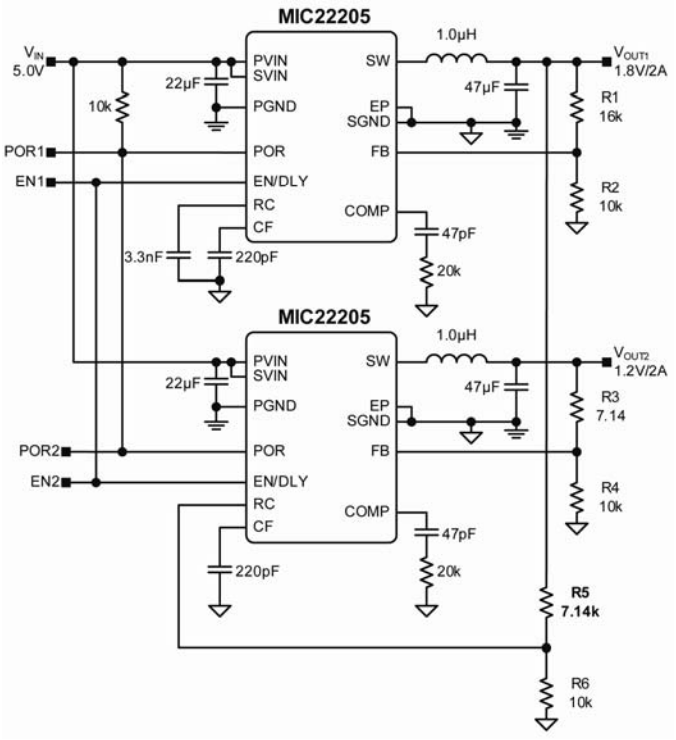
Delayed Sequencing:

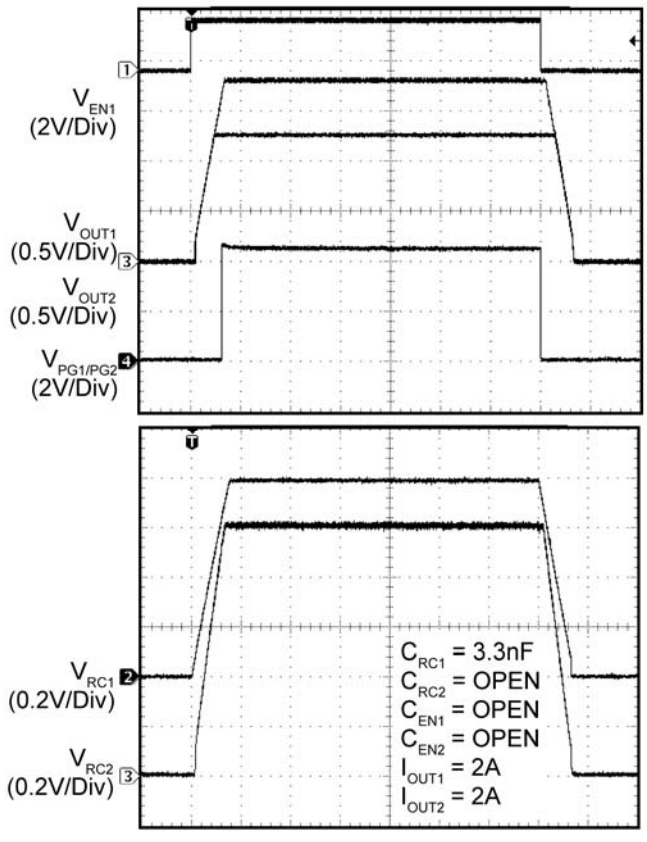




4.0ms/Div

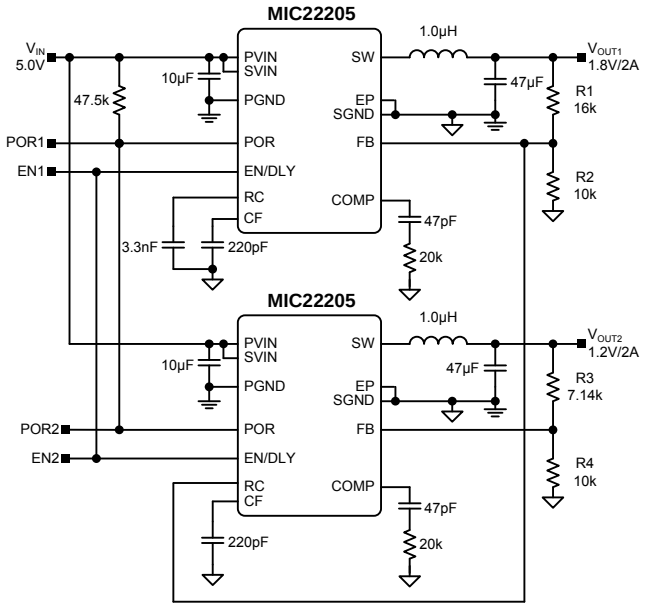
Normal Tracking:

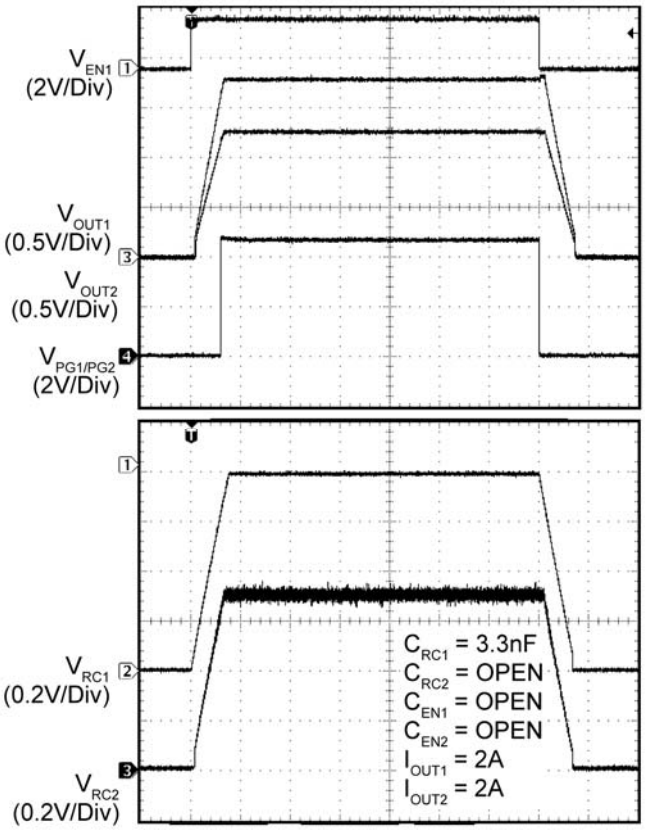




4.0ms/Div

Ratio Metric Tracking:





4.0ms/div

V_{IN} = 5V								
V_{OUT}	L	C_{OUT}	C_{COMP}	R_{COMP}	C_{FF}	R_{FF}	C_{FB}	R_{FB}
1.1V	3.3µH	2 x 47µF	100pF	5kΩ	N.U.	4.7kΩ	100pF	8.2kΩ
1.3V	1.5µH	2 x 47µF	100pF	5kΩ	1nF	4.7kΩ	100pF	5.49kΩ
1.8V	2.2µH	2 x 47µF	100pF	5kΩ	1nF	4.7kΩ	100pF	3.0kΩ
4.2V	1.5µH	2 x 47µF	100pF	20kΩ	1nF	4.7kΩ	100pF	953Ω

Table 3. Compensation Selection

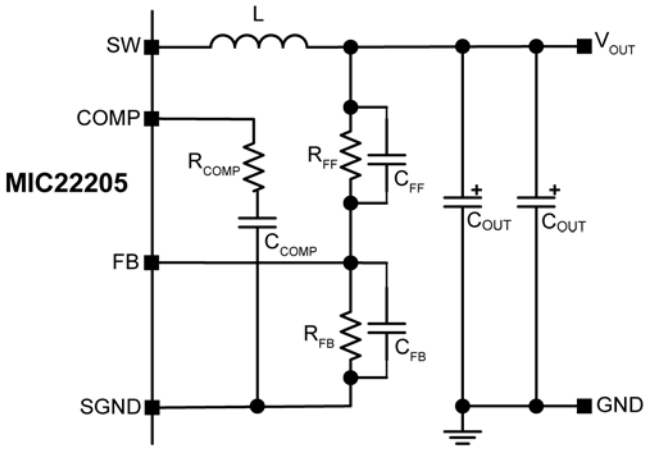


Figure 8. Schematic Reference

PCB Layout Guidelines

IMPORTANT: To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieving reliable, stable and efficient performance. A ground plane is required to control EMI, and to minimize the inductance in power, signal, and return paths.

Follow these guidelines to ensure proper operation of the MIC22205 converter:

IC

- The 2.2µF ceramic capacitor, which is connected to the SVIN pin, must be located right at the IC. The SVIN pin is noise sensitive, so placement of the capacitor is critical. Use wide traces to connect to the SVIN and SGND pins.
- The signal ground pin (SGND) must be connected directly to the ground planes. Do not route the SGND pin to the PGND pad on the top layer.
- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- A 10µF X5R or X7R dielectrics ceramic capacitor is recommended on the PVIN pin for bypassing.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications, and the operating voltage must be de-rated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply when power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom, as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

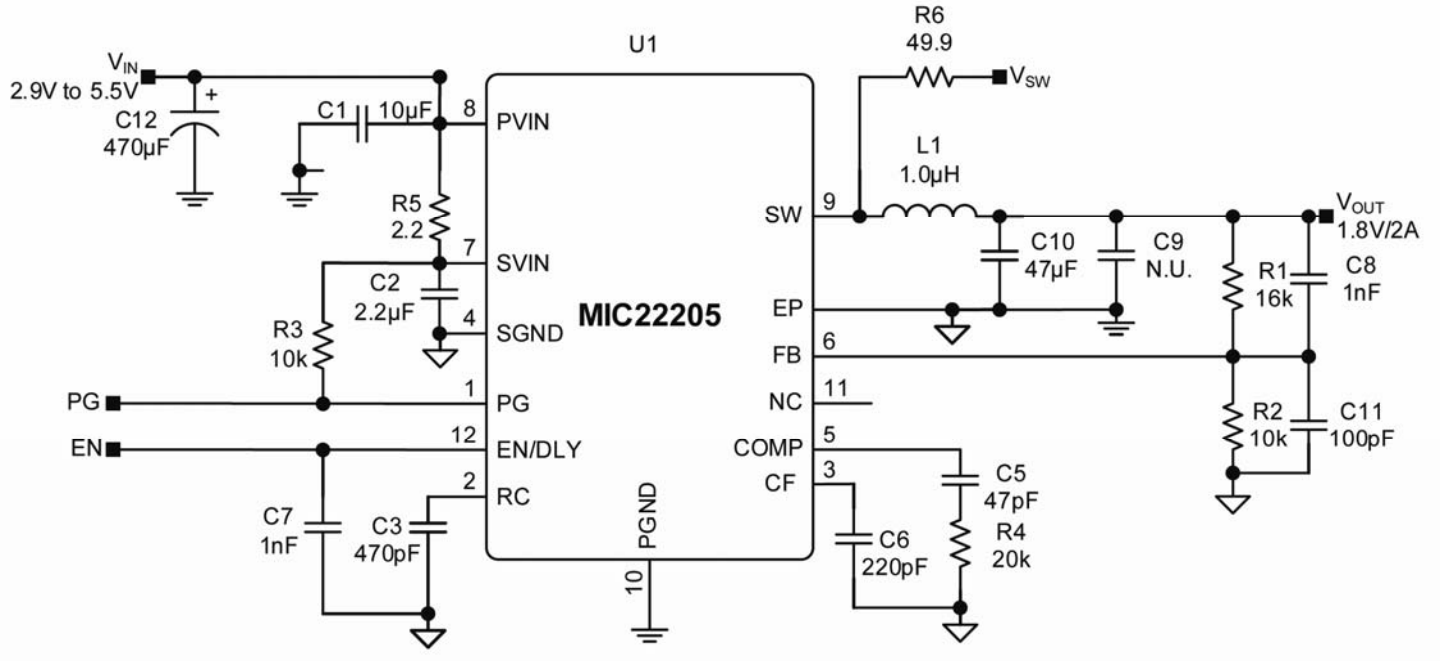
Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback divider network must be place close to the IC with the bottom of R2 connected to SGND.
- The feedback trace should be separate from the power trace, and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

RC Snubber

- Place the RC snubber on either side of the board, and as close to the SW pin as possible.

Evaluation Board Schematic



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	C2012X5R0J106K	TDK[1]	Capacitor, 10µF, 6.3V, X5R, Size 0805	1
	GRM2196R60J106K	Murata[2]		
	08056D106KAT2A	AVX[3]		
C2	C1608X5R0J225M	TDK[1]	Capacitor, 2.2µF, 6.3V, X5R, Size 0603	1
	GRM188R60J225M	Murata[2]		
	06036D225MAT2A	AVX [3]		
C3	C1608X7RH471K	TDK[1]	Capacitor, 470pF, 50V, X7R, Size 0603	
	GRM188R71H471KA01D	Murata[2]		
	06035C471KAT2A	AVX[3]		
C4				
C5	C1608C0G1H470J	TDK[1]	Capacitor, 47pF, 50V, NPO, Size 0603	1
	GQM1885C1H470JB01D	Murata[2]		
	06035A470JAT2A	AVX [3]		
C6	C1608C0G1H221J	TDK[1]	Capacitor, 220pF, 50V, NPO, Size 0603	1
	GRM1885C1H221JA01D	Murata[2]		
	06035A221JAT2A	AVX [3]		
C7, C8	C1608C0G1H102J	TDK[1]	Capacitor, 1nF, 50V, NPO, Size 0603	2
	GRM1885C1H102JA01D	Murata[2]		
	06035A102KAT2A	AVX [3]		

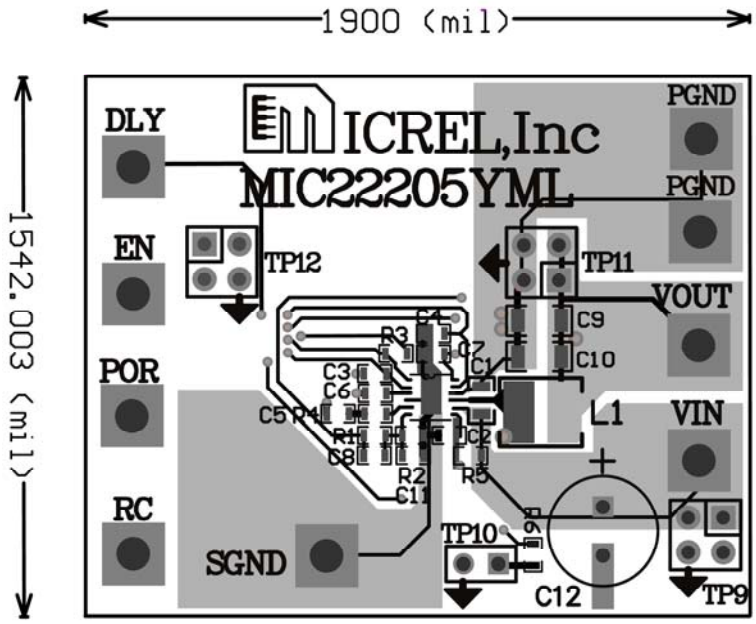
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
C9, C10	C3216X5R0J476M	TDK[1]	Capacitor, 47µF, 6.3V, X5R, Size 1206	2
	GRM31CR60J476ME19L	Murata[2]		
	1206D476MAT2A	AVX [3]		
C11	C1608C0G1H101J	TDK[1]	Capacitor, 100pF, 50V, NPO Size 0603	1
	GRM1885C1H101JA01D	Murata[2]		
	06035A101JAT2A	AVX [3]		
C12	B41125A3477M	Epcos[4]	470µF, 10V, Electrolytic, 8x10 case	1
L1	IHLP1616BZER1R0M11	Vishay [5]	Inductor , 1µH, 5A	1
R1	CRCW06031602FKEA	AVX [3]	Resistor, 16K, 1%, Size 0603	1
R2, R3	CRCW06031002FKEA	AVX [3]	Resistor, 10K, 1%, Size 0603	2
R4	CRCW060320K0FKEA	AVX [3]	Resistor, 20K, 1%, Size 0603	1
R5	CRCW06032R20FKEA	AVX [3]	Resistor, 2.2Ω, 1%, Size 0603	1
R6	CRCW060349R9FKEA	AVX [3]	Resistor, 49.9Ω, 1%, Size 0603	1
U1	**MIC22205YML**	**Micrel**[6]	**Integrated 2A Synchronous Buck Regulator**	**1**

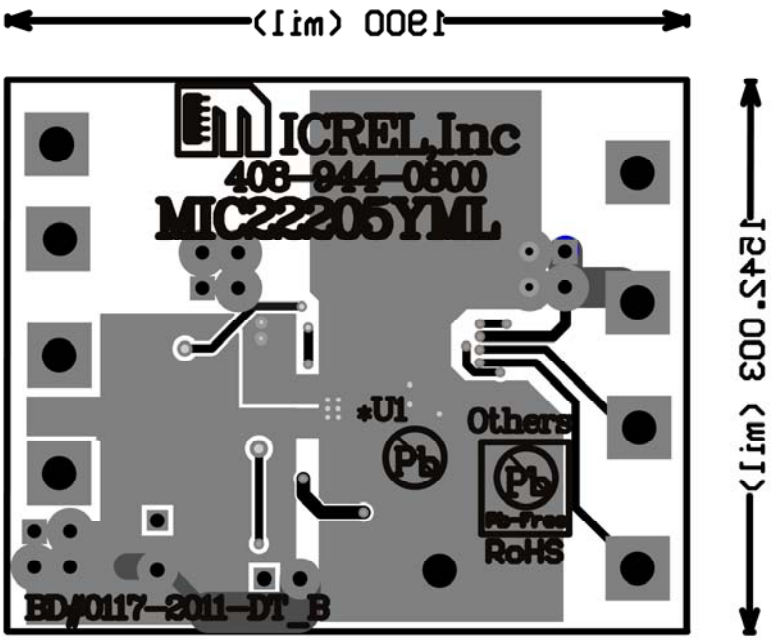
Notes:

1. TDK: www.tdk.com.
2. Murata: www.murata.com.
3. AVX: www.avx.com.
4. Epcos: www.epcos.com.
5. Vishay: www.vishay.com.
6. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

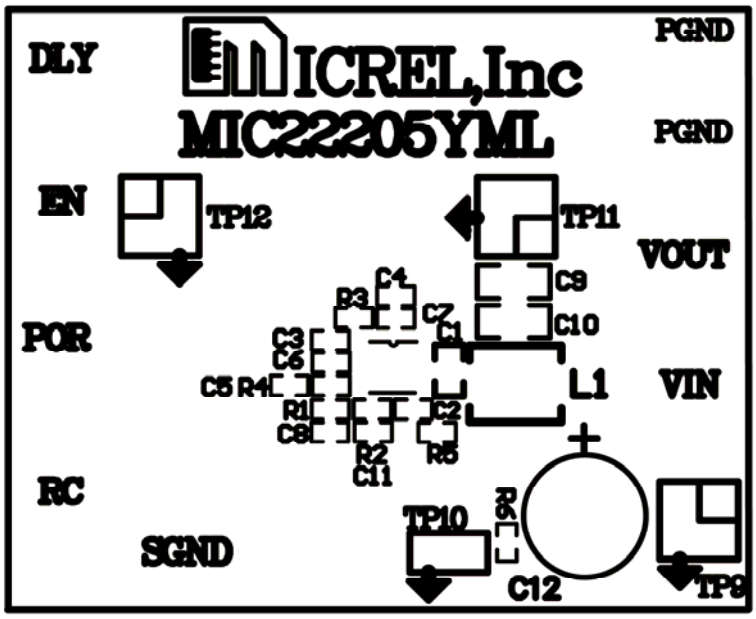


MIC22205 Evaluation Board Top Layer

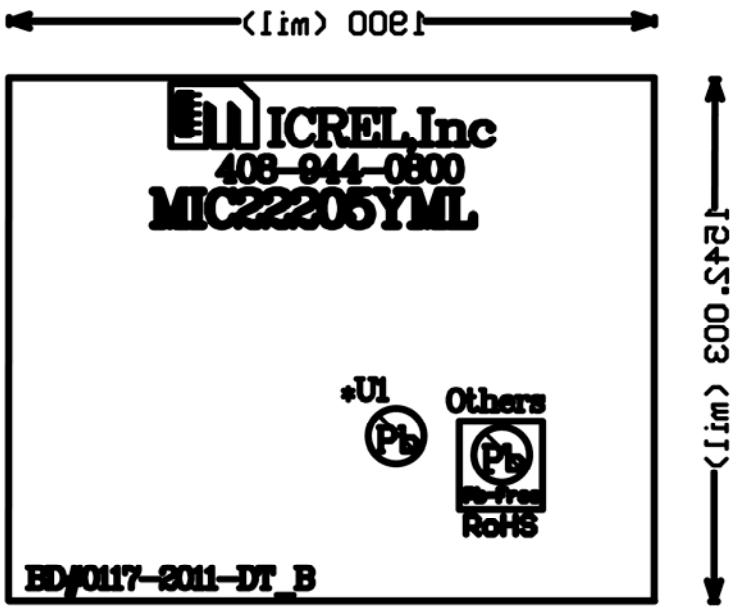


MIC22205 Evaluation Board Bottom Layer

PCB Layout Recommendations (Continued)

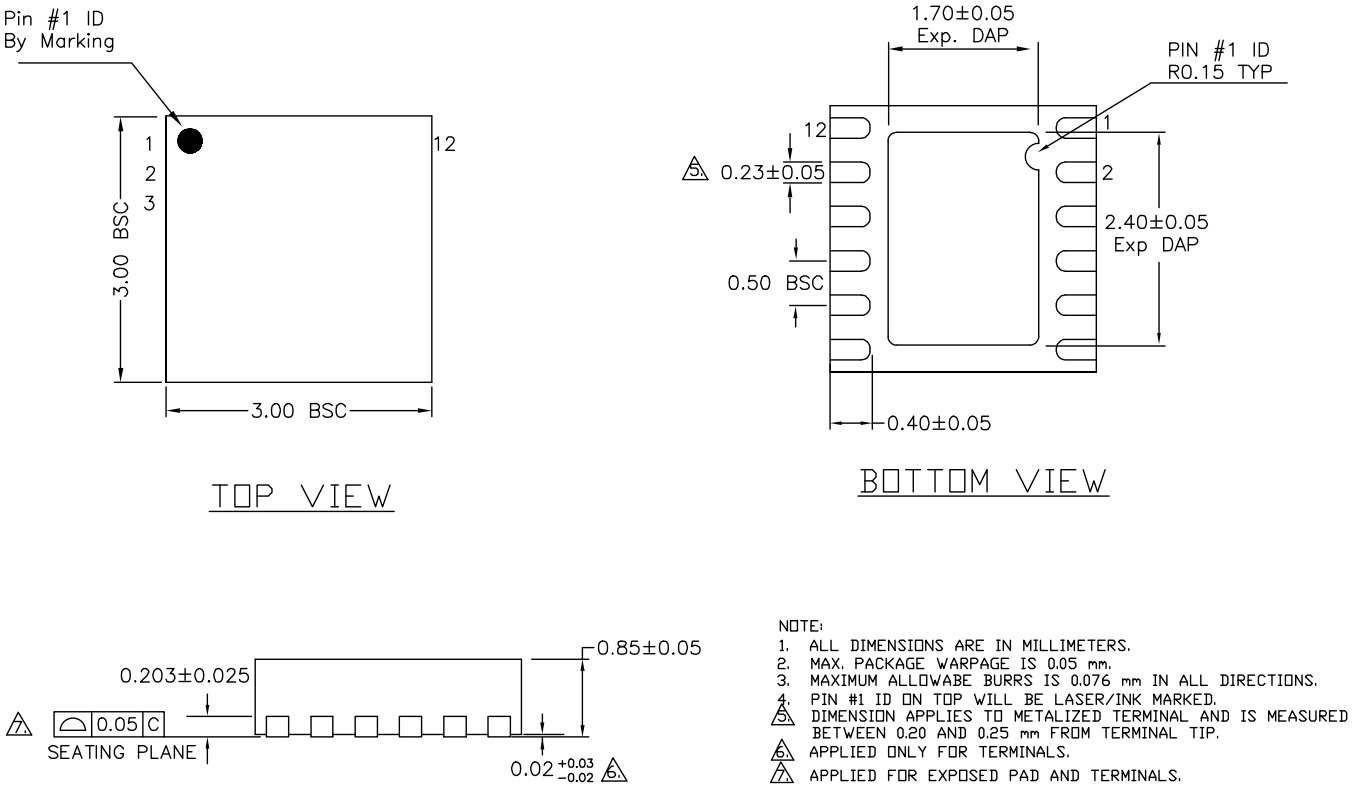


MIC22205 Evaluation Board Top Silk



MIC22205 Evaluation Board Bottom Silk

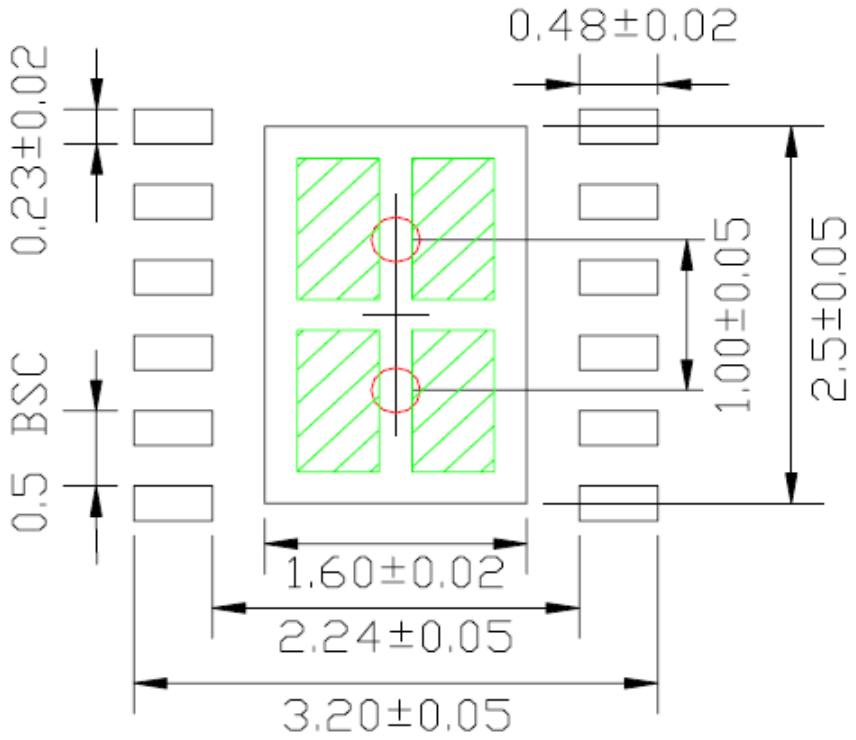
Package Information



12-Pin 3mm × 3mm MLF® (ML)

Recommended Landing Pattern

LP # MLF33D-12LD-LP-1
All units are in mm
Tolerance ± 0.05 if not noted



Red circle indicates Thermal Via. Size should be .300-.350 mm in diameter, 1.00 mm pitch and should be connected to GNI plane for maximum thermal performance.
Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Size should be 0.50x0.95 mm in size, 1.15 mm pitch.

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