MD1810

High-Speed Quad-MOSFET Driver

Features

- 6 ns Rise and Fall Time with 1000 pF Load
- 2A Peak Output Source/Sink Current
- 1.8V to 5V Input CMOS Compatible
- 5V to 12V Total Supply Voltage
- Smart Logic Threshold
- Low-jitter Design
- Four Matched Channels
- Outputs can Swing below Ground
- Output is High Impedance when Disabled
- Low-inductance Package
- High-performance Thermally Enhanced Package

Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Non-destructive Testing (NDT)
- PIN Diode Driver
- CCD Clock Driver/Buffer
- High-speed Level Translator

General Description

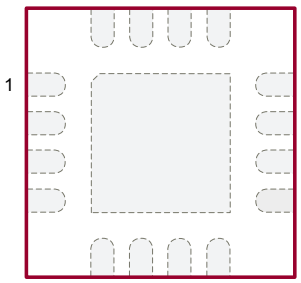
The MD1810 is a high-speed quad-MOSFET driver. It is designed to drive high-voltage P-channel and N-channel MOSFETs for medical ultrasound imaging applications. This driver can also be used for ultrasound metal flaw detection, NDT, piezoelectric transducer drive, clock drive, and PIN diode drive.

The MD1810 has four inputs which individually control four outputs. It also has an output enable (OE) pin. When OE is low, all of the outputs will be in a high impedance state regardless of their logic input control. When OE is high, the MD1810 sets the threshold logic transition to $(V_{OE}+V_{GND})/2$. This ensures the transition to always be at half the amplitude of the logic input signal. This allows the device to have inherent propagation delay matching regardless of the logic input amplitude.

The output stage of the MD1810 has separate power connections enabling the output signal L and H levels to be chosen independently from the V_{DD} and V_{SS} supply voltages. As an example, the input logic levels may be 0V and 1.8V, the control logic may be powered by +5V and –5V and the output L and H levels may be varied anywhere over the range of –5V to +5V. The output stage is capable of peak currents of up to ±2A, depending on the supply voltages used and load capacitance present.

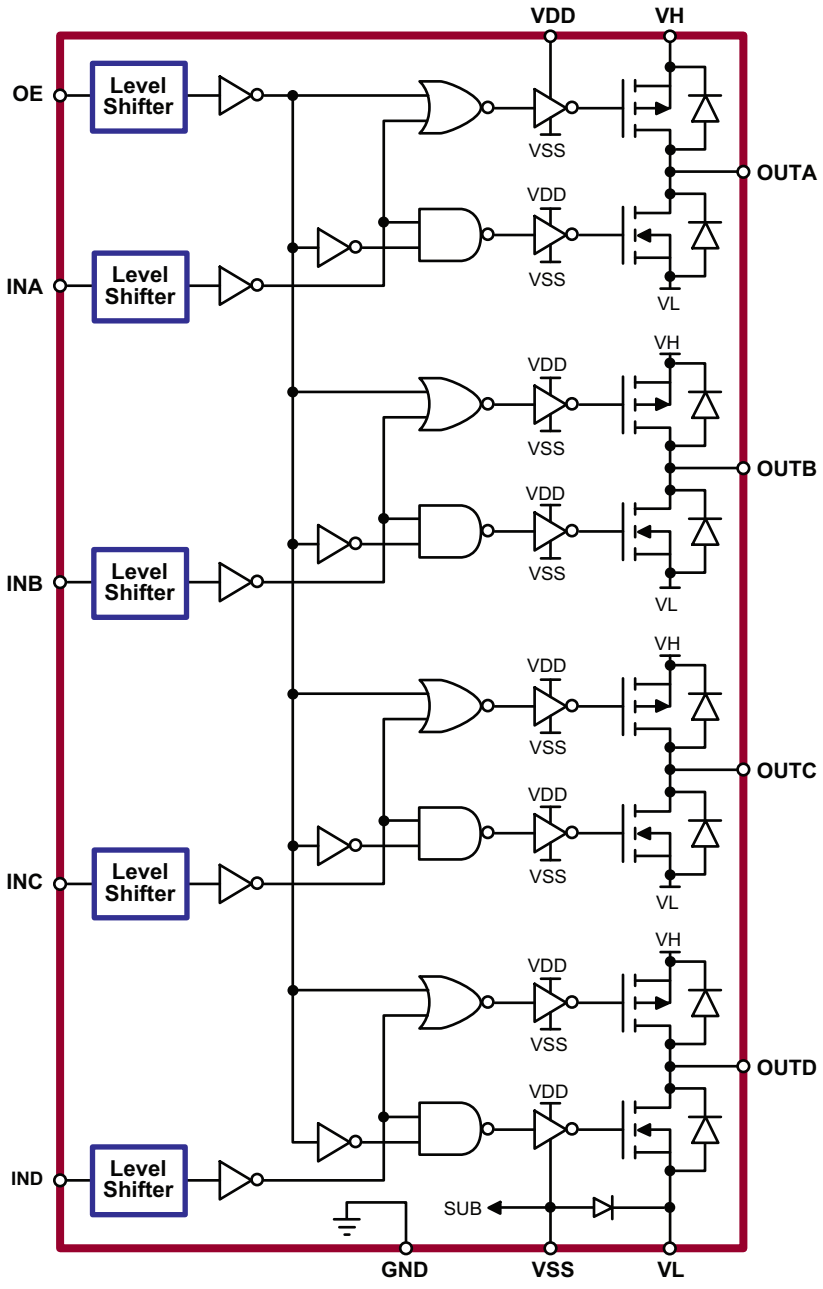
Package Type

16-lead VQFN
(Top view)

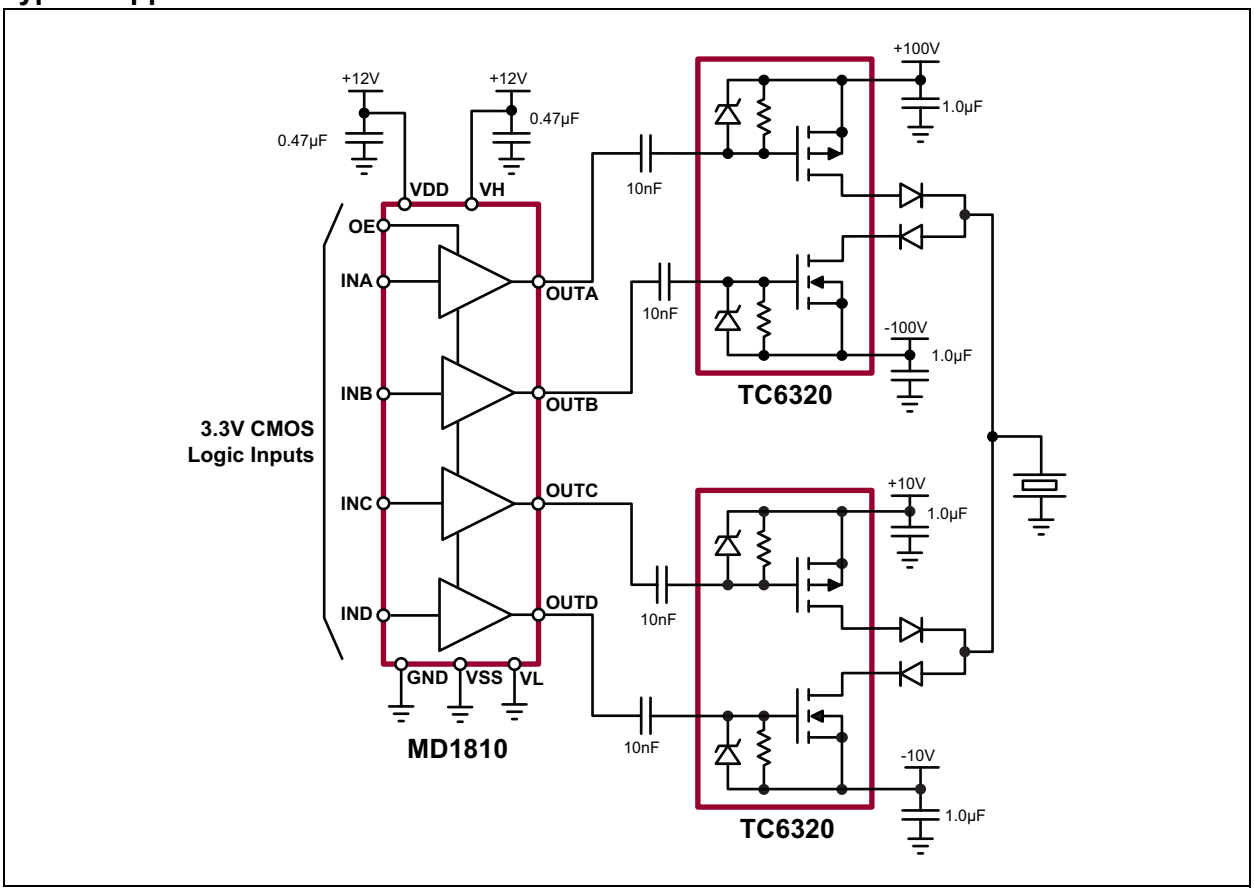


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Logic Supply Voltage, V_{DD}–V_{SS} ..... –0.5V to +13.5V
Output High Supply Voltage, V_H ..... V_L–0.5V to V_{DD} + 0.5V
Output Low Supply Voltage, V_L ..... V_{SS}–0.5V to V_H+ 0.5V
Low-side Supply Voltage, V_{SS} ..... –7V to + 0.5V
Logic Input Levels ..... V_{SS}–0.5V to GND +7V
Maximum Junction Temperature, T_J ..... +125°C
Operating Ambient Temperature, T_A ..... –20°C to +85°C
Storage Temperature, T_S ..... –65°C to +150°C
Package Power Dissipation 2.2W
ESD Rating (**Note 1**) ..... ESD Sensitive

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note1: Device is ESD sensitive. Handling precautions are recommended.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_H = V_{DD}$ = 12V, $V_L = V_{SS}$ = GND = 0V, V_{OE} = 3.3V and T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}–V_{SS}	4.5	—	13	V	2.5V ≤ V_{DD} ≤ 13V
Low-side Supply Voltage	V_{SS}	–5.5	—	0	V	
Output High Supply Voltage	V_H	V_{SS} +2	—	V_{DD}	V	
Output Low Supply Voltage	V_L	V_{SS}	—	V_{DD} –2	V	
V_{DD} Quiescent Current	I_{DDQ}	—	0.8	—	mA	No input transitions, OE = 1
V_H Quiescent Current	I_{HQ}	—	—	10	µA	
V_{DD} Average Current	I_{DD}	—	7	—	mA	One channel on at 5 MHz, no load
V_H Average Current	I_H	—	18	—	mA	
Input Logic Voltage High	V_{IH}	V_{OE}–0.3	—	5	V	For logic inputs INA, INB, INC and IND
Input logic Voltage Low	V_{IL}	0	—	0.3	V	
Input Logic Current High	I_{IH}	—	—	1	µA	
Input Logic Current Low	I_{IL}	—	—	1	µA	
OE Input Logic Voltage High	V_{IH}	1.7	—	5	V	For logic input OE
OE Input Logic Voltage Low	V_{IL}	0	—	0.3	V	
OE Input Logic Impedance to GND	R_{IN}	10	20	30	KΩ	
Logic Input Capacitance	C_{IN}	—	5	10	pF	All inputs
Output Sink Resistance	R_{SINK}	—	—	12.5	Ω	I_{SINK} = 50 mA
Output Source Resistance	R_{SOURCE}	—	—	12.5	Ω	I_{SOURCE} = 50 mA
Peak Output Sink Current	I_{SINK}	—	2	—	A	
Peak Output Source Current	I_{SOURCE}	—	2	—	A	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{OE} = 3.3V$ and $T_A = 25°C$						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Input or OE Rise and Fall Time	t_{irf}	—	—	10	ns	Logic input edge speed requirement
Propagation Delay when Output is from Low to High	t_{PLH}	—	7	—	ns	C_{LOAD} = 1000 pF, input signal rise/fall time of 2 ns (See **Timing Diagram**)
Propagation Delay when Output is from High to Low	t_{PHL}	—	7	—	ns	
Output Rise Time	t_r	—	6	—	ns	
Output Fall Time	t_f	—	6	—	ns	
Rise and Fall Time Matching	$\lvert t_r - t_f \rvert$	—	1	—	ns	For each channel
Propagation Low-to-High and High-to-Low Matching	$\lvert t_{PLH} - t_{PHL} \rvert$	—	1	—	ns	
Propagation Delay Matching	Δt_{dm}	—	±2	—	ns	Device-to-device delay match
Output Enable Time	t_{OE_ON}	—	200	—	ns	
	t_{OE_OFF}	—	9	—		

TEMPERATURE SPECIFICATIONS

Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Maximum Junction Temperature	T_J	—	—	+125	°C	
Operating Ambient Temperature	T_A	–20	—	+85	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
16-lead VQFN	θ_{JA}	—	25	—	°C/W	**Note 1**

Note 1: 1 oz. 4-layer 3” x 4” PCB

Timing Diagram

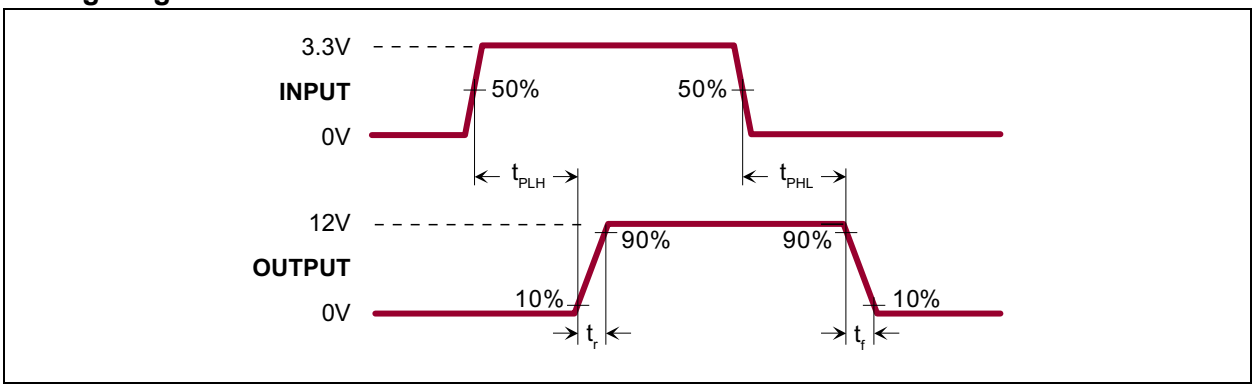


TABLE 1-1: TRUTH FUNCTION TABLE

Logic Inputs		Output
OE	**IN**	
H	L	V_L
H	H	V_H
L	X	High Z

2.0 PIN DESCRIPTION

The details on the pins of MD1810 are listed in Table 2-1. See **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	INB	Logic input. Input logic high will cause the output to swing to VH. Input logic low will cause the output to swing to VL. Keep all logic inputs low until IC powers up.
2	VL	Supply voltage for N-channel output stage
3	GND	Logic input ground reference
4	VL	Supply voltage for N-channel output stage
5	INC	Logic input. Input logic high will cause the output to swing to VH. Input logic low will cause the output to swing to VL. Keep all logic inputs low until IC powers up.
6	IND	
7	VSS	Low-side supply voltage. VSS is also connected to the IC substrate. It is required to be connected to the most negative potential of voltage supplies and powered up first.
8	OUTD	Output drivers
9	OUTC	
10 and 11	VH	Supply voltage for P-channel output stage
12	OUTB	Output drivers
13	OUTA	
14	VDD	High-side supply voltage
15	INA	Logic input. Input logic high will cause the output to swing to VH. Input logic low will cause the output to swing to VL. Keep all logic inputs low until IC powers up.
16	OE	Output enable logic input. When OE is high, $(V_{OE}+V_{GND})/2$ sets the threshold transition between logic-level high and low. When OE is low, all outputs are at high impedance. Keep OE low until IC powers up.
Substrate		The IC substrate is internally connected to the thermal pad. The thermal pad and VSS must be connected externally.

3.0 APPLICATION INFORMATION

For proper operation of the MD1810, low-inductance bypass capacitors should be used on the various supply pins. The GND input pin should be connected to the logic ground. On the other hand, the INA, INB, INC, IND, and OE pins should be connected to a logic source with a swing of GND to OE, where OE is 1.8V to 5V. Good trace practices should be followed corresponding the desired operating speed. The internal circuitry of the MD1810 is capable of operating up to 100 MHz, with the primary speed limitation being the loading effect of the load capacitance. Because of this speed and the high transient currents due to the capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the V_{SS} and V_L pins should have direct low-inductance feed-through connections to a ground plane. The power connection V_{DD} should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads.

The supplied voltages of V_H and V_L determine the output logic levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with a suitable bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1 µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor.

Pay particular attention to minimizing trace lengths, current loop area and using sufficient trace width to reduce inductance. Surface-mount components are highly recommended. Since the output impedance of this driver is very low, in some cases, it may be desirable to add a small series resistor in series with the output signal to obtain better waveform integrity at the load terminals. This will reduce the output voltage slew rate at the terminals of a capacitive load.

Ensure that parasitic couplings are minimized from the driver output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupled voltages may cause problems. The use of a solid ground plane and good power and signal layout practices will prevent this problem. Make sure that the circulating ground return current from a capacitive load will not react with common inductance and cause noise voltages in the input logic circuitry.

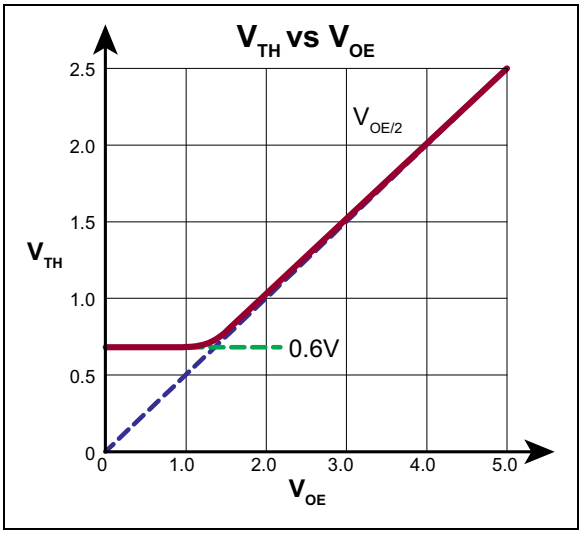


FIGURE 3-1: *V_{TH}/V_{OE} Curve.*

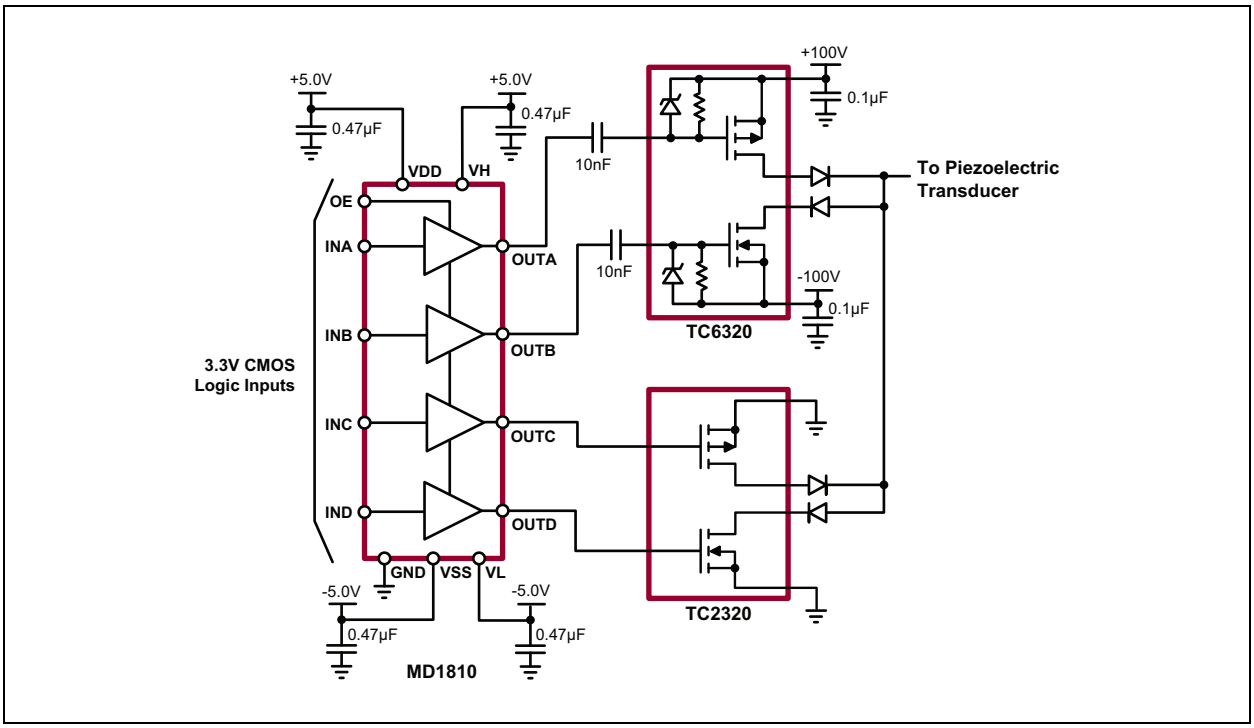


FIGURE 3-2: *1-channel Pulser.*

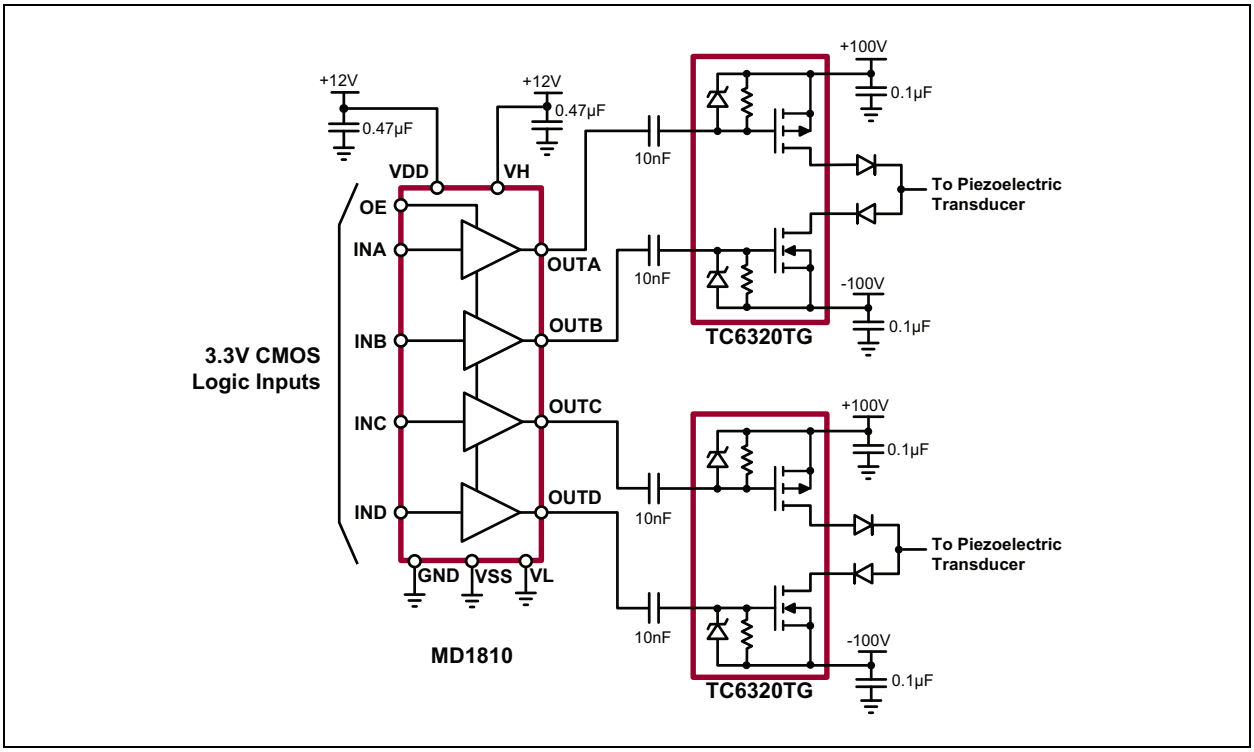


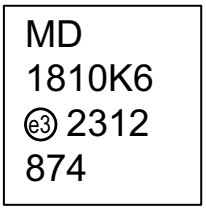
FIGURE 3-3: *2-channel Pulser.*

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

16-lead VQFN

Example

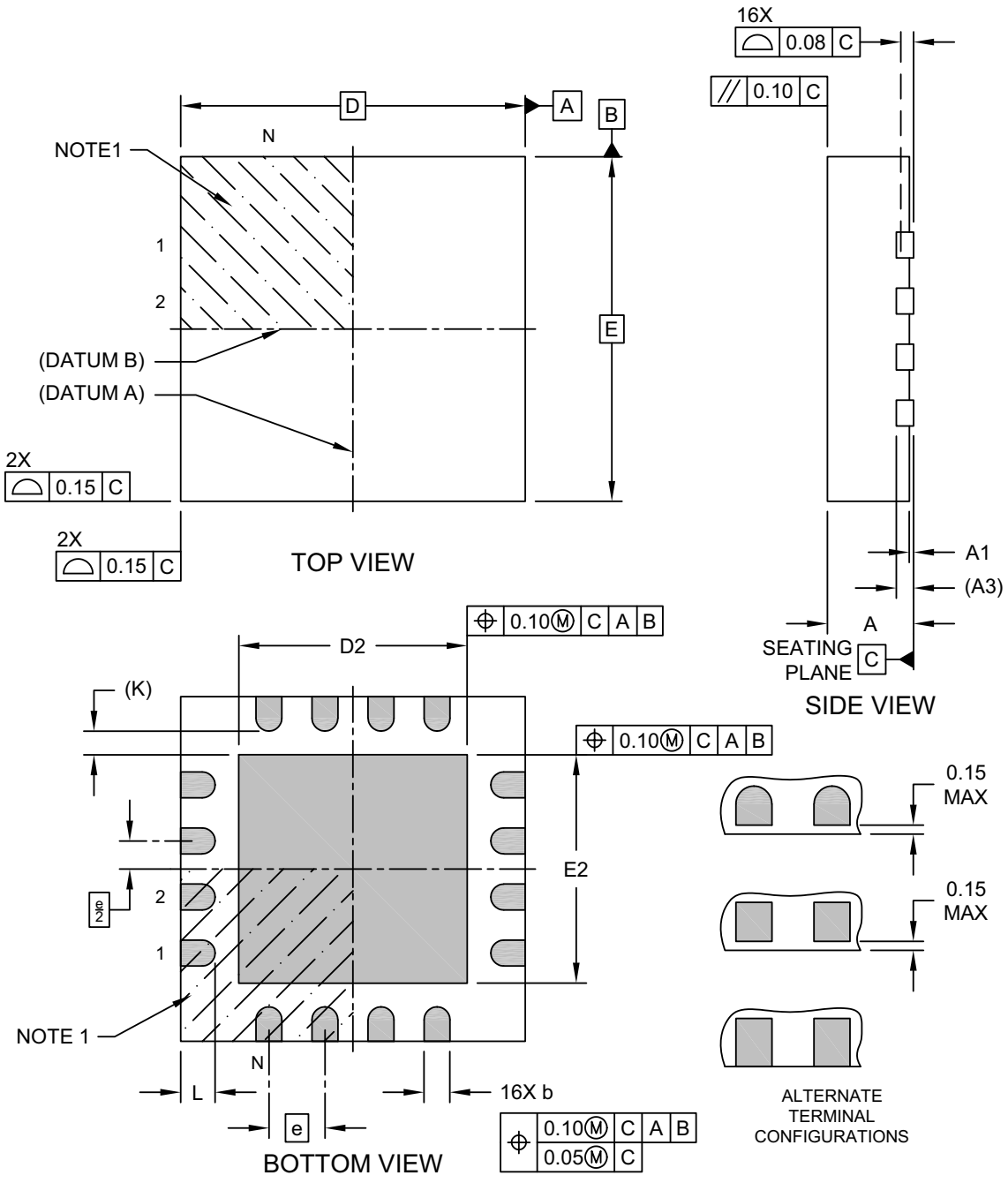


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

16-Lead Very Thin Plastic Quad Flat, No Lead (9DX) - 4x4x1.0 mm Body [VQFN]
With 2.65 mm Exposed Pad; Supertex Legacy Package K6_16_QFN_4x4_P065

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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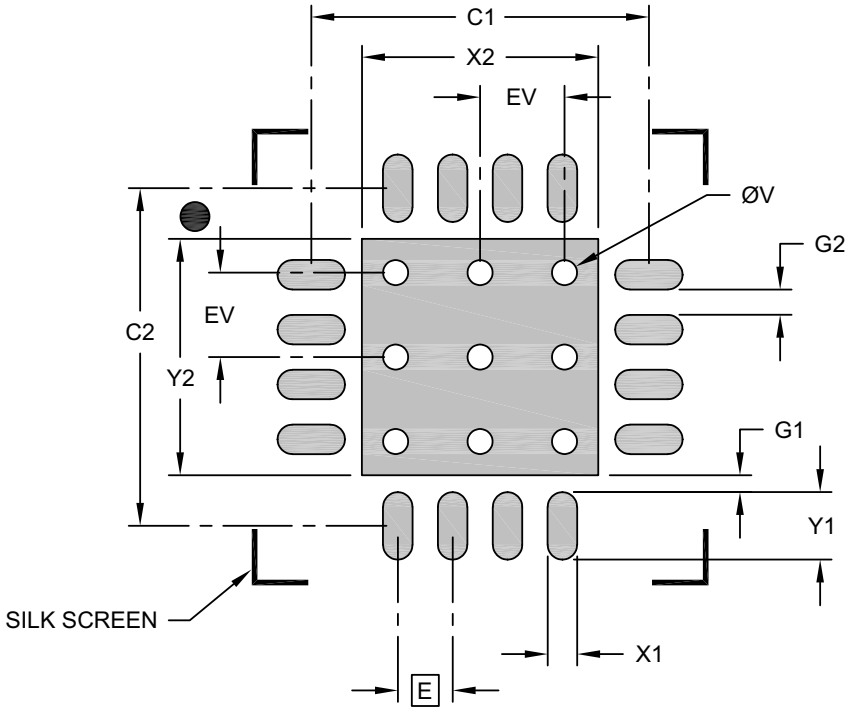
16-Lead Very Thin Plastic Quad Flat, No Lead (9DX) - 4x4x1.0 mm Body [VQFN]
With 2.65 mm Exposed Pad; Supertex Legacy Package K6_16_QFN_4x4_P065

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Center Pad Width	X2			2.80
Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (Xnn)	X1			0.35
Contact Pad Length (Xnn)	Y1			0.80
Contact Pad to Center Pad (Xnn)	G1	0.20		
Contact Pad to Contact Pad (Xnn)	G2	0.30		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

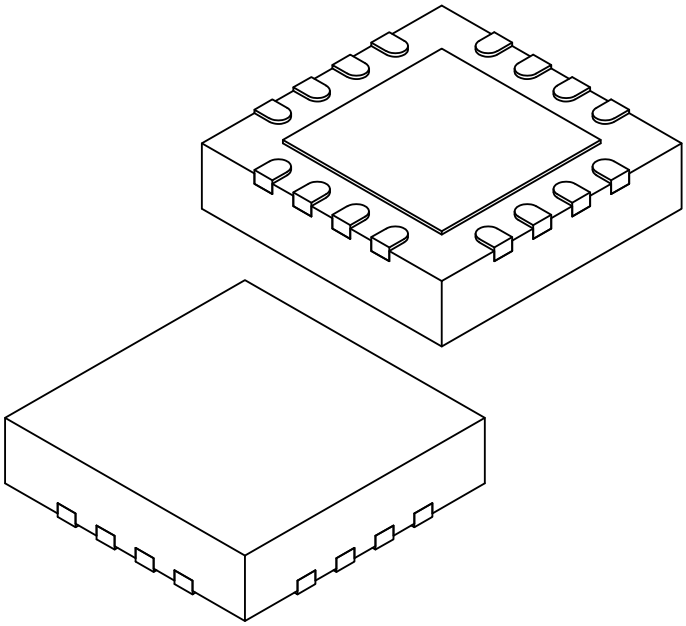
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2268 Rev A

16-Lead Very Thin Plastic Quad Flat, No Lead (9DX) - 4x4x1.0 mm Body [VQFN] With 2.65 mm Exposed Pad; Supertex Legacy Package K6_16_QFN_4x4_P065

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.65	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.65	2.80
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.28 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-268 Rev A Sheet 2 of 2

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2023)

- Converted Supertex Doc# DSFP-MD1810 to Microchip DS20005742A
- Changed package marking formats
- Changed the quantity of the 16-lead VQFN K6 package from 3000/Reel to 3300/Reel
- Updated package marking
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	MD1810	=	High-Speed Quad-MOSFET Driver
Package:	K6	=	16-lead VQFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3300/Reel for a K6 Package

Example:

a) MD1810K6-G: High-Speed Quad-MOSFET Driver, 16-lead VQFN, 3300/Reel

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