**Microsemi**

# High-Precision Clock Generators with Integrated VCXO

**MAX9450/MAX9451/MAX9452**

## General Description

The MAX9450/MAX9451/MAX9452 clock generators provide high-precision clocks for timing in SONET/SDH systems or Gigabit Ethernet systems. The MAX9450/MAX9451/MAX9452 can also provide clocks for the high-speed and high-resolution ADCs and DACs in 3G base stations. Additionally, the devices can also be used as a jitter attenuator for generating high-precision CLK signals.

The MAX9450/MAX9451/MAX9452 feature an integrated VCXO. This configuration eliminates the use of an external VCXO and provides a cost-effective solution for generating high-precision clocks. The MAX9450/MAX9451/MAX9452 feature two differential inputs and clock outputs. The inputs accept LVPECL, LVDS, differential signals, and LVCMOS. The input reference clocks range from 8kHz to 500MHz.

The MAX9450/MAX9451/MAX9452 offer LVPECL, HSTL, and LVDS outputs, respectively. The output range is up to 160MHz, depending on the selection of crystal. The input and output frequency selection is implemented through the I²C or SPI™ interface. The MAX9450/MAX9451/MAX9452 feature clock output jitter less than 0.8ps RMS (in a 12kHz to 20MHz band) and phase-noise attenuation greater than -130dBc/Hz at 100kHz. The phase-locked loop (PLL) filter can be set externally, and the filter bandwidth can vary from 1Hz to 20kHz.

The MAX9450/MAX9451/MAX9452 feature an input clock monitor with a hitless switch. When a failure is detected at the selected reference clock, the device can switch to the other reference clock. The reaction to the recovery of the failed reference clock can be revertive or nonrevertive. If both reference clocks fail, the PLL retains its nominal frequency within a range of ±20ppm at +25°C.

The MAX9450/MAX9451/MAX9452 operate from 2.4V to 3.6V supply and are available in 32-pin TQFP packages with exposed pads.

## Applications

SONET/SDH Systems

10 Gigabit Network Routers and Switches

3G Cellular Phone Base Stations

General Jitter Attenuation

*SPI is a trademark of Motorola, Inc.*

## Features

♦ **Integrated VCXO Provides a Cost-Effective Solution for High-Precision Clocks**

♦ **8kHz to 500MHz Input Frequency Range**

♦ **15MHz to 160MHz Output Frequency Range**

♦ **I²C or SPI Programming for the Input and Output Frequency Selection**

♦ **PLL Lock Range > ±60ppm**

♦ **Two Differential Outputs with Three Types of Signaling: LVPECL, LVDS, or HSTL**

♦ **Input Clock Monitor with Hitless Switch**

♦ **Internal Holdover Function within ±20ppm of the Nominal Frequency**

♦ **Low Output CLK Jitter: < 0.8ps RMS in the 12kHz to 20MHz Band**

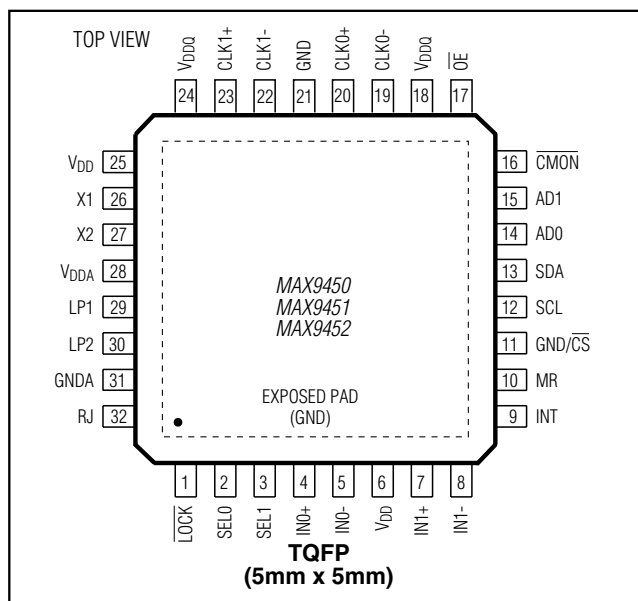♦ **Low Phase Noise > -130dBc at 100kHz, > -140dBc at 1MHz**

## Ordering Information

| PART | PIN-PACKAGE | OUTPUT | PKG CODE |
|---|---|---|---|
| **MAX9450**EHJ | 32 TQFP-EP* | LVPECL | H32E-6 |
| **MAX9451**EHJ | 32 TQFP-EP* | HSTL | H32E-6 |
| **MAX9452**EHJ | 32 TQFP-EP* | LVDS | H32E-6 |

**Note:** All devices are specified over the -40°C to +85°C temperature range.

For lead-free packages, contact factory.

*EP = Exposed paddle.*

## Pin Configuration



**TQFP**
**(5mm x 5mm)**

# High-Precision Clock Generators with Integrated VCXO

## ABSOLUTE MAXIMUM RATINGS

V_DD to GND ...........................................-0.3V to +4.0V
V_DDA to GNDA ......................................-0.3V to +4.0V
All Other Pins to GND ...................-0.3V to V_DD + 0.3V
Short-Circuit Duration (all pins) .................Continuous
Continuous Power Dissipation (T_A = +85°C)
   32-Pin TQFP (derate 27.8mW/°C above +70°C)........2222mW

Storage Temperature Range .............................-65°C to +165°C
Maximum Junction Temperature ....................................+150°C
Operating Temperature Range ..........................-40°C to +85°C
Lead Temperature (soldering, 10s) ................................+300°C
ESD Protection
   Human Body Model (R_D = 1.5kΩ, C_S = 100pF) ..............±2kV

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

(V_DDA = V_DD = V_DDQ = 2.4V to 3.6V, and V_DDQ = 1.4V to 1.6V for MAX9451, T_A = -40°C to +85°C. Typical values at V_DDA = V_DD = V_DDQ = 3.3V, and V_DDQ = 1.5V for MAX9451, T_A = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **LVCMOS INPUT (SEL_, CMON, OE, MR)** | | | | | | |
| Input High Level | V_IH1 | | 2.0 | | V_DD | V |
| Input Low Level | V_IL1 | | 0 | | 0.8 | V |
| Input Current | I_IN1 | V_IN = 0V to V_DD | -50 | | +50 | μA |
| **LVCMOS OUTPUT (INT, LOCK)** | | | | | | |
| Output High Level | V_OH1 | I_OH1 = -4mA | V_DD - 0.4 | | | V |
| Output Low Level | V_OL1 | I_OL1 = 4mA | | | 0.4 | V |
| **THREE-LEVEL INPUT (AD0, AD1)** | | | | | | |
| Input High Level | V_IH2 | | 1.8 | | | V |
| Input Low Level | V_IL2 | | | | 0.8 | V |
| Input Open Level | V_IO2 | Measured at the opened inputs | 1.05 | | 1.35 | V |
| Input Current | I_IL2, I_IH2 | V_IL2 = 0V or V_IH2 = V_DD | -15 | | +15 | μA |
| **DIFFERENTIAL INPUTS (IN0, IN1)** | | | | | | |
| Differential Input High Threshold | V_IDH | V_ID = V_IN+ - V_IN- | | | 50 | mV |
| Differential Input Low Threshold | V_IDL | V_ID = V_IN+ - V_IN- | -50 | | | mV |
| Common-Mode Input-Voltage Range | V_COM | V_ID = V_IN+ - V_IN- | \|V_ID / 2\| | | 2.4 - \|V_ID / 2\| | V |
| Input Current | I_IN+, I_IN- | | | -1 | +1 | μA |
| **MAX9450 OUTPUTS (CLK0, CLK1) (LVPECL)** | | | | | | |
| Output High Voltage | V_OH2 | 50Ω load connected to V_DDQ - 2.0V | V_DDQ - 1.42 | | V_DDQ - 1.00 | V |
| Output Low Voltage | V_OL2 | 50Ω load connected to V_DDQ - 2.0V | V_DDQ - 2.15 | | V_DDQ - 1.70 | V |
| **MAX9451 OUTPUTS (CLK0, CLK1) (differential HSTL)** | | | | | | |
| Output High-Level Voltage | V_OH3 | With 50Ω load resistor to GND, Figure 1 | V_DDQ - 0.4V | | V_DDQ | V |
| Output Low-Level Voltage | V_OL3 | With 50Ω to GND and 16mA sink current | | | 0.4 | V |
| **MAX9452 OUTPUTS (CLK0, CLK1) (LVDS)** | | | | | | |
| Differential Output Voltage | V_OD | With a total 100Ω load, Figure 1 | 300 | 370 | 450 | mV |
| Change in V_OD Between Complementary Output States | ΔV_OD | | | 10 | 35 | mV |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{DDA} = V_{DD} = V_{DDQ} = 2.4V$ to $3.6V$, and $V_{DDQ} = 1.4V$ to $1.6V$ for MAX9451, $T_A = -40°C$ to $+85°C$. Typical values at $V_{DDA} = V_{DD} = V_{DDQ} = 3.3V$, and $V_{DDQ} = 1.5V$ for MAX9451, $T_A = +25°C$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Offset Voltage | $V_{OS}$ | | | 1.05 | 1.2 | 1.35 | V |
| Change in $V_{OS}$ Between Complementary Output States | $\Delta V_{OS}$ | | | | 10 | 35 | mV |
| Output Short-Circuit Current | $I_{OS}$ | Two output pins connected to GND | | | -7.5 | -15 | mA |
| **SERIAL INTERFACE INPUT, OUTPUT (SCL, SDA, $\overline{CS}$)** | | | | | | | |
| Input High Level | $V_{IH}$ | | | 0.7 x $V_{DD}$ | | | V |
| Input Low Level | $V_{IL}$ | | | | | 0.3 x $V_{DD}$ | V |
| Input Leakage Current | $I_{IL}$ | | | -1 | | +1 | µA |
| Output Low Level | $V_{OL}$ | 3mA sink current | | | | 0.4 | V |
| Input Capacitance | $C_I$ | | | | 10 | | pF |
| **POWER CONSUMPTION** | | | | | | | |
| $V_{DD}$ and $V_{DDA}$ Supply Current | $I_{CC1}$ | Output clock frequency = 155MHz | MAX9450 | | 55 | 85 | mA |
| | | | MAX9451 | | 70 | 94 | |
| | | | MAX9452 | | 65 | 88 | |
| $V_{DDQ}$ Supply Current | $I_{CC2}$ | Output clock frequency = 155MHz (MAX9450) | MAX9450 | | 55 | 80 | mA |
| | | | MAX9451 | | 65 | 80 | |
| | | | MAX9452 | | 14 | 25 | |

## AC ELECTRICAL CHARACTERISTICS

($V_{DDA} = V_{DD} = V_{DDQ} = 2.4V$ to $3.6V$, and $V_{DDQ} = 1.4V$ to $1.6V$ for MAX9451, $T_A = -40°C$ to $+85°C$. $|V_{ID}| = 200mV$, $V_{COM} = |V_{ID} / 2|$ to $2.4 - |V_{ID} / 2|$. Typical values at $V_{DDA} = V_{DD} = V_{DDQ} = 3.3V$ and $V_{DDQ} = 1.5V$ for MAX9451, $T_A = +25°C$. $C_L = 10pF$, clock output = 155.5MHz and clock input = 19.44MHz, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CLK OUTPUTS (CLK0, CLK1)** | | | | | | |
| Reference Input Frequency | $f_{IN}$ | Measured at IN0 or IN1 | 0.008 | | 500 | MHz |
| Output Frequency | $f_{OUT}$ | Measured at CLK0 or CLK1 | 15 | | 160 | MHz |
| VCXO Pulling Range | | $C_L = 8pF$ (Note 2) | | | ±60 | ppm |
| Output-to-Output Skew | $t_{SKO}$ | Skew between CLK0 and CLK1 (MAX9450 and MAX9452) | | 50 | 90 | ps |
| | | Skew between CLK0 and CLK1 (MAX9451) | | 55 | 106 | |
| Rise Time | $t_R$ | 20% to 80% of output swing | | 0.4 | 0.590 | ns |
| Fall Time | $t_F$ | 80% to 20% of output swing | | 0.4 | 0.590 | ns |
| Duty Cycle | | | 43 | | 56 | % |
| Period Jitter (RMS) | $T_J$ | Measured at the band 12kHz to 20MHz | | 0.8 | | ps |
| Phase Noise | | 1kHz offset | | -70 | | dBc |
| | | 10kHz offset | | -110 | | |
| | | 100kHz offset | | -130 | | |
| | | 1MHz offset | | -140 | | |

# High-Precision Clock Generators with Integrated VCXO

## SERIAL I2C-COMPATIBLE INTERFACE TIMING CHARACTERISTICS

($V_{DD}$ = 2.4V to 3.6V, $T_A$ = -40°C to +85°C. See Figure 4 for the timing parameters definition.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial Clock | $f_{SCL}$ | | | | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | µs |
| Repeated Hold Time START Condition | $t_{HD,STA}$ | | 0.6 | | | µs |
| Repeated START Condition Setup Time | $t_{SU,STA}$ | | 0.6 | | | µs |
| STOP Condition Setup Time | $t_{SU,STO}$ | | 0.6 | | | µs |
| Data Hold Time | $t_{HD,DAT}$ | (Note 3) | 100 | | | ns |
| Data Setup Time | $t_{SU,DAT}$ | | 100 | | | ns |
| SCL Clock-Low Period | $t_{LOW}$ | | 1.3 | | | µs |
| SCL Clock-High Period | $t_{HIGH}$ | | 0.7 | | | µs |
| Maximum Receive SCL/SDA Rise Time | $t_R$ | | | 300 | | ns |
| Minimum Receive SCL/SDA Rise Time | $t_R$ | (Note 4) | | $20 + 0.1 \times C_b$ | | ns |
| Maximum Receive SCL/SDA Fall Time | $t_F$ | | | 300 | | ns |
| Minimum Receive SCL/SDA Fall Time | $t_F$ | (Note 4) | | $20 + 0.1 \times C_b$ | | ns |
| Fall Time of SDA, Transmitting | $t_{F,TX}$ | (Note 4) | $20 + 0.1C_b$ | | 250 | ns |
| Pulse Width of Suppressed Spike | $t_{SP}$ | (Note 5) | 0 | | 50 | ns |
| Capacitive Load for Each Bus Line | $C_B$ | (Note 4) | | | 400 | pF |

## SERIAL SPI INTERFACE TIMING CHARACTERISTICS

($V_{DD}$ = 2.4V to 3.6V, $T_A$ = -40°C to +85°C. See Figure 7 for the timing parameters definition.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Serial-Clock Frequency | $f_{SCL}$ | | | | 2 | MHz |
| $\overline{CS}$ Fall to CLK Rise Setup Time | $t_{CSS}$ | | 12.5 | | | ns |
| DIN Setup Time | $t_{DS}$ | | 12.5 | | | ns |
| DIN Hold Time | $t_{DH}$ | | 0 | | | ns |
| CLK High to $\overline{CS}$ High | $t_{CSH}$ | | 0 | | | ns |
| $\overline{CS}$ Pulse-High Time | $t_{CSW}$ | | 20 | | | ns |

**Note 1:** All timing AC electrical characteristics and timing specifications are guaranteed by design and not production tested.
**Note 2:** The VCXO tracks the input clock frequency by ±60ppm.
**Note 3:** A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined regions of SCL's falling edge.
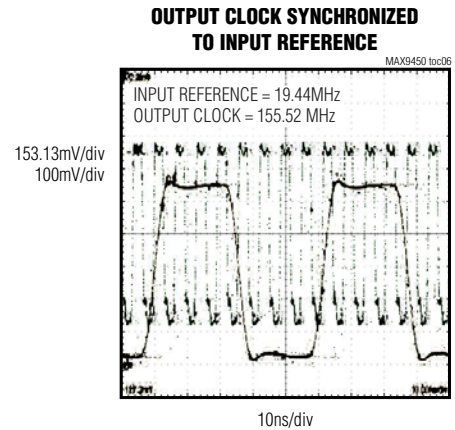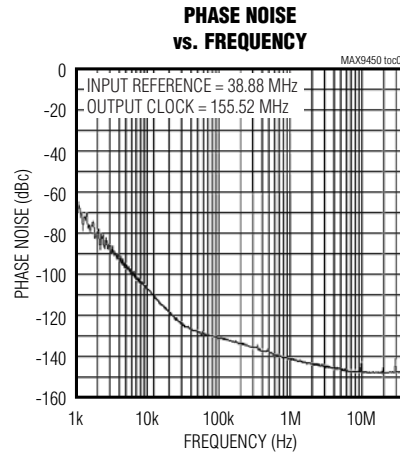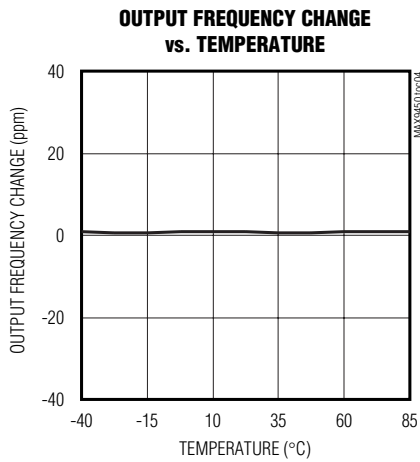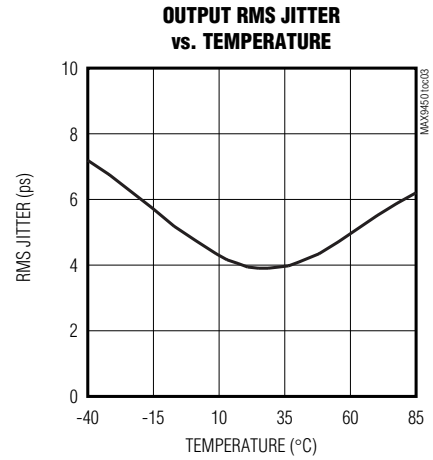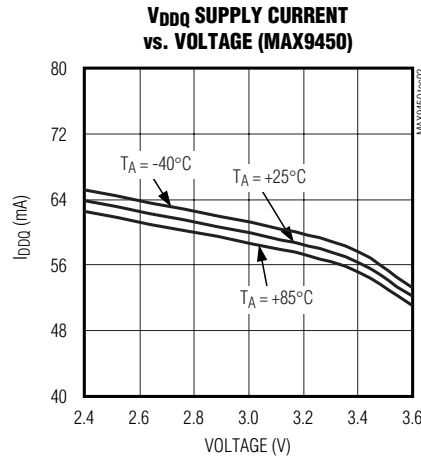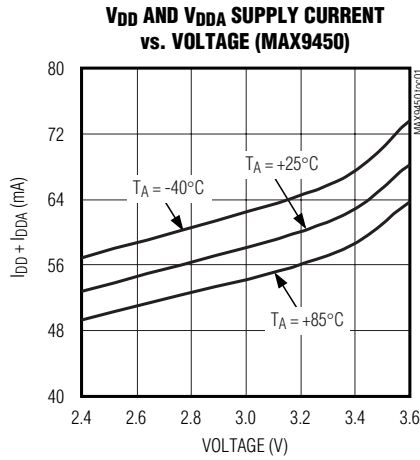**Note 4:** $C_B$ = total capacitance of one bus line in pF. Tested with $C_B$ = 400pF.
**Note 5:** Input filters on SDA and SCL suppress noise spikes less than 50ns.

## Typical Operating Characteristics

(V_DD = V_DDA = V_DDQ = 3.3V. T_A = +25°C, unless otherwise noted.)

**V_DD AND V_DDA SUPPLY CURRENT vs. VOLTAGE (MAX9450)**

**V_DDQ SUPPLY CURRENT vs. VOLTAGE (MAX9450)**

**OUTPUT RMS JITTER vs. TEMPERATURE**

**OUTPUT FREQUENCY CHANGE vs. TEMPERATURE**

**PHASE NOISE vs. FREQUENCY**

**OUTPUT CLOCK SYNCHRONIZED TO INPUT REFERENCE**

INPUT REFERENCE = 38.88 MHz
OUTPUT CLOCK = 155.52 MHz

INPUT REFERENCE = 19.44MHz
OUTPUT CLOCK = 155.52 MHz

153.13mV/div
100mV/div

10ns/div

**MAX9450/MAX9451/MAX9452**

**MAX9450/MAX9451/MAX9452**

_____ *Pin Description*

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $\overline{LOCK}$ | Lock Indicator. $\overline{LOCK}$ goes low when the PLL locks. $\overline{LOCK}$ is high when the PLL is not locked. |
| 2, 3 | SEL0, SEL1 | IN0_ and IN1_ Select Inputs. Drive SEL0 high to activate IN0; drive SEL1 high to activate IN1. Driving SEL0 and SEL1 low disables the corresponding input. A 165kΩ pullup resistor pulls SEL0 and SEL1 up to $V_{DD}$. |
| 4, 5 | IN0+, IN0- | Differential Reference Input Pair. IN0+ and IN0- accept LVPECL, LVDS, and LVCMOS signals. |
| 6, 25 | $V_{DD}$ | Digital Power Supply. Connect a 2.4V to 3.6V power supply to $V_{DD}$. Bypass $V_{DD}$ to GND with a 0.1µF capacitor. |
| 7, 8 | IN1+, IN1- | Differential Reference Input Pair. IN1+ and IN1- accept LVPECL, LVDS, and LVCMOS signals. |
| 9 | INT | Reference Input Condition Indicator. A high indicates a failed reference. |
| 10 | MR | Master Reset. Drive MR high to reset all I²C registers to their default state and INT to zero. |
| 11 | GND/$\overline{CS}$ | Ground and Chip-Select Input. Connect to GND in I²C mode. This is the chip-select input in SPI mode. |
| 12 | SCL | Clock Input. SCL is the clock input in I²C bus mode and SPI bus mode. |
| 13 | SDA | Data Input. SDA is the data input in I²C bus mode and SPI bus mode. |
| 14, 15 | AD0, AD1 | I²C Address Selection. Drive AD0 and AD1 high to convert the serial interface from I²C to SPI. GND/$\overline{CS}$ becomes $\overline{CS}$. See Table 3 for the unique addresses list. |
| 16 | $\overline{CMON}$ | Clock Monitor. Drive $\overline{CMON}$ low to enable the clock monitor. Drive $\overline{CMON}$ high to disable the clock monitor. |
| 17 | $\overline{OE}$ | Output Enable Input. Drive $\overline{OE}$ low to enable the clock outputs. Driving $\overline{OE}$ high disables the clock outputs, and the outputs go high impedance. An internal 165kΩ pullup resistor pulls $\overline{OE}$ up to $V_{DD}$. |
| 18, 24 | $V_{DDQ}$ | Clock-Output Power Supply. Connect a 2.4V to 3.6V power supply to $V_{DDQ}$ for the MAX9450 and MAX9452. Connect a 1.5V power supply to $V_{DDQ}$ for the MAX9451. Connect a 0.1µF bypass capacitor from $V_{DDQ}$ to GND. |
| 19, 20 | CLK0-, CLK0+ | Differential Clock Output 0. The MAX9450 features LVPECL outputs. The MAX9451 features HSTL outputs and the MAX9452 features LVDS outputs. |
| 21 | GND | Digital GND |
| 22, 23 | CLK1-, CLK1+ | Differential Clock Output 1. The MAX9450 features LVPECL outputs. The MAX9451 features HSTL outputs, and the MAX9452 features LVDS outputs. |
| 26, 27 | X1, X2 | Reference Crystal Input. Connect the reference crystal from X1 to X2. |
| 28 | $V_{DDA}$ | Analog Power Supply. Connect a 2.4V to 3.6V power supply to $V_{DDA}$. Bypass $V_{DDA}$ to GNDA with a 0.1µF capacitor. |
| 29, 30 | LP1, LP2 | External Loop Filter. Connect an RC circuit between LP1 and LP2. See the *External Loop Filter* section. |
| 31 | GNDA | Analog Ground |
| 32 | RJ | Charge-Pump Set Current. Connect an external resistor to GND to set the charge-pump current. See Table 11. |
| EP | EP | Exposed Paddle. Connect to ground. |

## Functional Diagram



12kΩ TO 200kΩ

6nF

60nF  10kΩ

CRYSTAL
15MHz TO 160MHz
FUNDAMENTAL MODE
AND AT CUT

RJ  LP2  LP1  X1  X2

$\overline{\text{LOCK}}$

LOCK DET

IN0+
IN0−
IN1+
IN1−

1/P  PFD/CP  LOOP FILTER  VCXO

DIV0
1/N0

DIV1
1/N1

CLK0+
CLK0−
CLK1+
CLK1−

MUX

$\overline{\text{OE}}$

$\overline{\text{CMON}}$
INT
SEL0
SEL1

CLK
MONITOR

LUT FOR P

1/M

LUT FOR M

LUT FOR N1, N2

SCL
SDA

I²C PORT

AD0
AD1

CONTROL
REGISTERS

SPI PORT

GND/$\overline{\text{CS}}$

MAX9450
MAX9451
MAX9452

MR  V$_{DDA}$  GNDA  V$_{DD}$  GND
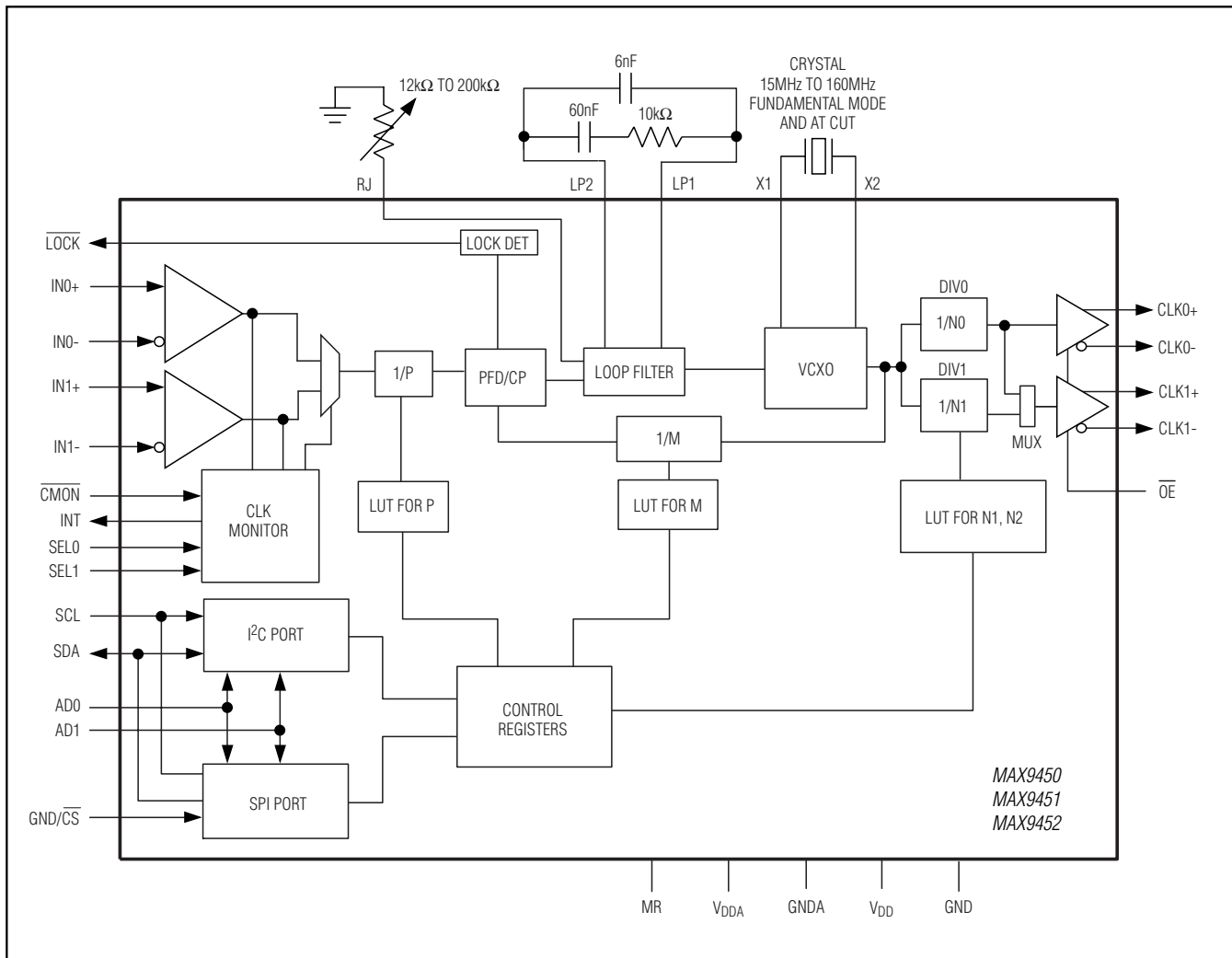
## Detailed Description

The MAX9450/MAX9451/MAX9452 clock generators provide high-precision clocks for timing in SONET/SDH systems or Gigabit Ethernet systems. The MAX9450/MAX9451/MAX9452 can also provide clocks for the high-speed and high-resolution ADCs and DACs in 3G base stations. Additionally, the MAX9450/MAX9451/MAX9452 can be used as a jitter attenuator for generating high-precision clock signals.

The MAX9450/MAX9451/MAX9452 feature two differential inputs and two differential clock outputs. The inputs accept LVPECL, LVDS, and LVCMOS signals. The input reference clock ranges from 8kHz to 500MHz and the output clock ranges from 15MHz to 160MHz. The internal clock monitor observes the condition of the input reference clocks and provides a hitless switch when an input failure is detected. The MAX9450/MAX9451/MAX9452 also provide holdover in case no input clock is supplied.

### Control and Status Registers

The MAX9450/MAX9451/MAX9452 contain eight 8-bit control registers named CR0 to CR7. The registers are accessible through the I²C/SPI interface. CR0 is for the frequency-dividing factor, P. CR1 and CR2 hold the values of the divider, M. CR3 and CR4 are for dividers

N1 and N2, respectively. CR5 and CR6 are the control function registers for output enabling, reference clock selection, and activation of the clock monitor and the holdover function. CR7 contains the status of clock monitor, holdover, and PLL locking. The addresses of the eight registers are shown in Table 4. Tables 5 through 10 show the register maps.

## Output Buffers

Three different output formats (LVPECL, HSTL, and LVDS) are available. Each output contains its own frequency divider. All the output clocks align to their coincident rising edges. After changing the dividing ratio, the output clocks complete the current cycle and stay logic-low until the rising edges of the newly divided clock. When CR5[7] is high, the MAX9450/MAX9451/MAX9452 set all the outputs to logic-low. Setting the bits CR5[6] and CR5[5] properly enables and disables the outputs individually; see Table 8. A disabled output is always in high impedance. At the receiver end, the two cables or PCB traces can be terminated as shown in Figure 1.

The VCXO output is divided down before driving the output buffers. Program the dividing factor through the serial interface. The MAX9450/MAX9451/MAX9452 feature two output dividers DIV0 and DIV1 (see the *Functional Diagram*). DIV0 drives OUT0 and either DIV0 or DIV1 can drive OUT1. CR6[2] sets which divider output drives OUT1. This function allows for programming OUT1 and OUT0 to different frequencies.

## Reference Clock Inputs

The MAX9450/MAX9451/MAX9452 feature two "anything" differential clock inputs. "Anything" means that the inputs take any differential signals, such as CML, LVDS, LVPECL, or HSTL. The inputs can also take a single-ended input. For example, with LVCMOS reference inputs, connect the inputs to the positive pins INn+ and connect the negative pins INn- to a reference voltage of $V_{DD}$ - 1.32V. See Figure 2.

Setting CR5[4] and CR6[3] selects the input reference. Failure detection and revert function apply only to IN0 and IN1. Also, SEL0 and SEL1 or CR5[3:2] can disable the corresponding inputs. See Table 2.

## Frequency Selection and Programming

The output frequency at CLKn, (n = 0, 1) is determined by the reference clock and the dividing factors M, Ni (i = 0, 1), and P, shown in the following equation:
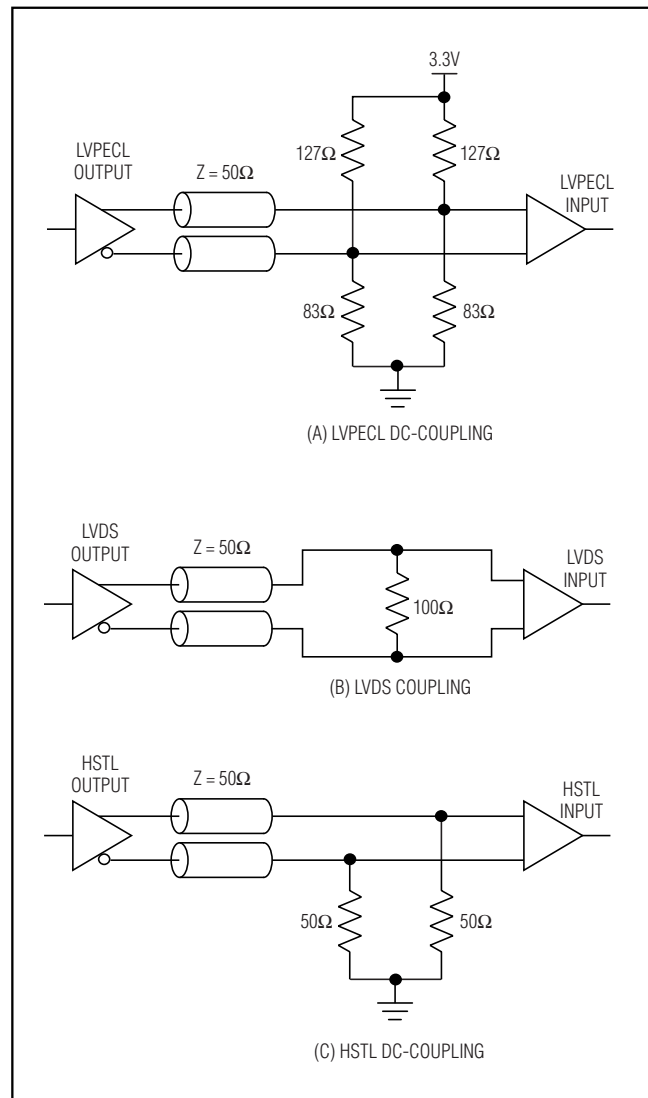
$$f_{CLKn} = f_{REF} \times \frac{M}{Ni \times P}$$
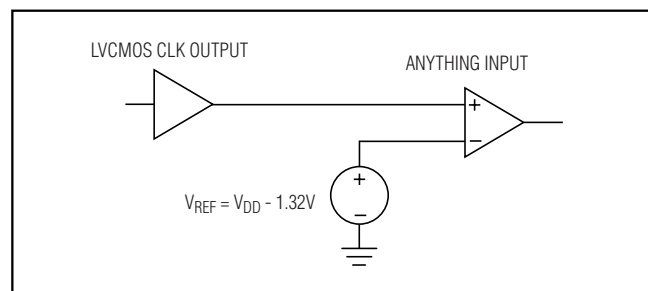


Figure 1. DC LVPECL, LVDS, and HSTL Termination



Figure 2. Connecting LVCMOS Output to LVPECL Input

where $f_{CLKn}$ is the frequency at the CLKn output, $f_{REF}$ is the frequency of the reference clock, M (1 to 32,768) is the dividing factor in the feedback loop, Ni (1, 2, 3, 4, 5, 6, 8, 16) are the dividing factors of the outputs, and P (1 to 256) is the dividing factor to the input reference clock. It is possible to set various frequencies at the two differential CLK_ outputs with this configuration. For example, in 10 Gigabit Ethernet or SONET applications, set the dividing factors to generate the required frequencies, as shown in Table 1.

### Input Clock Monitor

#### Failure Detection
The MAX9450/MAX9451/MAX9452 clock-failure-detection function monitors the two reference inputs simultaneously. If a reference input clock signal (IN_) does not transition for two or more VCO cycles, the device reports a failure by setting INT high and bit CR7[6] or CR7[5] to 1. See Table 9. After a reference clock failure, the monitor switches to the other valid input reference. At the same time, the clock monitor loads CR7 with the status of the reference clocks and which input is selected. The mapping of CR7 is given in Table 9. If one of the inputs is disabled according to the bits in CR5[3:2], then the monitor is disabled.

#### Revert Function
The response of the MAX9450/MAX9451/MAX9452 to a detected input failure depends on the setting of the revert function. If the failed input recovers from the failure, INT and CR7[5:6] resets to zero if revert is activated. If the recovered input is selected by CR5[4] as the default input reference, the MAX9450/MAX9451/MAX9452 reselect this input. If the revert function is not activated, once an input failure is detected, the monitor remains in the failure state with INT = 1 and CR7[5:6] = 1, until the MAX9450/MAX9451/MAX9452 are reset. Activate the revert function using the bit CR5[1].

#### Failure-Detection Monitor Reset
Reset the fault by toggling $\overline{CMON}$ from low to high, toggling MR or CR6[4] from low to high, or by toggling the bit CR5[0] from low to high. In revert mode, when the monitor is reset, INT and CR7[5:6] reset to zero and the default input is the one indicated by CR5[4].

#### Holdover Function
The holdover function locks the output frequency to its nominal value within ±20ppm. Activate this function by setting CR6[7] to 1. The MAX9450/MAX9451/MAX9452 enter holdover when the devices detect a failure from both input references. Setting CR6[6] to 1 forces the device into the holdover state, while resetting CR6[6] exits holdover.

Use a reset holdover. If the revert function is activated once an input is recovered from the failure, the device also exits holdover and switches to the recovered input reference. If both inputs recover simultaneously, the device switches to the default input.

VCXO frequency during holdover is the value of the frequency right before the failure of inputs.

When CR6[5] goes from 0 to 1, the value of the VCXO frequency is acquired and stored. The VCXO can be switched to this acquired frequency by setting CR6[1] to 1. Such a transition can happen in both the normal mode of operation and the holdover mode.

#### PLL Lock Detect
The MAX9450/MAX9451/MAX9452 also feature PLL lock detection. The MAX9450/MAX9451/MAX9452 compare the frequency of the phase-detector input with the output frequency of the loop frequency divider. When these two frequencies deviate more than 20ppm, the $\overline{LOCK}$ output goes high. At power-up, $\overline{LOCK}$ is high. $\overline{LOCK}$ goes low when the PLL locks. PLL lock time also depends on the loop filter bandwidth.

## Table 1. Output Frequency Selection and Register Content Values

| 10 GIGABIT ETHERNET | | | | | SONET | | | | |
|---|---|---|---|---|---|---|---|---|---|
| INPUT CLK: 50MHz | | | | | INPUT CLK: 19.44MHz | | | | |
| CRYSTAL FREQUENCY (MHz) | P | M | Ni | OUTPUT FREQUENCY (MHz) | CRYSTAL FREQUENCY (MHz) | P | M | Ni | OUTPUT FREQUENCY (MHz) |
| 50 | 2 | 2 | 1 | 50 | 51.84 | 1 | 8 | 1 | 51.84 |
| 125 | 2 | 5 | 2 | 62.5 | 77.76 | 1 | 4 | 1 | 77.76 |
| 125 | 2 | 5 | 1 | 125 | 155.52 | 1 | 8 | 1 | 155.52 |
| — | — | — | — | — | 155.52 | 1 | 4 | 2 | 77.76 |

**MAX9450/MAX9451/MAX9452**

### External Loop Filter

When the device switches from one input reference to the other or reverts to an input reference from holdover, the output phase changes smoothly during the transition due to the narrowband external PLL filter. The narrower the filter bandwidth is, the smoother the phase transition. However, if bandwidth is too narrow, it can cause some degradation on output jitter performance.

### Charge-Pump Current Setting

The MAX9450/MAX9451/MAX9452 allow external setting of the charge-pump current in the PLL. Connect a resistor from RJ to GNDA to set the PLL charge-pump current:

$$\text{charge-pump current (μA)} = 2.48 \times 1000 / (R_{SET} (kΩ) + 0.375)$$

where $R_{SET}$ is in kΩ and the value of the charge-pump current is in μA. Use $R_{SET}$ to adjust the loop response to meet individual application requirements. The charge-pump current and the external filter components change the PLL bandwidth. Table 11 shows the charge-pump current vs. the resistor's value.

The loop response equation is defined as:

$$\text{unity-gain bandwidth} = (I_{CP} \times R_{FILT} \times 12kHz) / M$$

where $I_{CP}$ is the charge-pump current set by REXT, $R_{FILT}$ is the external filter resistance, and M is the feedback divider.

### Input Disable

The two inputs can be disabled separately by SEL0 and SEL1 or the 2 bits in CR5[3:2]. Table 2 shows the state map.

### Power-Up and Master Reset

Upon power-up, default frequency divider rates and the states of the monitor, inputs, and outputs are set according to Table 10. Setting MR high or CR6[4] to 1 also resets the device. When the device resets, INT and CR7[5:6] go low and all the registers revert to their default values.

## Table 2. Input Activation by SEL0, SEL1, or CR5[3:2]

| SEL1 | SEL0 | CR5[3:2] | IN1 | IN0 |
|------|------|----------|-----|-----|
| 0 | 0 | 00 | Disabled | Disabled |
| 0 | 1 | 00 | Disabled | Enabled |
| 1 | 0 | 00 | Enabled | Disabled |
| 1 | 1 | 00 | Enabled | Enabled |
| X | X | 01 | Disabled | Enabled |
| X | X | 10 | Enabled | Disabled |
| X | X | 11 | Enabled | Enabled |

### I²C Interface

The control interface of the MAX9450/MAX9451/MAX9452 is an I²C or SPI depending on the states of AD0 and AD1. Drive both AD0 and AD1 high to active SPI mode. Otherwise, I²C is activated. The device operates as a slave that sends and receives data through the clock line, SCL, and data line, SDA, to achieve bidirectional communication with the masters. A master (typically a microcontroller) initiates all data transfers to and from slaves, and generates the SCL clock that synchronizes the data transfer. Figure 4 shows the timing of SCL and SDA. The SDA line operates as both an input and an open-drain output. SDA requires a pullup resistor, typically 4.7kΩ. The SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire bus, or if the master in a single-master system has an open-drain SCL output.

### I²C Device Address

Every I²C port has a 7-bit device address. This 7-bit address is the slave (MAX9450/MAX9451/MAX9452) ID for the master to write and read. In the MAX9450/MAX9451/MAX9452, the first 4 bits (1101) of the address are hard coded into the device at the factory. See Table 3. The last 3 bits of the address are input programmable by the three-level AD0 and AD1. This configuration provides eight selectable addresses for the MAX9450/MAX9451/MAX9452, allowing eight devices to be connected to one master.

### START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. The active master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3). The interval between a START and a STOP is called a session.
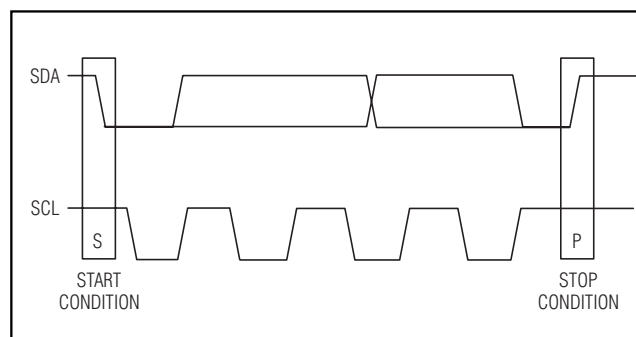


Figure 3. START and STOP Conditions

# High-Precision Clock Generators with Integrated VCXO

## Data Transfer and Acknowledge

Following the START condition, each SCL clock pulse transfers 1 bit. Between a START and a STOP, multiple bytes can be transferred on the 2-wire bus. The first 7 bits (B0–B6) are for the device address. The eighth bit (B7) indicates the writing (low) or reading (high) operation (W/R). The ninth bit (B8) is the ACK for the address and operation type. A low ACK bit indicates a successful transfer; otherwise, a high ACK bit indicates an unsuccessful transfer. The next 8 bits (register address), B9–B16, form the address byte for the control register to be written (Figure 4). The next bit, bit 17, is the ACK for the register address byte. The following byte (Data1) is the content to be written into the addressed register of the slave. After this, the address counter of I²C is increased by 1 (Rgst Addr + 1) and the next byte (Data2) writes into a new register. To read the contents in the MAX9450/MAX9451/MAX9452s' control registers, the master sends the register address to be read to the slave by a writing operation. Then it sends the byte of device address + R to the slave. The slave (MAX9450/MAX9451/MAX9452) responds with the content bytes from the registers, starting from the pointed register to the last register, CR8, consecutively back to the master (Figures 5 and 6).
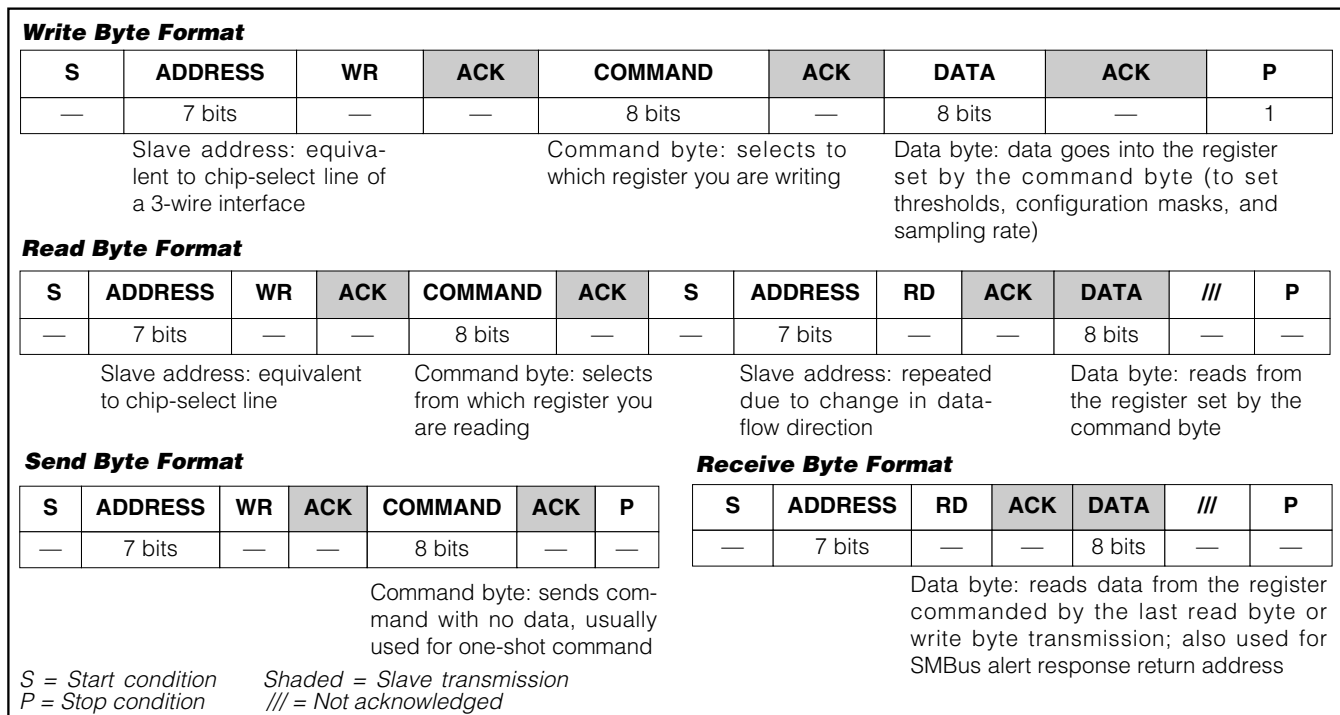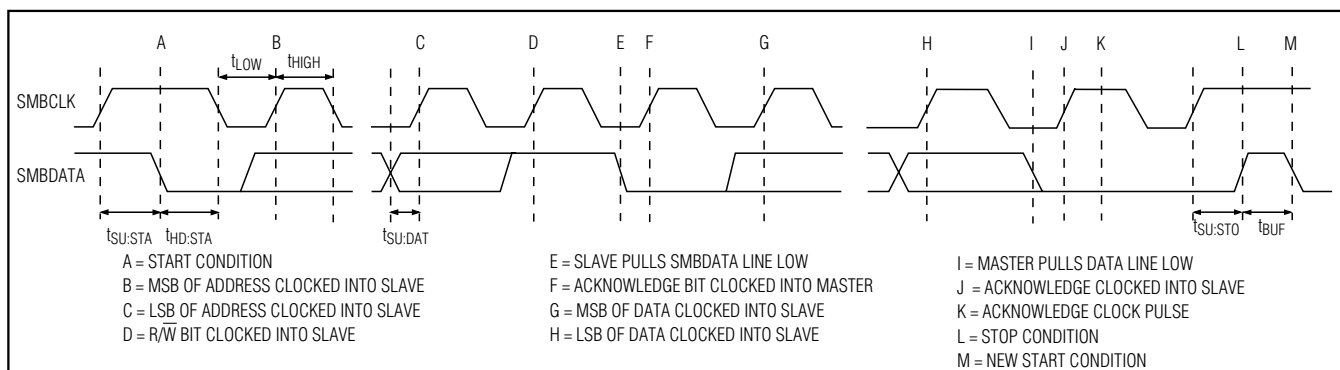
### Write Byte Format

| S | ADDRESS | WR | ACK | COMMAND | ACK | DATA | ACK | P |
|---|---------|----|----|---------|-----|------|-----|---|
| — | 7 bits | — | — | 8 bits | — | 8 bits | — | 1 |

Slave address: equivalent to chip-select line of a 3-wire interface

Command byte: selects to which register you are writing

Data byte: data goes into the register set by the command byte (to set thresholds, configuration masks, and sampling rate)

### Read Byte Format

| S | ADDRESS | WR | ACK | COMMAND | ACK | S | ADDRESS | RD | ACK | DATA | /// | P |
|---|---------|----|-----|---------|-----|---|---------|----|-----|------|-----|---|
| — | 7 bits | — | — | 8 bits | — | — | 7 bits | — | — | 8 bits | — | — |

Slave address: equivalent to chip-select line

Command byte: selects from which register you are reading

Slave address: repeated due to change in data-flow direction

Data byte: reads from the register set by the command byte

### Send Byte Format

| S | ADDRESS | WR | ACK | COMMAND | ACK | P |
|---|---------|----|-----|---------|-----|---|
| — | 7 bits | — | — | 8 bits | — | — |

Command byte: sends command with no data, usually used for one-shot command

### Receive Byte Format

| S | ADDRESS | RD | ACK | DATA | /// | P |
|---|---------|----|-----|------|-----|---|
| — | 7 bits | — | — | 8 bits | — | — |

Data byte: reads data from the register commanded by the last read byte or write byte transmission; also used for SMBus alert response return address

S = Start condition    Shaded = Slave transmission
P = Stop condition    /// = Not acknowledged

Figure 4. I²C Interface Data Structure



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/W̄ BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO SLAVE
H = LSB OF DATA CLOCKED INTO SLAVE
I = MASTER PULLS DATA LINE LOW
J = ACKNOWLEDGE CLOCKED INTO SLAVE
K = ACKNOWLEDGE CLOCK PULSE
L = STOP CONDITION
M = NEW START CONDITION

Figure 5. SMBus Write Timing Diagram
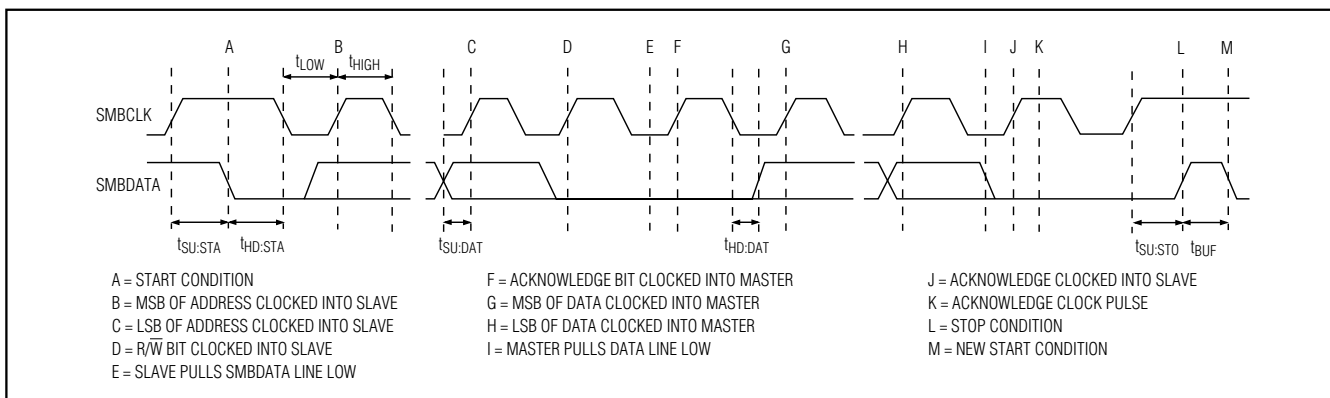
**MAX9450/MAX9451/MAX9452**



Figure 6. SMBus Read Timing Diagram

### SPI Interface

The SPI interface is activated when AD0 = AD1 = high. The SPI port is a write-only interface, and it uses the three inputs: $\overline{CS}$, SCL, and SDA. Bit D15 is always zero, indicating the write-only mode, as shown in Figure 5. D14–D8 are the register address bits and D7–D0 are the data bits. In Table 4, the register address mapping is still valid, except the first address bit on the left is not used. D14 is the MSB of the address, and D7 is the MSB of the data. D15–D0 are sent with MSB (D15) first. The maximum SCL frequency is 2MHz.

To perform a write, set D15 = 0, drive $\overline{CS}$ low, toggle SCL to latch SDA data on the rising edge, then drive $\overline{CS}$ high after 16 SCL cycles for two SCL cycles to signal the boundary of a 16-bit word (Figure 5). SCL must be low when $\overline{CS}$ falls at the start of a transmission. Switching of SCL and SDA is ignored unless $\overline{CS}$ is low. Figure 7 shows the SPI write operation timing diagram and Figure 8 shows SPI register address and data configuration function setting tables.
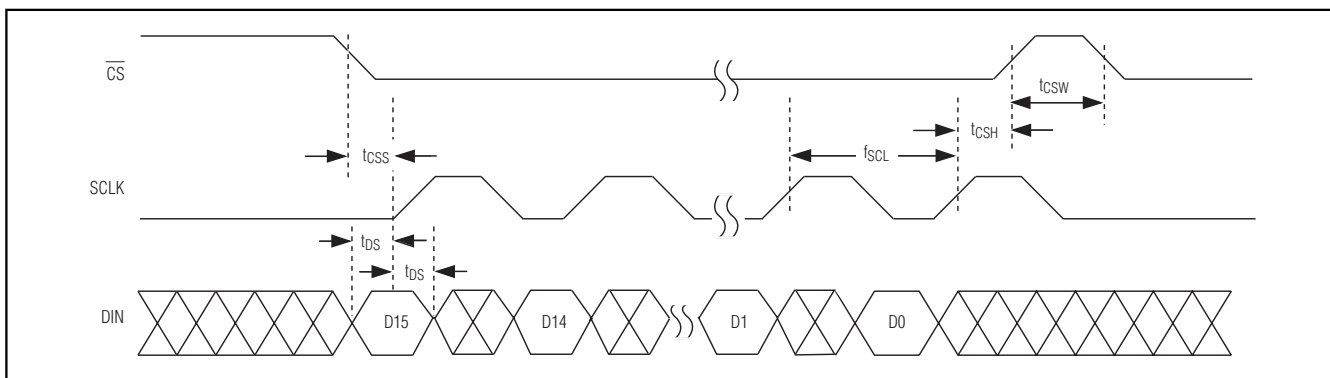


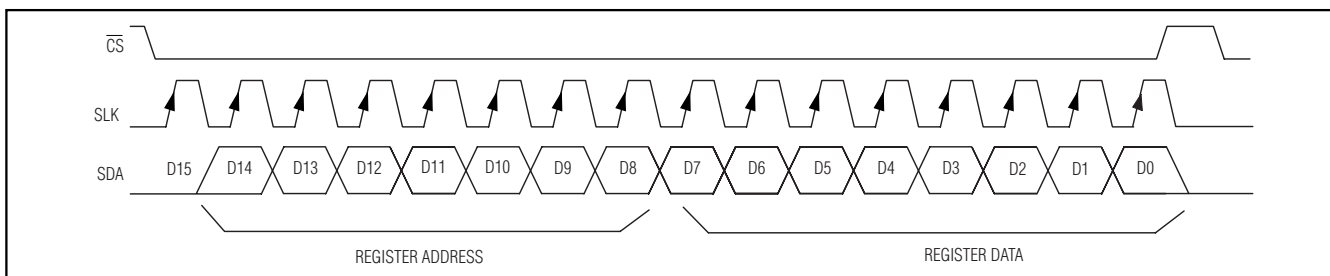Figure 7. SPI Write Operation Timing Diagram



Figure 8. SPI Register Address and Data Configuration Function Setting Tables

### Table 3. I²C Address Setting by AD0 and AD1

| AD0 | AD1 | ADDRESS |
|------|------|---------|
| Low | Low | 1101000 |
| Low | Open | 1101001 |
| Low | High | 1101010 |
| Open | Low | 1101011 |
| Open | Open | 1101100 |
| Open | High | 1101101 |
| High | Low | 1101110 |
| High | Open | 1101111 |
| High | High | Convert to SPI |

### Table 4. I²C and SPI Register Address*

| REGISTER NAME | REGISTER ADDRESS | FUNCTION |
|---------------|------------------|----------|
| CR0 | 00000000 | P divider |
| CR1 | 00000001 | M divider byte 1 |
| CR2 | 00000010 | M divider byte 2 |
| CR3 | 00000011 | N1 divider |
| CR4 | 00000100 | N2 divider |
| CR5 | 00000101 | Control |
| CR6 | 00000110 | Control |
| CR7 | 00000111 | Status |
| CR8 | 00001000 | Reserved |

*When the SPI port is activated, the first address bit on the left is omitted and the remaining 7 bits are used. The LSB is the first bit on the right.

### Table 5. Dividing Rate Setting for P Divider

| CR0 | DIVIDING RATE FOR P |
|-----|---------------------|
| 0000-0000 | 1 |
| 0000-0001 | 2 |
| — | — |
| 1111-1110 | 255 |
| 1111-1111 | 256 |

### Table 6. Dividing Rate Setting for M Divider

| CR1 | CR2[7:1]* | DIVIDING VALUE OF M |
|-----|-----------|---------------------|
| 0000-0000 | 0000-000 | 1 |
| 0000-0000 | 0000-001 | 2 |
| — | — | — |
| 1111-1111 | 0011-110 | 8191 |
| 1111-1111 | 0011-111 | 8192 |
| 1111-1111 | 1111-111 | 32,768 |

*CR2[0], the last LSB, is reserved.

### Table 7. Dividing Rate Setting for N0 and N1 Divider

| CR3* | DIVIDING VALUE OF N0 | CR4* | DIVIDING VALUE OF N1 |
|------|----------------------|------|----------------------|
| 000XXXXX | 1 | 000XXXXX | 1 |
| 001XXXXX | 2 | 001XXXXX | 2 |
| 010XXXXX | 3 | 010XXXXX | 3 |
| 011XXXXX | 4 | 011XXXXX | 4 |
| 100XXXXX | 5 | 100XXXXX | 5 |
| 101XXXXX | 6 | 101XXXXX | 6 |
| 110XXXXX | 8 | 110XXXXX | 8 |
| 111XXXXX | 16 | 111XXXXX | 16 |

*The last 5 LSBs of CR3[4:0] and CR4[4:0] are reserved.

*MAX9450/MAX9451/MAX9452*

## Table 8. Control Registers and Control Functions

| CR5, CR6 | FUNCTION | STATE |
|---|---|---|
| CR5[7] | Output disable | 0: Outputs are enabled<br>1: Outputs disabled to logic-low |
| CR5[6] | CLK0 enabling | 0: CLK0 is disabled to high impedance (overrides CR5[7] = 1 setting)<br>1: CLK0 is enabled |
| CR5[5] | CLK1 enabling | 0: CLK1 is disabled to high impedance (overrides CR5[7] = 1 setting)<br>1: CLK1 is enabled |
| CR5[4] | Default input setting | 0: IN0 is the default input<br>1: IN1 is the default input |
| CR5[3:2] | Input enabling | 00: The selection is controlled by SEL0, SEL1 (see Table 2)<br>01: Enable IN0, disable IN1<br>10: Enable IN1, disable IN0<br>11: Enable both IN0 and IN1 |
| CR5[1] | Revert function | 0: The function is not activated<br>1: The function is activated |
| CR5[0] | CLK monitor reset | CLK monitor is reset in revert mode: INT = 0 and CR7[7] = 0, and the PLL switches to the default input |
| CR6[7] | Holdover function enabling | 0: Holdover function is disabled<br>1: Holdover function is enabled |
| CR6[6] | Forced holdover | 0: Holdover is in normal mode<br>1: Holdover is forced to be activated<br>As the bit goes from 0 to 1, the current VCXO frequency is taken as the nominal value |
| CR6[5] | Acquiring nominal VCXO frequency | As this bit is toggling from 0 to 1, the current VCXO frequency is taking as the nominal holdover value |
| CR6[4] | Master reset | The bit acts at the same as the input MR; CR6[4] = 1, the chip is reset |
| CR6[3] | REF | This bit is always set to zero |
| CR6[2] | ODIV select | CR6[2] = 0: DIV0 output drives CLK2<br>CR6[2] = 1: DIV1 output drives CLK2 |
| CR6[1] | Acquire select | CR6[1] = 0 PLL controls the Xtal frequency<br>CR6[1] = 1 Xtal frequency is controlled by the acquired value (acquired at rising edge of CR6[5]) |
| CR6[0] | Reserved | — |

## Table 9. Mapping for the Input Monitor Status

| CR7 | FUNCTION | STATE |
|---|---|---|
| CR7[6] | Status of IN0 | 0: Normal<br>1: Failure detected |
| CR7[5] | Status of IN1 | |
| CR7[4] | Input clock selection indicator | 0: IN0 is currently used<br>1: IN1 is currently used |
| CR7[3] | LOCK indicator | 1: PLL not locked<br>0: PLL locked |
| CR7[2] | Holdover status | 1: Device is in holdover state<br>0: Device is in normal state |
| CR7[1:0] | Reserved | — |

## Table 10. Register Default Values at Power-Up

| REGISTER | ACTION | DEFAULT |
|---|---|---|
| CR0 | P = 1 | 00000000 |
| CR1 | M = 1 | 00000000 |
| CR2 | M = 1 | 00000000 |
| CR3 | N0 = 1 | 00000000 |
| CR4 | N1 = 1 | 00000000 |
| CR5, CR6 | 1. Outputs enable<br>2. IN0 is the default input<br>3. Both inputs are enabled by SEL0 and SEL1<br>4. Monitor is nonrevertive<br>5. Holdover is disabled | CR5: 01100000<br>CR6: 00000000 |
| CR7 | Status | 00000000 |
| CR8 | Reserved | 00000000 |

**Table 11. Resistor Value vs. Charge-Pump Current**

| RESISTOR (kΩ) | CURRENT (µA) |
|---|---|
| 12 | 200.5 |
| 20 | 121.88 |
| 50 | 49.41 |
| 100 | 24.86 |
| 150 | 16.61 |
| 200 | 12.48 |

## _____Applications Information

### Crystal Selection

The MAX9450/MAX9451/MAX9452 internal VCXO circuitry requires an external crystal. The frequency of the crystal ranges from 15MHz to 160MHz, depending on the application. It is important to use a quartz crystal that prevents reduction of the frequency pulling range, temperature stability, or excessive output phase jitter. Choose an AT-cut crystal that oscillates at the required frequency on its fundamental mode with a variation of 25ppm, including frequency accuracy and operating temperature range. Select a crystal with a load capacitance of 8pF and a motional capacitance of at least 7fF to achieve the specified pulling range.

Crystals from manufacturers KDS (www.kdsj.co.jp) and 4Timing (www.4timing.com) are recommended.

### LVDS Cables and Connectors

The interconnect for LVDS typically has a 100Ω differential impedance. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic-field-canceling effects.

### Power-Supply Bypassing

Bypass $V_{DDA}$, $V_{DD}$, and $V_{DDQ}$ to ground with high-frequency, surface-mount ceramic 0.1µF and 0.01µF capacitors. Place the capacitors as close as possible to the device with the 0.01µF capacitor closest to the device pins.

### Board Layout

Circuit-board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω (100Ω for LVDS outputs) characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or vias. Ensure the two traces are parallel and close to each other to increase common-mode noise immunity and reduce EMI. Matching the electrical length of the differential traces further reduces signal skew.

### Output Termination

Terminate the MAX9450 outputs with 50Ω to $V_{CC}$ - 2V or use an equivalent thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs.

The MAX9452 outputs are specified for a 100Ω load, but can drive 90Ω to 132Ω to accommodate various types of interconnects. The termination resistor at the driven receiver should match the differential characteristic impedance of the interconnect and be located close to the receiver input. Use a ±1% surface-mount termination resistor.
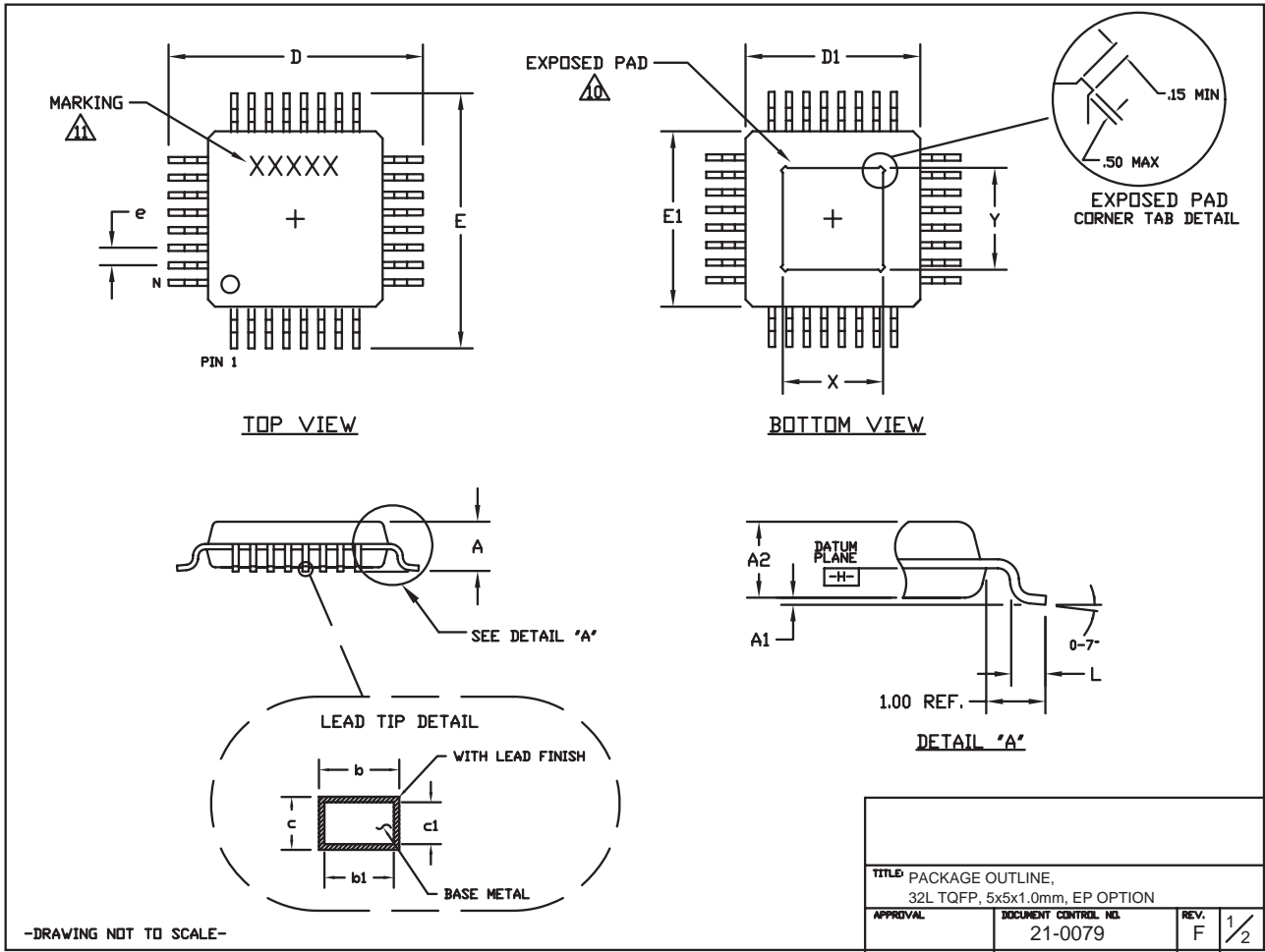
## _____Chip Information

PROCESS: CMOS

# High-Precision Clock Generators
# with Integrated VCXO

_____ *Package Information*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.microsemi.com.)



TOP VIEW

BOTTOM VIEW

EXPOSED PAD
CORNER TAB DETAIL

.15 MIN

.50 MAX

SEE DETAIL 'A'

LEAD TIP DETAIL

WITH LEAD FINISH

BASE METAL

DETAIL 'A'

DATUM PLANE

1.00 REF.

0-7°

32L,TQFP.EPS

-DRAWING NOT TO SCALE-

| TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0mm, EP OPTION | | | |
|---|---|---|---|
| APPROVAL | DOCUMENT CONTROL NO. 21-0079 | REV. F | 1/2 |

## Package Information (continued)

**NOTES:**

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

| COMMON DIMENSIONS | | |
|---|---|---|
| DIMENSIONS IN MILLIMETERS | | |
| JEDEC AAA-HD | | |
| 5x5x1.0 MM | | |
| | MIN. | MAX. |
| A | ~ | 1.20 |
| $A_1$ | 0.05 | 0.15 |
| $A_2$ | 0.95 | 1.05 |
| D | 6.80 | 7.20 |
| $D_1$ | 4.80 | 5.20 |
| E | 6.80 | 7.20 |
| $E_1$ | 4.80 | 5.20 |
| L | 0.45 | 0.75 |
| N | 32 | |
| e | 0.50 BSC. | |
| b | 0.17 | 0.27 |
| b1 | 0.17 | 0.23 |
| c | 0.09 | 0.20 |
| c1 | 0.09 | 0.16 |
| X | 2.70 | 3.30 |
| Y | 2.70 | 3.30 |

| TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0mm, EP OPTION | | | | |
|---|---|---|---|---|
| APPROVAL | DOCUMENT CONTROL NO. 21-0079 | REV. F | 2/2 | |

-DRAWING NOT TO SCALE-

# High-Precision Clock Generators
## with Integrated VCXO

| REVISION NUMBER | REVISION DATE | REVISION DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | — | Initial release | — |
| 1 | — | Various changes | — |
| 2 | 9/06 | Various changes | 1–4, 7–10, 12, 15, 16 |
| 3 | 11/07 | Fixed typo in crystal frequency range (*Functional Diagram)* | 7 |

MAX9450/MAX9451/MAX9452

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