



NPN/PNP Silicon Complementary Small Signal Dual Transistor Qualified per MIL-PRF-19500/421

Qualified Levels: JAN, JANTX, and **JANTXV**

DESCRIPTION

This 2N4854U device in a low profile 6-pin U package is military qualified up to a JANTXV level for high-reliability applications. Microsemi also offers numerous other products to meet higher and lower power voltage regulation applications.

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FEATURES

- Surface mount equivalent of JEDEC registered 2N4854
- JAN, JANTX, and JANTXV qualifications also available per MIL-PRF-19500/421
- RoHS compliant versions available (commercial grade only)



6-Pin "U" Package

APPLICATIONS / BENEFITS

- Low-profile and compact package design
- Lightweight

Also available in:





芃 6-Pin Flatpack package

MAXIMUM RATINGS

Parameters/Test Conditions	Symbol	Value per		Unit
		Each Transistor	Total Package	
Thermal Resistance Surface Mount Junction-to- Solder Point	R _{OJSP}	110	90	°C/W
Thermal Resistance Junction-to-Ambient (3)	$R_{\Theta JA}$	350	290	°C/W
Total Power Dissipation @ T _A = +25 °C ⁽¹⁾	P _T	0.30	0.60	W
Total Power Dissipation @ T _C = +25 °C (2)	P _T	1.0	2.0	W
Junction and Storage Temperature	T _J and T _{STG}	-65 to +200		°C
Collector-Base Voltage, Emitter Open	V_{CBO}	60		V
Emitter-Base Voltage, Collector Open	V_{EBO}	5		V
Collector-Emitter Voltage, Base Open	V_{CEO}	40		V
Collector Current, dc	Ic	600		mA
Lead to Case Voltage		+/- 120		V
Solder Temperature @ 10 s		260		°C

Notes: 1. For T_A > +25°C, derate linearly 1.71 mW/°C one transistor, 3.43 mW/°C both transistors.

- 2. For $T_C > +25$ °C, derate linearly 5.71 mW/°C one transistor, 11.43 mW/°C both transistors.
- 3. Ambient equates to PCB FR4 mounting (R_{EJPCB}) in Figure 2 and MIL-PRF-19500/421.

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MECHANICAL and PACKAGING

• CASE: Hermetically sealed ceramic (black), Au over Ni plated kovar lid

• TERMINALS: Au over Ni plated metallization

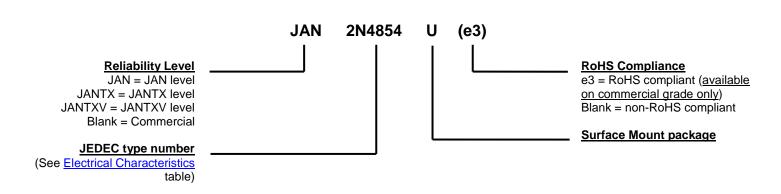
MARKING: Manufacturer's ID, part number, date code

POLARITY: See case outline.

• WEIGHT: 0.158 grams

• See Package Dimensions on last page.

PART NOMENCLATURE



SYMBOLS & DEFINITIONS				
Symbol	Definition			
Ι _Β	Base current: The value of the dc current into the base terminal.			
Ic	Collector current: The value of the dc current into the collector terminal.			
Ι _Ε	Emitter current: The value of the dc current into the emitter terminal.			
V _{CB}	Collector-base voltage: The dc voltage between the collector and the base.			
V _{CBO}	Collector-base voltage, base open: The voltage between the collector and base terminals when the emitter terminal is open-circuited.			
V_{CE}	Collector-emitter voltage: The dc voltage between the collector and the emitter.			
V _{CEO}	Collector-emitter voltage, base open: The voltage between the collector and the emitter terminals when the base terminal is open-circuited.			
V _{EB}	Emitter-base voltage: The dc voltage between the emitter and the base.			
V _{EBO}	Emitter-base voltage, collector open: The voltage between the emitter and base terminals with the collector terminal open-circuited.			



ELECTRICAL CHARACTERISTICS @ T_A= 25 °C unless otherwise noted

Characteristics	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS		•		
Collector-Emitter Breakdown Current	V(DD) 050	40		V
$I_C = 10 \text{ mA (pulsed)}$	V _{(BR)CEO}	40		V
Collector-Base Cutoff Current	lana		10	
$V_{CB} = 60 \text{ V}$	I _{CBO(1)}		10	μΑ
Collector-Base Cutoff Current	lono(a)		10	nA
$V_{CB} = 50 \text{ V}$	I _{CBO(2)}		10	ш
Emitter-Base Cutoff Current				
$V_{EB} = 5.0 \text{ V}$	I _{EBO(1)}		10	μΑ
$V_{EB} = 3.0 \text{ V}$	I _{EBO(2)}		10	nA
ON CHARACTERISTICS				
Forward-Current Transfer Ratio				
$I_C = 150 \text{ mA}, V_{CE} = 1 \text{ V}$	h _{FE}	50		
$I_C = 100 \mu\text{A}, \ V_{CE} = 10 \text{V}$		35		
$I_C = 1.0 \text{ mA}, V_{CE} = 10 \text{ V}$		50		
$I_C = 10 \text{ mA}, V_{CE} = 10 \text{ V}$		75		
$I_C = 150 \text{ mA}, V_{CE} = 10 \text{ V}$		100	300	
$I_C = 300 \text{ mA}, V_{CE} = 10 \text{ V}$		35		
Collector-Emitter Saturation Voltage	V _{CE(sat)}		0.40	V
$I_C = 150 \text{ mA}, I_B = 15 \text{ mA}$	OL(Sat)			
Base-Emitter Saturation Voltage	V _{BE(sat)}	0.80	1.25	V
$I_C = 150 \text{ mA}, I_B = 15 \text{ mA}$	VBE(sat)	0.00	1.20	•
DYNAMIC CHARACTERISTICS	·	-I		l.
Forward Current Transfer Ratio	h.,	-00	200	
$I_C = 1.0 \text{ mA}, V_{CE} = 10 \text{ V}, f = 1.0 \text{ kHz}$	h _{fe}	60	300	
Forward Current Transfer Ratio, Magnitude	lha I	2.0	40	
$I_C = 20 \text{ mA}, V_{CE} = 10 \text{ V}, f = 100 \text{ MHz}$	h _{fe}	2.0	10	
Small-Signal Common Emitter Input Impedance	1.	4.5	0.0	1.0
$I_C = 1.0 \text{ mA}, V_{CE} = 10 \text{ V}, f = 1.0 \text{ kHz}$	h _{ie}	1.5	9.0	kΩ
Small-Signal Common Emitter Output Admittance			50	
$I_C = 1.0 \text{ mA}, V_{CE} = 10 \text{ V}, f = 1.0 \text{ kHz}$	hoe		50	μhmo
Open Circuit Output Capacitance	0		0.0	
$V_{CB} = 10 \text{ V}, I_{E} = 0, 100 \text{ kHz} \le f \le 1.0 \text{ MHz}$	C _{obo}		8.0	pF
Noise Figure	NE		0.0	٩D
$I_C = 100 \mu A$, $V_{CE} = 10 V$, $f = 1.0 kHz$, $R_G = 1.0 kΩ$	NF		8.0	dB
SWITCHING CHARACTERISTICS				I
Turn-On Time (Saturated)	+		45	no
(Reference MIL-PRF-19500/421, figure 7)	t _{on}		45	ns
Turn-Off Time (Saturated)	t		300	ns
(Reference MIL-PRF-19500/421, figure 8)	t _{off}		300	113
Pulse Response (Non-Saturated)	t. t.,		18	ns
(Reference MIL-PRF-19500/421, figure 9)	ton + toff		10	113
(Reference Mile-1 RF - 13500/421, figure 3)				



GRAPHS

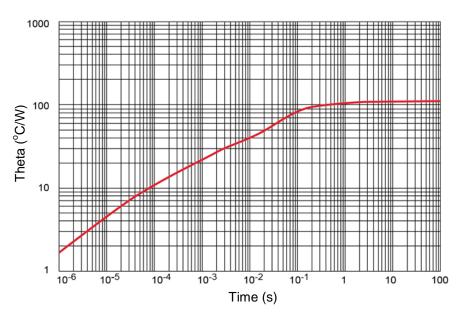


FIGURE 1
Thermal impedance graph (Røjsp)

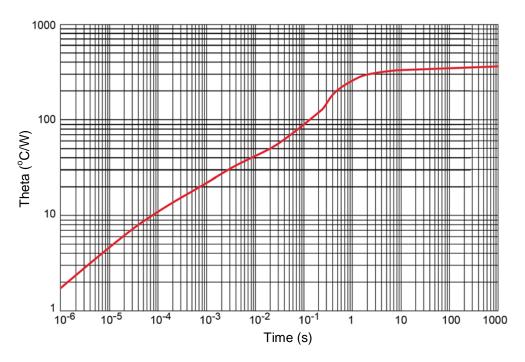
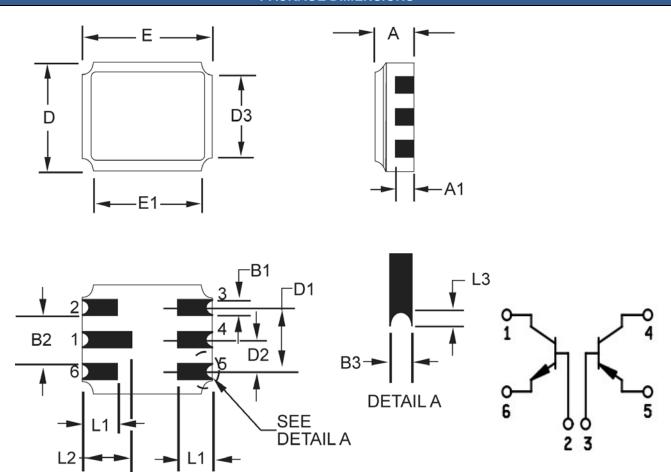


FIGURE 2

Thermal impedance graph (RøJPCB)



PACKAGE DIMENSIONS



	Dimension				
Ltr	Inch		Millimeters		Notes
	Min	Max	Min	Max	
Α	.058	.100	1.47	2.54	
A1	.026	.039	0.66	0.99	
B1	.022	.028	0.56	0.71	
B2	.072 Ref.		1.83 Ref.		
B3	.006	.022	0.15	0.56	
D	.165	.175	4.19	4.45	
D1	.095	.105	2.41	2.67	

		Dimensions			
Ltr	Inch		Millimeters		Notes
	Min	Max	Min	Max	
D2	.045	.055	1.14	1.40	
D3		.175		4.45	
Е	.240	.250	6.10	6.35	
E1		.250		6.35	
L1	.060	.070	1.52	1.78	
L2	.082	.098	2.08	2.49	
L3	.003	.007	0.08	0.18	

NOTES:

- 1. Dimensions are in inches.
- 2. Millimeters are given for general information only.
- 3. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.

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