LAN8841

Gigabit Ethernet Transceiver with GMII/MII/ RGMII and IEEE 1588v2 Support

Features

- Single-Chip 10/100/1000 Mbps Ethernet Transceiver Suitable for IEEE 802.3 Applications
- GMII/MII Standard Interface with 3.3V/2.5V/1.8V I/Os
- RGMII with 3.3V/2.5V/1.8V I/Os
  - RGMII Timing Supports On-Chip Delay According to RGMII Version 2.0, with Programming Options for External Delay and Making Adjustments and Corrections to TX and RX Timing Paths
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100/1000 Mbps) and Duplex (Half/Full)
- On-Chip Termination Resistors for the Differential Pairs
- On-Chip LDO Controller to Support Single 3.3V Supply Operation
- Jumbo Frame Support Up to 16 KB
- 125 MHz Reference Clock Output
- Energy-Detect Power-Down Mode for Reduced Power Consumption When Cable is Not Attached
- EtherSynch® IEEE 1588v2/PTP
  - Layer 2, UDP/IPv4 and UDP/IPv6 formats
  - Tagged and non-tagged frame formats
  - One-step and two-step modes of operation
- Energy Efficient Ethernet (EEE) Support with Low-Power Idle (LPI) Mode and Clock Stoppage for 100BASE-TX/1000BASE-T and Transmit Amplitude Reduction with 10BASE-Te Option
- Wake-On-LAN (WOL) Support with Robust Custom-Packet Detection
- Programmable LED Outputs for Link, Activity, and Speed
- Baseline Wander Correction
- LinkMD® TDR-based Cable Diagnostic to Identify Faulty Copper Cabling
- Signal Quality Indication
- Parametric NAND Tree Support to Detect Faults Between Chip I/Os and Board
- Loopback Modes for Diagnostics
- Automatic MDI/MDI-X Crossover to Detect and Correct Pair Swap at All Speeds of Operation
- Automatic Detection and Correction of Pair Swaps, Pair Skew, and Pair Polarity
- MDC/MDIO Management Interface for PHY Register Configuration
- Interrupt Pin Option
- Power-Down and Power-Saving Modes
- Operating Voltages
  - Core (VDD, VDDAL, VDDAL_PLL)
  - VDD I/O (VDDIO): 3.3V, 2.5V, or 1.8V
  - Transceiver (VDDAH): 3.3V or 2.5V
- Available in commercial (0°C to +70°C) and extended industrial (-40°C to +105°C) temperature ranges
- 64-pin VQFN (8 mm × 8 mm) Package

Target Applications

- Industrial Control
- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-Top Box
- Game Console
- IP Camera
- Triple-Play (Data, Voice, Video) Media Center
- Media Converter

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
1000BASE-T	1 Gbps Ethernet over twisted pair, IEEE 802.3 compliant
100BASE-TX	100 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
10BASE-T	10 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
ADC	Analog-to-Digital Converter
AFE	Analog Front End
AN, ANEG	Auto-Negotiation
BYTE	8-bits
DA	Destination Address
DCQ	Dynamic Channel Quality
EEE	Energy Efficient Ethernet
FCS	Frame Check Sequence
FSM	Finite State Machine
GMII	Gigabit Media Independent Interface
GPIO	General Purpose I/O
HOST	External system (Includes processor, application software, etc.)
LDO	Linear Drop-Out Regulator
LFSR	Linear Feedback Shift Register
MAC	Media Access Controller
MAGJACK	Configuration strap for power modes.
MDI	Medium Dependent Interface
MDIX	Media Independent Interface with Crossover
MII	Media Independent Interface
MLT-3	Multi-Level Transmission Encoding (3-Levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”.
N/A	Not Applicable
OTP	One Time Programmable
PCS	Physical Coding Sublayer
PLL	Phase Locked Loop
POR	Power on Reset.
PTP	Precision Time Protocol

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TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RGMII	Reduced Gigabit Media Independent Interface
SA	Source Address
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame
SQI	Signal Quality Indicator
UDP	User Datagram Protocol - A connectionless protocol run on top of IP networks

1.2 Buffer Types

TABLE 1-2: BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
AI	Analog input
AO	Analog output
AIO	Analog bidirectional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
RGMII_O	RGMII compliant output
VIS	Variable voltage Schmitt-triggered input
VO5	Variable voltage output with 5 mA sink and 5 mA source
VO10	Variable voltage output with 10 mA sink and 10 mA source
VOD10	Variable voltage open-drain output with 10 mA sink
VOS10	Variable voltage open-source output with 10 mA source
PU	70 KΩ (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	70 KΩ (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
P	Power pin

Note: Digital signals are not 5V tolerant unless specified.

1.3 Reference Documents

1. *IEEE 802.3™-2022 IEEE Standard for Ethernet,* https://standards.ieee.org/ieee/802.3/10422/
2. *Reduced Gigabit Media Independent Interface (RGMII) Specification Version 2.0,* https://web.archive.org/web/20160303171328/http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf
3. *OPEN Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0* http://www.opensig.org/download/document/218/Advanced_PHY_features_for_automotive_Ethernet_V1.0.pdf

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2.0 INTRODUCTION

2.1 General Description

The LAN8841 is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical-layer transceiver for transmission and reception of data on standard CAT-5 as well as CAT-5e and CAT-6 unshielded twisted pair (UTP) cables.

The LAN8841 offers the industry-standard GMII/MII (Gigabit Media Independent Interface/Media Independent Interface) for connection to GMII/MII MACs in Gigabit Ethernet processors and switches for data transfer at 1000 Mbps or 10/100 Mbps. An optional RGMII (Reduced Gigabit Media Independent Interface) mode is also provided, allowing the device to provide additional GPIOs.

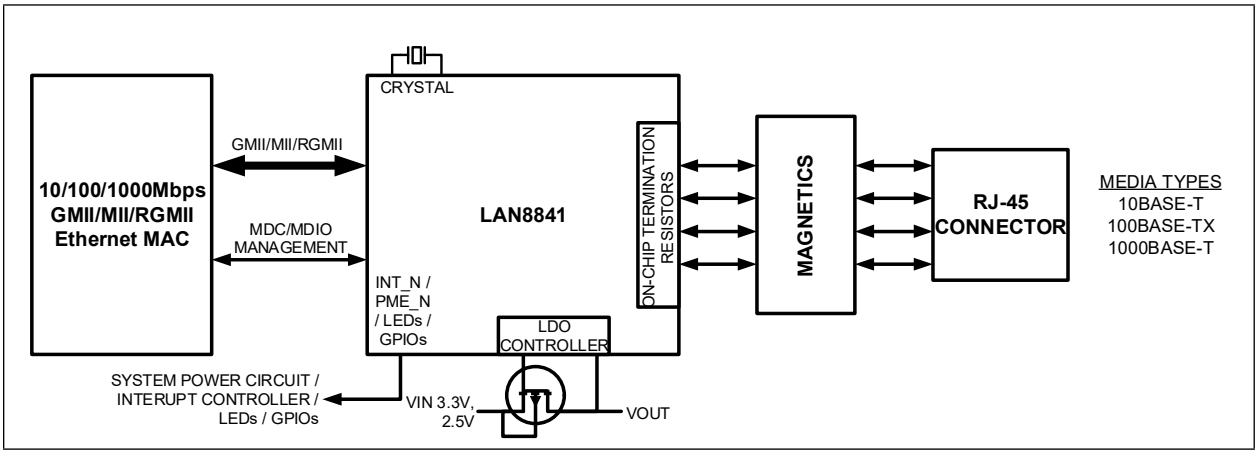
The IEEE1588-2008 PTP functions provide hardware support for the IEEE Std 1588-2008 (v2) Precision Time Protocol (PTP), allowing clock synchronization with remote Ethernet devices, packet time stamping, and time driven event generation. The device supports server or client modes for ordinary and boundary clock operations and a transparent clock per the IEEE Std 1588-2008 specification. End-to-end and peer-to-peer link delay mechanisms are supported as are one-step and two-step operations.

The LAN8841 reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the core voltage.

The LAN8841 offers diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between LAN8841 I/Os and the board. The LinkMD® TDR-based cable diagnostic identifies faulty copper cabling. Remote, external, and local loopback functions verify analog and digital data paths.

The LAN8841 is available in a 64-pin, RoHS Compliant VQFN package.

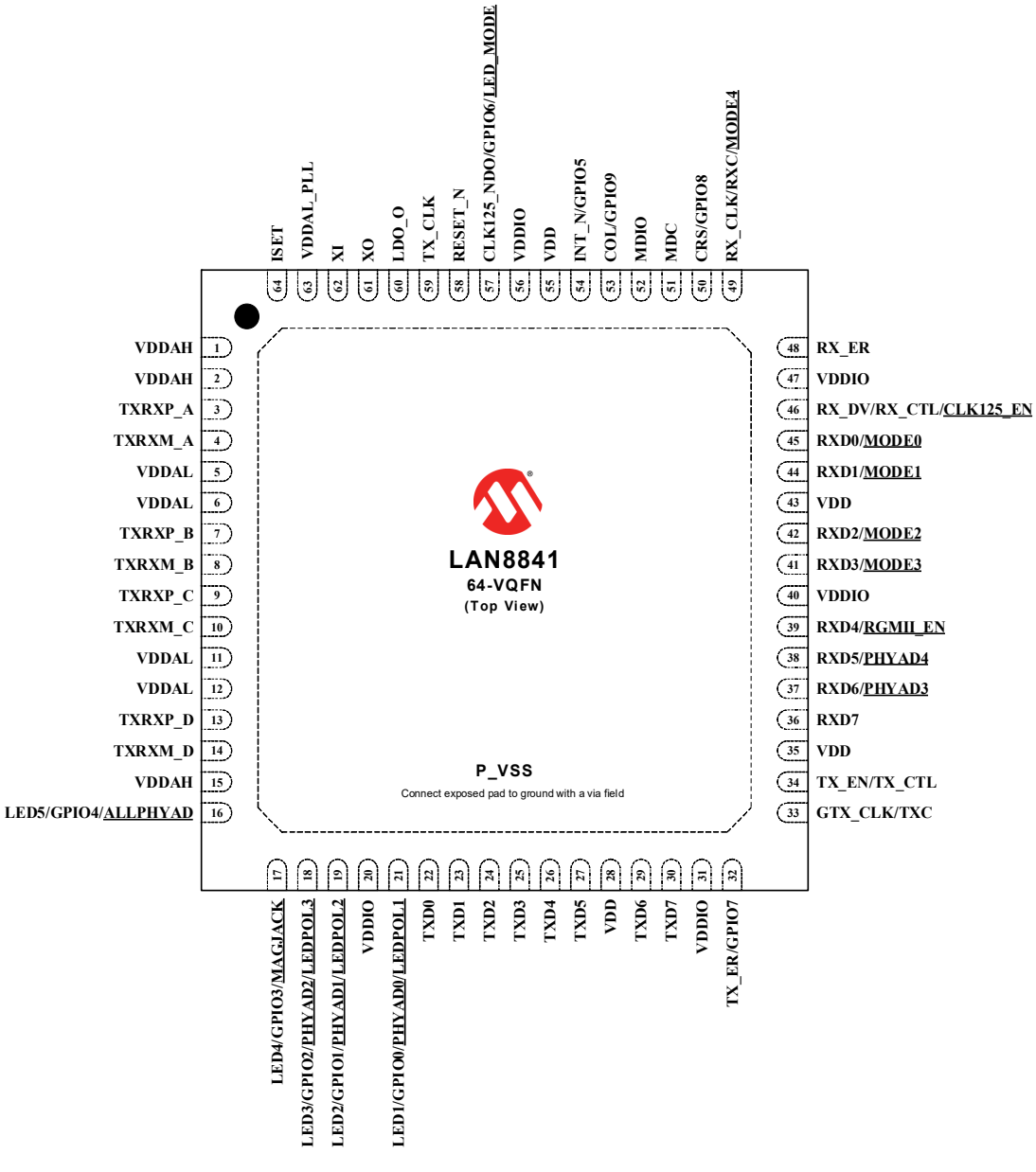
FIGURE 2-1: SYSTEM BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (**P_VSS**) on bottom of package must be connected to ground with a via field
Note: Configuration strap inputs are indicated with an underline
Note: PME_N, SOF_RX, SOF_TX, and 1588 event outputs are not shown since they can map to various GPIO pins

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TABLE 3-1: LAN8841 PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name
1	VDDAH	33	GTX_CLK/TXC
2	VDDAH	34	TX_EN/TX_CTL
3	TXRXP_A	35	VDD
4	TXRXM_A	36	RXD7
5	VDDAL	37	RXD6/PHYAD3
6	VDDAL	38	RXD5/PHYAD4
7	TXRXP_B	39	RXD4/RGMII_EN
8	TXRXM_B	40	VDDIO
9	TXRXP_C	41	RXD3/MODE3
10	TXRXM_C	42	RXD2/MODE2
11	VDDAL	43	VDD
12	VDDAL	44	RXD1/MODE1
13	TXRXP_D	45	RXD0/MODE0
14	TXRXM_D	46	RX_DV/RX_CTL/CLK125_EN
15	VDDAH	47	VDDIO
16	LED5/GPIO4/ALLPHYAD	48	RX_ER
17	LED4/GPIO3/MAGJACK	49	RX_CLK/RXC/MODE4
18	LED3/GPIO2/PHYAD2/LEDPOL3	50	CRS/GPIO8
19	LED2/GPIO1/PHYAD1/LEDPOL2	51	MDC
20	VDDIO	52	MDIO
21	LED1/GPIO0/PHYAD0/LEDPOL1	53	COL/GPIO9
22	TXD0	54	INT_N/GPIO5
23	TXD1	55	VDD
24	TXD2	56	VDDIO
25	TXD3	57	CLK125_NDO/GPIO6/LED_MODE
26	TXD4	58	RESET_N
27	TXD5	59	TX_CLK
28	VDD	60	LDO_O
29	TXD6	61	XO
30	TXD7	62	XI
31	VDDIO	63	VDDAL_PLL
32	TX_ER/GPIO7	64	ISET
Exposed Pad (P_VSS) must be connected to ground.			

3.2 Pin Descriptions

This section contains descriptions of the various LAN8841 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The pin function descriptions have been broken into functional groups as follows:

- Analog Front End
- GMII Interface
- RGMII Interface
- Crystal
- Miscellaneous
- Alternate Functions
- Strap Inputs
- I/O Power, Core Power and Ground

TABLE 3-2: ANALOG FRONT END

Name	Symbol	Buffer Type	Description
Ethernet TX/RX Positive Channel A	**TXRXP_A**	AIO	Media Dependent Interface[0], positive signal of differential pair 1000BT mode: **TXRXP_A** corresponds to BI_DA+. 10BT/100BTX mode: **TXRXP_A** is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively.
Ethernet TX/RX Negative Channel A	**TXRXM_A**	AIO	Media Dependent Interface[0], negative signal of differential pair 1000BT mode: **TXRXM_A** corresponds to BI_DA-. 10BT/100BTX mode: **TXRXM_A** is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively.
Ethernet TX/RX Positive Channel B	**TXRXP_B**	AIO	Media Dependent Interface[1], positive signal of differential pair 1000BT mode: **TXRXP_B** corresponds to BI_DB+. 10BT/100BTX mode: **TXRXP_B** is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively.
Ethernet TX/RX Negative Channel B	**TXRXM_B**	AIO	Media Dependent Interface[1], negative signal of differential pair 1000BT mode: **TXRXM_B** corresponds to BI_DB-. 10BT/100BTX mode: **TXRXP_B** is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively.

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TABLE 3-2: ANALOG FRONT END (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet TX/RX Positive Channel C	**TXRXP_C**	AIO	Media Dependent Interface[2], positive signal of differential pair 1000BT mode: **TXRXP_C** corresponds to BI_DC+. 10BT/100BTX mode: **TXRXP_C** is not used.
Ethernet TX/RX Negative Channel C	**TXRXM_C**	AIO	Media Dependent Interface[2], negative signal of differential pair 1000BT mode: **TXRXM_C** corresponds to BI_DC-. 10BT/100BTX mode: **TXRXM_C** is not used.
Ethernet TX/RX Positive Channel D	**TXRXP_D**	AIO	Media Dependent Interface[3], positive signal of differential pair 1000BT mode: **TXRXP_D** corresponds to BI_DD+. 10BT/100BTX mode: **TXRXP_D** is not used.
Ethernet TX/RX Negative Channel D	**TXRXM_D**	AIO	Media Dependent Interface[3], negative signal of differential pair 1000BT mode: **TXRXM_D** corresponds to BI_DD-. 10BT/100BTX mode: **TXRXM_D** is not used.

TABLE 3-3: GMII INTERFACE

Name	Symbol	Buffer Type	Description
Transmit Data	**TXD7** **TXD6** **TXD5** **TXD4** **TXD3** **TXD2** **TXD1** **TXD0**	VIS (PD)	The MAC transmits data to the PHY using these signals. **Note:** Bits 7-4 are not used in MII mode (10 and 100 Mbps). Internal pull-down resistors are enabled. **Note:** Bits 7-4 are not used in RGMII mode. Internal pull-down resistors are enabled.
Transmit Enable	**TX_EN**	VIS	Indicates the presence of valid data on **TXD**[7:0].
Transmit Error	**TX_ER**	VIS (PD)	Indicates a transmit error condition during frame transmission. Also used to request Low Power Idle for Energy Efficient Ethernet operation. **Note:** If the GMII/MII MAC does not provide the **TX_ER** output signal, this pin should have an external pull-down resistor or otherwise be tied low. **Note:** This pin is not used in RGMII mode. An internal pull-down resistor is enabled.
GMII Transmit Clock	**GTX_CLK**	VIS (PD)	GMII transmit reference clock. **Note:** This signal is not used in MII mode (10 and 100 Mbps). An internal pull-down resistor is enabled.

TABLE 3-3: GMII INTERFACE (CONTINUED)

Name	Symbol	Buffer Type	Description
MII Transmit Clock	**TX_CLK**	VO5 (PD)	MII transmit reference clock. **Note:** This signal is not used in GMII mode.
Collision Detect	**COL**	VO10 (PD)	Asserted to indicate detection of a collision condition. **Note:** Used in half-duplex mode only.
Carrier Sense	**CRS**	VO10 (PD)	Indicates detection of carrier. **Note:** Used in half-duplex mode only.
Receive Data	**RXD7** **RXD6** **RXD5** **RXD4** **RXD3** **RXD2** **RXD1** **RXD0**	VO5 (PD)	The PHY transfers data to the MAC using these signals. **Note:** Bits 7-4 are not used in MII mode and are driven low.
Receive Data Valid	**RX_DV**	VO5	Indicates that recovered and decoded data is being presented on the receive data pins.
Receive Error	**RX_ER**	VO5 (PD)	Asserted to indicate an error has been detected in the frame presently being transferred from the PHY. Also used to indicate Low Power Idle for Energy Efficient Ethernet operation.
Receive Clock	**RX_CLK**	VO5	Receive reference clock.

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TABLE 3-4: RGMII INTERFACE

Name	Symbol	Buffer Type	Description
Transmit Data	**TXD3** **TXD2** **TXD1** **TXD0**	VIS	The MAC transmits data to the PHY using these signals.
Transmit Control	**TX_CTL**	VIS	Indicates both the transmit data enable (TXEN) and transmit error (TXER) functions per the RGMII specification.
RGMII Transmit Clock	**TXC**	VIS	Used to latch data from the MAC into the PHY in RGMII mode. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz
Receive Data	**RXD3** **RXD2** **RXD1** **RXD0**	RGMII_O	The PHY transfers data to the MAC using these signals. The PHY's link status (speed, duplex and link) are indicated on these signals whenever Normal Data, Data Error, Carrier Extend, Carrier Sense, False Carrier or Lower Power Idle are not present.
Receive Control	**RX_CTL**	RGMII_O	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification.
RGMII Receive Clock	**RXC**	RGMII_O	Used to transfer data from the PHY to the MAC in RGMII mode. 1000BASE-T: 125MHz 100BASE-TX: 25MHz 10BASE-T: 2.5MHz

TABLE 3-5: CRYSTAL

Name	Symbol	BUFFER TYPE	DESCRIPTION
Crystal Input	**XI**	ICLK	When using a 25MHz crystal, this input is connected to one lead of the crystal. When using an clock source, this is the input from the oscillator. **Note:** The crystal or oscillator should have a tolerance of ±50ppm.
Crystal Output	**XO**	OCLK	When using a 25MHz crystal, this output is connected to one lead of the crystal. When using an external oscillator, this pin is not connected.

TABLE 3-6: MISCELLANEOUS

Name	Symbol	Buffer Type	Description
Indicator LEDs	**LED5** **LED4** **LED3** **LED2** **LED1**	VO10/ VOD10/ VOS10	Programmable LED outputs. The polarity of the pin depends upon the corresponding LED Polarity bit in the Output Control Register. The buffer type (push-pull or open-drain/open-source) depends on the setting of the corresponding LED Buffer Type bit in the Output Control Register. The polarity then determines open-drain (active low) and open-source (active high).
General Purpose I/O	**GPIO9** **GPIO8** **GPIO7** **GPIO6** **GPIO5** **GPIO4** **GPIO3** **GPIO2** **GPIO1** **GPIO0**	VIS/ VO10/ VOD10 (PU)	General purpose I/O The buffer type (push-pull or open-drain/open-source), direction, and pull-up depend on the settings in the GPIO registers. The GPIOs may be used to capture a 1588 timestamp and to clear the 1588 Local Time Counter event interrupts. GPIOs are shared with various pins.
Management Interface Data	**MDIO**	VIS/ VO10/ VOD10 (PU)	This is the management data from/to the MAC. **Note:** An external pull-up resistor to VDDIO in the range of 1.0 kΩ to 4.7 kΩ is required. (1.0 kΩ for high-speed MDIO operation). The buffer type (push-pull or open-drain/open-source) depends on the setting of the MDIO Buffer Type bit in the Output Control Register.
Management Interface Clock	**MDC**	VIS (PU)	This is the management clock input from the MAC.
PHY Interrupt	**INT_N**	VO10/ VOD10	Programmable interrupt output. The buffer type (push-pull or open-drain) depends on the setting of the INT Buffer Type bit in the Output Control Register and defaults to open-drain. The polarity depends on the setting of the Intr Polarity Invert bit in the Control Register and defaults to active low. **Note:** If the buffer type is set to open-drain, the polarity is forced to be active low.
CLK125 MHz	**CLK125_NDO**	VIS/ VO10	125 MHz clock output. This pin provides a 125 MHz reference clock output option for use by the MAC. This pin may also provide a 125 MHz clock output synchronous to the receive data for use in Synchronous Ethernet (SyncE) applications. This pin may also be used as the 1588 reference clock input.
System Reset	**RESET_N**	VIS (PU)	Chip reset (active low). Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N.

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TABLE 3-6: MISCELLANEOUS (CONTINUED)

Name	Symbol	Buffer Type	Description
LDO Controller Output	**LDO_O**	AO	On-chip core voltage LDO controller output. This pin drives the input gate of a P-channel MOSFET to generate the chip's core voltages. **Note:** If the system provides the core voltage, this pin is not used and can be left unconnected.
PHY Bias Resistor	**ISET**	AI	This pin should be connected to ground through a 6.04KΩ 1% resistor.

TABLE 3-7: ALTERNATE FUNCTIONS

Name	Symbol	Buffer Type	Description
Power Management Event	**PME_N**	VO10/ VOD10	Programmable **PME_N** output. When asserted, this pin signals that a WOL event has occurred. **PME_N** can be mapped to various GPIO pins. The buffer type (push-pull or open-drain) depends on the setting of the corresponding GPIO Buffer Type (GPIO_BUF) bit in the General Purpose IO Buffer Type Register (GPIO_BUF). The polarity is set by the PME Polarity bit in the Output Control Register.
Start of Frame	**SOF_RX** **SOF_TX**	VO10/ VOD10	RX and TX Start of Frame indications. When pulsed, these pins signal the start of frame. **SOF_RX** and **SOF_TX** can be mapped to various GPIO pins. The buffer type (push-pull or open-drain) depends on the setting of the corresponding GPIO Buffer Type (GPIO_BUF) bit in the General Purpose IO Buffer Type Register (GPIO_BUF). The polarity is always active high.

TABLE 3-7: ALTERNATE FUNCTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
1588 LTC Events	**1588_EVENT_A** **1588_EVENT_B**	VO10/ VOD10	1588 Local Time Counter Event output. When asserted, these pins signal that a 1588 Local Time Counter event has occurred. **1588_EVENT_A** and **1588_EVENT_B** can be mapped to various GPIO pins. The buffer type (push-pull or open-drain) depends on the setting of the corresponding GPIO Buffer Type (GPIO_BUF) bit in the General Purpose IO Buffer Type Register (GPIO_BUF). The polarity is set by the Clock Event Polarity Channel A (CLOCK_EVENT_POL_A) and Clock Event Polarity Channel B (CLOCK_EVENT_POL_B) bits of the PTP General Configuration Register (PTP_GENERAL_CONFIG).

TABLE 3-8: STRAP INPUTS

Name	Symbol	Buffer Type	Description
MagJack	**MAGJACK**	VIS	The **MAGJACK** strap-in pin is sampled and latched at power-up/reset and is used to set various registers for MagJack operation as follows: 0 = normal register settings 1 = MagJack register settings See Section 3.3, "Configuration Straps" for more information.
PHY Address	**PHYAD4** **PHYAD3** **PHYAD2** **PHYAD1** **PHYAD0**	VIS	The PHY address, **PHYAD**[4:0], is sampled and latched at power-up/reset and is configurable to any value from 0 to 1Fh. Each PHY address bit is configured as follows: Pulled-up = 1 Pulled-down = 0 See Section 3.3, "Configuration Straps" for more information.
LED Polarity	**LEDPOL3** **LEDPOL2** **LEDPOL1**	VIS	Since the LED pins are shared with configuration straps, the default polarity of the LED pins is determined during strap loading. If the strap value on a pin is a 0, the LED is set as active high (**LEDPOL**=1), since it is assumed that a LED to ground is used as the pull-down. If the strap value on a pin is 1, the LED is set as active low (**LEDPOL**=0), since it is assumed that a LED to VDDIO is used as the pull-up. See Section 3.3, "Configuration Straps" for more information.
All PHY Address Enable	**ALLPHYAD**	VIS	The **ALLPHYAD** strap-in pin is sampled and latched at power-up/reset and are defined as follows: 0 = PHY will respond to PHY address 0 as well as it's assigned PHY address 1 = PHY will respond to only it's assigned PHY address **Note:** This strap input is inverted compared to the All PHYAD Enable register bit. See Section 3.3, "Configuration Straps" for more information.

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TABLE 3-8: STRAP INPUTS (CONTINUED)

Name	Symbol	Buffer Type	Description
Device Mode	**MODE4** **MODE3** **MODE2** **MODE1** **MODE0**	VIS	The **MODE**[4:0] strap-in pins are sampled and latched at power-up/reset and are defined in Section 3.3.1, "Device Mode Select (MODE[4:0])". See Section 3.3, "Configuration Straps" for more information.
RGMII Enable	**RGMII_EN**	VIS	**RGMII_EN** is sampled and latched at power-up/reset and is defined as follows: 0 = MII/GMII Mode 1 = RGMII Mode See Section 3.3, "Configuration Straps" for more information.
125MHz Output Clock Enable	**CLK125_EN**	VIS	**CLK125_EN** is sampled and latched at power-up/reset and is defined as follows: 0 = Disable 125 MHz clock output 1 = Enable 125 MHz clock output CLK125_NDO provides the 125 MHz reference clock output option for use by the MAC. See Section 3.3, "Configuration Straps" for more information.
LED Mode	**LED_MODE**	VIS (PD)	**LED_MODE** is sampled and latched at power-up/reset and is defined as follows: 0 = Tri-color-LED mode 1 = Individual-LED mode See Section 3.3, "Configuration Straps" for more information.

TABLE 3-9: I/O POWER, CORE POWER AND GROUND

Name	Symbol	Buffer Type	Description
+2.5/3.3V Analog Power Supply	**VDDAH**	P	+2.5/3.3V analog power supply V_{DD}
+1.1V Analog Power Supply	**VDDAL**	P	+1.1V analog power supply V_{DD}
+1.1V Analog PLL Power Supply	**VDDAL_PLL**	P	+1.1V analog PLL power supply V_{DD}
+3.3/2.5/1.8V Variable I/O Power Supply Input	**VDDIO**	P	+3.3/2.5/1.8V variable I/O digital power supply V_{DD_IO}
+1.1V Digital Core Power Supply Input	**VDD**	P	+1.1V digital core power supply input
Paddle Ground	**P_VSS**	GND	Common ground. This exposed paddle must be connected to the ground plane with a via array.

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3.3 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are latched upon the release of pin reset (**RESET_N**). Configuration straps do not include internal resistors and require the use of external resistors.

Note:	The system designer must guarantee that configuration strap pins meet the timing requirements specified in Section 6.6.3, "Reset Pin Configuration Strap Timing". If configuration strap pins are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

Note:	When externally pulling configuration straps high, the strap should be tied to VDDIO.

APPLICATION NOTE: All straps should be pulled-up or pulled-down externally on the PCB to enable the desired operational state.

APPLICATION NOTE: Extreme care must be taken on strap input pins that may be used for General Purpose inputs. The General Purpose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.

3.3.1 DEVICE MODE SELECT (MODE[4:0])

The **MODE**[4:0] configuration straps select the device mode as follows:

Note:	1000BT Half Duplex is not advertised in any of the below device modes.

TABLE 3-10: DEVICE MODE SELECTIONS

Test Modes	
MODE [4:0]	**Mode**
00010	RESERVED
00011	RESERVED
00100	NAND tree mode
00101	RESERVED
00110	RESERVED
00111	Device power down mode
Functional Modes	
Power Down	
01000	Software Power Down PLL Enabled
01001	Software Power Down PLL Disabled
Auto-Negotiation Disabled, Auto MDIX Disabled, EEE Disabled	
01010	1000FD Leader PHY Note 3-1
01011	100FD
01100	100HD
01101	1000FD Follower PHY Note 3-1

***Legend:**

1000FD = 1000BASE-T Full Duplex
100FD = 100BASE-TX Full Duplex
100HD = 100BASE-TX Half Duplex
10FD = 10BASE-T Full Duplex
10HD = 10BASE-T Half Duplex

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TABLE 3-10: DEVICE MODE SELECTIONS (CONTINUED)

Auto-Negotiation Enabled, Auto MDIX Enabled, EEE Disabled, Asym & Sym Pause Advertised												
		Auto-Negotiation Advertisement									10BT cat3/5	AMDIX
		1000BT			100BTX			10BT		Asym / Sym Pause		
		FD	Single / Multi	EEE	FD	HD	EEE	FD	HD			
10000	1000FD Single Port 100FD/HD 10FD/HD	X	S		X	X		X	X	X	cat3	X
10001	1000FD Multi Port 100FD/HD 10FD/HD	X	M		X	X		X	X	X	cat3	X
10010	1000FD Single Port	X	S							X	na	X
10011	1000FD Multi Port	X	M							X	na	X
10100	100FD/HD				X	X				X	na	X
10101	100FD				X					X	na	X
10110	100HD					X				X	na	X
10111	100FD/HD 10FD/HD				X	X		X	X	X	cat3	X
Auto-Negotiation Enabled, Auto MDIX Enabled, EEE Enabled, Asym & Sym Pause Advertised												
		Auto-Negotiation Advertisement									10BT cat3/5	AMDIX
		1000BT			100BTX			10BT		Asym / Sym Pause		
		FD	Single / Multi	EEE	FD	HD	EEE	FD	HD			
11000	1000FD Single Port 100FD/HD 10FD/HD	X	S	X	X	X	X	X	X	X	cat5	X
11001	1000FD Multi Port 100FD/HD 10FD/HD	X	M	X	X	X	X	X	X	X	cat5	X
11010	1000FD Single Port	X	S	X						X	na	X
11011	1000FD Multi Port	X	M	X						X	na	X
11100	100FD/HD				X	X	X			X	na	X
11101	100FD				X		X			X	na	X
11111	100FD/HD 10FD/HD				X	X	X	X	X	X	cat5	X
RESERVED												
00000	RESERVED											
00001	RESERVED											
01110	RESERVED											
01111	RESERVED											
11110	RESERVED											

***Legend:**

1000FD = 1000BASE-T Full Duplex
100FD = 100BASE-TX Full Duplex
100HD = 100BASE-TX Half Duplex
10FD = 10BASE-T Full Duplex
10HD = 10BASE-T Half Duplex

Note 3-1 Normally, Auto-Negotiation is required for operation at 1000Mbps. These forced settings allow manual configuration without Auto-Negotiation, however both the local and link partner devices must support this operation.

3.3.2 MAGJACK (MAGJACK)

The **MAGJACK** configuration straps sets LAN8841 for compatibility with MagJack RJ-45s with common center-taps.

3.3.3 RGMII MODE SELECT (RGMII_EN)

The **RGMII_EN** configuration strap selects between the GMII/MII (pulled-down) and RGMII (pulled-up) modes of operation.

3.3.4 PHY ADDRESS (PHYAD[4:0])

The **PHYAD**[4:0] configuration straps set the value of the PHY's management address.

3.3.5 ALL PHYs ADDRESS (ALLPHYAD)

The **ALLPHYAD** configuration strap sets the default of the All-PHYAD Enable bit in the Common Control Register which enables (pulled-down) or disables (pulled-up) the PHY's ability to respond to PHY address 0 as well as its assigned PHY address.

Note:	This strap input is inverted compared to the register bit.

3.3.6 125MHZ OUTPUT CLOCK ENABLE (CLK125_EN)

The **CLK125_EN** configuration strap enables the 125 MHz clock output onto the **CLK125_NDO** pin (pulled-up).

The output clock defaults to a locally generated 125MHz clock. The recovered 125MHz RX clock can be selected for use in Synchronous Ethernet (SyncE) applications.

3.3.7 LED MODE SELECT (LED_MODE)

The **LED_MODE** configuration strap selects between Individual-LED (pulled-up) or Tri-color-LED (pulled-down) modes.

3.3.8 LED POLARITY (LEDPOL[3:1])

The **LEDPOL**[3:1] configuration straps set the default polarity of the LED pins.

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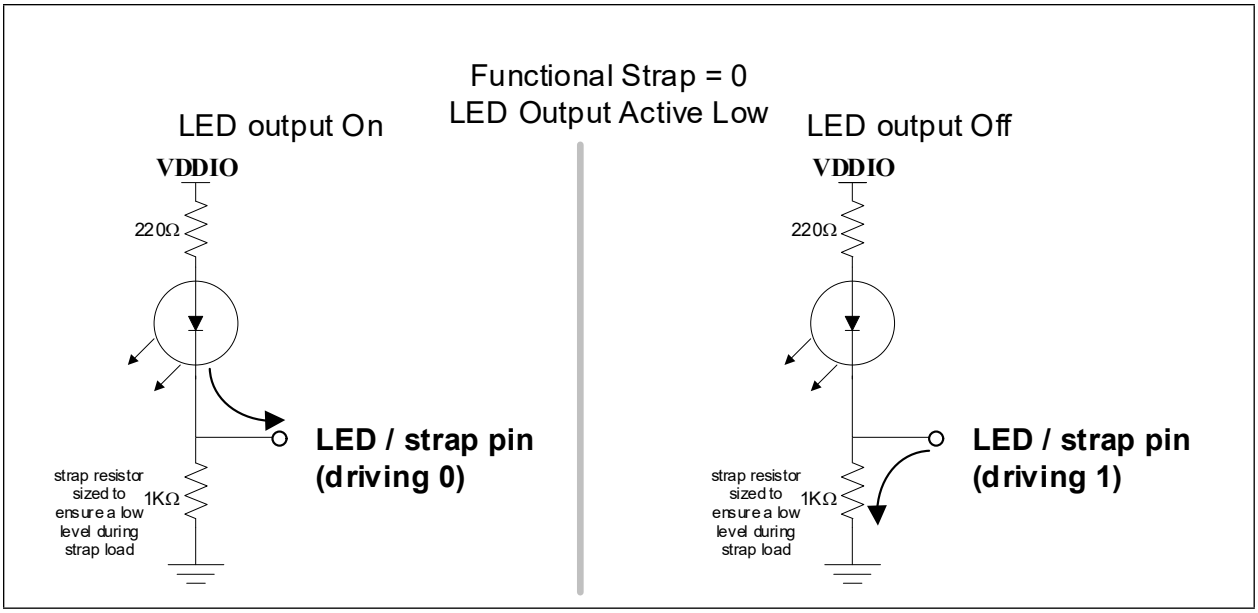
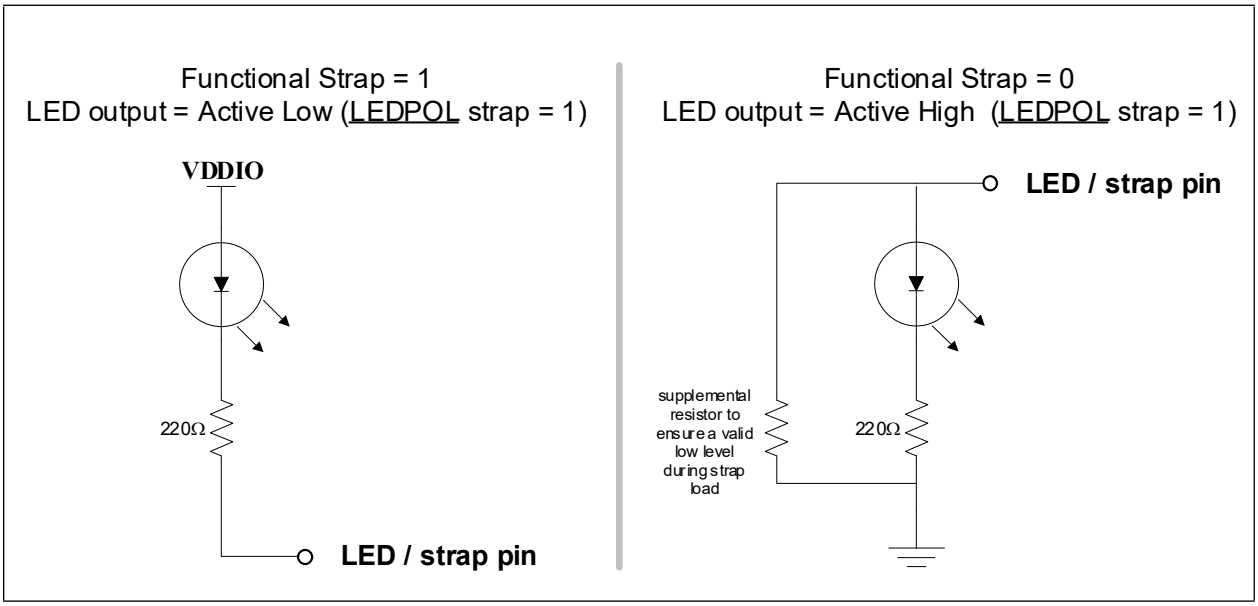
When a LED pin is used as a function mode strap (for example a PHY address bit), it is difficult to strap in a low value when a (active low) LED is connected via a resistor to **VDDIO**. A secondary pull-down resistor is needed to provide a low level during strap load time. When the LED is lit (pin driven low), the pull-down resistor is inconsequential. However, when the LED is not lit (pin driven high), the device drives wasted current, on the order of 3ma, through this resistor. This is especially important during power saving modes with multiple LEDs. This situation is shown in Figure 3-2.

FIGURE 3-2: LOW STRAP ON LED PIN



To avoid this, the default LED pin polarity, shown in the Strap Status Register, is automatically selected based on the inverse of the strap value. A LED, via a resistor, is then used as a pull-up, or as a pull-down.This is shown in Figure 3-3.

FIGURE 3-3: STRAP ON LED WITH POLARITY



3.4 Pin Alternate Functions

Various pins may be configured to carry alternate functions if the primary function is not required by the application:

- **LEDs 1-5** may be individually configured as **GPIO0-4** by setting the corresponding GPIO Enable (**GPIO_EN**) bits in the General Purpose IO Enable Register (**GPIO_EN**).
- During MII/GMII half-duplex operation, **COL** and **CRS** are not required and may be configured as **GPIO9-8** by setting the corresponding GPIO Enable (**GPIO_EN**) bits in the General Purpose IO Enable Register (**GPIO_EN**).
- During RGMII operation, **COL** and **CRS** are not used and may be configured as **GPIO9-8** by setting the corresponding GPIO Enable (**GPIO_EN**) bits in the General Purpose IO Enable Register (**GPIO_EN**).
- During MII/GMII operation if the host MAC does not generate transmit errors, TX_ER may be configured as **GPIO7** by setting the corresponding GPIO Enable (**GPIO_EN**) bit in the General Purpose IO Enable Register (**GPIO_EN**). The internal transmit error signal is forced inactive.
- During RGMII operation, **TX_ER** is not used and may be configured as **GPIO7** by setting the corresponding GPIO Enable (**GPIO_EN**) bit in the General Purpose IO Enable Register (**GPIO_EN**).
- INT_N may be configured as **GPIO5** by setting the corresponding GPIO Enable (**GPIO_EN**) bit in the General Purpose IO Enable Register (**GPIO_EN**).
- **CLK125_NDO** may be configured as GPIO6 by setting the corresponding GPIO Enable (**GPIO_EN**) bit in the General Purpose IO Enable Register (**GPIO_EN**).
- **CLK125_NDO** may be used as the 1588 reference clock input. **CLK125_NDO** does not have to be set as GPIO6 for this function.

3.4.1 GPIO PIN ALTERNATE FUNCTIONS

After a pin has been enabled as a GPIO, alternate output functions can be mapped onto the GPIO:

- 1588 inputs and output events may be mapped to any enabled GPIOs.
- **RX_SOF** and **TX_SOF** may be mapped to any enabled GPIO by setting the corresponding bits in the General Purpose IO Data Select 1 Register (GPIO_DATA_SEL1) or the General Purpose IO Data Select 2 Register (GPIO_DATA_SEL2).
- PME_N may be mapped to any enabled GPIO by setting the corresponding bits in the General Purpose IO Data Select 1 Register (GPIO_DATA_SEL1) or the General Purpose IO Data Select 2 Register (GPIO_DATA_SEL2).

APPLICATION NOTE: Extreme care must be taken on strap input pins that may be used for General Purpose inputs. The General Purpose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.

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4.0 DEVICE CONNECTIONS

4.1 Voltage Regulator

In order to facilitate ease of integration, this device includes an LDO controller for use with an external MOSFET to generate the core voltage supply.

4.1.1 MOSFET SELECTION

The selected MOSFET should exceed the following minimum requirements:

- P-channel
- 500 mA (continuous current)
- 3.3V or 2.5V (source – input voltage)
- 1.1V (drain – output voltage)
- VGS in the range of:
  - (–1.2V to –1.5V) @ 500 mA or 3.3V source voltage
  - (–1.0V to –1.1V) @ 500 mA for 2.5V source voltage

The V_{GS} for the MOSFET needs to be operating in the constant current saturated region, and not towards the $V_{GS(th)}$, the threshold voltage for the cut-off region of the MOSFET.

Refer to Table 6-15 for the LDO controller output driving range to the gate input of the MOSFET.

A 47µF electrolytic capacitor between 3.3V/2.5V source and ground is required. A 47µF electrolytic capacitor between core voltage and ground is required for proper LDO operation.

4.1.2 LDO DISABLE

The LDO controller can be disabled by setting the LDO Enable bit in Analog Control Register 11. An external source of 1.1V is necessary for operation in this case.

4.2 Power Connectivity

This section details the power connectivity of the device in the following modes of operation:

- Power Connectivity with Internal LDO Controller
- Power Connectivity with External 1.1V Power Supply

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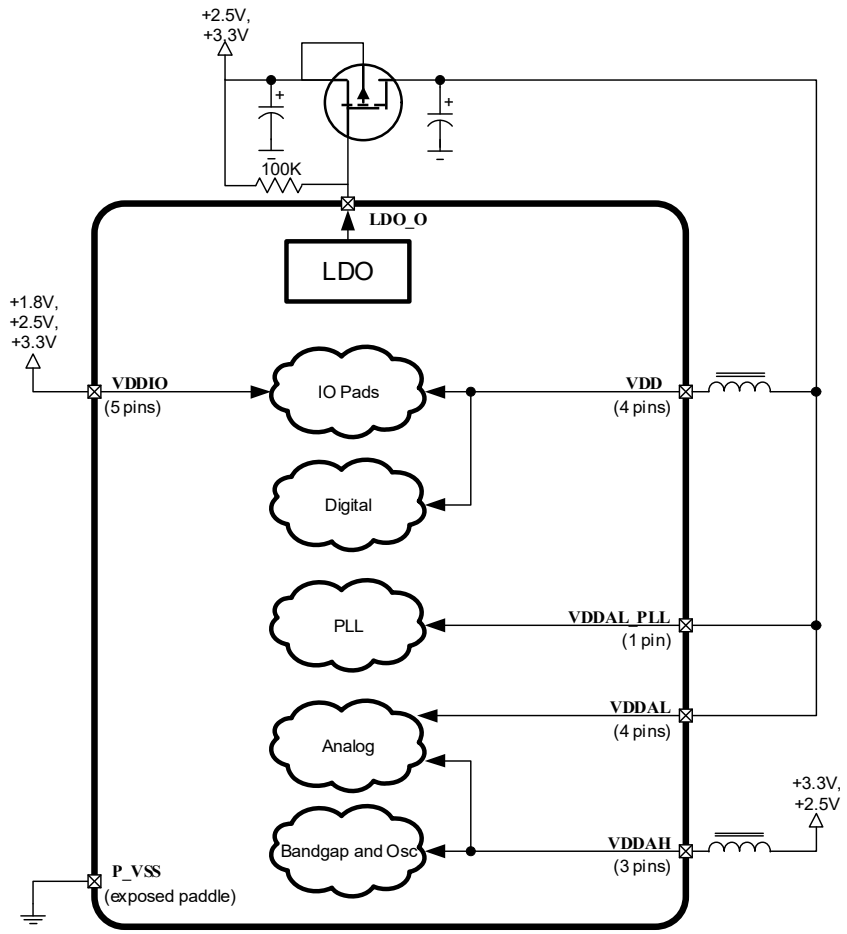
4.2.1 POWER CONNECTIVITY WITH INTERNAL LDO CONTROLLER

FIGURE 4-1: POWER CONNECTIVITY WITH INTERNAL LDO CONTROLLER



Notes: Bypass and bulk caps as needed for PCB.
Electrolytic capacitor required on MOSFET input and output.
100K resistor for in-rush current mitigation.

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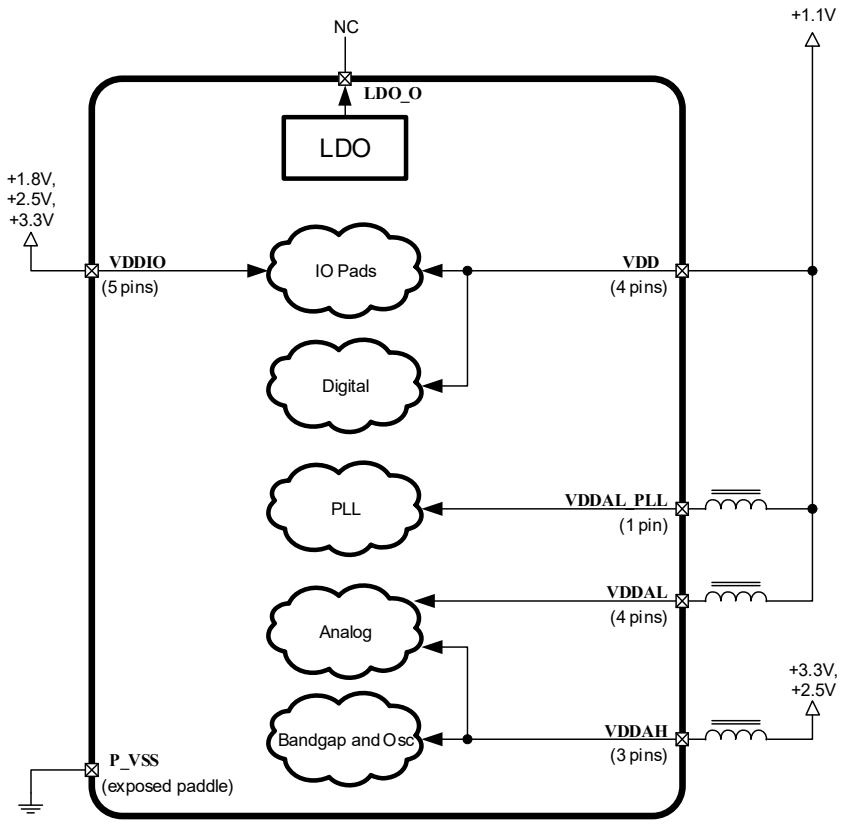
4.2.2 POWER CONNECTIVITY WITH EXTERNAL 1.1V POWER SUPPLY

FIGURE 4-2: POWER CONNECTIVITY WITH EXTERNAL 1.1V POWER SUPPLY



Notes: Bypass and bulk caps as needed for PCB.
Ferrites on **VDDAL** and **VDDAL_PLL** may be combined.

5.0 FUNCTIONAL DESCRIPTION

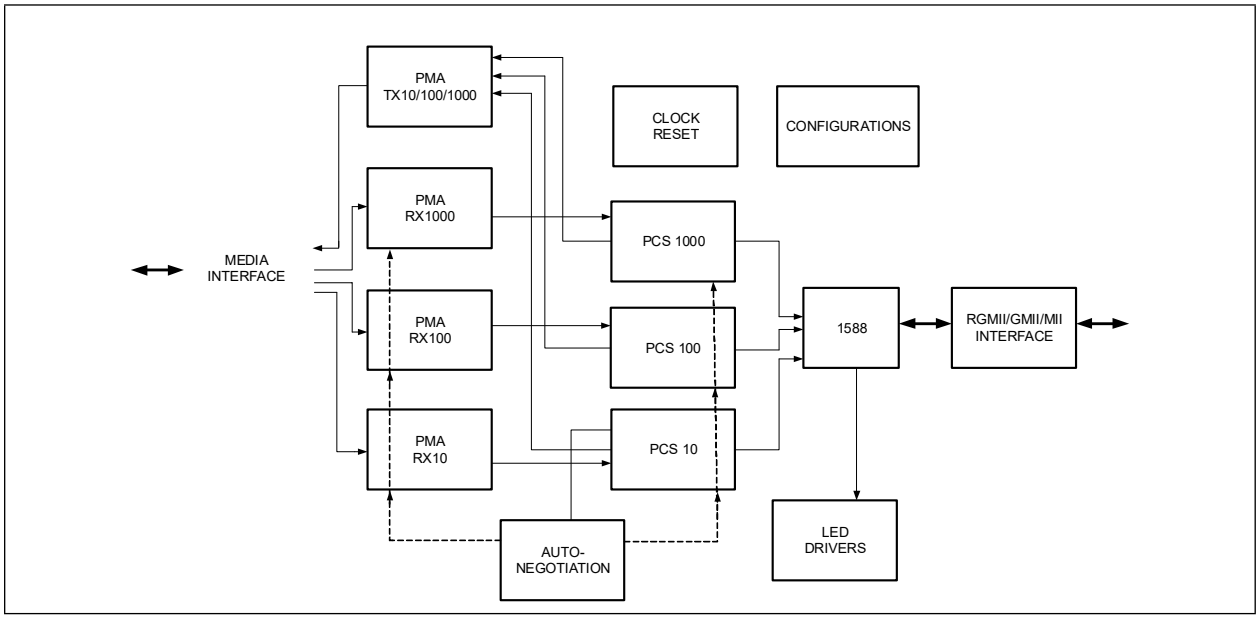
The LAN8841 is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver solution for transmission and reception of data over a standard CAT-5, as well as CAT-5e and CAT-6, unshielded twisted pair (UTP) cables.

The device reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the core voltage.

On the copper media interface, the device can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000BASE-T operation.

The LAN8841 provides the RGMII/GMII/MII interface for connection to GMACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000Mbps.Figure 5-1 shows a high-level block diagram of the LAN8841.

FIGURE 5-1: LAN8841 BLOCK DIAGRAM



5.1 10BASE-T/100BASE-TX Transceiver

5.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 6.04 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, and overshoot. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

5.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

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Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII/GMII or RGMII format and provided as the input data to the MAC.

5.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled using an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

5.1.4 10BASE-T TRANSMIT

The 10BASE-T output drivers are incorporated into the 100BASE-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/10BASE-Te signals have harmonic contents that are at least 31 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

5.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level-detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the device decodes a data frame. The receiver clock is maintained active during idle periods between receiving data frames.

The device removes all 7 bytes of the preamble and presents the received frame starting with the SFD (start of frame delimiter) to the MAC.

Auto-polarity correction is provided for the receiving differential pair to automatically swap and fix the incorrect +/– polarity wiring in the cabling.

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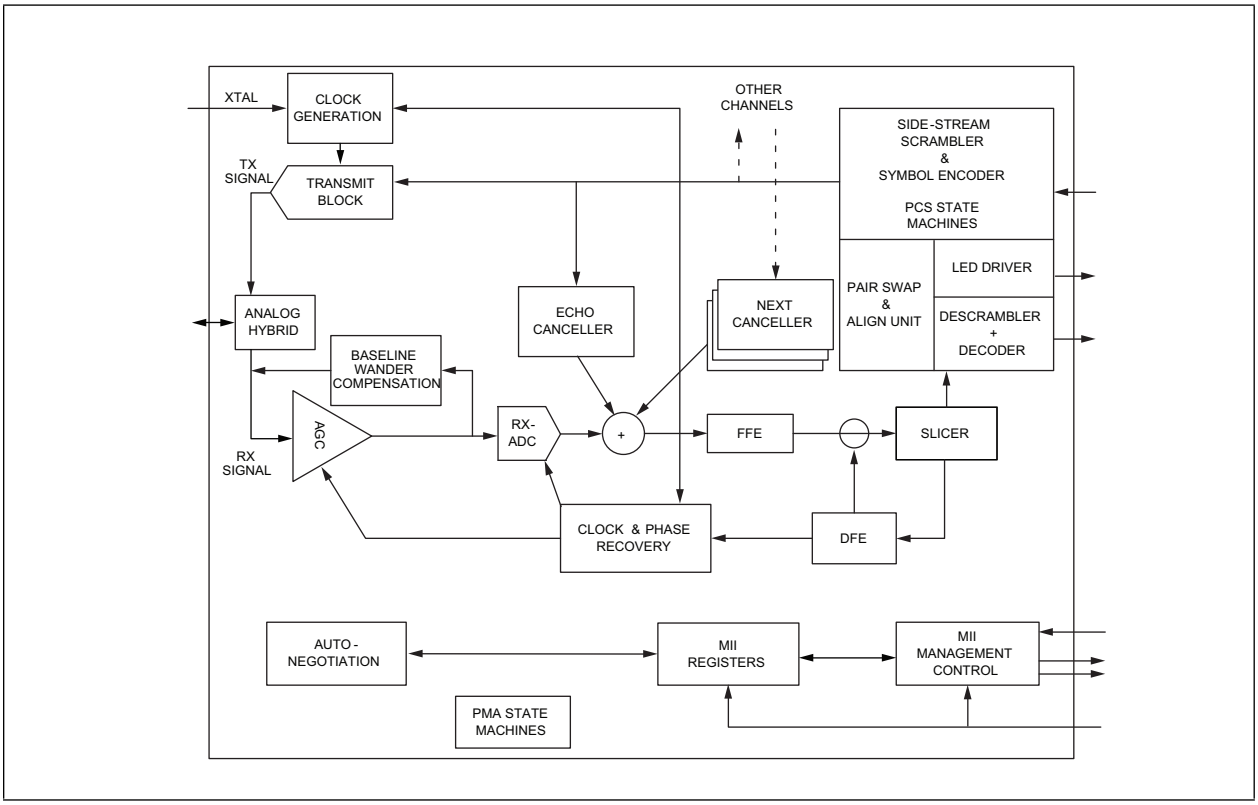
5.2 1000BASE-T Transceiver

The 1000BASE-T transceiver is based-on a mixed-signal/digital-signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancelers, cross-talk cancelers, precision clock recovery scheme, and power-efficient line drivers.

Figure 5-2 shows a high-level block diagram of a single channel of the 1000BASE-T transceiver for one of the four differential pairs.

FIGURE 5-2: 1000BASE-T BLOCK DIAGRAM - SINGLE CHANNEL



5.2.1 ANALOG ECHO-CANCELLATION CIRCUIT

In 1000BASE-T mode, the analog echo-cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

5.2.2 AUTOMATIC GAIN CONTROL (AGC)

In 1000BASE-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

5.2.3 ANALOG-TO-DIGITAL CONVERTER (ADC)

In 1000BASE-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

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5.2.4 TIMING RECOVERY CIRCUIT

In 1000BASE-T mode, the mixed-signal clock recovery circuit together with the digital phase-locked loop is used to recover and track the incoming timing information from the received data. The digital phase-locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000BASE-T follower PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000BASE-T leader PHY. Otherwise, the leader and follower will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

5.2.5 ADAPTIVE EQUALIZER

In 1000BASE-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The device uses a digital echo canceler to further reduce echo components on the receive signal.

In 1000BASE-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The device uses three NEXT cancelers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10BASE-T/100BASE-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

5.2.6 TRELLIS ENCODER AND DECODER

In 1000BASE-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one device is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order, and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

5.3 Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the device and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the device accordingly.

Table 5-1 shows the device's 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

TABLE 5-1: MDI/MDI-X PIN MAPPING

Pin (RJ-45 Pair)	MDI			MDI-X		
	1000BASE-T	100BASE-T	10BASE-T	1000BASE-T	100BASE-T	10BASE-T
TXRXP/M_A (1, 2)	A+/–	TX+/–	TX+/–	B+/–	RX+/–	RX+/–
TXRXP/M_B (3, 6)	B+/–	RX+/–	RX+/–	A+/–	TX+/–	TX+/–
TXRXP/M_C (4, 5)	C+/–	Not Used	Not Used	C+/–	Not Used	Not Used
TXRXP/M_D (7, 8)	D+/–	Not Used	Not Used	D+/–	Not Used	Not Used

Auto-MDIX detection is enabled in the device by default.

Auto-MDIX can be disable by setting the swapoff bit in the Digital Debug Control 1 Register. The MDI / MDI-X mode may then be manually selected by the mdi_set bit in the Digital Debug Control 1 Register.

The Auto-MDIX status bits are located in the Digital AX/AN Status Register.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

5.4 Alignment and Polarity Detection/Correction

In 1000BASE-T mode, the device supports 50 ns ±10 ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized.

Additionally, the device detects and corrects polarity errors on all MDI pairs, a useful capability that exceeds the requirements of the standard. Polarity detection and correction applies to 10BASE-T and 1000BASE-T and is not required for 100BASE-TX.

5.5 Wave Shaping, Slew-Rate Control, and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000BASE-T, a special partial-response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-T, pre-emphasis is used to extend the signal quality through the cable.

5.6 MagJack RJ-45 with Common Center-taps Operation

Normally the center-taps of the device side of the magnetics need to be capacitively coupled to signal ground. To operate with MagJack RJ-45s with common center-taps, the **MAGJACK** strap may be used. This strap sets the default of the MagJack_mode bit in the Operation Mode Strap Override Low Register, which in turn sets the values of the Power Management Mode Registers.

5.7 PLL Clock Synthesizer

The device generates 125 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from the external 25 MHz crystal or reference clock.

5.8 Auto-Negotiation

The device conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (unshielded twisted pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the operating mode.

The following list shows the speed and duplex operation mode from highest-to-lowest:

- Priority 1: 1000BASE-T, full-duplex
- Priority 2: 1000BASE-T, half-duplex

Note:	The device does not support 1000BASE-T, half-duplex and should not be enabled to advertise such.

- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 100BASE-TX, half-duplex
- Priority 5: 10BASE-T, full-duplex
- Priority 6: 10BASE-T, half-duplex

If auto-negotiation is not supported or the device's link partner is forced to bypass auto-negotiation for 10BASE-T and 100BASE-TX modes, the device sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the device to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

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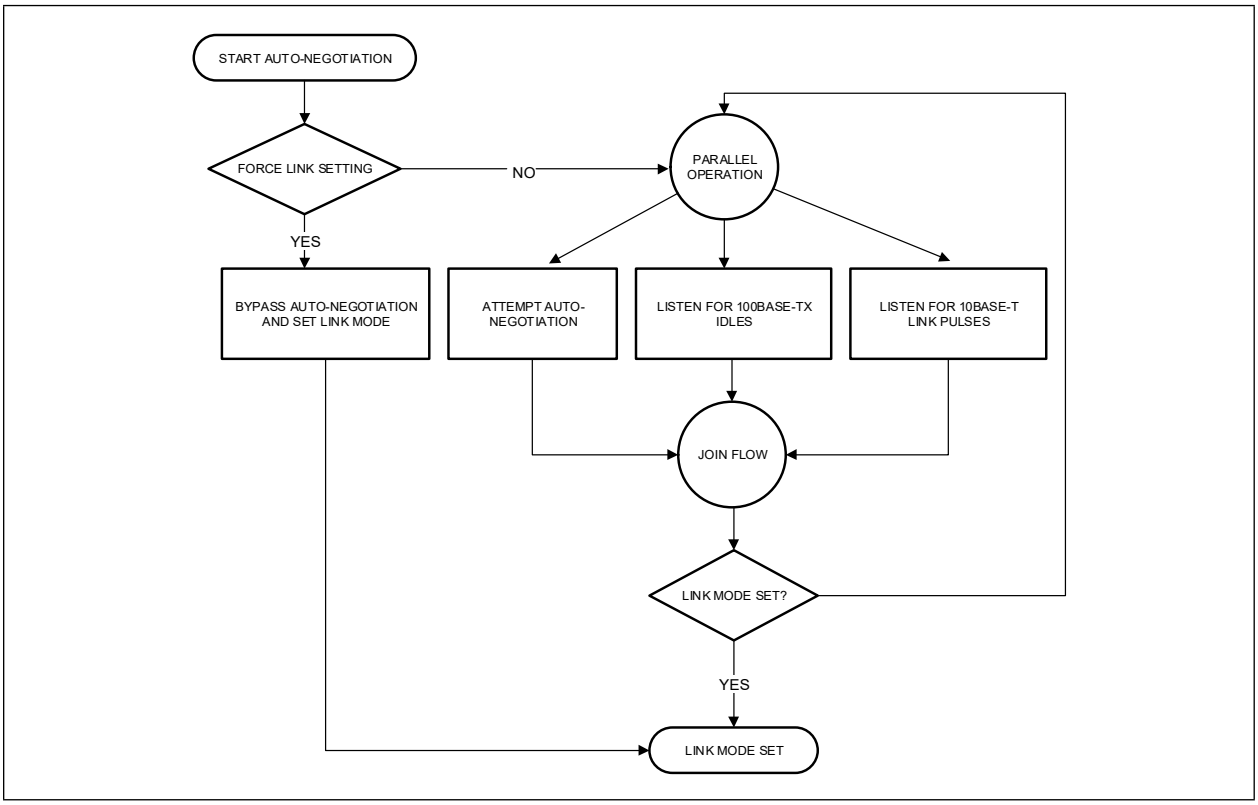
The auto-negotiation link-up process is shown in Figure 5-3.

FIGURE 5-3: AUTO-NEGOTIATION FLOW CHART



For 1000BASE-T mode, auto-negotiation is required and always used to establish a link. During 1000BASE-T auto-negotiation, the leader and follower configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled through the Basic Control Register, Bit [12]. If auto-negotiation is disabled, the speed is set by the Basic Control Register, Bits [6, 13] and the duplex is set by the Basic Control Register, Bit [8].

If the speed is changed on the fly, the link goes down and either auto-negotiation and parallel detection initiate until a common speed between the device and its link partner is re-established for a link.

If the link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through the Basic Control Register, Bit [9], or a link-down to link-up transition occurs (that is, disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in the Basic Status Register, Bit [2], and the link partner capabilities are updated in Registers 5h, 6h, 8h, and Ah.

The auto-negotiation finite state machines use interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions is summarized in Table 5-2.

TABLE 5-2: AUTO-NEGOTIATION TIMERS

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst Interval	16 ms
Transmit Pulse Interval	68 µs
FLP Detect Minimum Time	17.2 µs
FLP Detect Maximum Time	185 µs
Receive Minimum Burst Interval	6.8 ms
Receive Maximum Burst Interval	112 ms
Data Detect Minimum Interval	35.4 µs
Data Detect Maximum Interval	95 µs
NLP Test Minimum Interval	4.5 ms
NLP Test Maximum Interval	30 ms
Link Loss Time	52 ms
Break Link Time	1480 ms
Parallel Detection Wait Time	830 ms
Link Enable Wait Time	1000 ms

5.8.1 AUTO-NEGOTIATION NEXT PAGE USAGE

The device supports “Next Page” capability which is used to negotiate Gigabit Ethernet and Energy Efficient Ethernet functionality as well as to support software controlled pages.

As described in IEEE 802.3 Annex 40C “Add-on interface for additional Next Pages”, the device will autonomously send and receive the Gigabit Ethernet and Energy Efficient Ethernet next pages and then optionally send and receive software controlled next pages.

Gigabit Ethernet next pages consist of one message and two unformatted pages. The message page contains an 8 as the message code. The first unformatted page contains the information from the Auto-Negotiation Master Slave Control Register. The second unformatted page contains the Leader-Follower Seed value used to resolve the Leader-Follower selection. The result of the Gigabit Ethernet next pages exchange is stored in Auto-Negotiation Master Slave Status Register.

Gigabit Ethernet next pages are always transmitted, regardless of the advertised settings in the Auto-Negotiation Master Slave Control Register.

Energy Efficient Ethernet (EEE) next pages consist of one message and one unformatted page. The message page contains a 10 as the message code (this value can be overridden in the EEE Message Code Register). The unformatted page contains the information from the EEE Advertisement Register. The result of the Gigabit Ethernet next pages exchange is stored in EEE Link Partner Ability Register.

EEE next pages are transmitted only if the advertised setting in the EEE Advertisement Register is not zero.

APPLICATION NOTE: The Gigabit Ethernet and EEE next pages may be viewed in Auto-Negotiation Next Page RX Register as they are exchanged.

Following the EEE next page exchange, software controlled next pages are exchanged when the Next Page bit in the Auto-Negotiation Advertisement Register is set. Software controlled next page status is monitored via the Auto-Negotiation Expansion Register and Auto-Negotiation Next Page RX Register.

5.8.2 PARALLEL DETECT DUPLEX

Normally, and according to IEEE 802.3, when parallel detection is used to establish the link, the resulting operation is set to half duplex. An option exists to force this result to full duplex. This is enabled by setting the LP Force 100 FD Override and/or LP Force 10 FD Override bits in the Parallel Detect Full Duplex Override Register.

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5.9 10/100 Mbps Speeds Only

Some applications require link-up to be limited to 10/100 Mbps speeds only.

After power-up/reset, the device can be restricted to auto-negotiate and link-up to 10/100 Mbps speeds only by programming the following register settings:

1. Configure the Speed Select[1] bit in the Basic Control Register to '0' to disable the 1000 Mbps speed.
2. Configure the 1000BASE-T Full Duplex and 1000BASE-T Half Duplex bits in the Auto-Negotiation Master Slave Control Register to '00' to remove Auto-Negotiation advertisements for 1000 Mbps full/half duplex.
3. Write a '1' to the Restart Auto-Negotiation (PHY_RST_AN) bit in the Basic Control Register, a self-clearing bit, to force a restart of Auto-Negotiation.

Auto-Negotiation and 10BASE-T/100BASE-TX speeds use only differential pairs A and B. Differential pairs C and D can be left as no connects.

5.10 Energy Efficient Ethernet

The device implements Energy Efficient Ethernet (EEE) as described in IEEE Standard 802.3az. The specification is defined around an EEE-compliant MAC on the host side and an EEE-compliant link partner on the line side that support the special signaling associated with EEE. EEE saves power by keeping the AC signal on the copper Ethernet cable at approximately 0V peak-to-peak as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as low-power idle (LPI) mode or state.

As set by the **MODE[4:0]** configuration straps, the device has the EEE function enabled or disabled as the power-up default setting. The EEE function can be enabled or disabled by setting or clearing the following EEE advertisement bits in the EEE Advertisement Register (MMD Address 7h, Register 3Ch), followed by restarting auto-negotiation (writing a '1' to the Basic Control Register, Bit [9]):

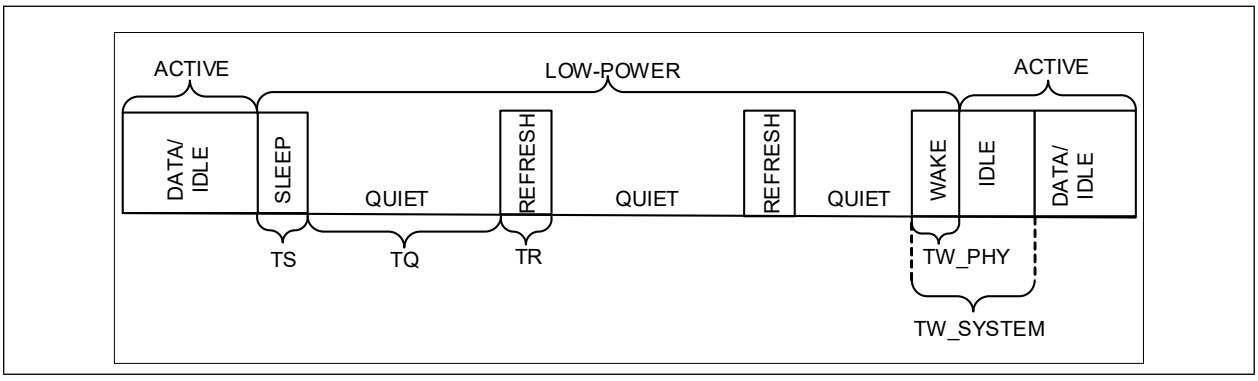
- 1000BASE-T EEE (Bit [2]) = 0/1 // Disable/Enable 1000 Mbps EEE mode
- 100BASE-TX EEE (Bit [1]) = 0/1 // Disable/Enable 100 Mbps EEE mode

During LPI mode, the copper link responds automatically when it receives traffic and resumes normal PHY operation immediately, without blockage of traffic or loss of packet. This involves exiting LPI mode and returning to normal 100/1000 Mbps operating mode. Wake-up times are <16 µs for 1000BASE-T and <30 µs for 100BASE-TX. The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

During LPI mode, refresh transmissions are used to maintain the link; power savings occur in quiet periods. Approximately every 20 to 22 milliseconds, a refresh transmission of 200 to 220 microseconds is sent to the link partner. The refresh transmissions and quiet periods are shown in Figure 5-4:

FIGURE 5-4: LPI MODE (REFRESH TRANSMISSIONS AND QUIET PERIODS)



Per the IEEE Standard, the device will wait for one second following link up before sending LPI. This is enabled by default via the lpi_1sec_delay bit in the EEE Wait Time Threshold and CRS Block Timer Register.

5.10.1 TRANSMIT DIRECTION CONTROL (MAC-TO-PHY)

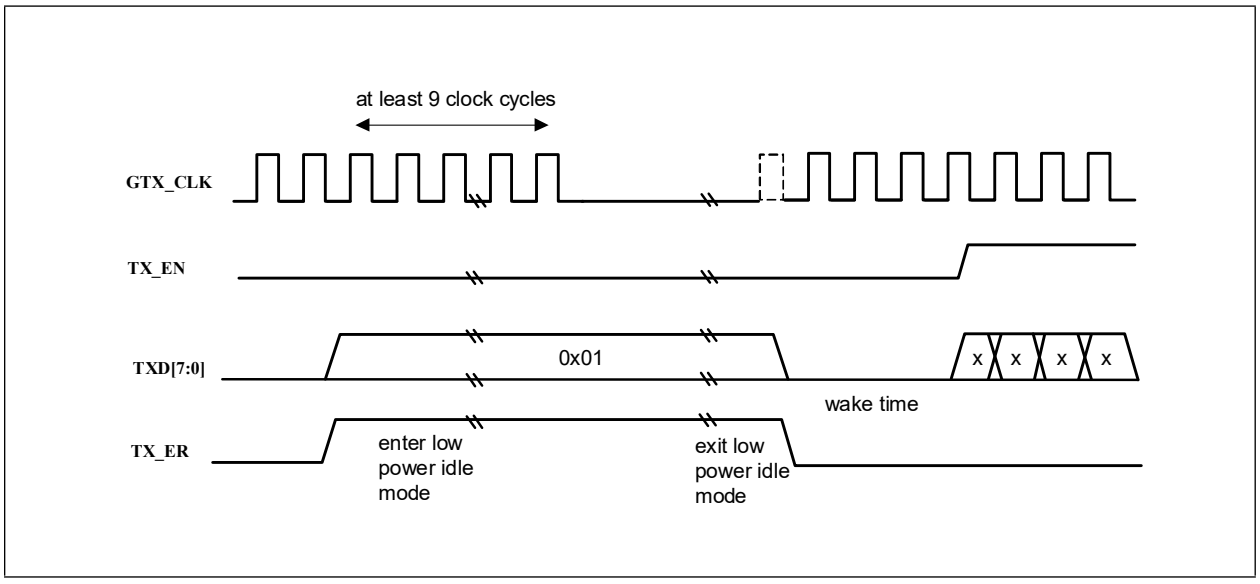
5.10.1.1 GMII/MII

On the GMII/MII interface, the device enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts **TX_EN**, asserts **TX_ER**, and sets **TXD[7:0]** to 0000_0001 for GMII (1000 Mbps) or **TXD[3:0]** to 0001 for MII (100 Mbps). The device remains in the transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the **TX_EN**, **TX_ER**, or TX data signals from their LPI state values, the device exits the LPI transmit state.

For GMII (1000 Mbps), as indicated by the Clock stop capable bit in the PCS Status 1 Register, the **GTX_CLK** signal may be stopped by the MAC to save additional power, after the GMII signals for the LPI state have been asserted for nine or more **GTX_CLK** clock cycles.

Figure 5-5: shows the LPI transition for GMII transmit.

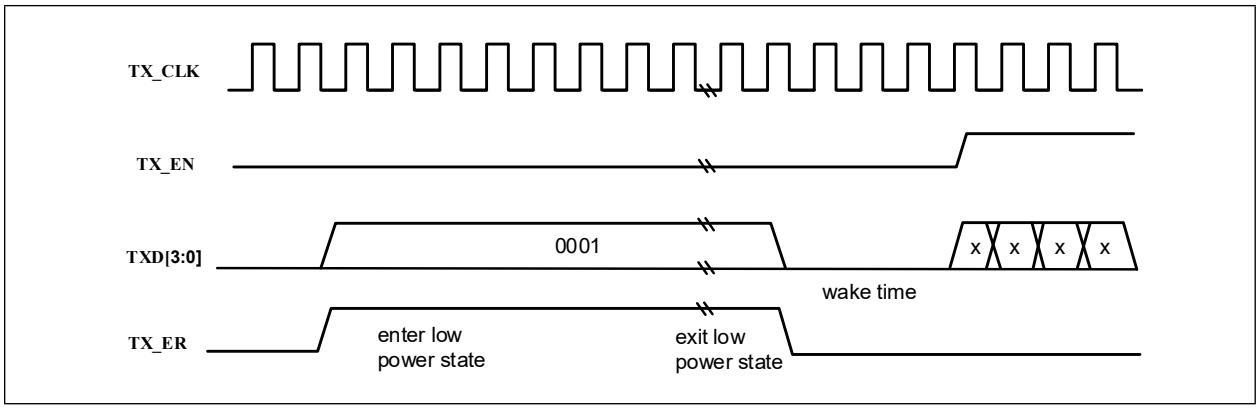
FIGURE 5-5: LPI TRANSITION - GMII (1000 MBPS) TRANSMIT



For MII (100 Mbps), the **TX_CLK** is not stopped, because it is sourced from the PHY and is used by the MAC for MII transmit.

Figure 5-6: shows the LPI transition for MII transmit.

FIGURE 5-6: LPI TRANSITION - MII (100 MBPS) TRANSMIT



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5.10.1.2 RGMII

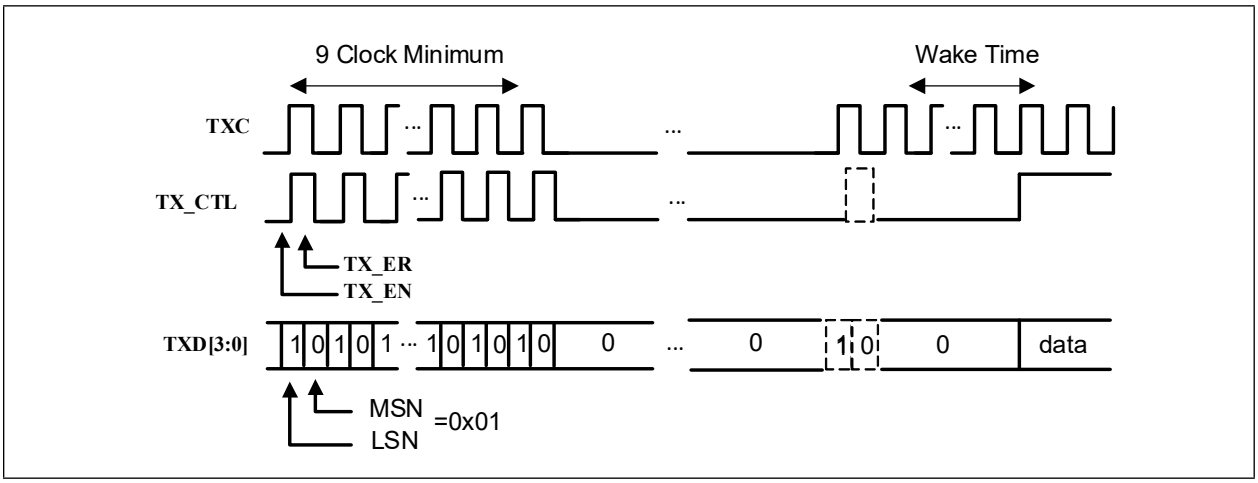
On the RGMII interface at 1000 Mbps, transmission from MAC-to-PHY uses both rising and falling edges of the **TXC** signal. The device uses the **TX_CTL** pin to clock in the logical equivalent of the **TX_EN** signal on the rising edge and the logical equivalent of the **TX_ER** signal on the falling edge. It also uses the **TXD[3:0]** pins to clock in the TX data low nibble bits [3:0] on the rising edge and the TX data high nibble Bits [7:4] on the falling edge.

The device enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts the logical equivalent of the **TX_EN** signal (the **TX_CTL** pin low on the rising edge), asserts the logical equivalent of the **TX_ER** signal (the **TX_CTL** pin high on the falling edge), and sets TX data Bits [7:0] to 0000_0001 (**TXD[3:0]** pins 0001 on the rising edge and 0000 on the falling edge). The device remains in the 1000Mbps transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the logical equivalent **TX_EN**, **TX_ER**, or TX data signals from their LPI state values, the device exits the LPI transmit state.

To save more power, as indicated by the Clock stop capable bit in the PCS Status 1 Register, the MAC can stop the **TXC** signal after the RGMII signals for the LPI state have been asserted for 9 or more **TXC** clock cycles. During the clock stoppage the **TX_CTL** and **TXD[3:0]** pins are most likely held low by the MAC.

Figure 5-7: shows the LPI transition for GMII transmit.

FIGURE 5-7: LPI TRANSITION - RGMII (1000 MBPS) TRANSMIT



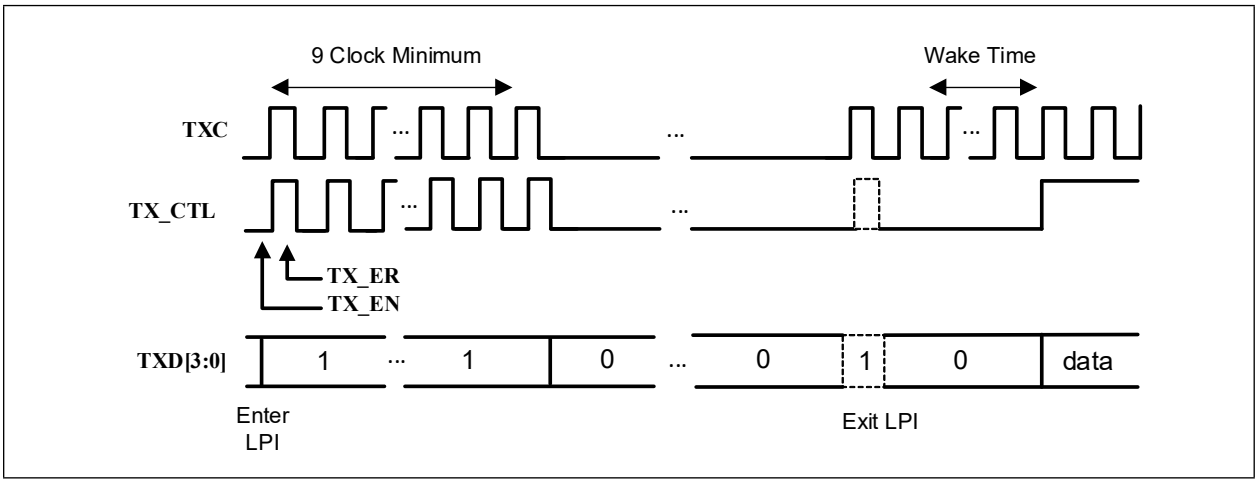
RGMII transmission at 100 Mbps from MAC-to-PHY uses both rising and falling edges of the **TXC** signal. The device uses the **TX_CTL** pin to clock in the logical equivalent of the **TX_EN** signal on the rising edge and the logical equivalent of the **TX_ER** signal on the falling edge. It also uses the **TXD[3:0]** pins to clock in the TX data bits [3:0] on the rising edge.

The device enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts the logical equivalent of the **TX_EN** signal (the **TX_CTL** pin low on the rising edge), asserts the logical equivalent of the **TX_ER** signal (the **TX_CTL** pin high on the falling edge), and sets TX data Bits [3:0] to 0001. The device remains in the 100Mbps transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the logical equivalent **TX_EN**, **TX_ER**, or TX data signals from their LPI state values, the device exits the LPI transmit state.

To save more power, as indicated by the Clock stop capable bit in the PCS Status 1 Register, the MAC can stop the **TXC** signal after the RGMII signals for the LPI state have been asserted for 9 or more **TXC** clock cycles. During the clock stoppage the **TX_CTL** and **TXD[3:0]** pins are most likely held low by the MAC.

Figure 5-8: shows the LPI transition for RGMII transmit in 100 Mbps mode.

FIGURE 5-8: LPI TRANSITION - RGMII (100 MBPS) TRANSMIT



5.10.2 RECEIVE DIRECTION CONTROL (PHY-TO-MAC)

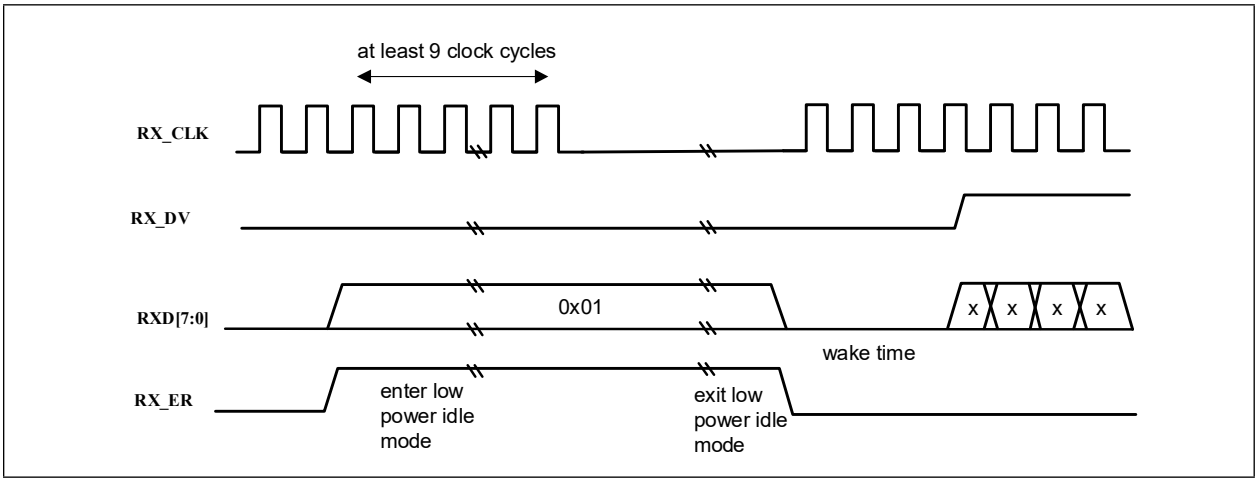
5.10.2.1 GMII/MII

On the GMII/MII interface, the device enters LPI mode for the receive direction when it receives the /P/ code bit pattern (Sleep/Refresh) from its EEE-compliant link partner. It then de-asserts **RX_DV**, asserts **RX_ER**, and drives **RXD[7:0]** to 0000_0001 for GMII (1000 Mbps) or **RXD[3:0]** to 0001 for MII (100 Mbps). The device remains in the receive LPI state while it continues to receive the refresh from its link partner, so it will continue to maintain and drive the LPI output states for the GMII/MII receive signals to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the device receives a non /P/ code bit pattern (non-refresh), it exits the receive LPI state and sets the **RX_DV**, **RX_ER**, and RX data signals to set a normal frame or normal idle.

To save more power, the device may stop the **RX_CLK** clock output to the MAC after nine or more **RX_CLK** clock cycles have occurred in the receive LPI state. The Clock-stop enable bit in the PCS Control 1 Register controls if the device stops the **RX_CLK** clock output. The device may restart **RX_CLK** at any time while it is asserting LPI, but shall restart **RX_CLK** so that at least one positive transition occurs before it deasserts LPI.

Figure 5-9:: shows the LPI transition for GMII receive.

FIGURE 5-9: LPI TRANSITION - GMII (1000 MBPS) RECEIVE



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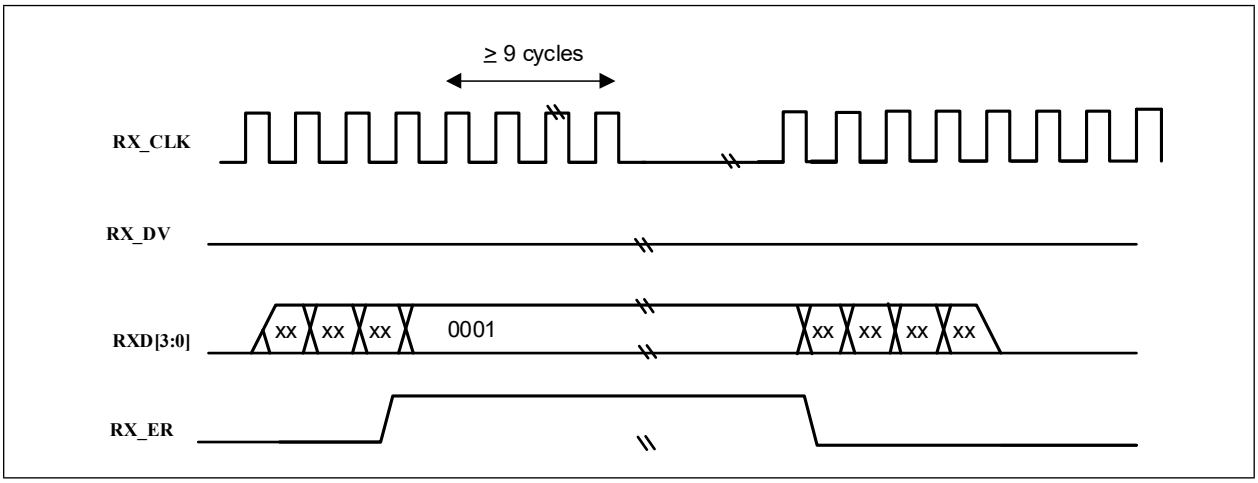
Similarly, for MII (100 Mbps), the device stops the **RX_CLK** clock output to the MAC after nine or more **RX_CLK** clock cycles have occurred in the receive LPI state, to save more power. The Clock-stop enable bit in the PCS Control 1 Register controls if the device stops the **RX_CLK** clock output. The device may restart **RX_CLK** at any time while it is asserting LPI, but shall restart **RX_CLK** so that at least one positive transition occurs before it deasserts LPI.

Figure 5-10: shows the LPI transition for MII receive.

FIGURE 5-10: LPI TRANSITION - MII (100 MBPS) RECEIVE



5.10.2.2 RGMII

On the RGMII interface at 1000 Mbps, reception from PHY-to-MAC uses both rising and falling edges of the **RXC** signal. The device uses the **RX_CTL** pin to clock out the logical equivalent of the **RX_DV** signal on the rising edge and the logical equivalent of the **RX_ER** signal on the falling edge. It also uses the **RXD[3:0]** pins to clock out the RX data low nibble bits [3:0] on the rising edge and the RX data high nibble bits [7:4] on the falling edge.

The device enters LPI mode for the receive direction when it receives the /P/ code bit pattern (sleep/refresh) from its EEE-compliant link partner. It then drives the logical equivalent of the **RX_DV** signal low (on the rising clock edge) and the logical equivalent of the **RX_ER** signal high (on the falling edge), to the MAC. Also, the **RXD[3:0]** pins are driven to 0001 on the rising clock edge and 0000 on the falling clock edge to set the RX data bits [7:0] to 0000_0001. The device remains in the 1000 Mbps receive LPI state while it continues to receive the refresh from its link partner, so it will continue to maintain and drive the LPI output states for the RGMII receive output pins to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the device receives a non /P/ code bit pattern (non-refresh), it exits the receive LPI state and sets the **RX_DV** and **RXD[3:0]** output pins accordingly for a normal frame or normal idle.

To save more power, the device stops the **RXC** clock output to the MAC after 9 or more **RXC** clock cycles have occurred in the receive LPI state. The Clock-stop enable bit in the PCS Control 1 Register controls if the device stops the **RXC** clock output. During the clock stoppage the **RX_CTL** and **RXD[3:0]** pins are held low by the device. The device may restart **RXC** at any time while it is asserting LPI, but shall restart **RXC** so that at least one positive transition occurs before it deasserts LPI.

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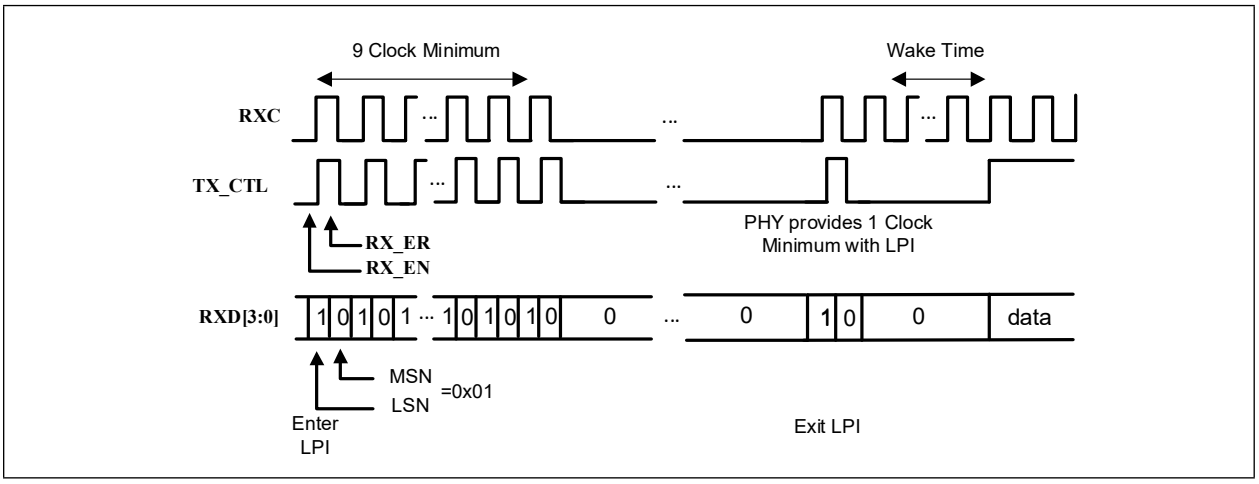
Figure 5-11: shows the LPI transition for RGMII receive in 1000 Mbps mode.

FIGURE 5-11: LPI TRANSITION - RGMII (1000 MBPS) RECEIVE



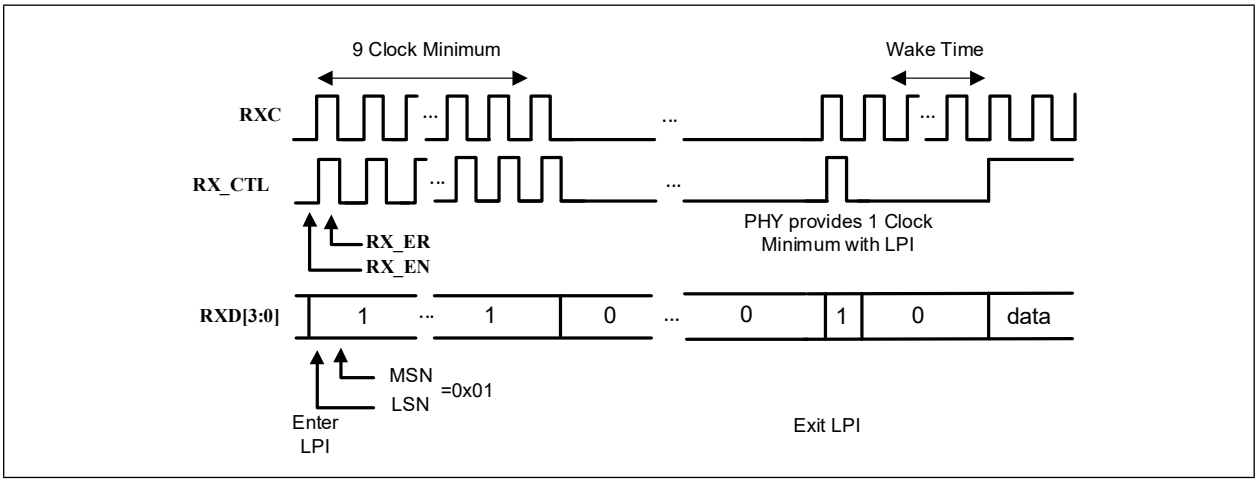
RGMII reception at 100 Mbps from PHY-to-MAC uses both rising and falling edges of the **RXC** signal. The device uses the **RX_CTL** pin to clock out the logical equivalent of the **RX_DV** signal on the rising edge and the logical equivalent of the **RX_ER** signal on the falling edge. It also uses the **RXD[3:0]** pins to clock out the RX data bits [3:0] on the rising edge.

The device enters LPI mode for the receive direction when it receives the /P/ code bit pattern (sleep/refresh) from its EEE-compliant link partner. It then drives the **RX_DV** pin low on the rising clock edge and high on the falling clock edge to de-assert the **RX_DV** signal and assert the **RX_ER** signal, respectively, to the MAC. Also, the **RXD[3:0]** pins are driven to 0001. The device remains in the 100 Mbps receive LPI state while it continues to receive the refresh from its link partner, so it will continue to maintain and drive the LPI output states for the RGMII receive output pins to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the device receives a non /P/ code bit pattern (non-refresh), it exits the receive LPI state and sets the **RX_DV** and **RXD[3:0]** output pins accordingly for a normal frame or normal idle.

To save more power, the device stops the **RXC** clock output to the MAC after 9 or more **RXC** clock cycles have occurred in the receive LPI state. The Clock-stop enable bit in the PCS Control 1 Register controls if the device stops the **RXC** clock output. During the clock stoppage the **RX_CTL** and **RXD[3:0]** pins are held low by the device. The device may restart **RXC** at any time while it is asserting LPI, but shall restart **RXC** so that at least one positive transition occurs before it deasserts LPI.

Figure 5-12: shows the LPI transition for RGMII receive in 100 Mbps mode.

FIGURE 5-12: LPI TRANSITION - RGMII (100 MBPS) RECEIVE



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5.10.3 10BASE-Te MODE

For standard (non-EEE) 10BASE-T mode, normal link pulses (NLPs) with long periods of no AC signal transmission are used to maintain the link during the idle period when there is no traffic activity. To save more power, the device provides the option to enable 10BASE-Te mode, which saves additional power by reducing the transmitted signal amplitude from 2.5V to 1.75V. As set by the **MODE[4:0]** configuration straps, 10BASE-Te mode is enabled or disabled by default and can be enabled or disabled by clearing or setting the p_cat3 bit in the AFED Control Register in MMD space.

5.10.4 REGISTERS ASSOCIATED WITH EEE

The following MMD registers are provided for EEE configuration and management:

- MMD Address 3h, Register 0h — PCS Control 1 Register
- MMD Address 3h, Register 1h — PCS Status 1 Register
- MMD Address 7h, Register 3Ch — EEE Advertisement Register
- MMD Address 7h, Register 3Dh — EEE Link Partner Ability Register
- MMD Address 1Ch, Register 9h — AFED Control Register

5.11 802.3br Frame Preemption

IEEE Standard 802.3br-2016 specifies a method for interspersing express traffic by preempting the transmission of a normal packet, transmitting the express packet and then resuming the normal packet. The receiver likewise reassembles the fragmented normal packet.

The preemption and reassembly is performed by a new MAC Merge sublayer, which resides between the MAC layer and the Reconciliation Sublayer and makes use of a newly defined mPacket format. This mPacket format starts with the normal preamble but supplements the normal Start of Frame Delimiter (SFD = 0xD5) with newly defined Start mPacket Delimiters (SMDs) of various values. Also added for certain mPackets is a fragment count octet.

Since these SMDs are effectively part of the data stream and not part of the framing (i.e. they are D codes), the PHY functions will pass these to the GMII/MII/RGMII as normal data.

Section 5.18 defines SOF pulse generation support for the SMDs.

Note:	In 10BASE-T, PCS LOOPBACK SWAP/POLARITY CONTROL REGISTER Bit 2 needs to be set so the preamble is preserved.

5.12 Dynamic Channel Quality (DCQ) (TC1 and TC12)

The device provides dynamic channel quality features that include Mean Square Error (MSE), Signal Quality Indicator (SQI), and peak Mean Square Error (pMSE) values. These features are designed to be compliant with Sections 6.1.1, 6.1.2, and 6.1.3 of the *OPEN Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0* specification and *TC-12 - Advanced diagnostics features for 1000BASE-T1 automotive Ethernet PHYs Version 1.7*, respectively. These DCQ features are detailed in the following sections:

- Mean Square Error (MSE)
- Signal Quality Indicator (SQI)
- Peak Mean Square Error (pMSE)

MLT-3 modulation is used for data transmission in 100BASE-TX and PAM5 modulation is used for data transmission in 1000BASE-T.

Logically, 100BASE-TX (MLT-3) and 1000BASE-T (PAM5) have signal values of {-1, 0, +1} and {-2, -1, 0, +1, +2}, respectively. These logic levels are mapped to slicer reference levels of {-128, 0, 128} for 100BASE-TX and {-128, -64, 0, 64, 128} for 1000BASE-T. The middle points (the compare thresholds) are {-64, 64} for 100BASE-TX and are {-96, -32, 32, 96} for 1000BASE-T.

Ideally, each receive data sample would be the maximum distance from the compare thresholds, with error values of 0. But because of noise and imperfection in real applications, the sampled data may be off from its ideal. The closer to the compare threshold, the worse the signal quality.

The slicer error is a measurement of how far the processed data off from its ideal location. The largest instantaneous slicer error for 1000BASE-T is +/-32. The largest instantaneous slicer error for 100BASE-TX is +/-64. A higher absolute slicer error means a degraded signal receiving condition.

5.12.1 MEAN SQUARE ERROR (MSE)

This section defines the implementation of section 6.1.1 of the TC1 and TC12 specifications. The device can provide detailed information of the dynamic signal quality by means of a MSE value. This mode is enabled by setting the sqi_enable bit in the DCQ Configuration Register. This bit must be set for all DCQ measurements.

With this method, the slicer error is converted into a squared value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window. For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value.

Note: The sqi_squ_mode_en bit in the DCQ Configuration Register must be set to choose square mode.

The sqi_kp field in the DCQ Configuration Register sets the weighting of the add back as a divide by $2^{\wedge sqi\_kp}$, effectively setting the filter bandwidth. As the sqi_kp value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value. Also as the sqi_kp value is increased, there will be less variation in the mean slicer error value reported.

The scale611 field in the DCQ Configuration Register is used to set a divide by factor (divide by $2^{\wedge scale611)}$ such that the MSE value is linearly scaled to the range of 0 to 511. If the divide by factor is too small, the MSE value is capped at a maximum of 511.

The filtered error value is saved every 65,536 symbols (524,288 us).

In order to capture the MSE Value, the DCQ Read Capture bit in the DCQ Configuration Register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ Mean Square Error Register.

In addition to the current MSE Value, the worst case MSE value since the last read of DCQ Mean Square Error Register is stored in DCQ Mean Square Error Worst Case Register.

5.12.2 SIGNAL QUALITY INDICATOR (SQI)

The device provides two SQI methods:

- SQI Method A: TC1 Section 6.1.2 compliant
- SQI Method B: Proprietary method

5.12.2.1 SQI Method A

This section defines the implementation of section 6.1.2 of the TC1 and TC12 specifications. This mode builds upon the Mean Square Error (MSE) method by mapping the MSE value onto a simple quality index. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration Register.

As in the Mean Square Error (MSE) method, the sqi_squ_mode_en bit in the DCQ Configuration Register must be set to choose square mode and the scale611 field in the DCQ Configuration Register is used to set the divide by factor (divide by $2^{\wedge scale611)}$ such that the MSE value is linearly scaled to the range of 0 to 511.The MSE value is compared to the thresholds set in the DCQ SQI Table Registers to provide a SQI value between 0 (worst value) and 7 (best value) as follows:

TABLE 5-3: MSE TO SQI MAPPING

MSE Value		SQI Value
Greater Than	**Less Than or Equal To**	
	SQI_TBL7.SQI_VALUE	7
SQI_TBL7.SQI_VALUE	SQI_TBL6.SQI_VALUE	6
SQI_TBL6.SQI_VALUE	SQI_TBL5.SQI_VALUE	5
SQI_TBL5.SQI_VALUE	SQI_TBL4.SQI_VALUE	4
SQI_TBL4.SQI_VALUE	SQI_TBL3.SQI_VALUE	3
SQI_TBL3.SQI_VALUE	SQI_TBL2.SQI_VALUE	2
SQI_TBL2.SQI_VALUE	SQI_TBL1.SQI_VALUE	1
SQI_TBL1.SQI_VALUE		0

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In order to capture the SQI value, the DCQ Read Capture bit in the DCQ Configuration Register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ SQI Register.

In addition to the current SQI the worst case (lowest) SQI since the last read is available in the SQI Worst Case field.

The correlation between the SQI values stored in the DCQ SQI Register and an according signal to noise ratio (SNR) based on AWG noise (bandwidth of 80MHz) is shown in Table 5-4. The bit error rates to be expected in the case of white noise as interference signal is shown in the table as well for information purposes.

A link loss only occurs if the SQI value is 0.

TABLE 5-4: SQI VALUE CORRELATION

SQI Value	Recommended BER for AWG Noise Model
0	BER>10^-10
1	
2	
3	
4	
5	BER<10^-10
6	
7	

5.12.2.2 SQI Method B

With the SQI Method B, the slicer error is converted into an absolute value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration Register.

For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value. The sqi_squ_mode_en bit in the DCQ Configuration Register is used to square the (scaled) slicer error.

The sqi_kp field in the DCQ Configuration Register sets the weighting of the add back as a divide by $2^{\wedge sqi\_kp}$, effectively setting the filter bandwidth. As the sqi_kp value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value. Also as the sqi_kp value is increased, there will be less variation in the mean slicer error value reported.

The filtered error value is saved every 65,536 symbols (524,288 us).

In order to capture the current error value, the DCQ Read Capture bit in the DCQ Configuration Register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit immediately self-clears and the result is available in the Mean Slicer Error Register.

A software based lookup table (derived empirically in lab conditions) may be used to report a SQI number.

5.12.3 PEAK MEAN SQUARE ERROR (PMSE)

This section defines the implementation of section 6.1.3 of the TC1 and TC12 specifications. The peak MSE value is intended to identify transient disturbances which are typically in the microsecond range. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration Register.

With this method, the slicer error is converted into a squared value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a moving time window.

For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value.

Note:	The sqi_squ_mode_en bit in the DCQ Configuration Register must be set to choose square mode.

The sqi_kp3 field in the DCQ Configuration Register sets the weighting of the add back as a divide by $2^{\wedge(sqi\_kp3)}$, effectively setting the filter bandwidth. As the sqi_kp3 value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value.

Every 65,536 symbols (524,288 us), the highest filtered value over that previous 524,288 us period is saved.

The scale613 field in the DCQ Configuration Register is used to set a divide by factor (divide by $2^{\wedge scale613+3)}$ such that the peak MSE value is linearly scaled to the range of 0 to 63. If the divided by factor is too small, the peak MSE value is capped at a maximum of 63.

In order to capture the Peak MSE Value, the DCQ Read Capture bit in the DCQ Configuration Register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ Peak MSE Register.

In addition to the current Peak MSE Value the worst case Peak MSE value since the last read of DCQ Peak MSE Register is stored in the same register.

5.13 Loopback Modes

The device supports the following loopback operations to verify analog and/or digital data paths.

- Digital (near-end) loopback.
- Remote (Far-End) loopback
  - Remote (Far-End) loopback with switch mode
- External connector loopback

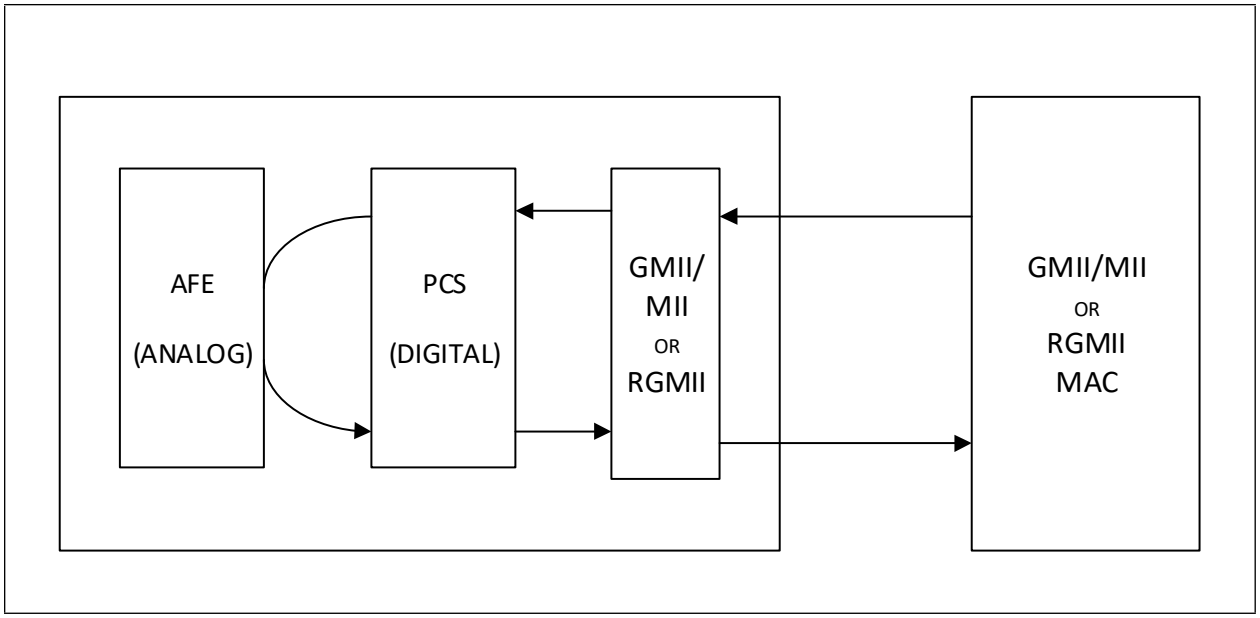
5.13.1 DIGITAL (NEAR-END) LOOPBACK

This loopback mode checks the GMII/MII or RGMII transmit and receive data paths between the device and the external MAC, and is supported for all three speeds (10/100/1000 Mbps) at full-duplex.

The loopback data path is shown in Figure 5-13:.

1. GMII/MII or RGMII MAC transmits frames to the device.
2. Frames are wrapped around inside the device.
3. The device transmits frames back to GMII/MII or RGMII MAC

FIGURE 5-13: DIGITAL (NEAR-END) LOOPBACK



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The following programming steps and register settings are used for local loopback mode.

For 1000 Mbps loopback,

1. Set Basic Control Register,
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode
2. Set Auto-Negotiation Master Slave Control Register,
   - Bit [12] = 1 // Enable leader-follower manual configuration
   - Bit [11] = 0 // Select follower configuration (required for loopback mode)

For 10/100 Mbps loopback,

1. Set Basic Control Register,
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 00 / 01 // Select 10 Mbps/100 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

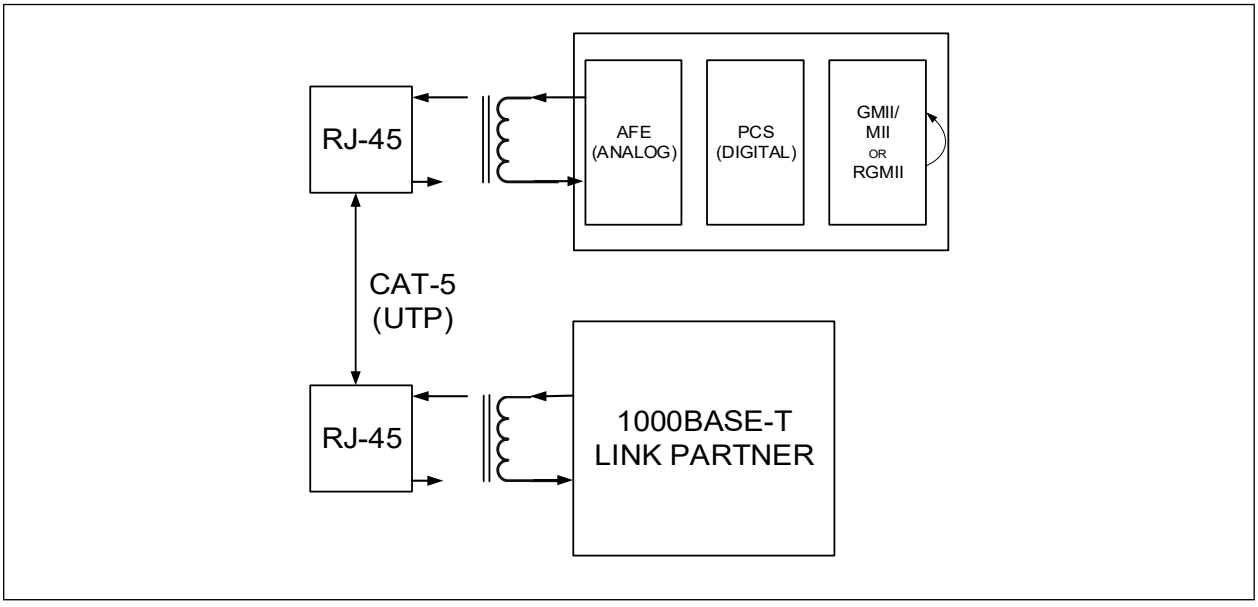
5.13.2 REMOTE (FAR-END) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the device and its link partner, and is supported for 1000BASE-T full-duplex mode only.

The loopback data path is shown in Figure 5-14:

1. The Gigabit PHY link partner transmits frames to the device.
2. Frames are wrapped around inside the device.
3. The device transmits frames back to the Gigabit PHY link partner.

FIGURE 5-14: REMOTE (FAR-END) LOOPBACK



The following programming steps and register settings are used for remote loopback mode.

1. Set Basic Control Register,
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

   Or just auto-negotiate and link up at 1000BASE-T full-duplex mode with the link partner.
2. Set PCS Loop-back Swap/Polarity Control Register,
3. Bit [8] = 1 // Enable remote loopback mode

5.13.2.1 Switch Mode Loopback

During Remote (Far-End) Loopback, an option may be enabled where the MAC DA and SA are swapped and the FCS is recalculated. This mode is useful for testing where a network switch is the link partner. Upon returning the modified frame to the switch, the switch may direct the frame to the original ingress port. This mode is enabled with the Switch Port Loopback bit in the Common Control Register.

5.13.3 EXTERNAL CONNECTOR LOOPBACK

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D, as shown in Figure 5-15. The connector loopback feature functions at all available interface speeds.

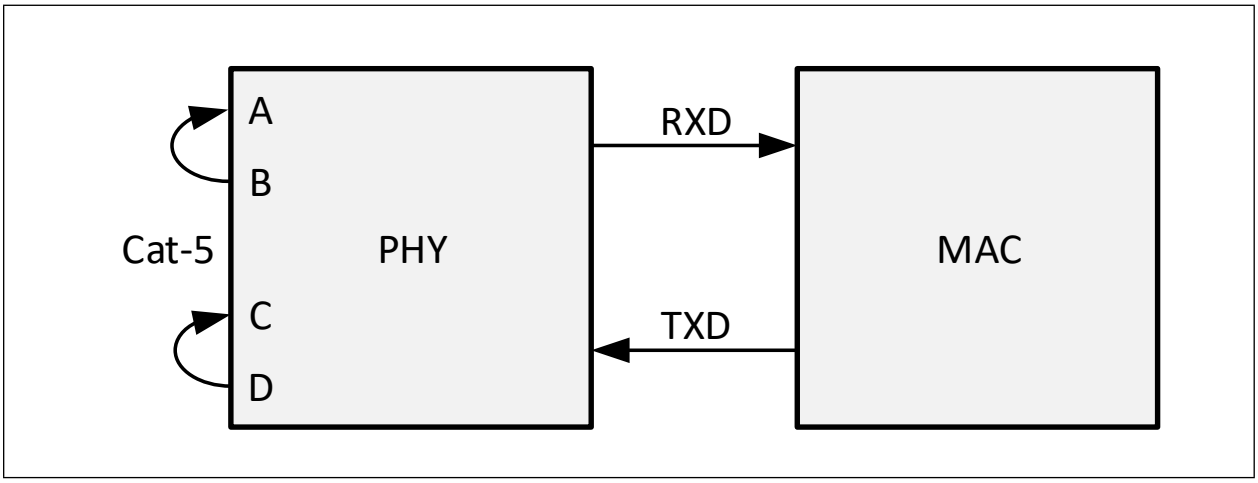
This loopback tests the PHY digital and MAC connectivity.

When using the connector loopback testing feature, the device Auto-Negotiation, speed, and duplex configuration is set using the Basic Control Register, Auto-Negotiation Advertisement Register, and Auto-Negotiation Master Slave Control Register.

For 1000BASE-T connector loopback, the following additional writes are required to be executed in the following order:

- Disable Auto-Negotiation and set the speed to 1000Mbps and the duplex to full by setting the Basic Control Register to a value of 0140h.
- Set the Leader-Follower configuration to leader by setting the Master/Slave Manual Configuration Enable and Master/Slave Manual Configuration Value bits in the Auto-Negotiation Master Slave Control Register.
- Enable the 1000BASE-T connector loopback by setting the Ext_lpbk bit in the Reserved Register.

FIGURE 5-15: EXTERNAL CONNECTOR LOOPBACK



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5.14 LinkMD® Cable Diagnostic

The LinkMD function uses Time Domain Reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches as well as the distance to the fault. Each of the four twisted pairs are tested separately.

LinkMD operates by sending a pulse of known amplitude and duration down the selected differential pair, then analyzing the polarity and shape of the reflected signal to determine the type of fault: open circuit for a positive/non-inverted amplitude reflection and short circuit for a negative/inverted amplitude reflection. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing the Cable Diagnostic Register.

To test each individual cable pair, set the cable pair in the Cable Diagnostics Test Pair (VCT_PAIR[1:0]) field of the Cable Diagnostic Register, along with setting the Cable Diagnostics Test Enable (VCT_EN) bit. The Cable Diagnostics Test Enable (VCT_EN) bit will self-clear when the test is concluded.

The test results (for the pair just tested) are available in the Cable Diagnostic Register. With the Bit[9:0] Definition (VCT_SEL[1:0]) field set to 0, the Cable Diagnostics Status (VCT_ST[1:0]) field will indicate a Normal (properly terminated), Open or Short condition, or a Failed Test.

If the test result was Open or Short, the Cable Diagnostics Data or Threshold (VCT_DATA[7:0]) field indicates the distance to the fault in meters as approximately:

- distance to fault = (VCT_DATA - 22) * 4 / cable propagation velocity

With an accuracy of +/- 2% to 3% for short and medium cables and +/- 5% to 6% for long cables. Inaccuracy is due to cable pitch differences between cable manufacturers, where cable pitch is the number of wire twists per unit cable length.

LinkMD supports diagnostic cable testing in the following three scenarios:

1. No Link Partner
2. Fully Passive Link Partner
3. Partially Active Link Partner

5.14.1 LinkMD WITH NO LINK PARTNER

In this scenario the remote end of the cable is unplugged.

Prior to running the cable diagnostics, perform a software reset (Basic Control Register, Bit [15] = 1). After reset, the following must be configured:

- Auto Negotiation disabled [Basic Control Register, Bit [12] = 0]
- Full Duplex set [Basic Control Register, Bit [8] = 1]
- Link Speed set to 1000Mbps [Basic Control Register, Bit [13] = 0, Bit [6] = 1]
- Auto MDI/MDI-X disabled [Digital Debug Control 1 Register, Bit [6] = 1]
- Leader-Follower configuration set to Follower [Auto-Negotiation Master Slave Control Register = 0x1200]

Wait 10ms prior to testing the pairs.

In this scenario, for each of the four twisted pairs LinkMD should only return Open or Short along with a distance.

- Open with “distance” providing the correct cable length indicates a good cable
- Short or Open with any other distance indicates a bad cable

After running the cable diagnostics, perform another software reset [Basic Control Register, Bit [15] = 1].

5.14.2 LinkMD WITH FULLY PASSIVE LINK PARTNER

In this scenario the remote end of the cable is connected to a Link Partner. The Link Partner must be powered down or configured to be in the following passive state:

- Auto Negotiation disabled
- Auto MDI/MDI-X disabled

Prior to running the cable diagnostics, perform a software reset (Basic Control Register, Bit [15] = 1). After reset, the following must be configured:

- Auto Negotiation disabled [Basic Control Register, Bit [12] = 0]

- Full Duplex set [Basic Control Register, Bit [8] = 1]
- Link Speed set to 1000Mbps [Basic Control Register, Bit [13] = 0, Bit [6] = 1]
- Auto MDI/MDI-X disabled [Digital Debug Control 1 Register, Bit [6] = 1]
- Leader-Follower configuration set to Follower [Auto-Negotiation Master Slave Control Register = 0x1200]

Wait 10ms prior to testing the pairs.

In this scenario, for each of the four twisted pairs LinkMD will return Open or Short along with a distance or Normal.

- Normal indicates a good cable which is properly terminated at the Link Partner. Due to no TDR reflections, no cable distance is available with this result (VCT_DATA[7:0] is invalid).
- Open or Short indicates a bad cable or improper Link Partner termination. VCT_DATA[7:0] indicates the distance to the cable fault.

After running the cable diagnostics, perform another software reset [Basic Control Register, Bit [15] = 1].

5.14.3 LinkMD WITH PARTIALLY ACTIVE LINK PARTNER

In this scenario the remote end of the cable is connected to a Link Partner. The Link Partner is powered up and in the following state:

- Auto Negotiation may be enabled, disabled, or unknown
- Auto MDI/MDI-X is disabled, but we are able to selectively configure MDI or MDI-X, as required for the LinkMD tests

Prior to running the cable diagnostics, perform a software reset (Basic Control Register, Bit [15] = 1). After reset, the following must be configured:

- Auto Negotiation disabled [Basic Control Register, Bit [12] = 0]
- Full Duplex set [Basic Control Register, Bit [8] = 1]
- Link Speed set to 1000Mbps [Basic Control Register, Bit [13] = 0, Bit [6] = 1]
- Auto MDI/MDI-X disabled [Digital Debug Control 1 Register, Bit [6] = 1]
- Leader-Follower configuration set to Follower [Auto-Negotiation Master Slave Control Register = 0x1200]

Wait 10ms prior to testing the pairs.

The LinkMD test is first run with the Link Partner in MDI mode on twisted pairs B, C, and D.

The LinkMD test is then run with the Link Partner in MDI-X mode on twisted pair A.

- Normal indicates a good cable which is properly terminated at the Link Partner. Due to no TDR reflections, no cable distance is available with this result (VCT_DATA[7:0] is invalid).
- Open or Short indicates a bad cable or improper Link Partner termination. VCT_DATA[7:0] indicates the distance to the cable fault.

After running the cable diagnostics, perform another software reset [Basic Control Register, Bit [15] = 1].

APPLICATION NOTE: If the Cable Diagnostics Status (VCT_ST[1:0]) field indicates Failed it is generally due to multiple pulses being received after sending out a single pulse. In this Partially Active test the Link Partner is allowed to be in the Auto-Negotiation state but if the Link Partner is mistakenly in forced 1000BASE-T or 100BASE-TX mode the test will fail.

APPLICATION NOTE: Any signal received from a link partner will interfere with the TDR test. Energy detection should first be checked on each wire pair by using the procedure in Section 7.29.2, "Energy-Detect Power-Down Mode".

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5.15 GMII Interface

The Gigabit Media Independent Interface (GMII) is compliant to the IEEE 802.3 Specification. It provides a common interface between GMII PHYs and MACs, and has the following key characteristics:

- Pin count is 24 pins (11 pins for data transmission, 11 pins for data reception, and 2 pins for carrier and collision indication).
- 1000 Mbps is supported at both half- and full-duplex.

Note:	The device does not support 1000BASE-T, half-duplex and should not be enabled to advertise such.

- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 8 bits wide, a byte.

In GMII operation, the GMII pins function as follows:

- The MAC sources the transmit reference clock, **GTX_CLK**, at 125 MHz for 1000 Mbps.
- The PHY recovers and sources the receive reference clock, **RX_CLK**, at 125 MHz for 1000 Mbps.
- **TX_EN**, **TXD[7:0]**, and TX_ER are sampled by the device on the rising edge of **GTX_CLK**.
- **RX_DV**, **RXD[7:0]**, and RX_ER are sampled by the MAC on the rising edge of **RX_CLK**.
- **CRS** and **COL** are driven by the LAN8841 and do not have to transition synchronously with respect to either **GTX_CLK** or **RX_CLK**.

The device combines GMII mode with MII mode to form GMII/MII mode to support data transfer at 10/100/1000 Mbps. After power-up or reset, the device is configured to GMII/MII mode if the **RGMII_EN** configuration strap is set to '0'. See the Configuration Straps section.

The device has the option to output a 125 MHz reference clock on **CLK125_NDO**. This clock provides a lower-cost reference clock alternative for GMII/MII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the **CLK125_EN** strap-in pin is pulled high (via the clk125 Enable bit in Common Control Register).

The device provides a dedicated transmit clock input pin (**GTX_CLK**) for GMII mode, which is sourced by the MAC for 1000 Mbps speed.

5.15.1 ISOLATE MODE

When the Isolate (PHY_ISO) bit in the Basic Control Register is set, the device will three-state the GMII output pins and ignore the GMII input pins. The optional **CLK125_NDO** output pin is an exception.

5.15.2 GMII SIGNAL DEFINITION

TABLE 4-12: describes the GMII signals. Refer to Clause 35 of the IEEE 802.3 Specification for more detailed information.

TABLE 5-5: GMII SIGNAL DEFINITION

GMII Signal Name	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
GTX_CLK	Input	Output	Transmit Reference Clock (125 MHz for 1000 Mbps)
TX_EN	Input	Output	Transmit Enable
TXD[7:0]	Input	Output	Transmit Data[7:0]
TX_ER	Input	Output	Transmit Error
RX_CLK	Output	Input	Receive Reference Clock (125 MHz for 1000 Mbps)
RX_DV	Output	Input	Receive Data Valid
RXD[7:0]	Output	Input	Receive Data[7:0]
RX_ER	Output	Input	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detected

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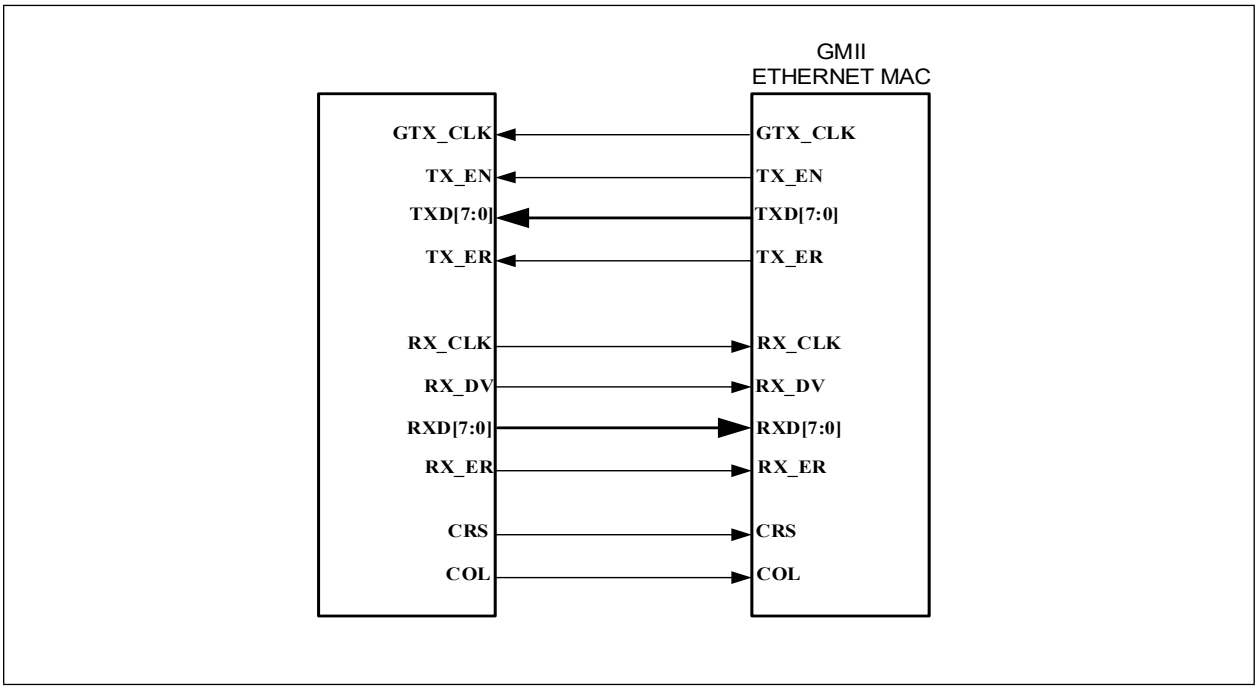
5.15.3 GMII SIGNAL DIAGRAM

The GMII pin connections to the MAC are shown in Figure 5-16:

FIGURE 5-16: GMII INTERFACE



5.16 MII Interface

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 16 pins (7 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10 Mbps and 100 Mbps are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4 bits wide, a nibble.

In MII operation, the MII pins function as follows:

- The PHY sources the transmit reference clock, **TX_CLK**, at 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- The PHY recovers and sources the receive reference clock, **RX_CLK**, at 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- **TX_EN**, **TXD**[3:0], and **TX_ER** are driven by the MAC and transition synchronously with respect to TX_CLK.
- **RX_DV**, **RXD**[3:0], and **RX_ER** are driven by the device and transition synchronously with respect to **RX_CLK**.
- **CRS** and **COL** are driven by the device and do not have to transition synchronously with respect to either **TX_CLK** or **RX_CLK**.

The device combines GMII mode with MII mode to form GMII/MII mode to support data transfer at 10/100/1000 Mbps. After power-up or reset, the device is configured to GMII/MII mode if the **RGMII_EN** configuration strap is set to '0'. See the Configuration Straps section.

The device has the option to output a 125 MHz reference clock on CLK125_NDO. This clock provides a lower-cost reference clock alternative for GMII/MII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the **CLK125_EN** strap-in pin is pulled high (via the clk125 Enable bit in Common Control Register).

The device provides a dedicated transmit clock output pin (**TX_CLK**) for MII mode, which is sourced by the device for 10/100 Mbps speed.

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5.16.1 ISOLATE MODE

When the Isolate (PHY_ISO) bit in the Basic Control Register is set, the device will three-state the MII output pins and ignore the MII input pins. The optional **CLK125_NDO** output pin is an exception.

5.16.2 MII SIGNAL DEFINITION

Table 5-6: describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

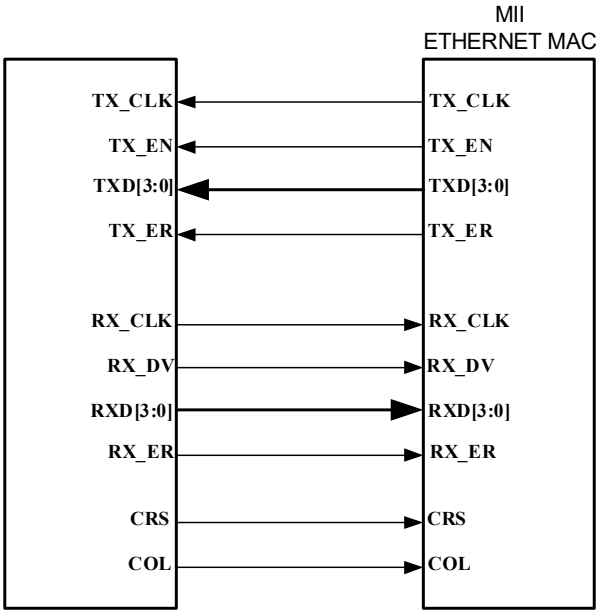
TABLE 5-6: MII SIGNAL DEFINITION

MII Signal Name	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
TX_CLK	Output	Input	Transmit Reference Clock (25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
TX_EN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data[3:0]
TX_ER	Input	Output	Transmit Error
RX_CLK	Output	Input	Receive Reference Clock (25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
RX_DV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data[3:0]
RX_ER	Output	Input	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

5.16.3 MII SIGNAL DIAGRAM

The MII pin connections to the MAC are shown in Figure 5-17:

FIGURE 5-17: MII INTERFACE



5.17 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) supports on-chip data-to-clock delay timing according to the RGMII Version 2.0 Specification, with programming options for external delay timing and to adjust and correct TX and RX timing paths. The RGMII also supports timing modes for the OPEN Alliance SIG TC6 - RGMII EPL (Electrical-Physical Layer) Recommendation for Automotive Application. The on-chip timing delay on the TX and RX clock paths is enabled or disabled as required by the operating mode.

RGMII provides a common interface between RGMII PHYs and MACs, and has the following key characteristics:

- Pin count is reduced from 24 pins for the IEEE Gigabit Media Independent Interface (GMII) to 12 pins for RGMII.
- All speeds (10 Mbps, 100 Mbps, and 1000 Mbps) are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each four bits wide, a nibble.

In RGMII operation, the RGMII pins function as follows:

- The MAC sources the transmit reference clock, **TXC**, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps.
- The PHY recovers and sources the receive reference clock, **RXC**, at 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps.
- For 1000BASE-T, the transmit data, **TXD[3:0]**, is presented on both edges of **TXC**, and the received data, RXD[3:0], is clocked out on both edges of the recovered 125 MHz clock, **RXC**.
- For 10BASE-T/100BASE-TX, the MAC holds **TX_CTL** low until both PHY and MAC operate at the same speed. During the speed transition, the receive clock is stretched on either a positive or negative pulse to ensure that no clock glitch is presented to the MAC.
- **TX_ER** and **RX_ER** are combined with **TX_EN** and **RX_DV**, respectively, to form **TX_CTL** and **RX_CTL**. These two RGMII control signals are valid at the falling clock edge.

On the device, after power-up or reset, the device is configured to RGMII mode if the **RGMII_EN** configuration strap is set to '1'. See the Configuration Straps section.

The device has the option to output a 125 MHz reference clock on the **CLK125_NDO** pin. This clock provides a lower-cost reference clock alternative for RGMII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the **CLK125_EN** strap-in pin is pulled high (via the clk125 Enable bit in Common Control Register).

5.17.1 ISOLATE MODE

When the Isolate (PHY_ISO) bit in the Basic Control Register is set, the device will three-state the RGMII output pins and ignore the RGMII input pins. The optional **CLK125_NDO** output pin is an exception.

5.17.2 RGMII SIGNAL DEFINITION

Table 5-7 describes the RGMII signals. Refer to the RGMII Version 2.0 Specification for more detailed information.

TABLE 5-7: RGMII SIGNAL DEFINITION

RGMII Signal Name	Pin Type (with respect to PHY)	Pin Type (with respect to MAC)	Description
TXC	Input	Output	Transmit Reference Clock (125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps)
TX_CTL	Input	Output	Transmit Control
TXD[3:0]	Input	Output	Transmit Data[3:0]
RXC	Output	Input	Receive Reference Clock (125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps)
RX_CTL	Output	Input	Receive Control
RXD[3:0]	Output	Input	Receive Data[3:0]

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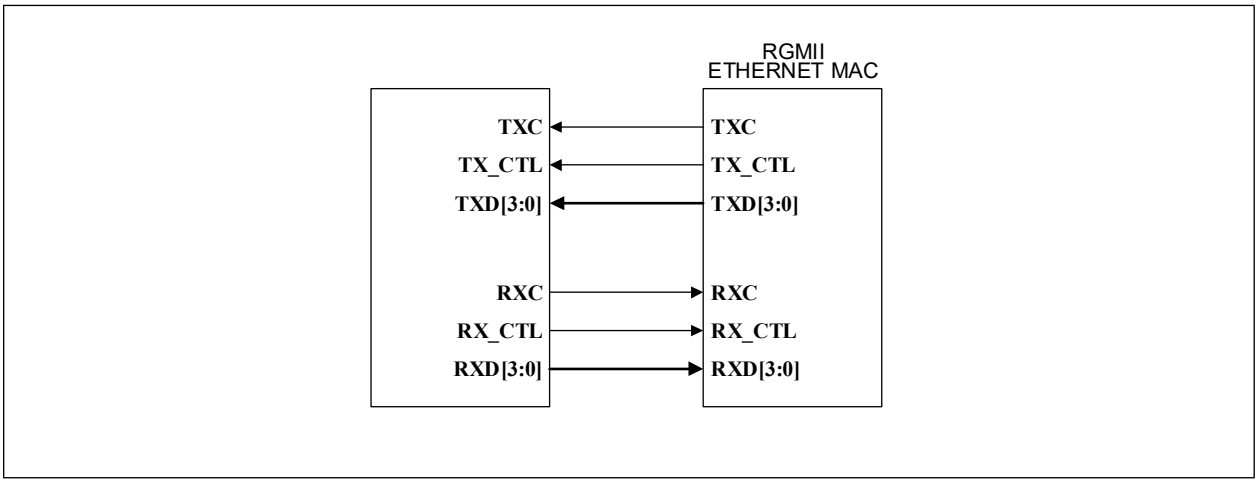
5.17.3 RGMII SIGNAL DIAGRAM

The RGMII pin connections to the MAC are shown in Figure 5-18:

FIGURE 5-18: RGMII INTERFACE



5.17.4 RGMII TIMING

5.17.4.1 RGMII ID Timing / TC6 Delay on Source (DoS) mode

As the default, after power-up or reset, the RGMII timing conforms to the timing requirements in the RGMII Version 2.0 Specification for Internal Delay mode as well as the timing requirements for the TC6 Delay on Source (DoS) mode.

For the transmit path (MAC to PHY), the device does not add any delay locally at its **TXC**, **TX_CTL** and **TXD[3:0]** input pins, and expects the **TXC** delay to be provided on-chip by the MAC.

APPLICATION NOTE: If MAC does not provide any delay or insufficient delay for the **TXC**, the device has two options. The device may add a fixed 2ns, DLL based delay to the **TXC** input. In addition to this fixed delay, pad skew registers can provide up to a 5.8 ns on-chip delay (~4.5 ns additional can be added to **TXC**, ~1.3 ns can be subtracted from **TX_CTL** and **TXD[3:0]**).

For the receive path (PHY to MAC), the device adds a fixed 2ns, DLL based delay to the **RXC** output pin with respect to **RX_CTL** and **RXD[3:0]** output pins.

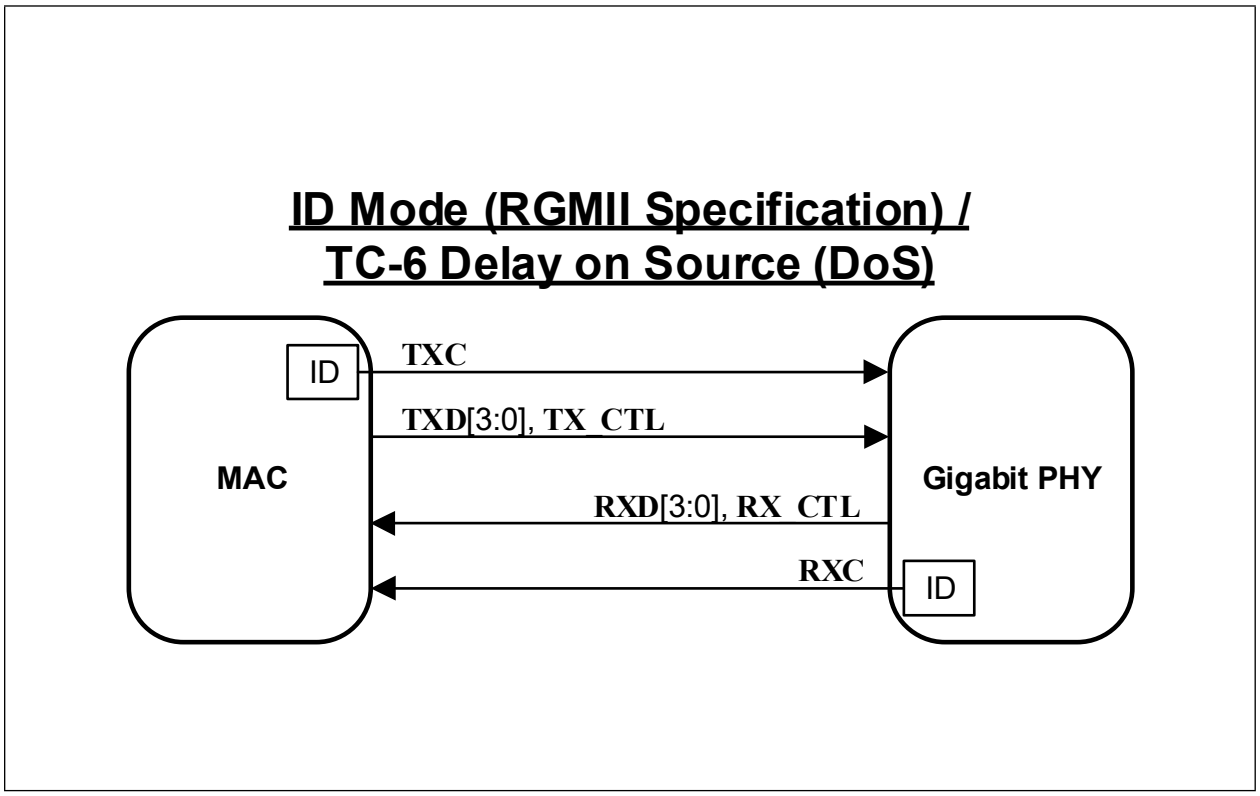
APPLICATION NOTE: If necessary, the device has pad skew registers that can adjust the **RXC** on-chip delay by up to an additional 5.8 ns (~4.5 ns additional can be added to **RXC**, ~1.3 ns can be subtracted from **RX_CTL** and **TXD[3:0]**).

The above default RGMII timings imply:

- **RXC** clock skew is set by the default register settings.
- **TXC** clock skew is provided by the MAC.
- No PCB delay is required for **TXC** and **RXC** clocks.

The following figure illustrates the RGMII Version 2.0 Specification Internal Delay / TC6 Delay on Source (DoS) operation.

FIGURE 5-19: RGMII VERSION 2.0 INTERNAL DELAY / TC6 DELAY ON SOURCE (DoS) OPERATION



When computing the RGMII timing relationships, delays along the entire data path must be aggregated to determine the total delay to be used for comparison between RGMII pins within their respective timing group. For the transmit data path, total delay includes MAC output delay, MAC-to-PHY PCB routing delay, and PHY input delay and skew setting (if any). For the receive data path, the total delay includes PHY output delay, PHY-to-MAC PCB routing delay, and MAC input delay and skew setting (if any).

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Figure 5-20, Figure 5-21 and Table 5-8 from the RGMII v2.0 Specification are provided as references to understanding RGMII v1.3 external delay and RGMII v2.0 on-chip delay timing operation.

FIGURE 5-20: RGMII V2.0 SPEC (MULTIPLEXING AND TIMING DIAGRAM – ORIGINAL RGMII (V1.3) WITH EXTERNAL DELAY)

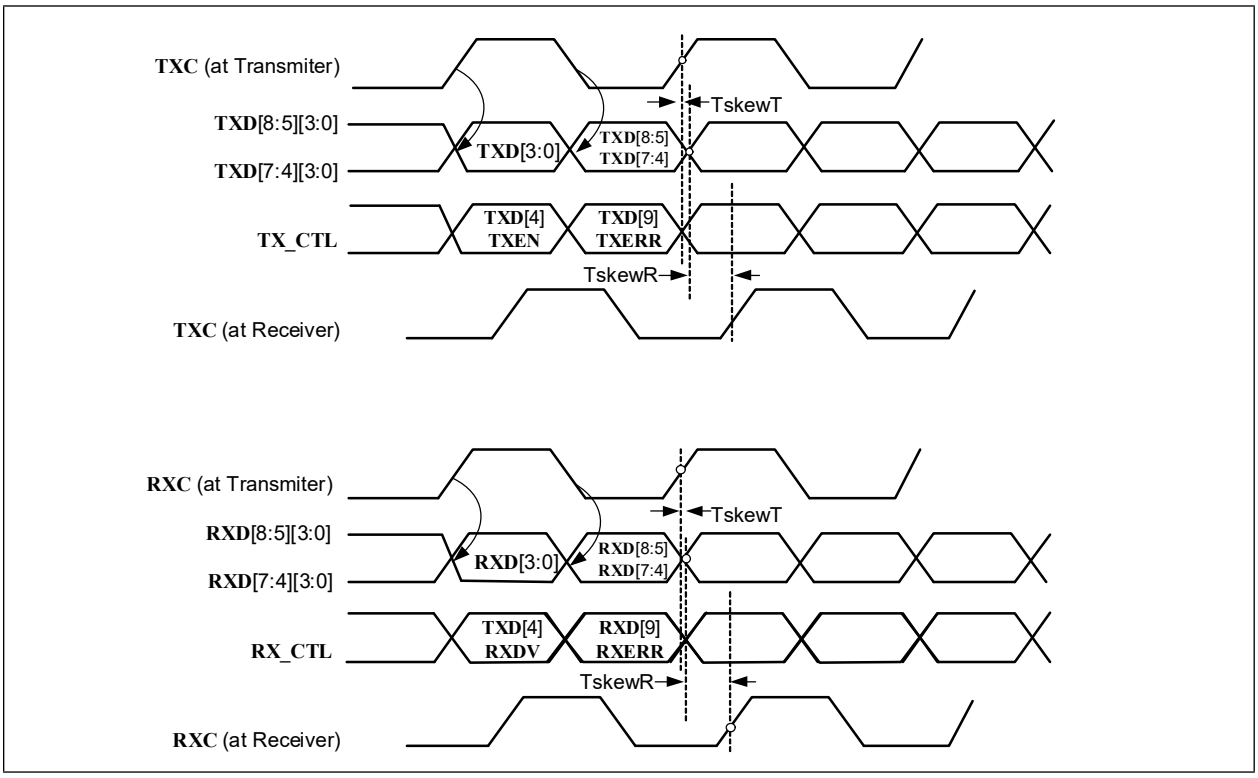
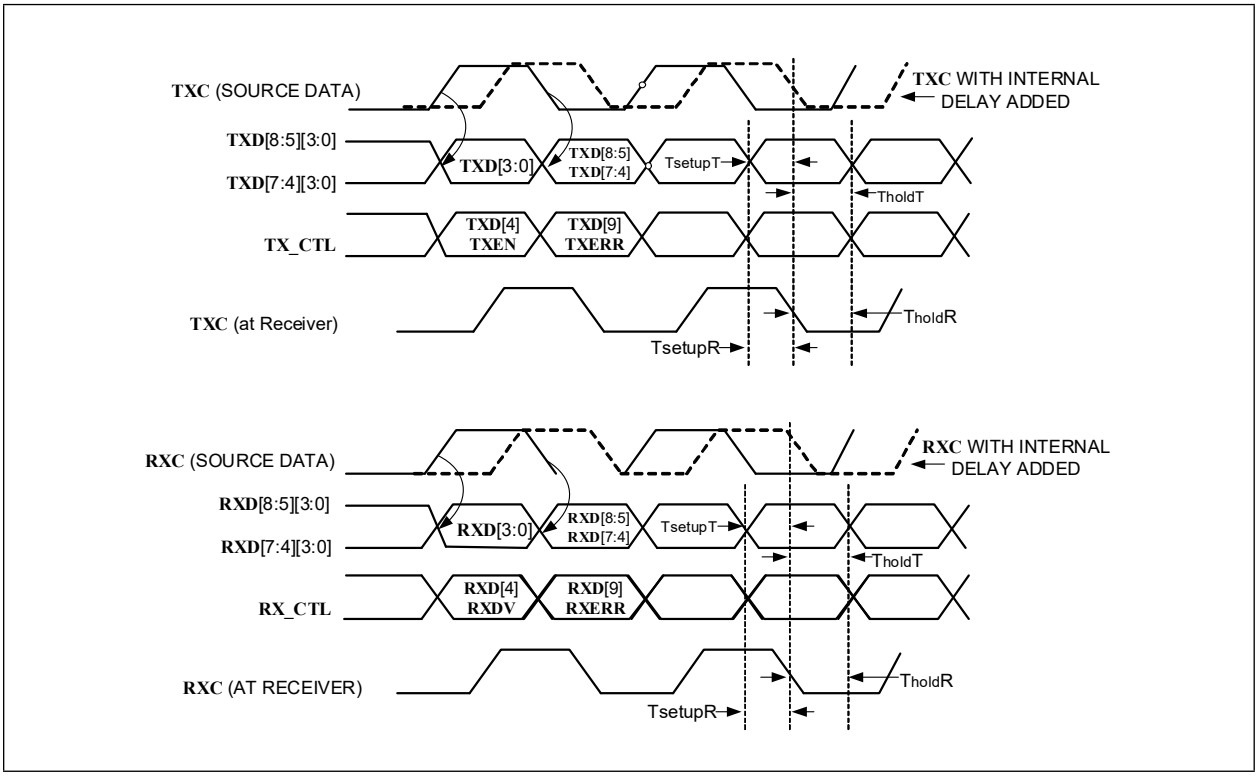


FIGURE 5-21: RGMII V2.0 SPEC (MULTIPLEXING AND TIMING DIAGRAM – RGMII-ID (V2.0) WITH INTERNAL CHIP DELAY)



The following notes provide clarification for Figure 5-21:

TXC (SOURCE DATA), solid line, is the MAC **GTX_CLK** clock output timing per RGMII v1.3 Specification (PCB delay line required or PHY internal delay required)

TXC (SOURCE DATA) WITH INTERNAL DELAY ADDED, dotted line, is the MAC **GTX_CLK** clock output timing per RGMII v2.0 Specification (no PCB delay required and no PHY internal delay required)

RXC (SOURCE DATA), solid line, is the PHY **RX_CLK** clock output timing per RGMII v1.3 Specification (PCB delay line required or MAC internal delay required)

RXC (SOURCE DATA) WITH INTERNAL DELAY ADDED, dotted line, is the PHY **RX_CLK** clock output timing per RGMII v2.0 Specification (no PCB delay required and no MAC internal delay required)

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TABLE 5-8: RGMII V2.0 SPECIFICATION

Parameter	Description	Min.	Typ.	Max.	Units
$T_{skew}T$	Data-to-clock output skew (at transmitter) per RGMII v1.3 (external delay)	-500	—	500	ps
$T_{skew}R$	Data-to-clock input skew (at receiver) per RGMII v1.3 (external delay)	1.0	—	2.6	ns
$T_{setup}T$	Data-to-clock output setup (at transmitter – integrated delay)	1.2	2.0	—	ns
$T_{hold}T$	Clock-to-data output hold (at transmitter – integrated delay)	1.2	2.0	—	ns
$T_{setup}R$	Data-to-clock input setup (at receiver – integrated delay)	1.0	2.0	—	ns
$T_{hold}R$	Clock-to-data input hold (at receiver – integrated delay)	1.0	2.0	—	ns
t_{cyc} (1000BASE-T)	Clock cycle duration for 1000BASE-T	7.2	8.0	8.8	ns
t_{cyc} (100BASE-TX)	Clock cycle duration for 100BASE-TX	36	40	44	ns
t_{cyc} (10BASE-T)	Clock cycle duration for 10BASE-T	360	400	440	ns

The RGMII Version 2.0 Specification defines the RGMII data-to-clock skews only for 1000 Mbps operation, which uses both clock edges for sampling the data and control signals at the 125 MHz clock frequency (8 ns period). For 10/100 Mbps operations, the data signals are sampled on the rising clock edge and the control signals are sampled on both clock edges. With slower clock frequencies, 2.5 MHz (400 ns period) for 10 Mbps and 25 MHz (40 ns period) for 100 Mbps, the RGMII data-to-clock skews for 10/100 Mbps operations will have greater timing margins than for 1000 Mbps operation, and therefore can be relaxed from 2.6 ns (maximum) for 1000 Mbps to 160 ns (maximum) for 10 Mbps and 16 ns (maximum) for 100 Mbps.

5.17.4.2 TC6 Delay on Destination (DoD) mode

In order to support the Delay on Destination (DoD) mode specified by the OPEN Alliance SIG TC6 - RGMII EPL (Electrical-Physical Layer) Recommendation for Automotive Application, the internal delay on the **RXC** is disabled and the internal delay on the **TXC** is enabled. This results in data and control, at the device pins, nominally centered about the clock edges. A bounded skew allows the data and control to occur before or after the clock edges.

For the transmit path (MAC to PHY), the device adds a fixed 2ns, DLL based delay locally at its **TXC** input with respect to **TX_CTL** and **TXD**[3:0] input pins. This effectively provides positive setup and hold timings to the internal flip flops.

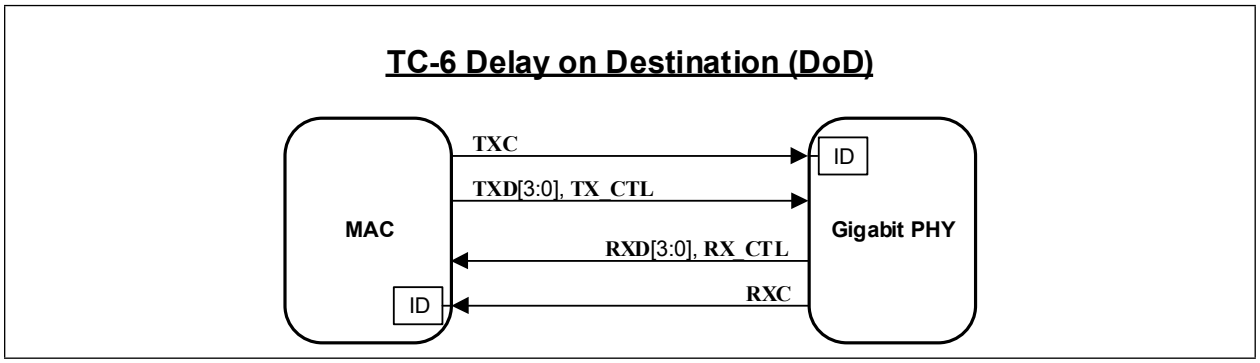
For the receive path (PHY to MAC), the device does not any additional delay locally to the **RXC** output pin. The MAC will provide a delay on its input clock pin.

The above default RGMII timings imply:

- **RXC** clock skew is provided by the MAC.
- **TXC** clock skew is set by the default register settings.
- No PCB delay is required for **TXC** and **RXC** clocks since both devices add internal delay on their input clocks.

The following figure illustrates the TC6 Delay on Destination (DoD) operation.

FIGURE 5-22: TC6 DELAY ON DESTINATION (DoD) OPERATION



5.17.4.3 RGMII DLL BASED CLOCK SKEW

The delays on **RXC** (enabled by default) and optionally on **TXC** (bypassed by default) are provided by internal DLLs. When the RGMII delay is bypassed the delay chain is completely omitted and the DLL output clock is the same as the DLL input clock (except for one multiplexer delay). DLL bypass is controlled by the bypass rxdll and bypass txdll bits of the RX DLL Control Register and the TX DLL Control Register for **RXC** and **TXC** respectively.

When DLL tuning is enabled (normal operation) the DLL is dynamically tuned. The txdll_tap_adj and rxdll_tap_adj fields in the TX DLL Control Register and the RX DLL Control Register are used to statically account for the output multiplexer stage in the delay chain. The larger the value the less of a delay there is on the clock. The DLL tap select value is dynamically calculated and adjusts the delay chain. The txdll_tap_sel and rxdll_tap_sel fields provide the default DLL tap select values before the first tuning cycle occurs.

When DLL tuning is disabled, by setting the rxdll_tune_disable or txdll_tune_disable bits in the RX DLL Control Register or TX DLL Control Register respectively, the DLL is not dynamically tuned but is still used to provide a fixed delay. The txdll_tap_sel and rxdll_tap_sel settings are used as fixed delay values. The txdll_tap_adj and rxdll_tap_adj fields are not used.

The DLL must be reset whenever a new value is programmed in txdll_tap_sel or rxdll_tap_sel fields. This is accomplished by the respective rxdll_reset or txdll_reset bit in the RX / TX DLL Reset and BIST Control Register.

Note:	These bits are not self-clearing and must be set then reset by software.

5.17.4.4 RGMII Pad Skew Registers

It is common to implement RGMII PHY-to-MAC designs that either PHY, MAC, or both PHY and MAC are not fully RGMII v2.0 compliant with on-chip clock delay. These combinations of mixed RGMII v1.3/v2.0 designs and plus sometimes non-matching RGMII PCB trace routings require a review of the entire RGMII system timings (PHY on-chip, PCB trace delay, MAC on-chip) to compute the aggregate clock delay and determine if the clock delay timing is met.

If timing adjustment is needed, pad skew registers are available for all RGMII pins (clocks, control signals, and data bits) to provide programming options to adjust or correct the timing relationship for each RGMII pin. Because RGMII is a source-synchronous bus interface, the timing relationship needs to be maintained only within the RGMII pin's respective timing group.

Clock Invert and Control Signal Pad Skew Register: **RX_CTL, TX_CTL**

RGMII RX Data Pad Skew Register: **RXD3, RXD2, RXD1, RXD0**

RGMII TX Data Pad Skew Register: **TXD3, TXD2, TXD1, TXD0**

Clock Pad Skew Register: **TXC, RXC**

The RGMII control signals and data bits have 4-bit skew settings, while the RGMII clocks have 5-bit skew settings.

Each register value increment is approximately:

Data and control: 56ps (min) to 187ps (max)

RXC and **TXC**: 56ps (min) to 187ps (max)

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A lower value decreases the delay, while a higher value increases the delay.

Table 5-9 and Table 5-10 list the approximate delay for each pad skew (value) setting.

TABLE 5-9: ABSOLUTE DELAY FOR 5-BIT PAD SKEW SETTING

Pad Skew Value	Delay (ns)
0_0000	-0.39(min) / -1.31(max)
0_0001	-0.34(min) / -1.12(max)
0_0010	-0.28(min) / -0.94(max)
0_0011	-0.22(min) / -0.75(max)
0_0100	-0.17(min) / -0.56(max)
0_0101	-0.11(min) / -0.37(max)
0_0110	-0.06(min) / -0.19(max)
0_0111	No delay adjustment (default value)
0_1000	0.06(min) / 0.19(max)
0_1001	0.11(min) / 0.37(max)
0_1010	0.17(min) / 0.56(max)
0_1011	0.22(min) / 0.75(max)
0_1100	0.28(min) / 0.94(max)
0_1101	0.34(min) / 1.12(max)
0_1110	0.39(min) / 1.31(max)
0_1111	0.45(min) / 1.50(max)
1_0000	0.50(min) / 1.68(max)
1_0001	0.56(min) / 1.87(max)
1_0010	0.62(min) / 2.06(max)
1_0011	0.67(min) / 2.24(max)
1_0100	0.73(min) / 2.43(max)
1_0101	0.78(min) / 2.62(max)
1_0110	0.84(min) / 2.81(max)
1_0111	0.90(min) / 2.99(max)
1_1000	0.95(min) / 3.18(max)
1_1001	1.01(min) / 3.37(max)
1_1010	1.06(min) / 3.55(max)
1_1011	1.12(min) / 3.74(max)
1_1100	1.18(min) / 3.93(max)
1_1101	1.23(min) / 4.11(max)
1_1110	1.29(min) / 4.30(max)
1_1111	1.34(min) / 4.49(max)

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TABLE 5-10: ABSOLUTE DELAY FOR 4-BIT PAD SKEW SETTING

Pad Skew Value	Delay (ns) (Si B0) (est.)
0000	-0.39(min) / -1.31(max)
0001	-0.34(min) / -1.12(max)
0010	-0.28(min) / -0.94(max)
0011	-0.22(min) / -0.75(max)
0100	-0.17(min) / -0.56(max)
0101	-0.11(min) / -0.37(max)
0110	-0.06(min) / -0.19(max)
0111	No delay adjustment (default value)
1000	0.06(min) / 0.19(max)
1001	0.11(min) / 0.37(max)
1010	0.17(min) / 0.56(max)
1011	0.22(min) / 0.75(max)
1100	0.28(min) / 0.94(max)
1101	0.34(min) / 1.12(max)
1110	0.39(min) / 1.31(max)
1111	0.45(min) / 1.50(max)

The following examples show how to read/write to the Clock Pad Skew Register **(**MMD Address 2h, Register 8h) for the RGMII **TXC** and **RXC** skew settings. MMD register access is through the MMD Access Control Register and MMD Access Address/Data Register. For more programming details, refer to the MMD Registers section.

- Read back value of MMD Address 2h, Register 8h.
  - Write MMD Access Control Register = 0x0002 // Select MMD Device Address 2h
  - Write MMD Access Address/Data Register = 0x0008 // Select Register 8h of MMD Device Address 2h
  - Write MMD Access Control Register = 0x4002 // Select register data for MMD Device Address 2h, Register 8h
  - Read MMD Access Address/Data Register // Read value of MMD Device Address 2h, Register 8h
- Write value 0x03FF (delay **TXC** and RXC pad skews to their maximum values) to the Clock Pad Skew Register **(**MMD Address 2h, Register 8h)
  - Write MMD Access Control Register = 0x0002 // Select MMD Device Address 2h
  - Write MMD Access Address/Data Register = 0x0008 // Select Register 8h of MMD Device Address 2h
  - Write MMD Access Control Register = 0x4002 // Select register data for MMD Device Address 2h, Register 8h
  - Write MMD Access Address/Data Register = 0x03FF // Write value 0x03FF to MMD Device Address 2h, Register 8h

5.17.5 RGMII IN-BAND STATUS

The device provides in-band status to the MAC during the inter-frame gap when **RX_CTL** is de-asserted. RGMII in-band status is always enabled after power-up.

The in-band status is sent to the MAC using the **RXD[3:0]** data pins, and is described in Table 5-11.

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TABLE 5-11: RGMII IN-BAND STATUS

RX_CTL	RXD3	RXD[2:1]	RXD0
0 / 0 (equivalent to **RX_DV** = 0 / **RX_ER** = 0)	Duplex Status 0 = Half-duplex 1 = Full-duplex	**RX_CLK** clock speed 00 = 2.5 MHz (10 Mbps) 01 = 25 MHz (100 Mbps) 10 = 125 MHz (1000 Mbps) 11 = Reserved	Link Status 0 = Link down 1 = Link up

5.17.6 RGMII EEE LOW POWER IDLE

The device supports EEE Low Power Idle on the RGMII interface. This is encoded as **RX_CTL** = 0/1 (equivalent to **RX_DV** = 0 / **RX_ER** = 1) and **RXD[3:0]** = 0x1 / 0x0 (equivalent to **RXD[7:0]** = 0x01) for receive and as **TX_CTL** = 0/1 (equivalent to **TX_EN** = 0 / TX_ER = 1) and **TXD[3:0]** = 0x1 / 0x0 (equivalent to **TXD[7:0]** = 0x01) for transmit.

5.18 Start of Frame (SOF) Indication

The device supports the generation of an SOF pulse for the receive and transmit paths. The SOF pulse is generated when the Start of Frame Delimiter (SFD octet 0xD5 immediately following the preamble) is detected by the PCS and can be output onto any enabled GPIO pin by setting the corresponding bits in the General Purpose IO Data Select 1 Register (GPIO_DATA_SEL1) or the General Purpose IO Data Select 2 Register (GPIO_DATA_SEL2).

The SOF pulse is always active high.

Note:	The GPIO needs to be enabled and its direction set as an output via the General Purpose IO Enable Register (GPIO_EN) and the General Purpose IO Direction Register (GPIO_DIR). The GPIO Buffer Type (GPIO_BUF) field in the General Purpose IO Buffer Type Register (GPIO_BUF) also applies.

5.18.1 802.3BR FRAME PREEMPTION

The SOF pulse can also be configured to detect 802.3br-2016 Start mPacket Delimiters (SMDs). When the SOF_preemption_enable bits in MMD2 Register 75 are set to “10”, the SOF pulse is generated for any of the SMD values listed in 802.3br-2016 *except* for the continuation frame: SMD-V (0x07), SMD-R (0x19), SMD-E (0xD5) and SMD-S[0,1,2,3] (0xE6. 0x4C, 0x7F or 0xB3). When the SOF_preemption_enable bits are set to “11”, the SOF pulse is also generated for the continuation SMD values: SMD-C[0,1,2,3] (0x61, 0x52, 0x9E or 0x2A).

5.18.2 SOF LATENCY

There is a fixed timing relationship from the time the transmitted SFD arrives at the PCS to when it appears on the line and from when the received SFD arrives on the line to when it is detected by the PCS. The latencies between the SFD pulse and the wire are as follows:

TABLE 5-12: SOF LATENCY

Speed	TX SFD Latency (start of SFD pulse to start of SFD on MDI output)	TX Variation per Link Up	TX Variation per Frame	RX SFD Latency (start of SFD on MDI input to start of SFD pulse)	RX Variation per Link Up	RX Variation per Frame
1000Mbps	138ns	0ns	0ns	430ns	0ns	+/-4ns
100Mbps (fixed mode Note 5-1)	140ns	0ns	0ns	615ns	0ns	+/-4ns
100Mbps (variable mode Note 5-1)	140ns	<2ns	0ns	488ns, 492ns, 498ns, 504ns, 508ns, 512ns, 520ns, 524 ns	8 @ 4ns steps	<2ns
10Mbps	654ns	0ns	0ns	2277ns, 2377ns, 2477ns, 2577ns	4 @ 100ns steps	+/-4ns

Note 5-1 For 100BASE-TX, at the expense of an increased variation between various link establishments, the receive latency may be reduced by clearing the Fixed 100BT latency bit in the Reserved Register.

5.19 MII Management (MIIM) Interface

The device supports the IEEE 802.3 MII management interface, also known as the Management Data Input / Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the device. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows an external controller to communicate with one or more devices. Each device is assigned a unique PHY address between 0h and 1Fh by the **PHYAD[4:0]** strapping pins.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers. See the Register Map section.

Table 5-13 shows the MII management frame format for the device.

TABLE 5-13: MII MANAGEMENT FRAME FORMAT

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

5.19.1 ALL PHYS ADDRESS

Normally, the Ethernet PHY is accessed at the PHY address set by the **PHYAD** strapping pins.

PHY Address 0h is optionally supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set the Basic Control Register to a value of 0x1940 to set Bit [11] to a value of one to enable software power-down).

PHY address 0 is enable (in addition to the PHY address set by the PHYAD strapping pins) when the All-PHYAD Enable bit in the Common Control Register is a 1.

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5.19.2 MDIO OUTPUT DRIVE MODE

The MDIO output pin drive mode is controlled by the MDIO Buffer Type bit in Output Control Register. When set to a 0, the MDIO output is open-drain. When set to a 1, the MDIO output is push-pull.

5.19.3 HIGHER-SPEED MDIO OPERATION

The MDIO bus can operate at standard speeds up to 2.5 MHz, as well higher speeds up to 8.33 MHz.

Default register values enable standard MDIO operation, that is MDIO operation up to 2.5 MHz MDC frequency with multiple PHYs on the MDIO bus, using an open-drain MDIO driver. Due to the use of an open-drain driver an external 1kΩ to 4.7kΩ pull-up resistor is required.

Up to 8.33 MHz, open-drain MDIO operation is supported however it is limited to a single PHY on the MDIO bus and requires the used of a 1kΩ external pull-up resistor.

The device can be configured to use a push-pull MDIO driver. The reconfiguration process requires initially running the MDIO bus at 2.5 MHz since an open-drain MDIO driver is used by default. The push-pull MDIO driver allows operation up to 8.33 MHz with the 1kΩ external pull-up resistor.

5.19.4 CLAUSE 45 PROTECTION

To facilitate interoperability with other PHYs that are managed with Clause 45 of the IEEE 802.3 Specification, the MIIM Interface will ignore management frames that do not contain a Start of Frame field equal to ‘01’.

APPLICATION NOTE: If preamble suppression is allowed (MF Preamble Suppression in the Basic Status Register equals 1) and the Start of Frame field is not equal ‘01’, the MIIM Interface will ignore the entire frame. It will not falsely detect the remainder of the frame as a new frame.

5.20 Interrupt (INT_N)

The **INT_N** pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the device. The Interrupt Enable Register contains the interrupt control bits that enable and disable the conditions for asserting the **INT_N** signal. The Interrupt Status Register contains the interrupt status bits that indicate which interrupt conditions have occurred. Most interrupt status bits are cleared upon reading. Some bits are read only and have a lower level register to indicate individual sources.

Note:	Bits in the Interrupt Status Register are set by the interrupt events regardless of the value of the corresponding bits in the Interrupt Enable Register.

The **INT_N** buffer type is selectable between open-drain and push-pull and is configured by the INT Buffer Type field in the Output Control Register. The default is open-drain.

The Intr Polarity Invert bit in the Control Register sets the interrupt level to active high or active low. The default is active low. If the buffer type is set to open-drain, the polarity is forced to be active low.

5.21 LED Support

The device provides five programmable LED output pins, **LED5** through **LED1**, which are configurable to support three LED modes. The LED mode is configured by the **LED_MODE** strap-in as well as the LED Mode bit in the UNH Test Register and is defined as follows:

- Individual-LED Mode: LED Mode = 1, **LED_MODE** strap input high (pulled up)
- Tri-Color LED Mode: LED Mode = 1, **LED_MODE** strap input low (pulled down) or left floating
- Enhanced LED Mode: LED Mode = 0, **LED_MODE** strap input is unused

Each LED output pin can directly drive an LED with a series resistor (typically 220Ω to 470Ω).

5.21.1 INDIVIDUAL-LED MODE

In Individual-LED mode, Table 5-14 specifies the LED functionality. The LED function is controlled by the mr_led_sel field in the PCS Loop-back Swap/Polarity Control Register.

Note: **LED_MODE** strap is pull-down by default (Tri-Color Mode). **LED_MODE** must be pulled up to enable Individual-LED Mode.

Note: The LEDs are forced OFF when the Isolate (PHY_ISO) bits in the Basic Control Register is set.

Note: The LEDs are forced OFF when the Power Down bit in the Basic Control Register is set.

TABLE 5-14: INDIVIDUAL-LED MODE - PIN DEFINITION

LED Pin	Pin State Note 5-2	LED Definition	mr_led_sel=11b	mr_led_sel=10b	mr_led_sel=01b	mr_led_sel=00b
LED5	H	OFF	No Link 100	No Link 100	No Link 100	rsvd
	L	ON	Link 100	Link 100	Link 100	
	Toggle	Blinking	-	Activity 100	-	
LED4	H	OFF	No Link 1000	No Link 1000	No Link 1000	rsvd
	L	ON	Link 1000	Link 1000	Link 1000	
	Toggle	Blinking	-	Activity 1000	-	
LED3	H	OFF	Link Off or Half Duplex	Link Off or Half Duplex	Link Off or Half Duplex	rsvd
	L	ON	Full Duplex and Link On (any speed)	Full Duplex and Link On (any speed)	Full Duplex and Link On (any speed)	
	Toggle	Blinking	Collision	Collision	Collision	
LED2	H	OFF	Link Off			
	L	ON	Link On (any speed)			
LED1	H	OFF	No Activity			
	Toggle	Blinking	Activity (RX, TX)			

Note 5-2 Assuming active low LEDs.

5.21.2 TRI-COLOR LED MODE

In Tri-color LED mode, the link and activity status are indicated by the **LED2** pin for 1000BASE-T; by the **LED1** pin for 100BASE-TX; and by both **LED2** and **LED1** pins, working in conjunction, for 10BASE-T. This is summarized in Table 5-15.

Note: This mode applies only to **LED1** and **LED2**, the other LEDs operate in Individual-LED mode.

Note: The LEDs are forced OFF when the Isolate (PHY_ISO) bits in the Basic Control Register is set.

Note: The LEDs are forced OFF when the Power Down bit in the Basic Control Register is set.

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TABLE 5-15: TRI-COLOR LED MODE - PIN DEFINITION

LED Pin (State) Note 5-3		LED Pin (Definition)		Link/Activity
LED2	LED1	LED2	LED1	
H	H	OFF	OFF	Link Off
L	H	ON	OFF	1000 Link/No Activity
Toggle	H	Blinking	OFF	1000 Link/Activity (RX, TX)
H	L	OFF	ON	100 Link/No Activity
H	Toggle	OFF	Blinking	100 Link/Activity (RX, TX)
L	L	ON	ON	10 Link/No Activity
Toggle	Toggle	Blinking	Blinking	10 Link/Activity (RX, TX)

Note 5-3 Assuming active low LEDs.

5.21.3 ENHANCED LED MODE

Enhanced LED mode is enabled when the device LED Mode bit in the UNH Test Register is cleared. In Enhanced LED mode, each LED can be configured to display different status information that can be selected by setting the corresponding LED Configuration field of the LED Mode Select Register. The modes are shown in Table 5-16. The blink/pulse-stretch and other LED settings can be configured via the LED Behavior Register.

Note: This mode applies only to **LED1**, **LED2**, **LED3** and **LED4**. **LED5** is disabled in this mode.

Note: The LEDs are forced OFF when the Power Down bit in the Basic Control Register is set.

TABLE 5-16: LED MODE AND FUNCTION SUMMARY

Mode	Name	Description
0	Link/Activity	1 (led off) = No link in any speed on any media interface. 0 (led on) = Valid link at any speed on any media interface. Blink or pulse stretch (led turns off) = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1 (led off) = No link at 1000BASE-T. 0 (led on) = Valid link at 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 1000BASE-T with activity present.
2	Link100/Activity	1 (led off) = No link at 100BASE-TX. 0 (led on) = Valid link at 100BASE-TX. Blink or pulse stretch (led turns off) = Valid link at 100BASE-TX with activity present.
3	Link10/Activity	1 (led off) = No link at 10BASE-T. 0 (led on) = Valid link at 10BASE-T. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T with activity present.
4	Link100/1000/Activity	1 (led off) = No link at 100BASE-TX or 1000BASE-T. 0 (led on) = Valid link at 100BASE-TX or 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 100BASE-TX or 1000BASE-T, with activity present.
5	Link10/1000/Activity	1 (led off) = No link at 10BASE-T or 1000BASE-T. 0 (led on) = Valid link at 10BASE-T or 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T or 1000BASE-T, with activity present.

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TABLE 5-16: LED MODE AND FUNCTION SUMMARY (CONTINUED)

Mode	Name	Description
6	Link10/100/Activity	1 (led off) = No link at 10BASE-T or 100BASE-TX. 0 (led on) = Valid link at 10BASE-T or 100BASE-TX. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T or 100BASE-TX, with activity present.
7	RESERVED	RESERVED
8	Duplex/Collision	1 (led off) = Link established in half-duplex mode, or no link established. 0 (led on) = Link established in full-duplex mode. Blink or pulse stretch (led turns on) = Link established in half-duplex mode but collisions are present.
9	Collision	1 (led off) = No collisions detected. Blink or pulse stretch (led turns on) = Collision detected.
10	Activity	1 (led off) = No activity present. Blink or pulse stretch (led turns on) = Activity present. (becomes TX activity present if the LED Activity Output Select bit in the LED Behavior Register is set to 1.)
11	RESERVED	RESERVED
12	Auto-Negotiation Fault Parallel Detect Fault	1 (led off) = No Parallel Detect fault present. 0 (led on) = Parallel Detect fault occurred.
13	RESERVED	RESERVED
14	Force LED Off	1 (led off) = De-asserts the LED.
15	Force LED On	0 (led on) = Asserts the LED.

5.21.3.1 LED Behavior

Using the LED Behavior Register, the following LED behaviors can be configured.

- LED Combine
- LED Blink or Pulse-Stretch
- Rate of LED Blink or Pulse-Stretch
- LED Pulsing Enable

5.21.3.1.1 LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin via the LED Combination Disables field of the LED Behavior Register. For example, a copper link running in 1000BASE-T mode with activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display if the combine feature is disabled.

5.21.3.1.2 LED Blink or Pulse-Stretch

This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin via the LED Pulse Stretch Enables field of the LED Behavior Register. Activity and collision events can occur randomly and intermittently throughout the link-up period.

Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin.

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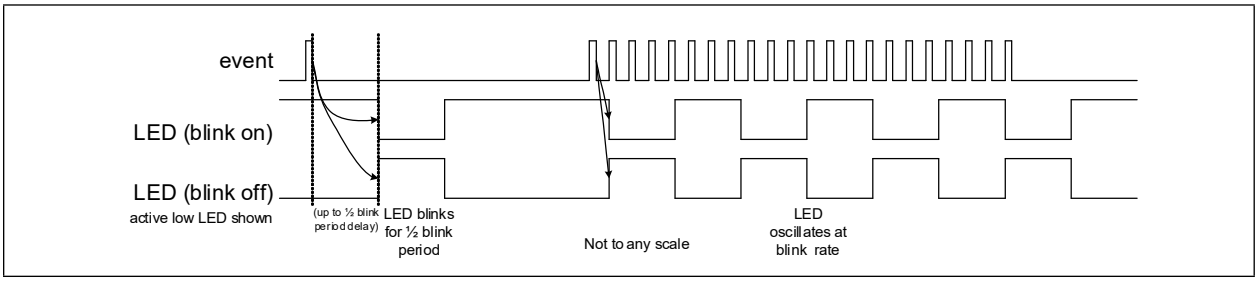
As shown in Figure 5-23, for a single event, the LED will blink (either on or off depending on the LED function) for half of the blink period. For continual events, the LED will oscillate at the blink rate.

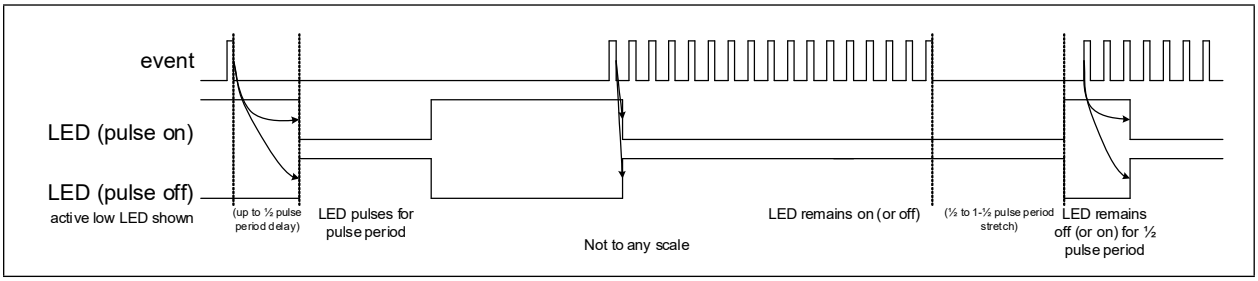
FIGURE 5-23: LED BLINK PATTERN



Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present.

As shown in Figure 5-24, for a single event, the LED will pulse (either on or off depending on the LED function) for the full pulse period. For continual events, the LED will remain on (or off) and will extend from a half to one and a half pulse periods once the events terminate. Once off (or on), the LED will remain in that state for at least a half pulse period.

FIGURE 5-24: LED PULSE PATTERN



The blink / pulse stretch rate can be configured, as detailed in Section 5.21.3.1.3, "Rate of LED Blink or Pulse-Stretch".

5.21.3.1.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when the blink/pulse-stretch is enabled (LED Pulse Stretch Enables) on an LED pin. This can be uniquely configured for each LED pin via the LED Blink / Pulse-Stretch Rate field of the LED Behavior Register. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms.

5.21.3.1.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be modulated at 5 kHz, 20% duty cycle, by setting the LED Pulsing Enable bit of the LED Behavior Register.

5.21.4 LED POLARITY AND BUFFER TYPE

The LED polarity is configured by the LED Polarity field in the Output Control Register. The default of this register is set by the strap values on the LED pins themselves, effectively making the polarity self setting.

The design of the LED polarity control takes into account that the LEDs are forced OFF with the Power Down and Isolate (PHY_ISO) bits in the Basic Control Register, no matter the polarity.

The LED buffer type is selectable between open-drain/open-source and push-pull and is configured by the LED Buffer Type field in the Output Control Register. If open-drain/open-source is selected, the polarity then determines open-drain (active low) and open-source (active high).

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5.22 GPIOs

The GPIO controller is comprised of 10 programmable input / output pins that are shared with other pins (see Section 3.4, "Pin Alternate Functions"). These pins are individually configurable via the GPIO registers.

For a pin to function as its GPIO, the GPIO must be enabled via the corresponding bit in the General Purpose IO Enable Register (**GPIO_EN**).

When configured as an input, via the General Purpose IO Direction Register (GPIO_DIR), the pin's pull-up is enabled. The corresponding General Purpose IO Data Register (GPIO_DATA) bit reflects the current state of the GPIO input.

Extreme care must be taken on strap input pins that may be used for General Purpose Inputs. The General Purpose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.

When configured as an output, the output buffer type is selected by the corresponding bit in the General Purpose IO Buffer Type Register (GPIO_BUF). Push/pull and open-drain output buffers are supported for each GPIO.

When functioning as an open-drain driver, the GPIO output pin is driven low when the corresponding bit in the General Purpose IO Data Register (GPIO_DATA) is cleared to 0 and is not driven when set to 1.

When a GPIO is enabled as a push/pull output, the value output to the GPIO pin is controlled via the corresponding bit in the General Purpose IO Data Register (GPIO_DATA).

When a GPIO is set to an output, the pin's pull-up is disabled, however the pin's input buffer remains enabled. A read of the General Purpose IO Data Register (GPIO_DATA) still returns the state of the GPIO input (not the previous value written to the register).

Note:	Unless otherwise determined by the normal pin function, the pull-up is only enabled if the pin is set as a GPIO input.

APPLICATION NOTE: Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
When functioning as an output, the pin's pull-up is disabled. An open-drain output may require an external pull-up depending on the application.

5.22.1 GPIO INTERRUPTS

Each GPIO provides the ability to trigger a unique GPIO interrupt in the General Purpose IO Interrupt Status Register (GPIO_INT_STS). Reading the GPIO Interrupt (**GPIO_INT**) bits of this register provides the current status of the corresponding interrupt. Each interrupt is enabled by setting the corresponding General Purpose IO Interrupt Enable Register (GPIO_INT_EN) bit. The GPIO Controller aggregates the enabled interrupt values into an internal signal that is sent to the main interrupt logic and is reflected via the GPIO Interrupt bit in the Interrupt Status Register.

Note:	Bits in the General Purpose IO Interrupt Status Register (GPIO_INT_STS) are set by the interrupt events regardless of the value of the corresponding bits in the General Purpose IO Interrupt Enable Register (GPIO_INT_EN).

As interrupts, GPIO inputs are level sensitive and must be active for greater than ~85 nS to be recognized (sampled by 2 consecutive 25MHz edges).

APPLICATION NOTE: Upon reset, GPIOs that were outputs may generate an active interrupt status as the system settles - typically when a low GPIO pin slowly rises due to the internal pull-up. The interrupt status bits within the General Purpose IO Interrupt Status Register (GPIO_INT_STS) should be cleared as part of the device initialization software routine.

5.22.1.1 GPIO Interrupt Polarity

The interrupt polarity can be set for each individually via the General Purpose IO Interrupt Polarity Register (GPIO_INT_POL). When set, a high logic level on the GPIO pin will set the corresponding interrupt bit in the General Purpose IO Interrupt Status Register (GPIO_INT_STS). When cleared, a low logic level on the GPIO pin will set the corresponding interrupt bit.

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5.22.2 GPIO ALTERNATE USAGE

Each GPIO has the ability to be used as for an alternate function. Once enabled as a GPIO, the output source is selected by the bits in the General Purpose IO Data Select 1 Register (GPIO_DATA_SEL1) and in the General Purpose IO Data Select 2 Register (GPIO_DATA_SEL2). The output buffer type (General Purpose IO Buffer Type Register (GPIO_BUF) applies to all of output sources.

5.23 Self-Test Frame Generation and Checking

The device is capable of generating and checking frames.

Normally, when connected to a link partner, a valid link-up indication must be established before test frames are generated. For certain cases, for example 10BASE-T compliance testing, a link partner may not be present. The Force_self_test_pgen_en bit in the Self-Test PGEN Enable Register may be used to override the link-up requirement.

If desired, the device can be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D, as shown in Figure 5-15.

If a loopback connector is to be used,

- Auto-negotiation should be disabled, full duplex set and the desired link speed set via the Basic Control Register.
- For 10BASE-T and 100BASE-TX:
  - Auto-MDIX should be disabled and the desired configuration (MDI vs. MDIX) selected via the swapoff and mdi_set bits in the Digital Debug Control 1 Register. Selecting MDI vs. MDIX will test different sections of the PHY.
- For 1000BASE-T:
  - Set the Leader-Follower configuration to leader by setting the Master/Slave Manual Configuration Enable and Master/Slave Manual Configuration Value bits in the Auto-Negotiation Master Slave Control Register.
  - Enable the 1000BASE-T connector loopback by setting the Ext_lpbk bit in the Reserved Register.

Two frame generation modes can be enabled. Single-Stream and Multiple-Stream.

5.23.1 SINGLE-STREAM FRAME GENERATION

In Single-Stream mode frames are sent at line-rate with a minimum Inter Frame Gap (IFG).

The Single-Stream frame has a length between 64 and 1518 bytes (including the MAC source and destination addresses, the Type/Length Field and the FCS). The frame length can be randomly selected or can be set to a fixed value by using the Self_test_packet_fixed_size_enable and Self_test_packet_fixed_size_length fields in the Self-Test PGEN Configuration Register. Note the Self_test_packet_fixed_size_length field does not include the MAC source and destination addresses, the Type/Length Field or the FCS.

The frame's MAC source and destination, Type/Length Field and payload can be set to all ones or all zeros as selected by the Self_test_packet_type[1:0] field in the Self-Test Enable Register.

If not set to all ones or all zeros, the MAC source and destination can be fully random using the Self_test_packet_random_MAC field in the Self-Test PGEN Configuration Register. If not fully random, one of two MAC source and destination address pairs is randomly selected from the DES1/SRC1 Register or the DES2/SRC2 Register.

If not set to all ones or all zeros, the Type/Length Field is set to the frame length selected above (not including the 18 bytes of MAC source and destination addresses, the Type/Length Field and the FCS).

If not set to all ones or all zeros, the frame payload is random.

The preamble, SFD and FCS are normal values.

Single-Stream frame generation is enabled by setting a frame count into the Self-Test Packet Count LO Register and Self-Test Packet Count HI Register and then setting the following in order:

- Force_self_test_pgen_en bit in the Self-Test PGEN Enable Register if needed to bypass link-up
- Self_test_en bit in the Self-Test Enable Register
- Self_test_frame_cnt_en bit in the Self-Test Frame Count Enable Register
- Self_test_pgen_en bit in the Self-Test PGEN Enable Register

5.23.2 MULTIPLE-STREAM FRAME GENERATION

In Multiple-Stream mode bursts of frames are sent at line-rate with a minimum IFG and with a random idle time between each burst. EEE LPI can be enabled during the idle time.

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The frame count for each burst is randomly selected as mask by the Frame Counter Mask Register.

The frame's MAC source and destination, Type/Length Field and payload can be set to all ones or all zeros as selected by the Self_test_packet_type[1:0] field in the Self-Test Enable Register.

If not set to all ones or all zeros, the MAC source and destination can be fully random using the Self_test_packet_random_MAC field in the Self-Test PGEN Configuration Register. If not fully random, one of two MAC source and destination address pairs is randomly selected at the beginning of each burst from the DES1/SRC1 Register or the DES2/SRC2 Register.

If not set to all ones or all zeros, the Type/Length Field is set to the frame length selected above (not including the 18 bytes of MAC source and destination addresses, the Type/Length Field and the FCS).

If not set to all ones or all zeros, the frame payload is random.

At the end of each burst a random idle time occurs. This is followed by a random period of EEE LPI (sleep) and then followed by a random wake-up recover time. The random time of sleep can be controlled with the Sleep Timer Counter Mask Register and the Sleep Counter Minimum Register. The sending of EEE LPI is enabled with the St_no_lpi bit in the Multi stream Control Register. Using the PHYs carrier sense EEE timer in lieu of the random wake-up timer can be enabled with the Crs_use_timer bit in the Multi stream Control Register.

Multiple-Stream mode is enabled by setting the following:

- Force_self_test_pgen_en bit in the Self-Test PGEN Enable Register if needed to bypass link-up
- Self_test_en bit in the Self-Test Enable Register
- St_multi_stream_en bit in the Multi stream Control Register
- St_frame_ctrl_en bit in the Multistream Start Register

Multiple-Stream mode runs continuously until disabled by clearing the St_frame_ctrl_en bit.

Optionally the Multiple-Stream mode can run for approximately 1 second by setting the Ipef_en bit in the Multi stream Control Register.

The cumulative count of frames that was sent for each destination / source pair can be read via the Self-Test Source 1/2 Count HI Extended, HI and LO Registers. These counters can be reset by setting and clearing the clr_src_frame bit in the Clear Source Counters Register.

5.23.3 FRAME CHECKING

There are three frame CRC checkers available, one on TX data from the MAC and two on the receive data from the line.

A count of good and errored frames from the MAC TX is available in the TX Correct Count HI Extended, HI and LO Registers and the TX Error Count HI and LO Registers. These counters are enabled by setting the GMII_TX_CRC_check_en bit in the Self-Test Enable Register. Clearing the GMII_TX_CRC_check_en bit clears the counters.

Two sets of good and errored frames counters received are available in the Self-Test Stream 1/2 Correct Count HI Extended, HI and LO Registers and the Self-Test Stream 1/2 Error Count HI and LO Registers.

Normally both sets of counters will count all frames. When the St2_trig_en or St1_trig_en bit in the Multi stream Control Register is set, the corresponding counter set will be qualified by matching the MAC destination address in the frame to the source address set in the DES1/SRC1 Register or in the DES2/SRC2 Register.

APPLICATION NOTE: In a PHY to PHY test, the DES1 and SRC1 (and DES2 and SRC2) settings in each PHY would be reversed such that PHY A sends frames to the MAC destination address that PHY B has set as it source. Hence the counters qualify the received frame's destination address with the local SRC addresses.

These counters are enabled by setting the Self_test_CRC_checker_enable bit in the Self-Test Enable Register. Clearing the Self_test_CRC_checker_enable bit clears the counters.

The counters have an option to automatically clear on a link down event. This is enabled by setting the Self_test_clear_counters_on_link_down bit in the Self-Test Enable Register.

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5.24 Power Management

The device incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

5.24.1 SMART POWER SAVING

For shorter cable lengths (< ~70 meters) the signal to noise ratio is sufficiently high to allow the reduction of ADC resolution as well as DPS taps, Based on the detected cable length, the device automatically reduces power consumption by approximately 20mW.

5.24.2 ENERGY-DETECT POWER-DOWN MODE (EDPD)

The device supports an Energy-Detect-Power-Down (EDPD) mode to save power when there is no link partner sending signals.

In EDPD Mode, the device shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Power can be reduced further by extending the time interval between the transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the device and its link partner, when operating in the same low-power state and with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them.

By default, EDPD mode is disabled after power-up. EDPD is enabled by setting the p_edpd_en in the EDPD Control Register within the MMD address space.

EDPD operation may be adjusted via the p_edpd_mask_timer[1:0], p_edpd_timer[1:0] and p_EDPD_random_dis fields in the EDPD Control Register within the MMD address space.

The energy detection change status can be read from the Interrupt Status Register. The current energy detection status can be read from the EDPD low power bit in the EDPD Control Register.

While the p_edpd_en bit is set, the cable link status will be down, and the energy detection normally monitors pairs A and B for energy. If the link speed is forced to 1000Mbps (by disabling auto-negotiation and setting the speed manually), the energy detection monitors all four pairs. For cable diagnostic purposes, individual wire pairs may be monitored by forcing the link speed to 1000Mbps and selecting the wire pair using the EDPD Wire Pair Selection bits in Analog Control Register 8.

The device's PLL is normally enabled during EDPD. It can be set to be disabled during EDPD by setting the DGT_edpd_pll_dis bit in MMD2 Spare 115 Register.

Normally, previous register setting are maintained when EDPD mode is cleared. With the PLL disabled, a device reset occurs following the removal of EDPD (or if the DGT_edpd_pll_dis bit is cleared during EDPD), in which case register settings will return to their defaults.

APPLICATION NOTE: If the reset is caused by the clearing of the DGT_edpd_pll_dis bit, the p_edpd_en bit will be cleared due to the device reset.

5.24.3 SOFTWARE POWER-DOWN MODE (SPD)

The device supports a software power down (SPD) mode. This mode is used to power down the device when it is not in use after power-up. Software power-down mode is enabled by writing a one to the Power Down bit in the Basic Control Register. The device may also be placed into software power-down by default by setting the **MODE[4:0]** configuration straps to '0100x'. The device exits the SPD state after a zero is written to the Power Down bit.

In the SPD state, the device disables most internal functions.

During SPD, the crystal oscillator and PLL are enabled and the internal (125MHz and 250MHz) clocks are gated, The standard registers (0 through 31) and the MII Management Interface operate using the crystal clock.

Previous register settings are maintained during and following the removal of SPD.

The following remain operational during SPD:

- MII Management Interface
  - Only access to the standard registers (0 through 31) is supported.
  - Access to MMD address spaces other than MMD address space 1 is possible if the spd_clock_gate_override bit is set.
  - Access to MMD address space 1 is not possible.
- Voltage Regulator Controller (LDO)

  - The LDO controller can be disabled by setting the active low LDO enable bit in Analog Control Register 11. An external source of 1.1V is necessary for operation in this case.
- PLL
  - Normally the PLL is enabled during SPD. It may be disabled by setting the spd_pll_disable bit described below.
- Crystal Oscillator
  - Normally the Crystal Oscillator is enabled during SPD. It may be disabled by setting the enXTALb bit described below.
- Bandgap
  - This is always enabled.
- Internal Slow Oscillator
  - This is always enabled.

The following are normally disabled during SPD:

- ADC / PGA / TX / common bias circuits
- DLL
- TX and RX clocks
  - If the above mentioned spd_clock_gate_override bit is set, TX and RX clocks would be enabled. They may alternately be stopped by setting the Isolate (PHY_ISO) bit in the Basic Control Register.
- **CLK125_NDO** pin
  - If the above mentioned spd_clock_gate_override bit is set, **CLK125_NDO** would be enabled (if previously enabled for clock output). It may alternately be disabled by clearing the clk125 Enable bit in Common Control Register.

5.24.3.1 SPD Extra Power Savings

To achieve a lower power usage, the PLL maybe disable during SPD by setting the spd_pll_disable bit in the Digital Debug Control 2 Register prior to entering SPD. The device may also be placed into software power-down with the PLL disabled by default by setting the **MODE[4:0]** configuration straps to '01001'.

With the PLL disabled, a device reset occurs following the removal of SPD (or if the spd_pll_disable bit is cleared during SPD). Register settings will return to their defaults, determined by the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

APPLICATION NOTE: If either the spd_pll_dis_mode or spd_pll_en_mode bits in the Operation Mode Strap Override Low Register are set, the device will return to SPD mode, potentially with the PLL disabled. In order to avoid this logical loop, software should clear the spd_pll_dis_mode and spd_pll_en_mode bits before exiting SPD.

To further reduce power usage, the crystal oscillator maybe disable by setting the enXTALb bit in Analog Control Register 1 after setting the spd_pll_disable bit and entering SPD.

Since the MII Management Interface operates using the crystal clock, once this bit is set, the device will become inaccessible. A pin reset or power cycle is required to resume operation.

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5.25 Wake-On-LAN

Wake-On-LAN (WOL) is normally a MAC-based function to wake up a host system (for example, an Ethernet end device, such as a PC) that is in standby power mode. Wake-up is triggered by receiving and detecting a special packet (commonly referred to as the “magic packet”) that is sent by the remote link partner. The device can perform the same WOL function if the MAC address of its associated MAC device is entered into the device registers for magic-packet detection. When the device detects the magic packet, it wakes up the host by driving its power management event (PME_N) output pin low.

By default, the WOL function is disabled. It is enabled by setting the enabling bit and configuring the associated registers for the selected wake-up detection method.

The device provides four methods to trigger a wake-up:

- Magic-packet detection
- Customized-packet detection
- Link status change detection
- Energy Detection

5.25.1 MAGIC-PACKET DETECTION

The magic packet’s frame format starts with 6 bytes of 0xFFh and is followed by 16 repetitions of the MAC address of its associated MAC device (local MAC device).

When the magic packet is detected from its link partner, the device asserts its PME_N output pin low.

The following MMD Address 2h registers are provided for magic-packet detection:

- Magic-packet detection is enabled by writing a ‘1’ to the En_mpkt_pmen bit in the Wake-On-LAN Control Register (MMD Address 2h, Register 10h, Bit [6]).
- The MAC address (for the local MAC device) is written to and stored in the Wake-On-LAN-MAC-LO Register, Wake-On-LAN-MAC-MI Register and Wake-On-LAN-MAC-HI Register (MMD Address 2h, Registers 11h – 13h).

The device does not generate the magic packet. The magic packet must be provided by the external system.

Magic packet detection status can be read from the Wake-on-LAN Magic Packet Receive Status Register.

Frame preemption reassembly (Section 5.11) is not supported for magic packet detection. The magic packet detection logic will ignore any packet that does not contain the standard SFD.

5.25.2 CUSTOMIZED-PACKET DETECTION

The customized packet has associated register/bit masks to select which byte, or bytes, of the first 64 bytes of the packet to use in the CRC calculation. After the device receives the packet from its link partner, the selected bytes for the received packet are used to calculate the CRC. The calculated CRC is compared to the expected CRC value that was previously written to and stored in the device registers. If there is a match, the device asserts its **PME_N** output pin low.

Four customized packets are provided to support four types of wake-up scenarios. A dedicated set of registers is used to configure and enable each customized packet.

The following MMD registers are provided for customized-packet detection:

- Each of the four customized packets is enabled via the Wake-On-LAN Control Register (MMD Address 2h, Register 10h):
  - Bit [2] // For customized packets, type 0
  - Bit [3] // For customized packets, type 1
  - Bit [4] // For customized packets, type 2
  - Bit [5] // For customized packets, type 3
- 32-bit expected CRCs are written to and stored in:
  - MMD Address 2h, Registers 14h – 15h // For customized packets, type 0
  - MMD Address 2h, Registers 16h – 17h // For customized packets, type 1
  - MMD Address 2h, Registers 18h – 19h // For customized packets, type 2
  - MMD Address 2h, Registers 1Ah – 1Bh // For customized packets, type 3
- Masks to indicate which of the first 64-bytes to use in the CRC calculation are set in:
  - MMD Address 2h, Registers 1Ch – 1Fh // For customized packets, type 0
  - MMD Address 2h, Registers 20h – 23h // For customized packets, type 1

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- MMD Address 2h, Registers 24h – 27h // For customized packets, type 2
- MMD Address 2h, Registers 28h – 2Bh // For customized packets, type 3

Customized packet detection status can be read from the Wake-on-LAN Custom Packet Receive Status Register.

Frame preemption reassembly (Section 5.11) is not supported for customized packet detection. The customized packet detection logic will ignore any packet that does not contain the standard SFD.

5.25.3 LINK STATUS CHANGE DETECTION

If link status change detection is enabled, the device asserts its **PME_N** output pin low whenever there is a link status change using the following bits in the Wake-On-LAN Control Register (MMD Address 2h, Register 10h):

- Bit [0] - En_link_up_pmen // For link-up detection
- Bit [1] - En_link_dn_pmen // For link-down detection

The link change status can be read from the Interrupt Status Register. The current link status can be read from the Basic Status Register.

Note:	Clearing the link change status by reading the Interrupt Status Register DOES NOT clear the link status change detection that asserts **PME_N**. In order to clear the **PME_N** indication, the En_link_up_pmen and/or En_link_dn_pmen control bits must be cleared.

5.25.4 ENERGY STATUS CHANGE DETECTION

During Energy Detect Power Down (Section 5.24.2) if the energy status change detection is enabled, the device asserts its **PME_N** output pin low whenever there is an energy detection status change using the following bits in the Wake-On-LAN Control Register (MMD Address 2h, Register 10h):

- Bit [11] - En_energy_detect_pmen // For energy detected
- Bit [12] - En_energy_off_pmen // For energy not detected

The energy detection change status can be read from the Interrupt Status Register. The current energy detection status can be read from the EDPD low power bit in the Analog Control Register 8.

5.25.5 PME_N OUTPUT SIGNAL

The **PME_N** output signal may be mapped to any enabled GPIO (including but not limited to **INT_N** and **LED1**) by setting the corresponding bits in the General Purpose IO Data Select 1 Register (GPIO_DATA_SEL1) or the General Purpose IO Data Select 2 Register (GPIO_DATA_SEL2).The GPIO needs to be enabled and its direction set as an output via the General Purpose IO Enable Register (**GPIO_EN**) and the General Purpose IO Direction Register (GPIO_DIR).

The PME buffer type is selectable between open-drain and push-pull and is configured by the GPIO Buffer Type (GPIO_BUF) field in the General Purpose IO Buffer Type Register (GPIO_BUF). The default is open-drain.

The PME Polarity bit in the Output Control Register sets the **PME_N** level to active high or active low. The default is active low.

The Pmen_out field in the Wake-On-LAN Control Register (MMD Address 2h, Register 10h, Bits [15:14]) defines the output functions for PME.

When asserted, the **PME_N** output is de-asserted by disabling the register bit that enabled the PME trigger source (magic packet, customized packet, link status change, energy detect status change).

5.26 NAND Tree Support

The device provides parametric NAND tree support for fault detection between chip I/Os and board. NAND tree mode is enabled at power-up/reset with the **MODE**[4:0] strap-in pins set to ‘00100’.

The NAND tree consists of a series chain of NAND gates with each input pin NANDed with the output of the previous NAND. Table 5-17 lists the NAND tree pin order. Input (1) is the start of the tree and is NANDed with a constant “1”.

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TABLE 5-17: NAND TREE TEST PIN ORDER

Pin	Description
LED5	Input
LED4	Input
LED3	Input
LED2	Input
LED1	Input
TXD0	Input
TXD1	Input
TXD2	Input
TXD3	Input
TXD4	Input
TXD5	Input
TXD6	Input
TXD7	Input
TX_ER	Input
GTX_CLK	Input
TX_EN	Input
RXD7	Input
RXD6	Input
RXD5	Input
RXD4	Input
RXD3	Input
RXD2	Input
RXD1	Input
RXD0	Input
RX_DV	Input
RX_ER	Input
RX_CLK	Input
CRS	Input
COL	Input
INT_N	Input
MDC	Input
MDIO	Input
TX_CLK	Input
CLK125_NDO	Output

To test any given pin, the pin is toggled while holding the lower ranked pins low and the higher ranked pins high. Depending on the position in the chain (odd or even), the output of the tree will reflect the tested input pin or its inverse (odd positions are inverted with respect to the output pin).

APPLICATION NOTE: Since the NAND tree output is on the **CLK125_NDO** pin, the pin must be enabled for output by using the **CLK125_EN** strap input.

5.27 PHY Resets

5.27.1 SOFTWARE RESET

The Gigabit Ethernet PHY may be reset by software by using the IEEE 802.3 standard PHY Soft Reset (**RESET**) bit in the Basic Control Register. This resets all the PHY and all its registers to their default state, with the following exceptions.

- The Variable IO are not re-tuned
  (but IO Pad Tune Control Register (**IO_TUNE_CTRL**) is reset)
- The RGMII DLLs are not re-tuned
  (but RX DLL Control Register and TX DLL Control Register are reset)
- The crystal oscillator amplitude and termination resistor are not re-trimmed
- Input straps are not re-loaded from the pins
  The Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register are not reset
  (Registers that default based on the input straps or on the override registers are reset)
- Analog Control Register 1, Analog Control Register 2, Analog Control Register 9, Analog Control Register 10, Analog Control Register 11, Analog Control Register 12 and Analog Control Register 13 are not reset
  (these may be reset with the AFE Soft Reset bit in the Digital Debug Control 2 Register)

An additional software reset is available by using the bit Software Reset bit in the Control Register. This resets all of the PHY except for its registers.

5.27.2 PHY POWER ON READY

Four voltages are monitored.

+1.1V Analog Power Supply (on **VDDAL**) set for ~0.8V (typical)

+1.1V Digital Core Power Supply (on **VDD**) set for ~0.9V (typical)

+2.5 / 3.3V Analog Power Supply (on **VDDAH**) set for ~2.1V (typical)

Variable I/O Power Supply (on **VDDIO**) set for ~1.5V (typical)

See Table 6-16, "POR Thresholds" for the D.C. characteristics of POR.

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6.0 OPERATIONAL CHARACTERISTICS

6.1 Absolute Maximum Ratings*

Supply Voltage (**VDDAL**, **VDDAL_PLL**, **VDD**) (Note 6-1) ..... –0.5V to +1.25V

Supply Voltage (**VDDAH**, **VDDIO**) (Note 6-1) ..... –0.5V to +3.63V

Input Voltage (all inputs) ..... –0.5V to +3.63V

Output Voltage (all outputs) ..... –0.5V to +3.63V

Storage Temperature (T_S) ..... -55°C to +150°C

Lead Temperature (soldering, 10s) ..... +260°C

Maximum Junction Temperature (T_J) ..... +125°C

HBM ESD Performance ..... +/-6kV

Note 6-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 6.2, "Operating Conditions**", Section 6.5, "DC Specifications", or any other applicable section of this specification is not implied.

6.2 Operating Conditions**

Supply Voltage (**VDDAL**, **VDDAL_PLL**, **VDD**) ..... +1.067V to +1.21V

Supply Voltage (**VDDAH** @ 3.3V) ..... +3.135 V to +3.63 V

Supply Voltage (**VDDAH** @ 2.5V) ..... +2.375 V to +2.75 V

Supply Voltage (**VDDIO** @ 3.3V) ..... +3.135 V to +3.63 V

Supply Voltage (**VDDIO** @ 2.5V) ..... +2.375 V to +2.75 V

Supply Voltage (**VDDIO** @ 1.8V) ..... +1.71 V to +1.98 V

Input voltage (all inputs) ..... –0.3 V to +3.63 V

Output voltage (all outputs) ..... –0.3 V to +3.63 V

Ambient Operating Temperature in Still Air (T_A) ..... Note 6-2

**The device is not guaranteed to function outside its operating ratings.

Note 6-2 Commercial (0°C to +70°C)
Extended Industrial (-40°C to +105°C)

Note:	Do not drive input signals without power supplied to the device.

6.3 Power Consumption

This section details the device power measurements taken over various operating conditions. Unless otherwise noted, all measurements were taken with power supplies at nominal values. Refer to Section 5.24, Power Management for a description of the power down modes.

The LAN8841 power consumption measurements are organized as follows:

- RGMII Power Consumption Summary
- GMII/MII Power Consumption Summary
- Section 6.3.1, PHY Power Consumption In RGMII Mode
  - Table 6-3, "Typical Current/Power Consumption - RGMII - Digital I/O (3.3V), Transceiver (3.3V)"
  - Table 6-4, "Typical Current/Power Consumption - RGMII - Digital I/O (2.5V), Transceiver (3.3V)"
  - Table 6-5, "Typical Current/Power Consumption - RGMII - Digital I/O (2.5V), Transceiver (2.5V)"
  - Table 6-6, "Typical Current/Power Consumption - RGMII - Digital I/O (1.8V), Transceiver (2.5V)"
- Section 6.3.2, "PHY Power Consumption in GMII/MII Mode"
  - Table 6-7, "Typical Current/Power Consumption - GMII/MII - Digital I/O (3.3V), Transceiver (3.3V)"
  - Table 6-8, "Typical Current/Power Consumption - GMII/MII - Digital I/O (2.5V), Transceiver (3.3V)"
  - Table 6-9, "Typical Current/Power Consumption - GMII/MII - Digital I/O (2.5V), Transceiver (2.5V)"
  - Table 6-10, "Typical Current/Power Consumption - GMII/MII - Digital I/O (1.8V), Transceiver (2.5V)"
  -

TABLE 6-1: RGMII POWER CONSUMPTION SUMMARY

Mode	Typical Power (mW) VDDIO = 3.3V VDDAH = 3.3V	Typical Power (mW) VDDIO = 2.5V VDDAH = 2.5V
1000BASE-T Link-Up (no traffic)	539	411
1000BASE-T Full-Duplex at 100% Utilization	583	434.5
100BASE-TX Link-Up (no traffic)	256.3	175
100BASE-TX Full-Duplex at 100% Utilization	276.1	185
10BASE-T Link-Up (no traffic)	106.7	66
10BASE-T Full-Duplex at 100% Utilization	169.4	108.5
10BASE-Te Link-Up (no traffic)	106.7	66
10BASE-Te Full-Duplex at 100% Utilization	156.2	96
EEE Mode - 1000 Mbps	343.2	218
EEE Mode - 100 Mbps	193.6	122
Energy Detect Power Down	63.8	43.5
Normal Operation (No Link)	116.6	83.5
HW Reset	42.9	25
Software Power Down	29.7	20
Software Power Down (Extra Savings)	9.9	7.5
Max Power (105° with VDDAH/VDDIO + 10%)	732	613

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TABLE 6-2: GMII/MII POWER CONSUMPTION SUMMARY

Mode	Typical Power (mW) VDDIO = 3.3V VDDAH = 3.3V	Typical Power (mW) VDDIO = 2.5V VDDAH = 2.5V
1000BASE-T Link-Up (no traffic)	539	411
1000BASE-T Full-Duplex at 100% Utilization	596.2	444.5
100BASE-TX Link-Up (no traffic)	256.3	175
100BASE-TX Full-Duplex at 100% Utilization	282.7	187.5
10BASE-T Link-Up (no traffic)	110	68.5
10BASE-T Full-Duplex at 100% Utilization	169.4	108.5
10BASE-Te Link-Up (no traffic)	156.2	66
10BASE-Te Full-Duplex at 100% Utilization	93.5	96
EEE Mode - 1000 Mbps	112.2	188
EEE Mode - 100 Mbps	414.7	127
Energy Detect Power Down	73.7	43.5
Normal Operation (No Link)	159.5	96
HW Reset	42.9	25
Software Power Down	36.3	20
Software Power Down (Extra Savings)	9.9	7.5
Max Power (105° with VDDAH/VDDIO + 10%)	732	613

6.3.1 PHY POWER CONSUMPTION IN RGMII MODE

TABLE 6-3: TYPICAL CURRENT/POWER CONSUMPTION - RGMII - DIGITAL I/O (3.3V), TRANSCEIVER (3.3V)

Condition	1.1V Core (VDD, VDDAL, VDDAL_PLL) (mA)	3.3V Digital I/O (VDDIO) (mA) Note 6-3	3.3V Transceiver (VDDAH) (mA)	Total Chip Power (mW)
1000BASE-T Link-Up (no traffic)	160	22	88	539
1000BASE-T Full-Duplex at 100% Utilization	170	32	88	583
100BASE-TX Link-Up (no traffic)	50	19	42	256.3
100BASE-TX Full-Duplex at 100% Utilization	50	25	42	276.1
10BASE-T Link-Up (no traffic)	10	9	20	106.7
10BASE-T Full-Duplex at 100% Utilization	10	18	30	169.4
10BASE-Te Link-Up (no traffic)	10	9	20	106.7
10BASE-Te Full-Duplex at 100% Utilization	10	18	26	156.2
EEE Mode – 1000 Mbps	30	35	59	343.2
EEE Mode – 100 Mbps (TX and RX in LPI)	20	19	33	193.6
Energy Detect Power Down	10	7	9	63.8
Normal Operation (No Link)	10	12	20	116.6
HW Reset	0	4	9	42.9
Software Power Down	0	1	8	29.7
Software Power Down (Extra Savings)	0	1	2	9.9

Note 6-3 Current sourced to LEDs and GPIOs is not included in these values.

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TABLE 6-4: TYPICAL CURRENT/POWER CONSUMPTION - RGMII - DIGITAL I/O (2.5V), TRANSCEIVER (3.3V)

Condition	1.1V Core (VDD, VDDAL, VDDAL_PLL) (mA)	2.5V Digital I/O (VDDIO) (mA) Note 6-4	3.3V Transceiver (VDDAH) (mA)	Total Chip Power (mW)
1000BASE-T Link-Up (no traffic)	160	13	88	498.9
1000BASE-T Full-Duplex at 100% Utilization	170	19	88	524.9
100BASE-TX Link-Up (no traffic)	50	10	42	218.6
100BASE-TX Full-Duplex at 100% Utilization	50	14	42	228.6
10BASE-T Link-Up (no traffic)	10	4	20	87
10BASE-T Full-Duplex at 100% Utilization	10	9	31	135.8
10BASE-Te Link-Up (no traffic)	10	4	20	87
10BASE-Te Full-Duplex at 100% Utilization	10	9	26	119.3
EEE Mode – 1000 Mbps	30	22	59	282.7
EEE Mode – 100 Mbps (TX and RX in LPI)	20	10	33	155.9
Energy Detect Power Down	10	5	9	53.2
Normal Operation (No Link)	10	9	20	99.5
HW Reset	0	2	9	34.7
Software Power Down	0	1	8	28.9
Software Power Down (Extra Savings)	0	1	2	9.1

Note 6-4 Current sourced to LEDs and GPIOs is not included in these values.

TABLE 6-5: TYPICAL CURRENT/POWER CONSUMPTION - RGMII - DIGITAL I/O (2.5V), TRANSCEIVER (2.5V)

Condition	1.1V Core (VDD, VDDAL, VDDAL_PLL) (mA)	2.5V Digital I/O (VDDIO) (mA) Note 6-5	2.5V Transceiver (VDDAH) (mA)	Total Chip Power (mW)
1000BASE-T Link-Up (no traffic)	160	13	81	411
1000BASE-T Full-Duplex at 100% Utilization	170	19	80	434.5
100BASE-TX Link-Up (no traffic)	50	10	38	175
100BASE-TX Full-Duplex at 100% Utilization	50	14	38	185
10BASE-T Link-Up (no traffic)	10	4	18	66
10BASE-T Full-Duplex at 100% Utilization	10	9	30	108.5
10BASE-Te Link-Up (no traffic)	10	4	18	66
10BASE-Te Full-Duplex at 100% Utilization	10	9	25	96
EEE Mode – 1000 Mbps	30	22	52	218
EEE Mode – 100 Mbps (TX and RX in LPI)	20	10	30	122
Energy Detect Power Down	10	5	8	43.5
Normal Operation (No Link)	10	9	20	83.5
HW Reset	0	2	8	25
Software Power Down	0	1	7	20
Software Power Down (Extra Savings)	0	1	2	7.5

Note 6-5 Current sourced to LEDs and GPIOs is not included in these values.

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TABLE 6-6: TYPICAL CURRENT/POWER CONSUMPTION - RGMII - DIGITAL I/O (1.8V), TRANSCEIVER (2.5V)

Condition	1.1V Core (VDD, VDDAL, VDDAL_PLL) (mA)	1.8V Digital I/O (VDDIO) (mA) Note 6-5	2.5V Transceiver (VDDAH) (mA)	Total Chip Power (mW)
1000BASE-T Link-Up (no traffic)	160	6	81	389.3
1000BASE-T Full-Duplex at 100% Utilization	170	8	80	401.4
100BASE-TX Link-Up (no traffic)	50	4	38	157.2
100BASE-TX Full-Duplex at 100% Utilization	50	5	38	159
10BASE-T Link-Up (no traffic)	10	1	18	57.8
10BASE-T Full-Duplex at 100% Utilization	10	3	30	91.4
10BASE-Te Link-Up (no traffic)	10	1	18	57.8
10BASE-Te Full-Duplex at 100% Utilization	10	3	25	78.9
EEE Mode – 1000 Mbps	30	12	52	184.6
EEE Mode – 100 Mbps (TX and RX in LPI)	20	4	30	104.2
Energy Detect Power Down	10	3	8	36.4
Normal Operation (No Link)	10	7	19	71.1
HW Reset	0	0	8	20
Software Power Down	0	0	7	17.5
Software Power Down (Extra Savings)	0	1	2	6.8

Note 6-6 Current sourced to LEDs and GPIOs is not included in these values.

6.3.2 PHY POWER CONSUMPTION IN GMII/MII MODE

TABLE 6-7: TYPICAL CURRENT/POWER CONSUMPTION - GMII/MII - DIGITAL I/O (3.3V), TRANSCEIVER (3.3V)

Condition	1.1V Core (VDD, VDDAL, VDDAL_PLL) (mA)	3.3V Digital I/O (VDDIO) (mA) Note 6-7	3.3V Transceiver (VDDAH) (mA)	Total Chip Power (mW)
1000BASE-T Link-Up (no traffic)	160	22	88	539
1000BASE-T Full-Duplex at 100% Utilization	170	36	88	596.2
100BASE-TX Link-Up (no traffic)	50	19	42	256.3
100BASE-TX Full-Duplex at 100% Utilization	50	27	42	282.7
10BASE-T Link-Up (no traffic)	10	10	20	110
10BASE-T Full-Duplex at 100% Utilization	10	18	30	169.4
10BASE-Te Link-Up (no traffic)	10	18	26	156.2
10BASE-Te Full-Duplex at 100% Utilization	10	5	20	93.5
EEE Mode – 1000 Mbps	30	4	20	112.2
EEE Mode – 100 Mbps (TX and RX in LPI)	20	31	88	414.7
Energy Detect Power Down	10	10	9	73.7
Normal Operation (No Link)	10	25	20	159.5
HW Reset	0	4	9	42.9
Software Power Down	0	3	8	36.3
Software Power Down (Extra Savings)	0	1	2	9.9

Note 6-7 Current sourced to LEDs and GPIOs is not included in these values.

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TABLE 6-8: TYPICAL CURRENT/POWER CONSUMPTION - GMII/MII - DIGITAL I/O (2.5V), TRANSCEIVER (3.3V)

Condition	1.1V Core (VDD, VDDAL, VDDAL_PLL) (mA)	2.5V Digital I/O (VDDIO) (mA) Note 6-8	3.3V Transceiver (VDDAH) (mA)	Total Chip Power (mW)
1000BASE-T Link-Up (no traffic)	160	13	88	498.9
1000BASE-T Full-Duplex at 100% Utilization	170	22	88	532.4
100BASE-TX Link-Up (no traffic)	50	10	42	218.6
100BASE-TX Full-Duplex at 100% Utilization	50	15	42	231.1
10BASE-T Link-Up (no traffic)	10	5	20	89.5
10BASE-T Full-Duplex at 100% Utilization	10	9	31	135.8
10BASE-Te Link-Up (no traffic)	10	4	20	87
10BASE-Te Full-Duplex at 100% Utilization	10	9	26	119.3
EEE Mode – 1000 Mbps	30	10	59	252.7
EEE Mode – 100 Mbps (TX and RX in LPI)	20	12	34	164.2
Energy Detect Power Down	10	5	9	53.2
Normal Operation (No Link)	10	16	20	117
HW Reset	0	2	9	34.7
Software Power Down	0	1	8	28.9
Software Power Down (Extra Savings)	0	1	2	9.1

Note 6-8 Current sourced to LEDs and GPIOs is not included in these values.

TABLE 6-9: TYPICAL CURRENT/POWER CONSUMPTION - GMII/MII - DIGITAL I/O (2.5V), TRANSCEIVER (2.5V)

Condition	1.1V Core (VDD, VDDAL, VDDAL_PLL) (mA)	2.5V Digital I/O (VDDIO) (mA) Note 6-9	2.5V Transceiver (VDDAH) (mA)	Total Chip Power (mW)
1000BASE-T Link-Up (no traffic)	160	13	81	411
1000BASE-T Full-Duplex at 100% Utilization	170	22	81	444.5
100BASE-TX Link-Up (no traffic)	50	10	38	175
100BASE-TX Full-Duplex at 100% Utilization	50	15	38	187.5
10BASE-T Link-Up (no traffic)	10	5	18	68.5
10BASE-T Full-Duplex at 100% Utilization	10	9	30	108.5
10BASE-Te Link-Up (no traffic)	10	4	18	66
10BASE-Te Full-Duplex at 100% Utilization	10	9	25	96
EEE Mode – 1000 Mbps	30	10	52	188
EEE Mode – 100 Mbps (TX and RX in LPI)	20	12	30	127
Energy Detect Power Down	10	5	8	43.5
Normal Operation (No Link)	10	16	18	96
HW Reset	0	2	8	25
Software Power Down	0	1	7	20
Software Power Down (Extra Savings)	0	1	2	7.5

Note 6-9 Current sourced to LEDs and GPIOs is not included in these values.

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TABLE 6-10: TYPICAL CURRENT/POWER CONSUMPTION - GMII/MII - DIGITAL I/O (1.8V), TRANSCEIVER (2.5V)

Condition	1.1V Core (VDD, VDDAL, VDDAL_PLL) (mA)	1.8V Digital I/O (VDDIO) (mA) Note 6-10	2.5V Transceiver (VDDAH) (mA)	Total Chip Power (mW)
1000BASE-T Link-Up (no traffic)	160	6	81	389.3
1000BASE-T Full-Duplex at 100% Utilization	170	10	81	407.5
100BASE-TX Link-Up (no traffic)	50	4	38	157.2
100BASE-TX Full-Duplex at 100% Utilization	50	6	38	160.8
10BASE-T Link-Up (no traffic)	10	1	18	57.8
10BASE-T Full-Duplex at 100% Utilization	10	3	30	91.4
10BASE-Te Link-Up (no traffic)	10	1	18	57.8
10BASE-Te Full-Duplex at 100% Utilization	10	3	25	78.9
EEE Mode – 1000 Mbps	30	5	52	172
EEE Mode – 100 Mbps (TX and RX in LPI)	20	5	30	106
Energy Detect Power Down	10	2	8	34.6
Normal Operation (No Link)	10	9	18	72.2
HW Reset	0	0	8	20
Software Power Down	0	1	7	19.3
Software Power Down (Extra Savings)	0	1	2	6.8

Note 6-10 Current sourced to LEDs and GPIOs is not included in these values.

6.4 Package Thermal Specifications

Thermal parameters are measured or estimated for devices with the ground soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air. The values provided are based on the package body, die size, and maximum power consumption.

TABLE 6-11: PACKAGE THERMAL PARAMETERS

Parameter	Symbol	Value	Units	Notes
Junction-to-Ambient	Θ_{JA}	25	°C/W	0 Meters/second
		20	°C/W	1 Meters/second
		19	°C/W	2.5 Meters/second
Junction-to-Top-of-Package	Ψ_{JT}	0.1	°C/W	0 Meters/second
Junction-to-Case	Θ_{JC}	8	°C/W	0 Meters/second
Junction-to-Board	Θ_{JB}	9	°C/W	-

Use the following formulas to calculate the junction temperature:

$$T_J = P \times \Theta_{JA} + T_A$$

$$T_J = P \times \Psi_{JT} + T_T$$

$$T_J = P \times \Theta_{JC} + T_C$$

TABLE 6-12: PACKAGE THERMALS LEGEND

Symbol	Description
T_J	Junction temperature
P	Power dissipated
Θ_{JA}	Junction-to-ambient-temperature
Θ_{JC}	Junction-to-top-of-package
Ψ_{JT}	Junction-to-bottom-of-case
T_A	Ambient temperature
T_C	Temperature of the bottom of the case
T_T	Temperature of the top of the case

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6.5 DC Specifications

TABLE 6-13: NON-VARIABLE I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
ICLK Type Input Buffer						Note 6-11
Low Input Level	V_{IL}			0.5	V	
High Input Level	V_{IH}	2.0			V	
Input Leakage	I_{IH}	-10		10	µA	

Note 6-11 **XI** can optionally be driven from a 25 MHz single-ended clock oscillator to which these specifications apply.

TABLE 6-14: VARIABLE I/O DC ELECTRICAL CHARACTERISTICS VDDIO = 1.8/2.5/3.3V

Parameter	Symbol	Min	Typ (1.8/2.5/3.3V)	Max	Units	Notes
VIS Type Input Buffer						
Low Input Level	V_{IL}			0.39x**VDDIO**	V	
High Input Level	V_{IH}	0.63x**VDDIO**			V	
Schmitt Falling Trip Point	V_{T-}	0.67	0.8/1.1/1.46	1.68	V	
Schmitt Rising Trip Point	V_{T+}	0.8	0.94/1.25/1.62	1.85	V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	109.9	149/148/164	219.4	mV	
Input Leakage (V_{IN} = **P_VSS** or **VDDIO**)	I_{IH}	-10		10	µA	Note 6-12
Input Capacitance	C_{IN}			3	pF	
Effective Pull-Up Resistance (V_{IN} = **P_VSS**)	R_{PU}	58.9	70	83.7	KΩ	
Effective Pull-Down Resistance (V_{IN} = **VDDIO**)	R_{PD}	58.7	70	84.5	KΩ	
VO5 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = -5 mA
High Output Level	V_{OH}	**VDDIO**-0.4			V	I_{OH} = 5 mA
Output Tri-State Leakage	I_{OZ}	-10		10	µA	Note 6-12

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TABLE 6-14: VARIABLE I/O DC ELECTRICAL CHARACTERISTICS VDDIO = 1.8/2.5/3.3V

Parameter	Symbol	Min	Typ (1.8/2.5/3.3V)	Max	Units	Notes
VO10 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = -10 mA
High Output Level	V_{OH}	**VDDIO**-0.4			V	I_{OH} = 10 mA
Output Tri-State Leakage	I_{OZ}	-10		10	µA	Note 6-12
VOD10 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = -10 mA
Output Tri-State Leakage	I_{OZ}	-10		10	µA	Note 6-12
VOS10 Type Buffer						
High Output Level	V_{OH}	**VDDIO**-0.4			V	I_{OH} = 10 mA
Output Tri-State Leakage	I_{OZ}	-10		10	µA	Note 6-12
RGMII Type Input Buffer						
Low Input Level	V_{IL}			0.4x**VDDIO**	V	
High Input Level	V_{IH}	0.6x**VDDIO**			V	
Schmitt Falling Trip Point	V_{T-}	0.76	0.90/1.11/1.42	1.64	V	
Schmitt Rising Trip Point	V_{T+}	0.85	0.99/1.23/1.55	1.76	V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	60	90/121/127	150	mV	
Input Leakage (V_{IN} = **P_VSS** or **VDDIO**)	I_{IH}	-15		15	µA	
Input Capacitance	C_{IN}			3	pF	
RGMII Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = -5 mA
High Output Level	V_{OH}	**VDDIO**-0.4			V	I_{OH} = 5 mA
Output Impedance	R_O		50/50/50		Ω	

Note 6-12 This specification applies to all inputs without pull-ups or pull-downs and three-stated bi-directional pins.

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TABLE 6-15: LDO CONTROLLER

Parameter	Symbol	Min	Typ	Max	Units	Notes
Output drive range for **LDO_O** to gate input of P-channel MOSFET	V_{LDO_O}	2.0		3.1[1]	V	**VDDAH** = 3.3V (-5%/+10%) for MOSFET source voltage
		1.0		2.0[1]	V	**VDDAH** = 2.5V (-5%/+10%) for MOSFET source voltage
Output of P-channel MOSFET		1.067		1.21	V	[2]

1: Value when **LDO** is enabled. V_{LDO_O} maximum may be as high as **VDDAH** when **LDO** is disabled.

2: Output is 1.067V-1.21V with default **LDO** tune of 001 in Analog Control Register 11. Please see LAN8841 Errata for more information.

Note: A capacitor between core voltage and ground is required to meet the parameters in this table. See Section 4.1.1 for details.

TABLE 6-16: POR THRESHOLDS

POR	Conditions	Rising threshold volts			Falling threshold volts			Hysteresis millivolts		
		min	typ	max	min	typ	max	min	typ	max
1.1V Ethernet PHY Analog (**VDDAL**)	**VDDAH** = 2.5V	0.73	0.76	0.80	0.64	0.68	0.80	0	80	114
	VDDAH = 3.3V	0.73	0.76	0.82	0.63	0.70	0.82	0	65	120
2.5V / 3.3V Ethernet PHY Analog (**VDDAH**)		1.9	2.1	2.2	1.8	2.0	2.1	65	110	145
1.1V Digital Core (**VDD**)	**VDDIO** = 1.8V Rise/Fall = 10uS	0.913	0.929	0.948	0.65	0.68	0.706	0.217	0.248	0.295
	VDDIO = 1.8V Rise/Fall = 10mS	0.853	0.862	0.876	0.737	0.749	0.758	0.107	0.112	0.122
	VDDIO = 2.5V Rise/Fall = 10uS	0.916	0.933	0.954	0.644	0.677	0.704	0.221	0.256	0.308
	VDDIO = 2.5V Rise/Fall = 10mS	0.853	0.862	0.877	0.737	0.749	0.757	0.107	0.112	0.123
	VDDIO =3.3V Rise/Fall = 10uS	0.918	0.937	0.962	0.638	0.672	0.701	0.226	0.265	0.322
	VDDIO =3.3V Rise/Fall = 10mS	0.853	0.862	0.877	0.737	0.749	0.757	0.107	0.112	0.123
3.3V / 2.5V / 1.8V Variable I/O (**VDDIO**)	**VDDIO** = 1.8V Rise/Fall = 10uS	1.62	1.8	1.98	0.815	0.997	1.167	0.453	0.802	1.164
	VDDIO = 1.8V Rise/Fall = 10mS	1.454	1.47	1.491	1.218	1.231	1.262	0.212	0.238	0.243
	VDDIO = 2.5V Rise/Fall = 10uS	2.02	2.17	2.67	0.8	0.986	1.159	0.88	1.183	1.81
	VDDIO = 2.5V Rise/Fall = 10mS	1.454	1.47	1.491	1.216	1.23	1.261	0.213	0.240	0.245
	VDDIO =3.3V Rise/Fall = 10uS	2.15	2.34	3.0	0.645	0.973	1.152	1.0	1.373	2.16
	VDDIO =3.3V Rise/Fall = 10mS	1.455	1.47	1.491	1.215	1.228	1.26	0.214	0.242	0.247

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6.6 AC Specifications

This section details the various AC timing specifications of the device.

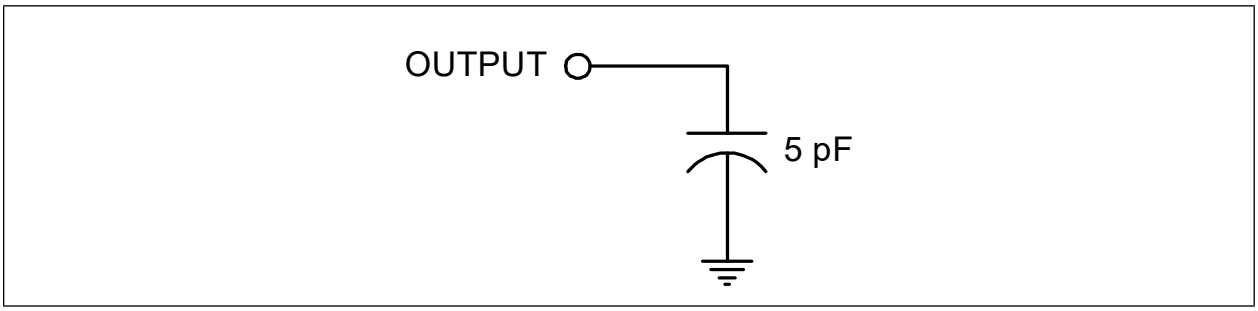
Note:	The GMII/MII timing adheres to or exceeds the IEEE 802.3 specification. Refer to the IEEE 802.3 specification for additional GMII/MII timing information.

Note:	The RGMII timing adheres to or exceeds the HP RGMII Specification Version 2.0. Refer to this specification for additional RGMII timing information.

6.6.1 EQUIVALENT TEST LOAD

Output timing specifications assume a 5pF equivalent test load, unless otherwise noted, as illustrated in Figure 6-1.

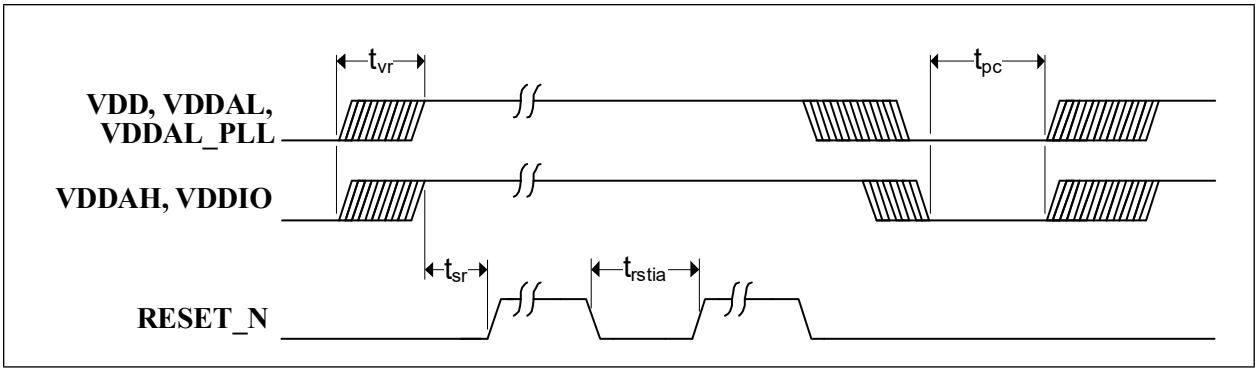
FIGURE 6-1: OUTPUT EQUIVALENT TEST LOAD



6.6.2 POWER SEQUENCE TIMING

These diagrams illustrates the device power sequencing requirements.

FIGURE 6-2: POWER SEQUENCE TIMING



The recommended power-up sequence is to have the transceiver (**VDDAH**) and digital I/O (**VDDIO**) voltages power up before the 1.1V core (**VDD**, **VDDAL**, **VDDAL_PLL**) voltage. If the 1.1V core must power up first, the maximum lead time for the 1.1V core voltage with respect to the transceiver and digital I/O voltages should be 200 µs.

There is no power sequence requirement between transceiver (**VDDAH**) and digital I/O (**VDDIO**) power rails.

The power-up waveforms must be monotonic for all supply voltages to the device.

RESET_N must be held asserted following stable voltages for the minimum period specified and if re-asserted, for the minimum period specified.

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The recommended power-down sequence is to have the 1.1V core voltage power-down before powering down the transceiver and digital I/O voltages.

Before the next power-up cycle, all supply voltages to the device should reach less than 0.4V and there should be a minimum wait time of 150 ms from power-off to power-on.

TABLE 6-17: POWER SEQUENCING TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{vr}	Supply voltages rise time (must be monotonic)			200	µs
t_{sr}	Stable supply voltages to de-assertion of reset	10			ms
t_{rstia}	**RESET_N** input assertion time	1			µs
t_{pc}	Supply voltages cycle off-to-on time	150			ms

6.6.3 RESET PIN CONFIGURATION STRAP TIMING

Figure 6-3 illustrates the **RESET_N** timing requirements and its relation to the configuration straps. **RESET_N** must be asserted for the minimum period specified.

FIGURE 6-3: RESET_N CONFIGURATION STRAP TIMING

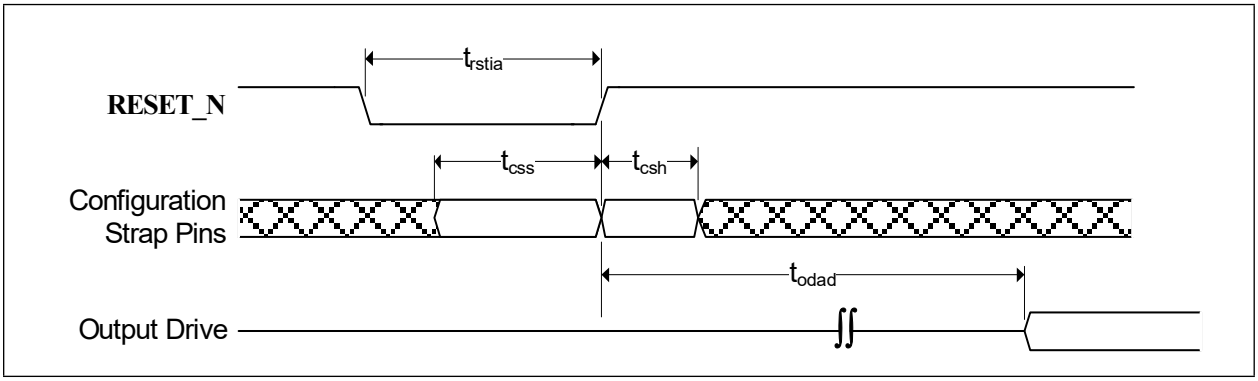

TABLE 6-18: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	1			µs
t_{css}	Configuration strap setup before **RESET_N** de-assertion	5			ns
t_{csh}	Configuration strap hold after **RESET_N** de-assertion	5			ns
t_{odad}	Output drive after **RESET_N** de-assertion	150			ns

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6.6.4 GMII TIMING (1000BASE-T)

This section specifies the GMII interface transmit and receive timing.

Note:	All GMII timing specifications assume a point-to-point test circuit as defined in Section 35.4.2.2 of the IEEE 802.3-2005 specification.

Note:	The below timing parameters assume default values for the following registers: Clock Invert and Control Signal Pad Skew Register RGMII RX Data Pad Skew Register RGMII TX Data Pad Skew Register Clock Pad Skew Register.

FIGURE 6-4: GMII TRANSMIT TIMING

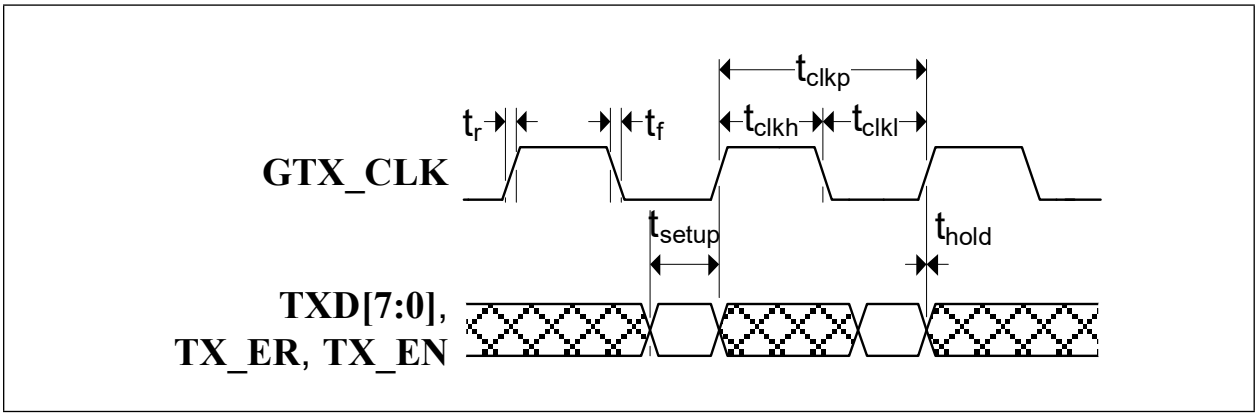

TABLE 6-19: GMII TRANSMIT TIMING VALUES

Symbol	Description	Min	Max	Units	Notes
f_{gtxclk}	**GTX_CLK** Frequency	125 - 100ppm	125 + 100ppm	MHz	
t_{clkp}	**GTX_CLK** period	7.5	8.5	ns	Note 6-13
t_{clkh}	**GTX_CLK** high time	2.5		ns	
t_{clkl}	**GTX_CLK** low time	2.5		ns	
t_{setup}	**TXD[7:0]**, **TX_EN**, **TX_ER** setup to rising edge of **GTX_CLK**	2.0		ns	Note 6-14
t_{hold}	**TXD[7:0]**, **TX_EN**, **TX_ER** hold time from rising edge of **GTX_CLK**	0		ns	Note 6-14
t_r	**GTX_CLK** rise time		1	ns	Note 6-15
t_f	**GTX_CLK** fall time		1	ns	Note 6-15

Note 6-13 Min/max limits are non-sustainable long term.

Note 6-14 These values match the IEEE specification.

Note 6-15 t_r and t_f are measured from $V_{IL\_AC(Max)}$=0.7V to $V_{IH\_AC(Min)}$=1.9V.

FIGURE 6-5: GMII RECEIVE TIMING

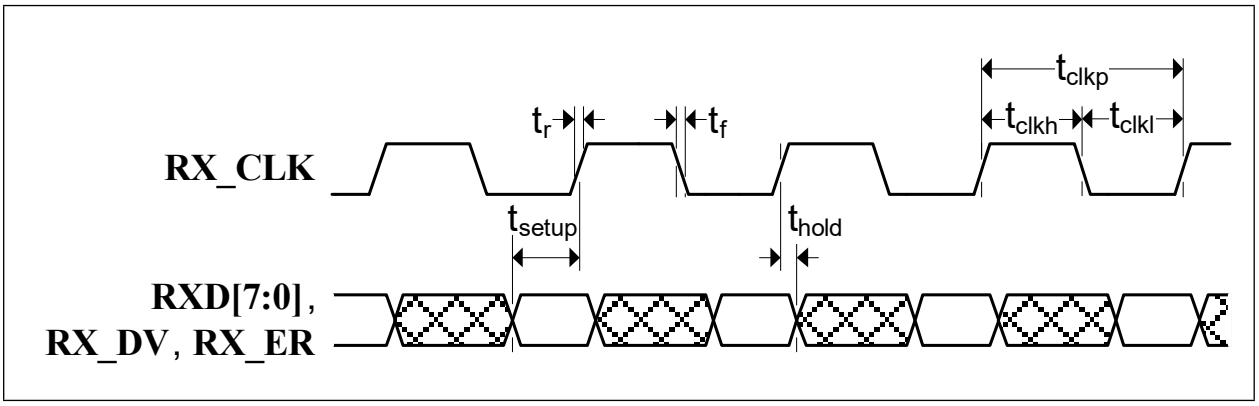

TABLE 6-20: GMII RECEIVE TIMING VALUES

Symbol	Description	Min	Max	Units	Notes
t_{clkp}	**RX_CLK** period	7.5		ns	Note 6-16
t_{clkh}	**RX_CLK** high time	2.5		ns	
t_{clkl}	**RX_CLK** low time	2.5		ns	
t_{setup}	**RXD[7:0]**, **RX_DV**, **RX_ER** setup time (provided by PHY) to rising edge of **RX_CLK**	3.0		ns	Note 6-17
t_{hold}	**RXD[7:0]**, **RX_DV**, **RX_ER** hold time (provided by PHY) after rising edge of **RX_CLK**	1.0		ns	Note 6-17
t_r	**RX_CLK** rise time		1	ns	Note 6-18
t_f	**RX_CLK** fall time		1	ns	Note 6-18

Note 6-16 Min limit is non-sustainable long term.

Note 6-17 These values provide 0.5ns margin beyond the IEEE specification.

Note 6-18 t_r and t_f are measured from $V_{IL\_AC(Max)}$=0.7V to $V_{IH\_AC(Min)}$=1.9V.

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6.6.5 MII TIMING (100BASE-TX, 10BASE-T)

This section specifies the MII interface transmit and receive timing.

The below timing parameters assume default values for the following registers:
Clock Invert and Control Signal Pad Skew Register
RGMII RX Data Pad Skew Register
RGMII TX Data Pad Skew Register
Clock Pad Skew Register

FIGURE 6-6: MII TRANSMIT TIMING

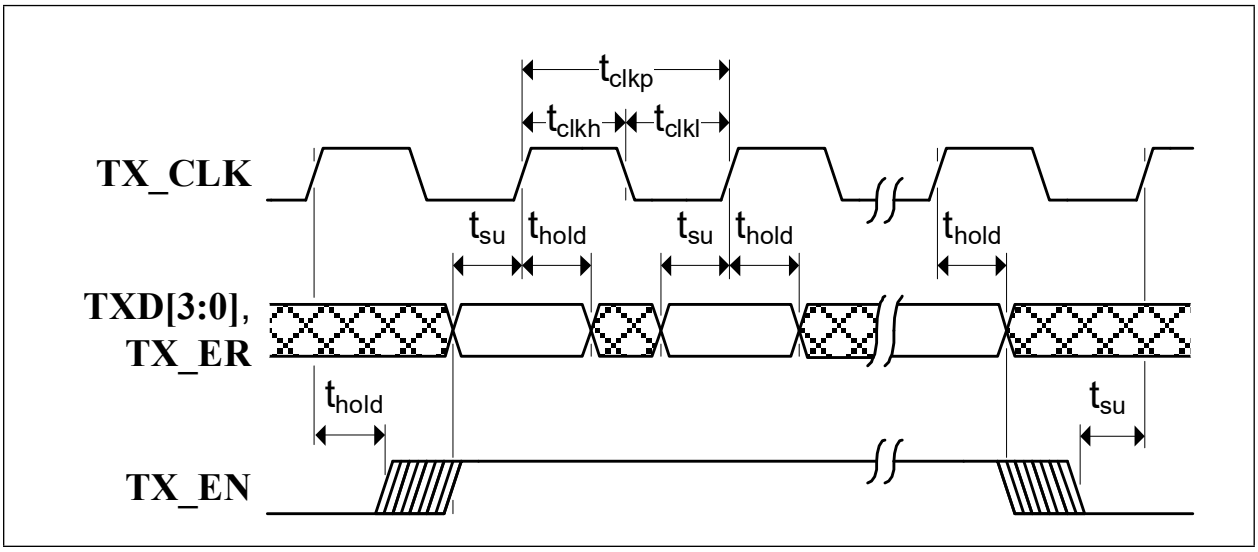

TABLE 6-21: MII TRANSMIT TIMING VALUES

Symbol	Description	Min	Max	Units	Notes
t_{clkp}	**TX_CLK** period	Note 6-19		ns	
t_{clkh}	**TX_CLK** high time	t_{clkp}*0.35	t_{clkp}*0.65	ns	
t_{clkl}	**TX_CLK** low time	t_{clkp}*0.35	t_{clkp}*0.65	ns	
t_{su}	**TXD[3:0]**, **TX_EN**, **TX_ER** setup time to rising edge of **TX_CLK**	13		ns	Note 6-20
t_{hold}	**TXD[3:0]**, **TX_EN**, **TX_ER** output hold from rising edge of **TX_CLK**	0		ns	Note 6-21

Note 6-19 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 6-20 This value provides 2 ns margin beyond the IEEE specification.

Note 6-21 This value matches the IEEE specification.

Timing was designed for system load between 10 pf and 25 pf.

FIGURE 6-7: MII RECEIVE TIMING

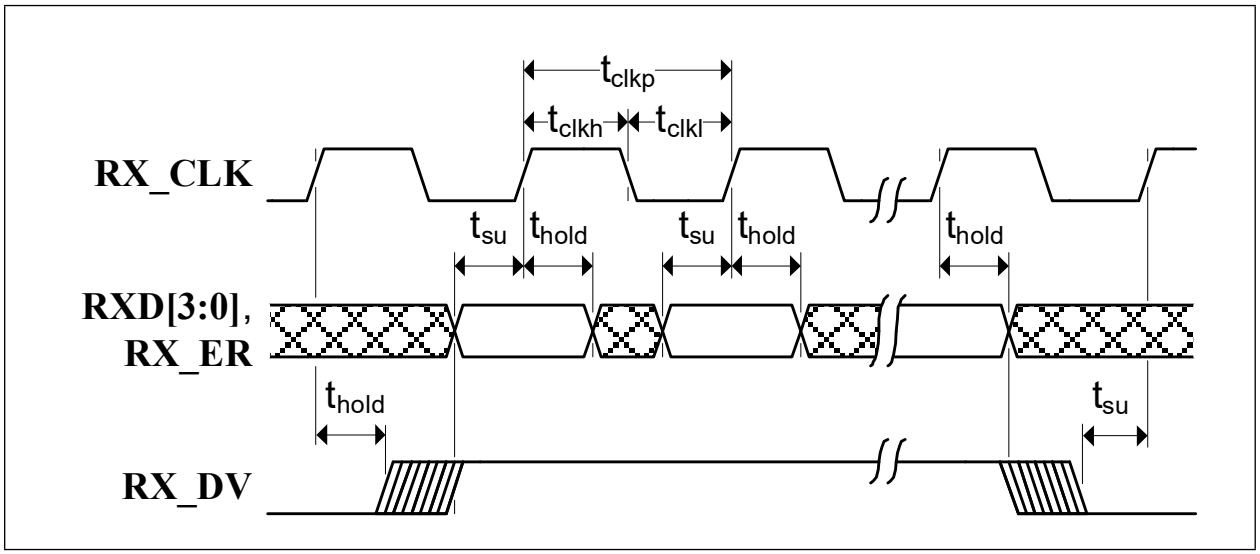

TABLE 6-22: MII RECEIVE TIMING VALUES

Symbol	Description	Min	Max	Units	Notes
t_{clkp}	**RX_CLK** period	Note 6-22		ns	
t_{clkh}	**RX_CLK** high time	t_{clkp}*0.35	t_{clkp}*0.65	ns	
t_{clkl}	**RX_CLK** low time	t_{clkp}*0.35	t_{clkp}*0.65	ns	
t_{su}	**RXD[3:0]**, **RX_DV**, **RX_ER** setup time (provided by PHY) to rising edge of **RX_CLK**	12		ns	Note 6-23
t_{hold}	**RXD[3:0]**, **RX_DV**, **RX_ER** hold time (provided by PHY) after rising edge of **RX_CLK**	12		ns	Note 6-23

Note 6-22 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 6-23 These values provide 2 ns margin beyond the IEEE specification.

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6.6.6 RGMII TIMING

This section specifies the RGMII interface transmit and receive timing. By default the device supports the Internal Delay mode specified by version 2.0 of the RGMII specification.

Note:	All RGMII timing specifications assume a point-to-point test circuit as defined in Figure 3 of the RGMII specification 2.0.

Note:	The below timing parameters assume default values for the following registers: Clock Invert and Control Signal Pad Skew Register RGMII RX Data Pad Skew Register RGMII TX Data Pad Skew Register Clock Pad Skew Register RX DLL Control Register TX DLL Control Register

6.6.6.1 TXC Internal Delay Disabled Timing (RGMII ID Mode / TC6 DoS Mode - MAC provides delayed clock)

FIGURE 6-8: TXC INTERNAL DELAY DISABLED (RGMII ID MODE / TC6 DoS MODE) TIMING

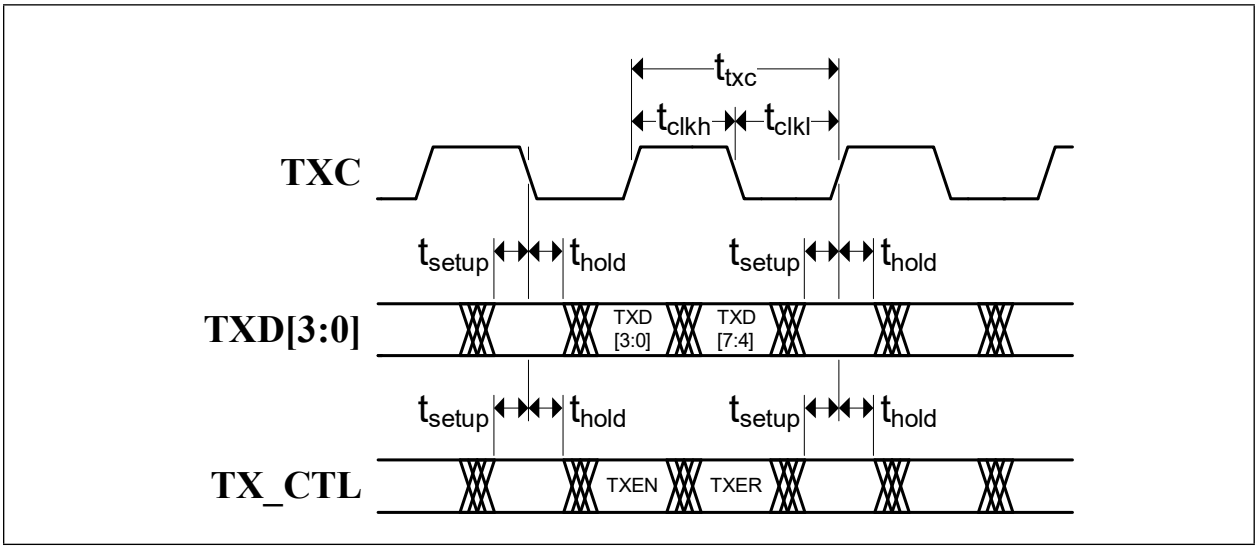

TABLE 6-23: RGMII TXC INTERNAL DELAY DISABLED (RGMII ID MODE / TC6 DoS MODE) TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{txc}	**TXC** period	Note 6-24	Note 6-25	Note 6-26	ns
t_{clkh}	**TXC** high time	Note 6-27	50	Note 6-28	%
t_{clkl}	**TXC** low time	Note 6-27	50	Note 6-28	%
t_{setup}	**TXD[3:0]**, **TX_CTL** setup time to edge of **TXC** (at inputs)	0.8 Note 6-29	2.0		ns
t_{hold}	**TXD[3:0]**, **TX_CTL** hold time after edge of **TXC** (at inputs)	0.8 Note 6-29	2.0		ns

Note 6-24 7.2ns for 1000BASE-T operation, 36ns for 100BASE-TX operation, 360ns for 10BASE-T operation. Minimum limits are non-sustainable long term.

Note 6-25 8ns for 1000BASE-T operation, 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 6-26 8.8ns for 1000BASE-T operation, 44ns for 100BASE-TX operation, 440ns for 10BASE-T operation. Maximum limits are non-sustainable long term.

Note 6-27 45% for 1000BASE-T operation, 40% for 100BASE-TX or 10BASE-T operation.

Note 6-28 55% for 1000BASE-T operation, 60% for 100BASE-TX or 10BASE-T operation.

Note 6-29 These values provide 0.2 ns margin beyond the RGMII specification and 0.25 ns margin beyond the TC6 specification.

6.6.6.2 RXC Internal Delay Enabled Timing (RGMII ID Mode / TC6 DoS Mode - PHY provides delayed clock)

FIGURE 6-9: RXC INTERNAL DELAY ENABLED (RGMII ID MODE / TC6 DoS MODE) TIMING

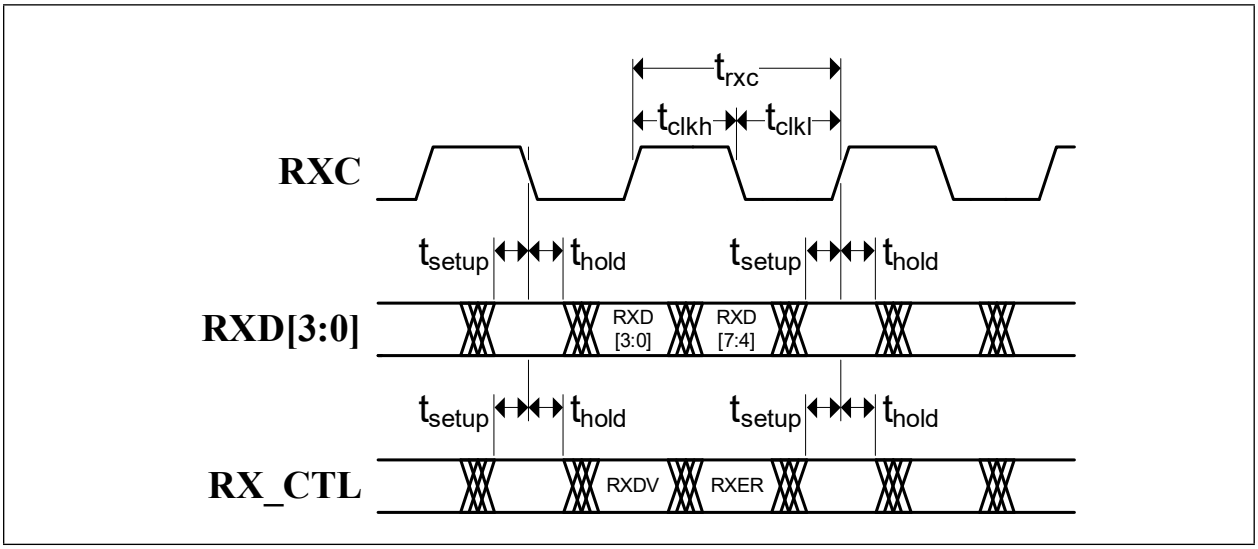

TABLE 6-24: RGMII RXC INTERNAL DELAY ENABLED (RGMII ID MODE / TC6 DoS MODE) TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{rxc}	**RXC** period	Note 6-30	Note 6-31	Note 6-32	ns
t_{clkh}	**RXC** high time	Note 6-33	50	Note 6-34	%
t_{clkl}	**RXC** low time	Note 6-33	50	Note 6-34	%
t_{setup}	**RXD[3:0]**, **RX_CTL** setup to edge of **RXC** (at outputs)	1.4 Note 6-35	2.0		ns
t_{hold}	**RXD[3:0]**, **RX_CTL** hold from edge of **RXC** (at outputs)	1.4 Note 6-35	2.0		ns

Note 6-30 7.2ns for 1000BASE-T operation, 36ns for 100BASE-TX operation, 360ns for 10BASE-T operation. Minimum limits are non-sustainable long term.

Note 6-31 8ns for 1000BASE-T operation, 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 6-32 8.8ns for 1000BASE-T operation, 44ns for 100BASE-TX operation, 440ns for 10BASE-T operation. Maximum limits are non-sustainable long term.

Note 6-33 45% for 1000BASE-T operation, 40% for 100BASE-TX or 10BASE-T operation.

Note 6-34 55% for 1000BASE-T operation, 60% for 100BASE-TX or 10BASE-T operation.

Note 6-35 These values provide 0.2 ns margin beyond the RGMII and TC6 specification.

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In order to support the Delay on Destination (DoD) mode specified by the OPEN Alliance SIG TC6 - RGMII EPL (Electrical-Physical Layer) Recommendation for Automotive Application, the internal delay on the **RXC** is disabled and the internal delay on the **TXC** is enabled. This results in data and control, at the device pins, nominally centered about the clock edges. A bounded skew allows the data and control to occur before or after the clock edges.

Note:	The below timing parameters assume default values for the following registers with the noted exceptions: Clock Invert and Control Signal Pad Skew Register RGMII RX Data Pad Skew Register RGMII TX Data Pad Skew Register Clock Pad Skew Register RX DLL Control Register - except for the bypass rxdll bit which is set TX DLL Control Register - except for the bypass txdll bit which is cleared

6.6.6.3 TXC Internal Delay Enabled Timing (TC6 DoD Mode - PHY provides delay on clock input)

FIGURE 6-10: TXC INTERNAL DELAY ENABLED (TC6 DoD MODE) TIMING

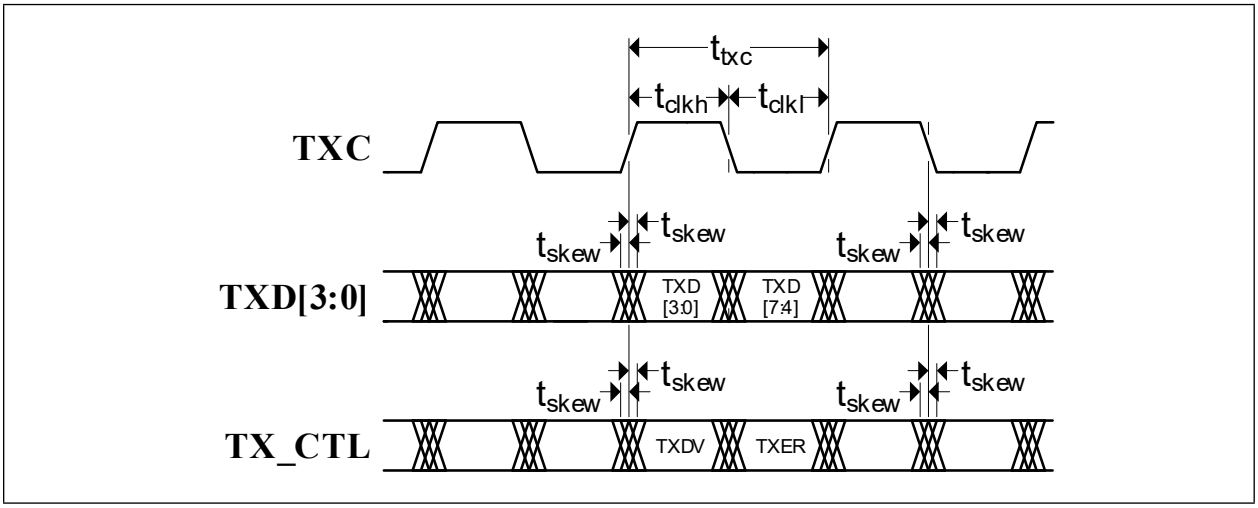

TABLE 6-25: RGMII TXC INTERNAL DELAY ENABLED (TC6 DoD MODE) TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{txc}	**TXC** period	Note 6-36	Note 6-37	Note 6-38	ns
t_{clkh}	**TXC** high time	Note 6-39	50	Note 6-40	%
t_{clkl}	**TXC** low time	Note 6-39	50	Note 6-40	%
t_{skew}	**TXD[3:0]**, **TX_CTL** to edge of **TXC** input skew	-850 Note 6-41	0	850 Note 6-41	ps

Note 6-36 7.2ns for 1000BASE-T operation, 36ns for 100BASE-TX operation, 360ns for 10BASE-T operation. Minimum limits are non-sustainable long term.

Note 6-37 8ns for 1000BASE-T operation, 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 6-38 8.8ns for 1000BASE-T operation, 44ns for 100BASE-TX operation, 440ns for 10BASE-T operation. Maximum limits are non-sustainable long term.

Note 6-39 45% for 1000BASE-T operation, 40% for 100BASE-TX or 10BASE-T operation.

Note 6-40 55% for 1000BASE-T operation, 60% for 100BASE-TX or 10BASE-T operation.

Note 6-41 These values provide 0.2 ns margin beyond the TC6 specification.

6.6.6.4 RXC Internal Delay Disabled Timing (TC6 DoD Mode - MAC provides delayed on clock input)

FIGURE 6-11: RXC INTERNAL DELAY DISABLED (TC6 DoD MODE) TIMING

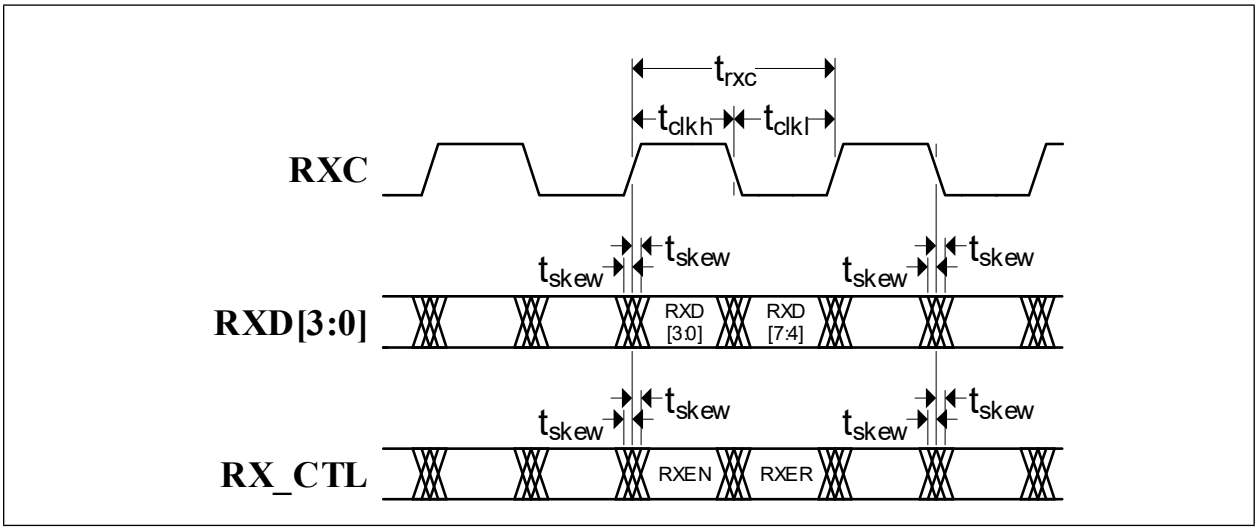

TABLE 6-26: RGMII RXC INTERNAL DELAY DISABLED (TC6 DoD MODE) TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{rxc}	**RXC** period	Note 6-42	Note 6-43	Note 6-44	ns
t_{clkh}	**RXC** high time	Note 6-45	50	Note 6-46	%
t_{clkl}	**RXC** low time	Note 6-45	50	Note 6-46	%
t_{skew}	**RXD[3:0]**, **RX_CTL** to edge of **RXC** output skew	-400 Note 6-47	0	400 Note 6-47	ps

Note 6-42 7.2ns for 1000BASE-T operation, 36ns for 100BASE-TX operation, 360ns for 10BASE-T operation. Minimum limits are non-sustainable long term.

Note 6-43 8ns for 1000BASE-T operation, 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

Note 6-44 8.8ns for 1000BASE-T operation, 44ns for 100BASE-TX operation, 440ns for 10BASE-T operation. Maximum limits are non-sustainable long term.

Note 6-45 45% for 1000BASE-T operation, 40% for 100BASE-TX or 10BASE-T operation.

Note 6-46 55% for 1000BASE-T operation, 60% for 100BASE-TX or 10BASE-T operation.

Note 6-47 These values provide 0.1 ns margin beyond the TC6 specification.

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6.6.7 AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

FIGURE 6-12: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

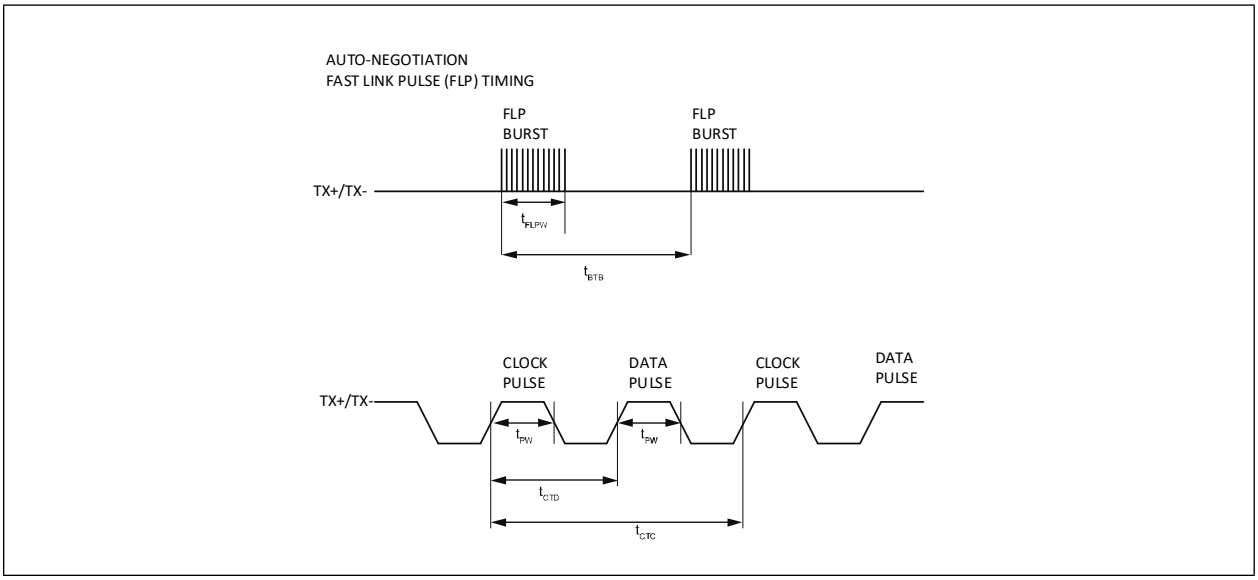

TABLE 6-27: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING PARAMETERS

Symbol	Description	Min	Typ	Max	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of clock/data pulses per FLP burst	17		33	

6.6.8 MDC/MDIO TIMING

This section specifies the **MDC/MDIO** timing of the device.

Note:	These timing numbers are valid for **MDIO** operation using push-pull **MDIO** buffers.

FIGURE 6-13: MDC/MDIO TIMING

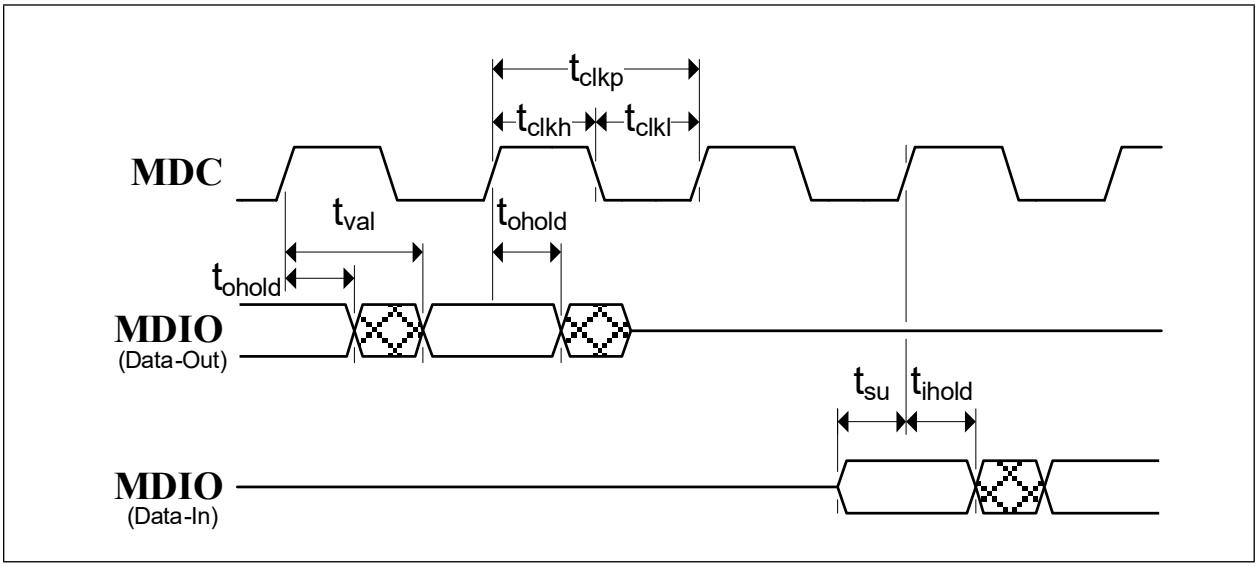

TABLE 6-28: MDC/MDIO TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{clkp}	**MDC** period	120 Note 6-48	400	Note 6-49	ns
t_{clkh}	**MDC** high time	40			ns
t_{clkl}	**MDC** low time	40			ns
t_{val}	**MDIO** (read from PHY) output valid from rising **MDIO** of **MDC**			80	ns
t_{ohold}	**MDIO** (read from **PHY**) output hold from rising edge of **MDC**	0			ns
t_{su}	**MDIO** (write to PHY) input setup time to rising edge of **MDC**	8 Note 6-50			ns
t_{ihold}	**MDIO** (write to PHY) input hold time after rising edge of **MDC**	8 Note 6-50			ns

Note 6-48 Test condition for 8.33 MHz (120 ns) is for one device PHY on the **MDIO** line with a 1.0 kΩ pull-up to the **VDDIO** supply rail.

Note 6-49 The device can operate with **MDC** clock frequencies generated from bit banging with GPIO pin in the 10s/100s of Hertz.

Note 6-50 These values provide 2 ns margin beyond the IEEE specification.

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6.6.9 GPIO SOF DETECTION TIMING

This section specifies the GPIO SOF timing of the device.

FIGURE 6-14: GPIO SOF TIMING

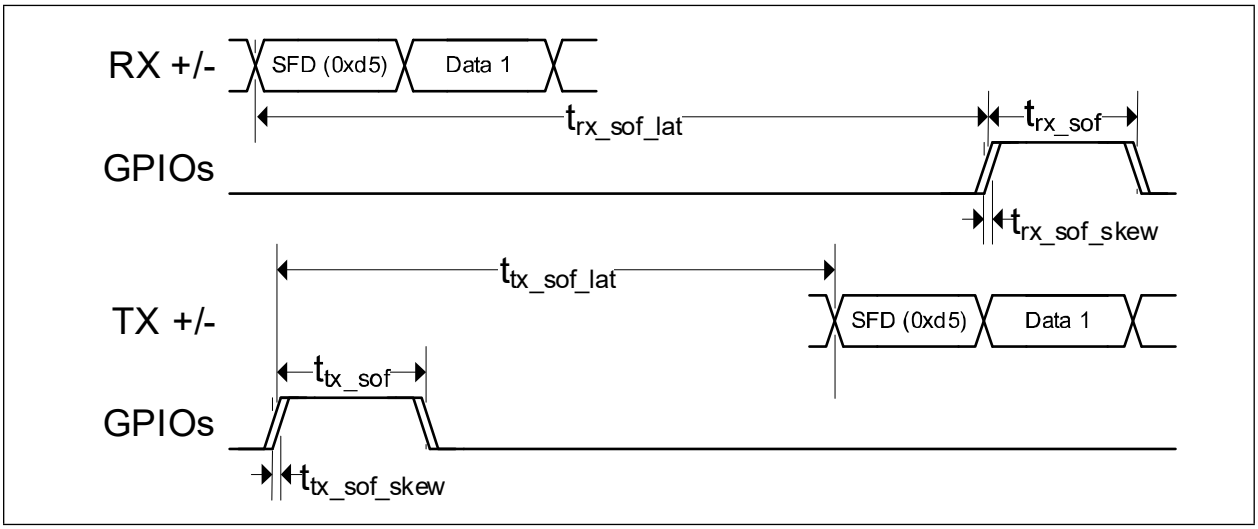

TABLE 6-29: GPIO SOF TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
$t_{rx\_sof\_lat}$	RX SOF latency		Note 6-51		-
t_{rx_sof}	RX SOF pulse width		Note 6-52		ns
$t_{rx\_sof\_skew}$	RX SOF skew between GPIOs			2	ns
$t_{tx\_sof\_lat}$	TX SOF latency		Note 6-51		-
t_{tx_sof}	TX SOF pulse width		Note 6-52		ns
$t_{tx\_sof\_skew}$	TX SOF skew between GPIOs			2	ns

Note 6-51 Refer to Section 5.18, Start of Frame (SOF) Indication.

Note 6-52 8ns for 1000BASE-T operation, 40ns for 100BASE-TX operation, 400ns for 10BASE-T operation.

6.7 Clock Circuit

The device can accept either a 25MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (+/- 50ppm) input. If the single-ended clock oscillator method is implemented, **XO** should be left unconnected and **XI** should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XI**/**XO**). See Table 6-30 for the recommended crystal specifications.

TABLE 6-30: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	+/-50	PPM	Note 6-53
Frequency Stability Over Temp	F_{temp}	-	-	+/-50	PPM	Note 6-53
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 6-54
Total Allowable PPM Budget		-	-	+/-50	PPM	Note 6-55
Shunt Capacitance	C_O	-	-	6	pF	
Load Capacitance	C_L	-	-	25	pF	
Drive Level	P_W	-	100	-	µW	
Equivalent Series Resistance	R_1	-	-	50	Ohm	
Operating Temperature Range		Note 6-56	-	Note 6-57	°C	
XI Pin Capacitance		-	2 typ	-	pF	Note 6-58
XO Pin Capacitance		-	2 typ	-	pF	Note 6-58

Note 6-53 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependent. Since any particular application must meet the IEEE +/-50 PPM Total PPM Budget, the combination of these two values must be approximately +/-45 PPM (allowing for aging).

Note 6-54 Frequency Deviation Over Time is also referred to as Aging.

Note 6-55 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as +/- 50 PPM.

Note 6-56 0°C for commercial version, -40°C for extended industrial version.

Note 6-57 +70°C for commercial version, +105°C for extended industrial version.

Note 6-58 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XO**/**XI** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

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6.8 Reset Circuit

The following are some reset circuit suggestions.

Figure 6-16 illustrates the reset circuit for powering up the LAN8841 if reset is triggered by the power supply.

FIGURE 6-15: RESET CIRCUIT IF TRIGGERED BY THE POWER SUPPLY

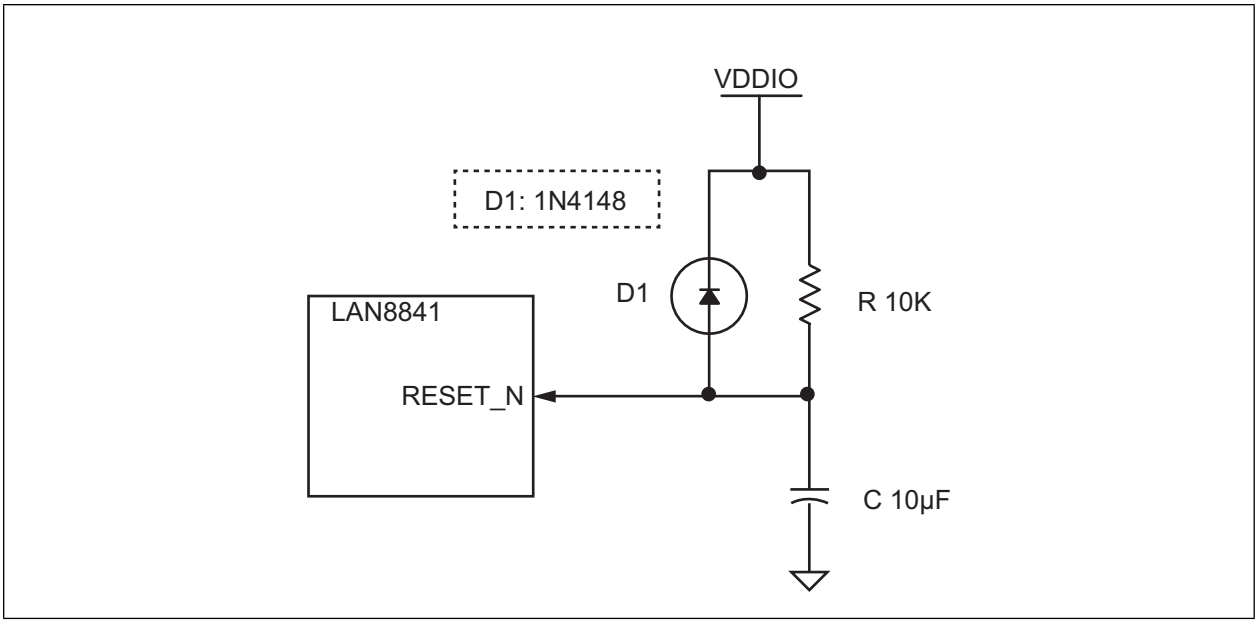


Figure 6-16 illustrates the reset circuit for applications where reset is driven by another device (for example, the CPU or an FPGA). At power-on-reset, R, C, and D1 provide the monotonic rise time to reset the LAN8841 device. The RST_OUT_N from the CPU/FPGA provides the warm reset after power-up.

The LAN8841 and CPU/FPGA references the same digital I/O voltage (**VDDIO**).

FIGURE 6-16: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET OUTPUT

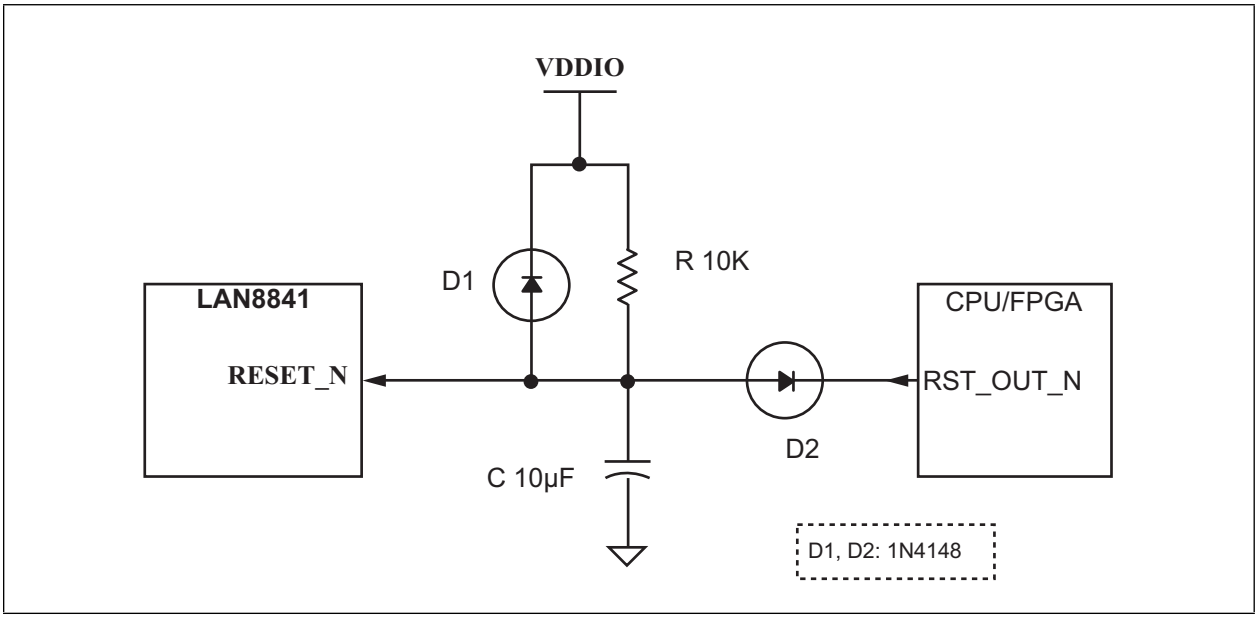
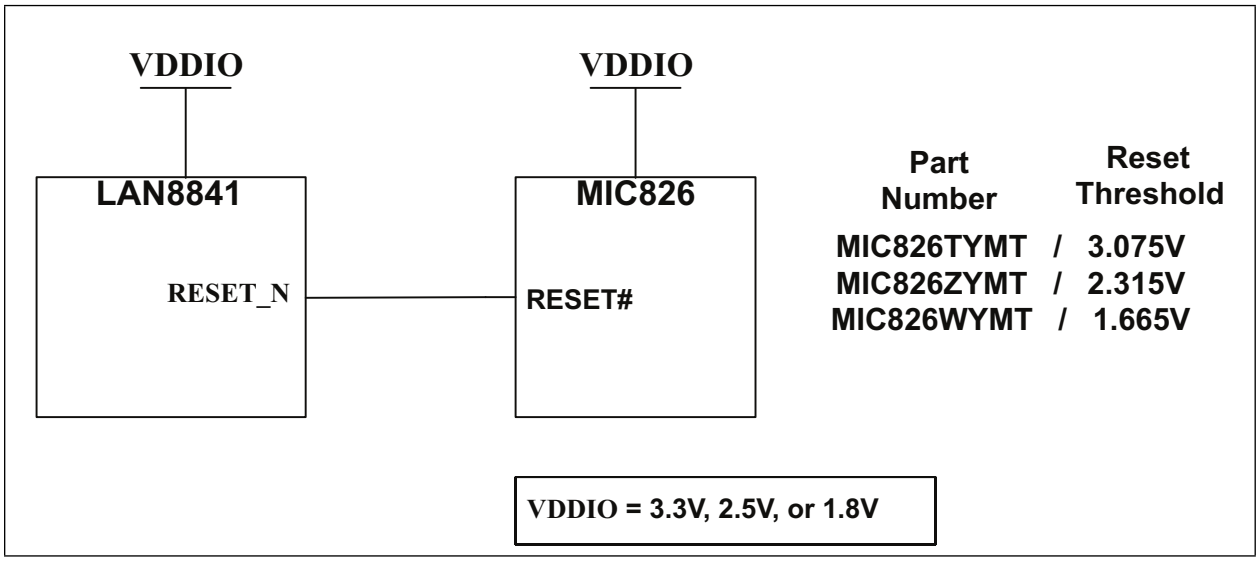


Figure 6-17 illustrates the reset circuit with an MIC826 voltage supervisor driving the LAN8841 reset input.

FIGURE 6-17: RESET CIRCUIT WITH MIC826 VOLTAGE SUPERVISOR



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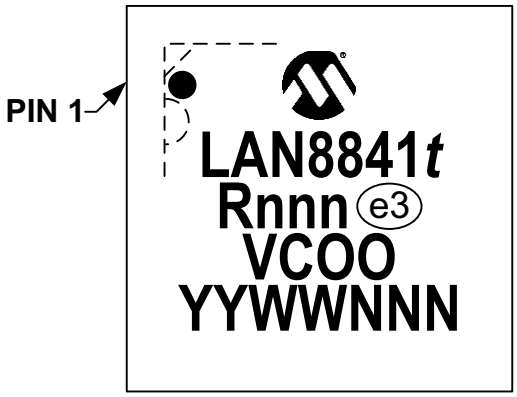
7.0 PACKAGE OUTLINE

7.1 Package Marking Information

64-VQFN (8x8 mm)



Legend:	*t*	Temperature range designator
	(Blank = commercial, v = extended industrial)	
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	V	Assembler
	COO	Country of Origin

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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7.2 Package Drawings

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

FIGURE 7-1: 64-LEAD VERY THIN PLASTIC QUAD FLAT, NO LEAD PACKAGE (Q2A) - 8X8X0.9 MM BODY [VQFN] WITH 6.5 MM EXPOSED PAD (DRAWINGS)

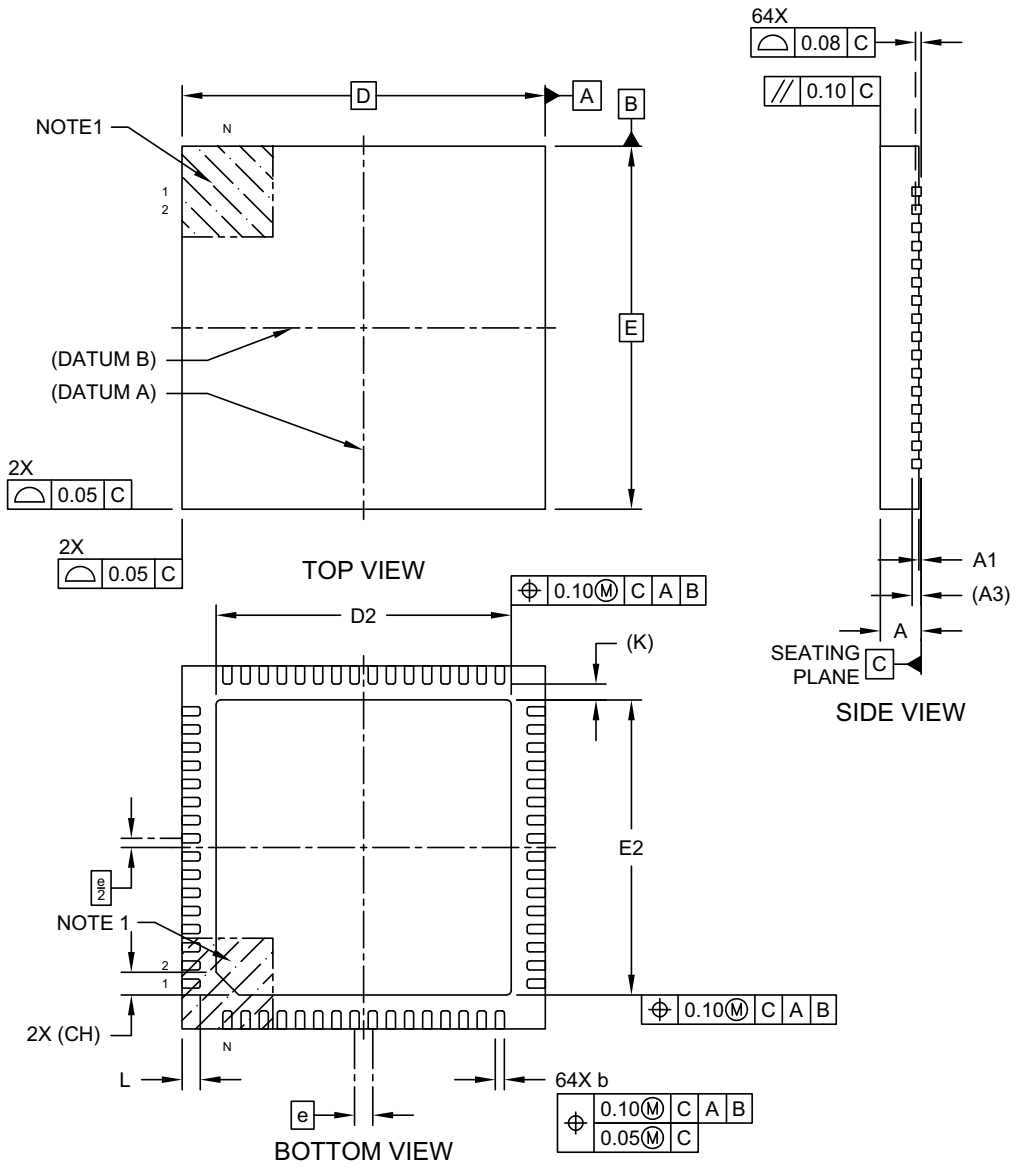

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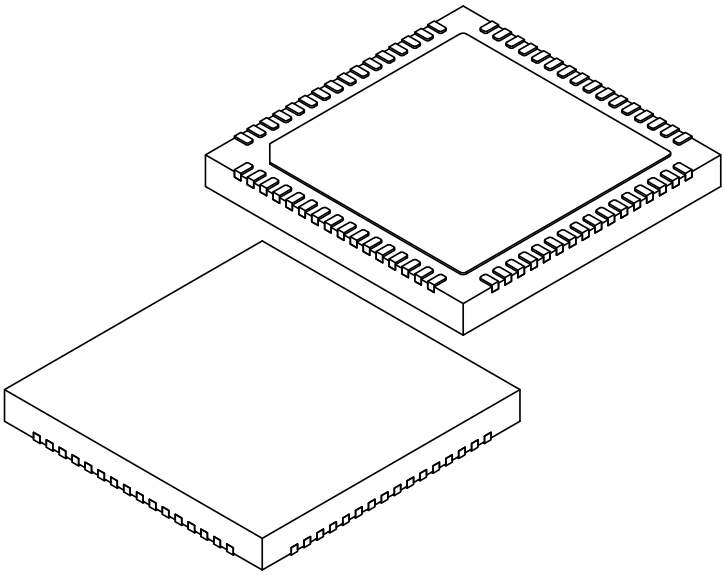
FIGURE 7-2: 64-LEAD VERY THIN PLASTIC QUAD FLAT, NO LEAD PACKAGE (Q2A) - 8X8X0.9 MM BODY [VQFN] WITH 6.5 MM EXPOSED PAD (DIMENSIONS)



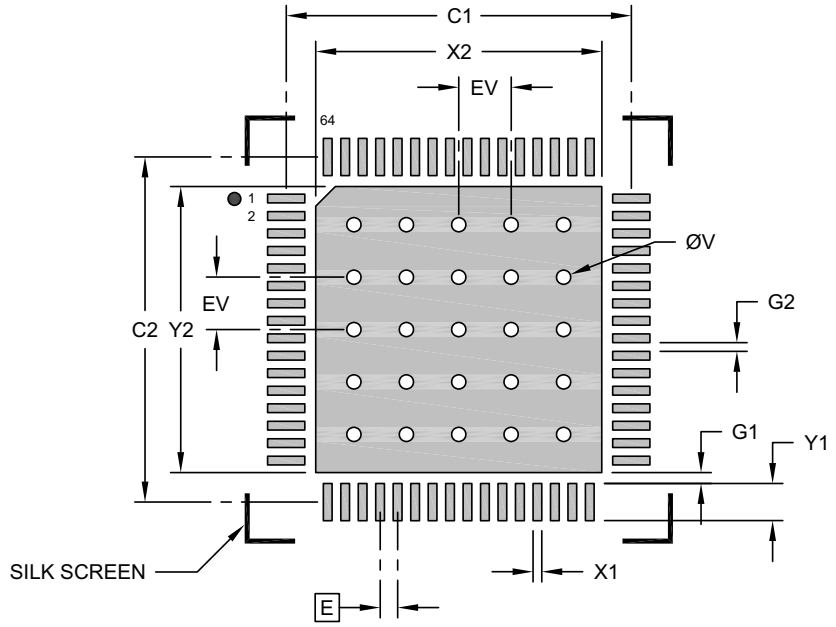
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.45	6.50	6.55
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.45	6.50	6.55
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.35 REF	
Exposed Pad Index Chamfer	CH		0.50 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1126-Q2A Rev A Sheet 2 of 2

FIGURE 7-3: 64-LEAD VERY THIN PLASTIC QUAD FLAT, NO LEAD PACKAGE (Q2A) - 8X8X0.9 MM BODY [VQFN] WITH 6.5 MM EXPOSED PAD (LANDING PATTERN)



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			6.55
Center Pad Length	Y2			6.55
Contact Pad Spacing	C1		7.90	
Contact Pad Spacing	C2		7.90	
Contact Pad Width (X64)	X1			0.20
Contact Pad Length (X64)	Y1			0.85
Contact Pad to Center Pad (X64)	G1	0.25		
Contact Pad to Contact Pad (X60)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: DOCUMENT REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00004726C (10-22-24)	Functional Description	Fast Link Failure support has been removed.
	Figure 3-1, Section 3.1, "Pin Assignments", Section 3.3.8, "LED Polarity (LEDPOL[3:1])"	Support for strapping pins LEDPOL4 and LEDPOL5 has been removed.
	Table 3-8, "Strap Inputs"	Pull down (PD) buffer type indicator has been added for LED_MODE.
	Section 3.3.2, "MagJack (MAGJACK)"	Definition has been updated from “The MAGJACK configuration straps sets the value of MMD28 registers 13h through 1Eh for compatibility with MagJack RJ-45s with common center-taps” to “The MAGJACK configuration straps sets LAN8841 for compatibility with MagJack RJ-45s with common center-taps.”
	Section 5.11, "802.3br Frame Preemption"	The following note has been added: “In 10BASE-T, PCS LOOPBACK SWAP/POLARITY CONTROL REGISTER Bit 2 needs to be set so the preamble is preserved.”
	Section 5.21, "LED Support"	Second bullet regarding Tri-Color Mode has been revised from “LED Mode = 1, LED_MODE strap input low (pulled down)” to “LED Mode = 1, LED_MODE strap input low (pulled down) or left floating.”
	Section 5.21.1, "Individual-LED Mode"	The following note has been added: “LED_MODE strap is pull-down by default (Tri-Color Mode). LED_MODE must be pulled up to enable Individual-LED Mode.”
DS00004726B (03-15-23)	Throughout Document	Updated “master” to leader and “slave” to follower where appropriate. Grammatical and formatting updates.
	Features	Removed “Tolerant” from I/O bullet descriptions
	Table 1-2, "Buffer Type Descriptions"	Removed VO24 buffer type.
	Table 1-2, "Buffer Type Descriptions"	Updated VO8, VOD8 and VOS8 buffer types and 8 mA source and sink descriptions to VO10, VOD10, VOS10 and 10 mA source and sink descriptions.
	Section 1.3, "Reference Documents"	Updated reference documents to current 802.3 specification.
	Section 2.1, "General Description"	Updated “master or slave modes” to “server or client modes”.
	Section 3.1, "Pin Assignments"	Updated Pin Assignment figures to remove preliminary schematic advisory.

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TABLE A-1: REVISION HISTORY (CONTINUED)

Revision	Section/Figure/Entry	Correction
	Table 3-6, "Miscellaneous"	In General Purpose I/O Pin Description, updated “clock” to “Local Time Counter”.
	Section 3.3, "Configuration Straps" and Section 3.4, "Pin Alternate Functions"	The following Application Note has been added to the beginning of Section 3.3 and the end of Section 3.4: “Extreme care must be taken on strap input pins that may be used for General Purpose inputs. The General Purpose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.”
	Section 3.3.1, "Device Mode Select (MODE[4:0])"	The following note has been removed: “MODE[4:0] definitions are preliminary and subject to change.”
	Table 3-10, "Device Mode Selections"	Updated “master” to “Leader PHY” and “slave” to “Follower PHY”.
	Table 3-10, "Device Mode Selections"	The following Application Note has been added to Modes 01010 and 01101: “Normally, Auto-Negotiation is required for operation at 1000Mbps. These forced settings allow manual configuration without Auto-Negotiation, however both the local and link partner devices must support this operation.”
	Figure 4-1, "Power Connectivity with Internal LDO Controller"	Updated the following pin count in diagram: VDD updated from 3 pins to 4 pins. In note, “MOSFET output” updated to “MOSFET input and output.” In note, “Ferrites on VDDAL and VDDAL_PLL may be combined” replaced with “100K resistor for inrush current migration.”
	Figure 4-2, "Power Connectivity with External 1.1V Power Supply"	Updated the following pin counts in diagram: VDD updated from 3 pins to 4 pins.
	Table 5-1, "MDI/MDI-X Pin Mapping"	Row TXRXP/M_C (4, 5), column 100BASE-T updated from “D+/-” to “C+/-”. Row TXRXP/M_D (7, 8), column 100BASE-T updated from “C+/-” to “D+/-”.
	Section 5.12, Dynamic Channel Quality (DCQ) (TC1 and TC12)	All instances of “TC1” updated to “TC1 and TC12”.
	Section 5.12, Dynamic Channel Quality (DCQ) (TC1 and TC12)	Added “and *Advanced diagnostics features for 1000BASE-T1 automotive Ethernet PHYs Version 1.7*” to “These features are designed to be compliant with Sections 6.1.1, 6.1.2, and 6.1.3 of the *OPEN Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0* specification.”
	Section 5.12.1, Mean Square Error (MSE) and Section 5.12.2, Signal Quality Indicator (SQI)	Updated “The filtered error value is saved every 1.0 ms (125,000 symbols) to “The filtered error value is saved every 65,536 symbols (524,288 us)” and moved several lines above as its own paragraph.

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TABLE A-1: REVISION HISTORY (CONTINUED)

Revision	Section/Figure/Entry	Correction
	Section 5.17.4.1, RGMII ID Timing / TC6 Delay on Source (DoS) mode	Updated “Figure 5-20 and Figure 5-21 from the RGMII v2.0 Specification...” to “Figure 5-20, Figure 5-21 and Table 5-8 from the RGMII v2.0 Specification...”.
	Table 5-17, "NAND Tree Test Pin Order"	Added LED5, LED4, and LED3 to table. Updated “LED1/PME_N1” to “LED1”. Updated “INT_N/PME_N2” to “INT_N”. Removed TXC, TX_CTL, RX_CTL and RXC.
	Table 6-4, "Typical Current/Power Consumption - RGMII - Digital I/O (2.5V), Transceiver (3.3V)"	In table title, updated “1.8V” to “2.5V”.
	Section 6.0, Operational Characteristics	Removed “On-Chip LDO Controller,” “Reference Circuits - LED Strap-In Pins” and “1588 GPIO Timing” sections from Operational Characteristics chapter.
	Section 7.0, Package Outline	Updated Package Marking Information.
DS00004726A (09-30-22)	All	Initial release.

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PART NO.	[X]	[-X]	/	XXX
Device	Media Type	Temp.		Package

Device:	LAN8841	
Media Type:	Blank	= Standard packaging (tray)
	T	= Tape and Reel(Note 1)
Temperature:	Blank	= 0°C to +70°C (Commercial)
	V	= -40°C to +105°C (Extended Industrial)
Package:	Q2A	= 64-pin VQFN (Sawn)

Examples:

a) LAN8841/Q2A
64-pin VQFN, Commercial Temperature, Tray

b) LAN8841T/Q2A
64-pin VQFN, Commercial Temperature, Tape and reel

c) LAN8841-V/Q2A
64-pin VQFN, Extended Industrial Temperature, Tray

d) LAN8841T-V/Q2A
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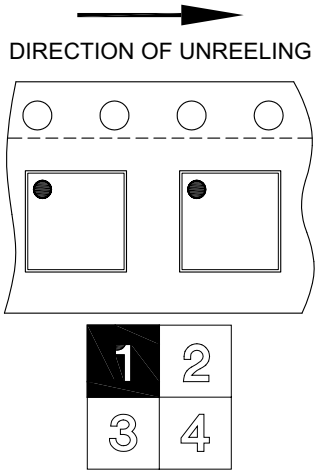

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