KSZ8851SNL

32-pin Single-Port Ethernet Controller
With Serial Peripheral Interface (SPI)

Evaluation Board User's Guide

Revision 1.1
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Revision History

Revision	Date	Summary of Changes
1.0	3/03/2008	Initial Release
1.1	4/21/10	Removed JP3 for EESK strapping option. Add JP3 for connection between VDD_IO and 1.8V (if VDD_IO is 1.8V). Changed the LED pulled up to 3.3V. Add 4.7K pull up on SO pin.

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1.0 Introduction

The KSZ8851SNL-Eval Evaluation Board is intended to provide a convenient and fast way to evaluate or demonstrate the functionality and performance of this new Single-Port Ethernet Controller KSZ8851SNL device from Micrel.

The KSZ8851SNL comes with a 32-pin, lead-free QFN (5mm x 5mm) package and provides an ideal solution for applications requiring Serial Peripheral Interface (SPI) between single-port Ethernet Controller and Host microcontroller.

This evaluation board is designed as a stand alone without microcontroller on board. By default the KSZ8851SNL-Eval board comes with an operation of no EEPROM for KSZ8851SNL device. Customer can directly wire the board for SPI interface. The purpose is to provide a simple tool that can be used to evaluate the KSZ8851SNL device by connecting via headers to customer provided Microcontroller or Non-PCI hardware platform.

Micrel provides a basic software driver based on SPI Interface solution and different operating system platforms to evaluate the KSZ8851SNL functionality and performance. The software includes a configuration utility to allow quick and easy device setup, initialization and transmit/receive packet. All KSZ8851SNL configuration pins, control signals and SPI interface are accessible either by jumpers, test points or headers.

2.0 Board Features

- One KSZ8851SNL 32-pin Single-Port Ethernet Controller with SPI for host interface
- Single +5V/GND power input from headers
- RJ-45 Jack for Fast Ethernet cable interface
- HP Auto-MDIX for automatic detection and correction for straight-through and crossover cables
- Two on board LDO voltage regulators, one for VDD_IO and the other for 3.3VA
- One AT93C46 for external EEPROM interface
- Two LED indicators for port status and activity
- One LED indicator for 3.3V output ready
- One LED indicator for Power Management Event (PME) output status
- Jumpers to configure strapping pin and VDD_IO voltage option
- Headers to wire the SPI interface from external hardware platform
- Manual reset button for quick reboot device after re-configuration of strapping pin

3.0 Evaluation Kit Contents

The KSZ8851SNL Evaluation Kit includes the following hardware:

- KSZ8851SNL Evaluation Board

The KSZ8851SNL Data Sheet and Hardware Design Package with the following collaterals that can be downloaded from Micrel's website at http://www.micrel.com

- KSZ8851SNL Eval Board Schematic (PDF and OrCAD DSN file)
- KSZ8851SNL Eval Board Gerber File (PDF version included)
- KSZ8851SNL Eval Board User's Guide (this document and included BOM)
- KSZ8851SNL IBIS Model

4.0 Hardware Description

The KSZ8851SNL-Eval (shown in Figure 1) comes in a compact form factor and plugs directly into industry standard test equipment such as Spirent SmartBits, the other side of board is wired to external host SPI interface through headers. Configuration of the KSZ8851SNL is accomplished through on-board jumper selections and/or by register access via the host SPI Interface.

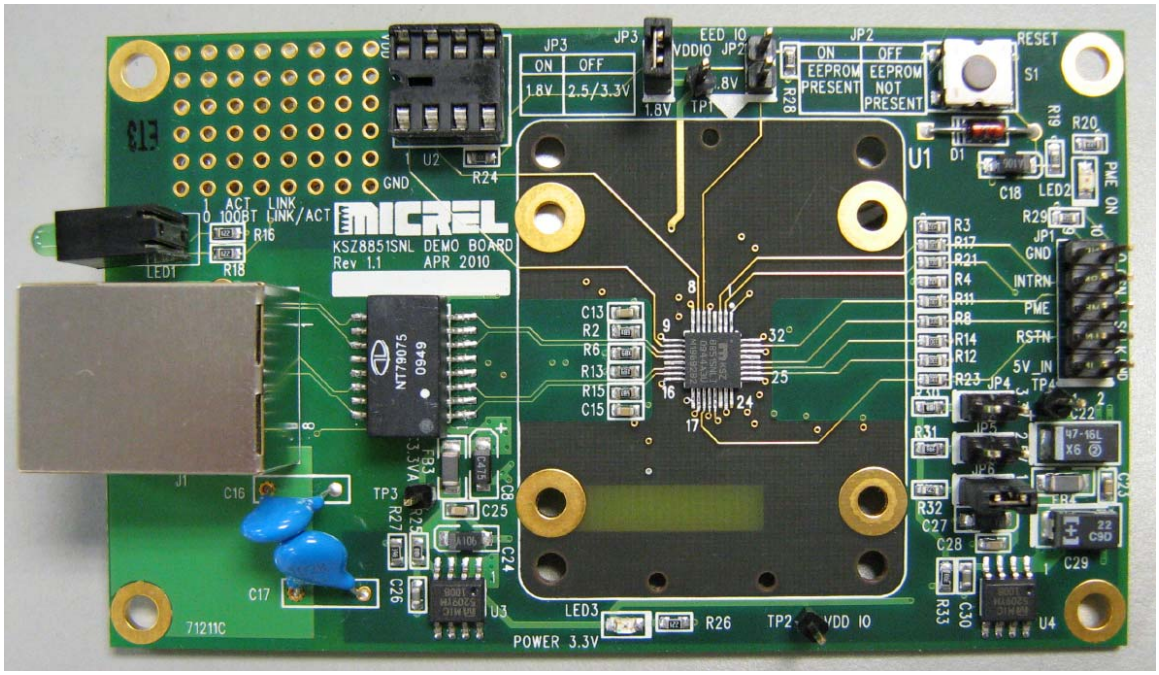

Figure 1. KSZ8851SNL Evaluation Board

Other features include a RJ-45 Jack for Fast Ethernet cable connection, transformer (Pulse H1102) to block DC level and provide a true AC coupling, EEPROM (Atmel AT93C46) to load MAC address when it is enabled, jumper to select LDO output for VDD_IO voltage, programmable LED indicators for reporting port link status and activity, and a manual reset button for quick reboot after re-configuration of strapping pins.

The KSZ8851SNL-Eval receives +5V DC input power supply from its Headers JP1.

4.1 Host SPI Interface

The KSZ8851SNL supports a SPI interface in slave mode. In this mode, a external SPI master device (micro-controller or CPU) supplies the operating serial clock (SCLK), chip select (CSN) and serial input data (SI) which is clocked in on the rising edge of SCLK to KSZ8851SNL device. Serial output data (SO) is driven out by the KSZ8851SNL on the rising edge of SCLK to external SPI master device. The falling edge of CSN is starting the SPI operation and the rising edge of CSN is ending the SPI operation. The SCLK stays low state when SPI operation is idle. Figure 6 shows the SPI interface connection for KSZ8851SNL.

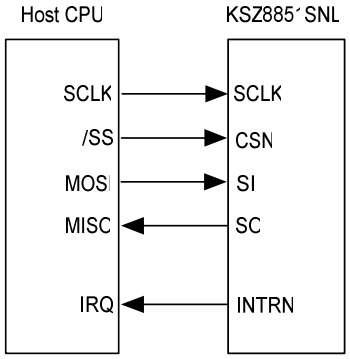

Figure 2. SPI Interface to KSZ8851SNL

The KSZ8851SNL-Eval board receives +5V power from the header JP1 (pin 1). Figure 3 shows the Host SPI interface connection with Spirent SmartBits for system set-up and performance test.

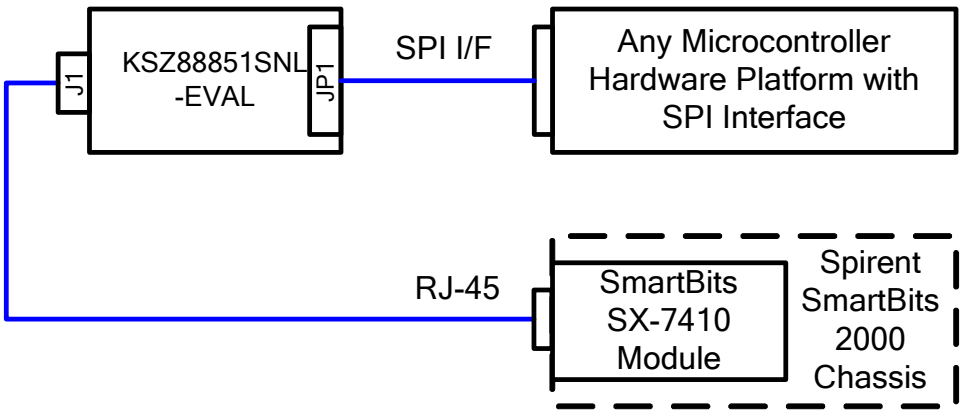

Figure 3. KSZ8851SNL-Eval Host SPI Interface Connection with Spirent SmartBits

The KSZ8851SNL-Eval has a 10-pin header (JP1) for Host SPI interface to any external Microcontroller hardware platform. Table 1 lists 4-wire SPI pin outs for the Host interface on header JP1. Table 2 lists the rest of control signals and power/ground pin outs for the Host interface on header JP1.

Pin # (JP1)	SPI Interface Signal Name	Description
4	SCLK	Serial clock input from host CPU for SPI interface. This clock speed can run up to 50 MHz
6	SI	Serial data in from host CPU for SPI interface
8	CSN	Chip Select Enable (Active low) from host CPU for SPI interface
10	SO	Serial data out to host CPU for SPI interface

Table 1. Header JP1 – Host Connection for SPI Interface

Pin # (JP1)	Power & Control Signal Names	Description
1	5.0V_IN	+5V power supply inputs for this board
2, 9	GND	Ground inputs/pins
3	RSTN	Reset input from host CPU
5	PME	Power Management Event output to host CPU
7	INTRN	Interrupt output to host CPU

Table 2. Header JP1 – Host Connection for Control and Power

4.2 Jumper Setting & Definition

The KSZ8851SNL-Eval does not require any jumper for normal operation except the VDD_IO option. During power-up, the KSZ8851SNL is configured using the chip's internal pull-up and pull-down resistors with its default strapping pin value which will set this device in operation of without EEPROM. Jumpers are provided to override the default settings, allowing for quick configuration and re-configuration of the board. To override the default settings, simply select and close the desired jumper setting(s) and toggle the on-board manual reset button (S1) for the new setting(s) to take effect.

The KSZ8851SNL-Eval jumper settings are defined in Table 3 below.

Jumper	Definition	Setting	Description
JP2	EED_IO	OFF (Default)	OFF: EEPROM is not present ON: EEPROM is present
JP3	1.8V	OFF (Default)	OFF: VDD_IO is 2.5V or 3.3V ON: VDD_IO is 1.8V
JP4	3.3V	ON (Default)	ON: to select 3.3V (JP5 and JP6 must be OFF) OFF: De-select 3.3V
JP5	2.5V	OFF (Default)	ON: to select 2.5V (JP4 and JP6 must be OFF) OFF: De-select 2.5V
JP6	1.8V	OFF (Default)	ON: to select 1.8V (JP4 and JP5 must be OFF) OFF: De-select 1.8V

Table 3. KSZ8851SNL-Eval Jumper Definition

4.3 Power Supply and Test Point Definition

The KSZ8851SNL-Eval is supplied from external +5.0V DC power through a Header (pin 1 at JP1), this +5.0V DC input is converted to both +3.3V with a Micrel LDO voltage regulator (U3, MIC5209BM) for 3.3VA analog power and VDD (option for 3.3V, 2.5V or 1.8V) with a Micrel LDO voltage regulator (U4, MIC5209BM) for VDD_IO digital power. The KSZ8851SNL contains an internal +1.8V LDO, to provide its core, analog and PLL voltages.

The KSZ8851SNL-Eval has four test points. They are defined in the following Table 4.

Test Point	Definition
TP1	1.8V digital core voltage output measurement from KSZ8851SNL internal LDO
TP2	3.3V Power supply measurement for VDD_IO
TP3	3.3VA Power supply measurement for VDD_A3.3
TP4	5.0V External power supply 5.0V_IN measurement

Table 4. KSZ8851SNL-Eval Test Point Definition

4.4 RJ-45 Connector and Transformer

The RJ-45 Jack (J1) connects to standard CAT-5 Ethernet cable to interface with 10Base-T/100Base-TX Ethernet devices. The LAN interface on the KSZ8851SNL is connected to a transformer (T1) with 50 ohm termination resistors for both TX+/- and RX+/- differential pairs. The line side of the transformer is connected to the RJ-45 connectors (J1).

J1 also supports Auto-MDIX and Auto-Negotiation / Forced Modes.

4.5 EEPROM and LED Indicators

It is optional in the KSZ8851SNL to use an external EEPROM. The EED_IO (JP2) must be pulled high (Jumper: ON) to use external EEPROM.
An external serial EEPROM with a standard microwire bus interface is used for non-volatile storage of information such as the host MAC address. The KSZ8851SNL can detect if the EEPROM is either a 1KB (93C46) or 4KB (93C66) EEPROM device. The EEPROM must be organized as 16-bit mode.

The KSZ8851SNL EEPROM format is given in Table 5.

WORD	15 8	7 0
0H	Reserved	
1H	Host MAC Address Byte 2	Host MAC Address Byte 1
2H	Host MAC Address Byte 4	Host MAC Address Byte 3
3H	Host MAC Address Byte 6	Host MAC Address Byte 5
4H – 6H	Reserved	
7H-3FH	Not used for KSZ8851SNL (available for user to use)	

Table 5. KSZ8851SNL EEPROM Format

A dual LED indicator (LED1) is located adjacent to the RJ-45 Connector (J1). The top LED is connected to LED1 (pin 32) and bottom LED is connected to LED0 (pin 1) of the KSZ8851SNL. The two LEDs are programmable to LED mode '0' or '1' via register 0xC6 bits [9], and are defined in the following Table 6.

	LED Mode	
	0 (Default)	**1**
LED1 (Top)	100BT	ACT
LED1 (Bottom)	LINK/ACT	LINK

Table 6. KSZ8851SNL-Eval Port Status LED Definition

Table 7 shows the rest of LEDs definition.

LED	Color	Description
LED2	Green	Power Management Event (PME) Status
LED3	Red	3.3V Power available indicator

Table 7. KSZ8851SNL-Eval LED Definition

4.6 Board Reset

The KSZ8851SNL-Eval generates a reset signal from the reset circuitry during power up. It also provides a push button S1 reset circuit to reset the KSZ8851SNL device. During power up, the board is automatically reset. User can also press reset button S1 on the board for a manual reset.

5.0 Bill of Materials

KSZ8851SNL Eval Board (Revision 1.1)

Item	Quantity	Reference	Part	Footprint	Vendor	Remark
1	4	C1,C4,C7,C8	4.7uF	SIZE A	Digikey 4932361-1	
2	12	C2,C3,C5,C9,C10,C11,C13	0.1uF	603		
		C15,C19,C23,C25,C28				
3	2	C6,C12	0.01uF	603		
4	4	C14,C18,C24,C27	10uF	SIZE A	Digikey 4932351-1	
5	2	C16,C17	1000pF/2KV	1808	399-3443-1-ND	
6	2	C20,C21	22pF	603		
7	1	C22	47uF	SIZE C		
8	2	C30,C26	470pF	603		
9	1	C29	22uF	SIZE B		
10	1	D1	1N4148	DIODE\.400		
11	2	D2,D3 (for reference & not design in)	GBLC03C_0	SOD-323		Option
12	4	FB1,FB2,FB3,FB4	FBEAD (Steward HI1206N101R-00)	1206		
13	1	JP1	HEADER	5x2 (TH 0.1mm)		
14	5	JP2,JP3,JP4,JP5,JP6	JUMPER	SIP\2P		
15	1	J1	RJ-45 Jack			
16	1	LED1	LEDx2 (Dialight 553-0122-300 Green)			
17	2	LED2 (green)	LED GRN (67-1553-1-ND 0805)		Digikey	
		LED3 (red)	LED RED (67-1553-1-ND 0805)		Digikey	
18	2	R1,R24	0	603		
19	4	R2,R6,R13,R15	49.9	603		
20	4	R3,R4,R28,R29	4.7K	603		
21	4	R5,R7,R9,R10	75	603		
22	7	R8,R11,R12,R14,R17,R21,R23	33	603		
23	4	R16,R18,R20,R26	220	603		
24	1	R19	10K	603		
25	1	R22	3.01K	603		
26	2	R30,R25	1.5K	603		
27	2	R33,R27	2.49K	603		
28	1	R31	2.46K	603		
29	1	R32	5.54K	603		
30	1	S1	SW PUSHBUTTON			
31	4	TP1,TP2,TP3,TP4	TestPoint			
32	1	T1	SINGLE H1102		PULSE	
33	1	U1	KSZ8851SNL (32-pin 5mmx5mm QFP)		Micrel	w/Socket
34	1	U2	AT93C46 SO8	DIP8	ATMEL	w/Socket
35	2	U3,U4	MIC5209BM	SOIC-8	Micrel	
36	1	U5 (for reference & not design in)	SRV05-4	SOT23-6		Option
37	1	Y1	25MHZ Crystal	CA-301	Digikey	SE3441-ND

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