KSZ8842-PMQL/PMBL

Two-Port Ethernet Switch with PCI Interface

Features

Switch Management

- Non-Blocking Switch Fabric Assures Fast Packet Delivery by Utilizing a 1K Entry MAC Address Look-Up Engine and a Store-and-Forward Architecture
- Fully Compliant with the IEEE802.3u Standards
- Full-Duplex IEEE 802.3x Flow Control (Pause) with Force Mode Option
- Half-Duplex Backpressure Flow Control

Advance Switch Management

- IEEE 802.1Q VLAN Support for Up to Sixteen Goups (Full-Range of VLAN IDs)
- VLAN ID Tag/Untag Options, Per Port Basis
- IEEE 802.1p/Q Tag Insertion or Removal On a Per-Port Basis (Egress)
- Programmable Rate Limiting at the Ingress and Egress Port
- Broadcast Storm Protection
- IEEE 802.1d Spanning Tree Protocol Support
- MAC Filtering Function to Filter Unicast Packets
- Unknown MAC Address Forwarding Function
- Direct Forwarding Mode Enabling the Processor to Identify the Ingress Port and to Specify the Egress Port
- IGMP v1/v2 Snooping Support for Multicast Packet Filtering
- IPV6 Multicast Listener Discovery (MLD) Snooping support

Monitoring

- Port Mirroring/Monitoring/Sniffing: Ingress and/or Egress Traffic to Any Port
- Management Information Base (MIB) Counters for Fully Compliant Statistics Gathering: 32 MIB Counters Per Port
- Loop Back Modes for Remote Failure Diagnostics

Comprehensive Register Access

- There are Three Kinds of Register Groups:
- The PCI Configuration Registers are Used to Initialize and Configure the PCI Interface
- The PCI Control/Status Registers are Used to Communicate Between the Host and KSZ8842-PMQL/PMBL
- Switch Registers are Used to Support Transceiver Control and Status. They are Configurable On-the-Fly (Port-Priority, 802.1p/d/Q, etc.)

QoS/CoS Packets Prioritization Support

- Per Port, 802.1p and DiffServ Based
- Re-Mapping of 802.1p Priority Field on a Per Port Basis

Power Modes, Packaging, and Power Supplies

- Full-chip Hardware Power-Down (Register Configuration not Saved) Provides for Low Power Dissipation
- Per Port-Based Software Power-Save on PHY (Idle Link Detection, Register Configuration Preserved)
- Single Power Supply: 3.3V
- Commercial Temperature Range: 0°C to +70°C
- Industrial Temperature Range: –40°C to +85°C
- Available in 128-Pin PQFP and 100-Ball LFBGA

Additional Features

- In Addition to Offering All of the Features of an Integrated Layer-Two Managed Switch, the KSZ8842-PMQL/PMBL Offers:
- Repeater Mode Capabilities to Allow for Cut Through in Latency Critical Industrial Ethernet or Embedded Ethernet Applications
- Dynamic Buffer Memory Scheme Essential for Applications Such as Video Over IP Where Image Jitter is Unacceptable
- Two-Port Switch with a 32-Bit/33 MHz PCI Processor Interface.
- Microchip LinkMD® Cable Diagnostics to Determine Cable Length, Diagnose Faulty Cables, and Determine Distance-to-Fault
- Hewlett Packard (HP) Auto MDI-X Crossover with Disable and Enable Options
- Four Priority Queues to Handle Voice, Video, Data, and Control Packets
- Ability to Transmit and Receive Jumbo Frame Sizes Up to 1916 Bytes

Applications

- Video Distribution Systems
- High-End Cable, Satellite, and IP Set-Top Boxes
- Video Over IP
- Voice Over IP (VoIP) and Analog Telephone Adapters (ATA)
- Industrial Control in Latency Critical Applications
- Motion Control
- Industrial Control Sensor Devices (Temperature, Pressure, Levels, and Valves)
- Security and Surveillance Cameras

Markets

- Fast Ethernet
- Embedded Ethernet
- Industrial Ethernet

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Table of Contents

1.0 INTRODUCTION

1.1 General Description

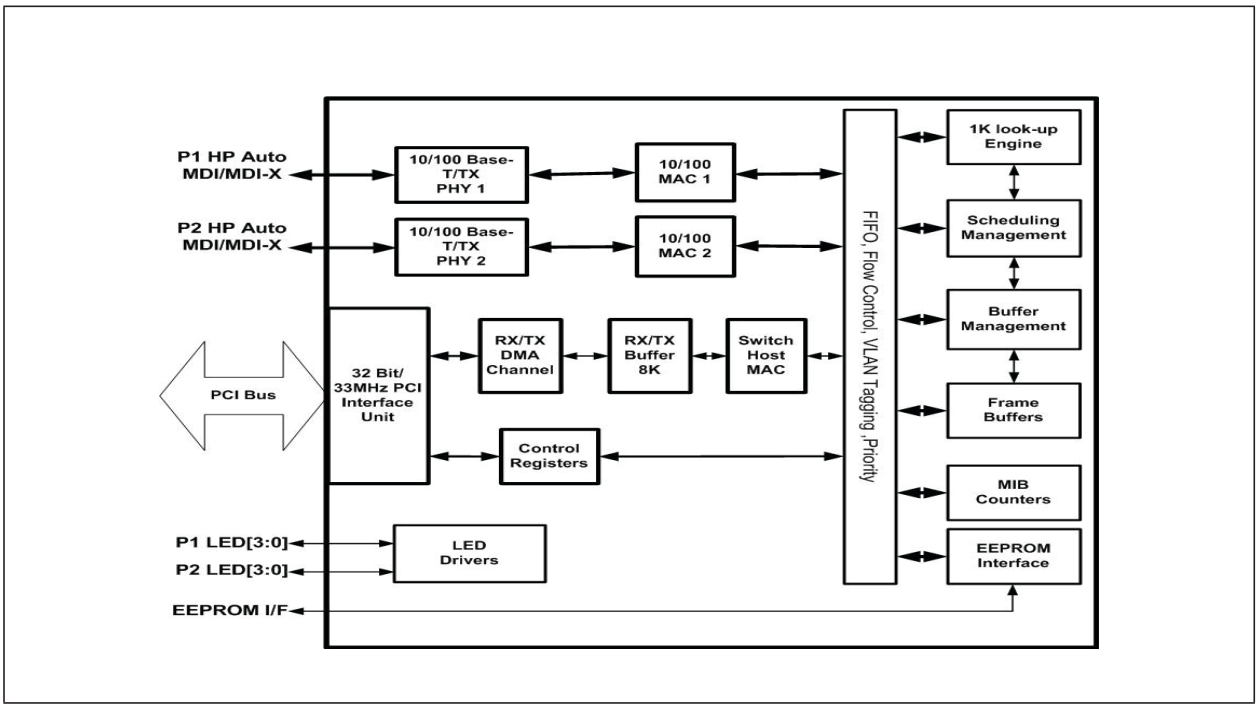
The KSZ8842-series of 2-port switches includes PCI and non-PCI CPU interfaces. This data sheet describes the KSZ8842-PMQL/PMBL PCI CPU interface chips. KSZ8842-PMQL is PQFP package chip, KSZ8842-PMBL is LFBGA package chip. For information on the KSZ8842-MQL/MBL CPU non-PCI interface switches, refer to the KSZ8842-MQL/MBL data sheet.

The KSZ8842-PMQL/PMBL is the industry's first fully managed two-port switch with a 32 bit/33MHz PCI processor interface. It is a proven, fourth generation, integrated layer two switch that is compliant with the IEEE 802.3u standard. An industrial temperature grade version of the KSZ8842-PMQL/PMBL, also can be ordered the KSZ8842-PMQLI/PMBL AM.

The KSZ8842-PMQL/PMBL can be configured as a switch or as a low-latency (<310 nanoseconds) repeater in latency-critical, embedded or industrial Ethernet applications. For industrial automation applications, the KSZ8842-PMQL/PMBL can run in half-duplex mode regardless of the application. The KSZ8842-PMQL/PMBL offers an extensive feature set that includes tag/port-based VLAN, quality of service (QoS) priority management, management information base (MIB) counters, and CPU control/data interfaces to effectively address Fast Ethernet applications.

The KSZ8842-PMQL/PMBL contains two 10/100 transceivers with patented, mixed-signal, low-power technology three media access control (MAC) units, a direct memory access (DMA) channel, a high-speed, non-blocking, switch fabric, a dedicated 1K entry forwarding table, and an on-chip frame buffer memory.

FIGURE 1-1: KSZ8842-PMQL/PMBL FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION AND BALLS CONFIGURATION

FIGURE 2-1: PIN CONFIGURATION FOR KSZ8842-PMQL (128-PIN PQFP) (TOP VIEW)

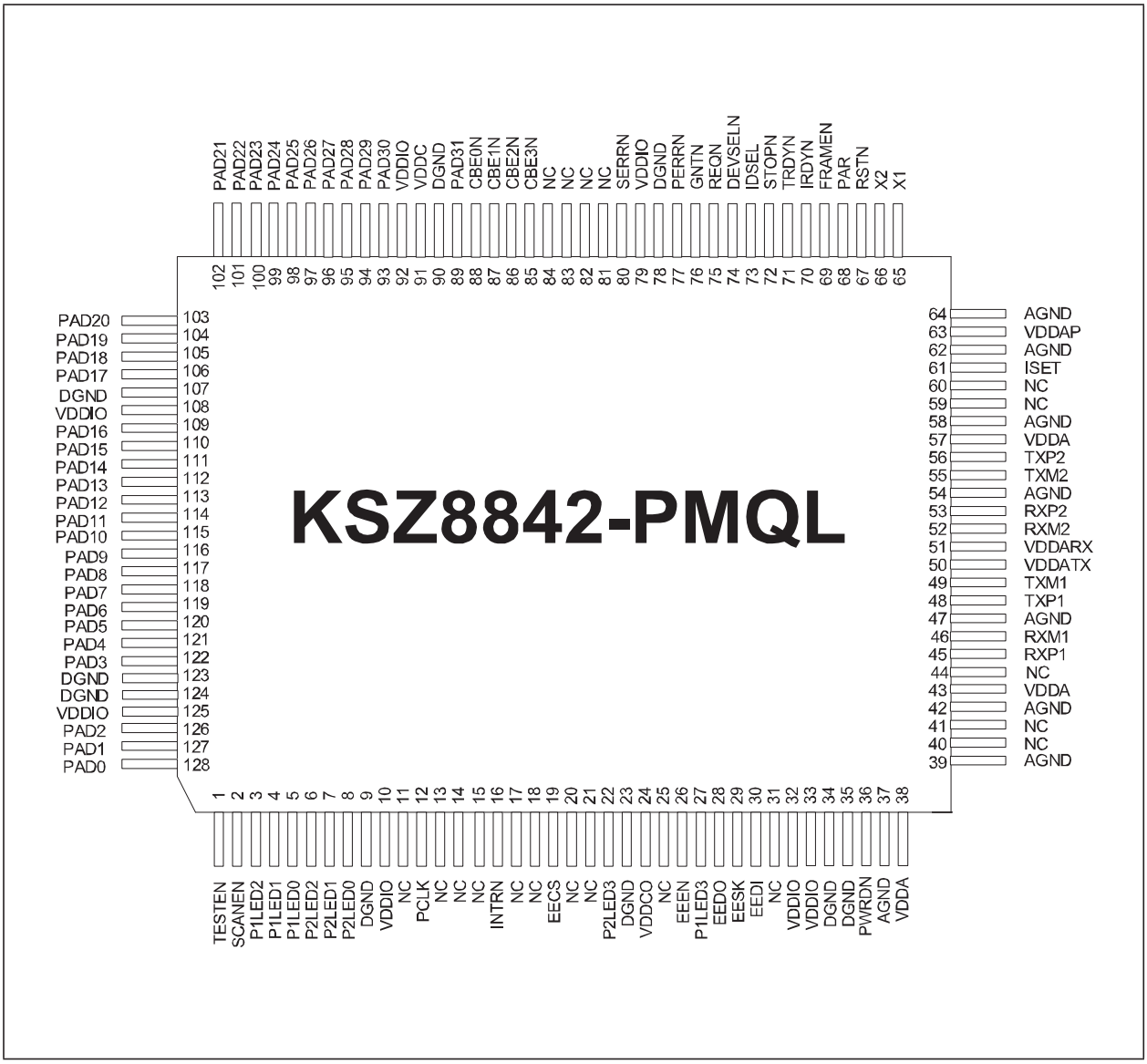


FIGURE 2-2: KSZ8842-PMBL 100-BALL LFBGA (TOP VIEW)

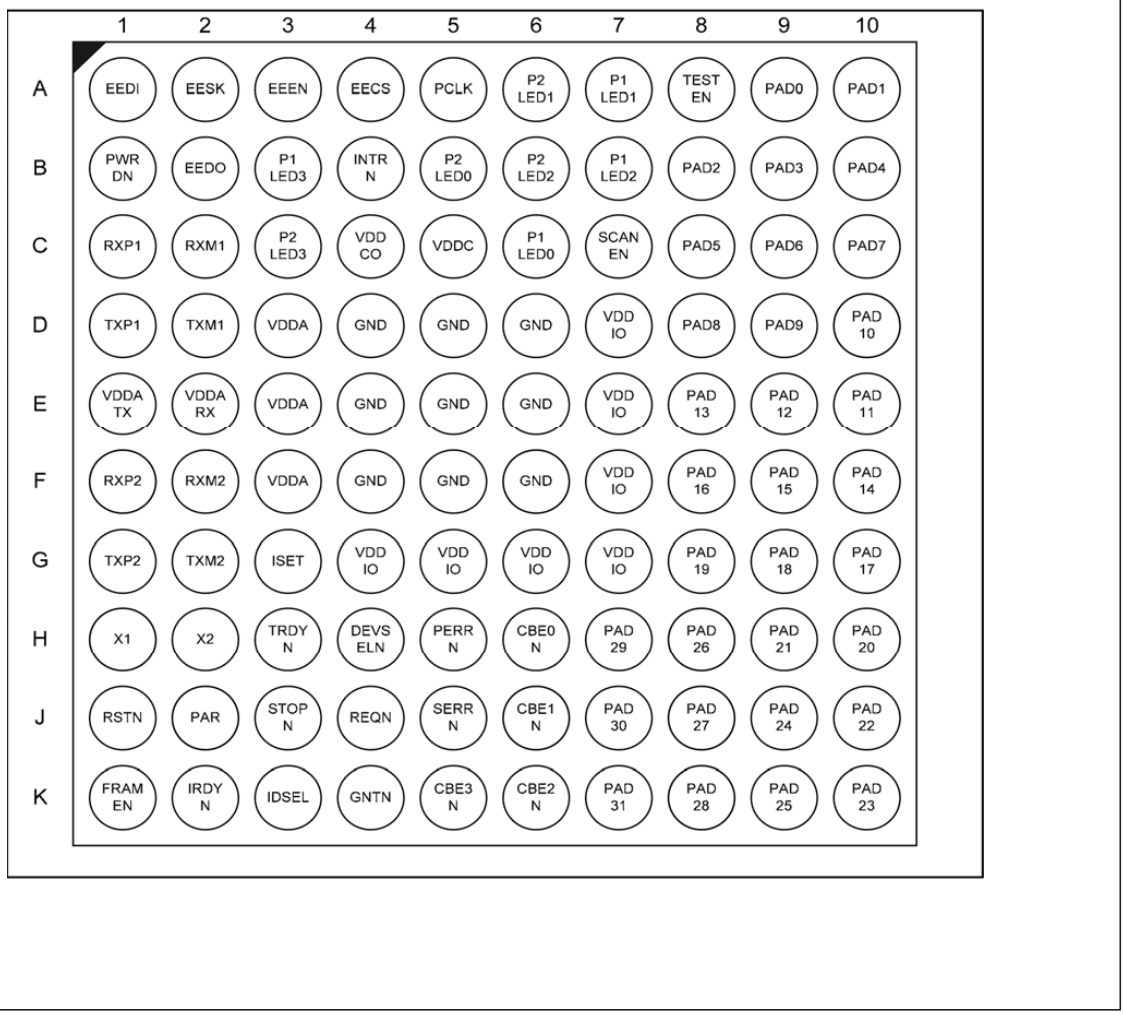


TABLE 2-1: SIGNALS

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Description</th></tr>
<tr><td>1</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>2</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>3
4
5
6
7
8</td><td>P1LED2
P1LED1
P1LED0
P2LED2
P2LED1
P2LED0</td><td>OPU</td><td>Port 1 and Port 2 LED Indicators, defined as follows:
LEDs turn on when low.
<table>
<tr><td></td><td colspan="2">Chip Global Control Register 5:
SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0, 0] Default</td><td>[0, 1]</td></tr>
<tr><td>P1LED3 /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
<tr><td></td><td colspan="2">Reg. SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[1, 0]</td><td>[1, 1]</td></tr>
<tr><td>P1LED3 /P2LED3</td><td>Activity</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Note: Link = On; Activity = Blink; Link/Act = On/Blink; Full-Duplex/Col = On/Blink; Full-Duplex = On (Full-duplex); Off (Half-duplex); Speed = On (100BASE-T); Off (10BASE-T)
Note: P1LED3 is pin 27. P2LED3 is pin 22.
Port 1 and Port 2 LED indicators1 for Repeater mode defined as follows:
<table>
<tr><td></td><td colspan="2">Switch Global Control Register 5:
SGCR5 bit [15,9]</td></tr>
<tr><td></td><td>[0,0] Default</td><td>[0,1] [1,0],[1,1]</td></tr>
<tr><td>P1LED3/P2LED3</td><td>RPT_COL, RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>RPT_Link3/RX,
RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>RPT_Link2/RX,
RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>RPT_Link1/RX,
RPT_ERR1</td><td>—</td></tr>
</table>
Note: RPT_COL = Blink; RPT_Link3/RX (Host Port) = On/Blink; RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink; RPT_ACT = On if any activity; RPT_ERR3 (Host port) = On if any CRC error; RPT_ERR2 (Port 2) = On if any CRC error; RPT_ERR1 (Port 1) = On if any CRC error</td></tr>
<tr><td>9</td><td>DGND</td><td>GND</td><td>Digital ground.</td></tr>
<tr><td>10</td><td>VDDIO</td><td>P</td><td>3.3V digital I/O V_{DD}</td></tr>
<tr><td>11</td><td>NC</td><td>—</td><td>No connect.</td></tr>
<tr><td>12</td><td>PCLK</td><td>IPD</td><td>PCI Bus Clock
This Clock provides the timing for all PCI bus phases. The rising edge defines the start of each phase. The clock maximum frequency is 33 MHz.</td></tr>
</table>

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
13	NC	—	No connect.
14	NC	—	No connect.
15	NC	—	No connect.
16	INTRN	OPD	Interrupt Request Active Low signal to host CPU to request an interrupt when any one of the interrupt conditions occurs in the registers. This pin should be pulled up externally.
17	NC	—	No connect.
18	NC	—	No connect.
19	EECS	OPU	EEPROM Chip Select This signal is used to select an external EEPROM device.
20	NC	—	No connect.
21	NC	—	No connect.
22	P2LED3	OPD	Port 2 LED Indicator See the description in pins 6, 7, and 8.
23	DGND	GND	Digital IO ground.
24	VDDCO	P	1.2V Core Voltage Output. (Internal 1.2V LDO power supply output) This pin provides 1.2V power supply to all 1.2V power pin, VDDC, VDDA, VDDAP. It is recommended the pin should be connected to 3.3V power rail by a 100Ω resistor for the internal LDO application. The 100Ω resistor is for Rev A6 and should no longer be fitted for latest Rev A7.
25	NC	—	No connect.
26	EEEN	IPD	EEPROM Enable EEPROM is enabled and connected when this pin is pulled up. EEPROM is disabled when this pin is pulled down or no connect.
27	P1LED3	OPD	Port 1 LED indicator See the description in pins 3, 4, and 5.
28	EEDO	OPD	EEPROM Data Out This pin is connected to DI input of the serial EEPROM.
29	EESK	OPD	EEPROM Serial Clock 4 µs serial clock to load configuration data from the serial EEPROM.
30	EEDI	IPD	EEPROM Data In This pin is connected to DO output of the serial EEPROM.
31	NC	—	No connect.
32	VDDIO	P	3.3V digital I/O V_{DD}
33	VDDIO	P	3.3V digital I/O V_{DD}
34	DGND	GND	Digital ground
35	DGND	GND	Digital ground
36	PWRDN	IPU	Full-chip power-down. Active Low
37	AGND	GND	Analog ground
38	VDDA	P	1.2V analog V_{DD}
39	AGND	GND	Analog ground
40	NC	—	No Connect
41	NC	—	No Connect
42	AGND	GND	Analog ground
43	VDDA	P	1.2V analog V_{DD}
44	NC	—	No Connect

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
45	RXP1	I/O	Physical receive (MDI) or transmit (MDIX) signal (+ differential)
46	RXM1	I/O	Physical receive (MDI) or transmit (MDIX) signal (– differential)
47	AGND	GND	Analog ground
48	TXP1	I/O	Physical transmit (MDI) or receive (MDIX) signal (+ differential)
49	TXM1	I/O	Physical transmit (MDI) or receive (MDIX) signal (– differential)
50	VDDATX	P	3.3V analog V_{DD}.
51	VDDARX	P	3.3V analog V_{DD}.
52	RXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (– differential)
53	RXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential)
54	AGND	GND	Analog ground
55	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (– differential)
56	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (+ differential)
57	VDDA	P	1.2 analog V_{DD}.
58	AGND	GND	Analog ground
59	NC	—	No connect
60	NC	—	No connect
61	ISET	O	Set physical transmit output current. Pull-down this pin with a 3.01 kΩ 1% resistor to ground.
62	AGND	GND	Analog ground
63	VDDAP	P	1.2V analog V_{DD} for PLL.
64	AGND	GND	Analog ground
65	X1	I	25 MHz crystal or oscillator clock connection. Pins (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. **Note:** Clock requirement is ±50 ppm for either crystal or oscillator.
66	X2	O	
67	RSTN	IPU	Hardware Reset, Active-Low RSTN will cause the KSZ8842-PMQL to reset all of its functional blocks. RSTN must be asserted for a minimum duration of 10 ms.
68	PAR	I/O	PCI Parity Even parity computed for PAD[31:0] and CBE[3:0]N, master drives PAR for address and write data phase, target drives PAR for read data phase.
69	FRAMEN	I/O	PCI Cycle Frame This signal is asserted low to indicate the beginning of the address phase of the bus transaction and deasserted before the final transfer of the data phase of the transaction in a bus master mode. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
70	IRDYN	I/O	PCI Initiator Ready As a bus master, this signal is asserted low to indicate valid data phases on PAD[31:0] during write data phases, indicates it is ready to accept data during read data phases. As a target, it'll monitor this IRDYN signal that indicates the master has put the data on the bus.
71	TRDYN	I/O	PCI Target Ready As a bus target, this signal is asserted low to indicate valid data phases on PAD[31:0] during read data phases, indicates it is ready to accept data during write data phases. As a master, it will monitor this TRDYN signal that indicates the target is ready for data during read/write operation.

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
72	STOPN	I/O	PCI Stop This signal is asserted low by the target device to request the master device to stop the current transaction.
73	IDSEL	I/O	PCI Initialization Device Select This signal is used to select the KSZ8842-PMQL during configuration read and write transaction.
74	DEVSELN	I/O	PCI Device Select This signal is asserted low when it is selected as a target during a bus transaction. As a bus master, the KSZ8842-PMQL samples this signal to ensure that a PCI target recognizes the destination address for the data transfer.
75	REQN	O	PCI Bus Request The KSZ8842-PMQL will assert this signal low to request PCI bus master operation.
76	GNTN	I	PCI Bus Grant This signal is asserted low to indicate to the KSZ8842-PMQL that it has been granted the PCI bus master operation.
77	PERRN	I/O	PCI Parity Error The KSZ8842-PMQL as a master or target will assert this signal low to indicate a parity error on any incoming data. As a bus master, it will monitor this signal on all write operations.
78	DGND	GND	Digital I/O ground
79	VDDIO	P	3.3V digital V_{DDIO}
80	SERRN	O	PCI System Error This system error signal is asserted low by the KSZ8841-PMQL. This signal is used to report address parity errors.
81	NC	—	No Connect
82	NC	—	No Connect
83	NC	—	No Connect
84	NC	—	No Connect
85	CBE3N	I/O	Command and Byte Enable These signals are multiplexed on the same PCI pins. During the address phase, these lines define the bus command. During the data phase, these lines are used as Byte Enables, The Byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data.
86	CBE2N	I/O	
87	CBE1N	I/O	
88	CBE0N	I/O	
89	PAD31	I/O	PCI Address/Data 31 Address and data are multiplexed on the all of the PAD pins. The PAD pins carry the physical address during the first clock cycle of a transaction and carry data during the subsequent clock cycles.
90	DGND	GND	Digital core ground
91	VDDC	P	1.2V digital core V_{DD}
92	VDDIO	P	3.3V digital I/O V_{DDI}
93	PAD30	I/O	PCI Address/Data 30
94	PAD29	I/O	PCI Address/Data 29
95	PAD28	I/O	PCI Address/Data 28
96	PAD27	I/O	PCI Address/Data 27
97	PAD26	I/O	PCI Address/Data 26
98	PAD25	I/O	PCI Address/Data 25

TABLE 2-1: SIGNALS (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
99	PAD24	I/O	PCI Address/Data 24
100	PAD23	I/O	PCI Address/Data 23
101	PAD22	I/O	PCI Address/Data 22
102	PAD21	I/O	PCI Address/Data 21
103	PAD20	I/O	PCI Address/Data 20
104	PAD19	I/O	PCI Address/Data 19
105	PAD18	I/O	PCI Address/Data 18
106	PAD17	I/O	PCI Address/Data 17
107	DGND	GND	Digital ground
108	VDDIO	P	3.3V digital I/O V_{DD}
109	PAD16	I/O	PCI Address/Data 16
110	PAD15	I/O	PCI Address/Data 15
111	PAD14	I/O	PCI Address/Data 14
112	PAD13	I/O	PCI Address/Data 13
113	PAD12	I/O	PCI Address/Data 12
114	PAD11	I/O	PCI Address/Data 11
115	PAD10	I/O	PCI Address/Data 10
116	PAD9	I/O	PCI Address/Data 9
117	PAD8	I/O	PCI Address/Data 8
118	PAD7	I/O	PCI Address/Data 7
119	PAD6	I/O	PCI Address/Data 6
120	PAD5	I/O	PCI Address/Data 5
121	PAD4	I/O	PCI Address/Data 4
122	PAD3	I/O	PCI Address/Data 3
123	DGND	GND	Digital IO ground
124	DGND	GND	Digital core ground
125	VDDIO	P	3.3V digital I/O V_{DD}
126	PAD2	I/O	PCI Address/Data 2
127	PAD1	I/O	PCI Address/Data 1
128	PAD0	I/O	PCI Address/Data 0

Note 2-1 P = Power supply; GND = Ground; I = Input; O = Output
I/O = Bi-directional
IPU = Input with internal pull-up.
IPD = Input with internal pull-down.
OPU = Output with internal pull-up.
OPD = Output with internal pull-down.

TABLE 2-2: BALLS DESCRIPTION OF KSZ8842-PMBL

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type
(Note 2-1)</th><th>Description</th></tr>
<tr><td>A8</td><td>TEST_EN</td><td>I</td><td>Test Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>C7</td><td>SCAN_EN</td><td>I</td><td>Scan Test Scan Mux Enable
For normal operation, pull-down this pin to ground.</td></tr>
<tr><td>B7
A7
C6
B6
A6
B5</td><td>P1LED2
P1LED1
P1LED0
P2LED2
P2LED1
P2LED0</td><td>OPU</td><td>Port 1 and Port 2 LED Indicators, defined as follows:
LEDs turn on when low.
<table>
<tr><th></th><th colspan="2">Chip Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0, 0] Default</th><th>[0, 1]</th></tr>
<tr><td>P1LED3 /P2LED3</td><td>—</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link/Activity</td><td>100Link/Activity</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full-Duplex/Col</td><td>10Link/Activity</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>Full-Duplex</td></tr>
</table>
<table>
<tr><th></th><th colspan="2">Reg. SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[1, 0]</th><th>[1, 1]</th></tr>
<tr><td>P1LED3 /P2LED3</td><td>Activity</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>Link</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>Full-Duplex/Col</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>Speed</td><td>—</td></tr>
</table>
Note: Link = On; Activity = Blink; Link/Act = On/Blink; Full-Duplex/Col = On/Blink; Full-Duplex = On (Full-duplex); Off (Half-duplex); Speed = On (100BASE-T); Off (10BASE-T)
Note: P1LED3 is pin 27. P2LED3 is pin 22.
Port 1 and Port 2 LED indicators1 for Repeater mode defined as follows:
<table>
<tr><th></th><th colspan="2">Switch Global Control Register 5: SGCR5 bit [15,9]</th></tr>
<tr><th></th><th>[0,0] Default</th><th>[0,1] [1,0],[1,1]</th></tr>
<tr><td>P1LED3/P2LED3</td><td>RPT_COL,
RPT_ACT</td><td>—</td></tr>
<tr><td>P1LED2/P2LED2</td><td>RPT_Link3/RX,
RPT_ERR3</td><td>—</td></tr>
<tr><td>P1LED1/P2LED1</td><td>RPT_Link2/RX,
RPT_ERR2</td><td>—</td></tr>
<tr><td>P1LED0/P2LED0</td><td>RPT_Link1/RX,
RPT_ERR1</td><td>—</td></tr>
</table>
Note: RPT_COL = Blink; RPT_Link3/RX (Host Port) = On/Blink; RPT_Link2/RX (Port 2) = On/Blink; RPT_Link1/RX (Port 1) = On/Blink; RPT_ACT = On if any activity; RPT_ERR3 (Host port) = On if any CRC error; RPT_ERR2 (Port 2) = On if any CRC error; RPT_ERR1 (Port 1) = On if any CRC error</td></tr>
<tr><td>A5</td><td>PCLK</td><td>IPD</td><td>PCI Bus Clock. This Clock provides the timing for all PCI bus phases. The rising edge defines the start of each phase. The clock maximum frequency is 33 MHz.</td></tr>
</table>

TABLE 2-2: BALLS DESCRIPTION OF KSZ8842-PMBL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
B4	INTRN	OPD	Interrupt Request. Active Low signal to host CPU to request an interrupt when any one of the interrupt conditions occurs in the registers. This pin should be pull-up externally.
A4	EECS	OPU	EEPROM Chip Select. This signal is used to select an external EEPROM device.
C3	P2LED3	OPD	Port 2 LED Indicator See the description in ball B5, B6 and A6.
A3	EEEN	IPD	EEPROM Enable EEPROM is enabled and connected when this pin is pull-up. EEPROM is disabled when this pin is pull-down or no connect.
B3	P1LED3	OPD	Port 1 LED indicator See the description in ball C7, A7 and B7.
B2	EEDO	OPD	No connect EEPROM Data Out: This pin is connected to DI input of the serial EEPROM.
A2	EESK	OPD	EEPROM Serial Clock: A 4 µs serial output clock to load configuration data from the serial EEPROM.
A1	EEDI	IPD	EEPROM Data In: This pin is connected to DO output of the serial EEPROM.
B1	PWRDN	IPU	Full-chip power-down. Active Low.
C1	RXP1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (+ differential)
C2	RXM1	I/O	Port 1 physical receive (MDI) or transmit (MDIX) signal (– differential)
D1	TXP1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (+ differential)
D2	TXM1	I/O	Port 1 physical transmit (MDI) or receive (MDIX) signal (– differential)
F2	RXM2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (– differential)
F1	RXP2	I/O	Port 2 physical receive (MDI) or transmit (MDIX) signal (+ differential)
G2	TXM2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (– differential)
G1	TXP2	I/O	Port 2 physical transmit (MDI) or receive (MDIX) signal (– differential)
G3	ISET	O	Set physical transmit output current. Pull-down this ball with a 3.01 kΩ 1% resistor.
H1	X1	I	25 MHz crystal/oscillator clock connections Balls (X1, X2) connect to a crystal. If an oscillator is used, X1 connects to a 3.3V tolerant oscillator and X2 is a no connect. Note: Clock is ±50 ppm for both crystal and oscillator.
H2	X2	O	
J1	RSTN	IPU	Hardware Reset, Active Low RSTN will cause the KSZ8842-PMBL to reset all of its functional blocks. RSTN must be asserted for a minimum duration of 10 ms.
J2	PAR	O	PCI Parity Even parity computed for PAD [31:0] and CBE[3:0]N, master drives PAR for address and write data phase, target drives PAR for read data phase.
K1	FRAMEN	I/O	PCI Cycle Frame This signal is asserted low to indicate the beginning of the address phase of the bus transaction and de-asserted before the final transfer of the data phase of the transaction in a bus master mode. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.

TABLE 2-2: BALLS DESCRIPTION OF KSZ8842-PMBL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
K2	IRDYN	I/O	PCI Initiator Ready As a bus master, this signal is asserted low to indicate valid data phases on PAD [31:0] during write data phases, indicates it is ready to accept data during read data phases. As a target, it'll monitor this IRDYN signal that indicates the master has put the data on the bus.
H3	TRDYN	I/O	PCI Target Ready As a bus target, this signal is asserted low to indicate valid data phases on PAD [31:0] during read data phases, indicating it is ready to accept data during write data phases. As a master, it will monitor this TRDYN signal that indicates the target is ready for data during read/write operation.
J3	STOPN	I/O	PCI Stop This signal is asserted low by the target device to stop the current transaction.
K3	IDSEL	I/O	PCI Initialization Device Select. This signal is used to select the KSZ8842-PMQL/PMBL during configuration read and write transactions.
H4	DEVSELN	I/O	PCI Device Select This signal is asserted low when it is selected as a target during a bus transaction. As a bus master, the KSZ8842-PMBL samples this signal to insure that the destination address for the data transfer is recognized by a PCI target.
J4	REQN	O	PCI Request The KSZ8842-PMBL will assert this signal low to request PCI bus master operation.
K4	GNTN	I	PCI Grant This signal is asserted low to indicate to the KSZ8842-PMBL that it has been granted the PCI bus master operation.
H5	PERRN	I/O	PCI Parity Error The KSZ8842-PMBL as a master or target will assert this signal low to indicate a parity error on any incoming data. As a bus master, it will monitor this signal on all write operations.
J5	SERRN	O	PCI System Error This system error signal is asserted low by the KSZ8842-PMBL.This signal is used to report address parity errors.
K5	CBE3N	I	Command and Byte Enable These signals are multiplexed on the same PCI pins. During the address phase, these lines define the bus command. During the data phase, these lines are used as Byte Enables. The Byte enables are valid for the entire data phase and determine which byte lanes carry meaningful.
K6	CBE2N	I	
J6	CBE1N	I	
H6	CBE0N	I	
K7	PAD31	I/O	PCI Address / Data 31 Address and data are multiplexed on the all of the PAD balls. The PAD pins carry the physical address during the first clock cycle of a transaction, and carry data during the subsequent clock cycles.
J7	PAD30	I/O	PCI Address / Data 30
H7	PAD29	I/O	PCI Address / Data 29
K8	PAD28	I/O	PCI Address / Data 28
J8	PAD27	I/O	PCI Address / Data 27
H8	PAD26	I/O	PCI Address / Data 26
K9	PAD25	I/O	PCI Address / Data 25

TABLE 2-2: BALLS DESCRIPTION OF KSZ8842-PMBL (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Description
J9	PAD24	I/O	PCI Address / Data 24
K10	PAD23	I/O	PCI Address / Data 23
J10	PAD22	I/O	PCI Address / Data 22
H9	PAD21	I/O	PCI Address / Data 21
H10	PAD20	I/O	PCI Address / Data 20
G8	PAD19	I/O	PCI Address / Data 19
G9	PAD18	I/O	PCI Address / Data 18
G10	PAD17	I/O	PCI Address / Data 17
F8	PAD16	I/O	PCI Address / Data 16
F9	PAD15	I/O	PCI Address / Data 15
F10	PAD14	I/O	PCI Address / Data 14
E8	PAD13	I/O	PCI Address / Data 13
E9	PAD12	I/O	PCI Address / Data 12
E10	PAD11	I/O	PCI Address / Data 11
D10	PAD10	I/O	PCI Address / Data 10
D9	PAD9	I/O	PCI Address / Data 9
D8	PAD8	I/O	PCI Address / Data 8
C10	PAD7	I/O	PCI Address / Data 7
C9	PAD6	I/O	PCI Address / Data 6
C8	PAD5	I/O	PCI Address / Data 5
B10	PAD4	I/O	PCI Address / Data 4
B9	PAD3	I/O	PCI Address / Data 3
B8	PAD2	I/O	PCI Address / Data 2
A10	PAD1	I/O	PCI Address / Data 1
A9	PAD0	I/O	PCI Address / Data 0
C5	VDDC	P	1.2V digital core V_{DD}
C4	VDDCO	P	1.2V Core Voltage Output. (internal 1.2V LDO power supply output) This ball is used to provide 1.2V power supply to all 1.2V power VDDC and VDDA. It is recommended the ball should be connected to 3.3V power rail by a 100Ω resistor for the internal LDO application. The 100Ω resistor is for Rev A6 and should no longer be fitted for latest Rev A7.
D3, E3, F3	VDDA	P	1.2V analog V_{DD}
D7, E7, F7, G4, G5, G6, G7	VDDIO	P	3.3V digital I/O V_{DD}
E1	VDDATX	P	3.3V analog V_{DD}
E2	VDDARX	P	3.3V analog VDD
D4, D5, D6, E4, E5, E6, F4, F5, F6	GND	GND	Ground

P = Power supply; GND = Ground; I = Input; O = Output
I/O = Bi-directional
IPU = Input with internal pull-up.
IPD = Input with internal pull-down.
OPU = Output with internal pull-up.
OPD = Output with internal pull-down.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8842-PMQL/PMBL contains one PCI interface unit, two 10/100 physical layer transceivers (PHYs), three MAC units, and a RX/TX DMA channel all integrated with a Layer-2 switch.

Physical signal transmission and reception are enhanced through the use of analog circuits in the PHY that make the design more efficient and allow for low power consumption.

3.1 PCI Bus Interface Unit

3.1.1 PCI BUS INTERFACE

The PCI Bus Interface implements PCI v2.2 bus protocols and configuration space. The KSZ8842-PMQL/PMBL supports bus master reads and writes to CPU memory, and CPU access to on-chip register space. When the CPU reads and writes the configuration registers of the KSZ8842-PMQL/PMBL, it is as a slave. So the KSZ8842-PMQL/PMBL can be either a PCI bus master or slave. The PCI Bus Interface is also responsible for managing the DMA interfaces and the host processors access. Arbitration logic within the PCI Bus Interface unit accepts bus requests from the TXDMA logic and RXDMA logic.

The PCI bus interface also manages interrupt generation for a host processor.

3.1.2 TXDMA LOGIC AND TX BUFFER MANAGER

The KSZ8842-PMQL/PMBL supports a multi-frame, multi-fragment DMA gather process. Descriptors representing frames are built and linked in system memory by a host processor. The TXDMA logic is responsible for transferring the multi-fragment frame data from the host memory into the TX buffer.

The KSZ8842-PMQL/PMBL uses 4K bytes of transmit data buffer between the TXDMA logic and transmit MAC. When the TXDMA logic determines there is enough space available in the TX buffer, the TXDMA logic will move any pending frame data into the TX buffer. The management mechanism depends on the transmit descriptor list.

3.1.3 RXDMA LOGIC AND RX BUFFER MANAGER

The KSZ8842-PMQL/PMBL supports a multi-frame, multi-fragment DMA scatter process. Descriptors representing frames are built and linked in system memory by the host processor. The RXDMA logic is responsible for transferring the frame data from the RX buffer to the host memory.

The KSZ8842-PMQL/PMBL uses 4K bytes of receive data buffer between the receive MAC and RXDMA logic. The management mechanism depends on the receive descriptor list.

3.2 Physical Layer Transceiver (PHY)

3.2.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external1% 3.01 kΩ resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

3.2.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer has to adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to an MII format and provided as the input data to the MAC.

3.2.3 PLL CLOCK SYNTHESIZER (RECOVERY)

The internal PLL clock synthesizer generates 125 MHz, 62.5 MHz, 41.66 MHz, and 25 MHz clocks by setting the on-chip bus speed control register OBCR for KSZ8842-PMQL/PMBL system timing. These internal clocks are generated from an external 25 MHz crystal or oscillator.

Note that the default setting is 25 MHz in the OBCR register; it is recommended that the software driver set it to 125 MHz for best performance.

3.2.4 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander.

Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence. Then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

3.2.5 10BASE-T TRANSMIT

The 10BASE-T driver is incorporated with the 100BASE-TX driver to allow for transmission using the same magnetic. They are internally wave-shaped and pre-emphasized into outputs with typical 2.3V amplitude. The harmonic contents are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.2.6 10BASE-T RECEIVE

On the receive side, input buffers and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RXP-or-RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8842-PMQL/PMBL decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

3.3 Power Management

The KSZ8842-PMQL/PMBL features a per port power-down mode. To save power, the user can power-down a port that is not in use by setting bit 11 in either P1CR4 or P1MBCR register for port 1, and set bit 11 in either P2CR4 or P2MBCR register for port 2. To bring the port back up, reset bit 11 in these registers.

In addition, there is a full chip power-down mode by pulling down the PWRDN pin/ball 36. When this pin is pulled down, the entire chip powers down. Transitioning this pin from pull-down to pull-up results in a power up and chip reset.

3.3.1 MDI/MDI-X AUTO CROSSOVER

To eliminate the need for crossover cables between similar devices, the KSZ8841-PMQL supports HP-Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP-Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns the transmit and receive pairs for the KSZ8841-PMQL device. This feature is extremely useful when end users are unaware of cable types in addition to saving on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers.

The IEEE 802.3u standard MDI and MDI-X definitions are illustrated in Table 3-1.

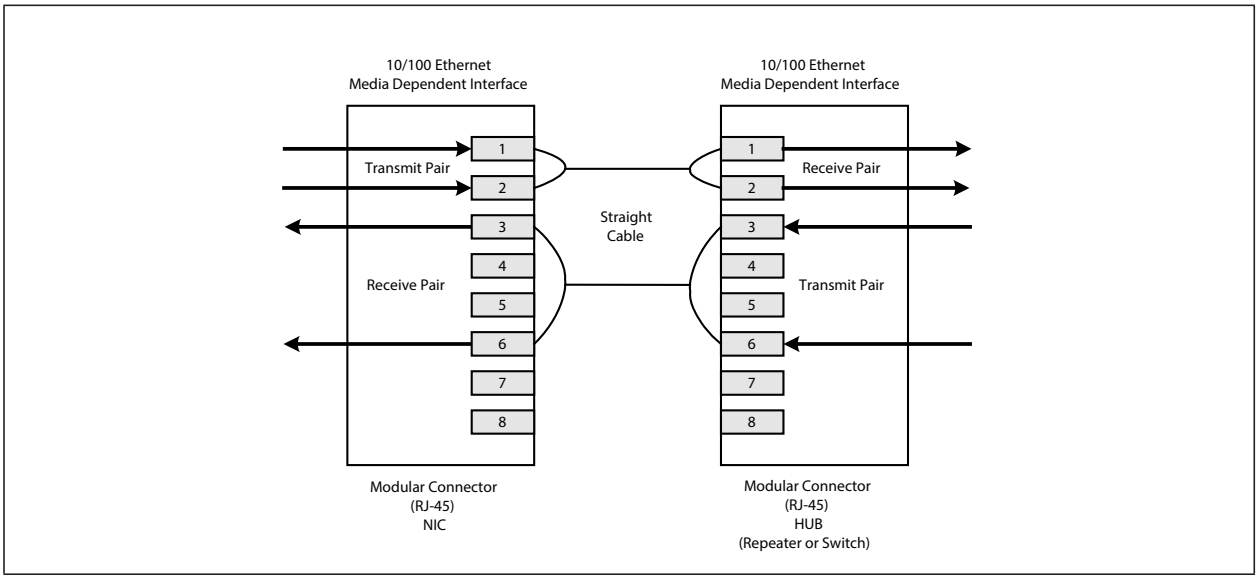
TABLE 3-1: MDI/MDI-X PIN DEFINITIONS

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.3.1.1 Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-1 depicts a typical straight cable connection between a NIC card (MDI) and a switch or hub (MDI-X).

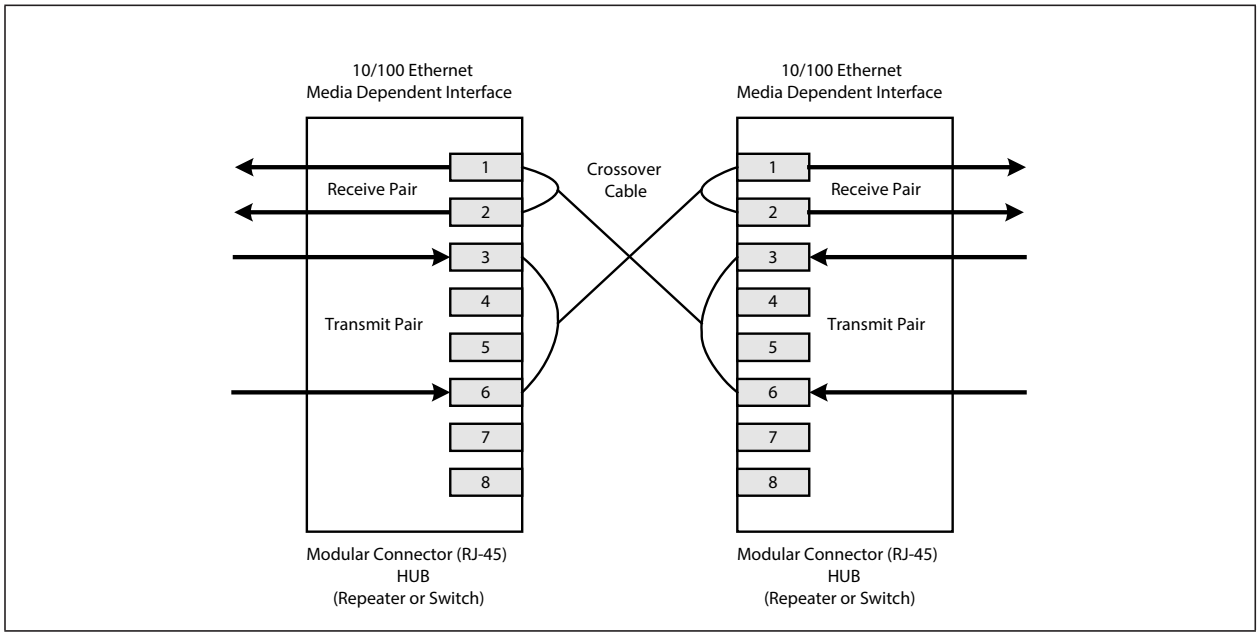
FIGURE 3-1: TYPICAL STRAIGHT CABLE CONNECTION



3.3.1.2 Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 3-2 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-2: TYPICAL CROSSOVER CABLE CONNECTION



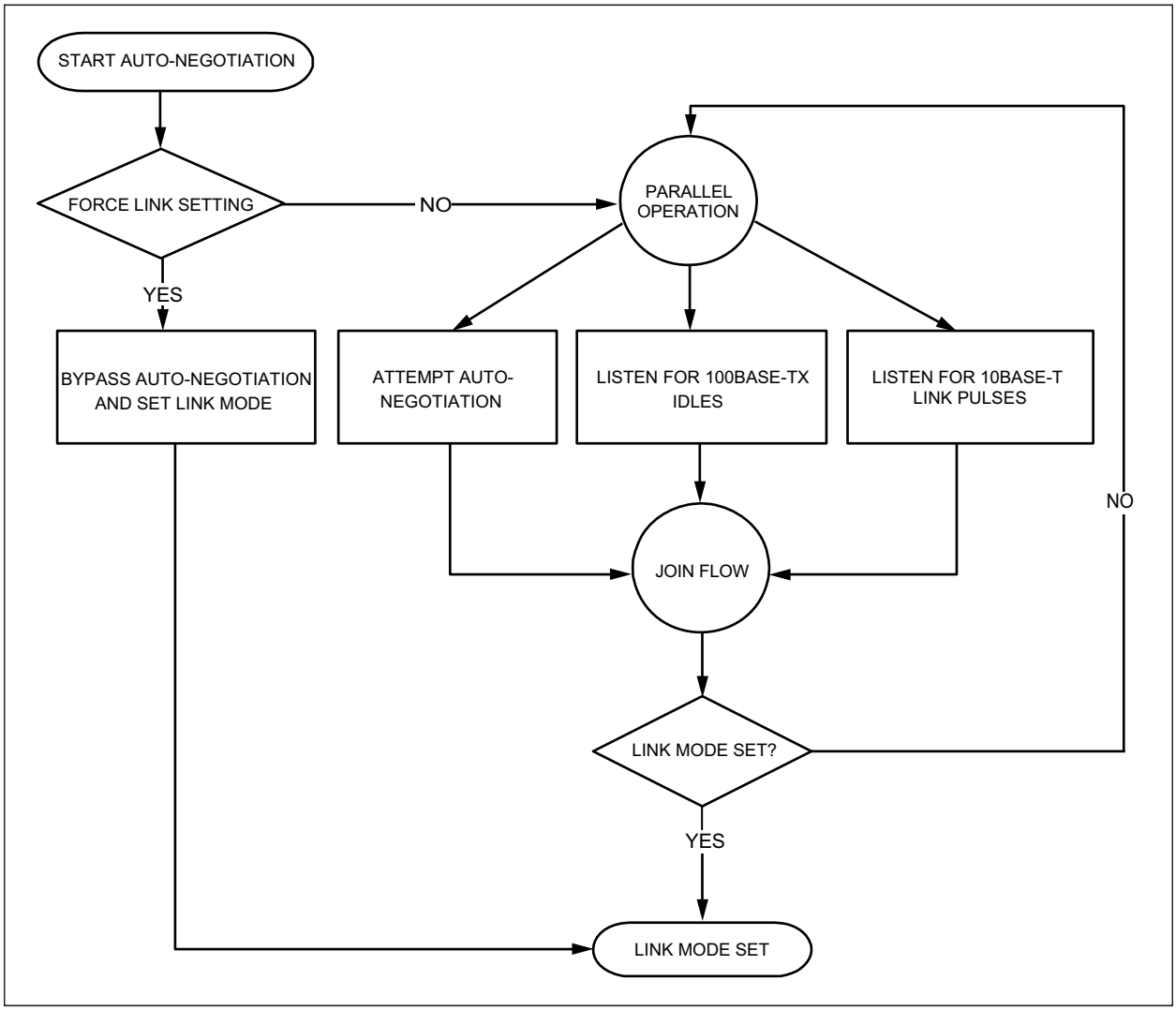
3.3.2 AUTO-NEGOTIATION

The KSZ8842-PMQL/PMBL confirms to the auto negotiation protocol as described by the 802.3 committee to allow the port to operate at either 10BASE-T or 100BASE-TX.

Auto negotiation allows unshielded twisted pair (UTP) link partners to select the best common mode of operation. In auto negotiation, the link partners advertise capabilities across the link to each other. If auto negotiation is not supported or the link partner to the KSZ8842-PMQL/PMBL is forced to bypass auto negotiation, the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The link setup process is shown in Figure 3-3.

FIGURE 3-3: AUTO-NEGOTIATION AND PARALLEL OPERATION



3.3.3 LINKMD® CABLE DIAGNOSTICS

The KSZ8842-PMQL/PMBL LinkMD® uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with a maximum distance of 200m and an accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format.

Note that cable diagnostics are only valid for copper connections. Fiber-optic operation is not supported.

3.3.3.1 Access

LinkMD is initiated by accessing register P1VCT, the LinkMD Control/Status register, in conjunction with register P1CR4, the 100BASE-TX PHY Controller register.

3.3.3.2 Usage

LinkMD can be run at any time. To use LinkMD, disable HP Auto-MDIX by writing a ‘1’ to P1CR4[10] to enable manual control over the pair used to transmit the LinkMD pulse. The self-clearing cable diagnostic test enable bit, P1VCT[15], is set to ‘1’ to start the test on this pair.

When bit P1VCT[15] returns to ‘0’, the test is complete. The test result is returned in bits P1VCT[14:13] and the distance is returned in bits P1VCT[8:0]. The cable diagnostic test results are as follows:

00 = Valid test, normal condition

01 = Valid test, open circuit in cable

10 = Valid test, short circuit in cable

11 = Invalid test, LinkMD failed

If P1VCT[14:13] =11, this indicates an invalid test, and occurs when the KSZ8841-PMQL is unable to shut down the link partner. In this instance, the test is not run, as it is not possible for the KSZ8841-PMQL to determine if the detected signal is a reflection of the signal generated or a signal from another source.

Cable distance can be approximated by the following formula:

Distance = P1VCT[8:0] x 0.4m

This constant may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

3.4 Media Access Control (MAC) and Switch

3.4.1 ADDRESS LOOKUP

The internal lookup table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information.

The KSZ8842-PMQL/PMBL is guaranteed to learn 1K addresses and distinguishes itself from hash-based lookup tables, which depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

3.4.2 LEARNING

The internal lookup engine updates its table with a new entry if the following conditions are met:

a) The received packet's Source Address (SA) does not exist in the lookup table.
b) The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted to make room for the new entry.

3.4.3 MIGRATION

The internal lookup engine also monitors whether a station has moved. If a station has moved, it updates the table accordingly. Migration happens when the following conditions are met:

a) The received packet's SA is in the table but the associated source port information is different.

b) The received packet is good; the packet has no receiving errors, and is of legal length.

The lookup engine updates the existing record in the table with the new source port information.

3.4.4 AGING

The lookup engine updates the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the lookup engine removes the record from the table. The lookup engine constantly performs the aging process and continuously removes aging records. The aging period is about 200 seconds. This feature can be enabled or disabled through Global Register SGCR1[10]).

3.4.5 FORWARDING

The KSZ8842-PMQL/PMBL forwards packets using the algorithm that is depicted in the following flowcharts. Figure 7 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 3-4. The packet is sent to PTF2.

FIGURE 3-4: DESTINATION ADDRESS LOOKUP FLOW CHART IN STAGE ONE

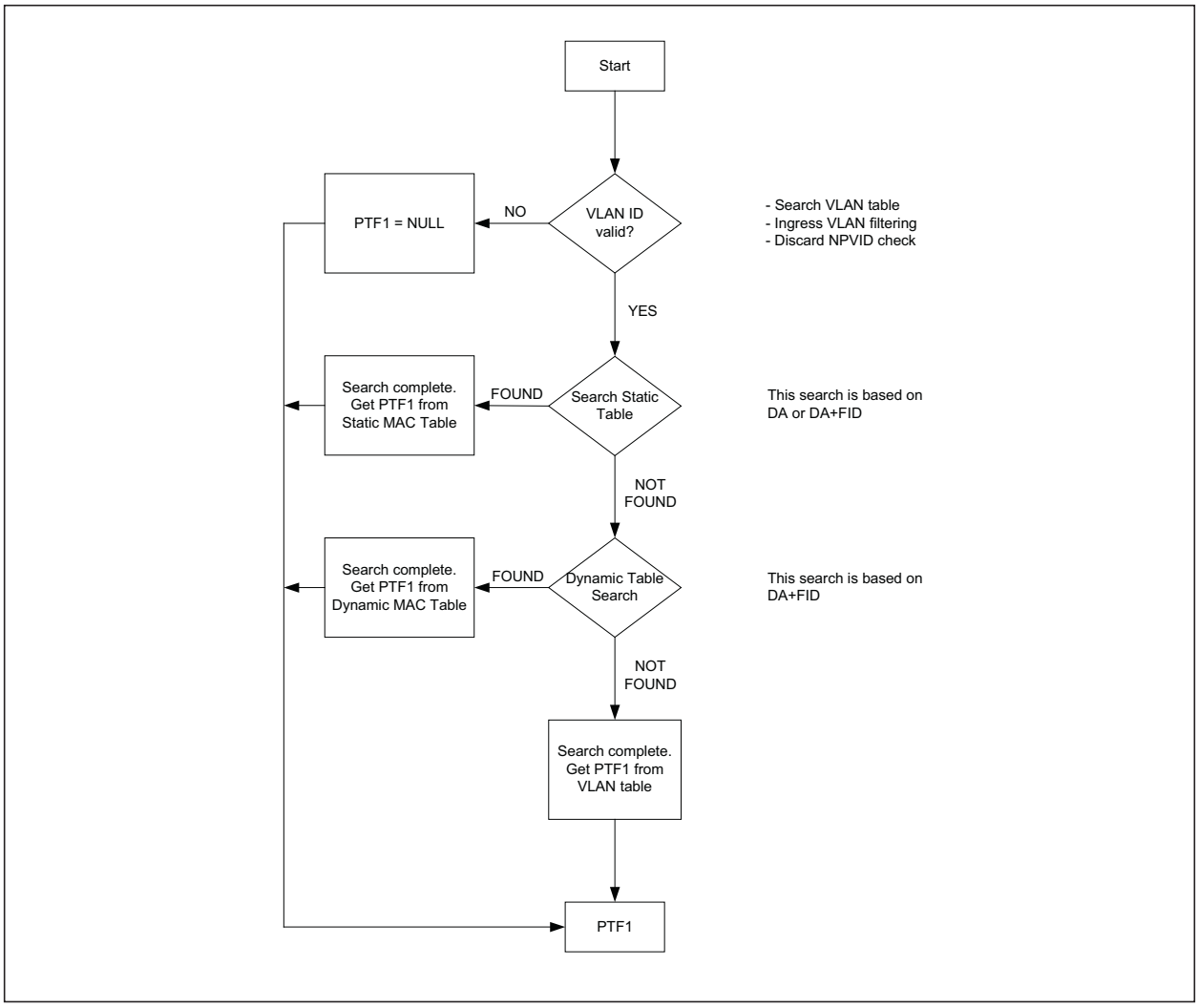
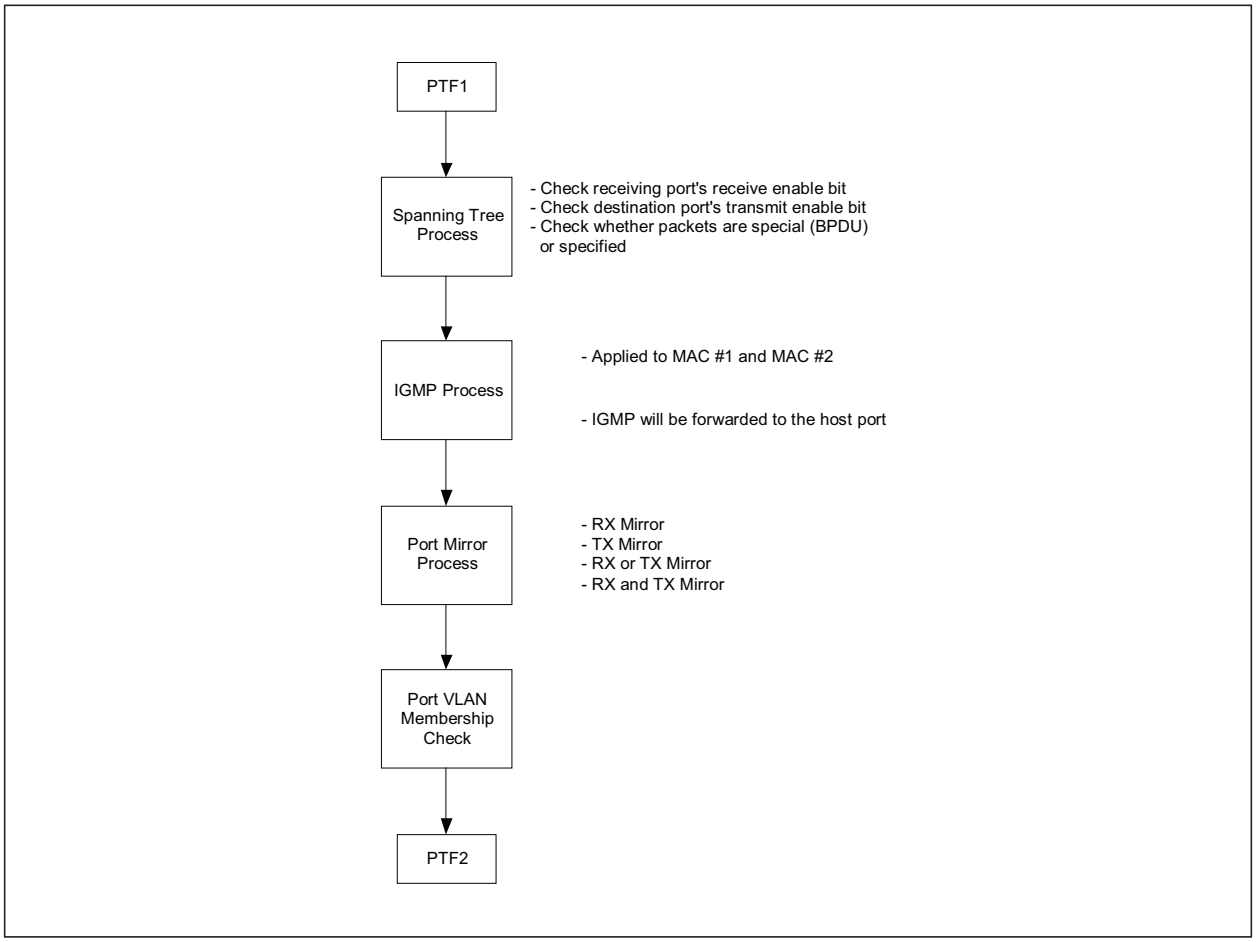


FIGURE 3-5: DESTINATION ADDRESS RESOLUTION FLOW CHART IN STAGE TWO



The KSZ8842-PMQL/PMBL will not forward the following packets:

- Error packets.

These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.

- 802.3x pause frames.

The KSZ8842-PMQL/PMBL intercepts these packets and performs the flow control.

- Local packets.

Based on destination address (DA) look-up. If the destination port from the lookup table matches the port from which the packet originated, the packet is defined as local.

3.4.6 SWITCHING ENGINE

The KSZ8842-PMQL/PMBL features a high-performance switching engine to move data to and from the MAC's packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The switching engine has a 32 KB internal frame buffer. This resource is shared between all the ports. There are a total of 256 buffers available. Each buffer is sized at 128B.

3.4.7 MAC OPERATION

The KSZ8842-PMQL/PMBL strictly abides by IEEE 802.3 standards to maximize compatibility. Additionally, there is an added MAC filtering function to filter Unicast packets. The MAC filtering function is useful in applications such as VoIP where restricting certain packets reduces congestion and thus improves performance.

3.4.8 INTER PACKET GAP (IPG)

If a frame is successfully transmitted, the minimum 96-bit time for IPG is measured between two consecutive packets. If the current packet is experiencing collisions, then the minimum 96-bit time for IPG is measured from carrier sense (CRS) to the next transmit packet.

3.4.9 BACK-OFF ALGORITHM

The KSZ8842-PMQL/PMBL implements the IEEE standard 802.3 binary exponential back-off algorithm in half-duplex mode, and optional aggressive mode back-off. After 16 collisions, the packet is optionally dropped depending upon the switch configuration in SGCR1 [8].

3.4.10 LATE COLLISION

If a transmit packet experiences collisions after 512 bit times of the transmission, then the packet is dropped.

3.4.11 LEGAL PACKET SIZE

The KSZ8842-PMQL/PMBL discards packets less than 64 bytes and can be programmed to accept packet size up to 1536 bytes in SGCR2 [1]. The KSZ8842-PMQL/PMBL can also be programmed for special applications to accept packet size up to 1916 bytes in SGCR2 [2].

3.4.12 FLOW CONTROL

The KSZ8842-PMQL/PMBL supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KSZ8842-PMQL/PMBL receives a pause control frame, the KSZ8862M will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (while it is flow controlled), only flow control packets from the KSZ8842-PMQL/PMBL are transmitted.

On the transmit side, the KSZ8842-PMQL/PMBL has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues, and available receive queues.

The KSZ8842-PMQL/PMBL will flow control a port that has just received a packet if the destination port resource is busy. The KSZ8842-PMQL/PMBL issues a flow control frame (XON), containing the maximum pause time as defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8842-PMQL/PMBL then sends out the other flow control frame (Xon) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is provided to prevent the flow control mechanism from being constantly activated and deactivated.

3.4.13 HALF-DUPLEX BACKPRESSURE

A half-duplex backpressure option (not in IEEE 802.3 standards) is also provided. The activation and deactivation conditions are the same in full-duplex mode. If backpressure is required, then the KSZ8842-PMQL/PMBL sends preambles to defer the other stations' transmission (carrier sense deference).

To avoid jabber and excessive deference (as defined in the 802.3 standard), after a certain time, the KSZ8862M discontinues the carrier sense and then raises it again quickly. This short silent time (no carrier sense) prevents other stations from sending out packets thus keeping other stations in a carrier sense deferred state. If the port has packets to send during a backpressure situation, then the carrier sense type backpressure is interrupted and those packets are transmitted instead. If there are no additional packets to send, then the carrier sense type backpressure is reactivated again until switch resources free up. If a collision occurs, then the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, thus reducing the chance of further collisions and carrier sense is maintained to prevent packet reception.

To ensure no packet loss in 10 BASE-T or 100 BASE-TX half-duplex modes, the user must enable the following:

a) Aggressive back off (bit 8 in SGCR1)
b) No excessive collision drop (bit 3 in SGCR2)

Note: These bits are not set in default, since this is not the IEEE standard.

3.4.14 BROADCAST STORM PROTECTION

The KSZ8862M has an intelligent option to protect the switch system from receiving too many broadcast packets. As the broadcast packets are forwarded to all ports except the source port, an excessive number of switch resources (bandwidth and available space in transmit queues) may be utilized. The KSZ8842-PMQL/PMBL has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally, and can be

enabled or disabled on a per port basis in P1CR1 [7] and P2CR1 [7]. The rate is based on a 67ms interval for 100BT and a 670ms interval for 10BT. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in SGCR3 [2:0] [15:8]. The default setting is 0x63 (99 decimal). This is equal to a rate of 1%, calculated as follows:

148,800 frames/sec x 67 ms/interval x 1% = 99 frames/interval (approx.) = 0 x 63

Note: 148,800 frames/sec is based on 64-byte block of packets in 100BASE-T with 12 bytes of IPG and 8 bytes of preamble between two packets.

3.4.15 REPEATER MODE

When KSZ8842-PMQL/PMBL is set to repeater mode (SGCR3[7] = 1), it only works on 100BT half-duplex mode. In repeater enabled mode, all ingress packets will broadcast to other two ports without MAC check and learning. Before setting the device to repeater mode, the user has to set bit 13 (100 Mbps), bit 12 (auto-negotiation disabled) and bit 8 (half duplex) in both P1MBCR and P2MBCR registers as well as to set bit 6 (host half duplex) in SGCR3 register for repeater mode.

The latency in repeater mode is defined from the 1st bit of DA into the ingress port 1 to the 1st bit of DA out of the egress port 2. The minimum is 270 ns and the maximum is 310 ns (one clock skew of 25 MHz between TX and RX).

3.4.16 CLOCK GENERATOR

The X1 and X2 pins are connected to a 25 MHz crystal. X1 can also serve as the connector to a 3.3V, 25 MHz oscillator (as described in the pin/ ball description). The PCI Bus Interface supports a maximum speed of 33 MHz PCLK (PCI Bus Clock).

3.5 Advanced Switch Functions

3.5.1 SPANNING TREE SUPPORT

To support spanning tree, the host port is the designated port for the processor.

The other ports can be configured in one of the five spanning tree states via “transmit enable”, “receive enable” and “learning disable” register settings in registers P1CR2 and P2CR2 for ports 1 and 2, respectively. Table 3-2 shows the port setting and software actions taken for each of the five spanning tree states.

TABLE 3-2: SPANNING TREE STATES

State	Port Setting	Software Action
Disable State: The port should not forward or receive any packets. Learning is disabled.	Transmit enable = “0”, Receive enable = “0”, Learning disable = “1”	The processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the Static MAC Address Table with “overriding bit” set) and the processor should discard those packets. Address learning is disabled on the port in this state.
Blocking State: Only packets to the processor are forwarded.	Transmit enable = “0”, Receive enable = “0”, Learning disable = “1”	The processor should not send any packets to the port(s) in this state. The processor should program the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.
Listening State: Only packets to and from the processor are forwarded. Learning is disabled.	Transmit enable = “0”, Receive enable = “0”, Learning disable = “1”	The processor should program the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is disabled on the port in this state.

TABLE 3-2: SPANNING TREE STATES

State	Port Setting	Software Action
Learning State: Only packets to and from the processor are forwarded. Learning is enabled.	Transmit enable = “0”, Receive enable = “0”, Learning disable = “0”	The processor should program the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state. Address learning is enabled on the port in this state.
Forwarding State Packets are forwarded and received normally. Learning is enabled.	Transmit enable = “1”, Receive enable = “1”, Learning disable = “0”	The processor programs the Static MAC Address Table with the entries that it needs to receive (for example, BPDU packets). The “overriding” bit is set so that the switch forwards those specific packets to the processor. The processor can send packets to the port(s) in this state. Address learning is enabled on the port in this state.

3.5.2 IGMP SUPPORT

For Internet Group Management Protocol (IGMP) support in Layer 2, the KSZ8842-PMQL/PMBL provides two components:

3.5.2.1 “IGMP” Snooping

The KSZ8842-PMQL/PMBL traps IGMP packets and forwards them only to the processor (host port). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2.

3.5.2.2 “Multicast Address Insertion” in the Static MAC Table

Once the multicast address is programmed in the Static MAC Table, the multicast session is trimmed to the subscribed ports, instead of broadcasting to all ports.

3.5.2.3 IPv6 MLD Snooping

The KSZ8842-PMQL/PMBL traps IPv6 Multicast Listener Discovery (MLD) packets and forwards them only to the processor (host port). MLD snooping is controlled by SGCR2 [13] (MLD snooping enable) and SGCR2 [12] (MLD option).

Setting SGCR2 [13] causes the KSZ8842-PMQL/PMBL to trap packets that meet all of the following conditions:

- IPv6 multicast packets
- Hop count limit = 1
- IPv6 next header = 1 or 58 (or = 0 with hop-by-hop next header = 1 or 58)
- If SGCR2[12] = 1, IPv6 next header = 43, 44, 50, 51, or 60 (or = 0 with hop-by-hop next header = 43, 44, 50, 51, or 60)

3.5.3 PORT MIRRORING SUPPORT

KSZ8842-PMQL/PMBL supports “Port Mirroring” comprehensively as:

3.5.3.1 “Receive Only” Mirror on a Port

All the packets received on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “receive sniff” and the host port is programmed to be the “sniffer port”. A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8842-PMQL/PMBL forwards the packet to both port 2 and the host port. The KSZ8842-PMQL/PMBL can optionally even forward “bad” received packets to the “sniffer port”.

3.5.3.2 “Transmit Only” Mirror on a Port

All the packets transmitted on the port are mirrored on the sniffer port. For example, port 1 is programmed to be “transmit sniff” and the host port is programmed to be the “sniffer port”. A packet received on port 2 is destined to port 1 after the internal lookup. The KSZ8842-PMQL/PMBL forwards the packet to both port 1 and the host port.

3.5.3.3 "Receive and Transmit Mirror" on Two Ports

All the packets received on port A and transmitted on port B are mirrored on the sniffer port. To turn on the "AND" feature, set register SGCR2, bit 8 to "1". For example, port 1 is programmed to be "receive sniff", port 2 is programmed to be "transmit sniff", and the host port is programmed to be the "sniffer port". A packet received on port 1 is destined to port 2 after the internal lookup. The KSZ8842-PMQL/PMBL forwards the packet to both port 2 and the host port.

Multiple ports can be selected as "receive sniff" or "transmit sniff". In addition, any port can be selected as the "sniffer port". All these per port features can be selected through registers P1CR2, P2CR2, and P3CR2 for ports 1, 2, and the host port, respectively.

3.6 IEEE 802.1Q VLAN Support

The KSZ8842-PMQL/PMBL supports 16 active VLANs out of the 4096 possible VLANs specified in the IEEE 802.1Q specification. KSZ8842-PMQL/PMBL provides a 16-entry VLAN table, which converts the 12-bits VLAN ID (VID) to the 4-bits Filter ID (FID) for address lookup. If a non-tagged or null-VID-tagged packet is received, the ingress port default VID is used for lookup. In VLAN mode, the lookup process starts with VLAN table lookup to determine whether the VID is valid. If the VID is not valid, the packet is dropped and its address is not learned. If the VID is valid, the FID is retrieved for further lookup. The FID + Destination Address (FID+DA) are used to determine the destination port. The FID + Source Address (FID+SA) are used for address learning (see Table 3-3 and Table 3-4).

TABLE 3-3: FID + DA LOOKUP IN VLAN MODE

DA Found in Static MAC Table	Use FID Flag	FID Match	DA+FID Found in Dynamic MAC Table	Action
No	Don't Care	Don't Care	No	Broadcast to the membership ports defined in the VLAN Table bits [18:16]
No	Don't Care	Don't Care	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	0	Don't Care	Don't Care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN Table bits KSZ8841PMQL/PMBL
Yes	1	No	Yes	Send to the destination port defined in the Dynamic MAC Address Table bits [53:52]
Yes	1	Yes	Don't Care	Send to the destination port(s) defined in the Static MAC Address Table bits [50:48]

TABLE 3-4: FID + SA LOOKUP IN VLAN MODE

FID+SA Found in Dynamic MAC Table	Action
No	Learn and add FID+SA to the Dynamic MAC Address Table
Yes	Update time stamp

3.7 QoS Priority Support

The KSZ8842-PMQL/PMBL provides Quality of Service (QoS) for applications such as VoIP and video conferencing. Offering four priority queues per port, the per-port transmit queue can be split into four priority queues: Queue 3 is the highest priority queue and Queue 0 is the lowest priority queue. Bit 0 of registers P1CR1, P2CR1, and P3CR1 is used to enable split transmit queues for ports 1, 2, and the host port, respectively.

3.7.1 PORT-BASED PRIORITY

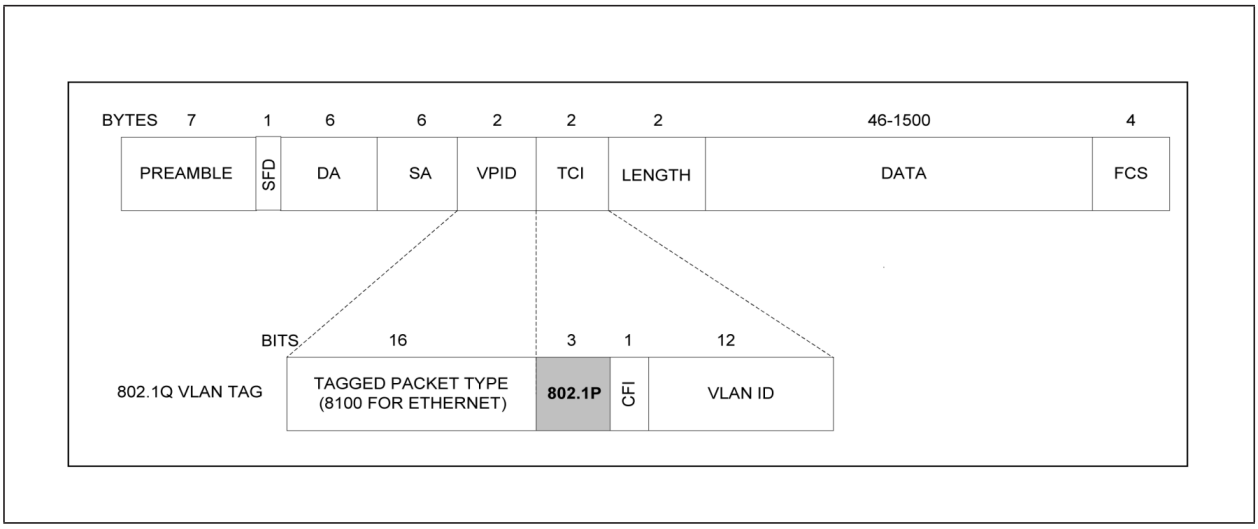
With port-based priority, each ingress port is individually classified as a specific priority level. All packets received at the high-priority receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. Bits[4:3] of registers P1CR1, P2CR1, and P3CR1 is used to enable port-based priority for Ports 1, 2, and the host port, respectively.

3.7.2 802.1P-BASED PRIORITY

For 802.1p-based priority, the KSZ8842-PMQL/PMBL examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and used to look up the “priority mapping” value, as specified by the register SGCR6. The “priority mapping” value is programmable.

Figure 3-6 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

FIGURE 3-6: 802.1P PRIORITY FIELD FORMAT



802.1p based priority is enabled by bit[5]of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively.

The KSZ8842-PMQL/PMBL provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the 2 bytes VLAN protocol ID (VPID) and the 2 bytes tag control information field (TCI), is also referred to as the 802.1Q VLAN tag.

Tag insertion is enabled by bit [2] of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively. At the egress port, untagged packets are tagged with the ingress port’s default tag. The default tags are programmed in register sets P1VIDCR, P2VIDCR, and P3VIDCR for Ports 1, 2, and the host port, respectively. The KSZ8852 does not add tags to already tagged packets.

Tag removal is enabled by bit [1] of registers P1CR1, P2CR1, and P3CR1 for Ports 1, 2, and the host port, respectively. At the egress port, tagged packets will have their 802.1Q VLAN Tags removed. The KSZ8852 will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

3.7.3 802.1P PRIORITY FIELD RE-MAPPING

This is a QoS feature that allows the KSZ8862M to set the “user priority ceiling” at any ingress port. If the ingress packet’s priority field has a higher priority value than the default tag’s priority field of the ingress port, the packet’s priority field is replaced with the default tag’s priority field. The “user priority ceiling” is enabled by bit[3] of registers P1CR2, P2CR2, and P3CR2 for Ports 1, 2, and the host port, respectively.

3.7.4 DIFFSERV-BASED PRIORITY

DiffServ-based priority uses the ToS registers shown in the Type-of-Service (ToS) Priority Control Registers section. The ToS priority control registers implement a fully-decoded, 128-bit differentiated services code point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant 6 bits of the ToS field are fully decoded, the resultant of the 64 possibilities is compared with the corresponding bits in the DSCP register to determine priority.

3.8 Rate-Limiting Support

The KSZ8842-PMQL/PMBL supports hardware rate limiting from 64 Kbps to 88 Mbps, independently on the “receive side” and on the “transmit side” as per port basis. For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up ingress rate control registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up egress rate control registers. The size of each frame has options to include minimum inter-frame gap (IFG) or preamble byte, in addition to the data field (from packet DA to FCS).

For ingress rate limiting, KSZ8842-PMQL/PMBL provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames. The KSZ8842-PMQL/PMBL counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit.

For egress rate limiting, the “leaky bucket” algorithm is applied to each output priority queue for shaping output traffic. Inter frame gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate.

To reduce congestion, it is a good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

3.8.1 MAC FILTERING FUNCTION

Use the static table to assign a dedicated MAC address to a specific port. When a unicast MAC address is not recorded in the static table, it is also not learned in the dynamic MAC table. The KSZ8862M includes an option that can filter or forward unicast packets for an unknown MAC address. This option is enabled by SGCR7 [7].

The unicast MAC address filtering function is useful in preventing the broadcast of unicast packets that could degrade the quality of this port in applications such as voice over Internet Protocol (VoIP).

3.8.2 CONFIGURATION INTERFACE

The KSZ8842-PMQL/PMBL operates only as a managed switch.

3.8.3 EEPROM INTERFACE

The external serial EEPROM with a standard microwire bus interface is used for non-volatile storage of information such as the host MAC address and ID, (for example, 93C46 or 93C66 EEPROM devices.)

If the EEEN pin/ball is pulled high, the KSZ8842-PMQL/PMBL performs an automatic read of the external EEPROM words 0H to 6H after the de-assertion of Reset. The EEPROM values are placed in certain host-accessible registers. EEPROM read/write functions can also be performed by software read/writes to the EEPCR registers.

The KSZ8842-PMQL/PMBL EEPROM format is shown in Table 3-5.

TABLE 3-5: EEPROM FORMAT

Word	15 8	7 0
0H	Reserved	
1H	Host MAC Address Byte 2	Host MAC Address Byte 1
2H	Host MAC Address Byte 4	Host MAC Address Byte 3
3H	Host MAC Address Byte 6	Host MAC Address Byte 5
4H	Subsystem ID	
5H	Subsystem Vendor ID	
6hH	Reserved	
7H - 3FH	Not used by KSZ8841PMQL/PMBL (available for user to use)	

3.9 Loopback Support

The KSZ8842-PMQL/PMBL provides loopback support for remote diagnostic of failure. In loopback mode, the speed at both PHY ports will be set to 100BASE-TX full-duplex mode. Two types of loopback are supported: Far-end Loopback and Near-end (Remote) Loopback.

3.9.1 NEAR-END (REMOTE) LOOPBACK

Near-end (Remote) loopback is conducted at PHY port 1 of the KSZ8842-PMQL/PMBL. The loopback path starts at the PHY port's receive inputs (RXPx/RXMx), wraps around at the same PHY port's PMD/PMA, and ends at the PHY port's transmit outputs (TXPx/TXMx).

Bit [1] of registers P1PHYCTRL and P2PHYCTRL is used to enable near-end loopback for ports 1 and 2, respectively. Alternatively, Bit [9] of registers P1SCSLMD and P2SCSLMD can also be used to enable near-end loopback. The both ports 1 and 2 near-end loopback paths are illustrated Figure 3-7.

3.9.2 FAR-END LOOPBACK

Far-end loopback is conducted between the KSZ8862M's two PHY ports. The loopback path starts at the "Originating." PHY port's receive inputs (RXP/RXM), wraps around at the "loopback" PHY port's PMD/PMA, and ends at the "Originating" PHY port's transmit outputs (TXP/TXM).

Bit [8] of registers P1CR4 and P2CR4 is used to enable far-end loopback for ports 1 and 2, respectively. Alternatively, Bit [14] of registers P1MBCR and P2MBCR can also be used to enable far-end loopback. The port 2 far-end loopback path is illustrated in Figure 3-8.

FIGURE 3-7: PORT 1 AND PORT 2 NEAR-END (REMOTE) LOOPBACK PATH

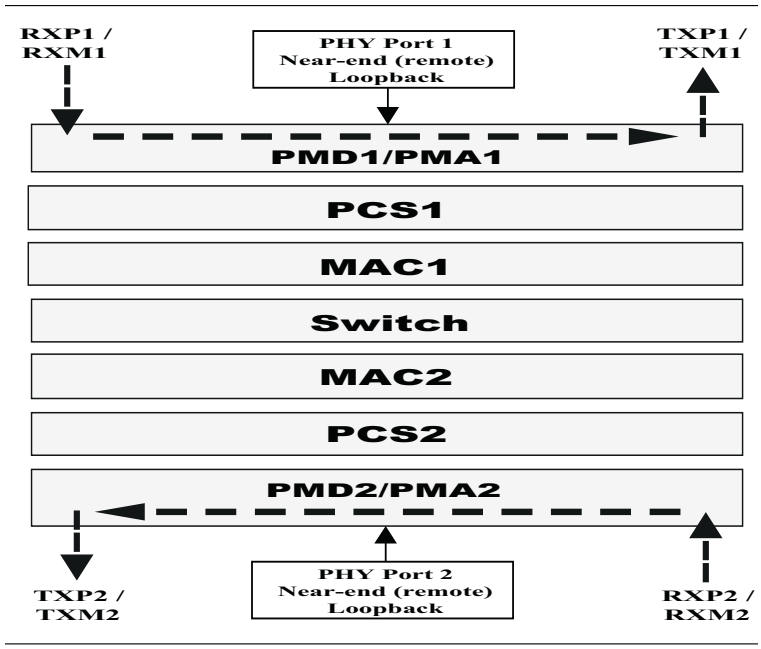
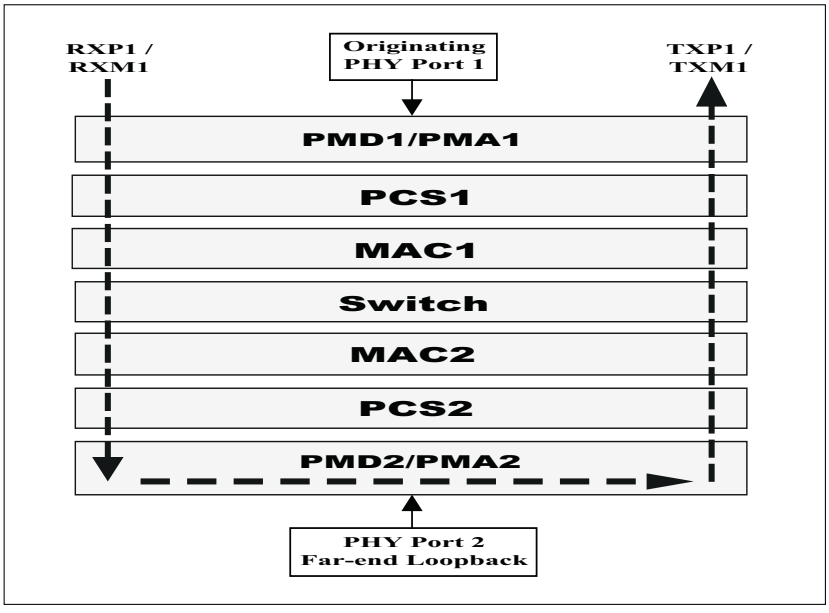


FIGURE 3-8: PORT 2 FAR-END LOOPBACK PATH



4.0 REGISTER DESCRIPTIONS

4.1 Host Communication

The descriptor lists and data buffers, collectively called the host communication, manage the actions and status related to buffer management. Commands and signals that control the functional operation of the KSZ8842-PMQL/PMBL are also described.

The KSZ8842-PMQL/PMBL and the driver communicate through the two data structures: Command and status registers (CSRs) and Descriptor Lists and Data Buffers.

Note: All unused bits of the data structure in this section are reserved and should be written by the driver as zero.

4.1.1 HOST COMMUNICATION DESCRIPTOR LISTS AND DATA BUFFERS

The KSZ8842-PMQL/PMBL transfers received data frames to the receive buffer in host memory and transmits data from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers.

There are two descriptor lists (one for receive and one for transmit) for the MAC DMA. The base address of each list is written in the TDLB register and in the RDLB register, respectively. A descriptor list is forward linked. The last descriptor may point back to the first entry to create a ring structure. Descriptors are chained by setting the next address to the next buffer in both receive and transmit descriptors.

The descriptor lists reside in the host physical memory address space. Each pointer points to one buffer and the second pointer points to the next descriptor. This enables the greatest flexibility for the host to chain any data buffers with discontinuous memory location. This eliminates processor-intensive tasks such as memory copying from the host to memory.

A data buffer contains either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; and buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. Data buffers reside in host physical memory space.

Receive Descriptors (RDES0 - RDES3)

Receive descriptor and buffer addresses must be Word aligned. Each receive descriptor provides one frame buffer, one byte count field, and control and status bits.

TABLE 4-1: RDES0 REGISTER BIT FIELDS

Bit	Description
31	OWN Own Bit When set, indicates that the descriptor is owned by the KSZ8842-PMQL/PMBL. When reset, indicates that the descriptor is owned by the host. The KSZ8841-PMQL clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	FS First Descriptor When set, indicates that this descriptor contains the first buffer of a frame.KSZ8842-PMQL/PMBLIf the buffer size of the first buffer is 0, the next buffer contains the beginning of the frame.
29	LS Last Descriptor When set, indicates that the buffer pointed by this descriptor is the last buffer of the frame.
28	IPE IP Checksum Error When set, indicates that the received frame is an IP packet and its IP checksum field does not match. This bit is valid only when last descriptor is set.
27	TCPE TCP Checksum Error When set, indicates that the received frame is a TCP/IP packet and its TCP checksum field does not match. This bit is valid only when last descriptor is set.
26	UDPE UDP Checksum Error When set, indicates that the received frame is an UDP/IP packet and its UDP checksum field does not match. This bit is valid only when last descriptor is set.

TABLE 4-1: RDES0 REGISTER BIT FIELDS (CONTINUED)

Bit	Description
25	ES Error Summary Indicates the logical OR of the following RDES0 bits: CRC error Frame too long Runt frame This bit is valid only when last descriptor is set.
24	MF Multicast Frame When set, indicates that this frame has a multicast address. This bit is valid only when last descriptor is set.
23 - 20	SPN Switch Engine Source Port Number This field indicates the source port where the packet originated. If bit 20 is set, it indicates the packet was received from port 1. If bit 21 is set, it indicates the packet was received from port 2. This field is valid only when the last descriptor is set. (Bits 23 and 22 are not used, but reserved for backward compatibility and future expansion.)
19	RE Report on MII Error When set, indicates that a receive error in the physical layer was reported during the frame reception.
18	TL Frame Too Long When set, indicates that the frame length exceeds the maximum size of 1518 bytes. This bit is valid only when last descriptor is set. Note: Frame too long is only a frame length indication and does not cause any frame truncation.
17	RF Runt Frame When set, indicates that this frame was damaged by a collision or premature termination before the collision window has passed. Runt frames are passed on to the host only if the pass bad frame bit is set.
16	CE CRC Error When set, indicates that a CRC error occurred on the received frame. This bit is valid only when last descriptor is set.
15	FT Frame Type When set, indicates that the frame is an Ethernet-type frame (frame length field is greater than 1500 bytes). When clear, indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames. This bit is valid only when last descriptor is set.
14 - 11	Reserved
10 - 0	FL Frame Length Indicates the length, in bytes, of the received frame, including the CRC. This field is valid only when last descriptor is set and descriptor error is reset.

TABLE 4-2: RDES1 REGISTER BIT FIELDS

Bit	Description
31 -26	Reserved
25	RER Receive End of Ring When set, indicates that the descriptor list reached its final descriptor. The KSZ8842-PMQL/PMBL returns to the base address of the list, thus creating a descriptor ring.
24 -12	Reserved
11 - 0	RBS Receive Buffer Size Indicates the size, in bytes, of the receive data buffer. If the field is 0, the KSZ8842-PMQL/PMBL ignores this buffer and moves to the next descriptor. The buffer size must be a multiple of 4.

TABLE 4-3: RDES2 REGISTER BIT FIELDS

Bit	Description
31 - 0	Buffer Address Indicates the physical memory address of the buffer. The buffer address must be Word aligned.

TABLE 4-4: RDES3 REGISTER BIT FIELDS

Bit	Description
31 - 0	Next Descriptor Address Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be Word aligned.

Transmit Descriptors (TDES0-TDES3)

Transmit descriptors must be Word aligned. Each descriptor provides one frame buffer, one byte count field, and control and status bits.

TABLE 4-5: TDES0 REGISTER BIT FIELDS

Bit	Description
31	OWN Own Bit When set, indicates that the descriptor is owned by the KSZ8842-PMQL/PMBL. When cleared, indicates that the descriptor is owned by the host. TheKSZ8842-PMQL/PMBL clears this bit either when it completes the frame transmission or when the buffer allocated in the descriptor is empty. The ownership bit of the first descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between the KSZ8842-PMQL/PMBL fetching a descriptor and the driver setting an ownership bit.
30 - 0	Reserved

TABLE 4-6: TDES1 REGISTER BIT FIELDS

Bit	Description
31	IC Interrupt on Completion When set, the KSZ8841-PMQL sets transmit interrupt after the present frame has been transmitted. It is valid only when last segment is set.
30	FS First Segment When set, indicates that the buffer contains the first segment of a frame.
29	LS Last Segment When set, indicates that the buffer contains the last segment of a frame.
28	IPCKG IP Checksum Generate When set, the KSZ8841-PMQL will generate correct IP checksum for outgoing frames that contains IP protocol header. The KSZ8842-PMQL/PMBL supports only a standard IP header, i.e., IP with a 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the IP checksum generate bit in the transmit mode register is not set. This bit should be always set for multiple-segment packets.
27	TCPCKG TCP Checksum Generate When set, theKSZ8842-PMQL/PMBL will generate correct TCP checksum for outgoing frames that contains IP and TCP protocol header. The KSZ8842-PMQL/PMBL supports only a standard IP header, i.e., IP with a 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the TCP checksum generate bit in the transmit mode register is not set. This bit should be always set for multiple-segment packets.

TABLE 4-6: TDES1 REGISTER BIT FIELDS (CONTINUED)

Bit	Description
26	UDPCKG UDP Checksum Generate When set, the KSZ8842-PMQL/PMBL will generate correct UDP checksum for outgoing frames that contains an IP and UDP protocol header. The KSZ8842-PMQL/PMBL supports only a standard IP header, i.e., IP with a 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set. This bit is used as a per-packet control when the UDP checksum generate bit in the transmit mode register is not set.
25	TER Transmit End of Ring When set, indicates that the descriptor pointer has reached its final descriptor. The KSZ8842-PMQL/PMBL returns to the base address of the list, forming a descriptor ring.
24	Reserved
23 - 20	SPN Switch Engine Destination Port Map When set, this field indicates the destination port(s) where the packet will be forwarded to. If bit 20 is set, it indicates the packet was received from port 1. If bit 21 is set, it indicates the packet was received from port 2. Setting all ports to 1 will cause the controller engine to broadcast the packet. Setting all bits to 0 has no effect. The controller engine forwards the packet according to its internal controller lookup algorithm. This field is valid only when the last descriptor is set. (Bits 23 and 22 are not used, but reserved for backward compatibility and future expansion.)
19 - 11	Reserved
10 - 0	TBS Transmit Buffer Size Indicates the size, in bytes, of the transmit data buffer. If this field is 0, the KSZ8842-PMQL/PMBL ignores this buffer and moves to the next descriptor.

TABLE 4-7: TDES2 REGISTER BIT FIELDS

Bit	Description
31 - 0	Buffer Address Indicates the physical memory address of the buffer. There is no limitation on the transmit buffer address alignment.

TABLE 4-8: TDES3 REGISTER BIT FIELDS

Bit	Description
31 - 0	Next Descriptor Address Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be Word aligned.

4.2 PCI Configuration Registers

The KSZ8842-PMQL/PMBL implements 12 configuration registers. These registers are described in the following sub-sections.

The KSZ8842-PMQL/PMBL enables a full software-driven initialization and configuration. This allows the software to identify and query the KSZ8842-PMQL/PMBL. The KSZ8842-PMQL/PMBL treats configuration space write operations to registers that are reserved as no-ops. That is, the access completes normally on the bus and the data is discarded. Read accesses, to reserved or unimplemented registers, complete normally and a data value of '0' is returned.

Software reset has no effect on the configuration registers. Hardware reset sets the configuration registers to their default values.

TABLE 4-9: LIST OF CONFIGURATION REGISTERS

Configuration Register	Identifier	I/O Address Offset	Default
Identification	CFID	00H	0x884116C6
Command and Status	CFCS	04H	0x02000000
Revision	CFRV	08H	0x02000010
Latency Timer	CFLT	0CH	0x00000000
Base Memory Address	CBMA	10H	0x00000000
Reserved	—	14H-28H	0x00000000
Subsystem ID	CSID	2CH	0x********
Reserved	—	38H	0x00000000
Interrupt	CFIT	3CH	0x28140100
Reserved	—	40H-4CH	0x00000000

Configuration ID Register (CFID Offset 00H)

The CFID register identifies the KSZ8842-PMQL/PMBL. Table 4-10 shows the CFID register bit fields.

TABLE 4-10: CONFIGURATION ID REGISTER (CFID OFFSET 00H)

Bit	Default	Description
31 - 16	0x8842	Device ID
15 - 0	0x16C6	Vendor ID Specifies the manufacturer of the KSZ8842-PMQL/PMBL.

The following table shows the access rules of the register.

TABLE 4-11: REGISTER ACCESS RULES

Category	Description
Value after hardware reset	0x884216C6
Write access rules	Write has no effect on the KSZ8842-PMQL/PMBL.

Command and Status Configuration Register (CFCS Offset 04H)

The CFCS register is divided into two sections: a command register (CFCS[15:0]) and a status register (CFCS[31:16]). The command register provides control of the KSZ8842-PMQL/PMBL's ability to generate and respond to PCI cycles. When '0' is written to this register, the KSZ8842-PMQL/PMBL logically disconnects from the PCI bus for all accesses except configuration accesses.

The status register records status information for the PCI bus-related events. The CFCS status bits are not cleared when they are read. Writing '1' to these bits clears them; writing '0' has no effect.

Table 4-12 describes the CFCS register bit fields.

TABLE 4-12: COMMAND AND STATUS CONFIGURATION REGISTER (CFCS OFFSET 04H)

Bit	Type	Default	Description
31	Status	0	Detected Parity Error When set, indicates that the KSZ8842-PMQL/PMBL detected a parity error, even if parity error handling is disabled in parity error response (CFCS[6]).
30	Status	0	Signal System Error When set, indicates that the KSZ8842-PMQL/PMBL asserted the system error SERR_N pin.
29	Status	0	Received Master Abort When set, indicates that the KSZ8842-PMQL/PMBL terminated a master transaction with master abort.
28	Status	0	Received Target Abort When set, indicates that the KSZ8842-PMQL/PMBL master transaction was terminated due to a target abort.
27	Status	0	Target Abort This bit is set by KSZ8842-PMQL/PMBL whenever it terminates with a Target Abort. The CSR registers are all 32-bit Little Endian format. For PCI register Read cycles, the KSZ8841-PMQL allows any different combination of CBEN. For PCI register bus cycles, only byte, word (16-bit), or Dword (32-bit) accesses are allowed. Any other combination is illegal and is target aborted.
26 - 25	Status	01	Device Select Timing Indicates the timing of the assertion of device select (DEVSEL_N). These bits are fixed at 01, which indicates a medium assertion of DEVSEL_N.
24	Status	0	Data Parity Report This bit is set when the following conditions are met: The KSZ8842-PMQL/PMBL asserts parity error PERR_N or it senses the assertion of PERR_N by another device. The KSZ8842-PMQL/PMBL operates as a bus master for the operation that caused the error. Parity error response (CFCS[6]) is set.
23 - 22	Reserved	00	Reserved
21	Status	0	66 MHz Capable 0 = Not 66 MHz capable
20 - 9	Reserved	0x000	Reserved
8	Command	0	System Error Enable When set, the KSZ8842-PMQL/PMBL asserts system error (SERR_N) when it detects a parity error on the address phase.
7	Reserved	0	Reserved
6	Command	0	Parity Error Response When set, the KSZ8842-PMQL/PMBL asserts fatal bus error after it detects a parity error. When reset, any detected parity error is ignored and the KSZ8841-PMQL continues normal operation. Parity checking is disabled after hardware reset.
5 - 3	Reserved	000	Reserved
2	Command	0	Master Operation When set, the KSZ8842-PMQL/PMBL is capable of acting as a bus master. When reset, the KSZ8842-PMQL/PMBL capability to generate PCI accesses is disabled. For normal operation, this bit must be set.

TABLE 4-12: COMMAND AND STATUS CONFIGURATION REGISTER (CFCS OFFSET 04H) (CONTINUED)

Bit	Type	Default	Description
1	Command	0	Memory Space Access When set, the KSZ8842-PMQL/PMBL responds to memory space accesses.When reset, the KSZ8842-PMQL/PMBL does not respond to memory space accesses.
0	Reserved	0	Reserved

Configuration Revision Register (CFRV Offset 08H)

The CFRV register contains the KSZ8842-PMQL/PMBL revision number. Table 4-13 below shows the CFRV register bit fields.

TABLE 4-13: CONFIGURATION REVISION REGISTER (CFRV OFFSET 08H)

Bit	Default	Description
31 - 24	0x02	Base Class Indicates the network controller and is equal to 2H.
23 - 16	0x00	Subclass Indicates the Fast/Gigabit Ethernet chip and is equal to 00H.
15 - 8	0x00	Reserved
7 - 4	0x1	Revision Number Indicates the KSZ8842-PMQL/PMBL revision number, and is equal to 1H. This number is incremented for subsequent revision.
3 - 0	0x0	Step Number Indicates the KSZ8842-PMQL/PMBL step number, and is equal to 0H (chip revision A). This number is incremented for subsequent KSZ8842-PMQL/PMBL steps within the current revision.

Configuration Latency Timer Register (CFLT Offset 0CH)

This register configures the cache line size field and the latency timer.

Table 4-14 below shows the CFLT register bit fields.

TABLE 4-14: CONFIGURATION LATENCY TIMER REGISTER (CFLT OFFSET 0CH)

Bit	Default	Description
31 - 16	0x00	Reserved
15 - 8	0x00	Configuration Latency Timer Specifies, in units of PCI bus clocks, the value of the latency timer of the KSZ8842-PMQL/PMBL. When the KSZ8841-PMQL asserts FRAME_N, it enables its latency timer to count. If the KSZ8841-PMQL deserts FRAME_N prior to count expiration, the content of the latency timer is ignored. Otherwise, after the count expires, the KSZ8842-PMQL/PMBL initiates transaction termination as soon as its GNT_N is deserted.
7 - 0	0x00	Cache Line Size Specifies, in unit of 32-bit words (Dword), the system cache line size.

Configuration Base Memory Address Register (CBMA Offset 10H)

The CBMA register specifies the base memory address for accessing the KSZ8842-PMQL/PMBL CSRs. This register must be initialized prior to accessing any CSR with memory access.

Table 4-15 shows the CBMA register bit fields.

TABLE 4-15: CONFIGURATION BASE MEMORY ADDRESS REGISTER (CBMA OFFSET 10H)

Bit	Default	Description
31 - 11	0	Configuration Base Memory Address Defines the base address assigned for mapping the KSZ8842-PMQL/PMBL CSRs.
10 - 1	0	This field value is 0 when read.
0	0	Memory Space Indicator Determines that the register maps into the Memory space. The value in this field is 0. This is a read-only field.

Subsystem ID Register (CSID Offset 2CH)

The CSID register is a read-only 32-bit register. The content of the CSID is loaded from the EEPROM after hardware reset. The loading period lasts at least 27,400 PCI cycles when the system is in 33 MHz mode, and starts 50 cycles after hardware reset desertion. If the host accesses the CSID before its content is loaded from the EEPROM, the KSZ8842-PMQL/PMBL responds with retry termination on the PCI bus.

Table 4-16 shows the CSID register bit fields.

TABLE 4-16: SUBSYSTEM ID REGISTER (CSID OFFSET 2CH)

Bit	Description
31 - 16	Subsystem ID Indicates a 16-bit field containing the subsystem ID.
15 - 0	Subsystem Vendor ID Indicates a 16-bit field containing the subsystem vendor ID.

The following table shows the access rules of the register.

TABLE 4-17: REGISTER ACCESS RULES

Category	Description
Value after hardware reset	Read from EEPROM.
Write access rules	Write has no effect on the KSZ8842-PMQL/PMBL.

Configuration Interrupt Register (CFIT Offset 3CH)

The CFIT register is divided into two sections: the interrupt line and the interrupt pin. CFIT configures both the system's interrupt and the KSZ8841-PMQL interrupt pin connection.

The following table shows the CFIT register bit fields.

TABLE 4-18: CONFIGURATION INTERRUPT REGISTER (CFIT OFFSET 3CH)

Bit	Default	Description
31 - 24	0x28	MAX_LAT This field indicates how often the device needs to gain access to the PCI bus. Time unit is equal to 0.25 µs, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 0x28 (10 µs).
23 - 16	0x14	MIN_GNT This field indicates the burst period length that the device needs. Time unit is equal to 0.25 µs, assuming a PCI clock frequency of 33 MHz. The value after a hardware reset is 0x14 (5 µs).

TABLE 4-18: CONFIGURATION INTERRUPT REGISTER (CFIT OFFSET 3CH) (CONTINUED)

Bit	Default	Description
15 - 8	0x01	Interrupt Pin/Ball Indicates which interrupt pin that the KSZ8841-PMQL uses. The KSZ8842-PMQL/PMBL uses INTA# and the read value is 0x01.
7 - 0	0x00	Interrupt Line Provides interrupt line routing information. The basic input/output system (BIOS) writes the routing information into to this field when it initialized and configures the system. The value in this field indicates which input of the system interrupt controller is connected to the KSZ8842-PMQL/PMBL's interrupt pin. The driver can use this information to determine priority and vector information. Values in this field are system architecture specific.

The following table shows the access rules of the register.

TABLE 4-19: REGISTER ACCESS RULES

Category	Description
Value after hardware reset	0x281401XX

4.3 PCI Control & Status Registers

The PCI CSR registers are all 32-bit in Little Endian format. For PCI register Read cycle, the KSZ8842-PMQL/PMBL allows any different combination of CBEN. For PCI register bus cycles, only byte, word (16-bit), or Dword (32-bit) accesses are allowed. Any other combinations are illegal and will be target aborted.

All other registers not included below are reserved.

MAC DMA Transmit Control Register (MDTXC Offset 0x0000)

The MAC DMA transmit control register establishes the transmit operating modes and commands for the port. This register should be one of the last CSRs to be written as part of the transmit initialization.

The following table shows the register bit fields.

TABLE 4-20: MAC DMA TRANSMIT CONTROL REGISTER (MDTXC OFFSET 0X0000)

Bit	Default	R/W	Description
31 - 30	—	RO	Reserved
29 - 24	0x00	R/W	MTBS DMA Transmit Burst Size This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the MAC DMA burst size is limited only by the amount of data stored in the transmit buffer before issuing a bus request. The MTBS can be programmed with permissible values 0,1, 2, 4, 8, 16, or 32. After reset, the MTBS default is 0, i.e. unlimited.
23 - 19	0x00	RO	Reserved
18	0	R/W	MTUCG MAC Transmit UDP Checksum Generate When set, the KSZ8842-PMQL/PMBL will generate correct UDP checksum for outgoing UDP/IP frames at port. When this bit is set, ADD CRC should also turn on.
17	0	R/W	MTTCG MAC Transmit TCP Checksum Generate When set, the KSZ8842-PMQL/PMBL will generate correct TCP checksum for outgoing TCP/IP frames at port. When this bit is set, ADD CRC should also turn on.

TABLE 4-20: MAC DMA TRANSMIT CONTROL REGISTER (MDTXC OFFSET 0X0000) (CONTINUED)

Bit	Default	R/W	Description
16	0	R/W	MTICG MAC Transmit IP Checksum Generate When set, the KSZ8842-PMQL/PMBL will generate correct IP checksum for outgoing IP frames at port. When this bit is set, ADD CRC should also turn on.
15 - 10	0x00	RO	Reserved
9	0	R/W	MTFCE MAC Transmit Flow Control Enable When this bit is set and the KSZ8842-PMQL/PMBL is in Full-Duplex mode, flow control is enabled and the KSZ8842-PMQL/PMBL will transmit a PAUSE frame when the Receive Buffer capacity has reached a level that may cause the buffer to overflow. When this bit is set and the KSZ8842-PMQL/PMBL is in Half-Duplex mode, back-pressure flow control is enabled. When this bit is cleared, no transmit flow control is enabled.
8 - 3	0x0	RO	Reserved
2	0	R/W	MTEP MAC DMA Transmit Enable Padding When set, the KSZ8842-PMQL/PMBL automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit automatically enables Add CRC feature.
1	0	R/W	MTAC MAC DMA Transmit Add CRC When set, the KSZ8842-PMQL/PMBL appends the CRC to the end of the transmission frame.
0	0	R/W	MTE MAC DMA TX Enable When the bit is set, the MDMA TX block is enabled and placed in a running state. When reset, the transmission process is placed in the stopped state after completing the transmission of the current frame. The stop transmission command is effective only when the transmission process is in the running state.

MAC DMA Receive Control Register (MDRXC Offset 0x0004)

The MAC DMA receive control register establishes the receive operating modes and commands for the port. This register should be one of the last CSRs to be written as part of the receive initialization.

The following table shows the register bit fields.

TABLE 4-21: MAC DMA RECEIVE CONTROL REGISTER (MDRXC OFFSET 0X0004)

Bit	Default	R/W	Description
31 - 30	00	RO	Reserved
29 - 24	0x00	R/W	MRBS DMA Receive Burst Size This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the MAC DMA burst size is limited only by the amount of data stored in the receive buffer before issuing a bus request. The MRBS can be programmed with permissible values 0,1, 2, 4, 8, 16, or 32. After reset, the MRBS default is 0, i.e. unlimited.
23 - 20	0x0	RO	Reserved
19	0	R/W	IP Header Alignment Enable 1 = Enable alignment of IP header to dWord address. Layer 2 header will not be dWord aligned anymore. Please look at RX descriptor 0 for the Layer 2 header address shift. 0 = IP Header alignment disabled.

TABLE 4-21: MAC DMA RECEIVE CONTROL REGISTER (MDRXC OFFSET 0X0004)

Bit	Default	R/W	Description
18	0	R/W	MRUCC MAC Receive UDP Checksum Check When set, the KSZ8842-PMQL/PMBL will check for correct UDP checksum for incoming UDP/IP frames at port. Packets received with incorrect UDP checksum will be discarded.
17	0	R/W	MRTCG MAC Receive TCP Checksum Check When set, the KSZ8842-PMQL/PMBL will check for correct TCP checksum for incoming TCP/IP frames at port. Packets received with incorrect TCP checksum will be discarded.
16	0	R/W	MRICG MAC Receive IP Checksum Check When set, the KSZ8842-PMQL/PMBL will check for correct IP checksum for incoming IP frames at port. Packets received with incorrect IP checksum will be discarded.
15 - 10	0x00	RO	Reserved
9	0	R/W	MRFCE MAC Receive Flow Control Enable When this bit is set and the KSZ8842-PMQL/PMBL is in Full-Duplex mode, flow control is enabled and the KSZ8842-PMQL/PMBL will acknowledge a PAUSE frame from MAC of the controller, the outgoing packets will be pending in the transmit buffer until the PAUSE control timer expires. This field has no meaning in half-duplex mode and should be programmed to 0. When this bit is cleared, no flow control is enabled.
8 - 7	00	RO	Reserved
6	0	R/W	MRB MAC Receive Broadcast When set, the MAC receive all broadcast frames.
5	0	R/W	MRM MAC Receive Multicast When set, the MAC receive all multicast frames (including broadcast).
4	0	R/W	MRU MAC Receive Unicast When set, the MAC receive unicast frames that match the 48-bit Station Address of the MAC.
3	0	R/W	MRE MAC DMA Receive Error Frame When set, the KSZ8842-PMQL/PMBL will pass the errors frames received to the host. Error frames include runt frames, oversized frames, CRC errors.
2	0	R/W	MRA MAC DMA Receive All When set, the KSZ8842-PMQL/PMBL receives all incoming frames, regardless of its destination address.
1	0	R/W	DMA Receive Multicast Hash-Table Enable Setting this bit enables the RX function to receive multicast frames that pass the CRC Hash filtering mechanism.
0	0	R/W	MRE MAC DMA RX Enable When the bit is set, the DMA RX block is enabled and placed in a running state. When reset, the receive process is placed in the stopped state after completing the reception of the current frame. The stop transmission command is effective only when the reception process is in the running state.

MAC DMA Transmit Start Command Register (MDTSC Offset 0x0008)

This register is written by the CPU when packets in the data buffer need to be transmitted. The following table shows the register bit fields.

TABLE 4-22: MAC DMA TRANSMIT START COMMAND REGISTER (MDTSC OFFSET 0X0008)

Bit	Default	R/W	Description
31 - 0	0x00000000	WO	WTSC Transmit Start Command When written with any value, the Transmit DMA checks for frames to be transmitted. If no descriptor is available, the transmit process returns to suspended state. If descriptors are available, the transmit process starts or resumes. This bit is self-clearing.

MAC DMA Receive Start Command Register (MDRSC Offset 0x000C)

This register is written by the CPU when there are frame data in receive buffer to be processed.

The following table shows the register bit fields.

TABLE 4-23: MAC DMA RECEIVE START COMMAND REGISTER (MDRSC OFFSET 0X000C)

Bit	Default	R/W	Description
31 - 0	0x00000000	WO	WRSC Receive Start Command When written with any value, the Receive DMA checks for descriptors to be acquired. If no descriptor is available, the receive process returns to suspended state and wait for the next receive restart command. If descriptors are available, the receive process resumes. This bit is self-clearing.

Transmit Descriptor List Base Address Register (TDLB Offset 0x0010)

This register is used for Transmit descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective START command is given.

Note that the descriptor lists must be Word (32-bit) aligned. The KSZ8842-PMQL/PMBL behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

TABLE 4-24: TRANSMIT DESCRIPTOR LIST BASE ADDRESS REGISTER (TDLB OFFSET 0X0010)

Bit	Default	R/W	Description
31 - 0	0x00000000	R/W	WSTL Start of Transmit List Note: Write can only occur when the transmit process stopped.

Receive Descriptor List Base Address Register (RDLB Offset 0x0014)

This register is used for Receive descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective START command is given.

Note that the descriptor lists must be Word (32-bit) aligned. The KSZ8842-PMQL/PMBL behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

TABLE 4-25: RECEIVE DESCRIPTOR LIST BASE ADDRESS REGISTER (RDLB OFFSET 0X0014)

Bit	Default	R/W	Description
31 - 0	0x0	R/W	WSRL Start of Receive List Note: Write can only occur when the transmit process stopped.

Reserved (Offset 0x0018)

Bit	Default	R/W	Description
31 - 0	0x0	RO	Reserved

Reserved (Offset 0x001C)

Bit	Default	R/W	Description
31 - 0	0x0	RO	Reserved

MAC Multicast Table 0 Register (MTR0 Offset 0x0020)

The 64-bit multicast table is used for group address filtering. The value is defined as the six most significant bits of the CRC of the DA. The two most significant bits select the register to be used, while the other determines the bit within the register.

TABLE 4-26: MAC MULTICAST TABLE 0 REGISTER (MTR0 OFFSET 0X0020)

Bit	Default	R/W	Description
31 - 0	0x0	R/W	MTR0 Multicast Table 0 When appropriate bit is set, the packet received with DA matches the CRC hashing function is received without being filtered. Note: when receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR then all multicast addresses are received regardless of the multicast table value.

MAC Multicast Table 1 Register (MTR1 Offset 0x0024)

The 64-bit multicast table is used for group address filtering. The value is defined as the six most significant bits of the CRC of the DA. The two most significant bits select the register to be used, while the other determines the bit within the register.

TABLE 4-27: MAC MULTICAST TABLE 1 REGISTER (MTR1 OFFSET 0X0024)

Bit	Default	R/W	Description
31 - 0	0x0	R/W	MTR0 Multicast Table 1 When appropriate bit is set, the packet received with DA matches the CRC hashing function is received without being filtered. Note: When receive all (RXRA) or receive multicast (RXRM) bit is set in the RXCR then all multicast addresses are received regardless of the multicast table value.

Interrupt Enable Register (INTEN Offset 0x0028)

This register enables the interrupts from the internal or external sources.

The following table shows the register bit fields.

TABLE 4-28: INTERRUPT ENABLE REGISTER (INTEN OFFSET 0X0028)

Bit	Default	R/W	Description
31	0	R/W	DMLCIE DMA MAC Link Changed Interrupt Enable When this bit is set, the DMA MAC Link Changed Interrupt is enabled. When this bit is reset, the DMA MAC Link Changed Interrupt is disabled.
30	0	R/W	DMTIE DMA MAC Transmit Interrupt Enable When this bit is set, the DMA MAC Transmit Interrupt is enabled. When this bit is reset, the DMA MAC Transmit Interrupt is disabled.

TABLE 4-28: INTERRUPT ENABLE REGISTER (INTEN OFFSET 0X0028) (CONTINUED)

Bit	Default	R/W	Description
29	0	R/W	DMRIE DMA MAC Receive Interrupt Enable When this bit is set, the DMA MAC Receive Interrupt is enabled. When this bit is reset, the DMA MAC Receive Interrupt is disabled.
28	0	R/W	DMTBUIE DMA MAC Transmit Buffer Unavailable Interrupt Enable When this bit is set, the DMA MAC Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the DMA MAC Transmit Buffer Unavailable Interrupt is disabled.
27	0	R/W	DMRBUIE DMA MAC Receive Buffer Unavailable Interrupt Enable When this bit is set, the DMA MAC Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the DMA MAC Receive Buffer Unavailable Interrupt is disabled.
26	0	R/W	DMTPSIE DMA MAC Transmit Process Stopped Interrupt Enable When this bit is set, the DMA MAC Transmit Process Stopped Interrupt is enabled. When this bit is reset, the DMA MAC Transmit Process Stopped Interrupt is disabled.
25	0	R/W	DMRPSIE DMA MAC Receive Process Stopped Interrupt Enable When this bit is set, the DMA MAC Receive Process Stopped Interrupt is enabled. When this bit is reset, the DMA MAC Receive Process Stopped Interrupt is disabled.
24 - 0	—	RO	Reserved

Interrupt Status Register (INTST Offset 0x002C)

This register contains all the status bits for the ARM CPU. When corresponding enable bit is set, it causes the CPU to be interrupted. This register is usually read by the driver during interrupt service routine or polling. The register bits are not cleared when read. Each field can be masked.

The following table shows the register bit fields.

TABLE 4-29: INTERRUPT STATUS REGISTER (INTST OFFSET 0X002C)

Bit	Default	R/W	Description
31	0	R/W	DMLCS DMA MAC Link Changed Status When this bit is set, it indicates that the DMA MAC link status has changed from link up to link down or from link down to link up. This edge-triggered interrupt status is cleared by writing 1 to this bit.
30	0	R/W	DMTS DMA MAC Transmit Status When this bit is set, it indicates that the DMA MAC has transmitted at least a frame on the DMA port and the MAC is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.
29	0	R/W	DMRS DMA MAC Receive Status When this bit is set, it indicates that the DMA MAC has received a frame from the DMA port and it is ready for the host to process This edge-triggered interrupt status is cleared by writing 1 to this bit.
28	0	R/W	DMTBUS DMA MAC Transmit Buffer Unavailable Status When this bit is set, it indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the KSZ8841-PMQL. The transmission process is suspended. To resume processing transmit descriptors, the host should change the ownership bit of the descriptor and then issue a transmit start command. This edge-triggered interrupt status is cleared by writing 1 to this bit.

TABLE 4-29: INTERRUPT STATUS REGISTER (INTST OFFSET 0X002C) (CONTINUED)

Bit	Default	R/W	Description
27	0	R/W	DMRBUS DMA MAC Receive Buffer Unavailable Status When this bit is set, it indicates that the descriptor list is owned by the host and cannot be acquired by the KSZ8842-PMQL/PMBL. The receiving process is suspended. To resume processing receive descriptors, the host should change the ownership of the descriptor and may issue a receive start command. If no receive start command is issued, the receiving process resumes when the next recognized incoming frame is received. After the first assertion, this bit is not asserted for any subsequent not owned receive descriptors fetches. This bit is asserted only when the previous receive descriptor was owned by the KSZ8842-PMQL/PMBL. This edge-triggered interrupt status is cleared by writing 1 to this bit.
26	0	R/W	DMTPSS DMA MAC Transmit Process Stopped Status Asserted when the DMA MAC transmit process enters the stopped state. This edge-triggered interrupt status is cleared by writing 1 to this bit.
25	0	R/W	DMRPSS DMA MAC Receive Process Stopped Status Asserted when the DMA MAC receive process enters the stopped state. This edge-triggered interrupt status is cleared by writing 1 to this bit.
24 - 0	—	RO	Reserved

MAC Additional Station Address Low Register (MAAL0-15)

The KSZ8842-PMQL/PMBL supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KSZ8841-PMQL will respond to when receiving frames on the port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

TABLE 4-30: MAC ADDITIONAL STATION ADDRESS LOW REGISTER (MAAL0-15)

Bit	Default	R/W	Description
31 - 0	—	R/W	MAAL0 MAC Additional Station Address 0 Low 4 bytes The least significant word of the additional MAC 0 station address.

MAC Additional Station Address High Register (MAAH0-15)

The KSZ8841-PMQL supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KSZ8841-PMQL will respond to when receiving frames on the port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

TABLE 4-31: MAC ADDITIONAL STATION ADDRESS HIGH REGISTER (MAAH0-15)

Bit	Default	R/W	Description
31	0	R/W	MAA0E MAC Additional Station Address 0 Enable When set, the additional MAC address is enabled for received frames. When reset, the additional MAC address is disabled.
30 - 16	0x0	RO	Reserved
15 - 0	—	R/W	MAAH0 MAC Additional Station Address 0 High 2 bytes The most significant word of the additional MAC 0 station address.

The following table shows the register map for all 16 additional MAC address registers.

TABLE 4-32: REGISTER MAP FOR ALL 16 MAC ADDRESS REGISTERS

Register	Identifier	Offset
ADD MAC Low 0	MAAL0	0x0080
ADD MAC High 0	MAAH0	0x0084
ADD MAC Low 1	MAAL1	0x0088
ADD MAC High 1	MAAH1	0x008C
ADD MAC Low 2	MAAL2	0x0090
ADD MAC High 2	MAAH2	0x0094
ADD MAC Low 3	MAAL3	0x0098
ADD MAC High 3	MAAH3	0x009C
ADD MAC Low 4	MAAL4	0x00A0
ADD MAC High 4	MAAH4	0x00A4
ADD MAC Low 5	MAAL5	0x00A8
ADD MAC High 5	MAAH5	0x00AC
ADD MAC Low 6	MAAL6	0x00B0
ADD MAC High 6	MAAH6	0x00B4
ADD MAC Low 7	MAAL7	0x00B8
ADD MAC High 7	MAAH7	0x00BC
ADD MAC Low 8	MAAL8	0x00C0
ADD MAC High 8	MAAH8	0x00C4
ADD MAC Low 9	MAAL9	0x00C8
ADD MAC High 9	MAAH9	0x00CC
ADD MAC Low 10	MAAL10	0x00D0
ADD MAC High 10	MAAH10	0x00D4
ADD MAC Low 11	MAAL11	0x00D8
ADD MAC High 11	MAAH11	0x00DC
ADD MAC Low 12	MAAL12	0x00E0
ADD MAC High 12	MAAH12	0x00E4
ADD MAC Low 13	MAAL13	0x00E8
ADD MAC High 13	MAAH13	0x00EC
ADD MAC Low 14	MAAL14	0x00F0
ADD MAC High 14	MAAH14	0x00F4
ADD MAC Low 15	MAAL15	0x00F8
ADD MAC High 15	MAAH15	0x00FC

4.4 MAC/PHY and Control Registers

MAC Address Register Low (0x0200): MARL

This register along with other 2 MAC address registers are loaded starting at word location 0x10 of the EEPROM upon hardware reset. The register can be modified by software driver, but will not modify the original MAC address value in the EEPROM. The MAC address is used to define the individual destination address that the KSZ8842-PMQL/PMBL host port will respond to when receiving unicast frames. This MAC address will become the source address when sending unicast frames from the host port to port-1 or port-2. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields for low word of MAC address.

TABLE 4-33: MAC ADDRESS REGISTER LOW (0X0200): MARL

Bit	Default	R/W	Description
15 - 0	—	R/W	MARL MAC Address Low The least significant word of the MAC address

This register along with the other two MAC address registers are loaded starting at word location 0x10 of the EEPROM upon hardware reset. The register can be modified by the software driver, but will not modify the original MAC address value in the EEPROM. MAC address is used to define the individual destination address the KSZ8842-PMQL/PMBL will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

TABLE 4-34: MAC ADDRESS REGISTER MIDDLE (0X0202): MARM

Bit	Default	R/W	Description
15 - 0	—	R/W	MARM MAC Address Middle The middle word of the MAC address

MAC Address Register High (0x0204): MARH

This register along with the other two MAC address registers are loaded starting at word location 0x10 of the EEPROM upon hardware reset. The register can be modified by software driver, but will not modify the original MAC address value in the EEPROM. MAC address is used to define the individual destination address the KSZ8842-PMQL/PMBL will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received from left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields for high word of MAC address.

TABLE 4-35: MAC ADDRESS REGISTER HIGH (0X0204): MARH

Bit	Default	R/W	Description
15 - 0	—	R/W	MARH MAC Address High The Most significant word of the MAC address

Reserved (Offset 0x0206 - 0x020A)

Bit	Default	R/W	Description
15 - 0	—	RO	Reserved

On-Chip Bus Control Register (Offset 0x0210): OBCR

This register controls the on-chip bus speed for the KSZ8842-PMQL/PMBL operations. It's used for power management when the external host CPU is running a slow frequency. The default of the on-chip bus speed is 25 MHz. When the external host CPU is running at a higher clock rate, it's recommended the on-chip bus is adjusted accordingly for the best performance.

TABLE 4-36: ON-CHIP BUS CONTROL REGISTER (OFFSET 0X0210): OBCR

Bit	Default	R/W	Description
15 - 2	—	RO	Reserved
1 - 0	0x3	R/W	OBSC On-Chip Bus Speed Control 00 = 125 MHz 01 = 62.5 MHz 10 = 41.66 MHz 11 = 25 MHz

EEPROM Control Register (Offset 0x0212): EEPCR

KSZ8842-PMQL/PMBL supports both with and without EEPROM system design. To support external EEPROM, tie the EEPROM Enable (EEEN) pin/ball to high; otherwise, tie it to Low (or no connect). Also, KSZ8842-PMQL/PMBL allows software to access (read and write) EEPROM directly. That is, the EEPROM access timing can be fully controlled by software if EEPROM Software Access bit is set.

TABLE 4-37: EEPROM CONTROL REGISTER (OFFSET 0X0212): EEPCR

Bit	Default	R/W	Description
15 - 5	0	RO	Reserved
4	0	R/W	EESA EEPROM Software Access 1 = Enable software to access EEPROM through bit 14 to bit 11. 0 = Disable software to access EEPROM.
3	00	RO	EECB EEPROM Status Bits Bit 3: Data receive from EEPROM. This bit directly reflects the value of the EEDI pin.
2	00	R/W	EECB EEPROM Control Bits Bit 2: Data In to EEPROM. This bit directly controls the device's the EEDO pin.
1	00	R/W	EECB EEPROM Control Bits Bit 1: Serial Clock. This bit directly controls the device's the EESK pin.
0	00	R/W	EECB EEPROM Control Bits Bit 0: Chip Select. This bit directly controls the device's the EECS pin.

Memory BIST Info Register (Offset 0x0214): MBIR

The following table shows the register bit fields.

TABLE 4-38: MEMORY BIST INFO REGISTER (OFFSET 0X0214): MBIR

Bit	Default	R/W	Description
15 - 13	0x0	RO	Reserved
12	—	RO	TXMBF TX Memory Bits Finish When set, it indicates the Memory Built In Self Test has completed for the TX Memory.
11	—	RO	TXMBFA TX Memory Bits Fail When set, it indicates the Memory Built In Self Test has failed.
10 - 5	—	RO	Reserved
4	—	RO	RXMBF RX Memory Bits Finish When set, it indicates the Memory Built In Self Test has completed for the RX Memory.
3	—	RO	RXMBFA RX Memory Bits Fail When set, it indicates the Memory Built In Self Test has failed.
2 - 0	—	RO	Reserved

Global Reset Register (Offset 0x0216): GRR

This register holds control information programmed by the CPU to control the global soft reset function.

TABLE 4-39: GLOBAL RESET REGISTER (OFFSET 0X0216): GRR

Bit	Default	R/W	Description
15 - 1	0x00	RO	Reserved
0	0	R/W	Global Soft Reset 1 = Software reset active 0 = Software reset inactive Set two times to finish the software reset, this soft reset bit will reset PCI control/status registers only.

Switch Registers

Switch ID and Enable Register (Offset 0x0400): SIDER

This register contains the switch ID, and the switch-enable control.

TABLE 4-40: SWITCH ID AND ENABLE REGISTER (OFFSET 0X0400): SIDER

Bit	Default	R/W	Description
15 - 8	0x88	RO	Family ID Chip family
7 - 4	0x04	RO	Chip ID
3 - 1	000	RO	Revision ID
0	—	R/W	Start Switch 1 = Start the chip

Switch Global Control Register 1 (Offset 0x0402): SGCR1

This register contains the global control bits for the switch function.

TABLE 4-41: SWITCH GLOBAL CONTROL REGISTER 1 (OFFSET 0X0402): SGCR1

Bit	Default	R/W	Description
15	0	RW	Pass All Frames 1 = Switch all packets including bad ones. Used solely for debugging purposes. Works in conjunction with Sniffer mode only.
14	0	RW	Reserved For factory test purposes only. Always write 0.
13	1	RW	IEEE 802.3x Transmit Direction Flow Control Enable 1 = will enable transmit direction flow control feature. 0 = will not enable transmit direction flow control feature. Switch will not generate any flow control packets.
12	1	RW	IEEE 802.3x Receive Direction Flow Control Enable 1 = will enable receive direction flow control feature. 0 = will not enable receive direction flow control feature. Switch will not react to any received flow control packets.
11	0	RW	Frame Length Field Check 1 = Enable checking frame length field in the IEEE packets. If the actual length does not match, the packet will be dropped (for Length/Type field < 1500).
10	1	RW	Aging Enable 1 = Enable age function in the chip. 0 = Disable age function in the chip.
9	0	RW	Fast Age Enable 1 = Turn on fast aging (800 µs).

TABLE 4-41: SWITCH GLOBAL CONTROL REGISTER 1 (OFFSET 0X0402): SGCR1 (CONTINUED)

Bit	Default	R/W	Description
8	0	RW	Aggressive Back-Off Enable 1 = Enable more aggressive back-off algorithm in half duplex mode to enhance performance. This is not an IEEE standard.
7 - 4	01	RW	Reserved
3	0	RW	Pass Flow Control Packet 1 = Switch will not filter 802.1x “flow control” packets.
2 - 1	00	RW	Reserved
0	0	RW	Link Change Age 1 = Link change from “link” to “no link” will cause fast aging (<800 µs) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 + 75 seconds). Note: If any port is unplugged, all addresses will be automatically aged out.

Switch Global Control Register 2 (Offset 0x0404): SGCR2

This register contains global control bits for the switch function.

TABLE 4-42: SWITCH GLOBAL CONTROL REGISTER 2 (OFFSET 0X0404): SGCR2

Bit	Default	R/W	Description
15	0	RW	802.1Q VLAN Enable 1 = 802.1Q VLAN mode is turned on. VLAN table must be set up before the operation. 0 = 802.1Q VLAN is disabled.
14	0	RW	IGMP Snoop Enable 1 = IGMP snoop is enabled. 0 = IGMP snoop is disabled.
13	0	RW	IPv6 MLD Snooping Enable 1 = Enable IPv6 MLD snooping.
12	0	RW	IPv6 MLD Snooping Option 1 = Enable IPv6 MLD snooping option.
11	0	RW	Priority Scheme select 0 = always TX higher priority packets first 1 = Weighted Fair Queuing enable. When all 4 queues has packets waiting to TX, the bandwidth allocation is q3:q2:q1:q0 = 8:4:2:1. If any queues is empty, the highest non-empty queue will get one more weighting. For example, if q2 is empty, q3:q2:q1:q0 will become (8+1): 0:2:1.
10 - 9	0	RW	Reserved. For factory test purposes only. Always write 0.
8	0	RW	Sniff Mode Select 1 = Performs RX and TX sniff (both the source port and destination port need to match). 0 = Performs RX or TX sniff (either the source port or destination port needs to match). This is the mode used to implement RX only sniff.
7	1	RW	Unicast Port-VLAN Mismatch Discard 1 = No packets can cross the VLAN boundary. 0 = Unicast packets (excluding unknown/multicast/broadcast) can cross the VLAN boundary.
6	1	RW	Multicast Storm Protection Disable 1 = “Broadcast Storm Protection” does not include multicast packets. Only DA = FF-FF-FF-FF-FF-FF packets are regulated. 0 = “Broadcast Storm Protection” includes DA = FF-FF-FF-FF-FF-FF and DA[40] = “1” packets.

TABLE 4-42: SWITCH GLOBAL CONTROL REGISTER 2 (OFFSET 0X0404): SGCR2 (CONTINUED)

Bit	Default	R/W	Description
5	1	RW	Back Pressure Mode 1 = Carrier sense-based back pressure is selected. 0 = Collision-based back pressure is selected.
4	1	RW	Flow Control and Back Pressure Fair Mode 1 = Fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, packets from the non-flow control port may be dropped. This prevents the flow control port from being flow controlled for an extended period of time. 0 = In this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port is flow controlled. This may not be “fair” to the flow control port.
3	0	RW	No Excessive Collision Drop 1 = The switch does not drop packets when 16 or more collisions occur. 0 = The switch drops packets when 16 or more collisions occur.
2	0	RW	Huge Packet Support 1 = Accepts packet sizes up to 1916 bytes (inclusive). This bit setting overrides setting from bit 1 of the same register. 0 = The max packet size is determined by bit [1] of this register.
1	0	RW	Legal Maximum Packet size check enable 0 = will accept packet sizes up to 1536 bytes (inclusive). 1 = 1522 bytes for tagged packets, 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.
0	0	RW	Priority Buffer Reserve 1 = Each port is pre-allocated 48 buffers, used exclusively for high priority (q3, q2, and q1) packets. Effective only when the multiple queue feature is turned on. 0 = Each port is pre-allocated 48 buffers used for all priority packets (q3, q2, q1, and q0).

Switch Global Control Register 3 (Offset 0x0406): SGCR3

This register contains global control bits for the switch function.

TABLE 4-43: SWITCH GLOBAL CONTROL REGISTER 3 (Offset 0x0406): SGCR3

Bit	Default	R/W	Description
15 - 8	0x63	RW	Broadcast Storm Protection Rate Bit [7:0] These bits, along with SGCR3[2:0], determine how many 64-byte blocks of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 670 ms for 10BT. The default is 1%.
7	0	RW	Repeater Mode 1 = enable repeater mode 0 = normal mode Note: The Repeater only supports 100BT, half duplex modes. When set to repeater mode, need to disable follow control in register MDTXC[9].
6	0	RW	Switch Host Port Duplex Mode 1 = enable switch host interface half duplex mode. 0 = enable switch host interface full duplex mode. (Keep default value to match DMA MAC to the full duplex mode only).
5	1	RW	Switch Host Port Flow Control Enable 1 = Enable full-duplex flow control on switch host interface. 0 = Disable full-duplex flow control on switch host interface.
4	0	RW	Reserved (must be 0).
3	0	RW	Null VID Replacement 1 = Replaces NULL VID with port VID (12 bits). 0 = No replacement for NULL VID.
2 - 0	000	RW	Broadcast Storm Protection Rate Bit [10:8] These bits, along with SGCR3[15:8] determine how many 64-byte blocks of packet data are allowed on an input port in a preset period. The period is 67 ms for 100BT or 670 ms for 10BT. The default is 1%.

Broadcast storm protection rate: 148,800 frames/sec * 67 ms/interval * 1% = 99 frames/interval (approx. 0x63).

Switch Global Control Register 4 (Offset 0x0408): SGCR4

This register contains the global control bits for the switch function.

TABLE 4-44: SWITCH GLOBAL CONTROL REGISTER 4 (OFFSET 0X0408): SGCR4

Bit	Default	R/W	Description
15 - 0	0x2400	RW	Reserved. For factory testing purposes only.

Switch Global Control Register 5 (Offset 0x040A): SGCR5

This register contains the global control for the chip function.

TABLE 4-45: SWITCH GLOBAL CONTROL REGISTER 5 (OFFSET 0X040A): SGCR5

Bit	Default	R/W	Description
15	0	R/W	**LEDSEL1** See description in bit 9.
14	0	R/W	Reserved
13	0	R/W	Reserved
12	0	R/W	Testing mode Reserved, must be 0
11 - 10	0x2	R/W	Reserved
9	0	R/W	**LEDSEL0** These two bits, LEDSEL1 and LEDSEL0, are used to select LED mode. Port n LED indicators, (where n = 1 for port 1 and n =2 for port 2) defined as below:
			[LEDSEL1, LEDSEL0] / **[0, 0]** / **[0, 1]**
			PxLED3 — —
			PxLED2 Link/Activity 100Link/Activity
			PxLED1 Full-Duplex/Col 10Link/Activity
			PxLED0 Speed Full-Duplex
			[LEDSEL1, LEDSEL0] / **[1, 0]** / **[1, 1]**
			PxLED3 Activity —
			PxLED2 Link —
			PxLED1 Full-Duplex/Col —
			PxLED0 Speed —
			Port 1 and port 2 LED indicators as repeater mode defined as follows:
			Switch Global Control Register 5: SGCR5 bit [15,9] Note: See pin/ball description for detail definition / [0,0] Default / [0,1] [1,0] [1,1]
			P1LED3 RPT_COL —
			P1LED2 RPT_Link3/RX —
			P1LED1 RPT_Link2/RX —
			P1LED0 RPT_Link1/RX —
			P2LED3 RPT_ACT —
			P2LED2 RPT_ERR3 —
			P2LED1 RPT_ERR2 —
			P2LED0 RPT_ERR1 —
8	0	RO	Reserved
7 - 0	0x35	RO	Reserved

Switch Global Control Register 6 (Offset 0x0410): SGCR6

This register contains global control bits for the switch function.

TABLE 4-46: SWITCH GLOBAL CONTROL REGISTER 6 (OFFSET 0X0410): SGCR6

Bit	Default	R/W	Description
15 - 14	0x3	R/W	Tag_0x7 IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x7.
13 - 12	0x3	R/W	Tag_0x6 IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x6.
11 - 10	0x2	R/W	Tag_0x5 IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x5.
9 - 8	0x2	R/W	Tag_0x4 IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x4.
7 - 6	0x1	R/W	Tag_0x3 IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x3.
5 - 4	0x1	R/W	Tag_0x2 IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x2.
3 - 2	0x0	R/W	Tag_0x1 IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x1.
1 - 0	0x0	R/W	Tag_0x0 IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE Tag has a value of 0x0.

Switch Global Control Register 7 (0x0412): SGCR7

This register contains global control bits for the switch function.

TABLE 4-47: SWITCH GLOBAL CONTROL REGISTER 7 (0X0412): SGCR7

Bit	Default	R/W	Description
15 - 8	0	R/W	Reserved
7	0	R/W	Unknown Default Port Enable Send packets with unknown destination address to specified ports in bits [2:0]. 1 = enable to send unknown DA packet.
6 - 3	0x0	R/W	For factory test only. Always write 0.
2 - 0	0x7	R/W	Unknown Packet Default Port(s) Specify which ports to send packets with unknown destination addresses. Feature is enabled by bit [7]. Bit 2 for the host port, bit 1 for port 2, and bit 0 for port 1.

Reserved (Offset 0x0414 - 0x046F)

MAC Address Register 1 (Offset 0x0470): MACAR1

This register contains the MAC address for the switch function. This MAC address is used to send the PAUSE frame.

TABLE 4-48: MAC ADDRESS REGISTER 1 (Offset 0x0470): MACAR1

Bit	Default	R/W	Description
15 - 0	0x0010	RW	MACA[47:32] Specify host MAC address 1. This value must be the same as MAC Address Register High (0x0204): MARH.

MAC Address Register 2 (Offset 0x0472): MACAR2

This register contains the MAC address for the switch function. This MAC address is used for sending PAUSE frame.

TABLE 4-49: MAC ADDRESS REGISTER 2 (OFFSET 0X0472): MACAR2

Bit	Default	R/W	Description
15 - 0	0xA1FF	RW	MACA[31:16] Specify host MAC address 2. This value must be the same as MAC Address Register Middle (0x0202): MARM.

MAC Address Register 3 (Offset 0x0474): MACAR3

This register contains the MAC address for the switch function. This MAC address is used for sending PAUSE frame.

TABLE 4-50: MAC ADDRESS REGISTER 3 (OFFSET 0X0474): MACAR3

Bit	Default	R/W	Description
15 - 0	0xFFFF	RW	MACA[15:0] Specify host MAC address 3. This value must be the same as MAC Address Register Low (0x0200): MARL.

Reserved (Offset 0x0476 - 0x047F)

This register is reserved.

TABLE 4-51: MAC ADDRESS REGISTER 2 (OFFSET 0X0472): MACAR2

Bit	Default	R/W	Description
15 - 0	0x0000	RO	Reserved

Priority Control Register 1 (Offset 0x0480): TOSR1

This register contains the TOS priority control for the switch function.

The IPv4/Ipv6 TOS priority control registers implement a fully decoded 64 DSCP (Differentiated Services Code Point) register used to determine priority from the 6 bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bits in the DSCP register to determine the priority

TABLE 4-52: TOS PRIORITY CONTROL REGISTER 1 (Offset 0x0480): TOSR1

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[15:14]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x1C.
13−12	0	R/W	**DSCP[13:12]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x18.
11−10	0	R/W	**DSCP[11:10]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x14.
9−8	0	R/W	**DSCP[9:8]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x10.
7−6	0	R/W	**DSCP[7:6**] The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x0C.
5−4	0	R/W	**DSCP[5:4]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x08.
3−2	0	R/W	**DSCP[3:2]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x04.
1−0	0	R/W	**DSCP[1:0]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x00.

TOS Priority Control Register 2 (0x482): TOSR2

This register contains the TOS priority control bits for the switch function.

TABLE 4-53: TOS PRIORITY CONTROL REGISTER 2 (0X482): TOSR2

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[31:30]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x3C.
13−12	0	R/W	**DSCP[29:28]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x38.
11−10	0	R/W	**DSCP[27:26]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x34.
9−8	0	R/W	**DSCP[25:24]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x30.
7−6	0	R/W	**DSCP[23:22**] The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x2C.
5−4	0	R/W	**DSCP[21:20]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x28.
3−2	0	R/W	**DSCP[19:18]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x24.
1−0	0	R/W	**DSCP[17:16]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x20.

TOS Priority Control Register 3 (0x484): TOSR3

This register contains the TOS priority control bits for the switch function.

TABLE 4-54: TOS PRIORITY CONTROL REGISTER 3 (0X484): TOSR3

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[47:46]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x5C.
13−12	0	R/W	**DSCP[45:44]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x58.
11−10	0	R/W	**DSCP[43:42]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x54.
9−8	0	R/W	**DSCP[41:40]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x50.
7−6	0	R/W	**DSCP[39:38]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x4C.
5−4	0	R/W	**DSCP[37:36]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x48.
3−2	0	R/W	**DSCP[35:34]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x44.
1−0	0	R/W	**DSCP[33:32]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x40.

TOS Priority Control Register 4 (0x486): TOSR4

This register contains the TOS priority control bits for the switch function.

TABLE 4-55: TOS PRIORITY CONTROL REGISTER 4 (0X486): TOSR4

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[63:62]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x7C.
13−12	0	R/W	**DSCP[61:60]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x78.
11−10	0	R/W	**DSCP[59:58]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x74.
9−8	0	R/W	**DSCP[57:56]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x70.
7−6	0	R/W	**DSCP[55:54]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x6C.
5−4	0	R/W	**DSCP[53:52]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x68.
3−2	0	R/W	**DSCP[51:50]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x64.
1−0	0	R/W	**DSCP[49:48]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x60.

TOS Priority Control Register 5 (0x488): TOSR5

This register contains the TOS priority control bits for the switch function.

TABLE 4-56: TOS PRIORITY CONTROL REGISTER 5 (0X488): TOSR5

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[79:78]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x9C.
13−12	0	R/W	**DSCP[77:76]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x98.
11−10	0	R/W	**DSCP[75:74]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x94.
9−8	0	R/W	**DSCP[73:72]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x90.
7−6	0	R/W	**DSCP[71:70]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x8C.
5−4	0	R/W	**DSCP[69:68]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x88.
3−2	0	R/W	**DSCP[67:66]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x84.
1−0	0	R/W	**DSCP[65:64]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0x80.

TOS Priority Control Register 6 (0x48A): TOSR6

This register contains the TOS priority control bits for the switch function.

TABLE 4-57: TOS PRIORITY CONTROL REGISTER 6 (0X48A): TOSR6

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[95:94]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value is 0xbC.
13−12	0	R/W	**DSCP[93:92]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb8.
11−10	0	R/W	**DSCP[91:90]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb4.
9−8	0	R/W	**DSCP[89:88]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xb0.
7−6	0	R/W	**DSCP[87:86]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xaC.
5−4	0	R/W	**DSCP[85:84]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa8.
3−2	0	R/W	**DSCP[83:82]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa4.
1−0	0	R/W	**DSCP[81:80]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xa0.

TOS Priority Control Register 7 (0x490): TOSR7

This register contains the TOS priority control bits for the switch function.

TABLE 4-58: TOS PRIORITY CONTROL REGISTER 7 (0X490): TOSR7

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[111:110]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xdC.
13−12	0	R/W	**DSCP[109:108]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd8.
11−10	0	R/W	**DSCP[107:106]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd4.
9−8	0	R/W	**DSCP[105:104]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xd0.
7−6	0	R/W	**DSCP[103:102]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xcC.
5−4	0	R/W	**DSCP[101:100]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc8.
3−2	0	R/W	**DSCP[99:98]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc4.
1−0	0	R/W	**DSCP[97:96]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xc0.

TOS Priority Control Register 8 (0x492): TOSR8

This register contains the TOS priority control bits for the switch function.

TABLE 4-59: TOS PRIORITY CONTROL REGISTER 7 (0X492): TOSR8

Bit	Default	R/W	Description
15−14	0	RW	**DSCP[127:126]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xfC.
13−12	0	R/W	**DSCP[125:124]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf8.
11−10	0	R/W	**DSCP[123:122]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf4.
9−8	0	R/W	**DSCP[121:120]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xf0.
7−6	0	R/W	**DSCP[119:118]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xeC.
5−4	0	R/W	**DSCP[117:116]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe8.
3−2	0	R/W	**DSCP[115:114]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe4.
1−0	0	R/W	**DSCP[113:112]** The value in this field is used as the frame's priority when bits [7:2] of the IP TOS/DiffServ/Traffic Class value are 0xe0.

Reserved (Offset 0x0494 - 0x0498A)

This register is reserved.

Bit	Default	R/W	Description
15 - 0	0x0000	RO	Reserved

Indirect Access Control Register (Offset 0x04A0): IACR

This register contains the indirect control for the MIB counter. Write IACR will actually trigger a command. Read or write access is determined by this register bit 12.

TABLE 4-60: INDIRECT ACCESS CONTROL REGISTER (OFFSET 0X04A0): IACR

Bit	Default	R/W	Description
15 - 13	000	R/W	Reserved
12	0	R/W	Read High. Write Low 1 = Read cycle 0 = Write cycle
11 - 10	00	R/W	Table select 00 = Static MAC address table selected 01 = VLAN table selected 10 = Dynamic address table selected 11 = MIB counter selected
9 - 0	0x000	R/W	Indirect address Bit 9 - 0 of indirect address

Note: Write IACR will actually trigger a command. Read or write access is determined by Register bit 12.

Indirect Access Data Register 1 (Offset 0x04A2): IADR1

This register contains the indirect data for the chip function.

TABLE 4-61: INDIRECT ACCESS DATA REGISTER 1 (OFFSET 0X04A2): IADR1

Bit	Default Value	R/W	Description
15 - 8	0x000	RO	Reserved
7	0	RO	CPU Read Status Only for dynamic and statistics counter reads. 1 = Read is still in progress. 0 = Read has completed.
6 - 3	0x0	RO	Reserved
2 - 0	000	RO	Indirect Data [66:64] Bits [66:64] of indirect data.

Indirect Access Data Register 2 (Offset 0x04A4): IADR2

This register contains the indirect data for the switch function.

TABLE 4-62: INDIRECT ACCESS DATA REGISTER 2 (OFFSET 0X04A4): IADR2

Bit	Default Value	R/W	Description
15 - 0	0x0000	RW	Indirect Data Bit 47-32 of indirect data.

Indirect Access Data Register 3 (Offset 0x04A6): IADR3

This register contains the indirect data for the chip function.

TABLE 4-63: INDIRECT ACCESS DATA REGISTER 3 (OFFSET 0X04A6): IADR3

Bit	Default Value	R/W	Description
15 - 0	0x0000	RW	Indirect Data Bit 63-48 of indirect data.

Indirect Access Data Register 3 (Offset 0x04A8): IADR4

This register contains the indirect data for the chip function.

TABLE 4-64: INDIRECT ACCESS DATA REGISTER 4 (OFFSET 0X04A8): IADR4

Bit	Default Value	R/W	Description
15 - 0	0x0000	R/W	Indirect Data Bit 15-0 of indirect data.

Indirect Access Data Register 5 (Offset 0x04AA): IADR5

This register contains the indirect data for the chip function.

TABLE 4-65: Indirect Access Data Register 5 (Offset 0x04AA): IADR5

Bit	Default Value	R/W	Description
15 - 0	0x0000	R/W	Indirect Data Bit 31-16 of indirect data.

Reserved (Offset 0x04B0 - 0x04BA)

Reserved (Offset 0x04C0 –0x04CF)

PHY 1 MII Register Basic Control Register (Offset 0x04D0): P1MBCR

This register contains the MII control for the switch port 1 function.

TABLE 4-66: PHY 1 MII REGISTER BASIC CONTROL REGISTER (OFFSET 0X04D0): P1MBCR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	Soft reset NOT SUPPORTED	—
14	0	R/W	Loop back 1 = Perform loop back as follows: Start: RXP1/RXM1 (port 2) Loop back: PMD/PMA of port 1's PHY End: TXP1/TXM1 (port 2) 0 = Normal operation	P1CR4, bit 8
13	0	R/W	Force 100 1 = Force 100 Mbps if AN is disabled (bit12) 0 = Force 10 Mbps if AN is disabled (bit12)	P1CR4, bit 6
12	1	R/W	AN enable 1 = Auto-negotiation enabled 0 = Auto-negotiation disabled	P1CR4, bit 7
11	0	R/W	Power down 1 = Power down 0 = Normal operation	P1CR4, bit 11
10	0	RO	Isolate NOT SUPPORTED	—
9	0	R/W	Restart AN 1 = Restart auto-negotiation 0 = Normal operation	P1CR4, bit 13
8	0	R/W	Force full-duplex 1 = Force full-duplex if AN is disabled (bit12) 0 = Force half-duplex if AN is disabled (bit12)	P1CR4, bit 5
7	0	RO	Collision test Not supported	—
6	0	RO	Reserved	—
5	0	R/W	HP_mdix 1 = HP Auto MDIX mode 0 = Microchip Auto MDIX mode	P1SR, bit 15
4	0	R/W	Force MDIX 1 = Force MDIX 0 = Normal operation	P1CR4, bit 9
3	0	R/W	Disable MDIX 1 = Disable auto MDIX 0 = Normal operation	P1CR4, bit 10
2	0	R/W	Disable far end fault 1 = Disable far end fault detection 0 = Normal operation	P1CR4, bit 12
1	0	R/W	Disable transmit 1 = Disable transmit 0 = Normal operation	P1CR4, bit 14
0	0	R/W	Disable LED 1 = Disable LED 0 = Normal operation	P1CR4, bit 15

PHY 1 MII Basic Status Register (Offset 0x04D2): P1MBSR

This register contains the MII control for the switch port 1 function.

TABLE 4-67: PHY 1 MII REGISTER BASIC STATUS REGISTER (OFFSET 0X04D2): P1MBSR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	T4 capable 1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	—
14	1	RO	100 Full capable 1 = 100BASE-TX full-duplex capable 0 = Not 100BASE-TX full-duplex capable	Always 1
13	1	RO	100 Half capable 1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	Always 1
12	1	RO	10 Full capable 1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	Always 1
11	1	RO	10 Half capable 1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	Always 1
10 - 7	0	RO	Reserved	—
6	0	RO	Preamble suppressed NOT SUPPORTED	—
5	0	RO	AN complete 1 = Auto-negotiation complete 0 = Auto-negotiation not completed	P1SR, bit 6
4	0	RO	Far end fault 1 = Far end fault detected 0 = No far end fault detected	P1SR, bit 8
3	1	RO	AN capable 1 = Auto-negotiation capable 0 = Not auto-negotiation capable	P1CR4, bit 7
2	0	RO	Link status 1 = Link is up 0 = Link is down	P1SR, bit 5
1	0	RO	Jabber test Not supported	—
0	0	RO	Extended capable 1 = Extended register capable 0 = Not extended register capable	—

PHY 1 PHYID Low Register (Offset 0x04D4): PHY1ILR

This register contains the PHY ID (low) for the chip function.

TABLE 4-68: PHY 1 PHYID LOW REGISTER (OFFSET 0X04D4): PHY1ILR

Bit	Default	R/W	Description
15 - 0	0x1430	RO	PHYID low Low order PHYID bits

PHY 1 PHYID High Register (Offset 0x04D6): PHY1IHR

This register contains the PHY ID (high) for the chip function.

TABLE 4-69: PHY 1 PHYID HIGH REGISTER (OFFSET 0X04D6): PHY1IHR

Bit	Default	R/W	Description
15 - 0	0x0022	RO	PHYID high High order PHYID bits

PHY 1 Auto-Negotiation Advertisement Register (Offset 0x04D8): P1ANAR

This register contains the auto-negotiation advertisement for the chip function.

TABLE 4-70: PHY 1 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (OFFSET 0X04D8): P1ANAR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	Next page NOT SUPPORTED	—
14	0	RO	Reserved	—
13	0	RO	Remote fault NOT SUPPORTED	—
12 - 11	0	RO	Reserved	—
10	1	R/W	Pause (follow control capability) 1 = Advertise pause ability 0 = Do not advertise pause ability	P1CR4, bit 4
9	0	R/W	Reserved	—
8	1	R/W	Adv 100 Full 1 = Advertise 100 full-duplex ability 0 = Do not advertise 100 full-duplex ability	P1CR4, bit 3
7	1	R/W	Adv 100 Half 1 = Advertise 100 half-duplex ability 0 = Do not advertise 100 half-duplex ability	P1CR4, bit 2
6	1	R/W	Adv 10 Full 1 = Advertise 10 full-duplex ability 0 = Do not advertise 10 full-duplex ability	P1CR4, bit 1
5	1	R/W	Adv 10 Half 1 = Advertise 10 half-duplex ability 0 = Do not advertise 10 half-duplex ability	P1CR4, bit 0
4 - 0	0_0001	RO	Selector field 802.3	—

PHY 1 Auto-Negotiation Link Partner Ability Register (Offset 0x04DA): P1ANLPR

This register contains the auto-negotiation link partner ability for the switch port 1 function.

TABLE 4-71: PHY 1 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (OFFSET 0X04DA): P1ANLPR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	Next page NOT SUPPORTED	—
14	0	RO	LP ACK NOT SUPPORTED	—
13	0	RO	Remote fault NOT SUPPORTED	—
12 - 11	0	RO	Reserved	—

TABLE 4-71: PHY 1 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (OFFSET 0X04DA): P1ANLPR (CONTINUED)

Bit	Default	R/W	Description	Bit Same As
10	0	RO	Pause Link partner pause capability	P1SR, bit 4
9	0	RO	Reserved	—
8	0	RO	Adv 100 Full Link partner 100 full capability	P1SR, bit 3
7	0	RO	Adv 100 Half Link partner 100 half capability	P1SR, bit 2
6	0	RO	Adv 10 Full Link partner 10 full capability	P1SR, bit 1
5	0	RO	Adv 10 Half Link partner 10 half capability	P1SR, bit 0
4 - 0	0_0000	RO	Reserved	—

PHY 2 MII Basic Control Register (Offset 0x04E0): P2MBCR

This register contains the MII control for the switch port 2 function.

TABLE 4-72: PHY 2 MII BASIC CONTROL REGISTER (OFFSET 0X04E0): P2MBCR

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	Soft reset Not supported.	—
14	0	R/W	**Loopback** 1 = Perform loopback as follows: Start: RXP2/RXM2 (Port 1) Loop back: PMD/PMA of Port 2's PHY End: TXP1/TXM1 (Port 1) 0 = Normal operation.	P2CR4, bit 8
13	0	R/W	**Force 100** 1 = 100 Mbps if AN is disabled (bit 12) 0 = 10 Mbps if AN is disabled (bit 12)	P2CR4, bit 6
12	1	R/W	**AN Enable** 1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	—
11	0	R/W	**Power-Down** 1 = Power-down. 0 = Normal operation.	P2CR4, bit11
10	0	RO	**Isolate** Not supported.	—
9	0	R/W	**Restart AN** 1 = Restart auto-negotiation. 0 = Normal operation.	P2CR4, bit13
8	0	R/W	**Force Full Duplex** 1 = Force full-duplex 0 = Force half-duplex.	P2CR4, bit5
7	0	RO	**Collision test** Not supported.	—
6	0	RO	Reserved	—
5	1	R/W	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Microchip Auto MDI-X mode.	P2CR4, bit15

TABLE 4-72: PHY 2 MII BASIC CONTROL REGISTER (OFFSET 0X04E0): P2MBCR (CONTINUED)

Bit	Default Value	R/W	Description	Bit Same As
4	0	R/W	**Force MDI-X** 1 = Force MDI-X. 0 = Normal operation.	P2CR4, bit9
3	0	R/W	**Disable MDI-X** 1 = Disable auto MDI-X. 0 = Normal operation.	P2CR4, bit10
2	0	R/W	**Disable Far-End-Fault** 1 = Disable far-end-fault detection. 0 = Normal operation.	P2CR4, bit12
1	0	R/W	**Disable Transmit** 1 = Disable transmit. 0 = Normal operation.	P2CR4, bit14
0	0	R/W	**Disable LED** 1 = Disable LED. 0 = Normal operation.	P2CR4, bit15

PHY 2 MII Basic Status Register (Offset 0x04E2): P2MBSR

This register contains the MII control for the switch port 2 function.

TABLE 4-73: PHY 2 MII REGISTER BASIC STATUS REGISTER (OFFSET 0X04E2): P2MBSR

Bit	Default	R/W	Description	Bit Same As
15	0	RO	T4 capable 1 = 100BASE-T4 capable 0 = Not 100BASE-T4 capable	—
14	1	RO	100 Full capable 1 = 100BASE-TX full-duplex capable 0 = Not 100BASE-TX full-duplex capable	Always 1
13	1	RO	100 Half capable 1 = 100BASE-TX half-duplex capable 0 = Not 100BASE-TX half-duplex capable	Always 1
12	1	RO	10 Full capable 1 = 10BASE-T full-duplex capable 0 = Not 10BASE-T full-duplex capable	Always 1
11	1	RO	10 Half capable 1 = 10BASE-T half-duplex capable 0 = Not 10BASE-T half-duplex capable	Always 1
10 - 7	0	RO	Reserved	—
6	0	RO	Preamble suppressed NOT SUPPORTED	—
5	0	RO	AN complete 1 = Auto-negotiation complete 0 = Auto-negotiation not completed	P1SR, bit 6
4	0	RO	Far end fault 1 = Far end fault detected 0 = No far end fault detected	P1SR, bit 8
3	1	RO	AN capable 1 = Auto-negotiation capable 0 = Not auto-negotiation capable	P1CR4, bit 7
2	0	RO	Link status 1 = Link is up 0 = Link is down	P1SR, bit 5

TABLE 4-73: PHY 2 MII REGISTER BASIC STATUS REGISTER (OFFSET 0X04E2): P2MBSR

Bit	Default	R/W	Description	Bit Same As
1	0	RO	Jabber test Not supported	—
0	0	RO	Extended capable 1 = Extended register capable 0 = Not extended register capable	—

PHY 2 PHYID Low Register (Offset 0x04E4): PHY2ILR

This register contains the PHY ID (low) for the switch port 2 function.

TABLE 4-74: PHY 2 PHYID LOW REGISTER (OFFSET 0X04E4): PHY2ILR

Bit	Default	R/W	Description
15 - 0	0x1430	RO	PHYID low Low order PHYID bits

PHY 2 PHYID High Register (Offset 0x04E6): PHY2IHR

This register contains the PHY ID (high) for the chip function.

TABLE 4-75: PHY 2 PHYID HIGH REGISTER (OFFSET 0X04E6): PHY2IHR

Bit	Default	R/W	Description
15 - 0	0x0022	RO	PHYID high High order PHYID bits

PHY 2 Auto-Negotiation Advertisement Register (Offset 0x04E8): P2ANAR

This register contains the auto-negotiation advertisement for the switch port 2 function.

TABLE 4-76: PHY 2 AUTO-NEGOTIATION ADVERTISEMENT REGISTER (OFFSET 0X04E8): P2ANAR

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	Next page Not supported.	—
14	0	RO	Reserved	—
13	0	RO	Remote fault Not supported.	—
12 - 11	0	RO	Reserved	—
10	1	R/W	Pause (flow control capability) 1 = Advertise pause capability. 0 = Do not advertise pause capability.	P2CR4, bit 4
9	0	RO	Reserved	—
8	1	R/W	Adv 100 Full 1 = Advertise 100 full-duplex capability. 0 = Do not advertise 100 full-duplex capability	P2CR4, bit 3
7	1	R/W	Adv 100 Half 1= Advertise 100 half-duplex capability. 0 = Do not advertise 100 half-duplex capability.	P2CR4, bit 2
6	1	R/W	Adv 10 Full 1 = Advertise 10 full-duplex capability. 0 = Do not advertise 10 full-duplex capability.	P2CR4, bit 1
5	1	R/W	Adv 10 Half 1 = Advertise 10 half-duplex capability. 0 = Do not advertise 10 half-duplex capability.	P2CR4, bit 0
4 - 0	0x01	RO	Selector Field 802.3	—

PHY 2 Auto-Negotiation Link Partner Ability Register (Offset 0x04EA): P2ANLPR

This register contains the auto-negotiation link partner ability for switch port 2 function.

TABLE 4-77: PHY 2 AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER (OFFSET 0X04EA): P2ANLPR

Bit	Default Value	R/W	Description	Bit Same As
15	0	RO	Next page Not supported.	—
14	0	RO	LP ACK Not supported.	—
13	0	RO	Remote fault Not supported.	—
12 - 11	0	RO	Reserved	—
10	0	RO	Pause Link partner pause capability.	P2SR, bit 4
9	0	RO	Reserved	—
8	0	RO	Adv 100 Full Link partner 100 full capability.	P2SR, bit3
7	0	RO	Adv 100 Half Link partner 100 half capability.	P2SR, bit2
6	0	RO	Adv 10 Full Link partner 10 full capability.	P2SR, bit1
5	0	RO	Adv 10 Half Link partner 10 half capability.	P2SR, bit0
4 - 0	0x01	RO	Reserved	—

PHY1 LinkMD® Control/Status (Offset 0x04F0): P1VCT

This register contains the LinkMD control and status of PHY 1.

TABLE 4-78: PHY1 LINKMD CONTROL/STATUS (OFFSET 0X04F0): P1VCT

Bit	Default	R/W	Description	Bit Same As
15	0	R/W SC	Vct_enable 1 = The cable diagnostic test is enabled. It'll be self-cleared after VCT test is done 0 = Indicates the cable diagnostic test is completed and the status information is valid for read	P1SCSLMD, bit 12
14 - 13	00	RO	Vct_result [00] = Normal condition [01] = Open condition has been detected in cable [10] = Short condition has been detected in cable [11] = Cable diagnostic test is failed	P1SCSLMD, bit 14:13
12	—	RO	Vct 10M short 1 = Less than 10 meter short	P1SCSLMD, bit 15
11 - 9	0	RO	Reserved	—
8 - 0	0	RO	Vct_fault_count Distance to the fault. The distance is approximately 0.4m x vct_fault_count	P1SCSLMD, bits 8:0

PHY2 Special Control/Status Register (Offset 0x04F2): P1PHYCTRL

This register contains the control and status information of PHY1.

TABLE 4-79: PHY2 SPECIAL CONTROL/STATUS REGISTER (OFFSET 0X04F2): P1PHYCTRL

Bit	Default Value	R/W	Description	Bit Same As
15 - 6	0	RO	Reserved	—
5	0	RO	Polarity Reverse (polrvs) 1 = Polarity is reversed. 0 = Polarity is not reversed.	P1SR, bit 13
4	0	RO	MDIX Status (mdix_st) 1 = MDI 0 = MDIX	P1SR, bit 7
3	0	R/W	Force Link (force_lnk) 1 = Force link pass. 0 = Normal operation.	P1SCSLMD, bit 11
2	1	R/W	Power Saving (pwrsave) 1 = Disable power saving. 0 = Enable power saving.	P1SCSLMD, bit 10
1	0	R/W	Remote (Near-end) Loopback 1 = Perform remote loopback at Port 1's PHY 0 = Normal operation	P1SCSLMD, bit 9
0	0	RO	Reserved	—

PHY2 LinkMD Control/Status (Offset 0x04F4): P2VCT

This register contains the LinkMD control and status information of PHY 2.

TABLE 4-80: PHY2 LINKMD CONTROL/STATUS (OFFSET 0X04F4): P2VCT

Bit	Default	R/W	Description	Bit Same As
15	0	R/W (Self-Clear)	Vct_enable 1 = Cable diagnostic test is enabled. It is self-cleared after the VCT test is done. 0 = Indicates that the cable diagnostic test is completed and the status information is valid for read.	P2SCSLMD, bit 12
14 - 13	0	RO	Vct_result [00] = Normal condition. [01] = Open condition detected in the cable. [10] = Short condition detected in the cable. [11] = Cable diagnostic test failed.	P2SCSLMD, bit 14 - 13
12	—	RO	Vct 10M Short 1 = Less than 10m short.	P2SCSLMD, bit 15
11 - 9	0	RO	Reserved	—
8 - 0	0	RO	Vct_fault_count Distance to the fault. The distance is approximately 0.4m*vct_fault_count.	P2SCSLMD, bit 8 - 0

PHY2 Special Control/Status Register (Offset 0x04F6): P2PHYCTRL

This register contains the control and status information of PHY2.

TABLE 4-81: PHY2 SPECIAL CONTROL/STATUS REGISTER (OFFSET 0X04F6): P2PHYCTRL

Bit	Default Value	R/W	Description	Bit Same As
15 - 6	0	RO	Reserved	—
5	0	RO	Polarity Reverse (polrvs) 1 = Polarity is reversed 0 = Polarity is not reversed	P2SR, bit 13
4	0	RO	MDIX Status (mdix_st) 1 = MDI 0 = MDIX	P2SR, bit 7
3	0	R/W	Force Link (force_lnk) 1 = Force link pass 0 = Normal operation	P2SCSLMD, bit 11
2	1	R/W	Power Saving (pwrsave) 1 = Disable power saving 0 = Enable power saving	P2SCSLMD, bit 10
1	0	R/W	Remote (Near-end) Loopback (rlb) 1 = Loop back at PMD/PMA of port 2's PHY 0 = Normal operation	P2SCSLMD, bit 9
0	0	RO	Reserved	—

Reserved (Offset 0x04F8 - 0x04FA)

Bit	Default	R/W	Description
15 - 0	0x0000	RO	Reserved

Port 1 Control Register 1 (Offset 0x0500): P1CR1

This register contains the global per port control for the switch port 1 function.

TABLE 4-82: PORT 1 CONTROL REGISTER 1 (OFFSET 0x0500): P1CR1

Bit	Default	R/W	Description
15 - 8	0x00	RO	Reserved
7	0	R/W	Broadcast Storm Protection Enable 1 = Enable broadcast storm protection for ingress packets on Port 1. 0 = Disable broadcast storm protection.
6	0	R/W	Diffserv Priority Classification Enable 1 = Enable DiffServ priority classification for ingress packets on Port 1. 0 = Disable DiffServ function.
5	0	R/W	802.1p Priority Classification Enable 1 = Enable 802.1p priority classification for ingress packets on Port 1. 0 = Disable 802.1p.
4 - 3	0x0	R/W	Port-Based Priority Classification 00 = Ingress packets on Port 1 are classified as priority 0 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on Port 1 are classified as priority 1 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on Port 1 are classified as priority 2 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on Port 1 are classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	Tag Insertion 1 = When packets are output on Port 1, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion.
1	0	RW	Tag Removal 1 = When packets are output on Port 1, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	TX Multiple Queues Select Enable 1 = the port output queue is split into four priority queues. 0 = single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.

Port 1 Control Register 2 (Offset 0x0502): P1CR2

This register contains the global per port control for the switch port 1 function.

TABLE 4-83: PORT 1 CONTROL REGISTER 2 (OFFSET 0x0502): P1CR2

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RW	Ingress VLAN Filtering 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	Discard Non PVID Packets 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	Force Flow Control 1 = Always enable flow control on the port, regardless of auto-negotiation result. 0 = The flow control is enabled based on auto-negotiation result.
11	0	RW	Back Pressure Enable 1 = Enable port's half-duplex back pressure. 0 = Disable port's half-duplex back pressure.
10	1	RW	Transmit Enable 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	Receive Enable 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	Learning Disable 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	Sniffer Port 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	Receive Sniff 1 = All packets received on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No receive monitoring.
5	0	RW	Transmit Sniff 1 = All packets transmitted on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No transmit monitoring.
4	0	RO	Reserved
3	0	RW	User Priority Ceiling 1 = If the packet's "priority field" is greater than the "user priority field" in the port VID control register bit[15:13], replace the packet's "priority field" with the "user priority field" in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet's "priority field."
2 - 0	111	RW	Port VLAN Membership Define the port's Port VLAN membership. Bit [2] stands for the host port, bit [1] for Port 2, and bit [0] for Port 1. The port can only communicate within the membership. A '1' includes a port in the membership; a '0' excludes a port from the membership.

Port 1 VID Control Register (Offset 0x0504): P1VIDCR

This register contains the global per port control for the switch port 1 function.

TABLE 4-84: PORT 1 VID CONTROL REGISTER (OFFSET 0X0504): P1VIDCR

Bit	Default	R/W	Description
15 - 13	000	RW	User Priority bits Port 1 tag [15:13] for priority
12	0	RW	CFI bit Port 1 tag [12] for CFI
11 - 0	0x001	RW	CFI bit Port 1 tag [11:0] for VID.

Note: P1VIDCR serve two purposes:

Associated with the ingress untagged packets, and used for egress tagging.

Default VID for the ingress untagged or null-VID-tagged packets, and used for address lookup.

Port 1 Control Register 3 (Offset 0x0506): P1CR3

This register contains the port 1 control register for the switch port 1 function.

TABLE 4-85: PORT 1 CONTROL REGISTER 3 (OFFSET 0X0506): P1CR3

Bit	Default	R/W	Description
15 - 4	0000	RO	Reserved
3 - 2	00	RW	Ingress Limit Mode These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	0	RW	Count Inter Frame Gap Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in ingress and egress rate calculations. 0 = IFG bytes are not counted.
0	0	RW	Count Preamble Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in ingress and egress rate limiting calculations. 0 = Preamble bytes are not counted.

Port 1 Ingress Rate Control Register (OFFSET 0X0508): P1IRCR

This register contains the port 1 ingress rate control register for the switch port 1 function.

TABLE 4-86: PORT 1 INGRESS RATE CONTROL REGISTER (O 0x0508): P1IRCR

Bit	Default	R/W	Description
15 - 12	0x0	RW	**Ingress Pri3 Rate** Priority 3 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).
11 - 8	0x0	RW	**Ingress Pri2 Rate** Priority 2 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).

TABLE 4-86: PORT 1 INGRESS RATE CONTROL REGISTER (O 0x0508): P1IRCR (CONTINUED)

Bit	Default	R/W	Description
7 - 4	0x0	RW	**Ingress Pri1 Rate** Priority 1 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).
3 - 0	0x0	RW	**Ingress Pri0 Rate** Priority 0 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).

Port 1 Egress Rate Control Register (Offset 0x050A): P1ERCR

This register contains the port 1 egress rate control register for the switch port 1 function.

TABLE 4-87: PORT 1 EGRESS RATE CONTROL REGISTER (OFFSET 0X050A): P1ERCR

Bit	Default	R/W	Description
15 - 12	0x0	RW	**Egress Pri3 Rate** Egress data rate limit for priority 3 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
11 - 8	0x0	RW	**Egress Pri2 Rate** Egress data rate limit for priority 2 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

TABLE 4-87: PORT 1 EGRESS RATE CONTROL REGISTER (OFFSET 0X050A): P1ERCR (CONTINUED)

Bit	Default	R/W	Description
7 - 4	0x0	RW	**Egress Pri1 Rate** Egress data rate limit for priority 1 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
3 - 0	0x0	RW	**Egress Pri0 Rate** Egress data rate limit for priority 0 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

Port 1 PHY Special Control/Status, LinkMD (Offset 0x0510): P1SCSLMD

This register contains the port LinkMD control register for the switch port 1 function.

TABLE 4-88: PORT 1 PHY SPECIAL CONTROL/STATUS, LINKMD (OFFSET 0X0510): P1SCSLMD

Bit	Default	R/W	Description	Bit Same As
15	0	RO	Vct 10M short Less than 10 meter short	P1VCT, bit 12
14 - 13	0	RO	Vct result [00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test is failed	P1VCT, bit 14 - 13
12	0	RO	Vct enable 1 = the cable diagnostic test is enabled. It'll be self-cleared after VCT test is done 0 = it indicates the cable diagnostic test is completed and the status information is valid for read	P1VCT, bit 15
11	0	RW SC	Force Link 1 = Force link pass 0 = Normal Operation	P1PHYCTRL, bit 3
10	1	RW	Power Saving 1 = Disable 0 = Enable power saving	P1PHYCTRL, bit 2
9	0	RW	Remote loop back 1 = Loop back at PMD/PMA of port 1's PHY 0 = normal operation	P1PHYCTRL, bit 1
8 - 0	0x000	RO	Vct fault count Distance to the fault. The distance is approximately 0.4mXvct_fault_count	P1PHYCTRL, bit 8 - 0

Port 1 Control Register 4 (Offset 0x0512): P1CR4

This register contains the global per port control for the chip function.

TABLE 4-89: PORT 1 CONTROL REGISTER 4 (OFFSET 0X0512): P1CR4

Bit	Default	R/W	Description	Bit Same As
15	0	R/W	LED off 1 = Turn off all port's LEDs (LED1_3, LED1_2, LED1_1, LED1_0. These pins will be driven high if this bit is set to one 0 = Normal operation	P1MBCR, bit 0
14	0	R/W	Txids 1 = Disable port's transmitter 0 = Normal operation	P1MBCR, bit 1
13	0	R/W	Restart AN 1 = Restart auto-negotiation 0 = Normal operation	P1MBCR, bit 9
12	0	R/W	Disable Far end fault 1 = Disable far end fault detection & pattern transmission. 0 = Enable far end fault detection & pattern transmission.	P1MBCR, bit 2
11	0	R/W	Power down 1 = Power down 0 = Normal operation	P1MBCR, bit 11
10	0	R/W	Disable auto MDI/MDIX 1 = Disable auto MDI/MDIX function 0 = Enable auto MDI/MDIX function	P1MBCR, bit 3
9	0	R/W	Force MDIX 1 = If auto MDI/MDIX is disabled, force PHY into MDIX mode 0 = Do not force PHY into MDIX mode	P1MBCR, bit 4
8	0	—	Loop Back 1 = perform loop back, as indicated: Start: RXP2/RXM2 (Port 2) Loop back: PMD/PMA of Port 1's PHY End: TXP2/YTXM2 (Port 2) 0 = Normal operation	P1MBCR, bit 14
7	1	R/W	Auto-Negotiation Enable 1 = Auto-negotiation is enable 0 = Disable auto-negotiation, speed and duplex are decided by bit 6 and 5 of the same register.	P1MBCR, bit 12
6	0	R/W	Force Speed 1 = Force 100BT if AN is disabled (bit 7) 0 = Force 10BT if AN is disabled (bit 7)	P1MBCR, bit 13
5	0	R/W	Force duplex 1 = Force full-duplex if (1) AN is disabled or (2) AN is enabled but failed. 0 = Force half-duplex if (1) AN is disabled or (2) AN is enabled but failed.	P1MBCR, bit 9
4	1	R/W	Advertised flow control capability 1 = Advertise flow control (pause) capability 0 = Suppress flow control (pause) capability from transmission to link partner	P1ANAR, bit 4
3	1	R/W	Advertised 100BT Full-duplex capability 1 = Advertise 100BT Full-duplex capability 0 = Suppress 100BT Full-duplex capability from transmission to link partner	P1ANAR, bit 3

TABLE 4-89: PORT 1 CONTROL REGISTER 4 (OFFSET 0X0512): P1CR4 (CONTINUED)

Bit	Default	R/W	Description	Bit Same As
2	1	R/W	Advertised 100BT half-duplex capability 1 = Advertise 100BT Half-duplex capability 0 = Suppress 100BT Half-duplex capability from transmission to link partner	P1ANAR, bit 2
1	1	R/W	Advertised 10BT Full-duplex capability 1 = Advertise 10BT Full-duplex capability 0 = Suppress 10BT Full-duplex capability from transmission to link partner	P1ANAR, bit 1
0	1	R/W	Advertised 10BT half-duplex capability 1 = Advertise 10BT Half-duplex capability 0 = Suppress 10BT Half-duplex capability from transmission to link partner	P1ANAR, bit 0

Port 1 Status Register (Offset 0x0514): P1SR

This register contains the global per port status for the chip function.

TABLE 4-90: PORT 1 STATUS REGISTER (OFFSET 0X0514): P1SR

Bit	Default	R/W	Description	Bit Same As
15	0	R/W	HP_mdix 1 = HP Auto MDIX mode 0 = Microchip Auto MDIX mode	P1MBCR, bit 5
14	0	RO	Reserved	—
13	0	RO	Polarity reverse 1 = Polarity is reversed 0 = Polarity is not reversed	P1PHYCTRL, bit 5
12	0	RO	Receive flow control enable 1 = Receive flow control feature is active 0 = Receive flow control feature is inactive	—
11	0	RO	Transmit flow control enable 1 = Transmit flow control feature is active 0 = Transmit flow control feature is inactive	—
10	0	RO	Operation Speed 1 = Link speed is 100 Mbps 0 = Link speed is 10 Mbps	—
9	0	RO	Operation duplex 1 = Link duplex is full 0 = Link duplex is half	—
8	0	RO	Far end fault 1 = Far end fault status detected 0 = No Far end fault status detected	P1MBSR, bit 4
7	0	RO	MDIX status 1 = MDIX 0 = MDI	P1PHYCTRL, bit 4
6	0	RO	AN done 1 = AN done 0 = AN not done	P1MBSR, bit 5
5	0	RO	Link good 1 = Link good 0 = Link not good	P1MBSR, bit 2

TABLE 4-90: PORT 1 STATUS REGISTER (OFFSET 0X0514): P1SR (CONTINUED)

Bit	Default	R/W	Description	Bit Same As
4	0	RO	Partner flow control capability 1 = Link partner flow control (pause) capable 0 = Link partner not flow control (pause) capable	P1ANLPR, bit 10
3	0	RO	Partner 100BT full-duplex capability 1 = Link partner 100BT full-duplex capable 0 = Link partner not 100BT full-duplex capable	P1ANLPR, bit 8
2	0	RO	Partner 100BT half-duplex capability 1 = Link partner 100BT half-duplex capable 0 = Link partner not 100BT half-duplex capable	P1ANLPR, bit 7
1	0	RO	Partner 10BT full-duplex capability 1 = Link partner 10BT full-duplex capable 0 = Link partner not 10BT full-duplex capable	P1ANLPR, bit 6
0	0	RO	Partner 10BT half-duplex capability 1 = Link partner 10BT half-duplex capable 0 = Link partner not 10BT half-duplex capable	P1ANLPR, bit 5

Reserved (Offset 0x0516 – 0x051A)

TABLE 4-91: RESERVED (OFFSET 0X0516 – 0X051A)

Bit	Default	R/W	Description
15 - 0	0x0000	RO	Reserved

Port 2 Control Register 1 (Offset 0x0520): P2CR1

This register contains the global per port control for the switch port 2 function.

TABLE 4-92: PORT 2 CONTROL REGISTER 1 (OFFSET 0x0520): P2CR1

Bit	Default	R/W	Description
15 - 8	0x00	RO	Reserved
7	0	R/W	Broadcast Storm Protection Enable 1 = Enable broadcast storm protection for ingress packets on Port 1. 0 = Disable broadcast storm protection.
6	0	R/W	Diffserv Priority Classification Enable 1 = Enable DiffServ priority classification for ingress packets on Port 1. 0 = Disable DiffServ function.
5	0	R/W	802.1p Priority Classification Enable 1 = Enable 802.1p priority classification for ingress packets on Port 1. 0 = Disable 802.1p.
4 - 3	0x0	R/W	Port-Based Priority Classification 00 = Ingress packets on Port 1 are classified as priority 0 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on Port 1 are classified as priority 1 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on Port 1 are classified as priority 2 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on Port 1 are classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	Tag Insertion 1 = When packets are output on Port 1, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion.
1	0	RW	Tag Removal 1 = When packets are output on Port 1, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	TX Multiple Queues Select Enable 1 = the port output queue is split into four priority queues. 0 = single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.

Port 2 Control Register 2 (Offset 0x0522): P2CR2

This register contains the global per port control for the switch port 2 function.

TABLE 4-93: PORT 2 CONTROL REGISTER 2 (OFFSET 0x0522): P2CR2

Bit	Default	R/W	Description
15	0	RO	Reserved
14	0	RW	Ingress VLAN Filtering 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	Discard Non PVID Packets 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	Force Flow Control 1 = Always enable flow control on the port, regardless of auto-negotiation result. 0 = The flow control is enabled based on auto-negotiation result.
11	0	RW	Back Pressure Enable 1 = Enable port's half-duplex back pressure. 0 = Disable port's half-duplex back pressure.
10	1	RW	Transmit Enable 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	Receive Enable 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	Learning Disable 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	Sniffer Port 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	Receive Sniff 1 = All packets received on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No receive monitoring.
5	0	RW	Transmit Sniff 1 = All packets transmitted on the port are marked as "monitored packets" and forwarded to the designated "sniffer port." 0 = No transmit monitoring.
4	0	RO	Reserved
3	0	RW	User Priority Ceiling 1 = If the packet's "priority field" is greater than the "user priority field" in the port VID control register bit[15:13], replace the packet's "priority field" with the "user priority field" in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet's "priority field."
2 - 0	111	RW	Port VLAN Membership Define the port's Port VLAN membership. Bit [2] stands for the host port, bit [1] for Port 2, and bit [0] for Port 1. The port can only communicate within the membership. A '1' includes a port in the membership; a '0' excludes a port from the membership.

Port 2 VID Control Register (Offset 0x0524): P2VIDCR

This register contains the global per port control for the switch port 2 function.

TABLE 4-94: PORT 2 VID CONTROL REGISTER (0X0524): P2VIDCR

Bit	Default	R/W	Description
15 - 13	000	RW	User Priority bits Port 2 tag [15-13] for priority
12	0	RW	CFI bit Port 2 tag [12] for CFI
11 - 0	0x001	RW	CFI bit Port 2 tag [11-0] for VID.

Note: P2VIDCR serve two purposes:

Associated with the ingress untagged packets, and used for egress tagging.

Default VID for the ingress untagged or null-VID-tagged packets, and used for address lookup.

Port 2 Control Register 3 (Offset 0x0526): P2CR3

This register contains the control register for the switch port 2 function.

TABLE 4-95: PORT 2 CONTROL REGISTER 3 (OFFSET 0X0526): P2CR3

Bit	Default	R/W	Description
15 - 4	0000	RO	Reserved
3 - 2	00	RW	Ingress Limit Mode These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	0	RW	Count Inter Frame Gap Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in ingress and egress rate calculations. 0 = IFG bytes are not counted.
0	0	RW	Count Preamble Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in ingress and egress rate limiting calculations. 0 = Preamble bytes are not counted.

Port 2 Ingress Rate Control Register (Offset 0x0528): P2IRCR

This register contains the port 2 ingress rate control register for the switch port 2 function.

TABLE 4-96: PORT 2 INGRESS RATE CONTROL REGISTER (OFFSET 0X0528): P2IRCR

Bit	Default	R/W	Description
15 - 12	0x0	RW	**Ingress Pri3 Rate** Priority 3 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).
11 - 8	0x0	RW	**Ingress Pri2 Rate** Priority 2 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).

TABLE 4-96: PORT 2 INGRESS RATE CONTROL REGISTER (OFFSET 0X0528): P2IRCR

Bit	Default	R/W	Description
7 - 4	0x0	RW	**Ingress Pri1 Rate** Priority 1 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).
3 - 0	0x0	RW	**Ingress Pri0 Rate** Priority 0 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).

Port 2 Egress Rate Control Register (Offset 0x052A): P2ERCR

This register contains the port 2 egress rate control register for the switch port 2 function.

TABLE 4-97: PORT 1 EGRESS RATE CONTROL REGISTER (OFFSET 0X052A): P2ERCR

Bit	Default	R/W	Description
15 - 12	0x0	RW	**Egress Pri3 Rate** Egress data rate limit for priority 3 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
11 - 8	0x0	RW	**Egress Pri2 Rate** Egress data rate limit for priority 2 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

TABLE 4-97: PORT 1 EGRESS RATE CONTROL REGISTER (OFFSET 0X052A): P2ERCR (CONTINUED)

Bit	Default	R/W	Description
7 - 4	0x0	RW	**Egress Pri1 Rate** Egress data rate limit for priority 1 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
3 - 0	0x0	RW	**Egress Pri0 Rate** Egress data rate limit for priority 0 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

Port 2 PHY Special Control/Status, LinkMD (Offset 0x0530): P2SCSLMD

This register contains the port 2 LinkMD control register for the switch port 2 function.

TABLE 4-98: PORT 2 PHY SPECIAL CONTROL/STATUS, LINKMD (OFFSET 0X0530): P2SCSLMD

Bit	Default	R/W	Description	Bit Same As
15	0	RO	Vct 10M short Less than 10 meter short	P2VCT, bit 12
14 - 13	0	RO	Vct result [00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test is failed	P2VCT, bit 14 - 13
12	0	RO	Vct enable 1 = the cable diagnostic test is enabled. It'll be self-cleared after VCT test is done 0 = it indicates the cable diagnostic test is completed and the status information is valid for read	P2VCT, bit 15
11	0	RW (self-clear)	Force Link 1 = Force link pass 0 = Normal Operation	P21PHYCTRL, bit 3
10	1	RW	Power Saving 1 = Disable 0 = Enable power saving	P2PHYCTRL, bit 2
9	0	RW	Remote loop back 1 = Loop back at PMD/PMA of port 2's PHY 0 = normal operation	P2PHYCTRL, bit 1
8 - 0	0	RO	Vct fault count Distance to the fault. The distance is approximately 0.4mxvct_fault_count	P2VCT, bit 8 - 0

Port 2 Control Register 4 (Offset 0x0532): P2CR4

This register contains the global per port control for the switch port 2 function.

TABLE 4-99: PORT 2 CONTROL REGISTER 4 (OFFSET 0X0532): P2CR4

Bit	Default	R/W	Description	Bit Same As:
15	0	RW	LED Off 1 = Turn off all of the port 2's LEDs (P2LED3, P2LED2, P2LED1, P2LED0). These pins are driven high if this bit is set to one 0 = normal operation	P2MBCR, bit 0
14	0	RW	Txids 1 = disable the port's transmitter 0 = normal operation	P2MBCR, bit 1
13	0	RW	Restart Auto-Negotiation 1 = Restart auto-negotiation 0 = Normal operation	P2MBCR, bit 9
12	0	RW	Reserved	P2MBCR, bit 2
11	0	RW	Power Down 1 = Power down 0 = Normal operation	P2MBCR, bit 11
10	0	RW	Disable Auto MDI/MDI-X 1 = Disable Auto-MDI/MDI-X function 0 = Enable Auto-MDI/MDI-X function	P2MBCR, bit 3

TABLE 4-99: PORT 2 CONTROL REGISTER 4 (OFFSET 0X0532): P2CR4 (CONTINUED)

Bit	Default	R/W	Description	Bit Same As:
9	0	RW	Force MDI-X 1 = If Auto-MDI/MDI-X is disabled, force PHY into MDI-X mode 0 = Do not force PHY into MDI-X mode	P2MBCR, bit 4
8	0	RW	Far-End Loopback 1 = Perform loopback, as indicated: Start: RXP2/RXM2 (Port 2) Loopback: PMD/PMA of Port 1's PHY End: TXP2/TXM2 (Port 2) 0 = Normal operation	P2MBCR, bit 14
7	1	RW	Auto-Negotiation Enable 1 = Auto-negotiation is enabled 0 = Disable auto-negotiation, speed, and duplex are decided by bits [6:5] of the same register	P2MBCR, bit 12
6	1	RW	Force Speed 1 = Force 100BT if auto-negotiation is disabled (bit [7]) 0 = Force 10BT if auto-negotiation is disabled (bit [7])	P2MBCR, bit 13
5	1	RW	Force Duplex 1 = Force full-duplex if auto-negotiation is disabled 0 = Force half-duplex if auto-negotiation is disabled This bit also determines duplex if auto-negotiation is enabled but fails. When AN is enabled, this bit should be set to zero	P2MBCR, bit 8
4	1	RW	Advertised Flow Control Capability 1 = Advertise flow control (pause) capability. 0 = Suppress flow control (pause) capability from transmission to link partner	P1ANAR, bit 10
3	1	RW	Advertised 100BT Full-Duplex Capability 1 = Advertise 100BT full-duplex capability. 0 = Suppress 100BT full-duplex capability from transmission to link partner.	P1ANAR, bit 8
2	1	RW	Advertised 100BT Half-Duplex Capability 1 = Advertise 100BT half-duplex capability. 0 = Suppress 100BT half-duplex capability from transmission to link partner.	P1ANAR, bit 7
1	1	RW	Advertised 10BT Full-Duplex Capability 1 = Advertise 10BT full-duplex capability. 0 = Suppress 10BT full-duplex capability from transmission to link partner.	P1ANAR, bit 6
0	1	RW	Advertised 10BT Half-Duplex Capability 1 = Advertise 10BT half-duplex capability. 0 = Suppress 10BT half-duplex capability from transmission to link partner.	P1ANAR, bit 5

Port 2 Status Register (Offset 0x0534): P2SR

This register contains the global per port status for the chip function.

TABLE 4-100: PORT 2 STATUS REGISTER (OFFSET 0X0534): P2SR

Bit	Default Value	R/W	Description	Same Bit As
15	1	R/W	**HP_mdix** 1 = HP Auto MDI-X mode. 0 = Microchip Auto MDI-X mode.	P2MBCR, bit 5
14	0	RO	Reserved	—
13	0	RO	**Polarity Reverse** 1 = Polarity is reversed. 0 = Polarity is not reversed.	P2PHYCTRL, bit 5
12	0	RO	**Receive Flow Control Enable** 1 = Receive flow control feature is active. 0 = Receive flow control feature is inactive.	—
11	0	RO	**Transmit Flow Control Enable** 1 = Transmit flow control feature is active. 0 = Transmit flow control feature is inactive.	—
10	0	RO	**Operation Speed** 1 = Link speed is 100 Mbps. 0 = Link speed is 10 Mbps.	—
9	0	RO	**Operation Duplex** 1 = Link duplex is full. 0 = Link duplex is half.	—
8	0	RO	Reserved	P2MBCR, bit 4
7	0	RO	**MDI-X Status** 1 = MDI. 0 = MDI-X.	P2PHYCTRL, bit 4
6	0	RO	**AN Done** 1 = AN done. 0 = AN not done.	P2MBSR, bit 5
5	0	RO	**Link Good** 1 = Link good. 0 = Link not good.	P2ANLPR, bit 2
4	0	RO	**Partner flow control capability** 1 = Link partner flow control (pause) capable. 0 = Link partner not flow control (pause) capable.	P2ANLPR, bit 10
3	0	RO	**Partner 100BT full-duplex capability** 1 = Link partner 100BT full-duplex capable. 0 = Link partner not 100BT full-duplex capable.	P2ANLPR, bit 8
2	0	RO	**Partner 100BT half-duplex capability** 1 = Link partner 100BT half-duplex capable. 0 = Link partner not 100BT half-duplex capable.	P2ANLPR, bit 7
1	0	RO	**Partner 10BT full-duplex capability** 1 = Link partner 10BT full-duplex capable. 0 = Link partner not 10BT full-duplex capable.	P2ANLPR, bit 6
0	0	RO	**Partner 10BT half-duplex capability** 1 = Link partner 10BT half-duplex capable. 0 = Link partner not 10BT half-duplex capable.	P2ANLPR, bit 5

Port 2 Reserved (Offset 0x0536 – 0x053A)

This register is reserved.

Bit	Default	R/W	Description
15 - 0	0x0000	RO	Reserved

Host Control Register 1 (Offset 0x0540): P3CR1

This register contains the global per port control for the switch host port function.

TABLE 4-101: HOST CONTROL REGISTER 1 (OFFSET 0X0540): P3CR1

Bit	Default	R/W	Description
15 - 8	0x00	RO	Reserved
7	0	R/W	Broadcast Storm Protection Enable 1 = Enable broadcast storm protection for ingress packets on Port 1. 0 = Disable broadcast storm protection.
6	0	R/W	Diffserv Priority Classification Enable 1 = Enable DiffServ priority classification for ingress packets on Port 1. 0 = Disable DiffServ function.
5	0	R/W	802.1p Priority Classification Enable 1 = Enable 802.1p priority classification for ingress packets on Port 1. 0 = Disable 802.1p.
4 - 3	0x0	R/W	Port-Based Priority Classification 00 = Ingress packets on Port 1 are classified as priority 0 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 01 = Ingress packets on Port 1 are classified as priority 1 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 10 = Ingress packets on Port 1 are classified as priority 2 queue if “DiffServ” or “802.1p” classification is not enabled or fails to classify. 11 = Ingress packets on Port 1 are classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. Note: “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.
2	0	RW	Tag Insertion 1 = When packets are output on Port 1, the switch adds 802.1p/q tags to packets without 802.1p/q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID”. 0 = Disable tag insertion.
1	0	RW	Tag Removal 1 = When packets are output on Port 1, the switch removes 802.1p/q tags from packets with 802.1p/q tags when received. The switch will not modify packets received without tags. 0 = Disable tag removal.
0	0	RW	TX Multiple Queues Select Enable 1 = the port output queue is split into four priority queues. 0 = single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.

Host Control Register 2 (Offset 0x0542): P3CR2

This register contains the global per port control for the switch host port function.

TABLE 4-102: HOST CONTROL REGISTER 2 (OFFSET 0X0542): P3CR2

Bit	Default	R/W	Description
15	0	RW	Reserved
14	0	RW	Ingress VLAN Filtering 1 = The switch discards packets whose VID port membership in VLAN table bits [18:16] does not include the ingress port VID. 0 = No ingress VLAN filtering.
13	0	RW	Discard Non PVID Packets 1 = The switch discards packets whose VID does not match the ingress port default VID. 0 = No packets are discarded.
12	0	RW	Reserved. For factory testing purpose only. Always write 0.
11	0	RW	Reserved Must be 0
10	1	RW	Transmit Enable 1 = Enable packet transmission on the port. 0 = Disable packet transmission on the port.
9	1	RW	Receive Enable 1 = Enable packet reception on the port. 0 = Disable packet reception on the port.
8	0	RW	Learning Disable 1 = Disable switch address learning capability. 0 = Enable switch address learning.
7	0	RW	Sniffer Port 1 = Port is designated as a sniffer port and transmits packets that are monitored. 0 = Port is a normal port.
6	0	RW	Receive Sniff 1 = All packets received on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No receive monitoring.
5	0	RW	Transmit Sniff 1 = All packets transmitted on the port are marked as “monitored packets” and forwarded to the designated “sniffer port.” 0 = No transmit monitoring.
4	0	RO	Reserved
3	0	RW	User Priority Ceiling 1 = If the packet’s “priority field” is greater than the “user priority field” in the port VID control register bit[15:13], replace the packet’s “priority field” with the “user priority field” in the port VID control register bit[15:13]. 0 = Do not compare and replace the packet’s “priority field.”
2 - 0	111	RW	Port VLAN Membership Define the port’s Port VLAN membership. Bit [2] stands for the host port, bit [1] for Port 2, and bit [0] for Port 1. The port can only communicate within the membership. A ‘1’ includes a port in the membership; a ‘0’ excludes a port from the membership.

Host VID Control Register (Offset 0x0544): P3VIDCR

This register contains the global per port control for the switch host port function.

TABLE 4-103: HOST VID CONTROL REGISTER (OFFSET 0X0544): P3VIDCR

Bit	Default	R/W	Description
15 - 13	000	RW	User Priority bits Port 1 tag [15:13] for priority
12	0	RW	CFI bit Port 1 tag [12] for CFI
11 - 0	0x001	RW	CFI bit Port 1 tag [11:0] for VID

Note: P3VIDCR serve two purposes:

Associated with the ingress untagged packets, and used for egress tagging.

Default VID for the ingress untagged or null-VID-tagged packets, and used for address lookup.

Host Control Register 3 (Offset 0x0546): P3CR3

This register contains the host port control register for the switch host port function.

TABLE 4-104: HOST CONTROL REGISTER 3 (OFFSET 0X0546): P3CR3

Bit	Default	R/W	Description
15 - 4	0000	RO	Reserved
3 - 2	00	RW	Ingress Limit Mode These bits determine what kinds of frames are limited and counted against ingress rate limiting as follows: 00 = Limit and count all frames. 01 = Limit and count Broadcast, Multicast, and flooded Unicast frames. 10 = Limit and count Broadcast and Multicast frames only. 11 = Limit and count Broadcast frames only.
1	0	RW	Count Inter Frame Gap Count IFG Bytes. 1 = Each frame's minimum inter frame gap. IFG bytes (12 per frame) are included in ingress and egress rate calculations. 0 = IFG bytes are not counted.
0	0	RW	Count Preamble Count preamble Bytes. 1 = Each frame's preamble bytes (8 per frame) are included in ingress and egress rate limiting calculations. 0 = Preamble bytes are not counted.

Host Ingress Rate Control Register (Offset 0x0548): P3IRCR

This register contains the host port ingress rate control register for the switch host port function.

TABLE 4-105: HOST INGRESS RATE CONTROL REGISTER (OFFSET 0X0548): P3IRCR

Bit	Default	R/W	Description
15 - 12	0x0	RW	**Ingress Pri3 Rate** Priority 3 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).
11 - 8	0x0	RW	**Ingress Pri2 Rate** Priority 2 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).

TABLE 4-105: HOST INGRESS RATE CONTROL REGISTER (OFFSET 0X0548): P3IRCR (CONTINUED)

Bit	Default	R/W	Description
7 - 4	0x0	RW	**Ingress Pri1 Rate** Priority 1 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).
3 - 0	0x0	RW	**Ingress Pri0 Rate** Priority 0 frames will be discarded after the ingress rate selected as shown below is reached or exceeded. 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Note: For 10BT, rate settings above 10 Mbps are set to the default value 0000 (not limited).

Host Egress Rate Control Register (Offset 0x054A): P3ERCR

This register contains the host port egress rate control register for the switch host port function.

TABLE 4-106: HOST EGRESS RATE CONTROL REGISTER (OFFSET 0X054A): P3ERCR

Bit	Default	R/W	Description
15 - 12	0x0	RW	**Egress Pri3 Rate** Egress data rate limit for priority 3 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
11 - 8	0x0	RW	**Egress Pri2 Rate** Egress data rate limit for priority 2 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

TABLE 4-106: HOST EGRESS RATE CONTROL REGISTER (OFFSET 0X054A): P3ERCR (CONTINUED)

Bit	Default	R/W	Description
7 - 4	0x0	RW	**Egress Pri1 Rate** Egress data rate limit for priority 1 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.
3 - 0	0x0	RW	**Egress Pri0 Rate** Egress data rate limit for priority 0 frames. Output traffic from this priority queue is shaped according to the egress rate selected below: 0000 = Not limited (default) 0001 = 64 Kbps 0010 = 128 Kbps 0011 = 256 Kbps 0100 = 512 Kbps 0101 = 1 Mbps 0110 = 2 Mbps 0111 = 4 Mbps 1000 = 8 Mbps 1001 = 16 Mbps 1010 = 32 Mbps 1011 = 48 Mbps 1100 = 64 Mbps 1101 = 72 Mbps 1110 = 80 Mbps 1111 = 88 Mbps Notes: For 10BT, rate settings above 10Mbps are set to the default value 0000 (not limited). When multiple queue select enable is off (only 1 queue per port), rate limiting applies only to priority 0 queue.

Reserved (Offset 0x0550)

This register is reserved.

TABLE 4-107: RESERVED (OFFSET 0X0550)

Bit	Default	R/W	Description
15 - 0	0x0000	RO	Reserved

Reserved (Offset 0x0554)

This register is reserved.

TABLE 4-108: RESERVED (OFFSET 0X0554)

Bit	Default	R/W	Description
15 - 0	0x0000	RO	Reserved

Reserved (Offset 0x0556)

This register is reserved.

TABLE 4-109: RESERVED (OFFSET 0X0556)

Bit	Default	R/W	Description
15 - 0	0x0000	RO	Reserved

Reserved (Offset 0x0560)

This register is reserved for internal testing.

TABLE 4-110: RESERVED (OFFSET 0X0560)

Bit	Default	R/W	Description
15 - 10	0x00	RO	Reserved
9 - 0	—	RO	Reserved

4.5 Management Information Base (MIB) Counters

The KSZ8842-PMQL/PMBL provides 32 MIB counters for port 1, port 2, and the host port. These counters are used to monitor the port activity for network management. The MIB counters are formatted “per port” and “per all port dropped packet” as shown in Table 4-111.

TABLE 4-111: FORMAT OF PER PORT MIB COUNTERS

Bit	Name	R/W	Description	Default
31	Overflow	RO	1 = Counter overflow. 0 = No counter overflow.	0
30	Count Valid	RO	1 = Counter value is valid. 0 = Counter value is not valid.	0
29 - 0	Counter Values	RO	Counter value	0

“Per Port” MIB counters are read using indirect memory access. The base address offsets and address ranges for both Ethernet ports are:

Port 1, base address of the MIB counter is 0x00 and range is (0x00 - 0x1f) as shown in Table 4-112.

Port 2, base address of the MIB counter is 0x20 and range is (0x20 - 0x3f) as shown in Table 4-112.

Host port, base address of the MIB counter is 0x40 and range is (0x40 - 0x5f) as shown in Table 4-112.

Per Port MIB counters read/write functions use Access Control register IACR (0x04A0) bit 12. The base address offset and address range for port 1 is 0x00 and range is (0x00 - 0x1F) that can be changed in register IACR (0x04A0) bits[9:0]. The data of MIB counters are from the Indirect Access data register IADR4 (0x04A8) and IADR5 (0x04AA) based on Table 4-112.

TABLE 4-112: PORT 1’S “PER PORT” MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx lo-priority (default) octet count including bad packets
0x1	Reserved	Reserved
0x2	RxUndersizePkt	Rx undersize packets w/ good CRC
0x3	RxFragments	Rx fragment packets w/ bad CRC, symbol errors or alignment errors
0x4	RxOversize	Rx oversize packets w/ good CRC (max: 1536 bytes)
0x5	RxJabbers	Rx packets longer than 1536 bytes w/ either CRC errors, alignment errors, or symbol errors
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal packet size
0x7	RxCRCError	Rx packets within (64,1916) bytes w/ an integral number of bytes and a bad CRC
0x8	RxAlignmentError	Rx packets within (64,1916) bytes w/ a non-integral number of bytes and a bad CRC
0x9	RxControl8808Pkts	Number of MAC control frames received by a port with 88-08h in EtherType field
0xA	RxPausePkts	Number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC
0xB	RxBroadcast	Rx good broadcast packets (not including error broadcast packets or valid multicast packets)
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, error multicast packets or valid broadcast packets)
0xD	RxUnicast	Rx good unicast packets
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length

TABLE 4-112: PORT 1'S "PER PORT" MIB COUNTERS INDIRECT MEMORY OFFSETS (CONTINUED)

Offset	Counter Name	Description
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1916 octets in length
0x14	TxLoPriorityByte	Tx lo-priority good octet count, including PAUSE packets
0x15	Reserved	Reserved
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet
0x17	TxPausePkts	Number of PAUSE frames transmitted by a port
0x18	TxBroadcastPkts	Tx good broadcast packets (not including error broadcast or valid multicast packets)
0x19	TxMulticastPkts	Tx good multicast packets (not including error multicast packets or valid broadcast packets)
0x1A	TxUnicastPkts	Tx good unicast packets
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium
0x1C	TxTotalCollision	Tx total collision, half-duplex only
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision

TABLE 4-113: ALL PORTS DROPPED PACKET" MIB COUNTERS FORMAT

Bit	Default	R/W	Description
30 - 16	—	RO	Reserved
15 - 0	0x0000	RO	Counter value

Note: "All Ports Dropped Packet" MIB Counters do not indicate overflow or validity; therefore, the application must keep track of overflow and valid conditions.

"All Ports Dropped Packet" MIB counters are read using indirect memory access. The address offsets for these counters are shown in Table 4-114.

TABLE 4-114: ALL PORTS DROPPED PACKET" MIB COUNTERS INDIRECT MEMORY OFFSETS

Offset	Counter Name	Description
0x100	Port1 TX Drop Packets	TX packets dropped due to lack of resources
0x101	Port2 TX Drop Packets	TX packets dropped due to lack of resources
0x103	Port1 RX Drop Packets	RX packets dropped due to lack of resources
0x104	Port2 RX Drop Packets	RX packets dropped due to lack of resources

Examples:

1. MIB Counter Read (read port 1 “Rx64Octets” counter at indirect address offset 0x0E)

Write to reg. IACR with 0x1C0E (set indirect address and trigger a read MIB counters operation)

Then

Read reg. IADR5 (MIB counter value 31-16) // If bit 31 = 1, there was a counter overflow

// If bit 30 = 0, restart (re-read) from this register

Read reg. IADR4 (MIB counter value 15-0)

2. MIB Counter Read (read port 2 “Rx64Octets” counter at indirect address offset 0x2E)

Write to reg. IACR with 0x1C2E (set indirect address and trigger a read MIB counters operation)

Then

Read reg. IADR5 (MIB counter value 31-16) // If bit 31 = 1, there was a counter overflow

// If bit 30 = 0, restart (re-read) from this register

Read reg. IADR4 (MIB counter value 15-0)

3. MIB Counter Read (read “Port1 TX Drop Packets” counter at indirect address offset 0x100)

Write to reg. IACR with 0x1d00 (set indirect address and trigger a read MIB counters operation)

Then

Read reg. IADR4 (MIB counter value 15-0)

4.5.1 ADDITIONAL MIB INFORMATION

Per Port MIB counters are designed as “read clear”. That is, these counters will be cleared after they are read.
All Ports Dropped Packet MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

4.6 Static MAC Address Table

The KSZ8842-PMQL/PMBL supports both a static and a dynamic MAC address table. In response to a Destination Address (DA) look up, The KSZ8842-PMQL/PMBL searches both tables to make a packet forwarding decision. In response to a Source Address (SA) look up, only the dynamic table is searched for aging, migration and learning purposes.

The static DA look up result takes precedence over the dynamic DA look up result. If there is a DA match in both tables, the result from the static table is used. These entries in the static table will not be aged out by the KSZ8842-PMQL/PMBL.

TABLE 4-115: STATIC MAC TABLE FORMAT (8 ENTRIES)

Bit	Default Value	R/W	Description
57 - 54	0000	RW	FID Filter VLAN ID − identifies one of the 16 active VLANs.
53	0	R/W	Use FID 1 = Specifies the use of FID+MAC for static table look up. 0 = Specifies only the use of MAC for static table look up.
52	0	R/W	Override 1 = Overrides the port setting transmit enable = “0” or receive enable = “0” setting. 0 = Specifies no override.
51	0	R/W	Valid 1 = Specifies that this entry is valid, and the look up result will be used. 0 = Specifies that this entry is not valid.
50 - 48	000	R/W	Forwarding Ports These 3 bits control the forwarding port(s): 000 = No forward. 001 = Forward to Port 1. 010 = Forward to Port 2. 100 = Forward to Port 3. 011 = Forward to Port 1 and Port 2. 110 = Forward to Port 2 and Port 3. 101 = Forward to Port 1 and Port 3. 111 = Broadcasting (excluding the ingress port).
47 - 0	0	R/W	MAC Address 48−bit MAC Address

Static MAC Table Lookup Examples:

Static Address Table Read (read the second entry at indirect address offset 0x01)

Write to Reg. IACR with 0x1001 (set indirect address and trigger a read static MAC table operation)

Then:

Read Reg. IADR3 (static MAC table bits [57:48])

Read Reg. IADR2 (static MAC table bits [47:32])

Read Reg. IADR5 (static MAC table bits [31:16])

Read Reg. IADR4 (static MAC table bits [15:0])

Static Address Table Write (write the eighth entry at indirect address offset 0x07)

Write to Reg. IADR3 (static MAC table bits [57:48])

Write to Reg. IADR2 (static MAC table bits[47:32])

Write to Reg. IADR5 (static MAC table bits [31:16])

Write to Reg. IADR4 (static MAC table bits [15:0])

Write to Reg. IACR with 0x0007 (set indirect address and trigger a write static MAC table operation)

4.7 Dynamic MAC Address Table

The Dynamic MAC Address (Table 4-116) is a read-only table.

TABLE 4-116: DYNAMIC MAC ADDRESS TABLE FORMAT (1024 ENTRIES)

Bit	Default	R/W	Description
71	—	RO	Data Not Ready 1 = Specifies that the entry is not ready, continue retrying until bit is set to “0”. 0 = Specifies that the entry is ready.
70 - 67	—	RO	Reserved
66	1	RO	MAC Empty 1 = Specifies that there is no valid entry in the table 0 = Specifies that there are valid entries in the table
65 - 56	00_0000_0000	RO	Number of Valid Entries Indicates how many valid entries in the table. 0x3ff means 1K entries. 0x001 means 2 entries. 0x000 and bit [66] = “0” means 1 entry. 0x000 and bit [66] = “1” means 0 entry.
55 - 54	—	RO	Timestamp Specifies the 2−bit counter for internal aging.
53 - 52	00	RO	Source Port Identifies the source port where FID+MAC is learned: 00 = Port 1 01 = Port 2 10 = Port 3 (host port)
51 - 48	0x0	RO	FID Specifies the filter ID.
47 - 0	0x0000_0000_0000	RO	MAC Address Specifies the 48−bit MAC Address.

Dynamic MAC Address Lookup Example:

1. Dynamic MAC Address Table Read (read the first entry at indirect address offset 0 and retrieve the MAC table size)

Write to Reg. IACR with 0x1800 (set indirect address and trigger a read dynamic MAC table operation)

Then:

Read Reg. IADR1 (dynamic MAC table bits [71:64]) // If bit [71] = “1”, restart (re-read) from this register

Read Reg. IADR3 (dynamic MAC table bits [63:48])

Read Reg. IADR2 (dynamic MAC table bits [47:32])

Read Reg. IADR5 (dynamic MAC table bits [31:16])

Read Reg. IADR4 (dynamic MAC table bits [15:0])

4.8 VLAN Table

The KSZ8862M uses the VLAN table to perform look-ups. If 802.1Q VLAN mode is enabled (SGCR2[15]), this table will be used to retrieve the VLAN information that is associated with the ingress packet. This information includes FID (Filter ID), VID (VLAN ID), and VLAN membership as described in Table 4-117:

TABLE 4-117: VLAN TABLE FORMAT (16 ENTRIES)

Bit	Default	R/W	Description
19	1	RW	Valid 1 = Specifies that this entry is valid, the look up result will be used. 0 = Specifies that this entry is not valid.
18 - 16	111	R/W	Membership Specifies which ports are members of the VLAN. If a DA look up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. For example: “101” means Port 3 and Port 1 are in this VLAN.
15 - 12	0x0	R/W	FID Specifies the Filter ID. The KSZ8852 supports 16 active VLANs represented by these four bit fields. The FID is the mapped ID. If 802.1Q VLAN is enabled, the look up will be based on FID+DA and FID+SA.
11 - 0	0x001	R/W	VID Specifies the IEEE 802.1Q 12 bits VLAN ID.

If 802.1Q VLAN mode is enabled, then KSZ8842-PMQL/PMBL will assign a VID to every ingress packet. If the packet is untagged or tagged with a null VID, then the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, then VID in the tag will be used. The look up process will start from the VLAN table look up. If the VID is not valid, then packet will be dropped and no address learning will take place. If the VID is valid, then FID is retrieved. The FID+DA and FID+SA lookups are performed. The FID+DA look up determines the forwarding ports. If FID+DA fails, then the packet will be broadcast to all the members (excluding the ingress port) of the VLAN. If FID+SA fails, then the FID+SA will be learned.

VLAN Table Lookup Examples:

1. VLAN Table Read (read the third entry, at the indirect address offset 0x02)

Write to Reg. IACR with 0x1402 (set indirect address and trigger a read VLAN table operation)

Then:

Read Reg. IADR5 (VLAN table bits [19:16])

Read Reg. IADR4 (VLAN table bits [15:0])

2. VLAN Table Write (write the seventh entry, at the indirect address offset 0x06)

Write to Reg. IADR5 (VLAN table bits [19:16])

Write to Reg. IADR4 (VLAN table bits [15:0])

Write to Reg. IACR with 0x1406 (set indirect address and trigger a read VLAN table operation)

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Supply Voltage
(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... –0.5V to +4.0V

Input Voltage (all inputs) ..... –0.5V to +5.0V

Output Voltage (all outputs) ..... –0.5V to +4.0V

Lead Temperature (soldering, 10s) ..... +270°C

Storage Temperature (T_S) ..... –55°C to +150°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than those listed in the table above may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.

5.2 Operating Ratings**

Supply Voltage
(V_{DDATX}, V_{DDARX}, V_{DDIO}) ..... +3.1V to +3.5V

Ambient Operating Temperature for MQL/MBL (T_A) ..... 0°C to +70°C

Ambient Operating Temperature for MQL/MBL AM (T_A) ..... –40°C to +85°C

Maximum Junction Temperature (T_J) ..... +125°C

Package Thermal Resistance (Note 5-1) .....

PQFP (θ_{JA}) ..... +42.91°C/W

PQFP (θ_{JC}) ..... +19.6°C/W

LFBGA (θ_{JA}) ..... +38.50°C/W

LFBGA (θ_{JC}) ..... +12.50°C/W

**The device is not guaranteed to function outside its operating ratings. Unused inputs must always be tied to an appropriate logic voltage level (Ground to VDD).

Note 5-1 No heat spreader (HS) in this package. The θ_{JC} / θ_{JA} are under air velocity 0 m/s.

Note: Do not drive input signals without power supplied to the device.

6.0 ELECTRICAL CHARACTERISTICS

Specification is for packaged product only. Single port's transformer consumes an additional 45 mA @ 3.3V for 100BASE-TX and 70 mA @ 3.3V for 10BASE-T.

TABLE 6-1: ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current for 100BASE-TX Operation (All Ports @ 100% Utilization)						
100BASE-TX (Analog Core + Digital Core + Transceiver + Digital I/O)	I_{DDXIO}	—	122	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V
Supply Current for 10BASE-T Operation (All Ports @ 100% Utilization)						
10BASE-T (Analog Core + Digital Core + Transceiver + Digital I/O)	I_{DDXIO}	—	90	—	mA	V_{DDATX}, V_{DDARX}, V_{DDIO} = 3.3V
CMOS Inputs						
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input Current	I_{IN}	–10	—	10	µA	V_{IN} = GND ~ V_{DDIO}
CMOS Outputs						
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = –8 mA
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output Tri-State Leakage	I_{OZ}	—	—	10	µA	—
100BASE-TX Transmit (measured differentially after 1:1 transformer) V_{DDATX} = 3.3V only						
Peak Differential Output Voltage	V_O	0.95	—	1.05	V	100Ω termination on the differential output.
Output Voltage Imbalance	V_{IMB}	—	—	2	%	100Ω termination on the differential output.
Rise/Fall Time	t_r/t_f	3	—	5	ns	—
Rise/Fall Time Imbalance	—	0	—	0.5	ns	—
Duty Cycle Distortion	—	—	—	±0.5	ns	—
Overshoot	—	—	—	5	%	—
Reference Voltage of I_{SET}	V_{SET}	—	0.5	—	V	—
Output Jitter	—	—	0.7	1.4	ns	Peak-to-peak
10BASE-T Receive						
Squelch Threshold	V_{SQ}	—	400	—	mV	5 MHz square wave
10BASE-T Transmit (measured differentially after 1:1 transformer) V_{DDATX} = 3.3V only						
Peak Differential Output Voltage	V_P	—	2.4	—	V	100Ω termination on the differential output.
Jitter Added	—	—	1.8	±3.5	ns	100Ω termination on the differential output

7.0 TIMING SPECIFICATIONS

For PCI timing, please refer to PCI Specification version 2.2.

7.1 EEPROM Timing

FIGURE 7-1: EEPROM READ CYCLE TIMING DIAGRAM

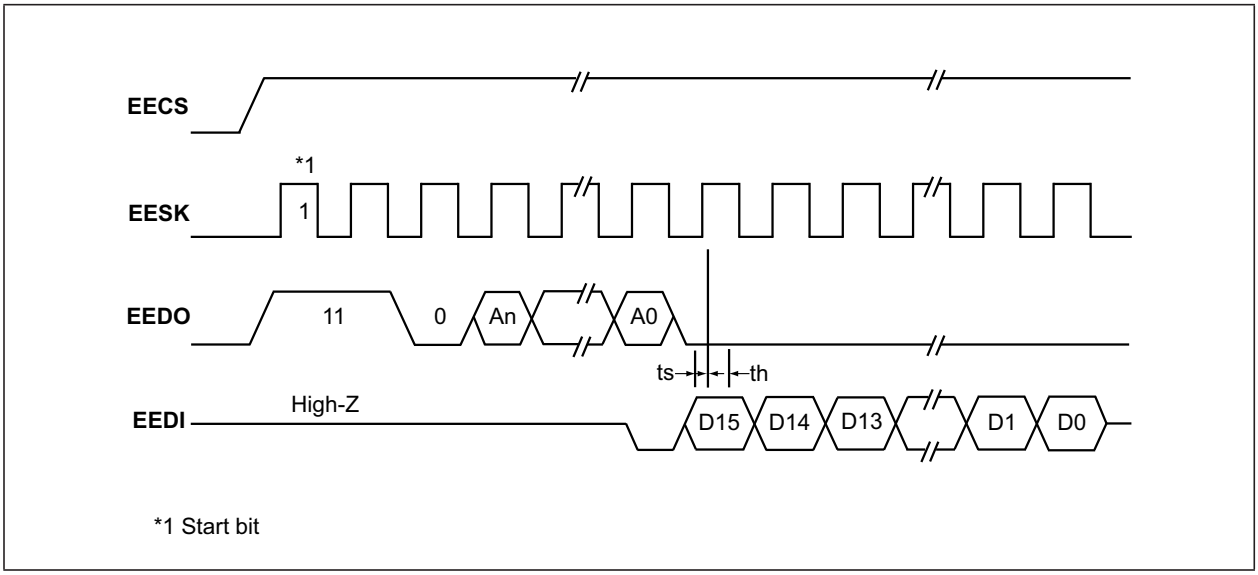


TABLE 7-1: EEPROM TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{cyc}	Clock cycle	—	4000	—	ns
t_s	Setup time	20	—	—	ns
t_h	Hold time	20	—	—	ns

7.2 Auto-Negotiation Timing

FIGURE 7-2: AUTO-NEGOTIATION TIMING

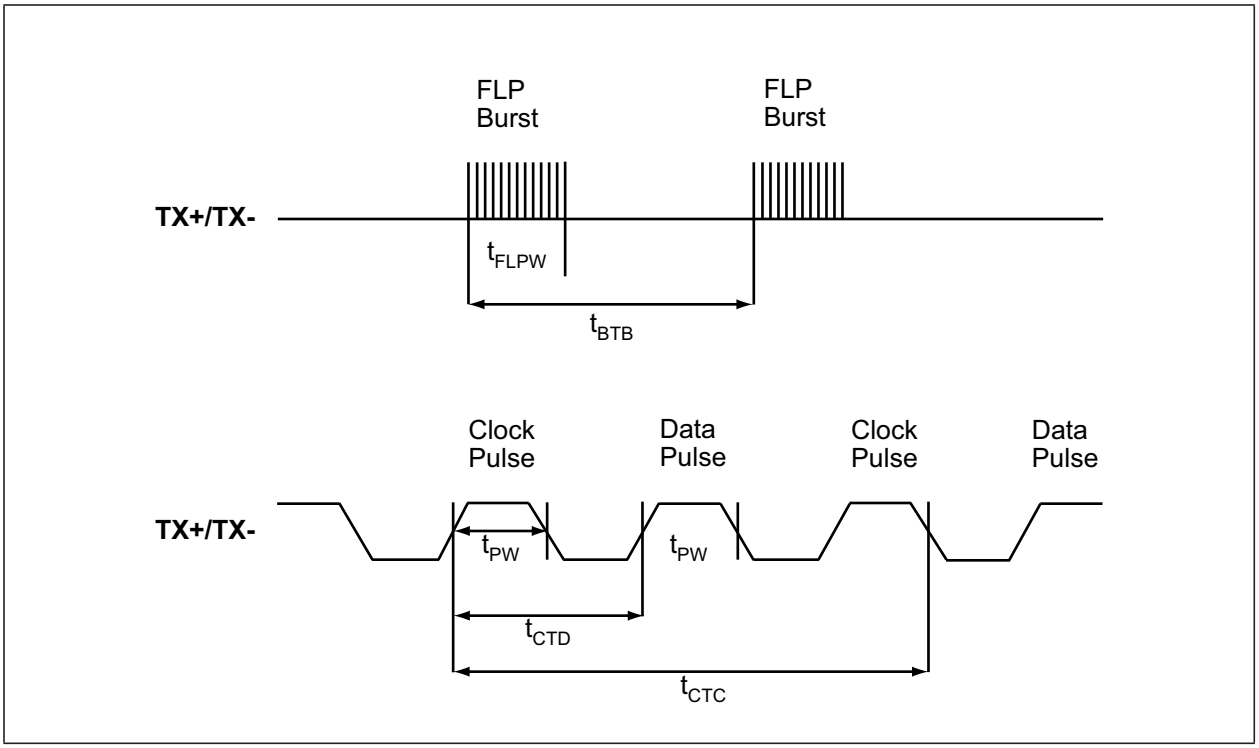


TABLE 7-2: AUTO-NEGOTIATION TIMING PARAMETERS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width	—	2	—	ms
t_{PW}	Clock/Data pulse width	—	100	—	ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
—	Number of Clock/Data pulses per burst	17	—	33	—

7.3 Reset Timing

As long as the stable supply voltages to reset High timing (minimum of 10 ms) are met, there is no power-sequencing requirement for the KSZ8842-PMQL/PMBL supply voltages (3.3V).

The reset timing requirement is summarized in Figure 7-3 and Table 7-3.

FIGURE 7-3: RESET TIMING

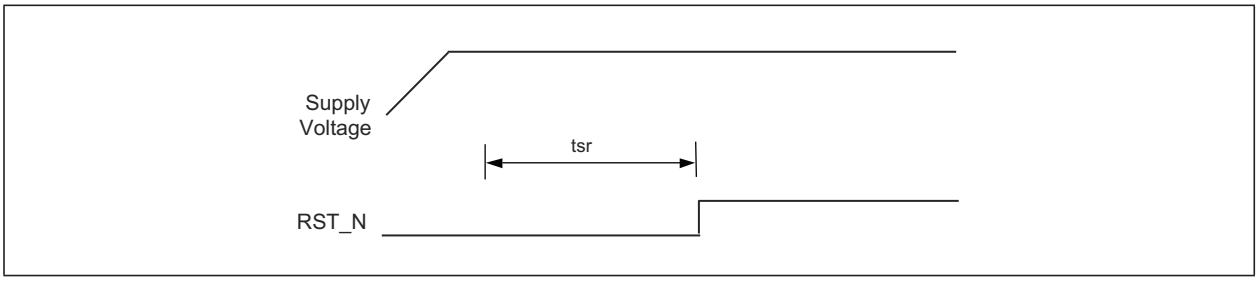


TABLE 7-3: RESET TIMING PARAMETERS

Parameter	Description	Min.	Typ.	Max.	Units
t_{SR}	Stable supply voltages to reset high	10	—	—	ms

8.0 SELECTION OF ISOLATION TRANSFORMERS

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements.

Table 8-1 lists recommended transformer characteristics.

TABLE 8-1: TRANSFORMER SELECTION CRITERIA

Parameter	Value	Test Conditions
Turns Ratio	1 CT : 1 CT	—
Open-Circuit Inductance (min.)	350 µH	100 mV, 100 kHz, 8 mA
Leakage Inductance (max.)	0.4 µH	1 MHz (min.)
Interwinding Capacitance (max.)	12 pF	—
D.C. Resistance (max.)	0.9Ω	—
Insertion Loss (max.)	1.0 dB	0 MHz to 65 MHz
HIPOT (min.)	1500 V_{RMS}	—

TABLE 8-2: QUALIFIED SINGLE-PORT MAGNETICS

Manufacturer	Part Number	Auto MDI-X
Pulse	H1102	Yes
Pulse (Low Cost)	H1260	Yes
Transpower	HB726	Yes
Bel Fuse	S558-5999-U7	Yes
Delta	LF8505	Yes
LanKom	LF-H41S	Yes
TDK (Mag Jack)	TLA-6T718	Yes

TABLE 8-3: TYPICAL REFERENCE CRYSTAL CHARACTERISTICS

Characteristic	Value
Frequency	25 MHz
Frequency Tolerance (max.)	±50 ppm
Load Capacitance (max.)	20 pF
Series Resistance	25Ω

9.0 PACKAGE OUTLINE

9.1 Package Marking Information

128-Lead PQFP*

```
MICREL
XXXXXXX
XXXX
YYWWA7
XXXXXYYWWNNN
●YYWWNNN
```

Example

```
MICREL
KSZ8842
PMQL
1925A7
G00001925267
●1925267
```

100-Ball LFBGA*

```
MICREL
XXXXXXX
XXXX
YYWWA7
XXXXXYYWWNNN
●YYWWNNN
```

Example

```
MICREL
KSZ8842
PMBL
1945A7
G00001945167
●1945167
```

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

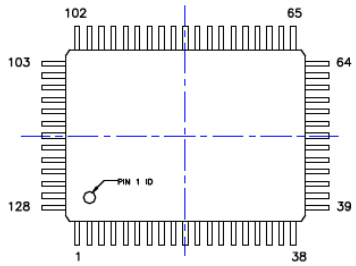
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

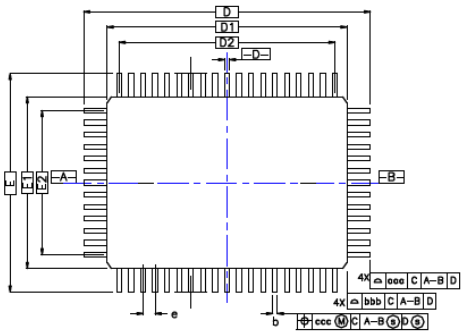
FIGURE 9-1: 128-LEAD PQFP 14 MM X 20 MM PACKAGE OUTLINE AND RECOMMENDED LAND PATTERN

TITLE
128 LEAD PQFP 14x20mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

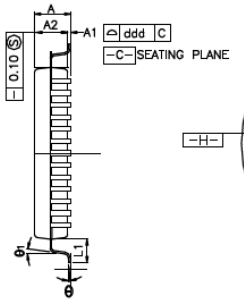
DRAWING #	PQFP14x20-128LD-PL-1	UNIT	MM [INCHES]



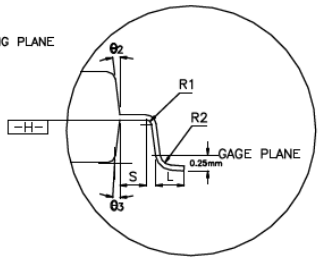
TOP VIEW
Note 1,2,3



BOTTOM VIEW
Note 1,2,3



SIDE VIEW
Note 1,2,3



DETAILED VIEW

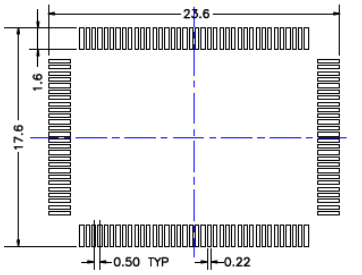
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2 , θ3	15° REF			15° REF		

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

CONTROL DIMENSIONS ARE IN MILLIMETERS.

NOTES :

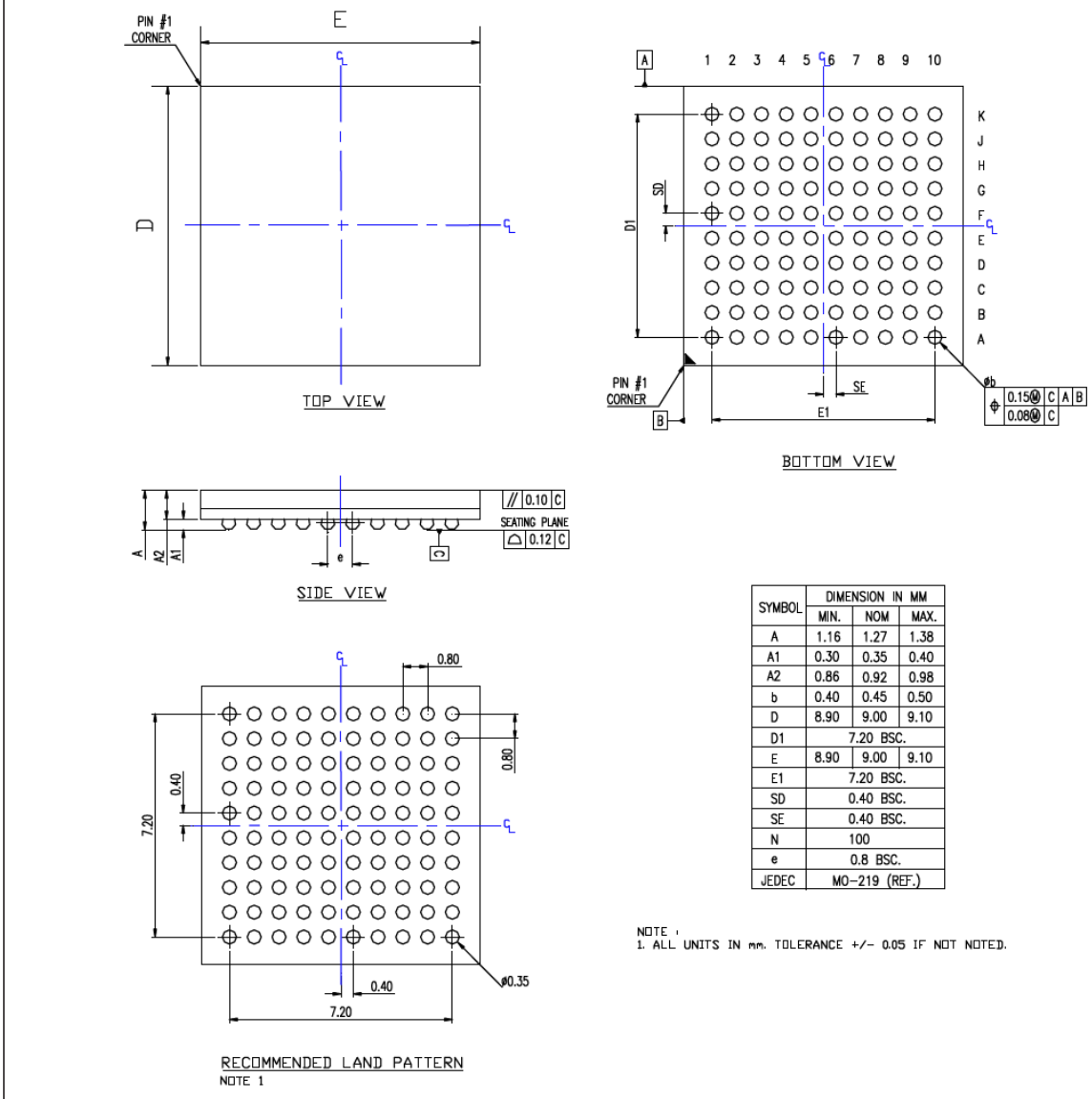
1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
3. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.
4. ALL UNITS IN mm. TOLERANCE +/− 0.05 IF NOT NOTED.



RECOMMENDED LAND PATTERN
Note 4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 9-2: 100-BALL LFBGA 9 MM X 9 MM PACKAGE OUTLINE AND RECOMMENDED LAND PATTERN



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003524A (07-2-2020)	—	Converted Micrel data sheet KSZ8842-PMQL/PMBL to Microchip DS00003524A. Minor text changes throughout.

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

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CUSTOMER SUPPORT

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XXX	X	XX	X	[X]	[-XX]
Device	Bus Design	Interface	Package	Supply Voltage	Temperature	Media Type

Device:	KSZ8842: Two-Port Ethernet Switch with PCI Interface
Bus Design:	P = PCI
Interface:	M = Management Interface
Package:	Q = 128-Lead PQFP B = 100-Ball LFBGA
Supply Voltage:	L = Single 3.3V Power Supply Supported with Internal 1.8V LDO
Temperature:	<blank> = 0°C to +70°C (Commercial) I = –40°C to +85°C (Industrial) AM = –40°C to +85°C (Automotive Grade)
Media Type:	<blank> = 66/Tray (PQFP option) <blank> = 260/Tray (LFBGA option) T/R = 1,000/Tape & Reel (LFBGA option)

Examples:

c) KSZ8842-PMQL
PCI Management Interface
128-Lead PQFP, Single 3.3V Power Supply
Commercial Temperature Range
66/Tray

d) KSZ8842-PMQLI
PCI Management Interface
128-Lead PQFP, Single 3.3V Power Supply
Industrial Temperature Range
66/Tray

e) KSZ8842-PMBL
PCI Management Interface
100-Lead LFBGA, Single 3.3V Power Supply
Commercial Temperature Range
260/Tray

f) KSZ8842-PMBL-AM
PCI Management Interface
100-Lead LFBGA, Single 3.3V Power Supply
Automotive Temperature Range
260/Tray

g) KSZ8842-PMBL-AM-TR
PCI Management Interface
100-Lead LFBGA, Single 3.3V Power Supply
Automotive Temperature Range
1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note the following details of the code protection feature on Microchip devices:

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