



# **KSZ8081MNX / KSZ8091MNX**

## **10Base-T/100Base-TX Physical Layer Transceiver**

### **Evaluation Board User's Guide**

**Revision 1.0 / August 2012**

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## Revision History

| Revision | Date    | Summary of Changes |
|----------|---------|--------------------|
| 1.0      | 8/15/12 | Initial Release    |

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## **1.0 Introduction**

The KSZ8081MNX / KSZ8091MNX is a 10Base-T/100Base-TX Physical Layer Transceiver with an MII MAC interface. It utilizes a unique mixed-signal design to extend signaling distance while reducing power consumption, and offers HP Auto MDI/MDI-X for reliable detection of and correction for crossover and straight-through cables, eliminating the need to differentiate between crossover and straight-through cables.

The KSZ8091MNX has all the identical rich features of the KSZ8081MNX plus support for Energy Efficient Ethernet (EEE) and Wake-on-LAN (WOL). The KSZ8081MNX / KSZ8091MNX come in a 32-pin, lead-free QFN package and provides an ideal solution for 10Base-T/100Base-TX applications that have tight PCB board space.

The KSZ8081MNX and KSZ8091MNX Eval Boards (KSZ8081MNX-EVAL and KSZ8091MNX-EVAL) provide a convenient platform to evaluate the features of the device. All configuration pins are accessible either by jumpers, test points or interface connectors.

## **2.0 Board Features**

- Micrel KSZ8081MNX or KSZ8091MNX 10Base-T/100Base-TX Physical Layer Transceiver
- RJ-45 Jack for Fast Ethernet cable interface
- HP Auto MDI/MDI-X for automatic detection and correction for straight-through and crossover cables
- MII (Media Independent Interface) Connector to interface with a MAC controller
- 2 LED Indicators for status and activity
- Jumpers to configure strapping pins
- Manual Reset Button for quick reboot after re-configuration of strapping pins

## **3.0 Evaluation Kit Contents**

The KSZ8081MNX and KSZ8091MNX Evaluation Kits include the following hardware:

- KSZ8081MNX or KSZ8091MNX Evaluation Board

A design package with the following collaterals that can be downloaded from Micrel's website at <http://www.micrel.com>

- KSZ8081MNX / KSZ8091MNX Eval Board Schematic (PDF and OrCAD DSN file)
- KSZ80x1 (32-QFN) Eval Board Gerber Files (PDF version included)
- KSZ8081MNX / KSZ8091MNX Eval Board User's Guide (this document)
- KSZ8081MNX and KSZ8091MNX IBIS Models

and the KSZ8081MNX / KSZ8081RNB and KSZ8091MNX / KSZ8091RNB Datasheets which are also available from Micrel's website.

## 4.0 Hardware Description

The KSZ8081MNX-EVAL / KSZ8091MNX-EVAL (shown in Figure 1) comes in a compact form factor and plugs directly into boards with Ethernet MACs that expose the MII interface. Configuration of the KSZ8081MNX / KSZ8091MNX is accomplished through on-board jumper selections and/or by PHY register access via the MDC/MDIO management pins of the MII Interface.

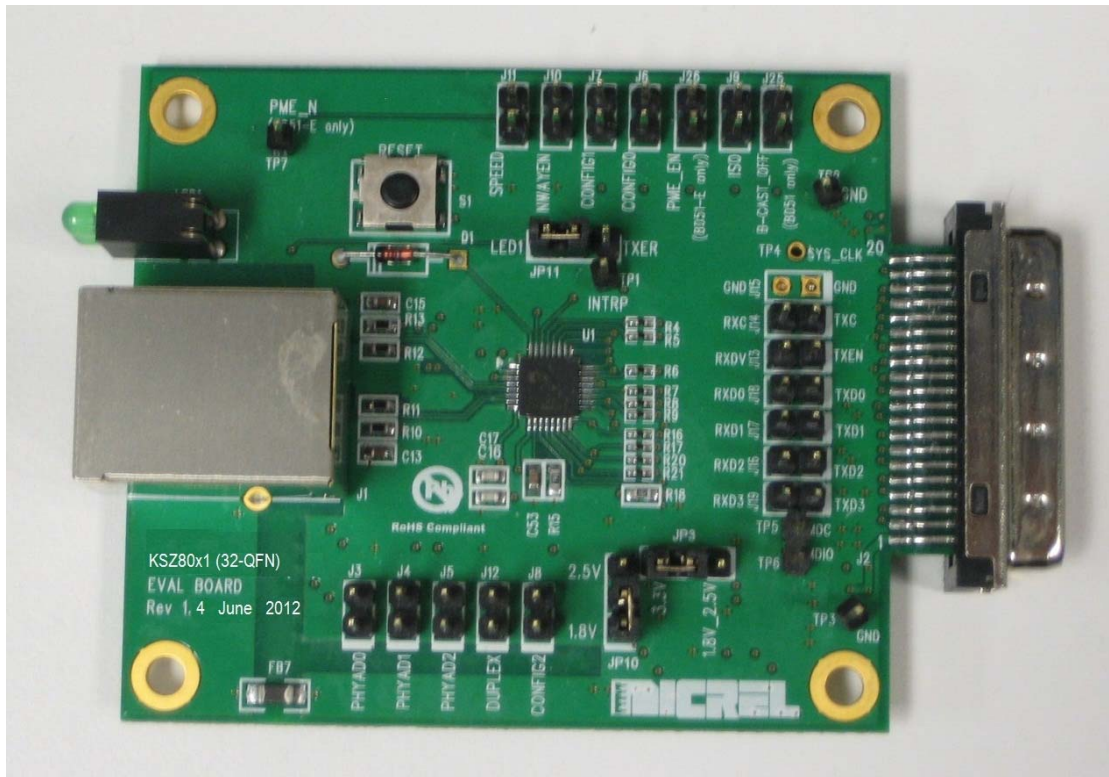


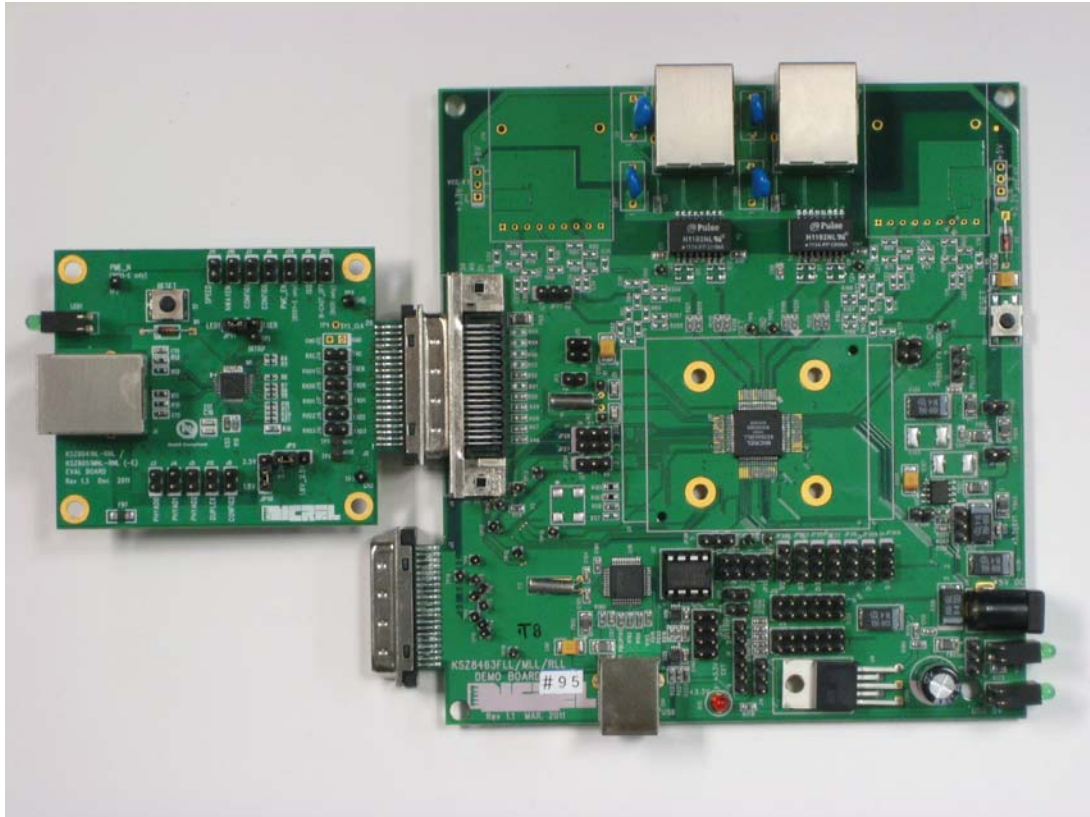
Figure 1. KSZ8081MNX Evaluation Board

Features include an RJ-45 Jack for Fast Ethernet cable connection, programmable LED indicators for reporting link status and activity, and a manual reset button for quick reboot after re-configuration of strapping pins.

The KSZ8081MNX-EVAL / KSZ8091MNX-EVAL receives +5V DC input power through its MII connector.

## 4.1 MII (Media Independent Interface)

The KSZ8081MNX-EVAL / KSZ8091MNX-EVAL receives power and accesses MII data and management information from the MII connector J2. Figure 2 shows the KSZ8081MNX-EVAL / KSZ8091MNX-EVAL connected to the Micrel KSZ8463MLI Evaluation Board.



**Figure 2. KSZ8081MNX-EVAL interfacing with KSZ8463MLI Evaluation Board**

The MII interface is defined by Clause 22 of the IEEE 802.3 Specification. MII Management (MIIM) is conducted thru pins MDC (clock line) and MDIO (data line). MIIM allows upper-layer devices to monitor and control the states of the KSZ8081MNX / KSZ8091MNX. An external device with MDC/MDIO capability can be used to read the PHY status or configure the PHY registers. The MIIM frame format and timing information can be found in the KSZ8081MNX and KSZ8091MNX datasheets and in Clause 22 of the IEEE 802.3 Specification.

The Eval Board has a 40-pin male edge connector that interfaces with and plugs directly into Fast Ethernet MAC boards with the mating AMP 787170-4 (40-pin, right angle, female) connector. Table 1 lists the pin outs for the MII interface on connector J2.

| Pin # | Signal | Pin # | Signal |
|-------|--------|-------|--------|
| 1     | +5V    | 21    | +5V    |
| 2     | MDIO   | 22    | Ground |
| 3     | MDC    | 23    | Ground |
| 4     | RXD3   | 24    | Ground |
| 5     | RXD2   | 25    | Ground |
| 6     | RXD1   | 26    | Ground |
| 7     | RXD0   | 27    | Ground |
| 8     | RXDV   | 28    | Ground |
| 9     | RXCLK  | 29    | Ground |
| 10    | RXER   | 30    | Ground |
| 11    | TXER   | 31    | Ground |
| 12    | TXCLK  | 32    | Ground |
| 13    | TXEN   | 33    | Ground |
| 14    | TXD0   | 34    | Ground |
| 15    | TXD1   | 35    | Ground |
| 16    | TXD2   | 36    | Ground |
| 17    | TXD3   | 37    | Ground |
| 18    | COL    | 38    | Ground |
| 19    | CRS    | 39    | Ground |
| 20    | +5V    | 40    | +5V    |

**Table 1. Connector J2 - MII Pin Definition**



## 4.2 Jumper Setting & Definition

At power-up, the KSZ8081MNX / KSZ8091MNX is configured using the chip's internal pull-up and pull-down resistors with its default strapping pin values. Jumpers are provided to override the default settings, allowing for quick configuration and re-configuration of the board. To override the default settings, simply select and close the desired jumper setting(s) and toggle the on-board manual reset button (S1) for the new setting(s) to take effect. The KSZ8081MNX-EVAL / KSZ8091MNX-EVAL strapping jumper settings are defined in Table 2 below.

| Jumper               | Definition                        | Open (default)   | Close              |             |      |                    |               |                      |                  |
|----------------------|-----------------------------------|--|--------------------|-------------|------|--------------------|---------------|----------------------|------------------|
| J3                   | PHYAD0                            | 1  | 0                  |             |      |                    |               |                      |                  |
| J4                   | PHYAD1                            | 0  | 1                  |             |      |                    |               |                      |                  |
| J5                   | PHYAD2                            | 0  | 1                  |             |      |                    |               |                      |                  |
| J6                   | CONFIG0                           | <table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>[open, open, open]</td><td>MII (default)</td></tr><tr><td>[close, close, open]</td><td>MII Back-to-Back</td></tr></table> <p>All other CONFIG[2:0] settings not listed are reserved (not used).</p> |                    | CONFIG[2:0] | Mode | [open, open, open] | MII (default) | [close, close, open] | MII Back-to-Back |
| CONFIG[2:0]          | Mode                              |  |                    |             |      |                    |               |                      |                  |
| [open, open, open]   | MII (default)                     |  |                    |             |      |                    |               |                      |                  |
| [close, close, open] | MII Back-to-Back                  |  |                    |             |      |                    |               |                      |                  |
| J7                   | CONFIG1                           |  |                    |             |      |                    |               |                      |                  |
| J8                   | CONFIG2                           |  |                    |             |      |                    |               |                      |                  |
| J9                   | Isolate Mode                      | Disable  | Enable             |             |      |                    |               |                      |                  |
| J10                  | Nway Auto-Negotiation             | Enable   | Disable            |             |      |                    |               |                      |                  |
| J11                  | Forced Speed (KSZ8081 only)       | 100Base-TX   | 10Base-T           |             |      |                    |               |                      |                  |
| J12                  | Forced Duplex                     | Half   | Full               |             |      |                    |               |                      |                  |
| J25                  | Broadcast Off – for PHY Address 0 | Broadcast PHY address  | Unique PHY address |             |      |                    |               |                      |                  |
| J26                  | PME_N Pin Enable (KSZ8091 only)   | Disable  | Enable             |             |      |                    |               |                      |                  |

**Table 2. KSZ8081MNX-EVAL / KSZ8091MNX-EVAL Strapping Jumper Definition**

The KSZ8081MNX-EVAL / KSZ8091MNX-EVAL has another set of jumpers that may be used to loopback the MII interface. To loopback, all six jumpers must be installed. The individual jumpers are defined in Table 3.

| Jumper | MII Signals | Normal Operation | MII Loopback Mode |
|--------|-------------|------------------|-------------------|
| J13    | RXDV / TXEN | Open             | Close             |
| J14    | RXC / TXC   | Open             | Close             |
| J16    | RXD2 / TXD2 | Open             | Close             |
| J17    | RXD1 / TXD1 | Open             | Close             |
| J18    | RXD0 / TXD0 | Open             | Close             |
| J19    | RXD3 / TXD3 | Open             | Close             |

**Table 3. KSZ8081MNX-EVAL / KSZ8091MNX-EVAL Loopback Jumper Definition**

The last group of jumpers is defined in Table 4 below. These jumpers are not related to reset strapping, nor to loopback. Two jumpers are used to set the VDDIO voltage, and one jumper is used to route pin 31 as dependent on the device part number.

Note that for the eval board to function, a jumper must be installed on JP3. If pins 1 & 2 of JP3 are closed, then a jumper must also be installed on JP10.

For the KSZ8091MNX, a jumper must be installed on pins 2 & 3 of JP11.

| Jumper | Definition                          | Close pins 1, 2                     | Close pins 2, 3                     |
|--------|-------------------------------------|-------------------------------------|-------------------------------------|
| JP3    | VDDIO voltage selection: 3.3V / low | VDDIO set by JP10                   | VDDIO = 3.3V                        |
| JP10   | VDDIO low voltage selection         | 1.8V_2.5V = 1.8V                    | 1.8V_2.5V = 2.5V                    |
| JP11   | Pin 31 connection (LED1 or TXER)    | For KSZ8081 only<br>(pin 31 = LED1) | For KSZ8091 only<br>(pin 31 = TXER) |

**Table 4. KSZ8081MNX-EVAL / KSZ8091MNX-EVAL Miscellaneous Jumper Definition**

Table 5 lists the strapping pin definitions for the KSZ8081MNX-EVAL / KSZ8091MNX-EVAL jumpers.

| Jumper         | Pin              | Pin Name                      | Pin Function  |             |      |     |               |     |                  |
|----------------|------------------|-------------------------------|---|-------------|------|-----|---------------|-----|------------------|
| J5<br>J4<br>J3 | 15<br>14<br>13   | PHYAD2<br>PHYAD1<br>PHYAD0    | <p>The PHY Address is latched at power-up / reset and is configurable to any value from 0 to 7.</p> <p>The default PHY Address is 00001.</p> <p>PHY Address 00000 is enabled only if the B-CAST_OFF strapping pin is pulled high.</p> <p>PHY Address bits [4:3] are always set to '00'.</p>                                   |             |      |     |               |     |                  |
| J8<br>J7<br>J6 | 18<br>29<br>28   | CONFIG2<br>CONFIG1<br>CONFIG0 | <p>The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:</p> <table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>110</td><td>MII Back-to-Back</td></tr></table> <p>All other CONFIG[2:0] settings not listed are reserved (not used).</p> | CONFIG[2:0] | Mode | 000 | MII (default) | 110 | MII Back-to-Back |
| CONFIG[2:0]    | Mode             |                               |   |             |      |     |               |     |                  |
| 000            | MII (default)    |                               |   |             |      |     |               |     |                  |
| 110            | MII Back-to-Back |                               |   |             |      |     |               |     |                  |
| J9             | 20               | ISO                           | <p>ISOLATE mode</p> <p>Pull-up = Enable</p> <p>Pull-down (default) = Disable</p> <p>At the de-assertion of reset, this pin value is latched into register 0h bit 10.</p>  |             |      |     |               |     |                  |

| Jumper | Pin | Pin Name                 | Pin Function   |
|--------|-----|--------------------------|--|
| J11    | 31  | SPEED<br>(KSZ8081 only)  | SPEED mode<br>Pull-up (default) = 100Mbps<br>Pull-down = 10Mbps<br>At the de-assertion of reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support. |
| J12    | 16  | DUPLEX                   | DUPLEX mode<br>Pull-up (default) = Half Duplex<br>Pull-down = Full Duplex<br>At the de-assertion of reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.  |
| J10    | 30  | NWAYEN                   | Nway Auto-Negotiation Enable<br>Pull-up (default) = Enable Auto-Negotiation<br>Pull-down = Disable Auto-Negotiation<br>At the de-assertion of reset, this pin value is latched into register 0h bit 12.  |
| J25    | 19  | B-CAST_OFF               | Broadcast Off – for PHY Address 0<br>Pull-up = PHY Address 0 is set as a unique PHY address<br>Pull-down (default) = PHY Address 0 is set as a broadcast PHY address<br>At the de-assertion of reset, this pin value is latched by the chip.                                   |
| J26    | 22  | PME_EN<br>(KSZ8091 only) | PME_N Output Pin for Wake-On-LAN Function<br>Pull-up = Enable<br>Pull-down = Disable<br>At the de-assertion of reset, this pin value is latched into the chip.   |
| N/A    | 21  | NAND_Tree#               | NAND Tree Mode<br>Pull-up (default) = Disable<br>Pull-down = Enable<br>At the de-assertion of reset, this pin value is latched by the chip.  |

**Table 5. Strapping Pin Definitions for KSZ8081MNX-EVAL / KSZ8091MNX-EVAL Jumpers**

### 4.3 Test Point Definition

The KSZ8081MNX-EVAL / KSZ8091MNX-EVAL has four test points. They are defined in the following table.

| Test Point | Definition   |
|------------|--|
| TP1        | Pin 21 (with external pull-up)<br>KSZ8081: Interrupt<br>KSZ8091: Interrupt or PME_N2 |
| TP2        | Ground   |
| TP3        | Ground   |
| TP7        | Pin 30<br>KSZ8081: LED0<br>KSZ8091: LED0 or PME_N1                                   |

**Table 6. KSZ8081MNX-EVAL / KSZ8091MNX-EVAL Test Point Definition**

### 4.4 RJ-45 Connector

The RJ-45 Connector (J1) is a TDK TLA-6T718A or similar integrated magnetic jack. It connects to standard CAT-5 Ethernet cable to interface with 10Base-T / 100Base-TX Ethernet devices.

### 4.5 LED Indicators

A dual LED indicator (LED1) is located adjacent to the RJ-45 Connector. The top LED and bottom LED are connected to LED1 (pin 31) and LED0 (pin 30) respectively.

The two LEDs are programmable to LED mode '00' or '01' via register 1Fh bits [5:4], and are defined in the following table.

| LED Mode | LED1 (pin 31)       |           |                | LED0 (pin 30)       |           |                |
|----------|---------------------|-----------|----------------|---------------------|-----------|----------------|
| 00       |                     |           |                |                     |           |                |
|          | Speed               | Pin State | LED Definition | Link/ Activity      | Pin State | LED Definition |
|          | 10Base-T            | H         | OFF            | No Link             | H         | OFF            |
|          | 100Base-Tx          | L         | ON             | Link                | L         | ON             |
|          |                     |           |                | Activity            | Toggle    | Blinking       |
| 01       |                     |           |                |                     |           |                |
|          | Activity            | Pin State | LED Definition | Link                | Pin State | Definition     |
|          | No Activity         | H         | OFF            | No Link             | H         | OFF            |
|          | Activity            | Toggle    | Blinking       | Link                | L         | ON             |
| 10       | Reserved – not used |           |                | Reserved – not used |           |                |
| 11       | Reserved – not used |           |                | Reserved – not used |           |                |

**Table 7. KSZ8081MNX / KSZ8091MNX LED Definition**

## 5.0 Bill of Materials

KSZ8081MNX / KSZ8091MNX Eval Board, Schematic Revision 1.0

| Item | Quantity | Reference   | Description                 | Package                |
|------|----------|---|-----------------------------|------------------------|
| 1    | 2        | C1,C2   | 47uF / Tantalum             | B-size                 |
| 2    | 1        | C3  | 22uF / Tantalum             | B-size                 |
| 3    | 10       | C4,C5,C7,C10,C11,C12,<br>C49,C51,C57,C58                                | 0.1uF                       | 0603                   |
| 4    | 4        | C6,C8,C48,C50   | 10uF / Tantalum             | A-size                 |
| 5    | 1        | C9  | 2.2uF                       | A-size                 |
| 6    | 2        | C16,C17   | 22pF                        | 0603                   |
| 7    | 1        | C52   | 470pF                       | 0603                   |
| 8    | 1        | D1  | 1N4148                      | DO-35 / axial lead     |
| 9    | 2        | FB1,FB7   | Ferrite Bead                | 1206                   |
| 10   | 1        | J1  | RJ-45 Mag Jack              | thru hole / PC mount   |
| 11   | 1        | J2  | Male MII Connector          | PCB edge mount         |
| 12   | 18       | J3,J4,J5,J6,J7,J8,J9,J10,<br>J11,J12,J13,J14,J16<br>J17,J18,J19,J25,J26 | Header 2X1                  | thru hole / 0.1" pitch |
| 13   | 3        | JP3,JP10,JP11   | Header 3X1                  | thru hole / 0.1" pitch |
| 14   | 1        | LED1  | LEDx2 / Green               | thru hole / 0.1" pitch |
| 15   | 1        | R1  | 100K                        | 0603                   |
| 16   | 1        | R2  | 10K                         | 0603                   |
| 17   | 9        | R3,R25,R26,R27,R28,<br>R29,R30,R102,R103                                | 4.7K                        | 0603                   |
| 18   | 10       | R4,R5,R6,R7,R8,R9,R16,<br>R17,R20,R21                                   | 33                          | 0603                   |
| 19   | 1        | R112  | 680                         | 0603                   |
| 20   | 1        | R15   | 6.49K                       | 0603                   |
| 21   | 2        | R22,R24   | 220                         | 0603                   |
| 22   | 5        | R18,R23,R31,R32,R33   | 1K                          | 0603                   |
| 23   | 2        | R111,R113   | 1.5K                        | 0603                   |
| 24   | 1        | S1  | SW PUSHBUTTON               | SMT                    |
| 25   | 4        | TP1,TP2,TP3,TP7   | TestPoint                   | thru hole / 0.1" pitch |
| 26   | 1        | U1  | KSZ8081MNX or<br>KSZ8091MNX | 32-pin QFN             |
| 27   | 1        | U2  | MIC5216-3.3YM5              | SOT-23-5               |
| 28   | 1        | U7  | MIC5207YM5                  | SOT-23-5               |
| 29   | 1        | Y1  | Xtal 25MHz +/-50ppm         | cylinder               |

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