IS1870/71

Bluetooth® Low Energy SoC

Features

- Bluetooth smart 5.0 Bluetooth Low Energy compliant
- 256 Kbytes embedded Flash memory
- UART/SPI/I^2C interface supported
- Integrated crystal oscillator operates with 32 MHz external crystal
- Temperature sensor supported
- 31 general purpose I/O (GPIO) pins for IS1870 SoC and 15 GPIO pins for IS1871 SoC
- Supports 4-channel pulse-width modulation (PWM) for IS1870 SoC and 1-channel PWM for IS1871 SoC
- Supports 12-bit ADC (ENOB=10 or 8 bits) for battery and voltage detection
- 16-channel ADC for IS1870 SoC and 6-channel ADC for IS1871 SoC are provided
- AES-CMAC hardware engine
- Beacon support
- Low power consumption
- Compact size:
  - IS1871: 4 mm x 4 mm 32QFN package
  - IS1870: 6 mm x 6 mm 48QFN package

Radio Frequency (RF)/Analog Features

- ISM band: 2.402 GHz to 2.480 GHz operation
- Channels: 0 to 39
- Rx sensitivity: -90 dBm in Bluetooth Low Energy mode
- Tx power: 0 dBm (typical)
- Received Signal Strength Indicator (RSSI) monitor

Operating Conditions

- Operating voltage: 1.9V to 3.6V
- Operating temperature: -40°C to +85°C

Applications

- Internet of Things (IoT)
- Wearable, fitness or healthcare
- Weighing scale
- Proximity/Find Me services
- Secure payment
- Digital beacons
- Consumer appliances or home automation
- Industrial

Packages

Type	IS1870	IS1871
Pin count	48	32
I/O pins (up to)	31	15
Contact/lead pitch	0.4	0.4
Dimensions	6x6x0.9	4x4x0.9
Package	QFN48	QFN32

Note: All dimensions are in millimeters (mm) unless specified.

NOTES:

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NOTES:

1.0 DEVICE OVERVIEW

The IS1870/71 SoC contains a 2.4 GHz transceiver, a Power Management Unit (PMU), Microchip's Bluetooth Low Energy software stack and an RF power amplifier.

The default factory configuration is designed to work with a host MCU to provide the user with an embedded Bluetooth Low Energy design setup for the IoT application domain.

Note:	Flexibility of the IS1870/71 SoC enables the user to work in a host-less implementation. In this configuration, the user can embed a full application into the IS1870/71 SoC. Contact your local Microchip representative for further guidance on obtaining this setup.

The IS1870/71 SoC provides:

- Simple integration and programming
- Reduced development time
- Superior Bluetooth Low Energy solution with low-cost system
- Interoperability with Apple® iOS and Android™ OS
- Wide range of application support

With the default factory configuration, the IS1870/71 SoC supports Beacon technology, where the automation of Bluetooth Low Energy connection/control and cloud connectivity are common.

The IS1870/71 SoC is optimized to maintain a low power wireless connection. The low power consumption and flexible power management maximize the IS1870/71 SoC lifetime in battery operated devices. A wide operating temperature range enables its applications in indoor and outdoor environments (industrial temperature range is -40°C to +85°C).

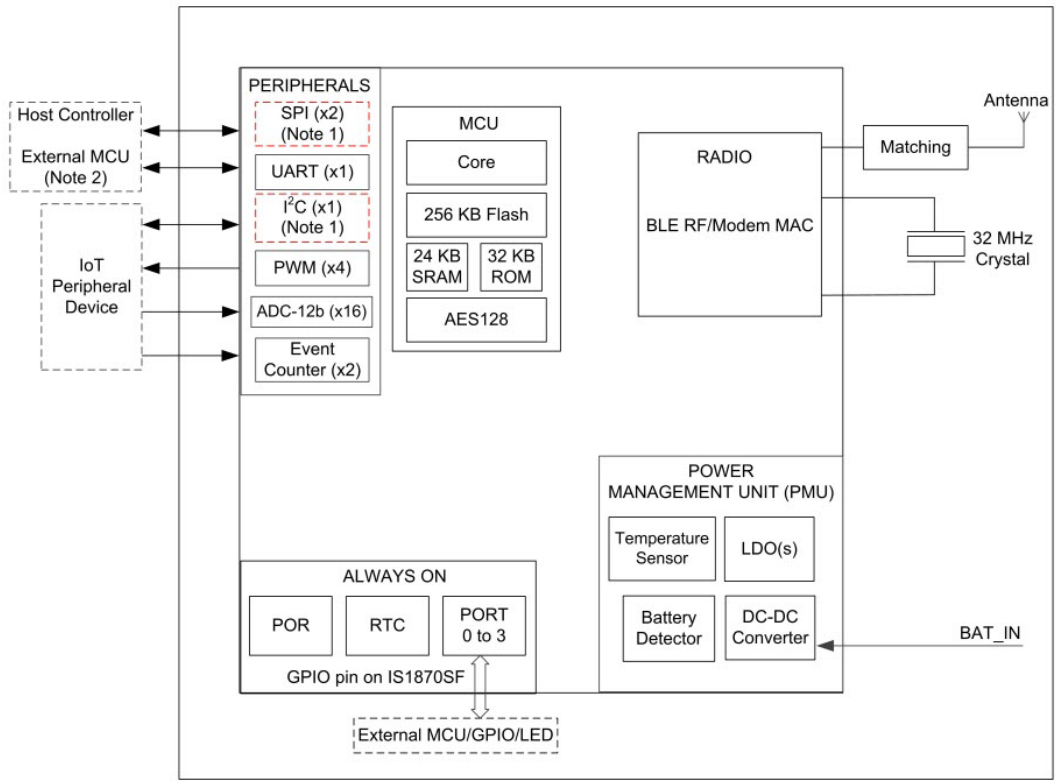
The small form factor package size of the IS1870/71 SoC is designed for wearable applications. The solution providers can minimize the module size to meet the market requirements, which is commonly seen in the IoT application domain.

To operate in the 2.4 GHz ISM band radio, the IS1870/71 SoC is certified for the Bluetooth v5.0 core specification, including support for the enhanced throughput and the Federal Information Processing Standard (FIPS) compliant encryption support for secure data connections.

The IS1870/71 SoC integrates transceiver and baseband functions to decrease external components. Microchip provides free Bluetooth stack firmware to build an embedded Bluetooth Low Energy solution, using the IS1870/71 SoC.

Figure 1-1 illustrates a typical block diagram of the IS1870 SoC.

FIGURE 1-1: BLOCK DIAGRAM OF THE IS1870 SOC

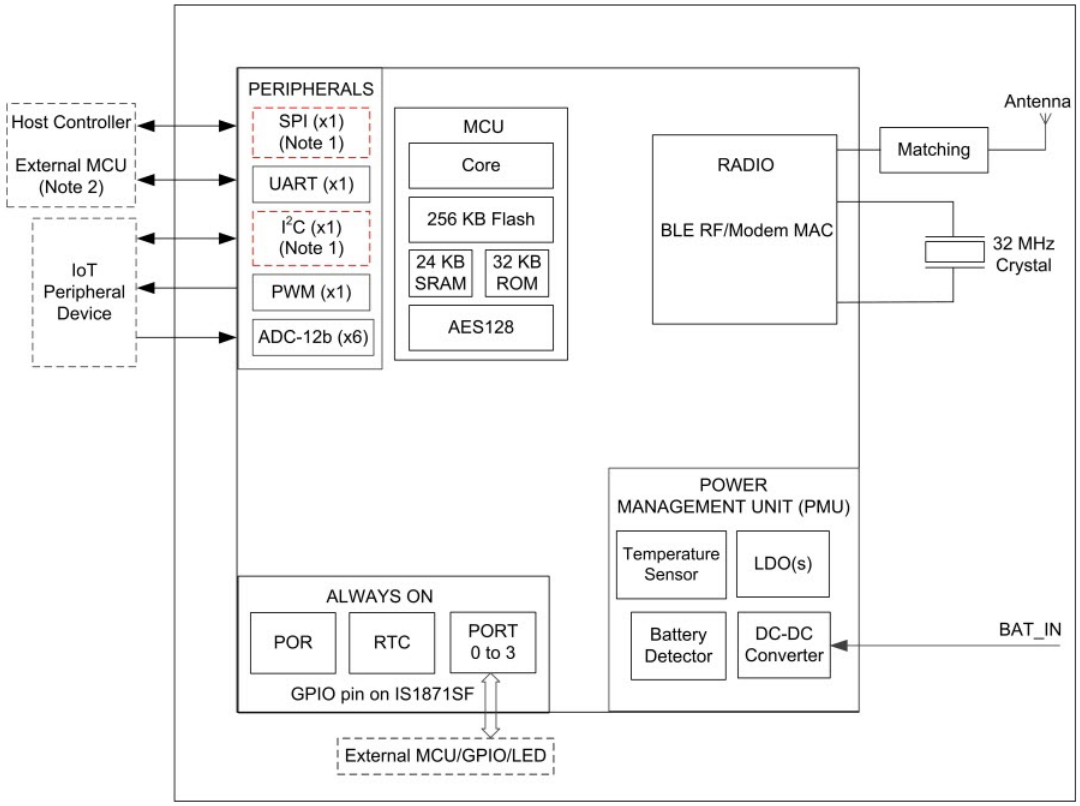


Note 1: Users can enable other peripheral (SPI and I^2C) functions of the IS1870/71 IC by changing the default factory firmware. For more details, contact local Microchip representatives.

2: An external host MCU is required when using the default factory firmware.

Figure 1-2 illustrates a typical block diagram of the IS1871 SoC-based system.

FIGURE 1-2: IS1871 SOC-BASED SYSTEM BLOCK DIAGRAM



Note 1: Users can enable other peripheral (SPI and I^2C) functions of the IS1870/71 IC by changing the default factory firmware. For more details, contact your local Microchip representatives.

2: An external host MCU is required when using the default factory firmware.

Table 1-1 provides the key features of the IS1870/71 SoC.

TABLE 1-1: KEY FEATURES

Features	IS1870	IS1871
UART	1	1
GPIO	31	15
12-bit ADC channels	16	6
PWM	4	1
SPI (see **Note 1**)	2	1
I^2C (see **Note 1**)	1	1
Pins	48	32
Size	6x6x0.9 mm	4x4x0.9 mm
Event counter	2	0
AES-CMAC H/W engine	Yes	Yes

Note 1: To make these peripherals available to a designer, contact your local Microchip representative.

Pin Description

Figure 1-3 and Figure 1-4 illustrate the IS1870 and IS1871 pin assignment details.

FIGURE 1-3: IS1870 SOC PIN ASSIGNMENT

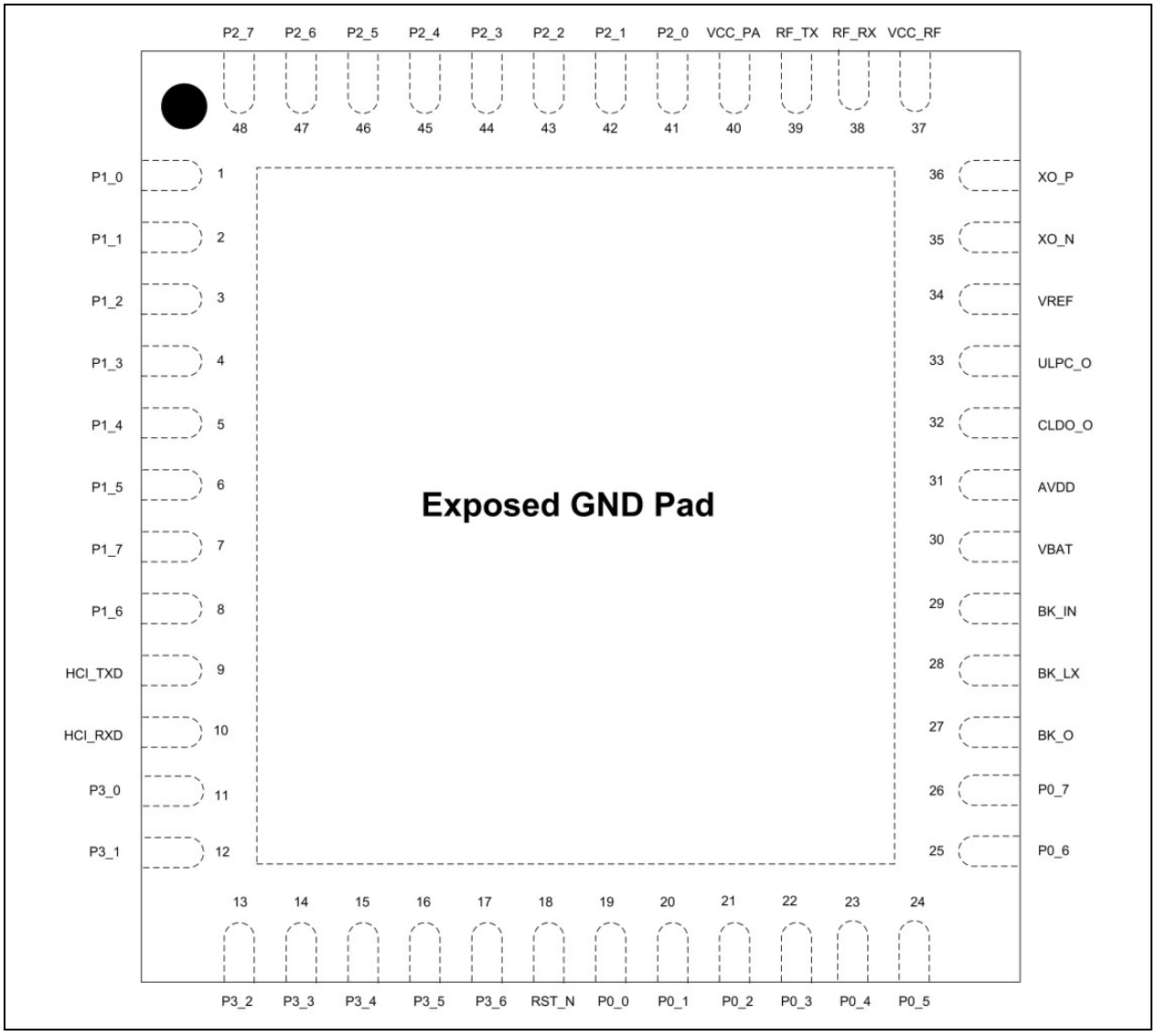


FIGURE 1-4: IS1871 SOC PIN ASSIGNMENT

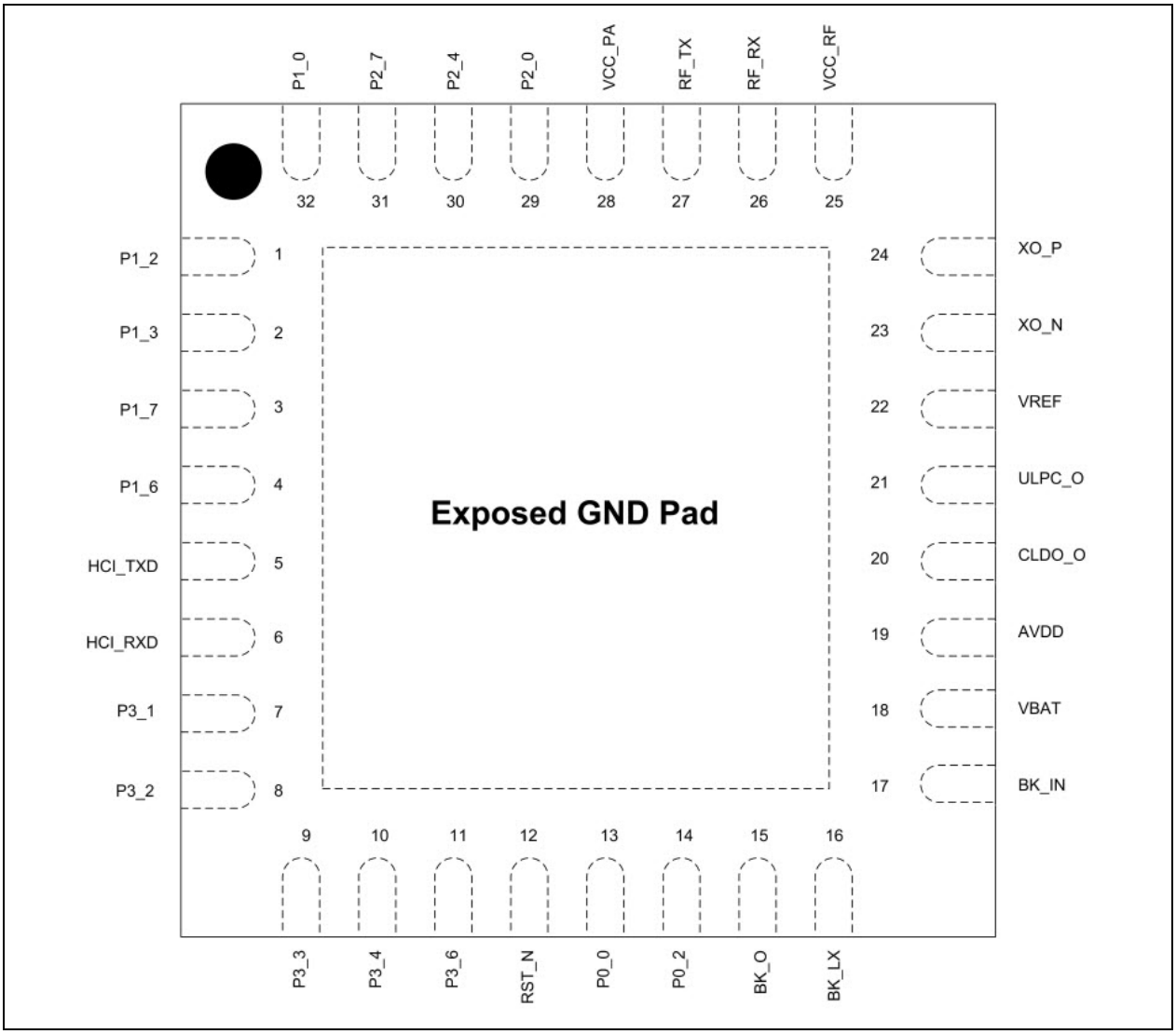


Table 1-2 provides the functions of the various pins in the IS1870/71 SoC.

TABLE 1-2: IS1870/71 SOC PIN DESCRIPTION

IS1870 Pin No.	IS1871 Pin No.	Pin Name	Type	Description
1	32	P1_0	DIO AI	GPIO: P1_0 ADC input: AD8 TX_CLS1: Class 1 RF Tx Control
2	—	P1_1	DIO AI DI	GPIO: P1_1 ADC input: AD9 SPI bus: MISO2: Second SPI bus (Central mode)
3	1	P1_2	DIO AI I/O	GPIO: P1_2 ADC input: AD10 I^2C SCL
4	2	P1_3	DIO AI DIO	GPIO: P1_3 ADC input: AD11 I^2C SDA
5	—	P1_4	DIO AI DI	GPIO: P1_4 ADC input: AD12 Event Counter
6	—	P1_5	DIO AI DI	GPIO: P1_5 ADC input: AD13 Event Counter
7	3	P1_7	DIO AO	GPIO: P1_7 External 32.768 kHz Crystal Output: XO32K
8	4	P1_6	DIO AI	GPIO: P1_6 External 32.768 kHz Crystal Input: XI32K
9	5	HCI_TXD	DO	HCI UART TXD
10	6	HCI_RXD	DI	HCI UART RXD
11	—	P3_0	DIO	GPIO: P3_0
12	7	P3_1	DIO DO	GPIO: P3_1 SPI bus: NCS, SPI Flash: CSN
13	8	P3_2	DIO DI	GPIO: P3_2 SPI bus: MISO, SPI Flash: SDO
14	9	P3_3	DIO DO	GPIO: P3_3 SPI bus: MOSI, SPI Flash: SDI
15	10	P3_4	DIO DO	GPIO: P3_4 SPI bus: SCLK, SPI Flash: SCK
16	—	P3_5	DIO AI	GPIO: P3_5 LED1
17	11	P3_6	DIO DO DO	GPIO: P3_6 UART flow-control RTS PWM0
18	12	RST_N	DI	External Reset
19	13	P0_0	DIO AI DI	GPIO: P0_0 ADC input: AD0 UART flow-control CTS
20	—	P0_1	DIO AI	GPIO: P0_1 ADC input: AD1

Legend: A = Analog D = Digital I = Input O = Output P = Power

TABLE 1-2: IS1870/71 SOC PIN DESCRIPTION (CONTINUED)

IS1870 Pin No.	IS1871 Pin No.	Pin Name	Type	Description
21	14	P0_2	DIO AI AI	GPIO: P0_2 ADC input: AD2 LED0
22	—	P0_3	DIO AI	GPIO:P0_3 ADC input: AD3
23	—	P0_4	DIO AI	GPIO:P0_4 ADC input: AD4
24	—	P0_5	DIO AI	GPIO:P0_5 ADC input: AD5
25	—	P0_6	DIO AI	GPIO:P0_6 ADC input: AD6
26	—	P0_7	DIO AI	GPIO:P0_7 ADC input: AD7
27	15	BK_O	P	1.55V buck regulator output. For internal use, do not connect to external devices)
28	16	BK_LX	P	1.55V buck regulator output. For internal use, do not connect to external devices
29	17	BK_IN	P	Buck input. Voltage Range: 1.9V to 3.6V
30	18	VBAT	P	Battery input. Voltage Range: 1.9V to 3.6V. Connect to BK_IN and a 10 µF decoupling capacitor, as illustrated in Figure A-1 and Figure A-3.
31	19	AVDD	P	Input of LDOs: CLDO, PALDO and RFLDO
32	20	CLDO_O	P	1.2V CLDO Output: Core-logic and memories supply, connect to 1 µF (X5R/X7R) capacitor
33	21	ULPC_O	P	1.2V Programmable ULPC Output: Always On logic and retention memory supply (for internal use, do not connect to external devices)
34	22	VREF	P	PMU band-gap reference voltage output for LDOs and buck (for internal use, do not connect to external devices)
35	23	XO_N	A	32 MHz crystal input negative
36	24	XO_P	A	32 MHz crystal input positive
37	25	VCC_RF	P	Power input for VCO and RF (1.28V). Connect to 1 µF (X5R/X7R) capacitor
38	26	Rx	AI	RF receive path
39	27	Tx	AO	RF transmit path
40	28	VCC_PA	P	Power supply for power amplifier (1.55V). Connect to 0.22 µF X5R/X7R
41	29	P2_0	DIO	Mode Configuration H: Application mode L: Test mode
42	—	P2_1	DIO DO	GPIO: P2_1 PWM0
43	—	P2_2	DIO DO	GPIO: P2_2 PWM1
44	—	P2_3	DIO DO	GPIO: P2_3 PWM2

Legend: A = Analog D = Digital I = Input O = Output P = Power

TABLE 1-2: IS1870/71 SOC PIN DESCRIPTION (CONTINUED)

IS1870 Pin No.	IS1871 Pin No.	Pin Name	Type	Description
45	30	P2_4	DIO	GPIO: P2_4 TX_CLS1: Class 1 RF RX Control
46	—	P2_5	DIO AI DO	GPIO: P2_5 ADC input: AD15 PWM3
47	—	P2_6	DIO	P26
48	31	P2_7	DIO AI DO	GPIO: P27 ADC input: AD14 SPI bus: NCS2, second SPI bus (Central mode)

Legend: A = Analog D = Digital I = Input O = Output P = Power

2.0 SYSTEM BLOCK DETAILS

2.1 System Block Descriptions

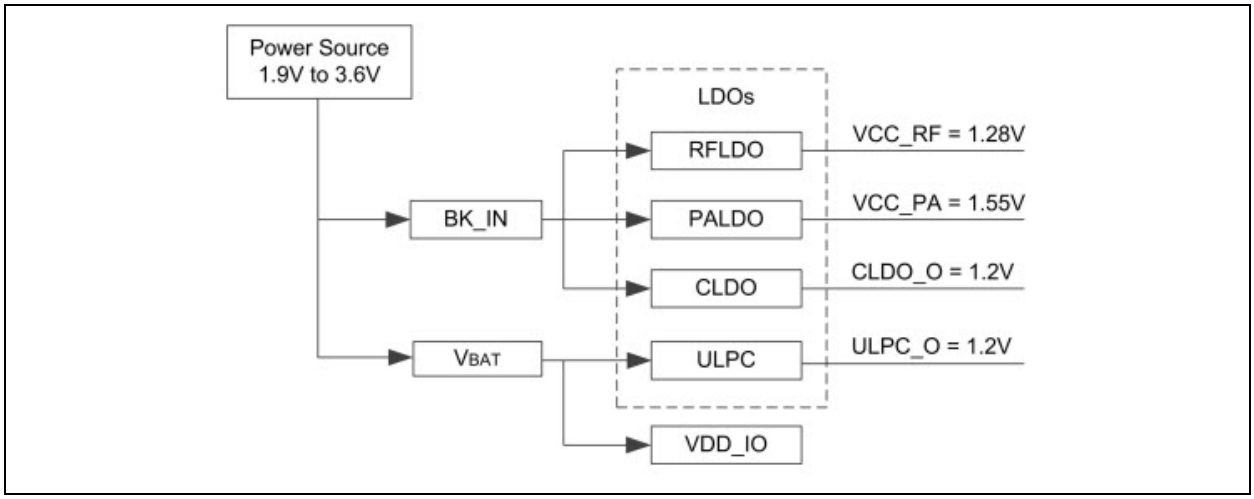
This section provides a description of the blocks used in the IS1870/71 SoC.

2.1.1 PMU

The IS1870/71 SoC includes a DC-DC converter and four LDOs. Microchip's Bluetooth Low Energy software stack is used for controlling and operating these LDOs in various modes, controlling the amount of time the peak current is active, maximizing the battery life. The factory firmware enables the designer to perform the calibration for the internal LDOs to compensate for variations in the board design and other manufacturing-related artifacts.

Figure 2-1 illustrates the power tree diagram of the IS1870/71 SoC.

FIGURE 2-1: IS1870/71 SOC POWER TREE DIAGRAM



2.1.2 ALWAYS ON LOGIC

Always On (AON) is the hardware-based state machine, which is controlled by Microchip's Bluetooth stack. Together, the software and hardware logic maintain the power-up, power-down and low power sequences of the IS1870/71 SoC, by providing optimal device performance. It includes an RTC timer and I/O detector to wake-up the system from Power-Saving mode using time out or external general I/O transition. This allows the SoC to run in Power-Saving mode while maintaining an active connection with a peer device and minimizing power consumption.

2.1.3 RF

This SoC is controlled by Microchip’s Bluetooth stack, which contains an on-chip RF circuit, a controller and a modulator (Tx)/demodulator (Rx). The Tx is used to control the synthesizer's phase and output power and modulate the data based on the Bluetooth Low Energy specifications. The Rx is used to decode the Bluetooth signal and optimize the performance, such as IQ-imbalance, suppress DC and flick noise. It is also used to compensate the frequency drift and offset, and filter out interference to maximize receiver sensitivity.

2.1.4 MCU

Microchip provides the Bluetooth Low Energy software stack, which runs on the IS1870/71 SoC’s internal 8051 core. The stack resides in a combination of ROM, RAM and embedded Flash. The software stack is responsible for scheduling the Bluetooth Low Energy tasks and for processing the Bluetooth Low Energy protocol and profiles.

2.2 System Block Specification

The following are the system block specifications.

> **Note:** The system blocks which make up the IS1870/71 SoC are listed below. However, some of the blocks used in the IS1870/71 SoC are controlled by the default factory firmware and are not available to the designer.

2.2.1 RF

- Bluetooth BT5.0 LE compliant SoC
- Frequency: 2.402 GHz to 2.480 GHz
- Programmable transmit output power up to +3 dBm maximum
- -25 dBm minimum Tx power to search nearby devices
- -90 dBm typical receiver power sensitivity
- Digital RSSI indicator (-50 dBm to -90 dBm)
- -40°C to +85°C Bluetooth Low Energy RF certified

2.2.2 PMU

- Operating battery input voltage range: 1.9V to 3.6V
- 1.28V RFLDO: RF IP power supply
- 1.55V PALDO: RF Tx power amplify supply
- 1.2V CLDO: Core-logic and memories supply
- 1.55V DC-DC switching buck converter
- 1.2V programmable ULPC to supply AON-logic and retention memory
- AON-logic to control power-up, power-down and wake-up procedures
- Internal 32 kHz (±250 ppm) ultra-low power oscillator
- Power-on Reset

2.2.3 MCU

- 8051 core with scalable clock
- ROM: 32 KB
- Main SRAM: 24 KB
- Embedded Flash: 256 KB for Device Firmware Upgrade (DFU) and run-time data storage

> **Note:** The Microchip provided Bluetooth Low Energy stack uses a portion of the available memory listed above. With the default factory firmware, the amount of memory used is fixed and the free memory is not available to the designer. As it is expected, the application will reside in the external host MCU. For details on altering the default factory setup, please contact your local Microchip representative.

2.2.4 PERIPHERALS

- Flexible GPIO pin configuration
- ADC:
  - 0V to 3.6V, 12-bit SDM-ADC with 16-channel (IS1870) or 6-Channel (IS1871) hybrid-I/O (Multi-Function). It can be configured as ADC or GPIO input
- Internal 1.9V to 3.6V battery voltage monitor
- Precision Temperature Sensor (PTS) for ambient temperature detection
- 4 MHz clock-rate full duplex 4-wire SPI with 256 bytes buffer DMA
- HCI over UART up to 921600 bps with flow-control
- Two wire serial interface (compatible to I^2C)

> **Note:** This peripheral is not available with the default factory firmware. For details on altering this default factory setup, contact your local Microchip representative.

- Three wire serial interface (compatible to SPI)

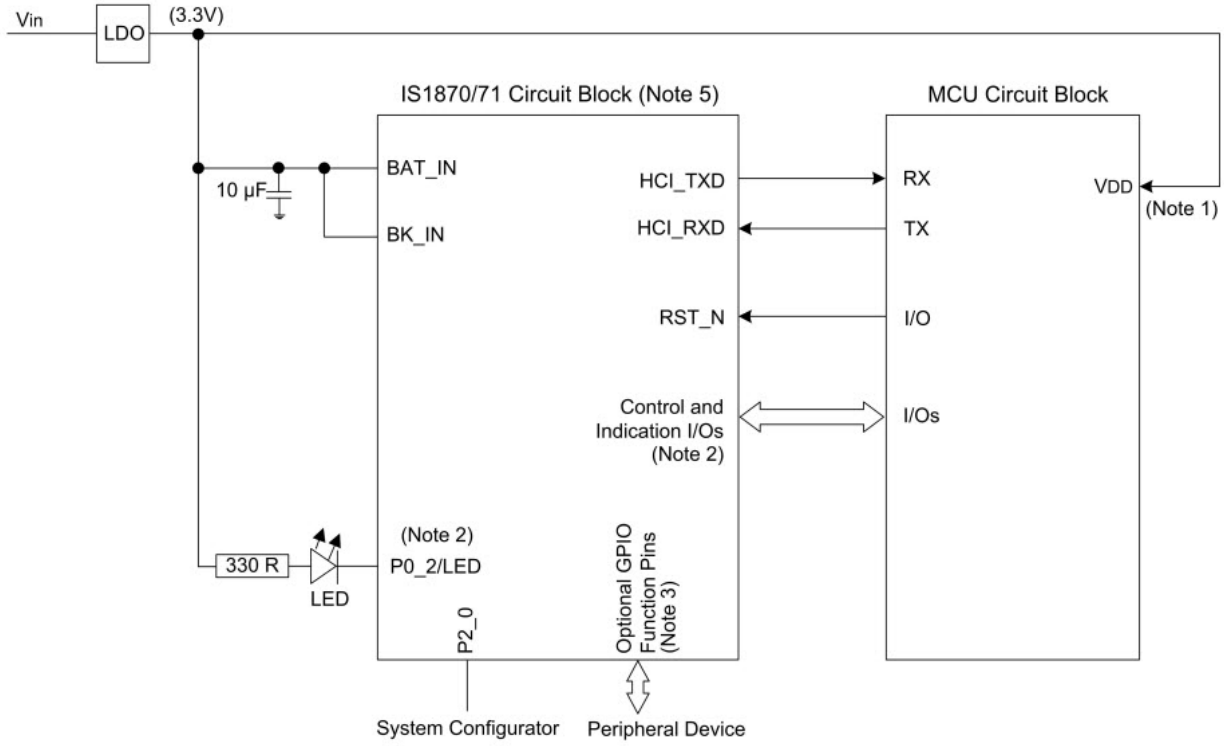
> **Note:** This peripheral is not available with the default factory firmware. For details on altering this default factory setup, please contact your local Microchip representative.

- GPIO pins with input internal pull up /Hi-Z selectable
- 24-bit low-power Real Time Counter (RTC) for background timer in Standby mode
- Watchdog timer
- Event Counter option (P1_4 and P1_5) provides capture/counter function to external events for frequency calculation. It provides 1K/32K/1M/16M clock rate option to count the frequency range from 60 Hz to 1 MHz. The continuous/one shot count mode can be selected
- Specific GPIO pins (P1_6 and P1_7) support external 32.768 kHz crystal option for RTC; however, the default from the factory is set to use the internal 32 kHz ultra low-power oscillator
- PWM:
  - 16-bit PWM design
  - Four Individual frequency and individual duty cycle channel outputs multiplexed with GPIO pins (P2_1, P2_2, P2_3 and P2_5)
  - Three clock source (32K, 1M and 16M) selections to program frequency range from 0.488 Hz to 8 MHz
  - Double buffers output compare registers and top register to avoid glitch
  - Two pair output configurable as inverse channel

2.3 Host MCU Interface Over UART

Figure 2-2 illustrates IS1870/71 SoC application block diagram. In the diagram the power supply (3.3V), UART interface and GPIO control and indication are listed.

FIGURE 2-2: IS1870/71 SOC APPLICATION BLOCK DIAGRAM WITH MCU



Note 1: Ensure BAT_IN (I/O voltage) and MCU V_{DD} voltage are compatible.

2: The control and indication ports are configurable in Microchip provided PC tool, referred to as the UI tool, see the product webpage for additional information.

3: Default factory firmware configuration enables the designer to control GPIO functions, ADC, PTS and PWM peripherals. The I^2C and SPI peripherals are not available with the default firmware. Contact your local Microchip representative for more details.

4: The GPIO applications of the IS1871 SoC have a reduced pin count, and some of the GPIO pins are not supported in the IS1871 SoC.

NOTES:

3.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the IS1870/71 SoC electrical characteristics. Additional information will be provided in future revisions of this document.

Absolute maximum ratings for the IS1870/71 devices are listed below. Exposure to the maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

(See Note)

Ambient temperature under bias with parts ending with 102 ..... -20°C to +70°C
Ambient temperature under bias with parts ending with 202 ..... -40°C to +85°C
Storage temperature ..... -40°C to +125°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +3.6V
Voltage on any pin with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Maximum output current sunk by any I/O pin.....12 mA
Maximum output current sourced by any I/O pin.....12 mA
ESD (according to machine model, JEDEC EIA/JESD22-A115-C)
Maximum output for all pins, excluding RF Tx pin .....±200V
Maximum output for all pins .....±150V
Maximum output (human-body model).....±2 kV
Maximum output (charge-device model).....±150V

Note:	Stresses listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions, and those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3-1 provides the recommended operating conditions of the IS1870/71 SoC.

TABLE 3-1: RECOMMENDED OPERATING CONDITIONS

Symbol	Min.	Typ.	Max.
PMU			
V_{DD} (V_{BAT}, BK_IN, AV_{DD})	1.9V	3.0V	3.6V
RST_N	1.9V	3.0V	3.6V
Other I/O	1.9V	—	3.6V
GPIO			
V_{IH} (Input High Voltage)	0.7 V_{DD}	—	V_{DD}
V_{IL} (Input Low Voltage)	VSS	—	0.3 V_{DD}
V_{OH} (Output High Voltage) (High drive, 12 mA)	0.8 V_{DD}	—	V_{DD}
V_{OL} (Output Low Voltage) (High drive, 12 mA)	VSS	—	0.2 V_{DD}
Pull up Resistance	34 kOhm	48 kOhm	74 kOhm
Pull down Resistance	29 kOhm	47 kOhm	86 kOhm
Supply Current (see **Note 1**)			
Tx mode peak current at V_{DD}=3V, Tx=0 dBm, Buck mode	—	10 mA at +25°C	13 mA at +70°C/+85°C
Rx mode peak current at V_{DD}=3V, Buck mode	—	10 mA at +25°C	13 mA at +70°C/+85°C
"Reduced current consumption" low power mode current (see **Note 2**)	—	60 µA at +25°C	—
"Shutdown" low power mode current (see **Note 2**)	1.0 µA	—	2.9 µA
Analog-to-Digital Converter (ADC) for IS1870/71-202			
Full scale (BAT_IN)	0V	3.0V	3.6V
Full scale (AD0 to AD15)	0V	—	3.6V
Operating Temperature Range	-40°C	25°C	85°C
Operating current	—	—	500 µA
DNL (ENOB 10-bit, ADC in 32 KHz Mode) (see **Note 3 and 4**)	-1	—	+1.5
INL (ENOB 10-bit, ADC in 32 KHz Mode) (see **Note 3 and 4**)	-2 LSB	—	+2 LSB
Precise Temperature Sensor (PTS) for IS1870/71-202			
Detect range	-40°C	—	+85°C
Digital Output	1160	—	2649
Resolution	—	12-bit/°C	—
Accuracy	-3°C	—	+3°C

Note 1: The current measurements are characterized across a sample of the BM70/71 module at room temperature (+25°C), unless otherwise noted.

2: For more details on "Reduced current consumption" or "Shutdown" low power modes, refer to the "*BM70/71 Bluetooth® Low Energy Module User's Guide*" (DS50002542). This rating is part of the characterization of the default factory firmware.

3: ADC performance characterized with V1.06 production firmware across a set of IC's are not tested during production.

4: Calculated DNL/INL values are determined using "Best Fit" method.

Table 3-2 provides the RF specifications of the IS1870/71 SoC.

TABLE 3-2: RF SPECIFICATIONS

Parameter		Min.	Typ.	Max.
Transmitter				
Frequency		2402 MHz	—	2480 MHz
Output Power		—	0 dBm	—
RF Power Control Range		-25 dBm	—	3 dBm
In-band Spurious (N±2)		—	-38.5 dBm	—
In-band Spurious (N±3)		—	-43.25 dBm	—
Modulation Characteristic - Frequency Deviation (see **Note 1**)		—	247 kHz	—
Receiver				
Frequency		2402 MHz	—	2480 MHz
Sensitivity Level (Interference active)		—	-90 dBm	—
Interference Performance	Co-channel	—	17 dB	—
	Adjacent ± 1 MHz	—	0 dB	—
	Adjacent ± 2 MHz	—	-25 dB	—
	Adjacent >= ± 3 MHz	—	-32 dB	—
Intermodulation Characteristic (n=3,4,5)		—	-37.5 dBm	—
Maximum Usable Level			0 dBm	

Note 1: Tested with a known pattern of ‘00001111’b being transmitted.

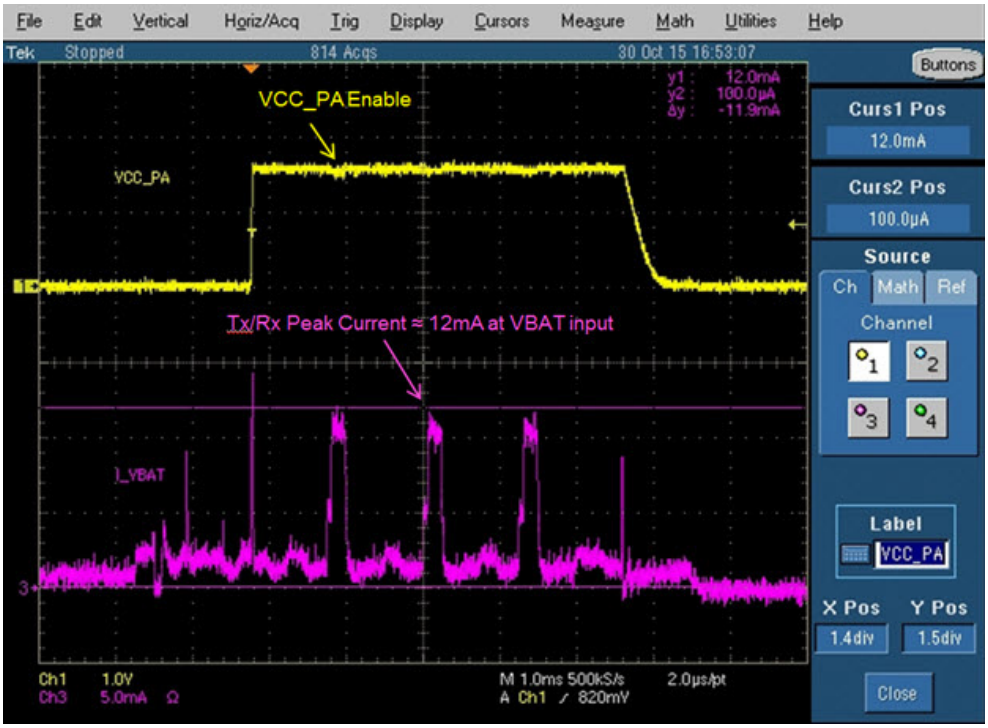
3.1 Current Consumption Details

3.1.1 Tx/Rx CURRENT CONSUMPTION DETAILS

Figure 3-1 illustrates the average current consumption of an advertising event during Bluetooth Low Energy operation of the IS1870/71 SoC.

The peak current of the VBAT input is 12 mA and the average current is around 230 µA. In this example the advertising interval is 100 ms and current consumption is measured at 3.3V VBAT input.

FIGURE 3-1: AVERAGE CURRENT CONSUMPTION DURING ADVERTISING

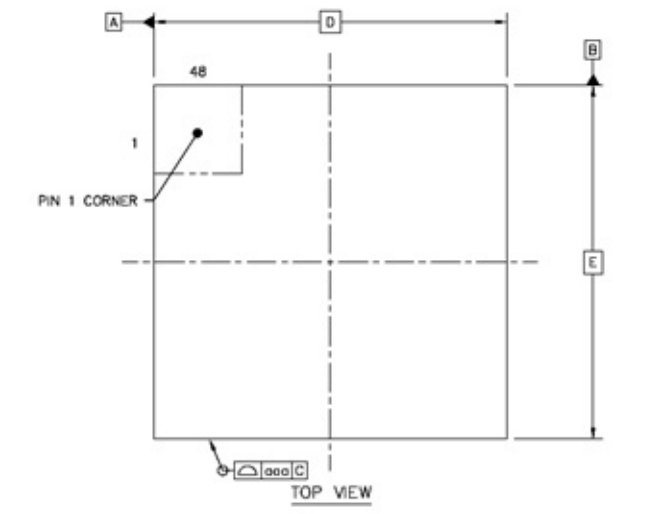


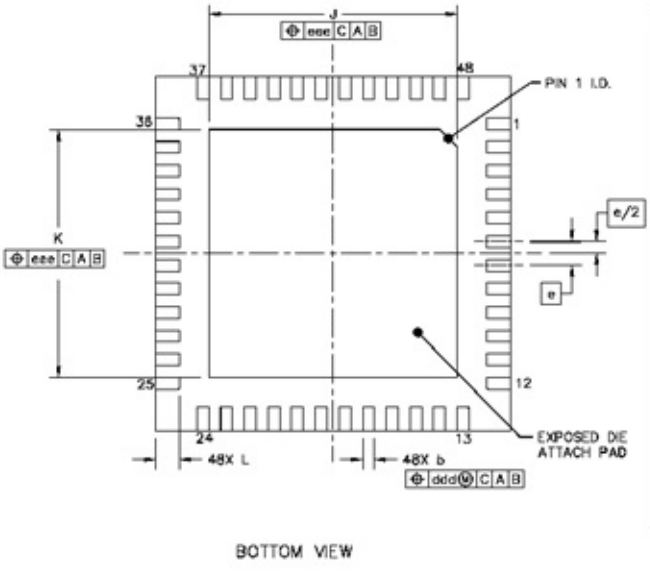
4.0 PACKAGE INFORMATION

Figure 4-1 through Figure 4-5 illustrate the package marking information of the IS1870SF IC.

4.1 48QFN, 6x6 mm SoC Outline (IS1870SF)

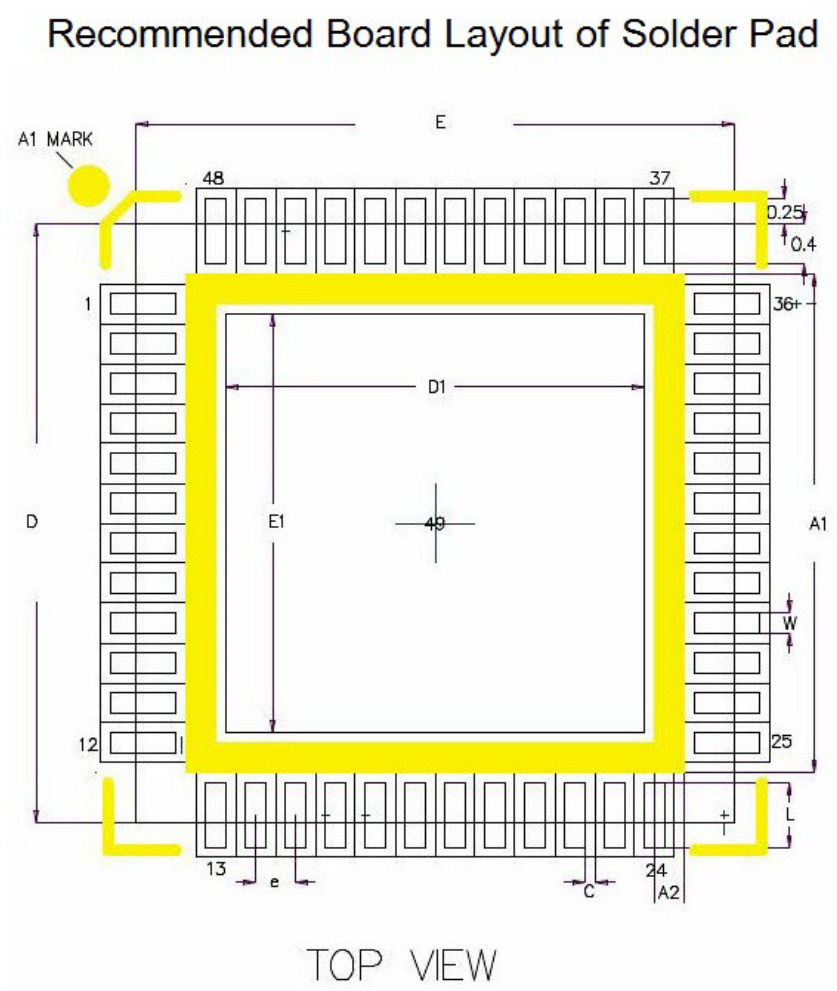
FIGURE 4-1: 48QFN, 6X6 MM PACKAGE INFORMATION (IS1870SF)





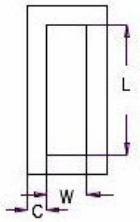
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	4.1	4.2	4.3
	Y	K	4.1	4.2	4.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

FIGURE 4-2: 48QFN, 6X6 MM FOOTPRINT INFORMATION (IS1870SF)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SILKSCREEN TOP L	A1		5	REF
SILKSCREEN TOP W	A2		0.3	REF
BODY SIZE	D		6	BSC
	E		6	BSC
EXPOSED PAD SIZE	D1		4.2	BSC
	E1		4.2	BSC
LEAD LENGTH	L		0.65	
LEAD WIDTH	W		0.2	
SOLDER MASKER OPEN	c		0.1	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		48	

UNIT : MM

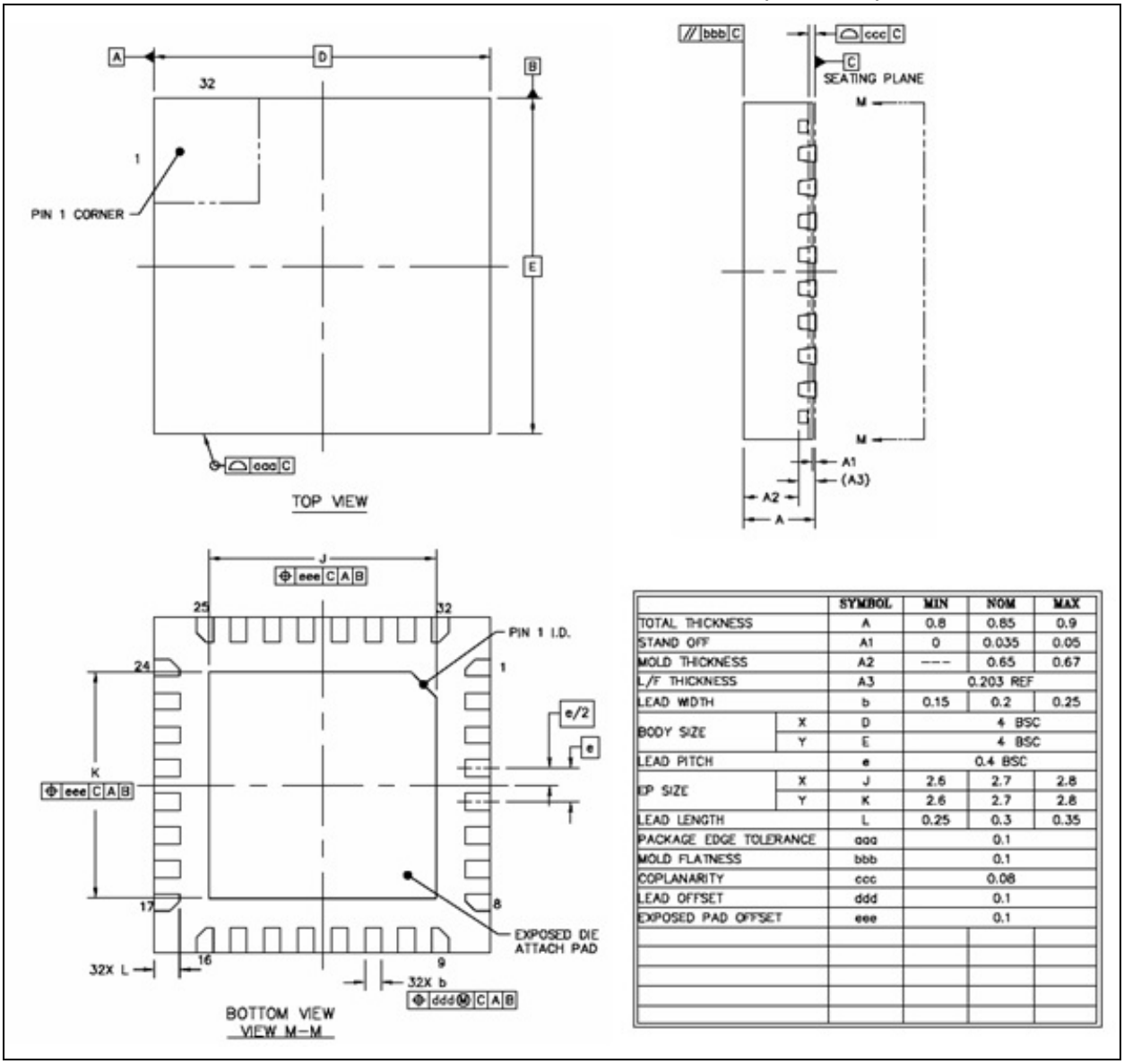


SOLDERMASK OPENING OUTSIDE OF LAND

SCALE 2:1

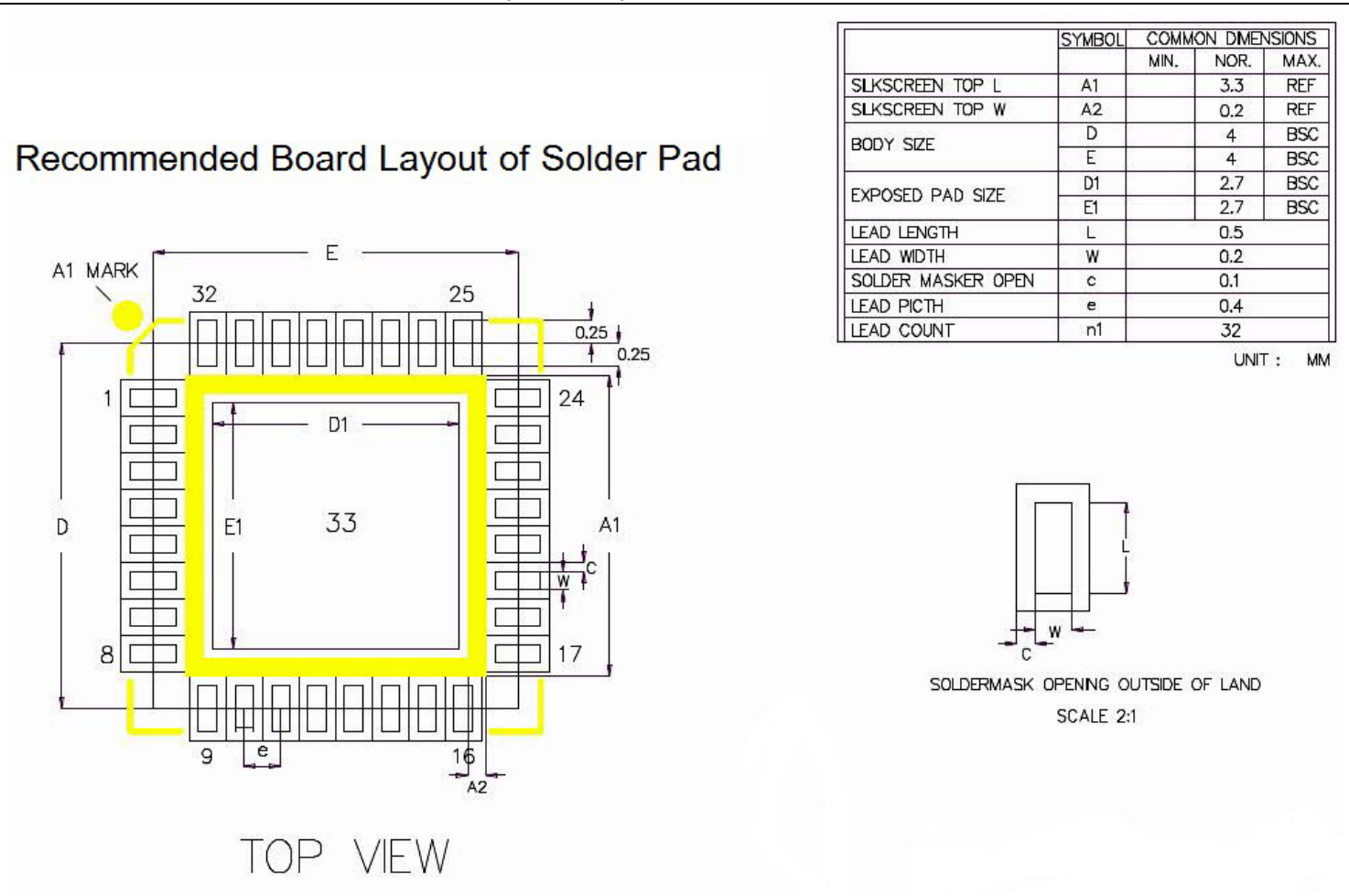
4.2 32QFN, 4x4 mm SoC Outline (IS1871SF)

FIGURE 4-3: 32QFN, 4X4 MM PACKAGE SIZE INFORMATION (IS1871SF)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.25	0.3	0.35
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

FIGURE 4-4: 32QFN FOOTPRINT INFORMATION (IS1871SF)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
SLKSCREEN TOP L	A1		3.3	REF
SLKSCREEN TOP W	A2		0.2	REF
BODY SIZE	D		4	BSC
	E		4	BSC
EXPOSED PAD SIZE	D1		2.7	BSC
	E1		2.7	BSC
LEAD LENGTH	L		0.5	
LEAD WIDTH	W		0.2	
SOLDER MASKER OPEN	c		0.1	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		32	

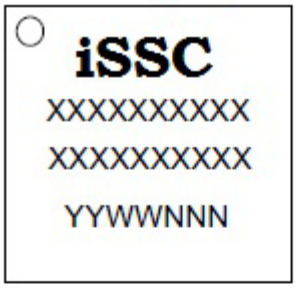
UNIT : MM

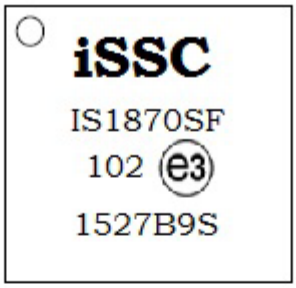
SOLDERMASK OPENING OUTSIDE OF LAND

SCALE 2:1

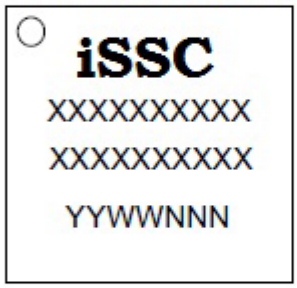
FIGURE 4-5: PACKAGE MARKING INFORMATION

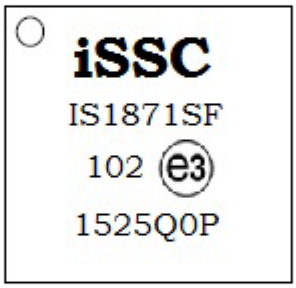
48-Lead QFN (6x6x0.9 mm)





32-Lead QFN (4x4x0.9 mm)





Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

NOTES:

5.0 REFLOW PROFILE AND STORAGE CONDITION

Figure 5-1 and Figure 5-2 illustrate the reflow profiles and stencil information of the IS1870/71 SoC.

5.1 Stencil of SMT Assembly Suggestion

5.1.1 STENCIL TYPE AND THICKNESS

- Laser cutting
- Stainless steel
- Thickness: 0.5 mm pitch, thickness more than 0.15 mm

5.1.2 APERTURE SIZE AND SHAPE FOR TERMINAL PAD

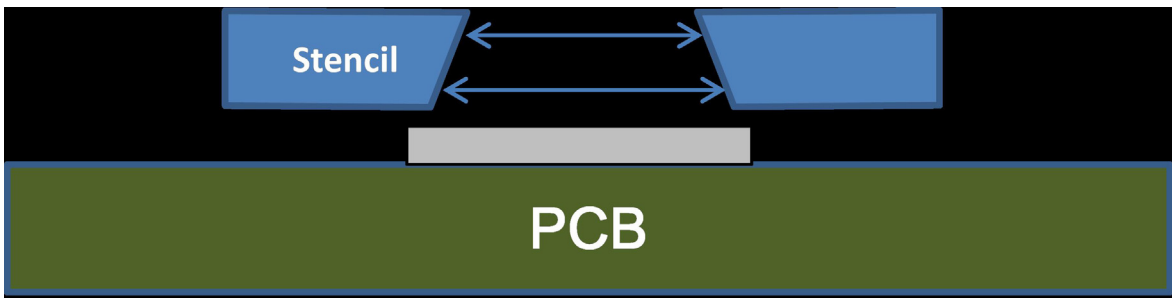
- Aspect ratio (width/thickness) more than 1.5
- Aperture shape
  - The stencil aperture is designed to match the pad size on the PCB
  - Oval-shape opening is used to get the optimum paste release
  - Rounded corners to minimize the clogging
  - Positive taper walls (5° tapering) with the bottom opening larger than the top opening

5.1.3 APERTURE DESIGN FOR THERMAL PAD

- Small multiple openings are used instead of one big opening, see Figure 5-1
- 60 to 80% solder paste coverage
- Rounded corners to minimize clogging
- Positive taper walls (5° tapering) with the bottom opening larger than the top opening, see Figure 5-2

FIGURE 5-1: REFLOW PROFILE

FIGURE 5-2: STENCIL TYPE

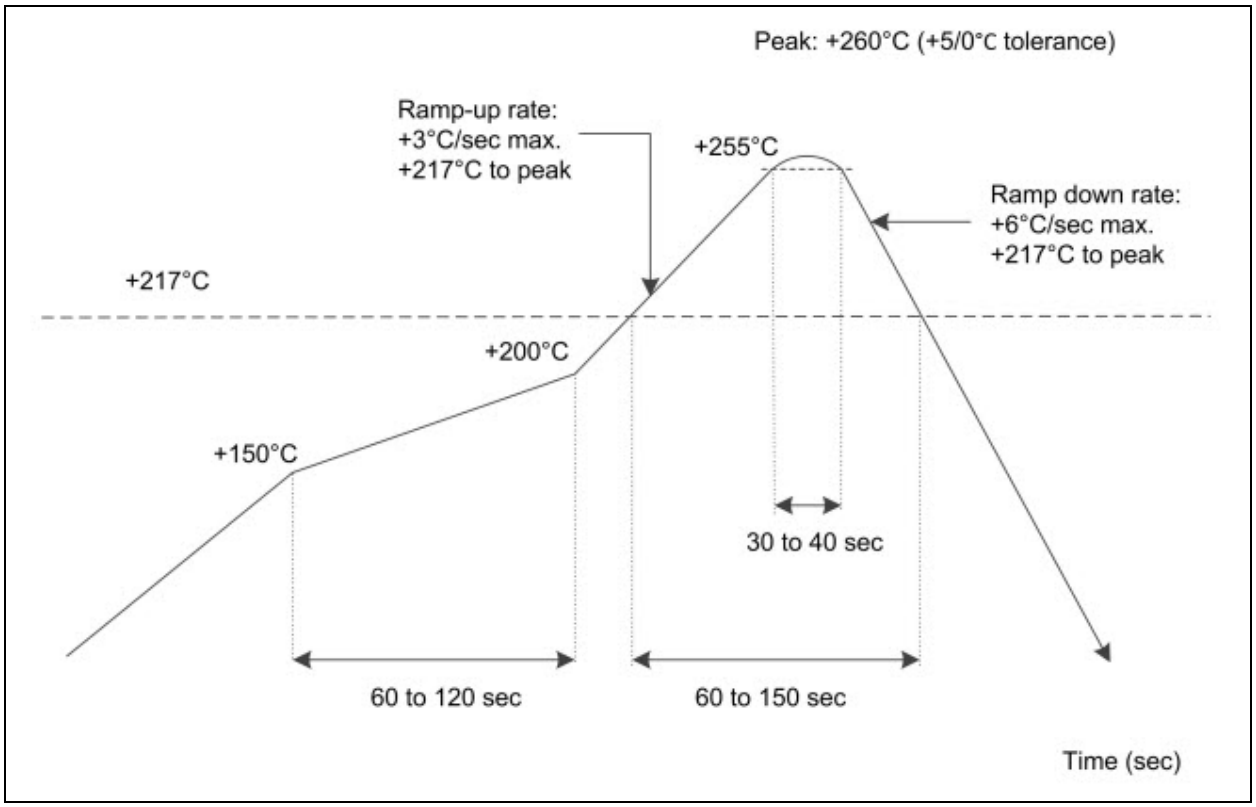


5.2 Reflow Profile

Figure 5-3 illustrates the reflow profile and the following are its specific features:

- Standard Condition: IPC/JEDEC J-STD-020
- Preheat: +150 ℃ to +200 ℃ for 60 to 120 seconds
- Average ramp-up rate (+217℃ to peak): +3℃/sec max
- Temperature maintained above +217 ℃ : 60 to 150 seconds
- Time within +5 ℃ of peak temperature: 30 to 40 seconds
- Peak temperature: +260 ℃ with 5/-0 ℃ tolerance
- Ramp-down rate (peak to +217℃): +6℃/sec. max
- Time within +25℃ to peak temperature: 8 minutes max
- Cycle interval: 5 minutes

FIGURE 5-3: REFLOW PROFILE



5.3 Storage Condition

Users are required to follow these specific storage conditions for the IS1870/71 SoC.

- The calculated shelf life in the sealed bag is 24 months at <+40 ℃ and <90% Relative Humidity (RH)
- After the bag is opened, devices that are subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions, i.e <+30 ℃ /60% RH

NOTES:

6.0 ORDERING GUIDE

Table 6-1 provides the ordering information for the IS1870/71 SoC.

TABLE 6-1: ORDERING GUIDE

Device	Bluetooth Version	Operating Temperature Range	Package	Part No.
IS1870SF-102	Bluetooth Low Energy SoC, Bluetooth Low Energy 5.0 compliant	-20°C to +70°C	48-Lead QFN, 6x6x0.9 mm^3, 0.4 mm pitch	IS1870SF-102
IS1871SF-102	Bluetooth Low Energy SoC, Bluetooth Low Energy 5.0 compliant	-20°C to +70°C	32-Lead QFN, 4x4x0.9 mm^3, 0.4 mm pitch	IS1871SF-102
IS1870SF-202	Bluetooth Low Energy SoC, Bluetooth Low Energy 5.0 compliant	-40°C to +85°C	48-Lead QFN, 6x6x0.9 mm^3, 0.4 mm pitch	IS1870SF-202
IS1871SF-202	Bluetooth Low Energy SoC, Bluetooth Low Energy 5.0 compliant	-40°C to +85°C	32-Lead QFN, 4x4x0.9 mm^3, 0.4 mm pitch	IS1871SF-202

Note: The IS1870/71 SoC can be purchased through a Microchip representative. Visit http://www.microchip.com/ for ordering information.

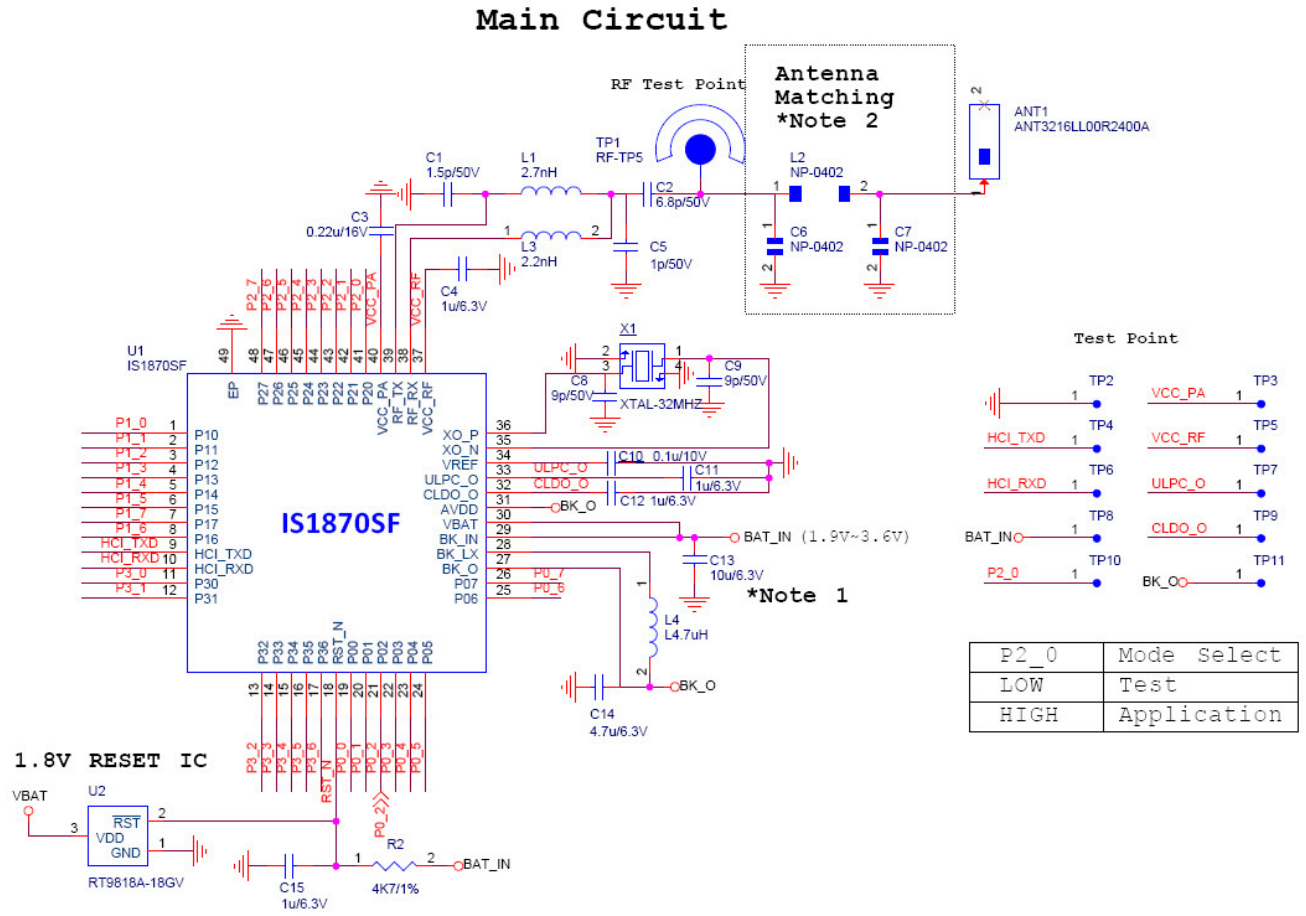
NOTES:

APPENDIX A: REFERENCE CIRCUIT

Figure A-1 through Figure A-4 illustrate a typical application circuit of the IS1870 and IS1871 SoC.

The application circuit lists the RF matching circuit, PMU power tree, LED option, test points and configuration table. The GPIOs can be configured to general I/O functions or the function of ADC, PTS, PWM and external 32.768 kHz crystal.

FIGURE A-1: IS1870 SOC APPLICATION CIRCUIT



Note 1: The C13, C14, L4, C12, C11, C10, C3 and C4 must be as close to the chip as possible.

2: The value of the antenna matching component depends on the user's antenna and PCB layout.

FIGURE A-2: IS1870 SOC APPLICATION CIRCUIT (OPTIONAL)

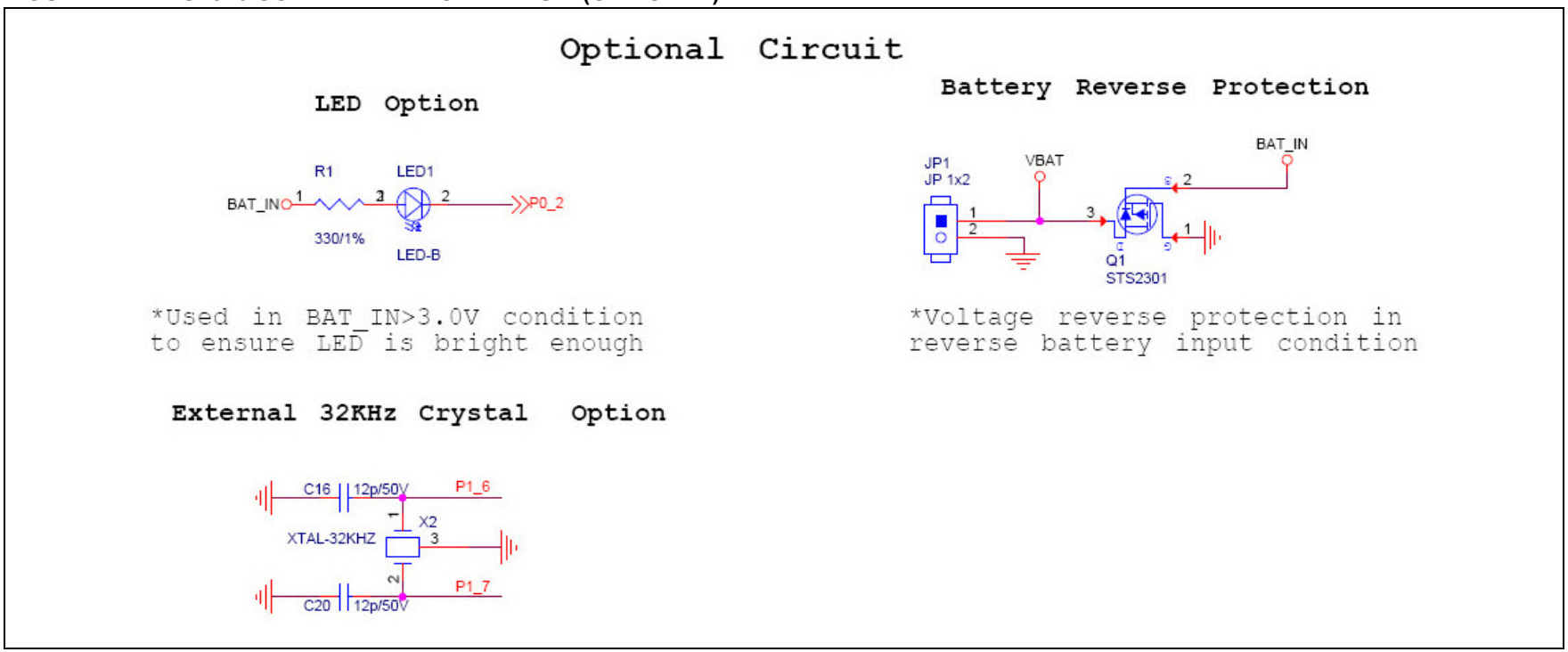
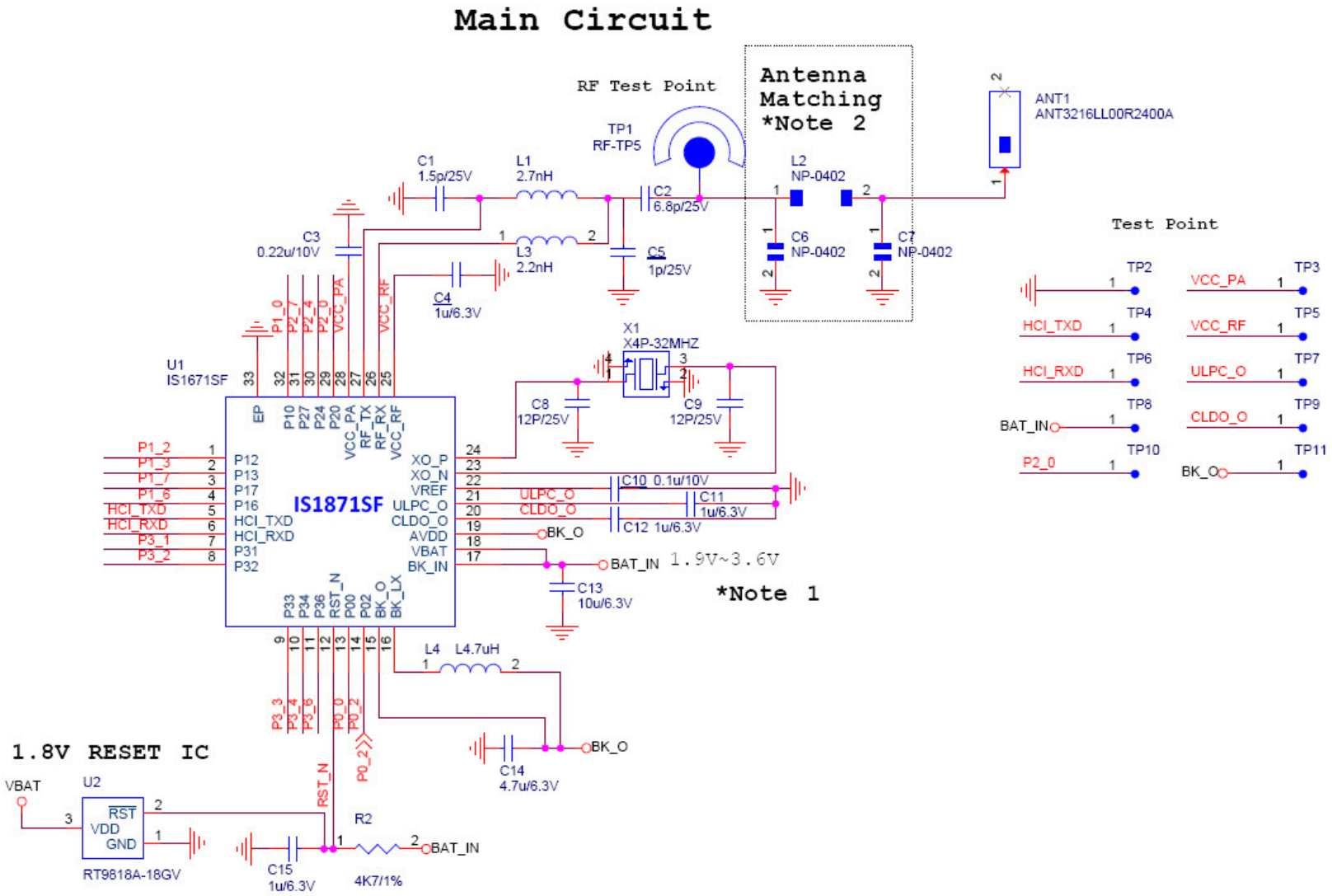


FIGURE A-3: IS1871 SOC APPLICATION CIRCUIT



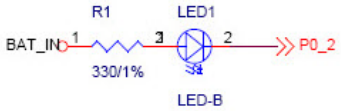
Note 1: The C13, C14, L4, C12, C11, C10, C3 and C4 must be as close to the chip as possible.

2: The value of the antenna matching component depends on the user's antenna and PCB layout.

FIGURE A-4: IS1871 SOC APPLICATION CIRCUIT (OPTIONAL)

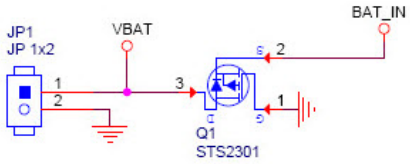
Optional Circuit

LED Option



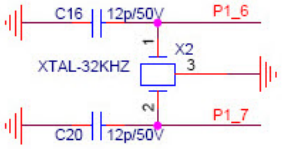
*Used in BAT_IN>3.0V condition to ensure LED is bright enough

Battery Reverse Protection



*Voltage reverse protection in reverse battery input condition

External 32KHz Crystal Option



APPENDIX B: LAYOUT GUIDELINES

B.1 RF Matching

The RF traces (Tx, Rx and antenna path) on the PCB antenna must match the 50 Ohm impedance. In Figure A-1, value of L1, L3, C1, C2 and C5 are fixed. The antenna matching components, C6, C7 and L2, must be adjusted to match with the 50 Ohm 2.4 GHz antenna.

B.2 PMU

The PMU section components, such as V_{BAT}, BK_IN, BK_O, BK_LX, AV_{DD}, ULPC_O, CLDO_O, V_{REF} must be kept close to the IS1870/71 SoC. The L4 and C14 of Buck section, illustrated in Figure A-1, must be selected carefully. The capacitor C14 is either 4.7 µF/ 6.3V, X5R or X7R type. The inductor L4 must be a high current (I_{DC}>300 mA) and low DCR (<1 Ohm) type.

For additional information on the PCB antenna design guidelines, contact your local Microchip sales office. A list of Microchip sales offices is given on the back page of this document.

B.3 Crystal

The XI 32 MHz crystal specification must be within the ±10 ppm range, see Figure A-1.

NOTES:

APPENDIX C: REVISION HISTORY

Revision A (October 2015)

This is the initial released version of this document.

Revision B (October 2015)

This revision includes the following changes as well as minor updates to text and formatting, which were incorporated throughout the document.

Status	Description
"Features"	The section has been updated with new information.
"Packages"	The section is updated with the package information.
1.0 "Device Overview"	Updated Figure 1-1 and Figure 1-2. Added Table 1-1

Revision C (March 2016)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

Status	Description
"Features"	The section is updated with new information.
1.0 "Device Overview"	Updated Figure 1-1 and Figure 1-2. Updated Table 1-1 and Table 1-2.
2.0 "System Block Details"	Updated **2.2 "System Block Specification"** and **2.3 "Host MCU Interface Over UART"** with new information.
3.0 "Electrical Characteristics"	Updated **3.1.1 "Tx/Rx Current Consumption Details"**. Updated Figure 3-1 and Figure 3-1. Updated Table 3-1 and Table 3-2.
5.3 "Storage Condition"	Deleted Figure 5-4.
6.0 "Ordering Guide"	Updated Table 6-1
Appendix A: "Reference Circuit"	Updated Figure A-1 and Figure A-3 Added Figure A-2 and Figure A-4
Appendix C: Bill of Material	Deleted

Revision D (February 2017)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

Section	Update Description
"Features"	Updated this section.
"Packages"	Updated the I/O pins details.
"Operating Conditions"	Updated the operating temperature details.
1.0 "Device Overview"	Updated Figure 1-1 and Figure 1-2.
2.0 "System Block Details"	Updated Figure 2-2.
3.0 "Electrical Characteristics"	Updated ambient temperature, maximum output (human-body model) details and Table 3-1. Added Table 3-2.
6.0 "Ordering Guide"	Updated Table 6-1

Revision E (February 2018)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

Section	Update Description
1.0 “Device Overview”	Updated Table 1-2.
3.0 “Electrical Characteristics”	Updated Table 3-1.

Revision F (February 2021)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

Section	Update Description
2.2 “System Block Specification”	Performed following change: • 4-wire master/slave SPI to 4-wire SPI
3.0 “Electrical Characteristics”	Updated the following values in Table 3-1. • Digital Output Min value from 1387 to 1160 • Digital Output Max value from 2448 to 2649

Revision G (September 2021)

This revision includes the following changes and minor updates to text and formatting, which were incorporated throughout the document.

Section	Update Description
1.0 “Device Overview”	Performed following change: • Updated Bluetooth version from 4.2 to 5.0 • Updated Table 1-2 with new terminology, see the following note
2.2 “System Block Specification”	Performed the following change: • Updated Bluetooth version from 4.2 to 5.0
6.0 “Ordering Guide”	Performed the following change: • Updated Bluetooth version from 4.2 to 5.0

Note: Microchip is aware that some terminologies used in the technical documents and existing software codes of this product are outdated and unsuitable. This document may use these new terminologies, which may or may not reflect on the source codes, software GUIs, and the documents referenced within this document. The following table shows the relevant terminology changes made in this document.

TABLE G-1: TERMINOLOGY RELATED CHANGES

Old Terminology	New Terminology	Description
Master mode	Central mode	Table 1-2 is updated with new terminology.

Note the following details of the code protection feature on Microchip products:

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Microchip:

IS1870SF-102-TRAY IS1871SF-102 IS1870SF-102 IS1871SF-102-TRAY IS1870SF-202 IS1870SF-202-TRAY IS1871SF-202 IS1871SF-202-TRAY