HV9963

Closed-Loop LED Driver with Enhanced PWM Dimming

Features

- Switch-mode Controller for Single-switch Drivers:
  - Buck
  - Boost
  - Buck-boost
  - SEPIC
- High Output Current Accuracy
- High PWM Dimming Ratio (>5000:1)
- Internal 40V Linear Regulator
- Internal ±2% Voltage Reference
- Constant Frequency Operation with Sync Capability
- Programmable Soft Start
- 10V Gate Drivers
- Hiccup Mode Protection for both LED String Short-Circuit and Open-Circuit conditions

Applications

- RGB or White LED Backlighting
- Battery-Powered LED Lamps
- Other DC/DC LED Drivers

General Description

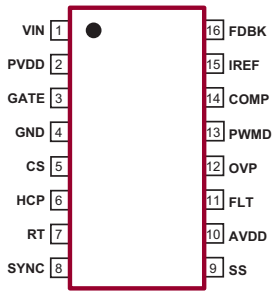
The HV9963 is a Current-mode control LED driver IC designed to control single-switch PWM converters (buck, boost, buck-boost, or SEPIC) in a Constant Frequency mode. The controller uses a Peak Current-mode control scheme (with programmable slope compensation) and includes an internal transconductance amplifier to accurately control the output current over all line and load conditions. Multiple HV9963s can be synchronized with each other or with an external clock using a SYNC pin. The IC also provides a disconnect switch GATE drive output, which can disconnect the LEDs using an external disconnect FET in case of a Fault condition and help achieve high PWM dimming ratio. The 10V external FET drivers allow the use of standard level FETs. The low-voltage 5.0V AV_{DD} is used to power the internal control logic circuitry and also acts as a reference voltage to set the output LED current level.

The HV9963 includes an enhanced PWM dimming logic that enables very high PWM dimming ratios.

The HV9963 also provides a TTL-compatible, low-frequency PWM dimming input that can accept an external control signal with a duty ratio of 0% to100% and a frequency of up to a few tens of kilohertz.

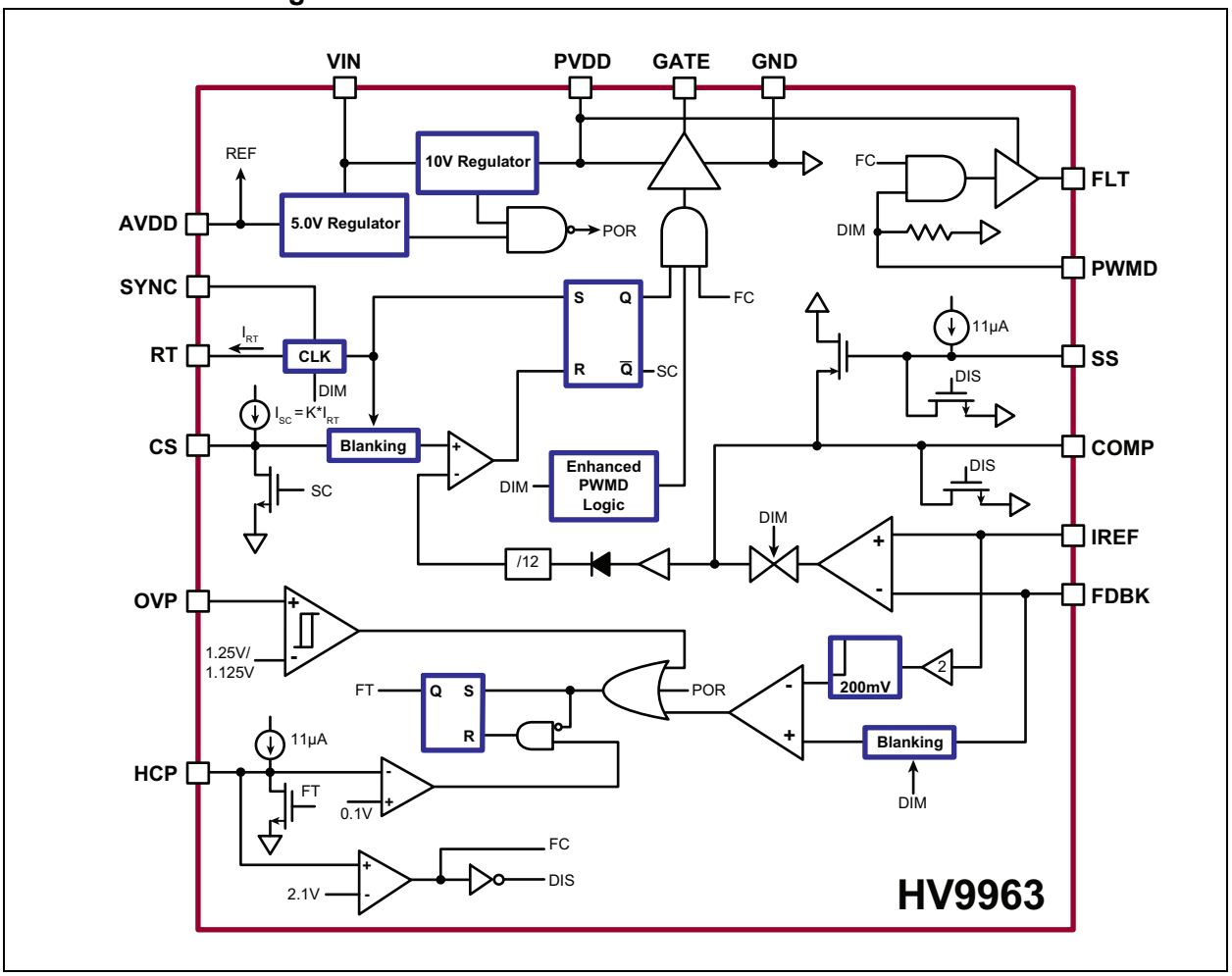
Package Type

16-lead SOIC
(Top view)

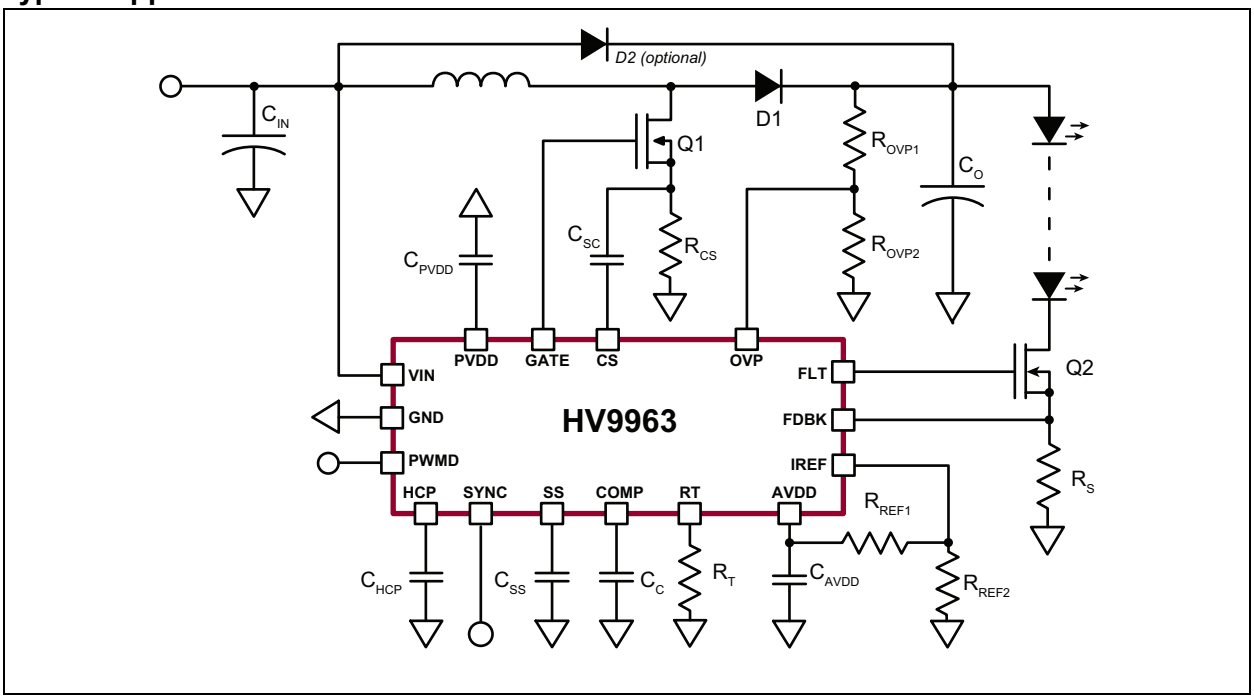


Refer to Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN} to GND .....–0.5V to +45V
PV_{DD} to GND .....–0.3V to +13V
GATE and FLT to GND.....–0.3V to PV_{DD} +0.3V
AV_{DD} to GND.....–0.3V to +6V
IREF to GND .....–0.3V to +3.5V
All Other Pins to GND ..... –0.3V to AV_{DD} +0.3V
Continuous Power Dissipation (T_A= +25°C)..... 1000 mW
Junction Temperature Range ..... –40°C to +150°C
Storage Temperature Range ..... –65°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C, V_{IN} = 24V, C_{PVDD} = 1 µF, C_{AVDD} = 1 µF, C_{GATE} = 2 nF, C_{FLT} = 330 pF unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
INPUT						
Input DC Supply Voltage Range	V_{INDC}	8	—	40	V	DC input voltage
Shutdown Mode Supply Current	I_{INSD}	—	—	2	mA	PWMD = GND
INTERNAL REGULATOR FOR GATE DRIVERS						
PV_{DD} Internally Regulated Voltage	PV_{DD}	9.5	10	10.5	V	V_{IN} = 12V to 40V, R_T = 44.2 kΩ, PWMD = AV_{DD}
PV_{DD} Undervoltage Lockout Upper Threshold	$UVLO_{RISE}$	6.55	—	7.2	V	PV_{DD} rising (**Note 1**)
PV_{DD} Undervoltage Lockout Hysteresis	$UVLO_{HYST}$	—	500	—	mV	PV_{DD} falling
Minimum PV_{DD} Voltage	$PV_{DD,MIN}$	8	—	—	V	V_{IN} = 9V, R_T = 44.2 kΩ, PWMD = AV_{DD} (**Note 1**)
INTERNAL LOW-VOLTAGE REGULATOR						
AV_{DD} Internally Regulated Voltage	AV_{DD}	4.9	5	5.1	V	V_{IN} = 8V to 40V
		4.85	—	5.1	V	V_{IN} = 8V to 40V, 0°C < T_A < +85°C
		4.82	—	5.1	V	V_{IN} = 8V to 40V, –40°C < T_A < +125°C
AV_{DD} Undervoltage Lockout Upper Threshold	$UVLO_{RISE,A}$	4.6	—	4.7	V	AV_{DD} rising (**Note 2**)
AV_{DD} Undervoltage Hysteresis	$UVLO_{HYST,A}$	—	600	—	mV	AV_{DD} falling (**Note 2**)
External Current Draw	$I_{AVDD,EXT}$	0	—	500	µA	
PWM DIMMING						
PWMD Input Low Voltage	$V_{PWMD(LO)}$	—	—	0.8	V	(**Note 1**)

Note 1: The specifications which apply over the full operating ambient temperature range at –40°C < T_A < +125°C are guaranteed by design and characterization.

2: For design guidance only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: T_A = 25°C, V_{IN} = 24V, C_{PVDD} = 1 µF, C_{AVDD} = 1 µF, C_{GATE} = 2 nF, C_{FLT} = 330 pF unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PWMD Input High Voltage	$V_{PWMD(HI)}$	2	—	—	V	(**Note 1**)
PWMD Pull-Down Resistance	R_{PWMD}	50	100	150	kΩ	V_{PWMD} = 3.3V
GATE DRIVER						
Gate Short-Circuit Current, Sourcing	I_{SOURCE}	0.2	—	—	A	V_{GATE} = 0V
Gate Sinking Current	I_{SINK}	0.4	—	—	A	V_{GATE} = 10V
Gate Output Rise Time	t_{RISE}	—	—	60	ns	
Gate Output Fall Time	t_{FALL}	—	—	60	ns	
OVERVOLTAGE PROTECTION						
Overvoltage Rising Trip Point	$V_{OVP,RISING}$	1.2	1.25	1.4	V	OVP rising (**Note 1**)
Overvoltage Hysteresis	$V_{OVP,HYST}$	—	0.125	—	V	OVP falling
HICCUP TIMER						
Charging Current	I_{HCP+}	8.8	11	20	µA	HCP = GND
Voltage Swing for Hiccup Timer	ΔV_{HCP}	—	2	—	V	
Discharging Current	I_{HCP-}	10	—	—	mA	V_{HCP} = 5V
SOFT START						
Charging Current	I_{SS+}	8.8	11	20	µA	SS = GND
Discharging Current	I_{SS-}	1	—	—	mA	V_{SS} = 5V
SLOPE COMPENSATION						
ON Resistance of Discharge FET at CS Pin	$R_{DIS,CS}$	100	300	600	Ω	(**Note 1**)
Current Sourced Out of CS Pin	I_{SC}	1.8	2	4	µA	R_T = 237 kΩ
CURRENT SENSE						
Leading Edge Blanking	$t_{BLANK,CS}$	100	—	300	ns	(**Note 1**)
Delay to Output of Comparator	t_{DELAY1}	—	—	200	ns	COMP = A_{VDD}, 50 mV overdrive at CS
Internal Resistor Divider Ratio (COMP to CS)	R_{DIV}	—	0.0833	—	—	(**Note 2**)
Comparator Offset Voltage	V_{OFFSET}	–20	—	+20	mV	
INTERNAL TRANSCONDUCTANCE OPAMP						
Gain Bandwidth Product	GBW	—	1	—	MHz	150 pF capacitance at COMP pin (**Note 2**)
Open-Loop DC Gain	A_V	65	—	—	dB	Output open
Input Common Mode Range	V_{CM}	–0.3	—	3	V	(**Note 2**)
Output Voltage Range	V_O	0.7	—	AV_{DD}–0.7	V	(**Note 2**)
Transconductance	g_m	1600	2000	2400	µA/V	
Input Offset Voltage	$V_{OS(IN)}$	–3	—	+3	mV	V_{IREF} = 200 mV (**Note 1**)
COMP Sink Current	$I_{COMP,SINK}$	–0.2	—	—	mA	V_{FDBK} = AV_{DD}, V_{IREF} = 0V, V_{COMP} = 0V (**Note 2**)

Note 1: The specifications which apply over the full operating ambient temperature range at –40°C < T_A < +125°C are guaranteed by design and characterization.

2: For design guidance only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: T_A = 25°C, V_{IN} = 24V, C_{PVDD} = 1 µF, C_{AVDD} = 1 µF, C_{GATE} = 2 nF, C_{FLT} = 330 pF unless otherwise specified.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
COMP Source Current	$I_{COMP,SRC}$	0.2	—	—	mA	V_{FDBK} = 0V, V_{IREF} = 3V, V_{COMP} = AV_{DD}–0.7V (**Note 2**)
Input Bias Current	I_{BIAS}	—	0.5	1	nA	(**Note 2**)
Discharging Current	$I_{COMP,DIS}$	1	—	—	mA	V_{COMP} = 5V
OSCILLATOR						
Oscillator Frequency	f_{OSC1}	88	100	112	kHz	R_T = 237 kΩ (**Note 1**)
	f_{OSC2}	460	520	580	kHz	R_T = 44.2 kΩ (**Note 1**)
Oscillator Frequency Range	f_{OSC}	—	—	600	kHz	(**Note 2**)
Maximum Duty Cycle	D_{MAX}	87	—	94	%	(**Note 1**)
Sync Input High	V_{SYNCH}	2	—	—	V	
Sync Input Low	V_{SYNCL}	—	—	0.8	V	
Sync Output Current	$I_{OUTSYNC}$	—	25	—	µA	
Sync Input Current	I_{INSYNC}	0	—	200	µA	
OUTPUT LED STRING SHORT-CIRCUIT						
Gain for Short-Circuit Comparator	G_{SC}	1.8	2	2.4	—	
Voltage at IREF Pin to Disable the Short-Circuit Comparator	$V_{DISABLE}$	1.19	1.25	1.31	V	PWMD = AV_{DD}, V_{FDBK} = 3.2V, FLT is HIGH.
Minimum Output Voltage of the Gain Stage	V_{OMIN}	0.14	0.20	0.30	V	IREF = GND (**Note 1**)
Propagation Time for Short-Circuit Detection	$t_{PD,OFF}$	—	—	250	ns	PWMD = AV_{DD}, V_{IREF} = 400 mV, V_{FDBK} step from 0 mV to 900 mV, FLT goes from high to low, No capacitance at FLT pin
Fault Output Rise Time	$t_{FAULT,RISE}$	—	—	500	ns	
Fault Output Fall Time	$t_{FAULT,FALL}$	—	—	300	ns	
Blanking Time	$t_{BLANK,SC}$	400	—	800	ns	(**Note 1**)

Note 1: The specifications which apply over the full operating ambient temperature range at –40°C < T_A < +125°C are guaranteed by design and characterization.

2: For design guidance only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
TEMPERATURE RANGES						
Operating Ambient Temperature	T_A	–40	—	+125	°C	
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Storage Temperature	Ts	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
16-lead SOIC	θ_{JA}	—	83	—	°C/W	

2.0 PIN DESCRIPTION

Table 2-1 shows the pin description details of HV9963.
Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN DESCRIPTION TABLE

Pin Number	Pin Name	Description
1	V_{IN}	This pin is the input of a 40V high-voltage regulator, and should not be left unconnected. If a voltage at PV_{DD} is being applied from an external power supply, the V_{IN} and PV_{DD} pins should be shorted.
2	PV_{DD}	This pin is a regulated 10V supply for the two gate drivers, FLT and GATE. It must be bypassed with a low ESR capacitor to GND (at least 1 µF).
3	GATE	This is the GATE driver output for the switching FET.
4	GND	This is the ground return for the entire low-power analog internal circuitry as well as gate drivers. This pin must be connected to the return path from the input.
5	CS	This pin is used to sense the source current of the external power FET. It includes a built-in 100 ns (minimum) blanking time.
6	HCP	This pin provides the hiccup timer in case of a fault. A capacitor at this pin programs the hiccup time.
7	RT	This pin sets the frequency of the power circuit. A resistor between RT and GND will program the circuit in Constant Frequency mode. The switching frequency is synchronized to the PWMD input. The oscillator will turn on once PWMD goes high.
8	SYNC	This I/O pin may be connected to the SYNC pin of other HV9963 circuits and will cause the oscillators to lock to the highest frequency oscillator.
9	SS	This pin is used to provide soft start upon turn-on of the IC. A capacitor at this pin programs the soft start time.
10	AV_{DD}	This is a power supply pin for all internal control circuits. This voltage is also used as reference voltage both internally and externally. It must be bypassed with a low ESR capacitor to GND (at least 0.1 µF).
11	FLT	This pin is used to drive an external disconnect FET which disconnects the load from the circuit during a Fault condition or during PWM dimming to achieve a very high dimming ratio.
12	OVP	This pin provides the overvoltage protection for the converter. When the voltage at this pin exceeds 1.25V, the GATE output of the HV9963 is turned off and FLT goes low. The hiccup timer starts when the voltage at the pin goes below 1.125V. Upon completion of the hiccup timing, the IC attempts to restart.
13	PWMD	When this pin is pulled to GND (or left open), switching of the HV9963 is disabled. When an external TTL high level is applied to it, switching will resume.
14	COMP	Stable closed-loop control can be accomplished by connecting a compensation network between COMP and GND.
15	IREF	The voltage at this pin sets the output current level. The output current reference voltage can be set using a resistor divider from the AV_{DD} pin. Connecting a voltage greater than 1.25V at this pin will disable the short-circuit comparator.
16	FDBK	This pin provides output current feedback voltage to the HV9963 using a current sense resistor.

3.0 DETAILED DESCRIPTION

3.1 Power Topology

The HV9963 is a Switch-mode LED driver designed to control a buck, boost, or SEPIC converter in a Constant Frequency mode. The IC includes internal linear regulators, which enable it to operate at input voltages from 9V to 40V. The IC includes features typically required for LED drivers like open LED protection, output LED string short-circuit protection, linear and PWM dimming, and accurate LED current control. It also includes logic to enable enhanced PWM dimming, which allows dimming ratios in excess of 5000:1.

3.2 Power Supply to the IC (V_{IN}, PV_{DD}, and AV_{DD})

The HV9963 can be powered directly from its V_{IN} pin that takes a voltage of up to 40V. There are two linear regulators within the HV9963—a 10V linear regulator (PV_{DD}), which is used for the two FET drivers, and a 5V linear regulator (AV_{DD}), which supplies power to the rest of the control logic. The IC also has a built-in undervoltage lockout which shuts off the IC if the voltage at either V_{DD} pin falls below its UVLO lower threshold. Both V_{DD} pins must be bypassed by a low-ESR capacitor (≥0.1 µF) for proper operation.

The input current drawn from the external power supply or V_{IN} pin is the sum of the 1.5 mA (maximum) current drawn by the all the internal circuitry and the current drawn by the GATE drivers, which in turn depends on the switching frequencies and the GATE charges of the external FETs. See Equation 3-1:

EQUATION 3-1:

$$I_{IN} = 1.5mA + (Q_{g1} \bullet f_S) + (Q_{g2} \bullet f_{PWMD})$$

In the above equation, f_S is the switching frequency of the converter. f_{PWMD} is the frequency of the applied PWM dimming signal. Q_{g1} is the gate charge of the external boost FET, and Q_{g2} is the gate charge of the disconnect FET. (Both gate charges can be obtained from the FET data sheets.)

The AV_{DD} pin can also be used as a reference voltage to set the LED current using a resistor divider to the IREF pin.

3.3 Oscillator (RT)

The switching frequency of the converter is set by an on-chip oscillator with a resistor connected between RT pin and GND pin. The resistor value can be determined as calculated in Equation 3-2:

EQUATION 3-2:

$$R_T \approx \left(\frac{1}{43pF \bullet f_S}\right) - 322\Omega$$

The oscillator is also timed to the PWM dimming signal to improve the PWM dimming performance. The oscillator is turned off when PWMD is low. It is enabled when PWMD goes high.

3.4 Synchronization (SYNC)

The SYNC pin is an input/output (I/O) port to a fault-tolerant peer-to-peer and/or master clock synchronization circuit. For synchronization, the SYNC pins of multiple HV9963-based converters can be connected together and may also be attached to the open drain output or the buffered output of a master clock. When connected in this manner, the oscillators will lock to the device with the highest operating frequency. When synchronizing multiple ICs, it is recommended that the same timing resistor value (corresponding the switching frequency) be used in all the HV9963 circuits.

On rare occasions, given the length of the connecting lines for the SYNC pins, a resistor between SYNC and GND may be required to damp any ringing due to parasitic capacitance. It is recommended that the resistor chosen be greater than 300 kΩ.

When synchronized in this manner, a permanent High or Low condition on the SYNC pin will result in a loss of synchronization, but the HV9963-based converters will continue to operate at their individually set operating frequencies. Since loss of synchronization will not result in total system failure, the SYNC pin is considered fault tolerant.

3.5 Current Sense (CS)

The current sense input is used to sense the source current of the switching FET. The CS input of the HV9963 includes a built-in 100 ns (minimum) blanking time to prevent spurious turn-off due to the initial current spike when the FET turns on.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 12 (11R:1R). This voltage is used as the reference for the current sense comparator. Since the maximum voltage of the COMP pin is AV_{DD}–0.7V, this voltage determines the maximum reference current for the current sense comparator and thus the maximum inductor current.

The switch current sense resistor R_{CS} should be chosen so that the input inductor current is limited to below the saturation current level of the input inductor. For Discontinuous Conduction mode, no slope compensation is necessary. In this case, the switch current sense resistor is computed as shown in Equation 3-3:

EQUATION 3-3:

$$R_{CS} = \frac{AV_{DD} - 0.7V}{12 \bullet I_{SAT}}$$

Where I_{SAT} is the maximum desired peak inductor current

For Continuous Conduction mode converters operating in the Constant Frequency mode, slope compensation becomes necessary to ensure the stability of the Peak Current mode controller if the operating duty cycle is greater than 50%. This factor must also be accounted for when determining the R_{CS}. See **Section 3.6 "Slope Compensation"**.

3.6 Slope Compensation

Choosing a slope compensation that is one-half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

Slope compensation in the HV9963 can be programmed by one external capacitor C_{SC} between the CS pin and resistor R_{CS}. (See Figure 3-1.) A current proportional to the switching frequency is sourced out of the CS pin. (See Equation 3-4.)

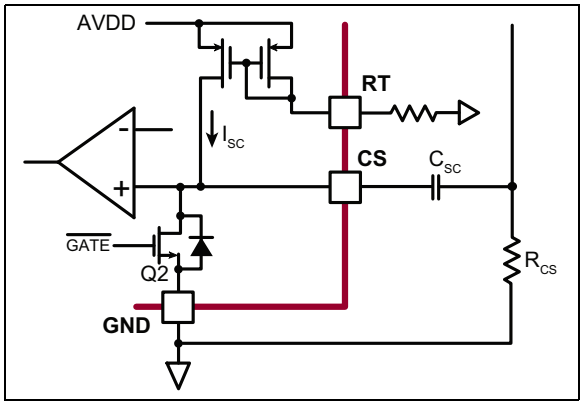


FIGURE 3-1: *Slope Compensation Circuit.*

EQUATION 3-4:

$$I_{SC} = 2\mu A \bullet \frac{f_S}{100kHz}$$

This current flows into the capacitor C_{SC} and produces a ramp voltage across it. The voltage at the CS pin is then the sum of the voltage across the capacitor and the voltage across the current sense resistor, with the voltage across the capacitor providing the required slope compensation. When the GATE turns low, an internal pull-down FET discharges the capacitor.

Assuming a down slope current slew rate of DS (A/µs) for the inductor current, the current sense resistor can be computed as illustrated in Equation 3-5:

EQUATION 3-5:

$$R_{CS} = \frac{AV_{DD} - 0.7V}{12} \bullet \frac{1}{\frac{DS \bullet 10^6 \bullet 0.93}{2 \bullet f_S} + I_{SAT}}$$

The slope compensation capacitor is chosen to provide the necessary amount of slope compensation required to maintain stability. Refer to Equation 3-6.

EQUATION 3-6:

$$C_{SC} = \frac{I_{SC}}{\frac{DS}{2} \bullet 10^6 \bullet R_{CS}}$$

Note that sometimes excessive stray inductance in the current sense path may cause the slope compensation circuit to mistrigger. This section describes the cause of the problem and the solution.

Figure 3-2 shows the detailed slope compensation circuit with a parasitic inductance L_P between the ground of the boost converter power stage and the ground of the HV9963. Also shown is the drain capacitance of the boost FET Q1, which is the total capacitance at the drain node.

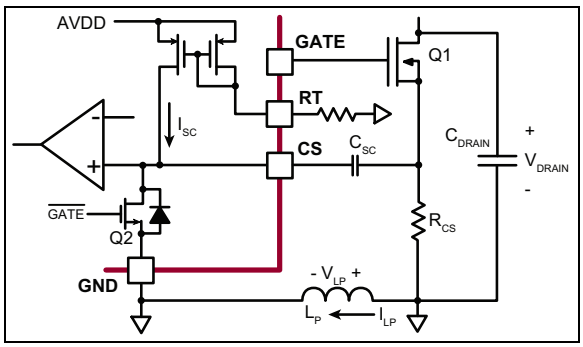


FIGURE 3-2: *Slope Compensation Circuit with Parasitics.*

When FET Q1 is switched off, the internal discharge FET Q2 is turned on, and the capacitor C_{SC} is discharged. Also, C_{DRAIN} is charged to the output voltage V_O. When the FET Q1 is turned on, the drain node of the FET is pulled to ground (Q2 is turned off just before Q1 is turned on). This causes the drain capacitance to discharge through the FET Q1, resulting in a current spike as shown in Figure 3-3. This current spike causes a voltage to develop across the parasitic inductance. As long as the current is increasing through the inductance, the voltage developed across the parasitic inductance is successfully blocked by the body diode of Q2. However, during the falling edge of the current spike, the voltage across the parasitic inductance causes the body diode to become forward biased. This conduction path through the body diode of

Q2 causes pre-charge of C_{SC}. The pre-charge voltage can be fairly high since the current's rate of fall is very large.

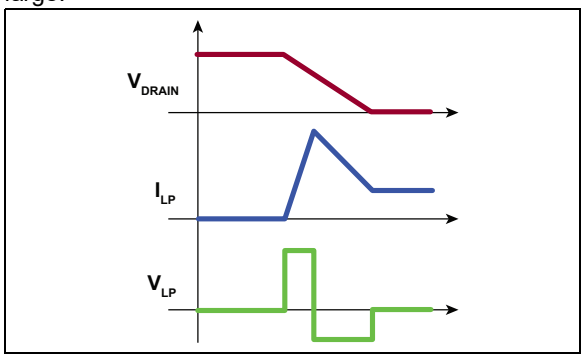


FIGURE 3-3: *Waveforms during Turn-on.*

For example, a typical current spike usually lasts about 100 ns. Assuming a 3A peak current (this is the typical value of the saturation current of the FET that can be much higher) and equal distribution between the rise and fall times, a 10 nH parasitic inductance causes a pre-charge voltage, which is calculated in Equation 3-7.

EQUATION 3-7:

$$V_{PRE-CHARGE} = 10nH \bullet \frac{3A}{50ns} = 600mV$$

As seen in the equation above, a very conservative estimate of the pre-charge voltage is already larger than the Steady state peak current sense voltage and will cause the converter to falsely trip.

To prevent this, a resistor (typically 500Ω to 800Ω) can be added in series with the capacitor C_{SC} as shown in Figure 3-4. This resistor limits the charging current from the parasitic inductance into the capacitor. However, the resistor will also slow down the discharge of the capacitor during the FET Q1 off-time, so the switching frequency and the slope compensation capacitor will limit the maximum external resistance. Refer to Equation 3-8.

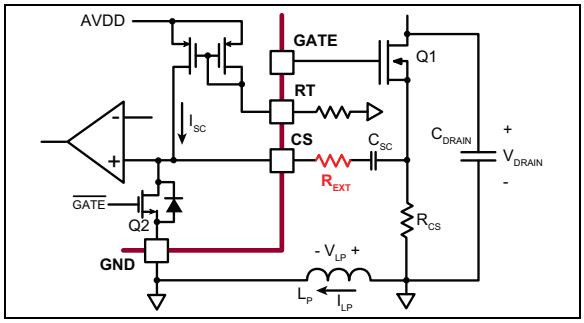


FIGURE 3-4: *Modified Slope Compensation Circuit.*

EQUATION 3-8:

$$R_{EXT,MAX} = \left(\frac{1}{3}\right) \bullet \left(\frac{0.07}{f_S}\right) \bullet \left(\frac{1}{C_{SC}}\right) - 600\Omega$$

3.7 FLT Output

The FLT pin is used to drive a disconnect FET when HV9963 is configured as boost and SEPIC converters. In the case of boost converters, when there is a short-circuit fault at the output LED string, there is a direct path from the input source to ground which can cause high currents to flow. The disconnect switch is used to interrupt this path and prevent damage to the converter.

The disconnect switch also helps to disconnect the output filter capacitors for the boost and SEPIC converters from the LED load during PWM dimming. The switch also enables a very high PWM dimming ratio.

3.8 Control of the LED Current (IREF, FDBK, and COMP)

The LED current in the HV9963 is controlled in a closed-loop manner. The current reference which sets the LED current at the IREF pin is set using a resistor divider from the AVDD pin. It can also be set externally with a low-voltage source. This reference voltage is compared to the voltage from the LED current sense resistor R_S at the FDBK pin by a transconductance amplifier.

The LED current at full brightness is set with Equation 3-9.

EQUATION 3-9:

$$I_O = \frac{V_{IREF}}{R_S}$$

HV9963 includes a 1 MHz transconductance operational amplifier with tristate output, which is used to close the feedback loops and provide accurate current control. The compensation network is connected to the COMP pin.

The output of the op-amp is buffered and connected to the current sense comparator using a 11R:1R resistor divider.

The output of the op-amp is also controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the op-amp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge and the COMP pin voltage unchanged when the PWMD signal has turned off the gate drive. When the

PWMD is changed from low back to high again, the voltage on the integrating capacitor will force the converter into a Steady state almost instantaneously.

Note:	The absolute maximum voltage rating of the IREF pin is 3.5V, and the voltage applied at this pin should not exceed this rating.

3.9 Soft Start (SS)

Soft start of the LED current can be achieved by connecting a capacitor at the SS pin. The rate of rise of SS pin voltage limits the LED current's rate of rise.

Upon start-up, the capacitance at the COMP network is being charged by the 200 µA sourcing current of the transconductance amplifier. Without the soft start function, this larger current would cause the COMP voltage to increase faster than the boost converter's response time, causing overshoots in the LED current during start-up.

The SS pin is used to prevent these LED current overshoots by limiting the COMP pin's voltage rise rate. A capacitor at the soft start pin programs the voltage rise rate at the pin. The SS pin holds the COMP pin voltage to 1V above the SS pin voltage and thereby controls the COMP pin's voltage rise rate. The COMP pin is released once the COMP voltage reaches its Steady state.

When the steady state voltage at the COMP pin voltage ($V_{COMP(SS)}$) and the desired rise time of the LED current ($t_{RISE,ILED}$) have been determined, the capacitance required at the SS pin can be computed as specified in Equation 3-10:

EQUATION 3-10:

$$C_{SS} = \frac{11\mu A \bullet t_{RISE,\,ILED}}{V_{COMP(SS)} - 1V}$$

3.10 Linear Dimming

Linear dimming can be performed in the HV9963 by varying the voltages at the IREF pin. Note that since the HV9963 is a Peak Current mode controller, it has a minimum on time for the GATE output. This minimum on time will prevent the converter from completely turning off even when the IREF pin is pulled to GND. Thus, linear dimming cannot accomplish true zero-LED current for the HV9963. To get zero-LED current, PWM dimming has to be used.

Due to the offset voltage of the short-circuit comparator as well as the non-linearity of the X2 gain stage, pulling the IREF pin very close to GND might trigger the internal short-circuit comparator and shut down the IC. To overcome this, the output of the gain stage is limited to 140 mV (minimum), allowing the IREF pin to be pulled all the way to 0V without triggering the short-circuit comparator.

3.11 PWM Dimming (PWMD)

PWM dimming in the HV9963 can be accomplished using a TTL-compatible square wave voltage signal source at the PWMD pin.

The HV9963 has an enhanced PWM dimming capability, which allows PWM dimming to widths less than one switching cycle with no drop in the LED current.

The enhanced PWM dimming performance of the HV9963 can be best explained by considering typical boost converter circuits without this functionality. When the PWM dimming pulse becomes very small (less than one switching cycle for a DCM design or less than five switching cycles for a CCM design), the boost converter is turned off before the input current can reach its Steady state value. This causes the input power to drop, which is manifested in the output as a drop in the LED current. Refer to Figure 3-5 and Figure 3-6 for a CCM design.

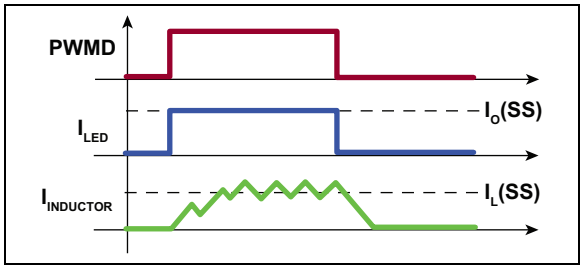


FIGURE 3-5: *PWM Dimming with Dimming On-Time far greater than One Switching Time Period.*

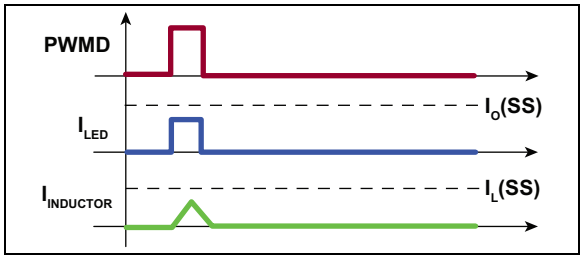


FIGURE 3-6: *PWM Dimming with Dimming On-Time equal to One Switching Time Period.*

In the above figures, I_O(SS) and I_L(SS) refer to the steady state values at PWMD duty = 100% for the output current and inductor current, respectively. As can be seen in Figure 3-6, the inductor current does not rise enough to trip the CS comparator. This causes the closed-loop amplifier to lose control of the LED current and COMP voltage rises to AV_{DD}.

In the HV9963, however, this problem can be overcome by keeping the boost converter on, even though PWMD has gone down to zero. The boost converter may remain turned on until the inductor

current reaches the threshold in Steady state at 100% PWM dimming duty cycle. This will ensure that enough power is delivered to the output. Thus, the amplifier still has control over the LED current, and the LED current will be in regulation as shown in Figure 3-7.

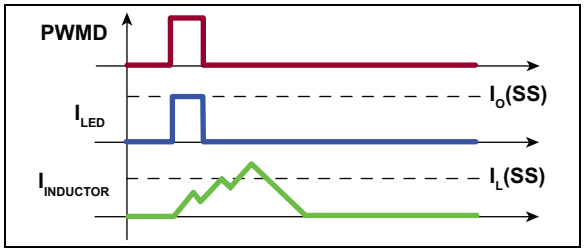


***FIGURE 3-7:** PWM Dimming with Dimming On-Time equal to One Switching Time Period with the HV9963.*

When the PWM signal is high, the GATE and FLT pins are enabled and the output of the transconductance op-amp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The FLT pin goes low, turning off the disconnect switch. However, the GATE pin is kept enabled and the switching FET is kept switching until the switch current sensed by the current sense resistor R_{CS} at the CS pin reaches the Steady state threshold at the undimmed full brightness LED current output.

Note: Disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The chosen filter capacitor should be large enough, so it can absorb the inductor energy without any significant change of the voltage across it. If the capacitor voltage change is significant, it would cause a turn-on spike in the inductor current when PWMD goes high.

3.12 Fault Conditions and Hiccup Timer (OVP, HCP)

The HV9963 is a robust controller which can protect the LEDs and the LED driver in case of Fault conditions. The HV9963 includes both open LED protection and output LED string short-circuit protection. In both cases, the HV9963 shuts down and attempts to restart after a hiccup time. The hiccup time is programmed by the capacitor at the HCP pin.

When a Fault condition is detected, both GATE and FLT outputs are disabled and the COMP, SS, and HCP pins are pulled to GND. Once the voltage at the HCP pin falls below 0.1V, and the Fault condition has disappeared, the capacitor at the HCP pin is released and is charged slowly by a 11 µA current source. Once the capacitor is charged to 2.1V, the COMP and SS pins are released and the GATE and FLT pins are allowed to turn on. Then, the converter will go into a Soft-start mode, ensuring a smooth recovery for the LED current.

3.13 Hiccup Timer (HCP)

The value of the capacitor required for a given hiccup time is calculated as seen in Equation 3-11 below:

EQUATION 3-11:

$$C_{HCP} = \frac{11\mu A \bullet t_{HICCUP}}{2V}$$

3.14 LED String Short-Circuit Protection

When a LED String Short-circuit condition is detected (output current becomes higher than twice the Steady state current), the GATE and FLT outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the Short-circuit condition disappears. At this time, the hiccup timer is started. Once the timing is complete, the converter attempts to restart. If the Fault condition still persists, the converter shuts down and goes through the cycle again. If the Fault condition is cleared (due to a momentary output short) the converter will start regulating the output current normally. This allows the LED driver to recover from accidental shorts without having to reset the IC.

During Short-circuit conditions, there are two factors that determine the hiccup time. The first factor is the time t_{COMP} required to discharge the compensation capacitor. The COMP discharge time t_{COMP} is calculated as shown in Equation 3-12.

EQUATION 3-12:

For Type 1 compensation network which is a single capacitor C_C at the COMP pin,

$$t_{COMP} = 3 \bullet 5000\Omega \bullet C_C$$

For Type 2 compensation network which is a series combination of R_Z and C_Z in parallel with C_C at the COMP pin,

$$t_{COMP} = 3 \bullet R_Z \bullet C_Z$$

The second factor is the time t_{IND} required for the inductor to discharge completely after the Short-circuit condition has been cleared. The inductor discharge time t_{IND} is computed as illustrated in Equation 3-13.

EQUATION 3-13:

$$t_{IND} = \frac{\Pi}{4}\sqrt{L \bullet C_O}$$

Where L and C_O are input inductor and output capacitor of the power stage, respectively

The hiccup time is then chosen as shown in Equation 3-14.

EQUATION 3-14:

$$t_{HICCUP} > max(t_{COMP}, t_{IND})$$

Note that the power rating of the LED current sense resistor has to be chosen properly if it has to survive a persistent Fault condition. The power rating can be determined using Equation 3-15.

EQUATION 3-15:

$$P_{RS} \geq \frac{I^2_{SAT} \bullet R_S \bullet (t_{FAULT} + t_{PD,OFF})}{t_{HICCUP}}$$

Where I_{SAT} is the saturation current of the disconnect FET. In the case of HV9963, t_{FAULT} + $t_{PD,OFF}$ is 550 ns (maximum)

3.15 False Triggering of the Short-Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string might cause a spike in the output current when the disconnect FET is turned on. If this spike is detected by the short-circuit comparator, it will cause the IC to falsely detect an Overcurrent condition and shut down.

To prevent these false triggers in the HV9963, there is a built-in 600 ns blanking network for the short-circuit comparator. This blanking network is activated when the PWMD input goes high. Thus, the short-circuit comparator will not see the spike in the LED current during the PWM dimming turn-on transition. Once the blanking timer is completed, the short-circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short-circuit will depend on the condition of the PWMD input.

If the output short-circuit exists before the PWM dimming signal goes high, the total detection time is determined as demonstrated in Equation 3-16.

EQUATION 3-16:

$$t_{DETECT1} = t_{BLANK,SC} + t_{PD,OFF} \approx 1050ns(max)$$

If the short-circuit occurs when the PWM dimming signal is already high, the time to detect is computed as shown in Equation 3-17.

EQUATION 3-17:

$$t_{DETECT1} = t_{PD,OFF} \approx 250ns(max)$$

3.16 Overvoltage Protection

The HV9963 provides hysteretic overvoltage protection allowing the IC to recover in case the LED load is disconnected momentarily.

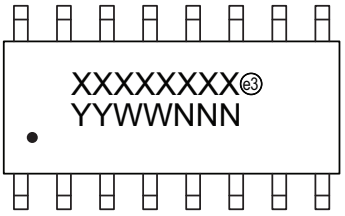
When the load is disconnected in a boost converter, the output voltage rises as the output capacitor starts charging. When the output voltage reaches the OVP rising threshold, the HV9963 detects an Overvoltage condition and turns off the converter. The converter is turned back on only when the output voltage falls below the falling OVP threshold, which is 10% lower than the rising threshold. This time is mostly dictated by the R-C time constant of the output capacitor C_O and the resistor network used to sense overvoltage (R_{OVP1} + R_{OVP2}). In case of a persistent Open Circuit condition, this cycle keeps repeating, maintaining the output voltage within a 10% band of the OVP thresholds.

In most designs, the lower threshold voltage of the overvoltage protection—10% below $V_{OVP,RISING}$ at which the HV9963 attempts to restart—will be more than the LED string voltage. Thus, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED string voltage will cause a spike in the output current. This causes a short-circuit to be detected, and the HV9963 will trigger short-circuit protection. This behavior continues until the output voltage becomes lower than the LED string voltage. At which point, no Fault will be detected and normal operation of the circuit will commence.

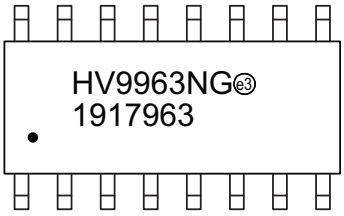
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

16-lead SOIC



Example

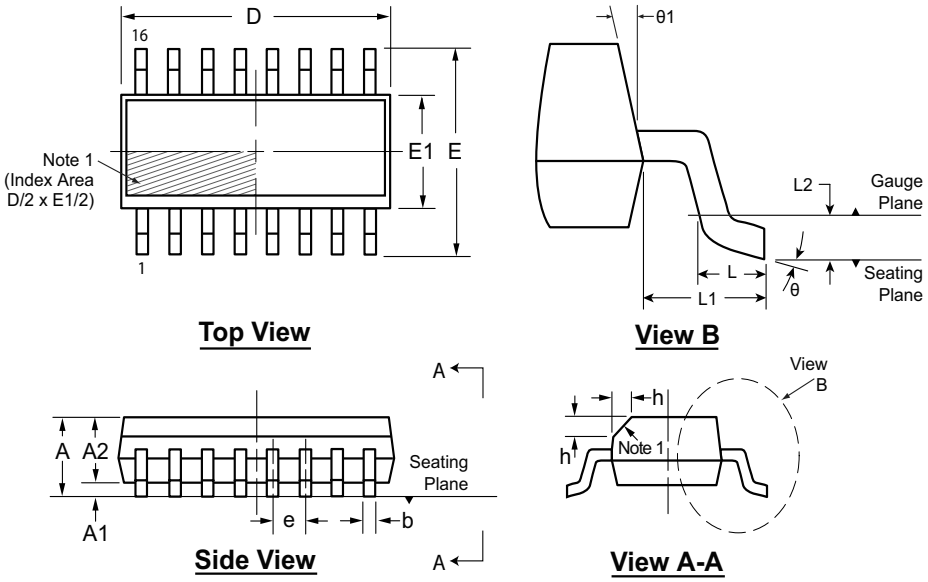


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2019)

- Converted Supertex Doc# DSFP-HV9963 to Microchip DS20005594A
- Changed the packaging quantity of the M901 media type from 1000/Reel to 2600/Reel
- Changed the packaging quantity of M934 media type from 2500/Reel to 2600/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9963	=	Closed-loop LED Driver with Enhanced PWM Dimming
Package:	NG	=	16-lead SOIC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	45/Tube for an NG Package
	M901	=	2600/Reel for an NG Package
	M934	=	2600/Reel for an NG Package

Note: For media types M901 and M934, the base quantity for tape and reel was standardized to 2600/reel. Both options will result in delivery of the same number of parts/reel.

Examples:

a) HV9963NG-G: Closed-loop LED Driver with Enhanced PWM Dimming, 16-lead SOIC Package, 45/Tube

b) HV9963NG-G-M901: Closed-loop LED Driver with Enhanced PWM Dimming, 16-lead SOIC Package, 2600/Reel

c) HV9963NG-G-M934: Closed-loop LED Driver with Enhanced PWM Dimming, 16-lead SOIC Package, 2600/Reel

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