

## Low-Noise Dimmable EL Lamp Driver

### Features

- Adjustable Output Regulation for Dimming
- 220 V<sub>PP</sub> Output Voltage for Higher Brightness
- Single-cell Lithium Ion-compatible
- 150 nA Shutdown Current
- Separately Adjustable Lamp and Converter Frequencies
- Split Supply Capability

### Applications

- Mobile Cellular Phone Keypads
- Personal Digital Assistant (PDA)
- Handheld Wireless Communication Products
- Global Positioning Systems (GPS)

### General Description

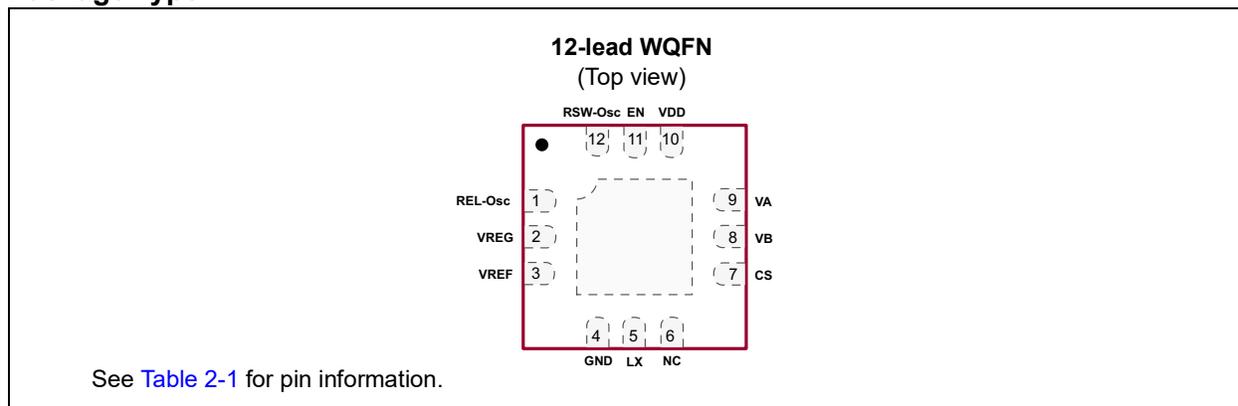
The HV860 is a high-voltage driver designed for driving Electroluminescent (EL) lamps of up to 5 in<sup>2</sup>. The input supply voltage range is from 2.5V to 4.5V. The device uses a single inductor and a minimum number of passive components. By using an internal voltage reference, the regulated output voltage is at a nominal voltage of 110V. The EL lamp will therefore see ±110V. An enable pin (EN) is available to turn on and turn off the device via a logic signal.

The HV860 has two internal oscillators, a switching MOSFET, and a high-voltage EL lamp driver H-bridge. The frequency for the switching MOSFET is set by an external resistor connected between the RSW-Osc pin and the supply pin, VDD. The EL lamp driver frequency is set by an external resistor connected between REL-Osc pin and VDD pin. An external inductor is connected between the L<sub>X</sub> and VDD pins or VIN for split supply applications. A 3 nF capacitor is connected between C<sub>S</sub> and ground. The EL lamp is connected between VA and VB.

The switching MOSFET charges the external inductor and discharges it into the capacitor at C<sub>S</sub>. The voltage at C<sub>S</sub> will start to increase. Once the voltage at C<sub>S</sub> reaches a nominal value of 110V, the switching MOSFET is turned off to conserve power. The outputs VA and VB are configured as an H-bridge and are switching in opposite states to achieve ±110V across the EL lamp.

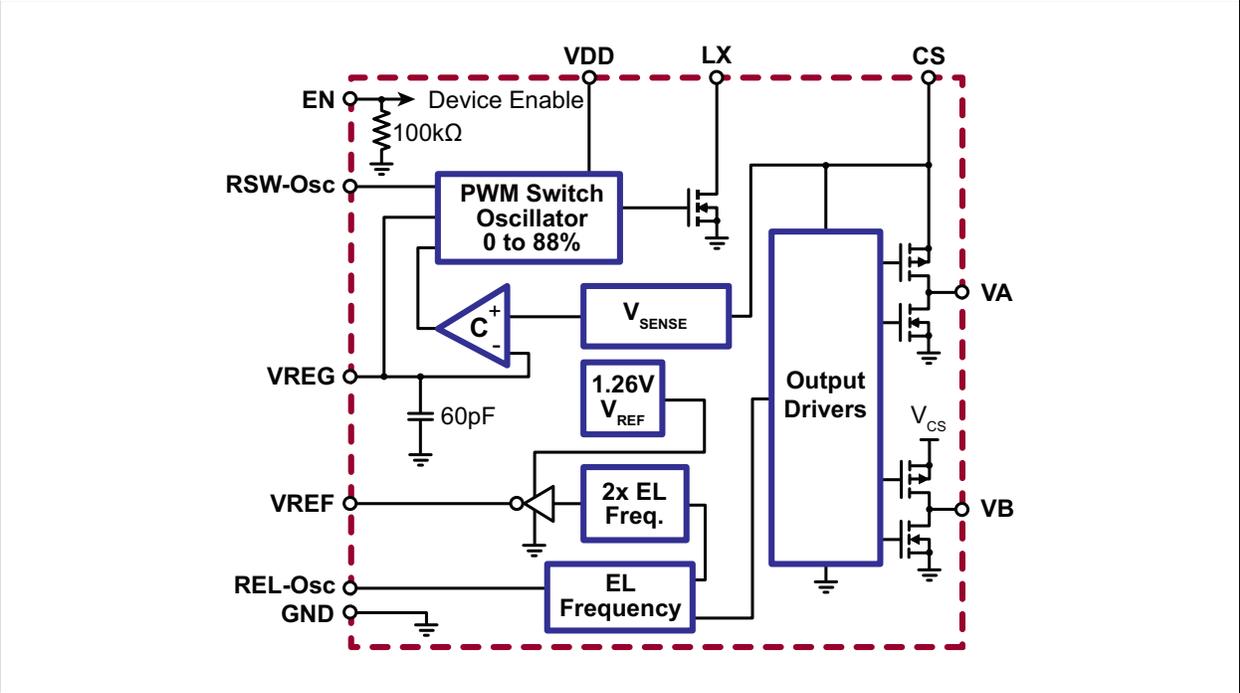
EL lamp dimming can be accomplished by changing the input voltage to the VREG pin. The VREG pin allows an external voltage source to control the V<sub>CS</sub> amplitude. The V<sub>CS</sub> voltage is approximately 87 times the voltage seen on V<sub>REG</sub>.

### Package Type

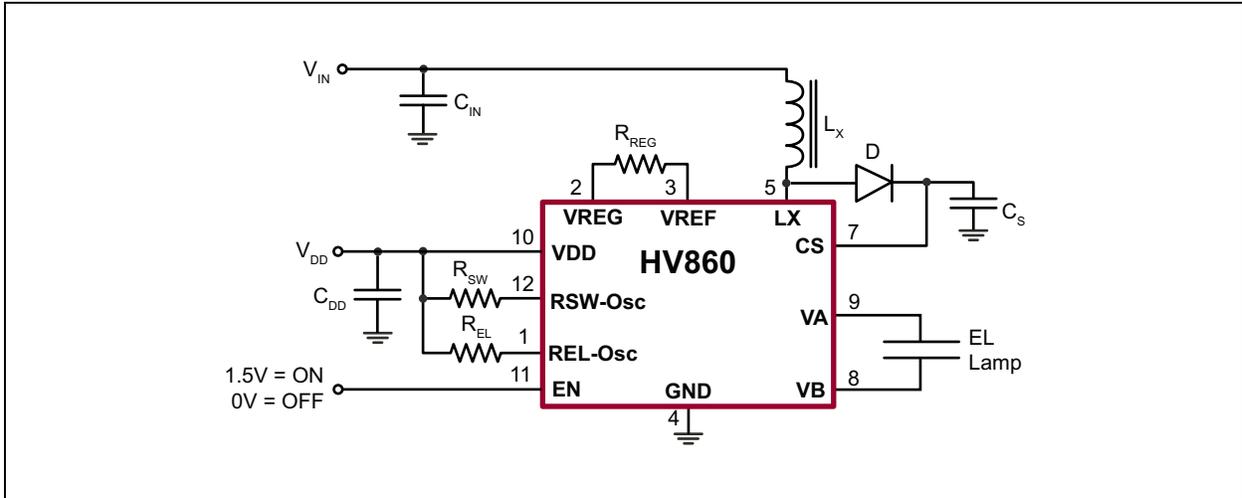


# HV860

## Functional Block Diagram



## Typical Application Circuit



# HV860

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings<sup>(†)</sup>

Supply Voltage, $V_{DD}$ .....	-0.5V to 6V
Operating Ambient Temperature Range, $T_A$ .....	-40°C to +85°C
Storage Temperature Range, $T_S$ .....	-65°C to +150°C
Output Voltage, $V_{CS}$ .....	-0.5V to +120V
External Input Voltage, $V_{REG}$ .....	1.33V
Power Dissipation:	
12-lead WQFN (3 X 3) .....	1.6W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Voltage	$V_{DD}$	2.5	—	4.5	V	
Switching Frequency	$f_{SW}$	40	—	200	KHz	
EL Lamp Frequency	$f_{EL}$	150	—	500	Hz	
EL Lamp Capacitance Load	$C_{LOAD}$	0	—	20	nF	
Operating Ambient Temperature Range	$T_A$	-40	—	+85	°C	

### ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^\circ\text{C}$ unless otherwise specified.						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
On-resistance of Switching Transistor	$R_{DS(ON)}$	—	—	6	$\Omega$	$I = 100\text{ mA}$
Maximum Output Regulation Voltage	$V_{CS}$	90	—	120	V	$V_{DD} = 2.5\text{V to }4.5\text{V}$
Output Regulation Voltage	$V_{CS}$	—	95	—	V	$V_{DD} = 2.5\text{V to }4.5\text{V},$ $V_{REG} = 1.092\text{V}$
		—	75	—		$V_{DD} = 2.5\text{V to }4.5\text{V},$ $V_{REG} = 0.862\text{V}$
		—	55	—		$V_{DD} = 2.5\text{V to }4.5\text{V},$ $V_{REG} = 0.632\text{V}$
External Input Voltage Range	$V_{REG}$	0	—	1.33	V	$V_{DD} = 2.5\text{V to }4.5\text{V}$
$V_{REF}$ Output High Voltage	$V_{REFH}$	1.18	1.26	1.33	V	$V_{DD} = 2.5\text{V to }4.5\text{V}$
Quiescent $V_{DD}$ Supply Current	$I_{DDQ}$	—	—	150	nA	EN = Low
Input Current going into the $V_{DD}$ Pin	$I_{DD}$	—	—	250	$\mu\text{A}$	$V_{DD} = 2.5\text{V to }4.5\text{V},$ $R_{EL} = 2\text{ M}\Omega, R_{SW} = 1\text{ M}\Omega$
Input Current including Inductor Current	$I_{IN}$	—	16	30	mA	$V_{IN} = 3\text{V}$ See <a href="#">Figure 3-1</a> .
Quiescent $V_{IN}$ Supply Current	$I_{INQ}$	—	—	200	nA	$V_{IN} = 4.2\text{V}, \text{EN} = \text{Low}$ See <a href="#">Figure 3-1</a> .
EL Lamp Frequency	$f_{EL}$	160	200	240	Hz	$R_{EL} = 2\text{ M}\Omega$
Switching Transistor Frequency	$f_{SW}$	76	90	104	kHz	$R_{SW} = 1\text{ M}\Omega$
Switching Transistor Duty Cycle	D	—	—	88	%	
LOGIC INPUTS						
Enable Input Logic High Voltage	$V_{IH}$	1.5	—	$V_{DD}$	V	$V_{DD} = 2.5\text{V to }4.5\text{V}$

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications:  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Enable Input Logic Low Voltage	$V_{IL}$	0	—	0.2	V	$V_{DD} = 2.5\text{V to }4.5\text{V}$
Enable Input Logic High Current	$I_{IH}$	—	—	100	$\mu\text{A}$	$V_{IH} = V_{DD} = 2.5\text{V to }4.5\text{V}$
Enable Input Logic Low Current	$I_{IL}$	—	—	-1	$\mu\text{A}$	$V_{IL} = 0\text{V}, V_{DD} = 2.5\text{V to }4.5\text{V}$
Enable Input Capacitance	$C_{IN}$	—	—	15	pF	

## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Ambient Temperature Range	$T_A$	-40	—	+85	$^\circ\text{C}$	
Storage Temperature Range	$T_S$	-65	—	+150	$^\circ\text{C}$	
<b>PACKAGE THERMAL RESISTANCE</b>						
12-lead WQFN	$\theta_{JA}$	—	40	—	$^\circ\text{C/W}$	

# HV860

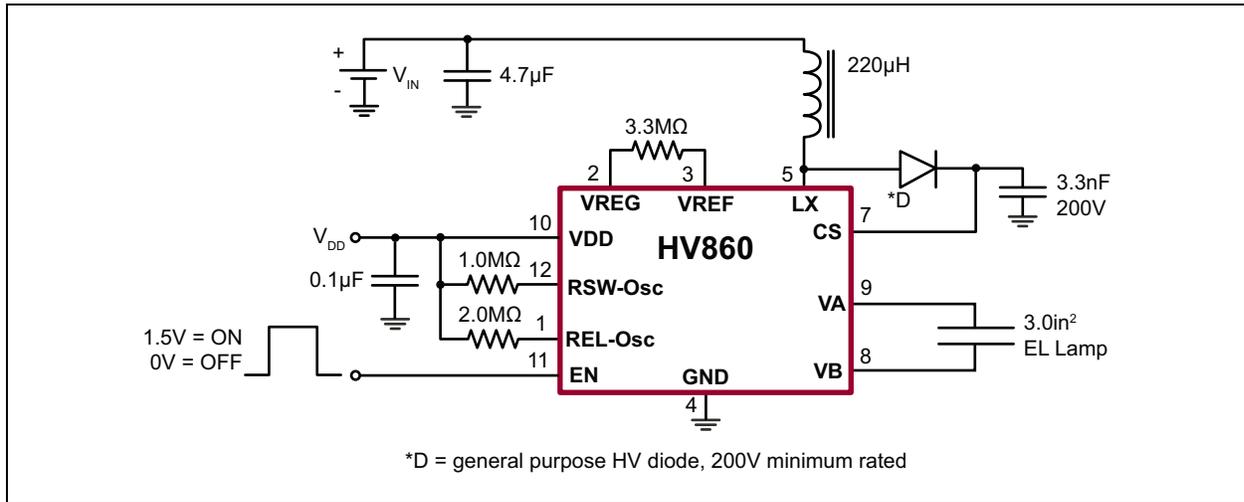
## 2.0 PIN DESCRIPTION

The details on the pins of HV860 are listed in [Table 2-1](#). Refer to [Package Type](#) for the location of pins.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	REL-Osc	External resistor from $R_{EL-Osc}$ to $V_{DD}$ sets the EL frequency. The EL frequency is inversely proportional to the external $R_{EL}$ resistor value. Reducing the resistor value by a factor of two determines an increase in the EL frequency by two.
2	VREG	Input voltage to set $V_{CS}$ regulation voltage. This pin allows an external voltage source to control the $V_{CS}$ amplitude. EL lamp dimming can be accomplished by varying the input voltage at $V_{REG}$ . The $V_{CS}$ voltage is approximately 87 times the voltage seen on $V_{REG}$ . The external resistor $R_{REG}$ , connected between $V_{REG}$ and $V_{REF}$ pins, controls the $V_{CS}$ charging rate. The charging rate is inversely proportional to the $R_{REG}$ resistor value.
3	VREF	Switched internal reference voltage
4	GND	Device ground
5	LX	Drain of internal switching MOSFET. Connection for an external inductor.  The inductor $L_X$ is used to boost the low-input voltage by inductive flyback. When the internal switch is on, the inductor is being charged. When the internal switch is off, the charge stored in the inductor will be transferred to the high-voltage capacitor, $C_S$ . The energy stored in the capacitor is transferred to the internal H-bridge, and therefore to the EL lamp. In general, smaller value inductors, which can handle more current, are more suitable to drive larger size lamps. As the inductor value decreases, the switching frequency of the inductor (controlled by $R_{SW}$ ) should be increased to avoid saturation. A 220 $\mu$ H inductor with 5.5 $\Omega$ series DC resistance is typically recommended. For inductors with the same inductance value, but with lower series DC resistance, lower $R_{SW}$ resistor value is needed to prevent high current draw and inductor saturation.
6	NC	No internal connections to the device
7	CS	High voltage-regulated output. Connection for an external high-voltage capacitor to ground.
8	VB	$V_B$ side of the EL lamp driver H-bridge. Connection for one of the EL lamp terminals.
9	VA	$V_A$ side of the EL lamp driver H-bridge. Connection for one of the EL lamp terminals.
10	VDD	Low-voltage input supply pin
11	EN	Logic input pin. Logic high will enable the device. This pin has an 100 k $\Omega$ internal pull-down resistor to GND.
12	RSW-Osc	External resistor from $R_{SW-Osc}$ to $V_{DD}$ sets the switch converter frequency. The switch converter frequency is inversely proportional to the external $R_{SW}$ resistor value. Reducing the resistor value by a factor of two will result in increasing the switch converter frequency by two.

## 3.0 APPLICATION INFORMATION

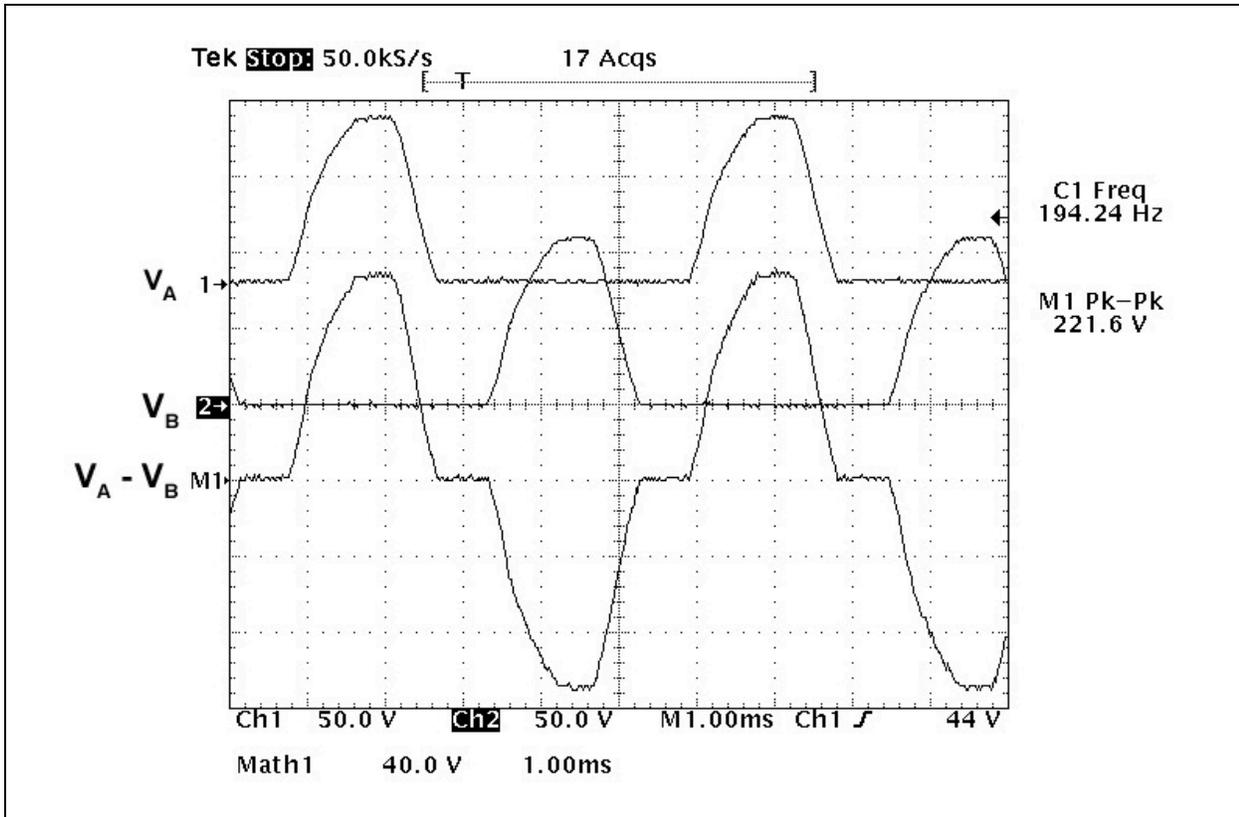


**FIGURE 3-1:** Typical Application Circuit/Test Circuit.

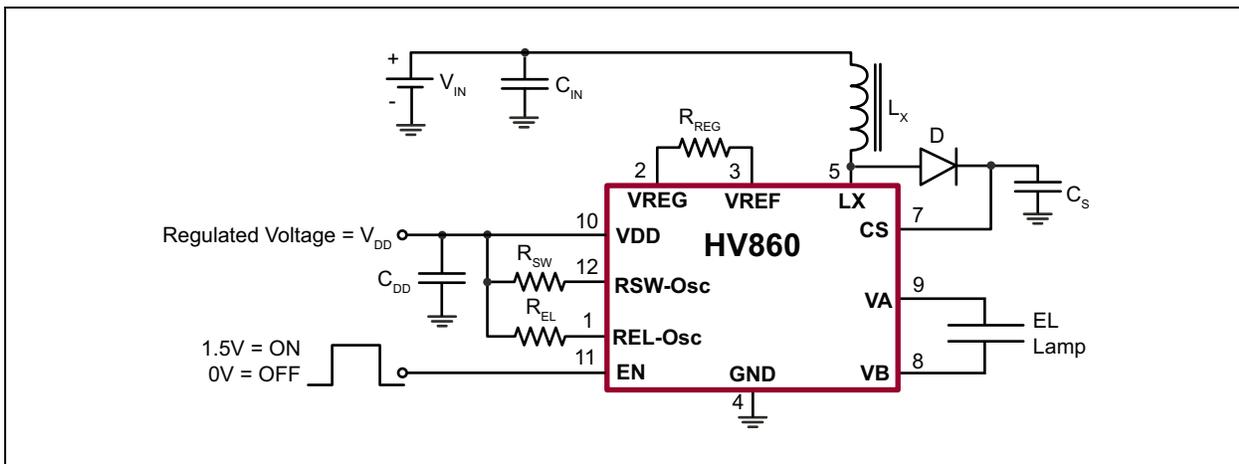
**TABLE 3-1:** TYPICAL PERFORMANCE

$V_{DD}$ (V)	Lamp Size (in <sup>2</sup> )	$V_{IN}$ (V)	$I_{IN}$ (mA)	$V_{CS}$ (V)	$f_{EL}$ (Hz)	Brightness (cd/m <sup>2</sup> )
3	3	3.3	19.42	110	194	20.32
		3.7	17.95			21.4
		4.2	16.02			21.81

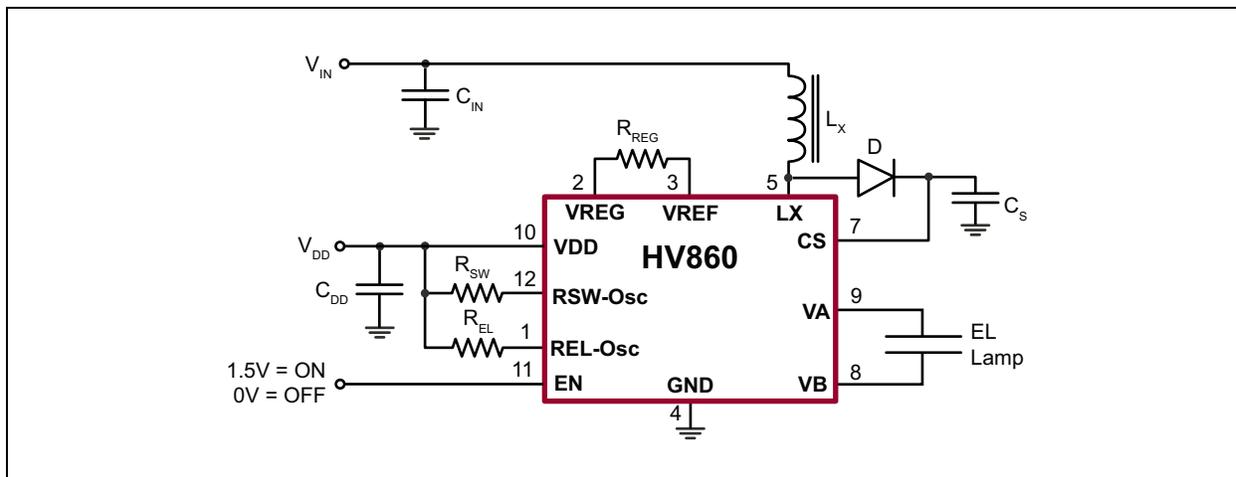
# HV860



**FIGURE 3-2:** Typical Waveform on  $V_A$ ,  $V_B$  and Differential Waveform  $V_A - V_B$ .



**FIGURE 3-3:** Split Supply and Enable/Disable Configuration.



**FIGURE 3-4:** Typical Application Circuit for Audible Noise Reduction.

### 3.1 Split Supply Configuration

The HV860 can also be used for handheld devices operating from a battery where a regulated voltage is available. This is shown in the Typical Application Circuit in [Figure 3-3](#). The regulated voltage can be used to run the internal logic of the HV860. The amount of current necessary to run the internal logic is 250  $\mu$ A (maximum value). Therefore, the regulated voltage could easily provide the current without being loaded down.

### 3.2 Enable/Disable Configuration

The HV860 can be easily enabled and disabled via a logic control signal at the EN pin as illustrated in the Typical Application Circuit in [Figure 3-3](#). The control signal can be from a microprocessor. When the microprocessor signal is high, the device is enabled. When the signal is low, it is disabled.

### 3.3 Audible Noise Reduction

When the EL lamp is lit, the EL lamp emits an audible noise. This is due to the EL lamp construction. The audible noise generated by the EL lamp can be a major problem for applications where the EL lamp is held close to the ear, such as cellular phones. The HV860 employs a proprietary circuit to help minimize the EL lamp's audible noise by using a single resistor,  $R_{REG}$ , as shown in the Typical Application Circuit for Audible Noise Reduction in [Figure 3-4](#).

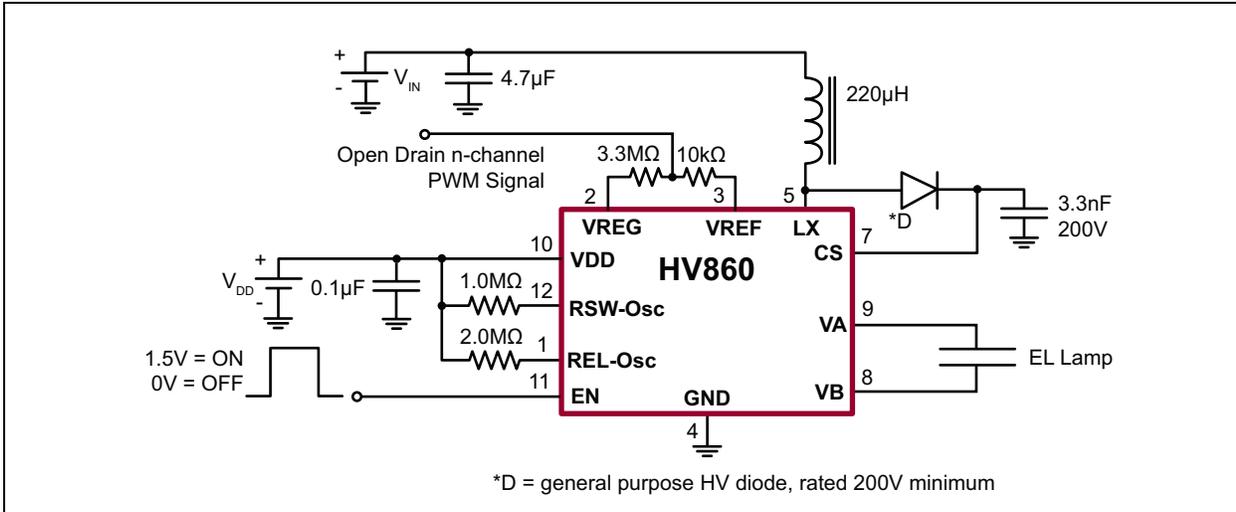
### 3.4 Minimizing EL Lamp Audible Noise

The audible noise from the EL lamp can be minimized with the proper selection of  $R_{REG}$ .  $R_{REG}$  is connected between the  $V_{REF}$  and  $V_{REG}$  pins.  $V_{REG}$  has an internal 60 pF capacitor to ground. The EL lamp noise can be minimized without much loss in brightness by setting the RC time constant to be approximately 1/12 of the EL frequency's period.

### 3.5 EL Lamp Dimming Using PWM

Reducing the voltage amplitude at the  $V_{REG}$  pin reduces the voltage on the  $C_S$  pin, which effectively reduces the peak-to-peak voltage the EL lamp sees. [Figure 3-5](#) illustrates a circuit to dim the lamp by changing the duty cycle of a PWM signal. A 10 k $\Omega$  resistor is connected in series with a 3.3 M $\Omega$  resistor. An N-channel open-drain PWM signal is used to pull the 10 k $\Omega$  resistor to ground. The effective voltage on the  $V_{REG}$  pin will be proportional to the duty cycle of the PWM signal. The PWM operating frequency can be anywhere between 20 kHz to 100 kHz.

# HV860



**FIGURE 3-5:** PWM Dimming Circuit.

## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

12-lead WQFN

Example

XXXXX
YYWW
NNN

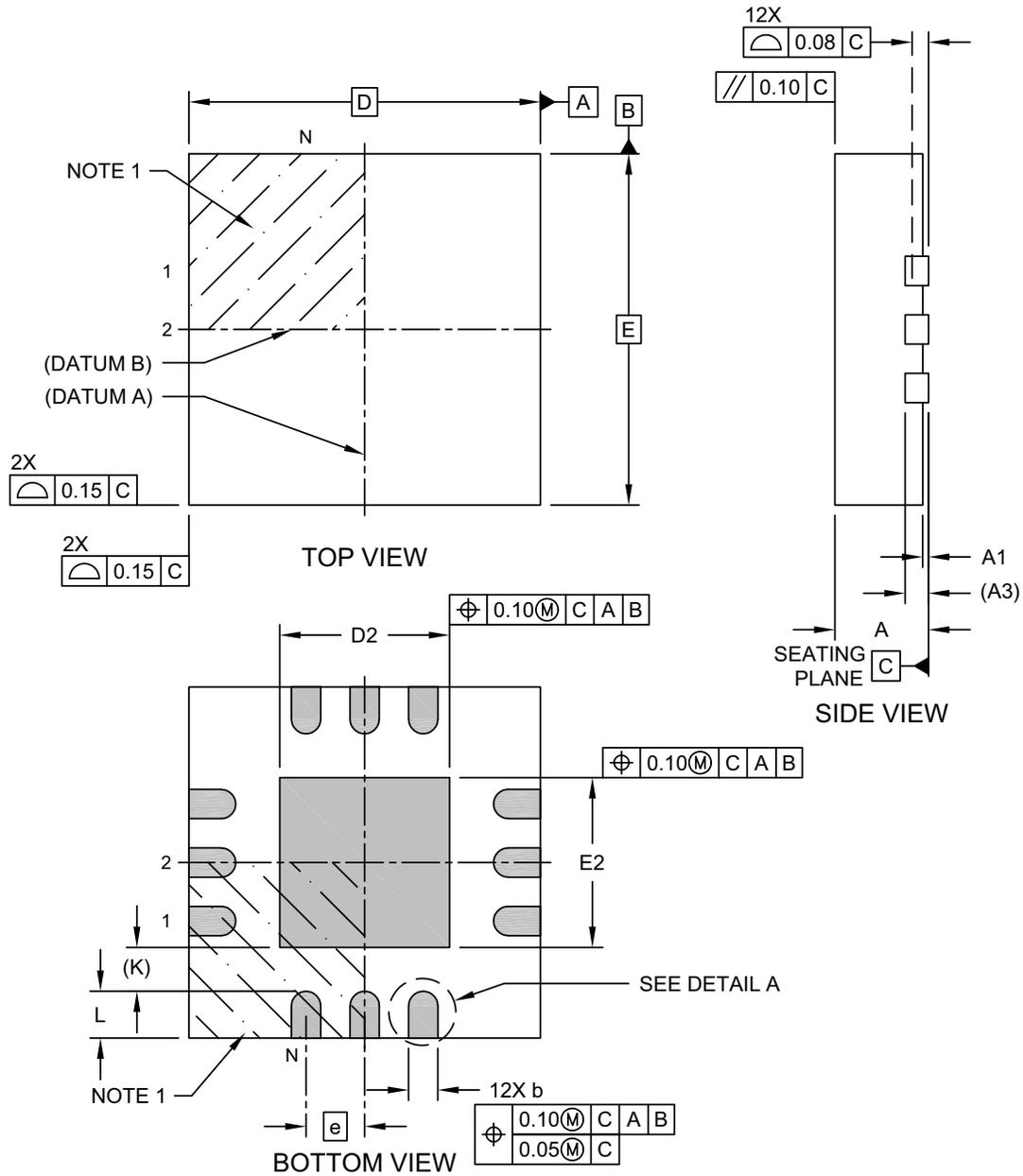
H860
2313
321

<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (  ) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

# HV860

## 12-Lead Very, Very Thin Plastic Quad Flat, No Lead (2PX) - 3x3x0.8 mm Body [WQFN] Supertex Legacy Package K7

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

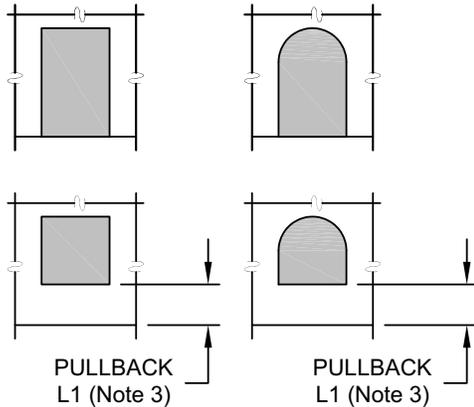


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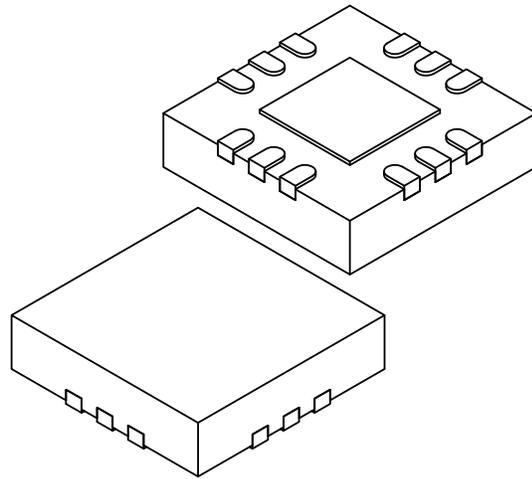
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## 12-Lead Very, Very Thin Plastic Quad Flat, No Lead (2PX) - 3x3x0.8 mm Body [WQFN] Supertex Legacy Package K7

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



**DETAIL A**  
ALTERNATE TERMINAL CONFIGURATIONS



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	12		
Pitch	e	0.50 BSC		
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	1.25	1.45	1.65
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.25	1.45	1.65
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Pullback (Note 3)	L1	–	–	0.15
Terminal-to-Exposed-Pad	K	0.38 REF		

**Notes:**

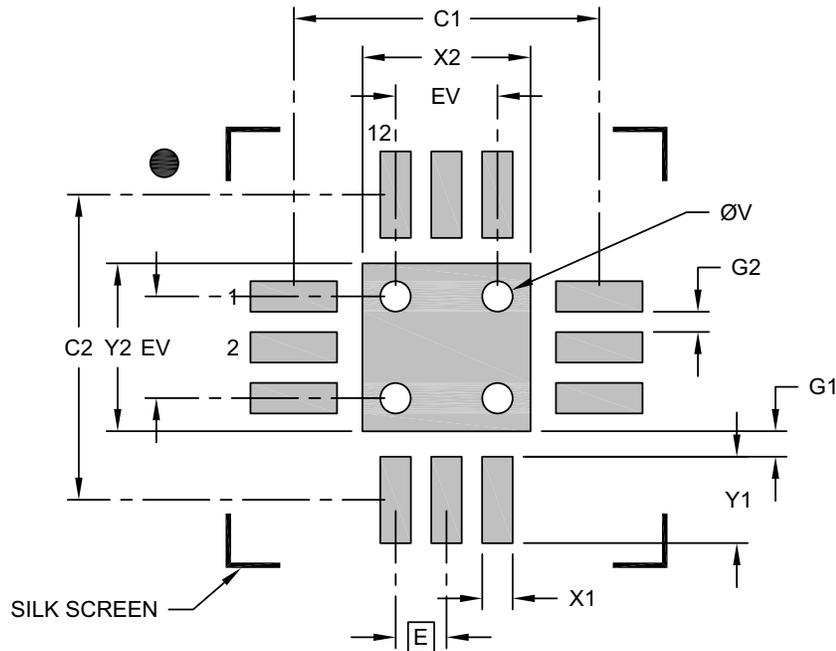
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-302 Rev A Sheet 2 of 2

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## 12-Lead Very, Very Thin Plastic Quad Flat, No Lead (2PX) - 3x3x0.8 mm Body [WQFN] Supertex Legacy Package K7

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.65
Optional Center Pad Length	Y2			1.65
Contact Pad Spacing	C1		3.00	
Contact Pad Spacing	C2		3.00	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.25		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2302 Rev A

## APPENDIX A: REVISION HISTORY

### Revision A (June 2023)

- Converted Supertex Doc# DSFP-HV860 to Microchip DS20005906A
- Changed the package marking format
- Changed the quantity of the 12-lead WQFN Package from 3000/Reel to 3300/Reel to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

# HV860

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<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	HV860	=	Low-Noise Dimmable EL Lamp Driver		
Package:	K7	=	12-lead WQFN (3 X 3)		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Type:	(blank)	=	3300/Reel for a K7 Package		

**Example:**

a) HV860K7-G: Low-Noise Dimmable EL Lamp Driver, 12-lead WQFN (3 X 3), 3300/Reel

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