DSC8103 | DSC8123

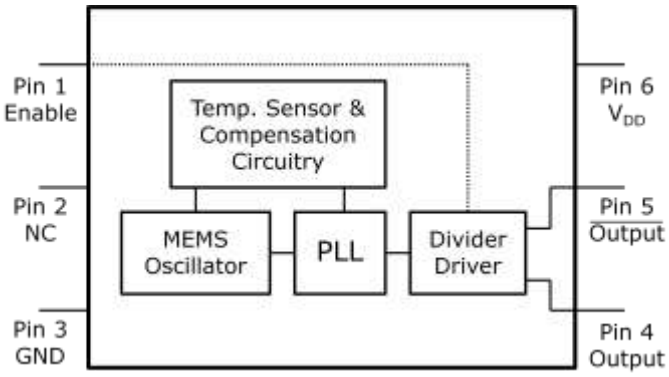
Programmable Low-Jitter Precision LVDS Oscillator

General Description

The DSC8103 & DSC8123 series of high performance field-programmable oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. Using the TIMEFLASH programmer, the end user can easily program the oscillators' frequency in the field for immediate testing or use in advance prototype development or production.

DSC8103 has a standby feature allowing it to completely power-down when EN pin is pulled low; whereas for DSC8123, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 3.2x2.5 mm^2, and are "drop-in" replacement for standard 6-pin LVDS quartz oscillators.

Block Diagram



Output Enable Modes

EN Pin	DSC8103	DSC8123
High	Outputs Active	Outputs Active
NC	Outputs Active	Outputs Active
Low	Standby	Outputs Disabled

Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Short Lead Time: 2 Weeks**
- **Wide Freq. Range: 10 to 460 MHz**
- **Small Industry Standard Footprints**
  - 2.5x2.0, 3.2x2.5, 5.0x3.2, & 7.0x5.0 mm
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Low Current Consumption**
- **Supply Range of 2.25 to 3.6 V**
- **Standby & Output Enable Function**
- **Lead Free & RoHS Compliant**
- **LVPECL & HCSL Versions Available**

Applications

- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express: Gen 1 & Gen 2**
- **DisplayPort**

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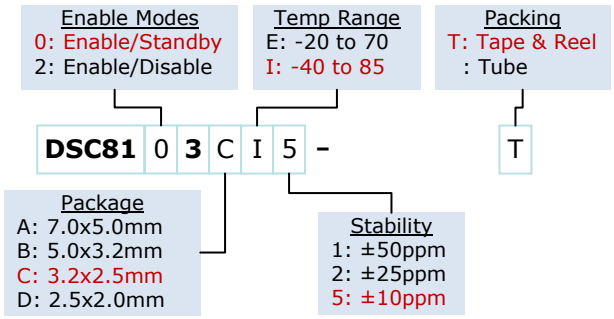
Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Note: 1000+ years of data retention on internal memory

Ordering Code



Specifications

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Supply Current	I_{DD}	EN pin low – outputs are disabled DSC8103 DSC8123		 20	 0.095 22	mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time[2]	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	 V_{IH} V_{IL}		 0.75xV_{DD} -		 - 0.25xV_{DD}	V
Output Disable Time[3]	t_{DA}				5	ns
Output Enable Time	t_{EN}	DSC8103 DSC8123			5 20	ms ns
Enable Pull-Up Resistor[4]		Pull-up resistor exist		40		kΩ
LVDS Outputs						
Supply Current	I_{DD}	Output Enabled, R_L=50Ω		29	32	mA
Output offset Voltage	V_{OS}	R=100Ω Differential	1.125		1.4	V
Delta Offset Voltage	ΔV_{OS}				50	mV
Pk to Pk Output Swing	V_{PP}	Single-Ended		350		mV
Output Transition time[3] Rise Time Fall Time	 t_R t_F	20% to 80% R_L=50Ω, C_L= 2pF		200		ps
Frequency	f_0	Single Frequency	10		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter	J_{PER}			2.5		ps_{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.28 0.4 1.7	 2	ps_{RMS}

Notes:
1. Pin 6 V_{DD} should be filtered with 0.1uf capacitor.
2. t_{su} is time to 100ppm of output frequency after V_{DD} is applied and outputs are enabled.
3. Output Waveform and Test Circuit figures below define the parameters.
4. Output is enabled if pad is floated or not connected.

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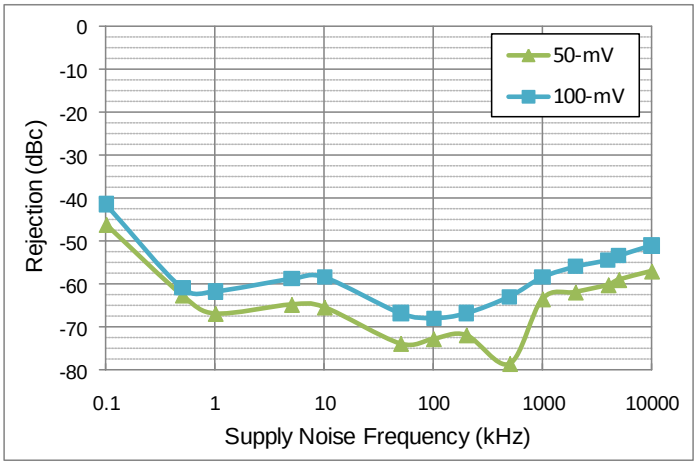
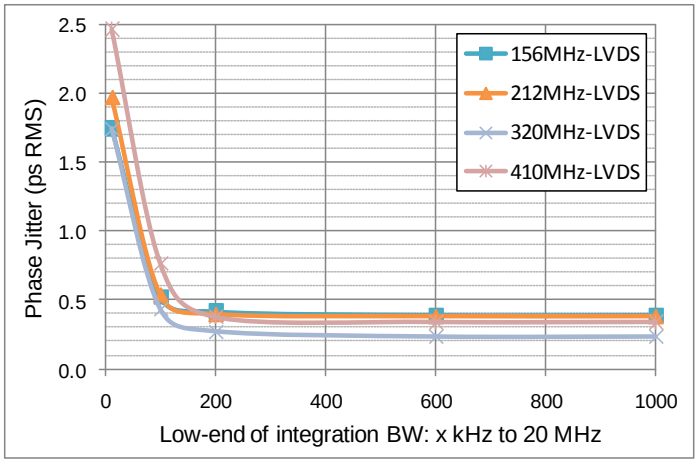
Nominal Performance Parameters (Unless specified otherwise: T=25° C, V_{DD}=3.3 V)

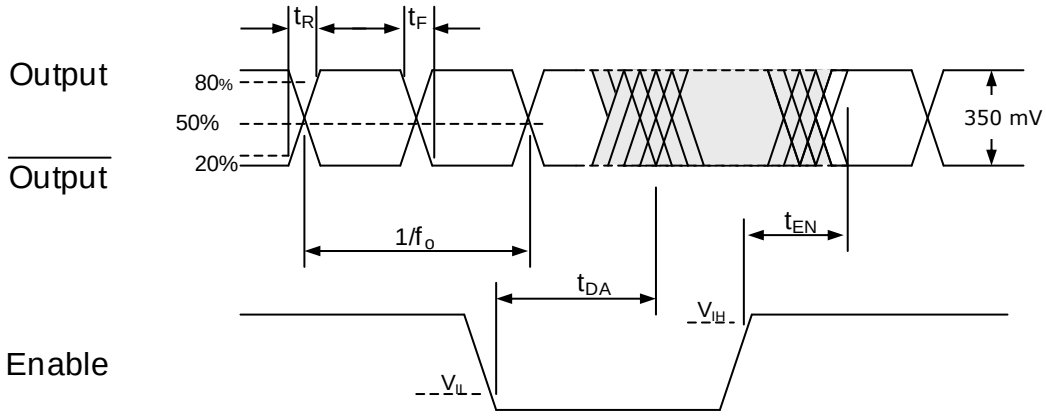


Power supply rejection ratio

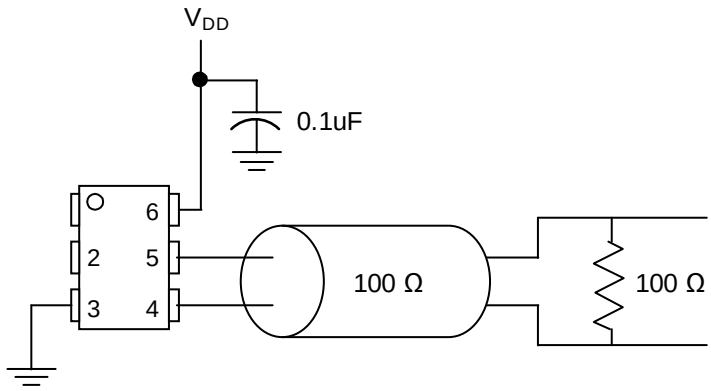


Phase jitter (integrated phase noise)

Output Waveform



Typical Termination Scheme



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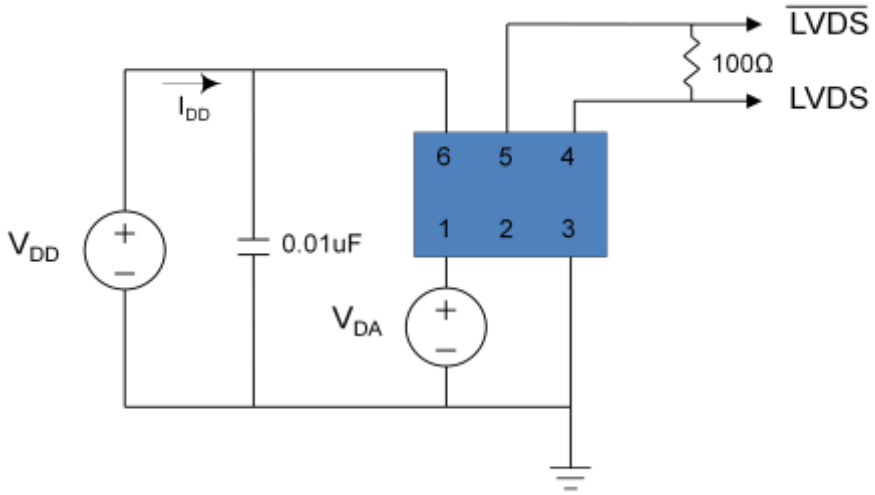
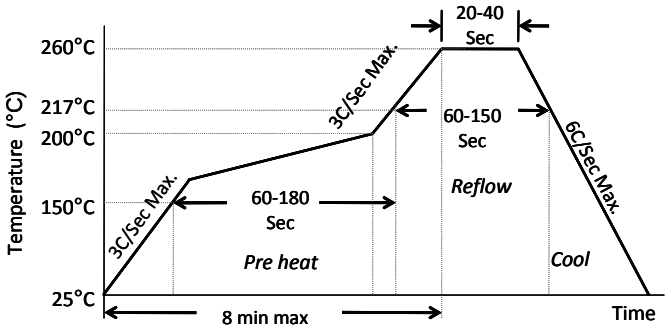
Test Circuit



Solder Reflow Profile



MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

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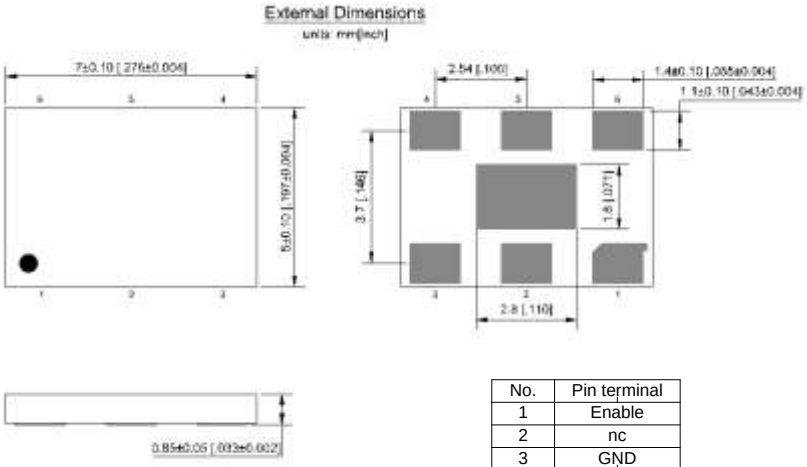
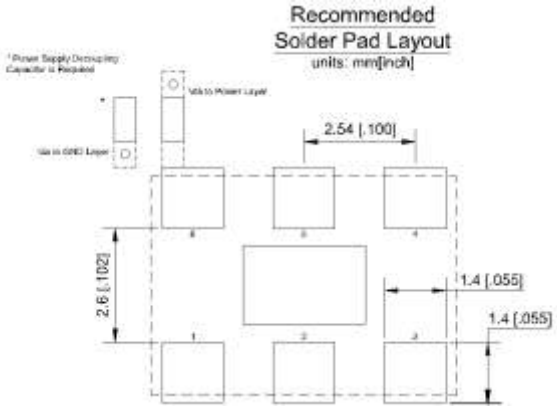
Package Dimensions

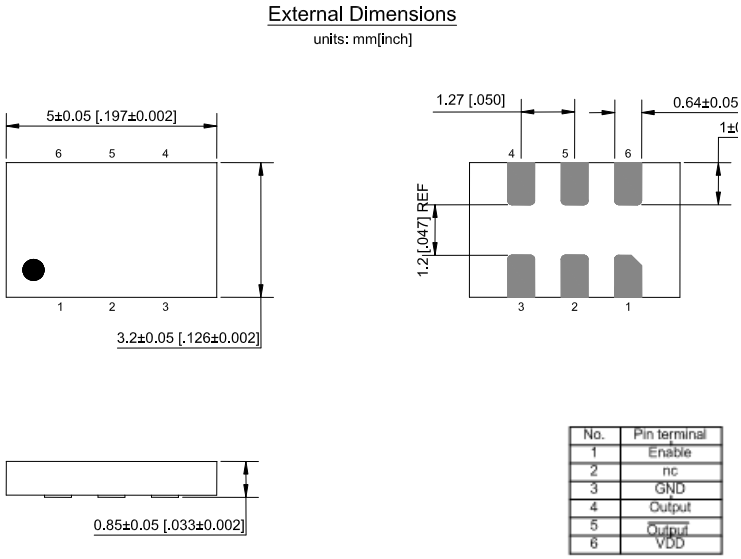
7.0 x 5.0 mm Plastic Package



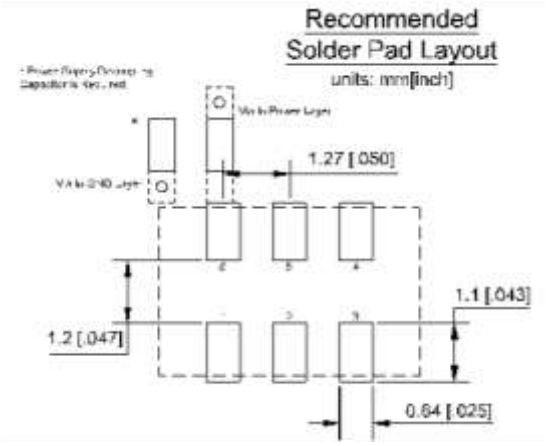
No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	$\overline{\text{Output}}$
6	VDD



5.0 x 3.2 mm Plastic Package



No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	$\overline{\text{Output}}$
6	VDD



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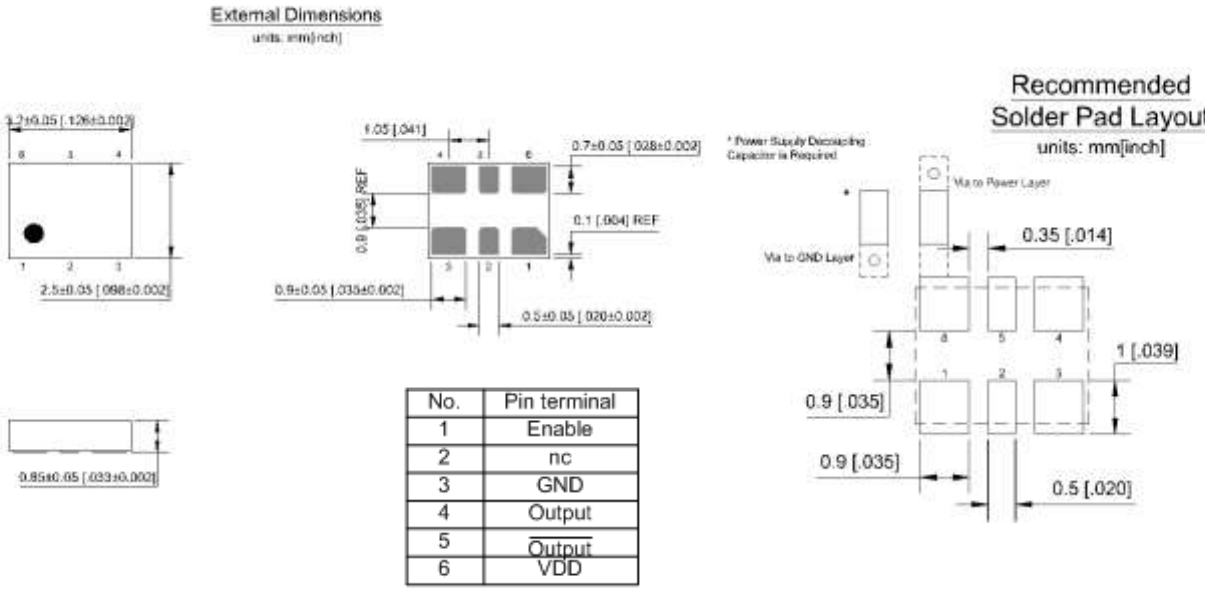
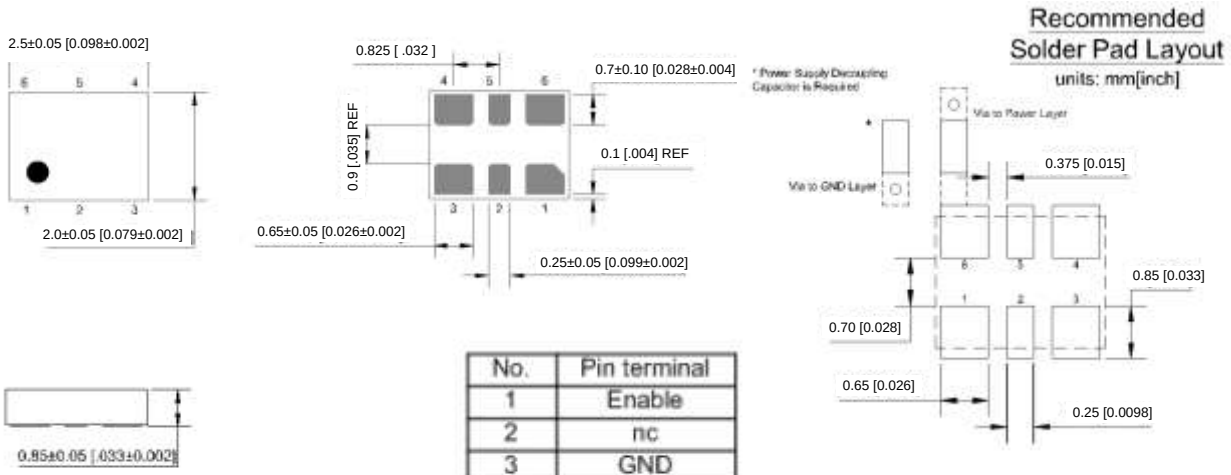
3.2 x 2.5 mm Plastic Package



No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	$\overline{\text{Output}}$
6	VDD

2.5 x 2.0 mm Plastic Package



No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	$\overline{\text{Output}}$
6	VDD

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