DSC612

Two-Output Low Power MEMS Clock Generator

Features

- MEMS-Based Clock Generator Eliminates the Need for External Crystal or Reference Clock
- Two LVCMOS Output Clocks: 2 kHz to 100 MHz
- Low Power Consumption: ~5 mA (Both Outputs Active)
- Wide Supply Voltage Range: 1.71V to 3.63V
- Ultra-Small Package Sizes:
  - 1.6 mm x 1.2 mm
  - 2.0 mm x 1.6 mm
  - 2.5 mm x 2.0 mm
- High Frequency Stability: ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range:
  - Automotive: –40°C to +125°C
  - Ext. Industrial: –40°C to +105°C
  - Industrial: –40°C to +85°C
  - Commercial: –20°C to +70°C
- Excellent Shock and Vibration Immunity:
  - Shock: Qualified to MIL-STD-883E Method 2002.3. Test Condition G (30,000g)
  - Vibration: Qualified to MIL-STD-883E Method 2007.2, Test Condition C (70g)
- High Reliability
- Lead-Free and RoHS-Compliant
- Automotive Option AEC-Q100 Available

Applications

- Low Power/Portable Applications: IoT, Embedded/Smart Devices
- Consumer: Home Healthcare, Fitness Devices, Home Automation
- Industrial: Building/Factory Automation, Surveillance Cameras

General Description

The DSC612 is a MEMS low power, ultra-small footprint, crystal-less family of clock generators. The DSC612 family is factory-configurable and generates up to two independent LVCMOS outputs. Each output can be configured to generate any frequency from 2 kHz to 100 MHz.

The DSC612 implements Microchip's proven PureSilicon™ MEMS technology to provide low jitter and high stability across a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, Microchip's crystal-less™ clock generators significantly enhance reliability and accelerate product development.

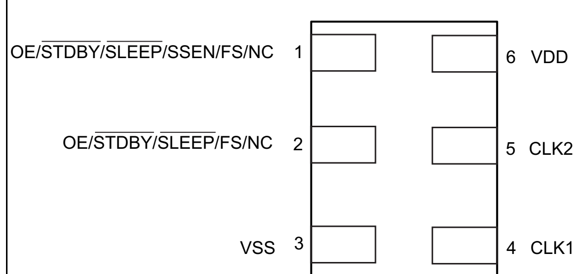
The DSC612 has two control inputs that can be configured to function as output enable/disable, standby, sleep, spread spectrum enable, and frequency select. The DSC612 is available in space saving 6-pin, 1.6 mm x 1.2 mm, 2.0 mm x 1.6 mm, and 2.5 mm x 2.0 mm VFLGA plastic packages.

The DSC612 spread spectrum function includes both center and down spreading, and is explained further in the Spread Spectrum section.

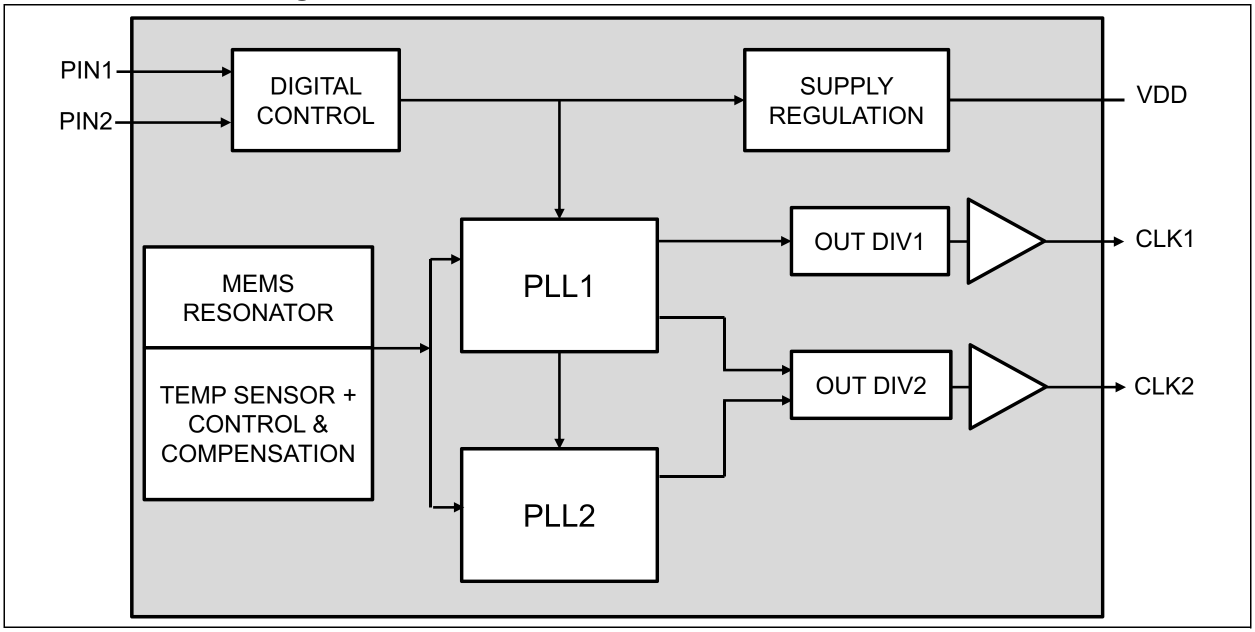
The DSC612 is a highly configurable device and is factory programmed to meet the customer's needs. Microchip's ClockWorks Configurator must be used to choose the necessary options, create the final part number, data sheet, and order samples.

Package Type

DSC612
6-Lead VFLGA
(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage .... –0.3V to +4.0V
Input Voltage .... –0.3V to V_{DD} + 0.3V
ESD Protection (HBM) .... 4 kV
ESD Protection (MM) 400V
ESD Protection (CDM) .... 2 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 1.8V ±5% to 3.3V ±10%; T_A = –40°C to +125°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	1.71	—	3.63	V	Note 1
Active Supply Current	I_{DD}	—	5	6	mA	f_{CLK1} = 27 MHz, f_{CLK2} = 25 MHz, V_{DD} = 1.8V, No Load
Active Supply Current (Sleep Mode, 1 PLL Off)	I_{DDSL}	—	3	—	mA	CLK2 = SLEEP, f_{CLK1} = 25 MHz, V_{DD} = 1.8V, No Load
Active Supply Current (32.768 kHz Output Only)	I_{DD32k}	—	1.4	—	mA	CLK2 = SLEEP, f_{CLK1} = 32.768 kHz, V_{DD} = 1.8V, No Load
Standby Supply Current, Note 2	I_{STDBY}	—	1.0	—	µA	V_{DD} = 1.8V/2.5V
		—	1.5	—		V_{DD} = 3.3V
Frequency Stability, Note 3	Δf	—	—	±20	ppm	All temperature ranges
		—	—	±25		
		—	—	±50		
Aging	Δf	—	—	±5	ppm	1st year @ +25°C
		—	—	±1		Per year after the first year
Startup Time	t_{SU}	—	—	1.5	ms	From 90% V_{DD} to valid clock output, T = +25°C
Input Logic Levels, Note 4	V_{IH}	0.7 x V_{DD}	—	—	V	Input logic high
	V_{IL}	—	—	0.3 x V_{DD}		Input logic low
Output Disable Time	t_{DA}	—	—	200 + 2 Periods	ns	Note 5
Output Enable Time	t_{EN}	—	1.0	—	µs	Note 6
Enable Pull-Up Resistor	—	—	300	—	kΩ	Note 7
Output Logic Levels	V_{OHY}	0.8 x V_{DD}	—	—	V	I = 6 mA (high drive) or I = 3 mA (standard drive)
	V_{OLY}	—	—	0.2 x V_{DD}		I = –6 mA (high drive) or I = –3 mA (standard drive)

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = 1.8V ±5% to 3.3V ±10%; T_A = –40°C to +125°C, unless noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Transition Time, Rise Time/Fall Time	t_{RY1}/t_{FY1}	—	1.2	2.0	ns	Standard drive 20% - 80% C_L = 10 pF, V_{DD} = 1.8V
		—	0.6	1.2	ns	Standard drive 20% - 80% C_L = 10 pF, V_{DD} = 2.5V/3.3V
	t_{RY2}/t_{FY2}	—	1.0	1.5	ns	High drive 20% - 80% C_L = 15 pF, V_{DD} = 1.8V
		—	0.5	1.0	ns	High drive 20% - 80% C_L = 15 pF, V_{DD} = 2.5V/3.3V
Frequency	f0	0.002	—	100	MHz	—
Output Duty Cycle	SYM	45	—	55	%	—
Period Jitter, RMS	J_{PER}	—	17	—	ps	f_{CLK1} = 24 MHz, f_{CLK2} = 27 MHz, V_{DD} = 1.8V
		—	14	—		f_{CLK1} = 24 MHz, f_{CLK2} = 27 MHz, V_{DD} = 3.3V
		—	9	—		f_{CLK1} = 27 MHz, f_{CLK2} = 27 MHz or 32.768 kHz, V_{DD} = 3.3V
Period Jitter, Peak-to-Peak	J_{PER}	—	120	—	ps	f_{CLK1} = 24 MHz, f_{CLK2} = 27 MHz, V_{DD} = 1.8V
		—	100	—		f_{CLK1} = 24 MHz, f_{CLK2} = 27 MHz, V_{DD} = 3.3V
		—	80	—		f_{CLK1} = 27 MHz, f_{CLK2} = 27 MHz or 32.768 kHz, V_{DD} = 3.3V
Cycle-to-Cycle Jitter (peak)	$J_{Cy\text{-}Cy}$	—	105	—	ps	f_{CLK1} = 24 MHz, f_{CLK2} = 27 MHz, V_{DD} = 1.8V
		—	90	—		f_{CLK1} = 24 MHz, f_{CLK2} = 27 MHz, V_{DD} = 3.3V
		—	70	—		f_{CLK1} = 27 MHz, f_{CLK2} = 27 MHz or 32.768 kHz, V_{DD} = 3.3V

Note 1: V_{DD} pin should be filtered with a 0.1 µF capacitor.
2: Excludes input pull-up current.
3: Includes frequency variations due to initial tolerance, temperature, and power supply voltage.
4: Input waveform must be monotonic with rise/fall time < 10 ms.
5: Output disable time takes up to two Periods of the output waveform, plus 200 ns.
6: For parts configured with OE, not Standby.
7: Output is enabled if pad is floated or not connected.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–55	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 40s

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The DSC612 is a highly configurable device and can be factory programmed in many different ways to meet the customer's needs. Microchip's ClockWorks Configurator http://clockworks.microchip.com/Timing/ must be used to choose the necessary options, create the final part number, data sheet, and order samples. The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: DSC612 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	OE	Output Enable: H = Active, L = Disabled (High Impedance).
	$\overline{\text{STDBY}}$	Standby: H = Device is active, L = Device is in standby (Low Power Mode).
	FS	Frequency Select: H = Output Frequency 1, L = Output Frequency 2.
	$\overline{\text{SLEEP}}$	Sleep: H= Output Enabled, L= Output and associated PLL Disabled.
	SSEN	Spread Spectrum: H = Enabled, L = Disabled.
	NC	Non-functional, do not connect.
2	OE	Output Enable: H = Active, L = Disabled (High Impedance).
	$\overline{\text{STDBY}}$	Standby: H = Device is active, L = Device is in standby (Low Power Mode).
	FS	Frequency Select: H = Output Frequency 1, L = Output Frequency 2.
	$\overline{\text{SLEEP}}$	Sleep: H= Output Enabled, L= Output and associated PLL Disabled
	NC	Non-functional, do not connect.
3	VSS	Ground.
4	CLK1	Factory configurable LVCMOS clock output 1: 2 kHz to 100 MHz, standard drive or high drive.
5	CLK2	Factory configurable LVCMOS clock output 2: 2 kHz to 100 MHz, standard drive or high drive.
6	VDD	Power Supply: 1.71V to 3.63V.

An explanation of the different options listed in Table 2-1 follows:

2.1 Pin 1 and Pin 2

These are control pins and each may be configured to fulfill one of six different functions. If not actively driven, a 10 kΩ pull-up resistor is recommended.

2.1.1 OUTPUT ENABLE (OE)

Both pin 1 and pin 2 may be configured as Output Enable. Either or both outputs may be turned on and off according to the state of the pins.

2.1.2 $\overline{\text{STANDBY}}$

Either pin 1 or pin 2 (but not both) may be configured as standby. When the pin is low, both outputs will be off and the device will enter a low power mode.

2.1.3 $\overline{\text{SLEEP}}$

Either pin 1 or pin 2 (but not both) may be configured as sleep. When the pin is low, one phase lock loop (PLL) will shut down, enabling power saving. Any output driven by that PLL will be turned off.

2.1.4 SPREAD SPECTRUM ENABLE (SSEN)

Only pin 1 may be configured as SSEN. When the pin is high, the associated output will be spread in frequency. When the pin is low, no spreading will occur.

2.1.5 FREQUENCY SELECT (FS)

Both pin 1 and pin 2 may be configured as FS. Each output may be set to one of two pre-programmed frequencies (four pre-programmed frequencies in total).

2.1.6 NC

Both pin 1 and pin 2 may be configured as NC. In this case, the pins are non-functional and the device is programmed and fixed according to the choices in ClockWorks Configurator.

2.2 Pins 3 through 6

Pins 3 and 6 are the supply terminals, V_{SS} and V_{DD} respectively. Pins 4 and 5 are the two clock outputs, CLK1 and CLK2 respectively. CLK1 and CLK2 outputs are programmable to Standard and High Drive strengths settings through ClockWorks Configurator.

3.0 SPREAD SPECTRUM

Spread spectrum is a slow modulation of the clock frequency over time. The PLL inside the MEMS oscillator is modulated with a triangular wave at 33 kHz. With such a slow modulation, the peak spectral energy of both the fundamental and all the harmonics is spread over a wider frequency range. This significantly reduces peak energy density, thus providing an EMI reduction. The triangular wave is chosen because of its flat spectral density.

The DSC612 MEMS oscillator family offers several modulation options: the spreading is either center spread or down spread with respect to the clock frequency. Center spreading ranges from ±0.25% to ±2.5%, while down spreading ranges from –0.25% to –3%.

If the clock frequency is 100 MHz and center spreading with ±1% is chosen, the output clock will range from 99 MHz to 101 MHz. If down spreading with –2% is chosen, the output clock will range from 98 MHz to 100 MHz.

Figure 3-1 and Figure 3-2 show a spectrum example of the DSC612 with a 33.333 MHz clock, modulated with central spread of ±1%.

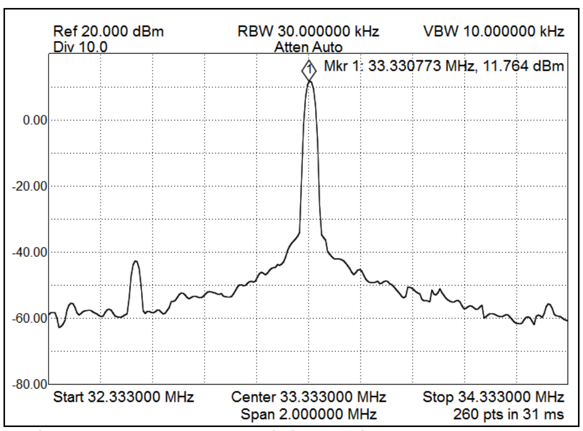


FIGURE 3-1: *DSC612 Spectrum at 33.333 MHz with Modulation Turned Off.*

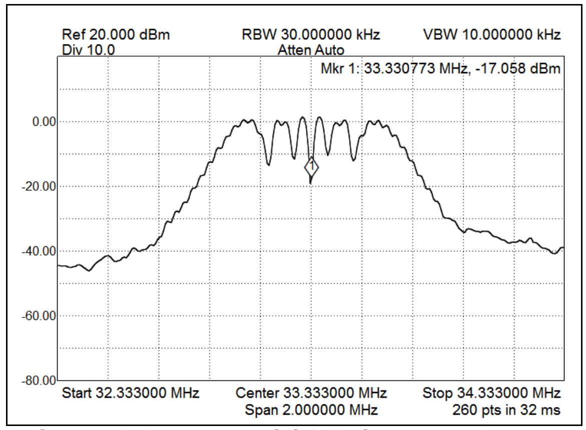


FIGURE 3-2: *DSC612 Spectrum at 33.333 MHz with Modulation Turned On.*

It is noticeable that the spread spectrum provides a reduction of about 10 dB from the peak power. Such a reduction may also be estimated by the following equation:

EQUATION 3-1:

$$EMI\ \text{Reduction} = 10 \times Log10(|S| \times fc \div RBW)$$

Where:

S	Peak-to-peak spread percentage (0.01, this example).
fc	Carrier frequency (33.333 MHz, this example).
RBW	Resolution bandwidth of the spectrum analyzer (30 kHz, this example).

The theoretical calculation for this example provides 10.45 dB, which is consistent with the measurement.

Similarly to the fundamental frequency, all the harmonics are spread and attenuated in similar fashion. Figure 3-3 shows how the DSC612 fundamental at 33.333 MHz and its odd harmonics are attenuated when various types of modulations are selected. For picture clarity, only the center spread options are shown. However, down spread with corresponding percentage provides the same level of harmonic attenuation (e.g. central spread of ±1% provides the same harmonics attenuation of down spread with –2%).

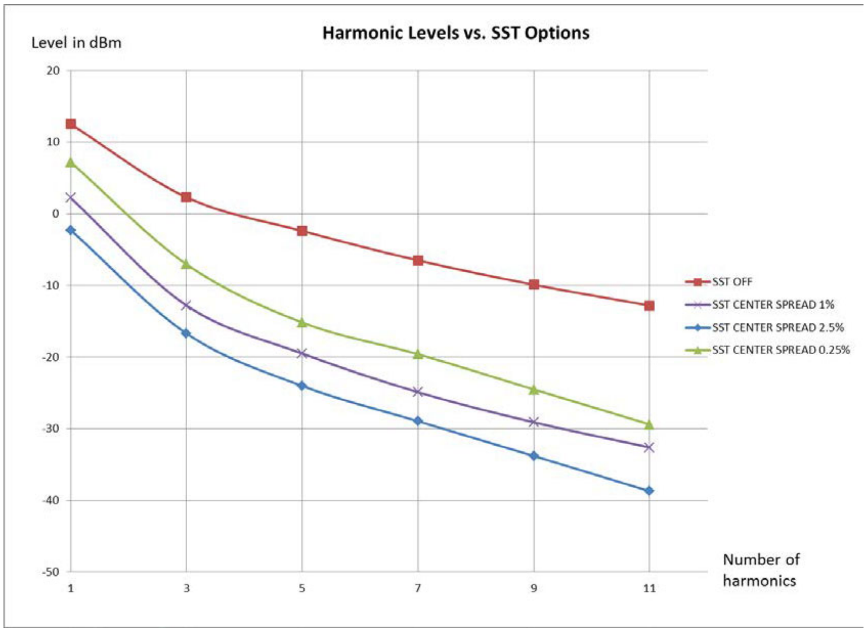


FIGURE 3-3: *DSC612 Harmonic Levels with Various Spread Spectrum Options.*

Visit Microchip's ClockWorks Configurator to select Spread Spectrum options.

4.0 OUTPUT WAVEFORM

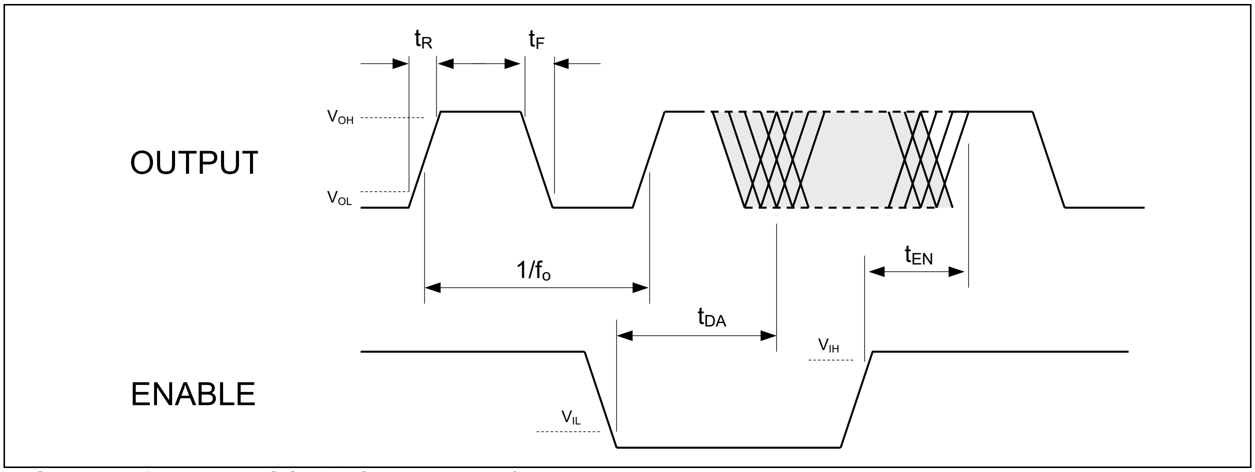


FIGURE 4-1: *DSC612 Output Waveform.*

5.0 BOARD LAYOUT

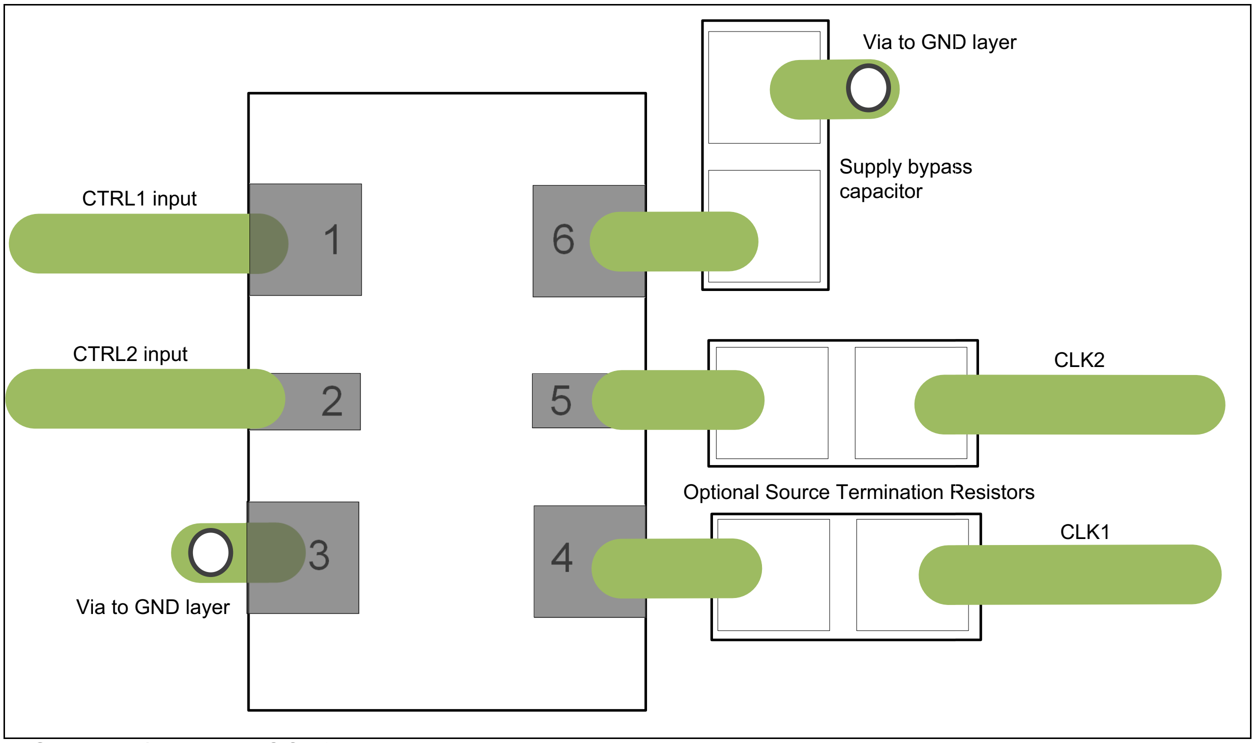


FIGURE 5-1: *DSC612 Board Layout.*

6.0 SOLDER REFLOW PROFILE

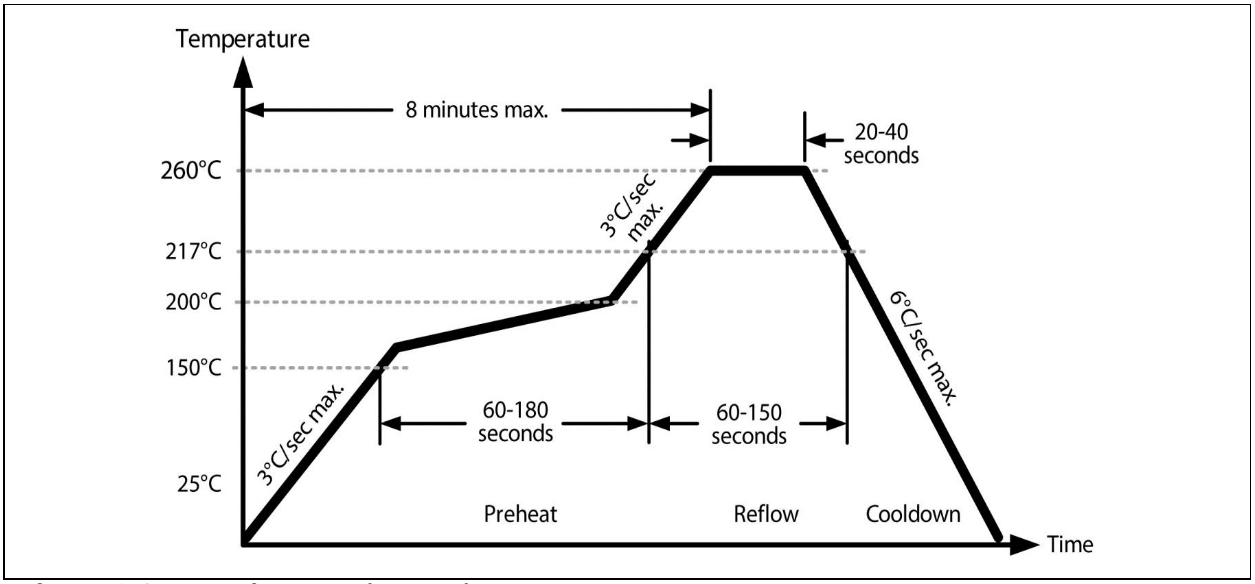


FIGURE 6-1: Solder Reflow Profile.

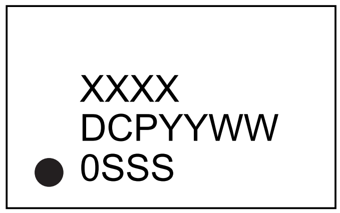
TABLE 6-1: SOLDER REFLOW

MSL 1 @ 260°C Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

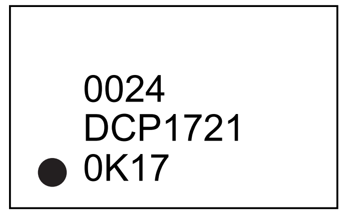
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

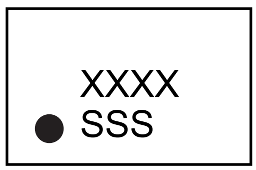
6-Lead VFLGA*
(2.5mm x 2.0mm)



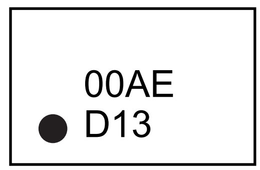
Example



6-Lead VFLGA*
(1.2mm x 1.6mm)
(1.6mm x 2.0mm)



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

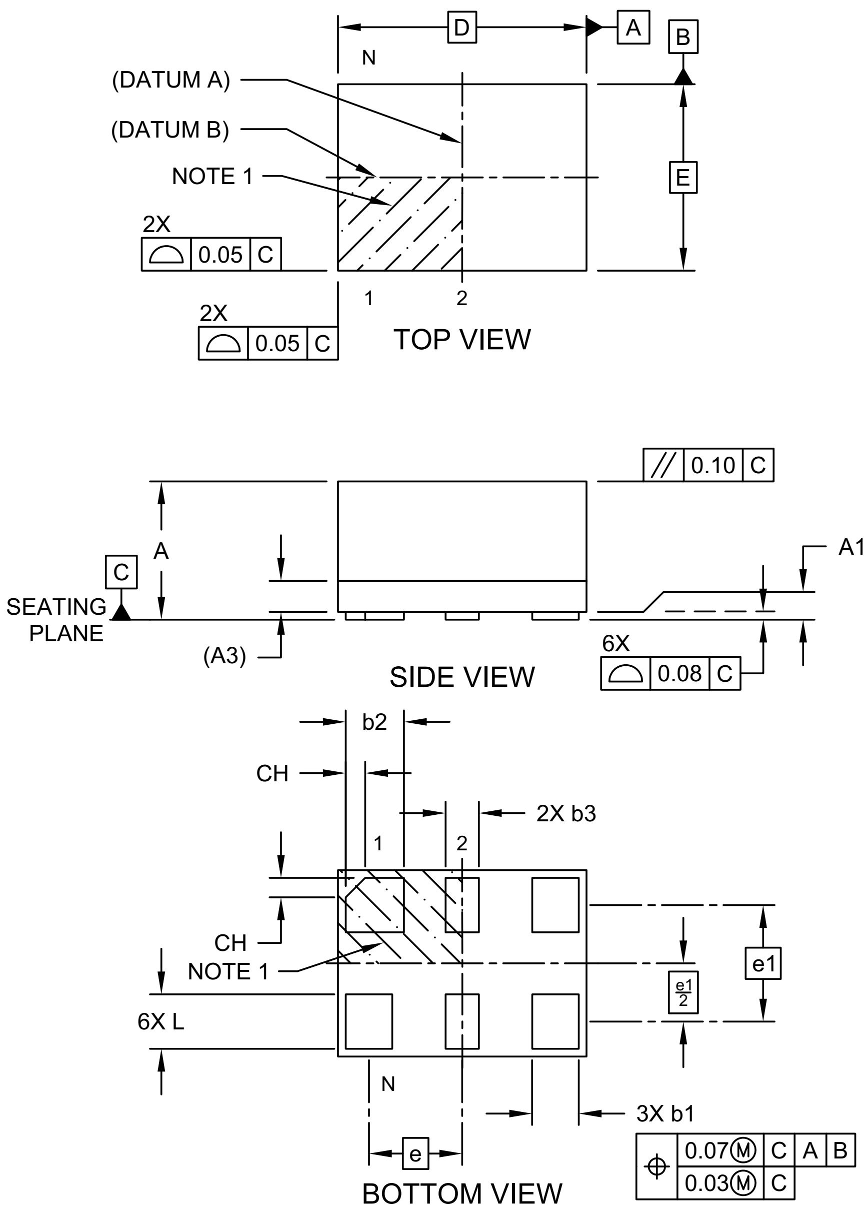
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

6-Lead 1.6 mm x 1.2 mm VFLGA Package Outline and Recommended Land Pattern

6-Lead Very Thin Fine Pitch Land Grid Array (AVA) - 1.6x1.2 mm Body [VFLGA]

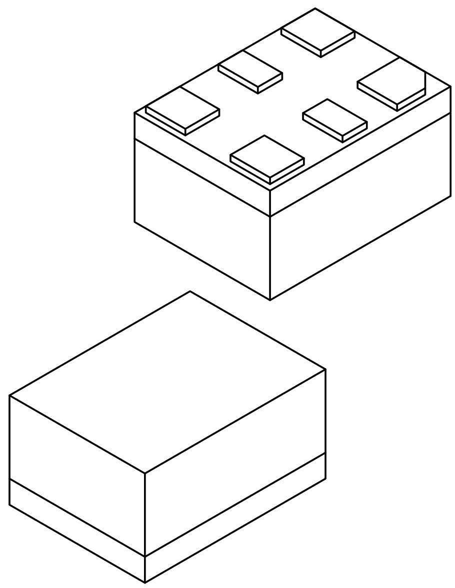
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1203A Sheet 1 of 2

6-Lead Very Thin Fine Pitch Land Grid Array (AVA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Terminal Pitch	e		0.60 BSC	
Terminal Pitch	e1		0.75 BSC	
Overall Height	A	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3		0.20 REF	
Overall Length	D		1.60 BSC	
Overall Width	E		1.20 BSC	
Terminal Width	b1	0.25	0.30	0.35
Terminal Width	b2	0.325	0.375	0.425
Terminal Width	b3	0.20	0.25	0.30
Terminal Length	L	0.30	0.35	0.40
Terminal 1 Index Chamfer	CH	-	0.125	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

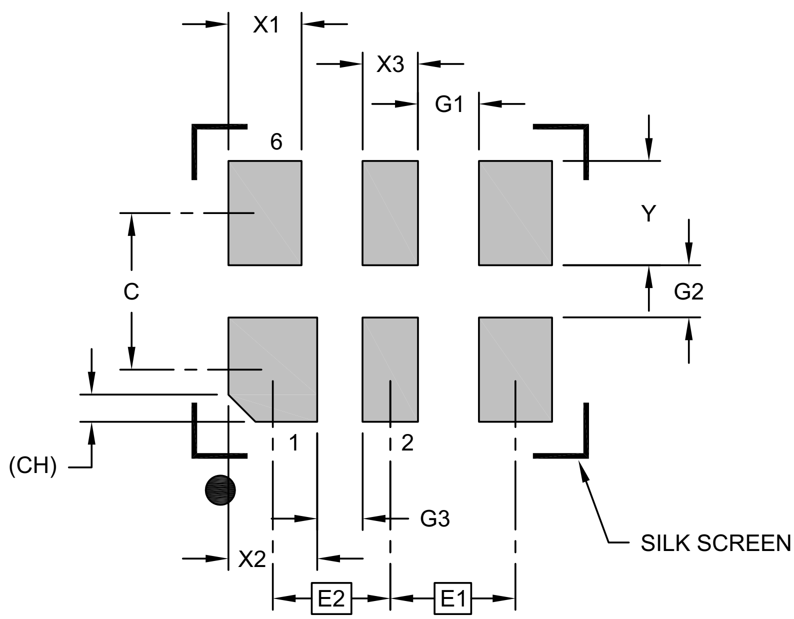
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1203A Sheet 2 of 2

6-Lead Very Thin Fine Pitch Land Grid Array (AVA) - 1.6x1.2 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS	
	Dimension Limits	MIN	NOM	MAX
Contact Pitch (X3)	E1		0.60 BSC	
Contact Pitch	E2		0.56 BSC	
Contact Spacing	C		0.75	
Contact Width (X3)	X1			0.35
Contact Width	X2			0.43
Contact Width (X2)	X3			0.27
Contact Pad Length (X6)	Y			0.50
Space Between Contacts (X4)	G1	0.29		
Space Between Contacts (X3)	G2	0.25		
Space Between Contacts	G3	0.22		
Contact 1 Index Chamfer	CH		0.13 X 45° REF	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

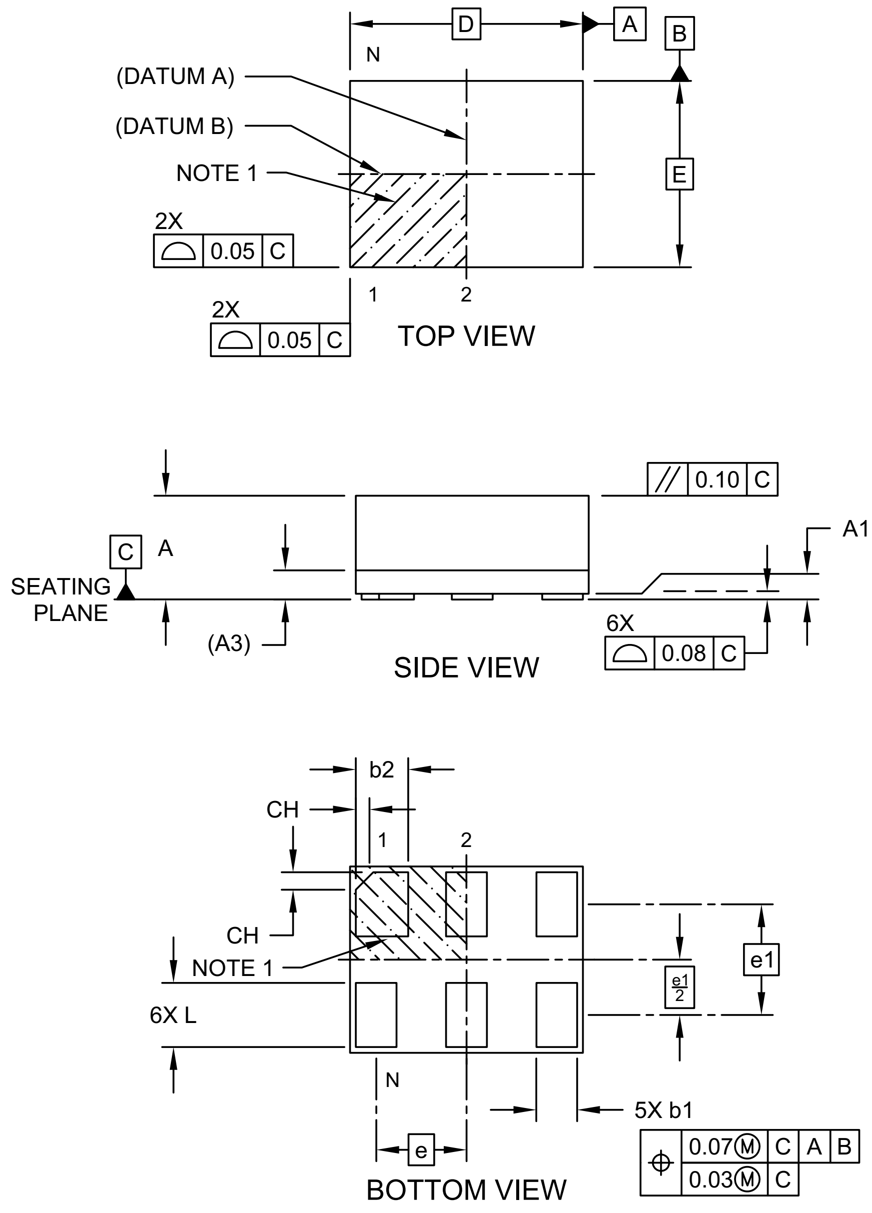
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3203A

6-Lead 2.0 mm x 1.6 mm VFLGA Package Outline and Recommended Land Pattern

6-Lead Very Thin Fine Pitch Land Grid Array (ATA) - 2.0x1.6 mm Body [VFLGA]

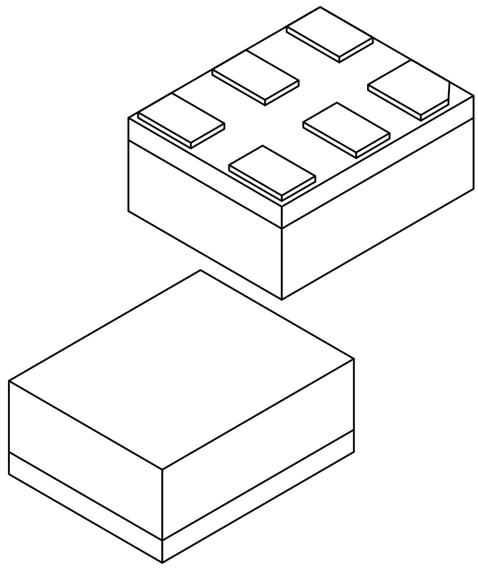
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1201A Sheet 1 of 2

6-Lead Very Thin Fine Pitch Land Grid Array (ATA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		6	
Terminal Pitch	e		0.775 BSC	
Terminal Pitch	e1		0.95 BSC	
Overall Height	A	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		1.60 BSC	
Terminal Width	b1	0.30	0.35	0.40
Terminal Width	b2	0.40	0.45	0.50
Terminal Length	L	0.50	0.55	0.60
Terminal 1 Index Chamfer	CH	-	0.15	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

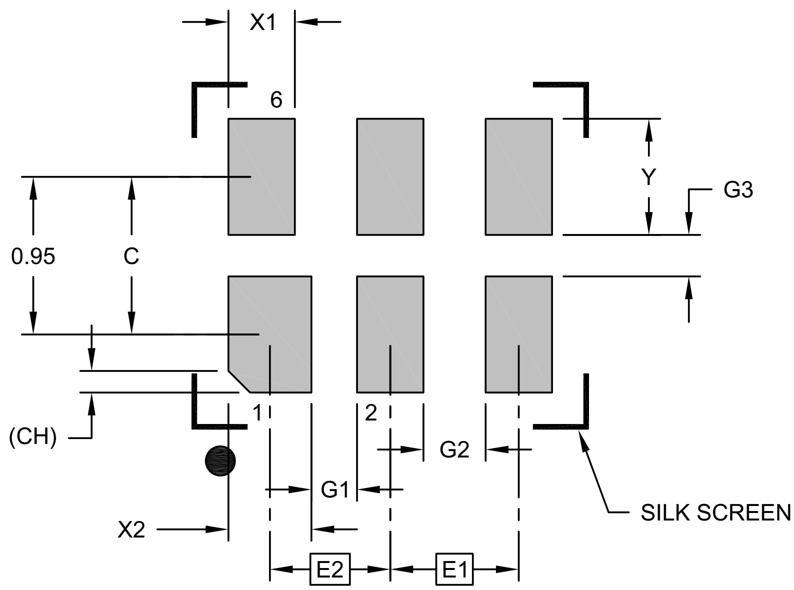
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1201A Sheet 2 of 2

6-Lead Very Thin Fine Pitch Land Grid Array (ATA) - 2.0x1.6 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E1	0.78 BSC		
Contact Pitch	E2	0.73 BSC		
Contact Spacing	C		0.95	
Contact Width (X4)	X1			0.40
Contact Width (X2)	X2			0.45
Contact Pad Length (X6)	Y			0.70
Space Between Contacts (X4)	G1	0.28		
Space Between Contacts (X3)	G2	0.38		
Space Between Contacts (X3)	G3	0.25		
Contact 1 Index Chamfer	CH	0.13 X 45° REF		

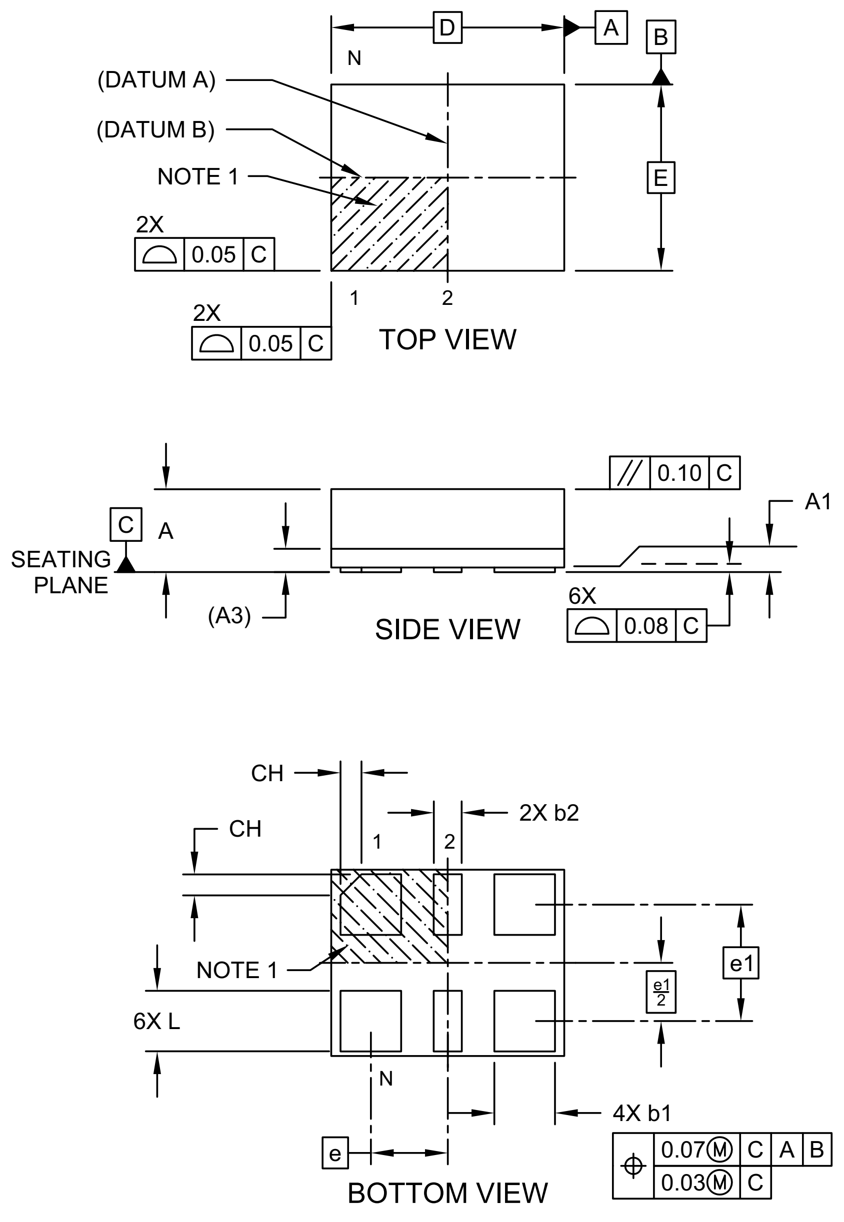
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3201A

6-Lead 2.5 mm x 2.0 mm VFLGA Package Outline and Recommended Land Pattern

6-Lead Very Thin Fine Pitch Land Grid Array (AWA) - 2.5x2.0 mm Body [VFLGA]

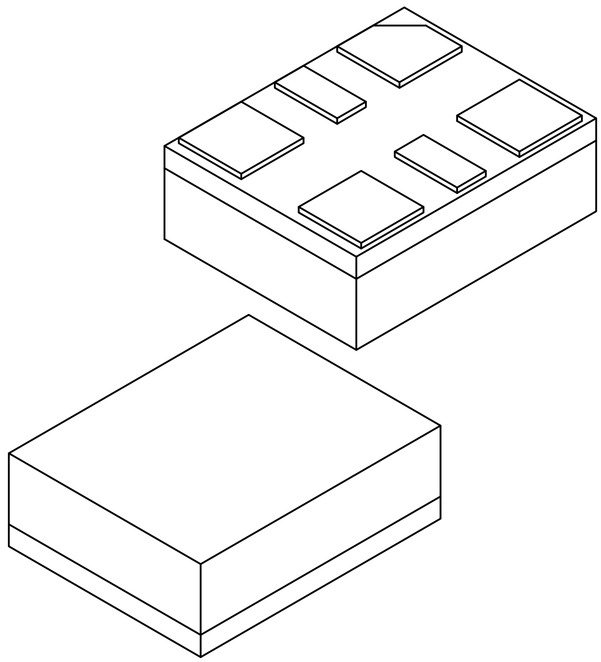
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1204A Sheet 1 of 2

6-Lead Very Thin Fine Pitch Land Grid Array (AWA) - 2.5x2.0 mm Body [VFLGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Terminal Pitch	e		0.825 BSC	
Terminal Pitch	e1		1.25 BSC	
Overall Height	A	0.79	0.84	0.89
Standoff	A1	0.00	0.02	0.05
Substrate Thickness (with Terminals)	A3		0.20 REF	
Overall Length	D		2.50 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.25	0.30	0.35
Terminal Length	L	0.60	0.65	0.70
Terminal 1 Index Chamfer	CH	-	0.225	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

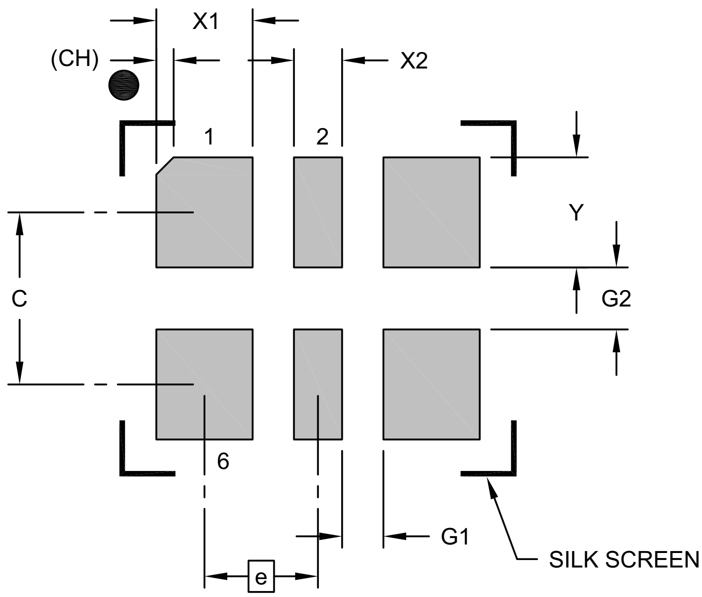
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1204A Sheet 2 of 2

6-Lead Very Thin Fine Pitch Land Grid Array (AWA) - 2.5x2.0 mm Body [VFLGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.825 BSC		
Contact Spacing	C	1.25 BSC		
Contact Width (X4)	X1			0.70
Contact Width (X2)	X2			0.35
Contact Pad Length (X6)	Y			0.80
Space Between Contacts (X4)	G1	0.30		
Space Between Contacts (X3)	G2	0.45		
Contact 1 Index Chamfer	CH	0.13 X 45° REF		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3204A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Initial release of DSC612 as Microchip data sheet DS20006023A.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	X	-XXXX	X
Device	Package	Temperature	Frequency Stability	Revision	Configuration #	Special Processing

Device:	DSC612:		Two-Output Low Power MEMS Clock Generator
Package:	R	=	6-Lead 2.5 mm x 2.0 mm VFLGA
	N	=	6-Lead 2.0 mm x 1.6 mm VFLGA
	P	=	6-Lead 1.6 mm x 1.2 mm VFLGA
Temperature:	E	=	–20°C to +70°C
	I	=	–40°C to +85°C
	L	=	–40°C to +105°C
	A	=	–40°C to +125°C
Frequency Stability:	1	=	±50 ppm
	2	=	±25 ppm
	3	=	±20 ppm
Revision:	A	=	1st Revision
Configuration Number:	User-Defined in the ClockWorks Configurator		
Special Processing:	<blank>	=	140/Tube (R Package Option)
	<blank>	=	100/Bag (N & P Package Options)
	T	=	1,000/Reel
	B	=	3,000/Reel

The DSC612 is a highly configurable device and is factory programmed to meet the customer's needs. Microchip's ClockWorks Configurator must be used to choose the necessary options, create the final part number, data sheet, and order samples.

Examples:

a) DSC612RE1A-0024T:
Two-Output Low Power MEMS Clock Generator, 6-Lead 2.5 mm x 2.0 mm VFLGA, –20°C to +70°C, ±50 ppm, 1st Revision, 1,000/Reel

b) DSC612NL2A-2885:
Two-Output Low Power MEMS Clock Generator, 6-Lead 2.0 mm x 1.6 mm VFLGA, –40°C to +105°C, ±25 ppm, 1st Revision, 100/Bag

c) DSC612PA3A-8751B:
Two-Output Low Power MEMS Clock Generator, 6-Lead 1.6 mm x 1.2 mm VFLGA, –40°C to +125°C, ±20 ppm, 1st Revision, 3,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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