

ATF16V8B, ATF16V8BQ*, and ATF16V8BQL

High-performance EE PLD

DATASHEET

Features

- Industry-standard Architecture
 - Emulates Many 20-pin PALs[®]
 - Low-cost Easy-to-use Software Tools
- High-speed Electrically-erasable Programmable Logic Devices
 - 10ns Maximum Pin-to-pin Delay
- Automatic 5mA Standby for ATF16V8BQL
- CMOS and TTL Compatible Inputs and Outputs
 - Input and I/O Pull-up Resistors
- Advanced Flash Technology
 - Reprogrammable
 - 100% Tested
- High-reliability CMOS Process
 - 20 Year Data Retention
 - 100 Erase/Write Cycles
 - 2,000V ESD Protection
 - 200mA Latchup Immunity
- Industrial Temperature Range
- Dual-in-line and Surface Mount Packages in Standard Pinouts
- PCI-compliant
- Green Package Options (Pb/Halide-free/RoHS Compliant)

Description

The Atmel® ATF16V8B(QL) is a high-performance CMOS Electrically-Erasable Programmable Logic Device (EE PLD) that utilizes the Atmel proven electrically-erasable Flash memory technology. All speed ranges are specified over the full $5.0V \pm 10\%$ range for industrial temperature range.

The ATF16V8BQL provides edge-sensing low-power PLD solution with low standby power consumption (5mA typical). The ATF16V8BQL powers down automatically to the low-power mode through the Input Transition Detection (ITD) circuitry when the device is idle.

The ATF16V8B(QL) incorporate a super set of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

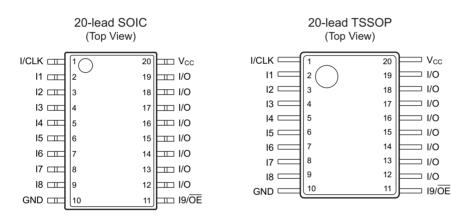
*The ATF16V8BQ is Replaced by ATF16V8B and ATF16V8BQL

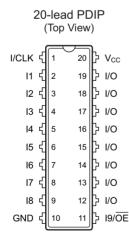
1. Pin Configurations and Pinouts

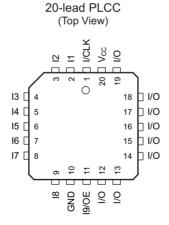
Table 1-1. Pin Configurations

Pin Name	Function
CLK	Clock
GND	Ground
1	Logic Inputs
I/O	Bi-directional Buffers
ŌĒ	Output Enable
V _{CC}	+5V Power Supply

Figure 1-1. Pinouts



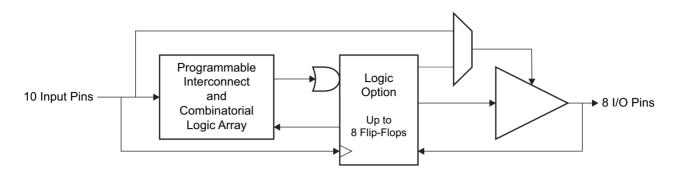




Note: Drawings are not to scale.

2. Block Diagram

Figure 2-1. Block Diagram





3. Electrical Characteristics

3.1 Absolute Maximum Ratings*

Temperature Under Bias55°C to +125°C
Storage Temperature65°C to +150°C
Voltage on Any Pin with Respect to Ground2.0V to +7.0V ⁽¹⁾
Voltage on Input Pins with Respect to Ground During Programming2.0V to +14.0V ⁽¹⁾
Programming Voltage with Respect to Ground2.0V to +14.0V ⁽¹⁾

*Notice: Stresses beyond those listed under
"Absolute Maximum Ratings" may cause
permanent damage to the device. This is
a stress rating only and functional
operation of the device at these or any
other conditions beyond those indicated
in the operational sections of this
specification is not implied. Exposure to
absolute maximum rating conditions for
extended periods may affect device
reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20ns.

3.2 Pin Capacitance

Table 3-1. Pin Capacitance (f = 1MHz, $T = 25°C^{(1)}$)

	Тур	Max	Units	Conditions
C _{IN}	5	8	pF	V _{IN} = 0V
C _{OUT}	6	8	pF	V _{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

3.3 DC and AC Operating Conditions

Table 3-2. DC and AC Operating Conditions

	Industrial
Operating Temperature (Ambient)	-40°C to +85°C
V _{CC} Power Supply	5.0V ± 10%

3.4 DC Characteristics

Table 3-3. DC Characteristics

Symbol	Parameter	Condition		Min	Тур	Max	Units
I _{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}(Max)$			-35	-100	μA
I _{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$				10	μA
			B-10		55	95	
I _{CC}	Power Supply Current, Standby	V _{CC} = Max V _{IN} = Max, Outputs Open	B-15		50	80	mA
			BQL-15		5	15	
	Clocked Power Supply Current	V _{CC} = Max, Outputs Open f = 15MHz	B-10		60	100	mA
I _{CC2}			B-15		55	95	
			BQL-15		20	40	
I _{OS} ⁽¹⁾	Output Short Circuit Current	V _{OUT} = 0.5 V				-130	mA
V _{IL}	Input Low Voltage			-0.5		0.8	V
V _{IH}	Input High Voltage					V _{CC} + 0.75	V
V _{OL}	Output High Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min}$ $I_{OL} = 24\text{mA}$				0.5	V
V _{OH}	Output High Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min}$	I _{OH} = -4.0 mA	2.4			V

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30s.



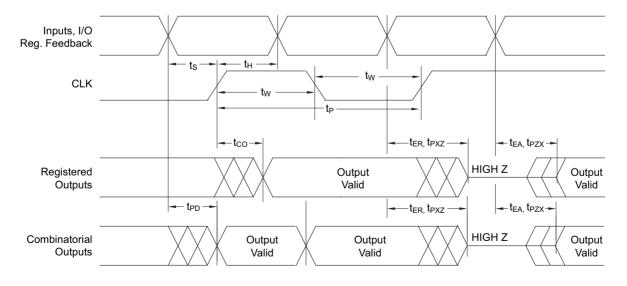
3.5 AC Characteristics

Table 3-4. AC Characteristics⁽¹⁾

			-1	10	-1	15	
Symbol	Parameter		Min	Max	Min	Max	Units
t _{PD}	Input or Feedback to Non-Registered Output	8 outputs switching	3	10	3	15	ns
t _{CF}	Clock to Feedback			6		8	ns
t _{CO}	Clock to Output		2	7	2	10	ns
t _S	Input or Feedback Setup Tim	е	7.5		12		ns
t _H	Hold Time		0		0		ns
t _P	Clock Period		12		16		ns
t _W	Clock Width		6		8		ns
	External Feedback 1/(t _S + t _{CC})		68		45	
f _{MAX}	Internal Feedback 1/(t _S + t _{CF})			74		50	MHz
	No Feedback 1/(t _P)			83		62	
t _{EA}	Input to Output Enable — Product Term		3	10	3	15	ns
t _{ER}	Input to Output Disable — Product Term		2	10	2	15	ns
t _{PZX}	OE pin to Output Enable		2	10	2	15	ns
t _{PXZ}	OE pin to Output Disable		1.5	10	1.5	15	ns

Note: 1. See ordering information for valid part numbers and speed grades.

Figure 3-1. AC Waveforms^(3.6)

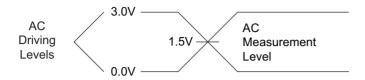


Note 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V 3.0V, unless otherwise specified.

3.6 Input Test Waveforms

3.6.1 Input Test Waveforms and Measurement Levels

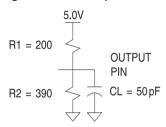
Figure 3-2. Input Test Waveforms and Measurement Levels



 t_R , $t_F < 5$ ns (10% to 90%)

3.6.2 Output Test Loads (Commercial)

Figure 3-3. Output Test Loads



C₁ includes Test fixture and Probe capacitance

3.7 Power-up Reset

The registers in the ATF16V8B(QL) are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

- 1. The V_{CC} rise must be monotonic,
- 2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
- 3. The clock must remain stable during t_{PR} .

Figure 3-4. Power-up Reset Waveforms

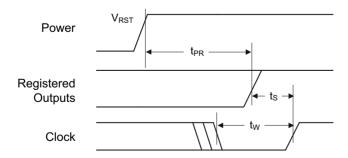




Table 3-5. Power-up Reset Parameters

Parameter	Description	Тур	Max	Units
t _{PR}	Power-up Reset Time	600	1,000	ns
V _{RST}	Power-up Reset Voltage	3.8	4.5	V

3.8 Preload of Registered Outputs

The ATF16V8B(QL) device registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

4. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8B(QL) fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

5. Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

6. Programming/Erasing

Programming/erasing is performed using standard PLD programmers.

7. Input and I/O Pull-ups

All ATF16V8B(QL) family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to V_{CC} . This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be over driven by TTL-compatible drivers (see input and I/O diagrams below).

Figure 7-1. Input Diagram

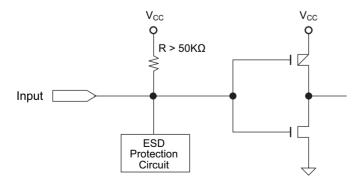
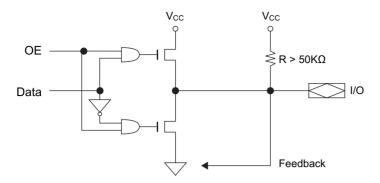




Figure 7-2. I/O Diagram



8. Functional Logic Diagram Description

The logic option and functional diagrams describe the ATF16V8B(QL) architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8B(QL) can be configured in one of three different modes. Each mode makes the ATF16V8B(QL) look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8B(QL) universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8B(QL) can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the content of the ATF16V8B(QL). Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the security fuse.

9. Software Support

Atmel WinCUPL is a free tool, available on Atmel's web site and can be used to design in all members of the ATF16V8B(QL) family of SPLDs. The below table lists the Atmel WinCUPL device mnemonics for the different macrocell configuration modes.

Table 9-1. Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
CUPL, Atmel WinCUPL	G16V8MS	G16V8MA	G16V8AS	G16V8



10. Macrocell Configuration

Software compilers support the three different OMC modes as different device types. Most compilers have the ability to automatically select the device type, generally based on the register usage and Output Enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode:

Registered Mode

Pin 1 and pin 11 are permanently configured as clock and output enable respectively. These pins cannot be configured as dedicated inputs in the registered mode.

Complex Mode

Pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

Simple Mode

All feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

10.1 ATF16V8B(QL) Registered Mode

PAL Device Emulation/PAL Replacement. The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the \overline{OE} pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

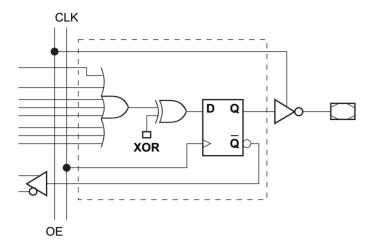
Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

- 16R8 •
- 16R616RP6

16RP8

16R416RP4

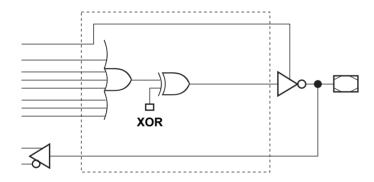
Figure 10-1. Registered Configuration for Registered Mode⁽¹⁾⁽²⁾



Notes: 1. Pin 1 controls common CLK for the registered outputs. Pin 11 controls common \overline{OE} for the registered outputs. Pin 1 and Pin 11 are permanently configured as CLK and \overline{OE} .

2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Figure 10-2. Combinatorial Configuration for Registered Mode⁽¹⁾⁽²⁾

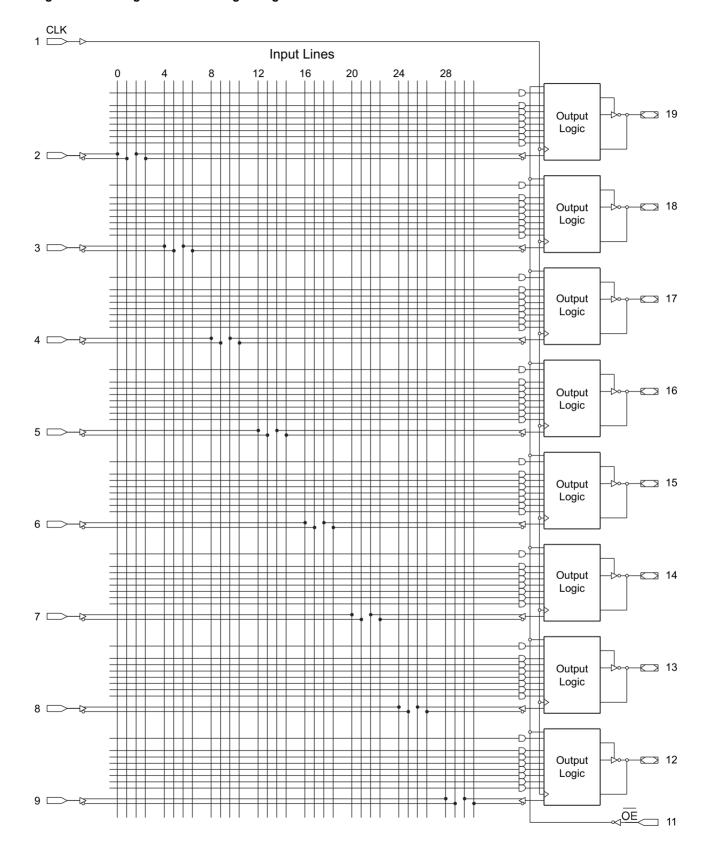


Notes: 1. Pin 1 and Pin 11 are permanently configured as CLK and \overline{OE} .

2. The development software configures all the architecture control bits and checks for proper pin usage automatically.



Figure 10-3. Registered Mode Logic Diagram



10.2 ATF16V8B(QL) Complex Mode

PAL Device Emulation/PAL Replacement. In the complex mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

- 16L8
- 16H8
- 16P8

Figure 10-4. Complex Mode Option

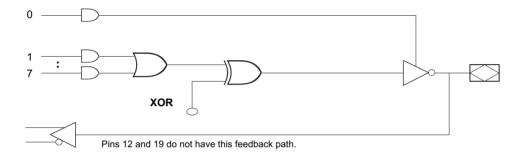
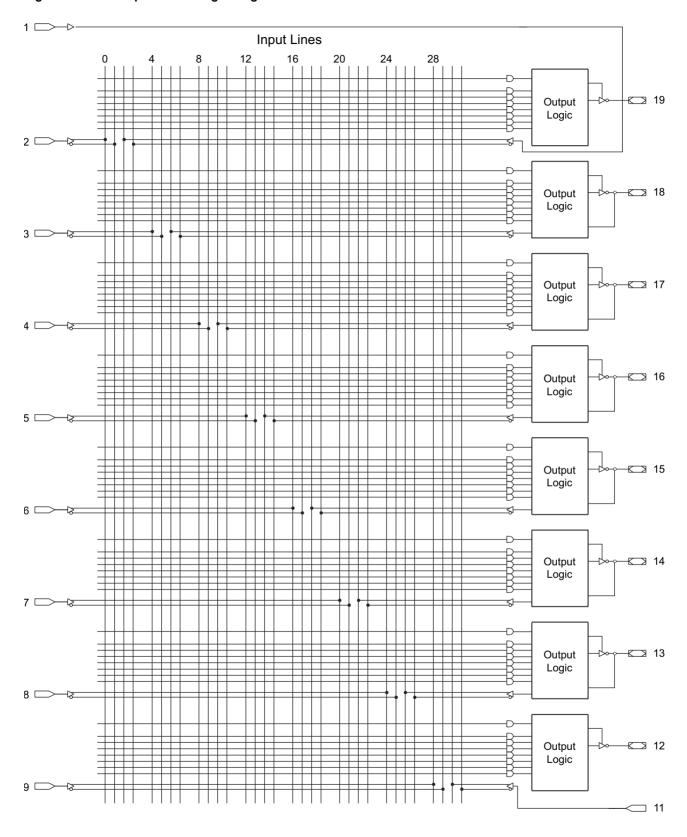




Figure 10-5. Complex Mode Logic Diagram



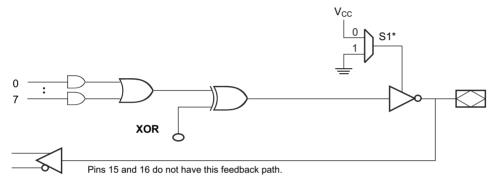
10.3 ATF16V8B(QL) Simple Mode

PAL Device Emulation/PAL Replacement. In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

•	10L8	•	10H8	•	10P8
•	12L6	•	12H6	•	12P6
•	14L4	•	14H4	•	14P4
•	16L2	•	16H2	•	16P2

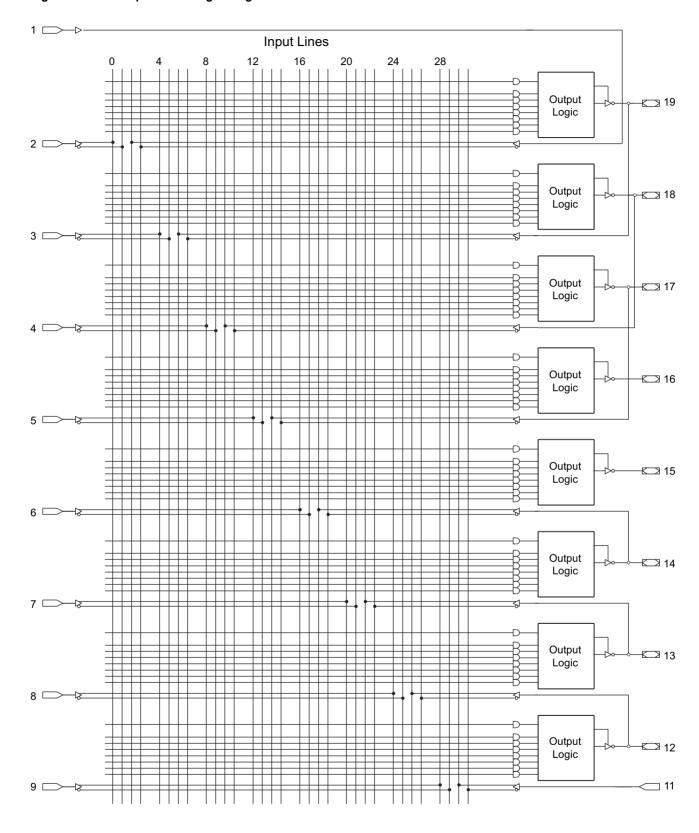
Figure 10-6. Simple Mode Option



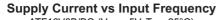
^{*} Pins 15 and 16 are always enabled.

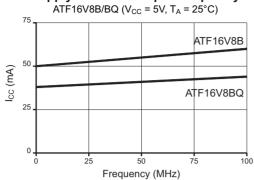


Figure 10-7. Simple Mode Logic Diagram

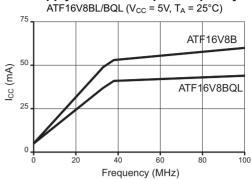


11. Test Characterization Data

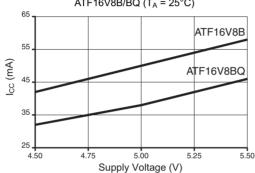




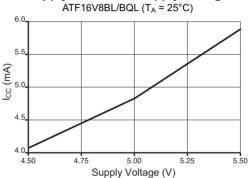
Supply Current vs Input Frequency



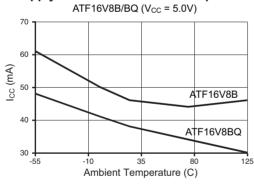
Supply Current vs Supply Voltage ATF16V8B/BQ (T_A = 25°C)



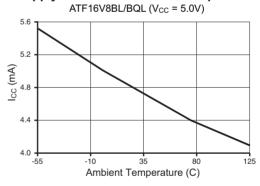
Supply Current vs Supply Voltage



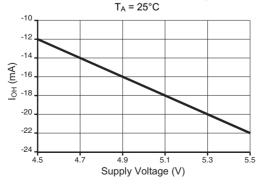
Supply Current vs Ambient Temperature



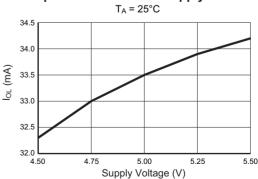
Supply Current vs Ambient Temperature



Output Source Current vs Supply Current

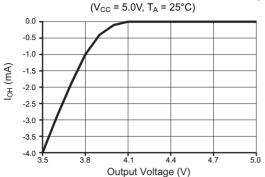


Output Sink Current vs Supply Current

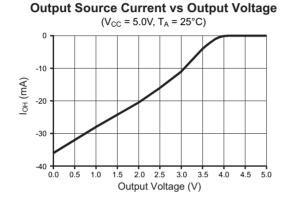




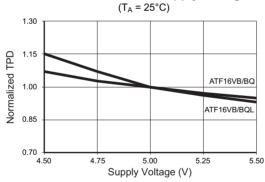
Output Source Current vs Outpute Voltage



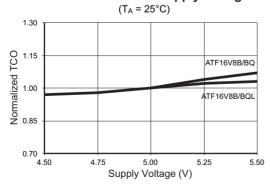
Output voltage (v)



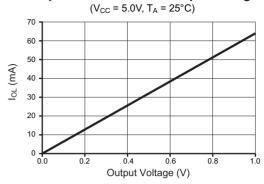
Normalized TPD vs Supply Voltage



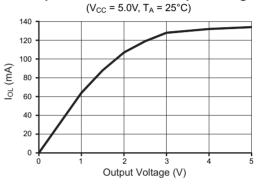
Normalized TCO vs Supply Voltage



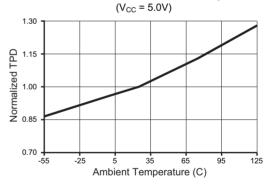
Output Sink Current vs Output Voltage



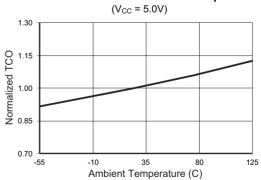
Output Sink Current vs Output Voltage



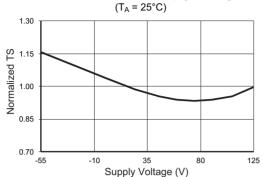
Normalized TPD vs Ambient Temperature



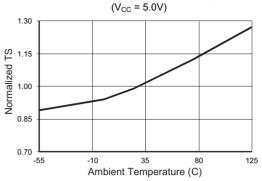
Normalized TCO vs Ambient Temperature



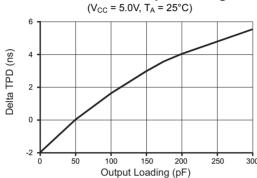
Normalized TS vs Supply Voltage



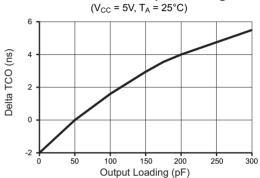
Normalized TS vs Ambient Temperature



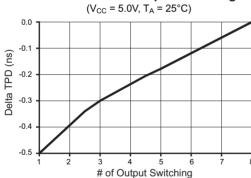
Delta TPD vs Output Loading



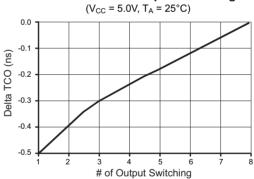
Delta TCO vs Output Loading



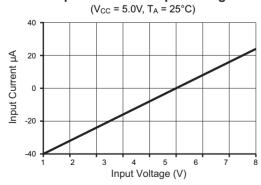
Delta TPD vs # Output Switching



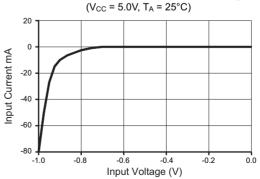
Delta TCO vs # Output Switching



Input Current vs Input Voltage



Input Clamp Current vs Input Voltage





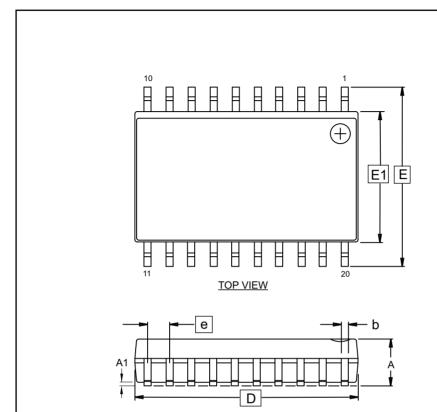
12. Ordering Information

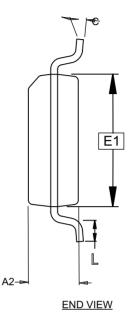
t _{PD} (ns)	t _s (ns)	t _{co} (ns)	Ordering Code	Package	Operation Range
10	7.5	7	ATF16V8B-10JU	20J	
	ATF16V8B-15XU 20X (Pb/Halide-fro	20S2	Industrial		
4.5		(Pb/Halide-free/RoHS Compliant)			
15		(-40°C to +85°C)			
			ATF16V8B-15JU	20J	
			ATF16V8BQL-15SU	20S2	
45	40	ATF16V8BQL-15XU 20X Industrial			
15	` ` ` ` ` ` ` ` ` ` ` ` ` ` ` ` ` ` `	(Pb/Halide-free/RoHS Compliant) (-40°C to +85°C)			
		ATF16V8BQL-15JU	ATF16V8BQL-15JU	20J	

	Package Type					
20S2	20-lead, 0.300" wide, Plastic Gull-wing Small Outline (SOIC)					
20X	20-lead, 4.4mm wide, Plastic Thin Shrink Small Outline (TSSOP)					
20P3	20-lead, 0.300" wide, Plastic Dual Inline Package (PDIP)					
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)					

13. Packaging Information

13.1 20S2 — 20-lead SOIC





Notes:

SIDE VIEW

- This drawing is for general information only. Refer to JEDEC Drawing MS-013, Variation AC, for proper dimensions, tolerances, datums, etc.
- Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrustions or gate burrs shall not exceed 0.15 mm per end.
 Diminsion E1 does not include interlead flash or protursion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
- 3. The package top may be smaller than the package bottom. Dimensions D and E1 are determinded at the outermost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- 4. The dimensions apply to the flat section of the lead between 0.10 to 0.25 mm from the lead tip.
- Dimension 'b' does not include the dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of the 'b' dimension at maximum material condition. The dambar may not be located on the lower radius of the foot.
- 'A1' is defined as the vertical distance from the seating plane to the lowest point on the package body excluding the lid or thermal enhancement on the cavity down package configuration.

COMMON DIMENSIONS (Unit of Measure = mm)

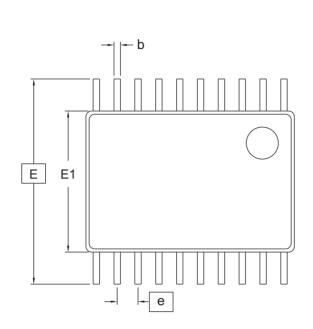
SYMBOL	MIN	NOM	MAX	NOTE
D	,	12.80 BS	SC .	2,3
E1		7.50 BS	С	2,3
E	Ì	10.30 BS	SC .	
А	ı	-	2.65	
A1	0.10	-	0.30	6
A2	2.05	-	-	
е				
b	0.31	-	0.51	4,5
L	0.40	-	1.27	
С	0.20	-	0.33	4

7/1/14

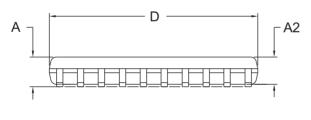
∕ltmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	20S2 , 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	SRJ	20\$2	Е



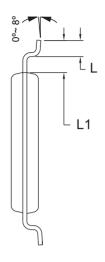
13.2 20X — 20-lead TSSOP



Top View



Side View



End View

COMMON DIMENSIONS (Unit of Measure = mm)

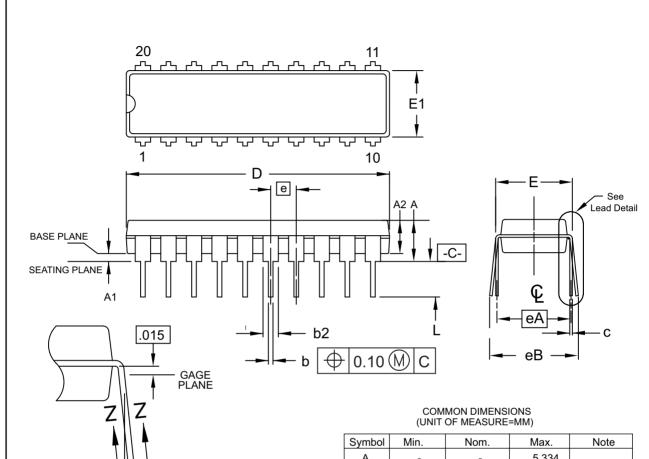
SYMBOL	MIN	NOM	MAX	NOTE
D	6.40	6.50	6.60	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
А	_	-	1.20	
A2	0.80	1.00	1.05	
b	0.19	-	0.30	4
е	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			

- Notes: 1. This drawing is for general information only. Please refer to JEDEC Drawing MO-153, Variation AC, for additional
 - 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
 - 3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
 - 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
 - 5. Dimension D and E1 to be determined at Datum Plane H.

09/26/11

∕ltmel	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	20X, 20-lead 4.4 x 6.5 mm Body, 0.65 mm Lead Pitch, Thin Shrink Small Outline Package (TSSOP)	TLN	20X	D

13.3 20P3 — 20-lead PDIP



Notes:

1. This package conforms to JEDEC reference MS-001, Variation AD.

-eC

Lead Detail

2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

	,		•	
Symbol	Min.	Nom.	Max.	Note
Α	-	-	5.334	
A1	0.381	-	•	
A2	2.921	3.302	4.953	
b	0.356	0.457	0.588	
b2	1.143	1.524	1.778	
С	0.203	0.254	0.356	
D	24.892	26.162	26.924	Note 2
E	7.620	7.874	8.255	
E1	6.096	6.350	7.112	Note 2
L	2.921	3.302	3.810	
е		2.54 BSC		
eA		7.62 BSC		
eB	-	-	10.922	
eC	0.000	-	1.524	

1/6/12

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Package Drawing Contact: packagedrawings@atmel.com TITLE

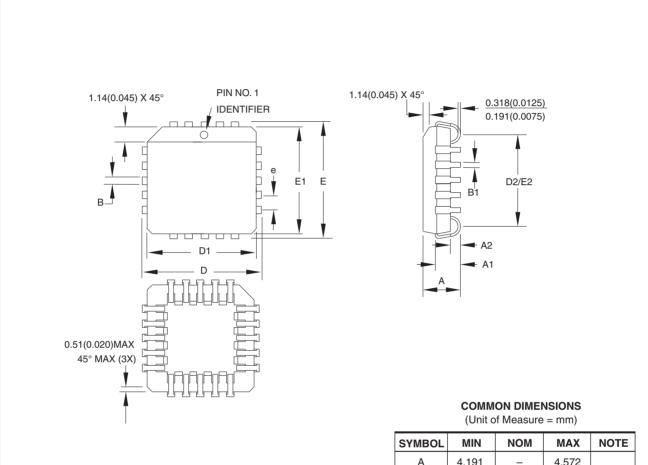
20P3, 20-lead, 0.300"/7.62 mm Wide Plastic Dual Inline Package (PDIP)

GPC	
PQD	

DRAWING NO. REV. F 20P3



13.4 20J — 20-lead PLCC



- Notes: 1. This package conforms to JEDEC reference MS-018, Variation AA
 - 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 - 3. Lead coplanarity is 0.004" (0.102mm) maximum

(OTHE OT MICAGAIC = ITHIT)				
SYMBOL	MIN	NOM	MAX	NOTE
Α	4.191	_	4.572	
A1	2.286	_	3.048	
A2	0.508	_	_	
D	9.779	_	10.033	
D1	8.890	_	9.042	Note 2
Е	9.779	_	10.033	
E1	8.890	_	9.042	Note 2
D2/E2	7.366	_	8.382	
В	0.660	_	0.813	
B1	0.330	_	0.533	
е	1.270 TYP			

10/04/01

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Package Drawing Contact: packagedrawings@atmel.com TITLE 20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC) DRAWING NO. | REV. 20J В

14. Revision History

Doc. Rev.	Date	Comments
0364K	07/2014	Removed ATF16V8BQ device and commercial options due to becoming obsolete. Updated package drawings to most current versions and the 20S to 20S2 package drawing. Updated template, Atmel logos, disclaimer page.
0364J	07/2005	Green Package options added in 2005.
	1999	ATF16V8B-25 JC/PC/SC/XC/JI/PI/SI/XI and ATF16V8BQL-25 JC/PC/SC/XC/JI/PI/SI/XI were obsoleted in August 1999 and removed from the datasheet.















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