APPLICATION NOTE

ATA6663/ATA6664 Development Board

ATA6663/ATA6664

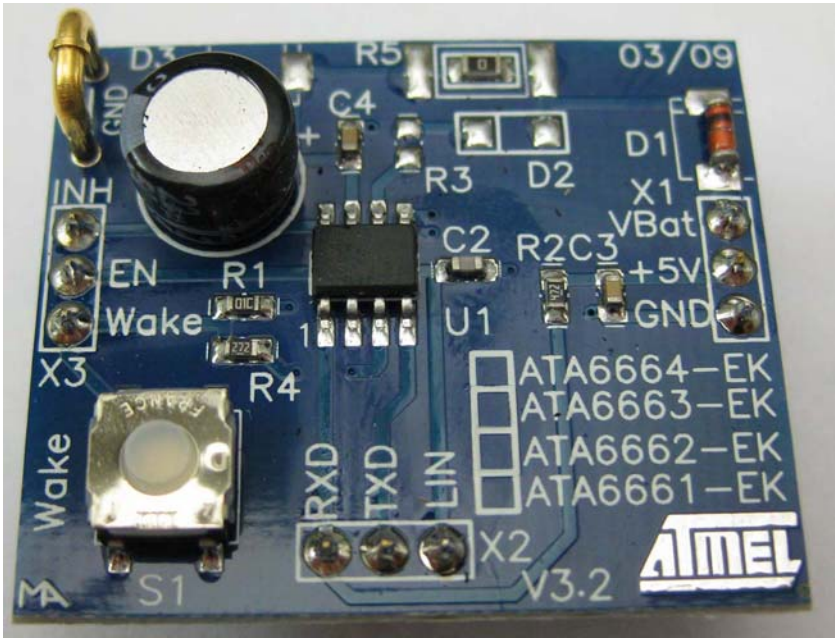
Introduction

The development board for the Atmel® ATA6663/ATA6664 (Atmel ATA6663-EK, ATA6664-EK) is designed to give users a quick start using these ICs and prototyping and testing new designs. The Atmel ATA6663/ATA6664 is a fully integrated LIN transceiver complying with the LIN 2.0, 2.1 specification and SAEJ2602-2. The devices are nearly identical, the only difference is that the TXD dominant timeout-timer is disabled at the Atmel ATA6664 so this device is able to send a static low signal on the LIN bus. The Atmel ATA6663 is the successor IC of the Atmel ATA6662 with an enhanced EMC performance and improved wake-up behavior resulting in a very low sleep mode current consumption even in the case of a floating bus or a short-circuit between the bus line and GND.

The ICs are the interface between the LIN protocol handler and the physical layer and is designed to handle the low-speed data communication in vehicles for example in convenience electronics. Improved slope control on the LIN bus ensures secure data communication of up to 20kBaud.

This document has been created as a quick start guide for using the development board of the Atmel ATA6663/ATA6664. Please refer to the corresponding datasheet for more detailed information about the Atmel ATA6663/ATA6664 itself.

Figure 1. Atmel ATA6663/ATA6664 Development Board



Development Board Features

The development board for the Atmel® ATA6663/ATA6664 supports the following features:

- Includes all components necessary for Atmel ATA6663/ATA6664 operation
- All pins are easily accessible
- Can be used for master or slave operation
- Wake-up pulse via an on-board switch

Quick Start

The development board for the Atmel ATA6663/ATA6664 is shipped with all components necessary to immediately start the development of a LIN slave node.

Connecting an external 12V DC power supply between the terminals VBAT and GND puts the IC in fail-safe mode. In this mode, the INH pin is switched to the VS level which can be used to enable an external voltage regulator (not included on the board). The LIN pin is in the recessive state.

Please note that the communication is still inactive during fail-safe mode.

To communicate via the LIN bus interface, you have to switch the device into normal mode by applying a high level (for example 5V) at pin EN.

As RXD is an open-drain output, the required pull-up resistor R2 can be activated by applying +5V DC voltage, on the designated pin on the board.

1. Hardware Description

In the following sections only the normal operating conditions are described. Refer to the corresponding datasheet for detailed information about the features mentioned.

1.1 Power Supply (VBAT, +5V and GND)

The development board requires an external 5.7V to 27V DC power supply between the terminals VBAT and GND. The input circuit is protected against inverse polarity with the protection diode D1, resulting in a difference between the VBAT and VS level of approximately 0.7V.

The DC voltage at pin +5V is only required for activating the pull-up resistor for the pin RXD.

1.2 LIN Interface (LIN, TXD and RXD)

1.2.1 Bus Pin (LIN)

A low-side driver with internal current limitation, thermal shutdown, and an internal pull-up resistor in compliance with LIN spec 2.x is implemented. The internal pull-up resistor is active in normal and fail-safe mode. The LIN receiver thresholds are compatible with the LIN protocol specification. The reverse current from the LIN bus to Vs is <2µA, even when Vbat is disconnected.

At a short circuit between LIN and $V_{Battery}$, the output limits the output current. Due to the power dissipation, the chip temperature exceeds the overtemperature threshold and the LIN output is switched off. The chip cools down and after the temperature hysteresis the output switches on again. RXD stays high because LIN is high.

On the board the LIN pin is assembled with a 220pF capacitor to ground. Additionally, the two extra components diode D2 (LL4148) in series with resistor R3 (1kΩ) required for using the development board for a LIN master application have designated placeholders for convenient mounting.

1.2.2 Input/Output Pin (TXD)

In normal mode the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be low in order to have a low LIN bus (dominant state). The TXD pin has an internal pull-down resistor. If TXD is high, the LIN output transistor is turned off and the bus is in the recessive state. If TXD is low, the LIN output transistor is turned on and the bus is in the dominant state.

An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 27ms, the LIN pin is switched off (recessive mode). To reset this mode, TXD needs to be switched to high (>10µs) before switching LIN to dominant again. This feature is disabled in the ATA6664, meaning this device is able to send a static low to the bus and is therefore highly suitable for very low data rates.

During fail-safe mode the TXD pin is used as an output and signals the wake-up source if an external pull-up resistor is connected. The TXD output transistor is current limited to <8mA.

1.2.3 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD, LIN low (dominant state) is indicated by a low level at RXD. The output is an open drain, therefore it is compatible with a 3.3V or 5V power supply. The output is short circuit protected.

Please note that the ATA6663/ATA6664 has to be in normal mode in order to have the communication via LIN enabled.

After a wake-up the device is in fail-safe mode and the RXD pin switches to low in order to interrupt the microcontroller.

1.3 System Control (EN, INH and WAKE)

1.3.1 Enable Pin (EN)

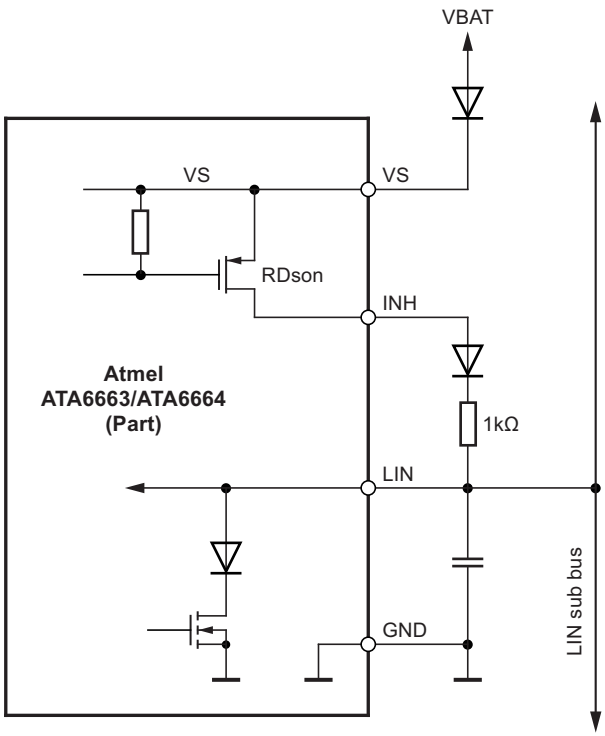
This pin controls the operating mode of the interface. If EN = 1, the interface is in normal mode with transmission paths from TXD to LIN and from LIN to RXD both active. After a falling edge on EN while TXD is set to high, the device switches to sleep mode, no transmission is possible anymore, and the LIN pin is pulled to VS by a weak current source.

During sleep mode the device is still supplied from the battery voltage with the supply current of typically 10µA. The pin EN provides a pull-down resistor in order to force the transceiver into sleep mode for fail-safe reasons in the case of an unconnected EN line.

1.3.2 Inhibit Pin (INH)

This pin is a high-side switch to VS and it is intended to be used to control an external voltage regulator or to switch the LIN master pull-up resistor on/off in case the device is used in a master node (see Figure 1-1). The output transistor is protected by internal temperature monitoring. If the device is in normal or in fail-safe mode, the inhibit high-side switch is turned on, in sleep mode it is turned off.

Figure 1-1. Switching the LIN Master Pull-up Resistor by the INH Output



With this measure the current consumption in the case of a short circuit between LIN and GND can be reduced to a minimum, because the Atmel ATA6663/ATA6664 can be switched into sleep mode and therefore the INH output is off.

A wake-up event on the LIN bus (remote wake-up) or at the pin wake (local wake-up) switches the IC into fail-safe mode in which the INH output is on. The same happens after a system power-up.

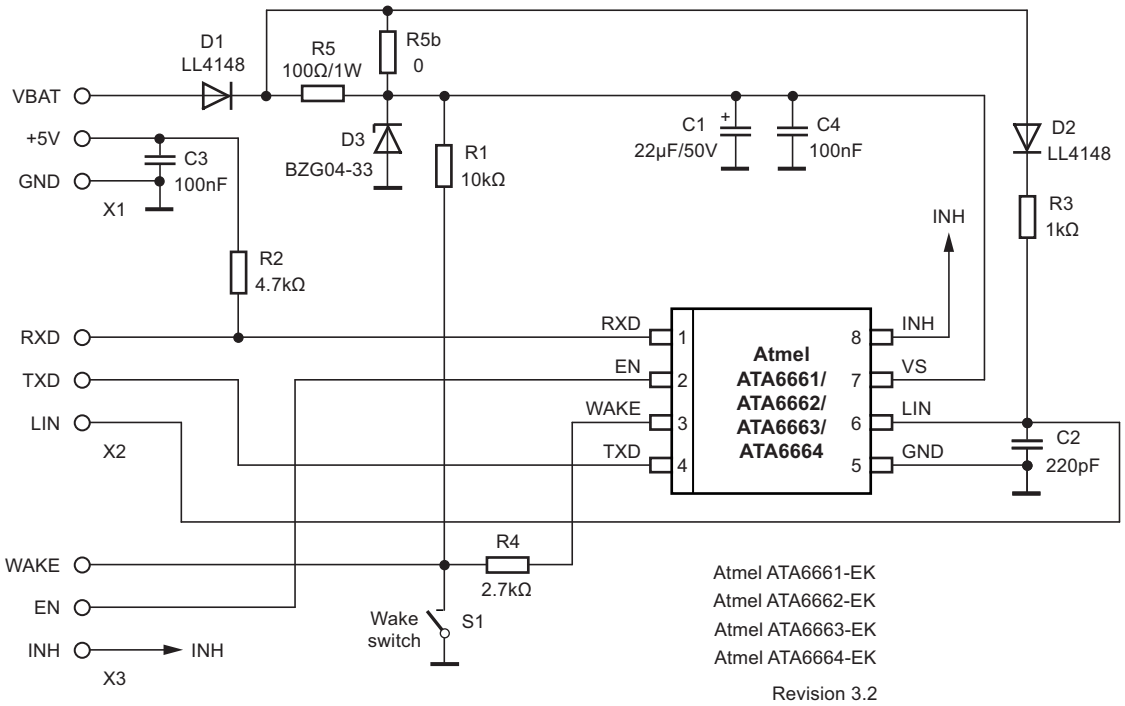
1.3.3 Wake Pin (WAKE)

This pin is a high voltage input used to wake up the device from sleep mode. It is usually connected to an external switch in order to generate a local wake-up. A pull-up current source with typically –10µA is implemented as well as a debounce timer. On the development board there is the push button S1 to generate a local wake-up by pulling the WAKE pin to GND. The resistor R4 = 2.7kΩ is needed to limit the input current in the case of voltage transients.

Even if the WAKE pin is pulled to GND, it is possible to switch the IC into sleep mode. If no local wake-up is required for the application, the WAKE pin can be connected directly to the VS pin.

2. Schematic and Layout of the Atmel ATA6663/ATA6664 Development Board

Figure 2-1. Schematic of the Development Board for the Atmel ATA6663/ATA6664



Notes: 1. D2 and R3 are only required for a master node.
2. R5 and D3 are not used, R5b is 0Ω.

Figure 2-2. Board Component Placement; Top Side, Top View

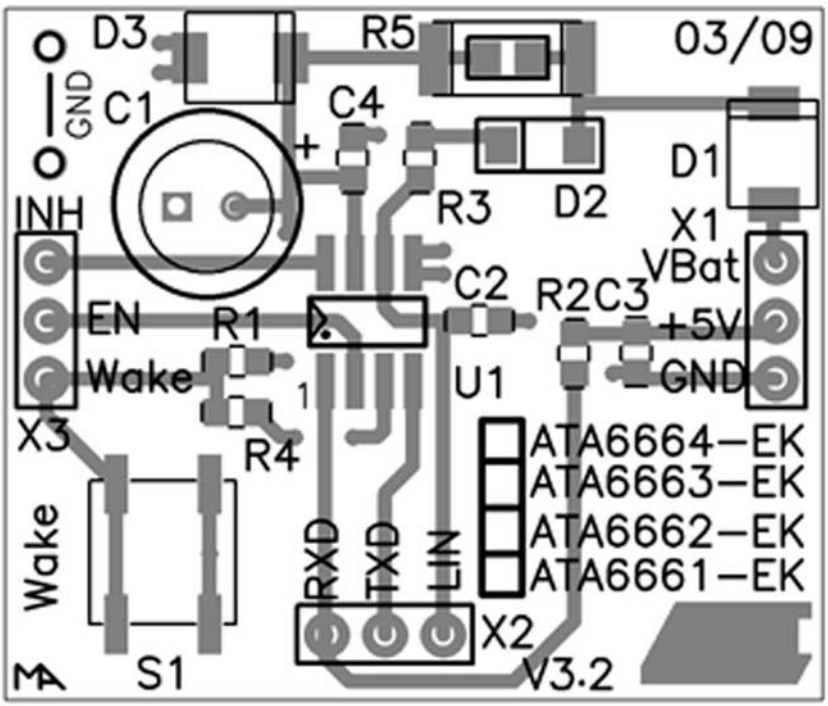


Figure 2-3. Atmel ATA6663/ATA6664 Development Board; Top Side, Top View

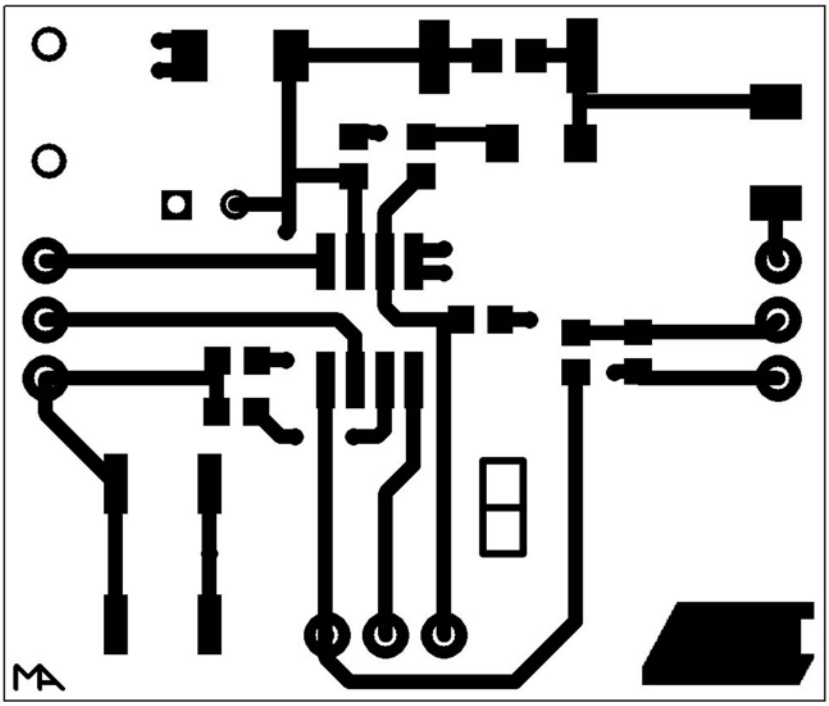
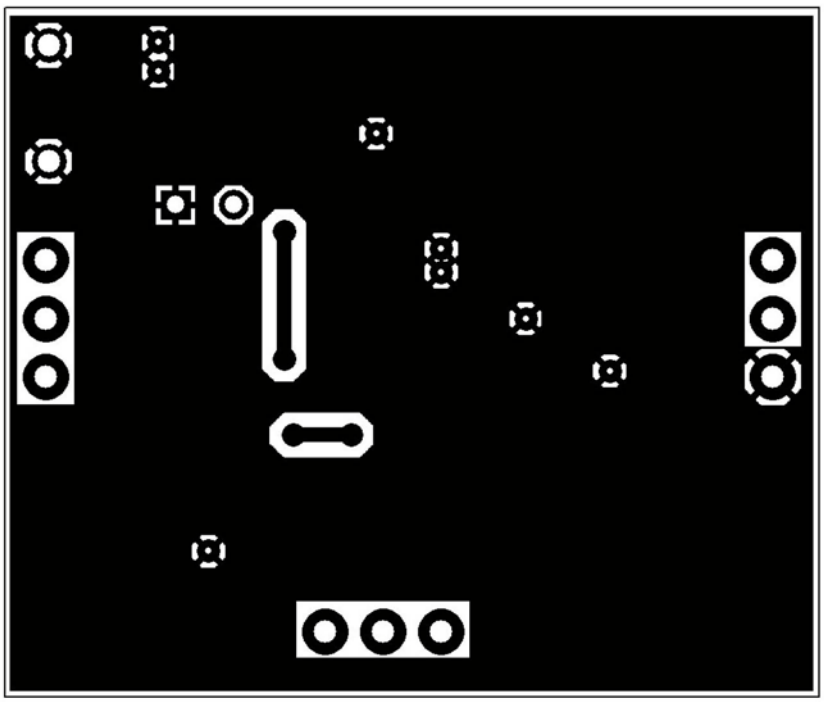


Figure 2-4. Atmel ATA6663/ATA6664 Development Board; Bottom Side, Top View (Transparent PCB View)



3. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9201B-AUTO-06/15	• Put document in the latest template

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