



ATWINC3400A-MU

ATWINC3400A-MU IEEE® 802.11 b/g/n Network Controller with Integrated Bluetooth® SoC

Introduction

The Microchip ATWINC3400 is an IEEE 802.11 b/g/n RF/Baseband/Medium Access Control (MAC) network controller with Bluetooth Low Energy. It is Bluetooth 5.0 certified and optimized for low-power and high-performance applications. The ATWINC3400 radio features fully integrated Power Amplifier (PA), Low Noise Amplifier (LNA), Switch, Power Management Unit (PMU) and integrated Flash memory for system software. The ATWINC3400 offers high integration and minimal bill of materials thereby reducing system cost. The ATWINC3400 external clock sources needed are a high-speed crystal or oscillator with 26 MHz, and a 32.768 kHz clock for sleep operation. The ATWINC3400 is available in small, 6*6mm QFN packaging.

The ATWINC3400 utilizes highly optimized IEEE 802.11 and Bluetooth coexistence protocols, and provides a Serial Peripheral Interface (SPI) to interface with the host controller.

Features

Wi-Fi® Features:

- IEEE 802.11 b/g/n with Single Spatial Stream (1x1), 2.4 GHz ISM Band
- Integrated PA and T/R Switch
- Superior Sensitivity and Range via Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Supports Soft-AP
- Supports IEEE 802.11 WEP, WPA, and WPA2 Personal and WPA2 Enterprise (firmware v. 1.3.1 or later)
- Superior MAC Throughput through Hardware Accelerated Two-Level A-MSDU/A-MPDU Frame Aggregation and Block Acknowledgment
- On-Chip Memory Management Engine to Reduce the Host Load
- Operating Temperature Range from -40°C to +85°C
- SPI Host Interface
- Integrated Flash Memory for Wi-Fi and Bluetooth System Software
- Low Leakage On-Chip Memory for State Variables
- Fast AP Re-Association (150 ms)
- On-Chip Network Stack to Offload Host MCU
 - Network Features: TCP, UDP, DHCP, ARP, HTTP, TLS, DNS, and SNTP

Bluetooth Features:

- Bluetooth Low Energy 5.0
- Adaptive Frequency Hopping (AFH)
- Superior Sensitivity and Range

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1. Ordering Information and IC Marking

The following table provides the ordering details for the ATWINC3400.

Table 1-1. Ordering Details

Ordering Code	Package Type	Package Size	IC Marking
ATWINC3400A-MU-ABCD	QFN in Tray, Tape and Reel	6 mm x 6 mm	ATWINC3400A

Note:

1. ABCD interprets as:
"A" can be "Y" indicating Tray or "T" indicating Tape and Reel.
"BCD" equals to "042" for part assigned with a MAC ID and blank for part with no MAC ID.
The following table lists the possible combinations for ordering the ATWINC3400A.

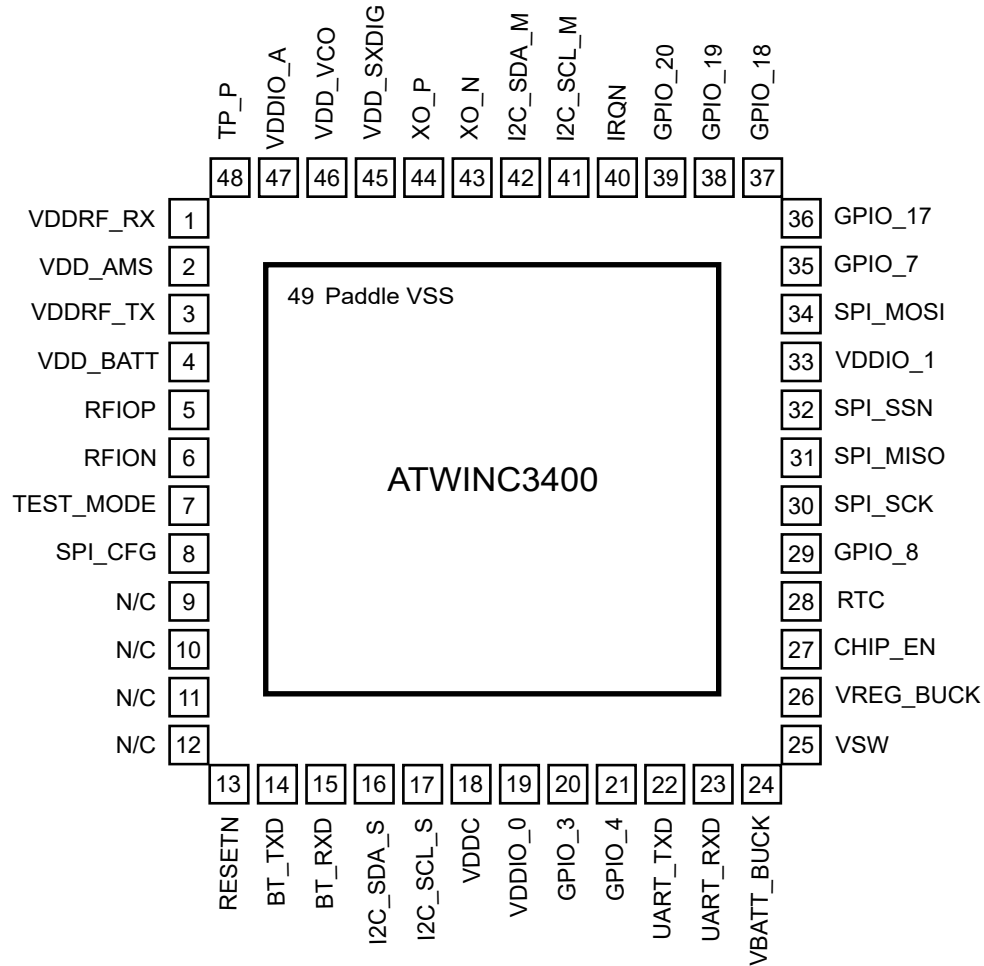
Table 1-2.

Ordering Code	Description
ATWINC3400A-MU-T	No MAC ID and ship in Tape and Reel
ATWINC3400A-MU-T042	MAC ID assigned and ship in Tape and Reel
ATWINC3400A-MU-Y	No MAC ID and ship in Tray
ATWINC3400A-MU-Y042	MAC ID assigned and ship in Tray

2.2 Pinout Information

ATWINC3400 is offered in an exposed pad 48-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in following figure.

Figure 2-2. ATWINC3400 Pin Assignment



2.3 Pinout Description

The ATWINC3400 pins with default peripheral mapping are described in the following table.

Table 2-1. ATWINC3400 Pin Description

Pin Number	Pin Name	Pin Type	Description
1	VDDRF_RX	Power	Tuner RF RX Supply
2	VDD_AMS	Power	Tuner BB Supply
3	VDDRF_TX	Power	Tuner RF TX Supply
4	VDD_BATT	Power	Battery Supply for PA
5	RFIOP	Analog	Wi-Fi/BLE Pos RF Differential I/O
6	RFION	Analog	Wi-Fi/BLE Neg RF Differential I/O

.....continued

Pin Number	Pin Name	Pin Type	Description
7	TEST_MODE	Digital Input	Test Mode – Tie to GND
8	SPI_CFG	Digital Input	Tie to VDDIO through 1 MΩ resistor for selecting SPI interface
9	N/C	-	Not Connected
10	N/C	-	Not Connected
11	N/C	-	Not Connected
12	N/C	-	Not Connected
13	RESETN	Digital Input	<ul style="list-style-type: none"> Active-Low Hard Reset pin When the Reset pin is asserted low, the module is in the Reset state. When the Reset pin is asserted high, the module functions normally This pin must connect to a host output that is low by default on power-up. If the host output is tri-stated, add a 1 MΩ pull down resistor to ensure a low level at power-up
14	BT_TXD	Digital I/O, Programmable Pull-Up	<ul style="list-style-type: none"> Bluetooth UART Transmit Data Output pin Used only during debug for DTM interface. SPI is the data and control interface with host microcontroller It is recommended to add a test point for this pin
15	BT_RXD	Digital I/O, Programmable Pull-Up	<ul style="list-style-type: none"> Bluetooth UART Receive Data Input pin Used only during debug for DTM interface. SPI is the data and control interface with host microcontroller It is recommended to add a test point for this pin
16	I2C_SDA_S	Digital I/O, Programmable Pull-Up	<ul style="list-style-type: none"> I2C Slave Data pin Used only for test purposes. It is recommended to add a test point for this pin
17	I2C_SCL_S	Digital I/O, Programmable Pull-Up	<ul style="list-style-type: none"> I2C Slave Clock pin Used only for test purposes. It is recommended to add a test point for this pin
18	VDDC	Power	Digital Core Power Supply
19	VDDIO_0	Power	Digital I/O Power Supply

.....continued

Pin Number	Pin Name	Pin Type	Description
20	GPIO_3	Digital I/O, Programmable Pull-Up	GPIO_3 ⁽¹⁾
21	GPIO_4	Digital I/O, Programmable Pull-Up	GPIO_4 ⁽¹⁾
22	UART_TXD	Digital I/O, Programmable Pull-Up	<ul style="list-style-type: none"> • Wi-Fi UART TXD Output pin • Used only for debug development purposes. It is recommended to add a test point for this pin
23	UART_RXD	Digital I/O, Programmable Pull-Up	<ul style="list-style-type: none"> • Wi-Fi UART RXD Input pin • Used only for debug development purposes. It is recommended to add a test point for this pin
24	VBATT_BUCK	Power	Battery Supply for DC Converter
25	VSW	Power	Switching Output of DC Converter
26	VREG_BUCK	Power	Core Power from DC Converter
27	CHIP_EN	Analog	<ul style="list-style-type: none"> • PMU Enable pin • When the CHIP_EN pin is asserted high, the module is enabled. When the CHIP_EN pin is asserted low, the module is disabled or put into Power-Down mode • Connect to a host output that is low by default at power-up. If the host output is tri-stated, add a 1 MΩ pull down resistor if necessary to ensure a low level at power-up
28	RTC	Digital I/O, Programmable Pull-Up	<ul style="list-style-type: none"> • RTC Clock Input pin • This pin must connect to a 32.768 kHz clock source.
29	GPIO8	Digital I/O, Programmable Pull-Up	GPIO_8 ⁽¹⁾
30	SPI_SCK	Digital I/O, Programmable Pull-Up	SPI Clock
31	SPI_MISO	Digital I/O, Programmable Pull-Up	SPI MISO (Master In Slave Output) pin
32	SPI_SSN	Digital I/O, Programmable Pull-Up	SPI Slave Select
33	VDDIO_1	Power	Digital I/O Power Supply
34	SPI_MOSI	Digital I/O, Programmable Pull-Up	SPI MOSI (Multiple Output Slave Input) pin
35	GPIO7	Digital I/O, Programmable Pull-Up	GPIO_7 ⁽¹⁾
36	GPIO_17	Digital I/O, Programmable Pull-Down	GPIO_17 ⁽¹⁾
37	GPIO_18	Digital I/O, Programmable Pull-Down	GPIO_18 ⁽¹⁾
38	GPIO_19	Digital I/O, Programmable Pull-Down	GPIO_19 ⁽¹⁾
39	GPIO_20	Digital I/O, Programmable Pull-Down	GPIO_20 ⁽¹⁾

.....continued			
Pin Number	Pin Name	Pin Type	Description
40	IRQN	Digital I/O, Programmable Pull-Up	<ul style="list-style-type: none"> ATWINC3400A Module Host Interrupt Request Output pin This pin must connect to a host interrupt pin
41	I2C_SCL_M	Digital I/O, Programmable Pull-Up	I2C Mater Clock Pin
42	I2C_SDA_M	Digital I/O, Programmable Pull-Up	I2C Master Data Pin
43	XO_N	Analog	Crystal Oscillator N
44	XO_P	Analog	Crystal Oscillator P
45	VDD_SXDIG	Power	SX Power Supply
46	VDD_VCO	Power	VCO Power Supply
47	VDDIO_A	Power	Tuner VDDIO Power Supply
48	TP_P	Analog	Test Pin, leave unconnected
49	PADDLE VSS	Power	Connect to System Board Ground

Note:

- Usage of the GPIO functionality is not supported by the FW. The data sheet is updated once support for this feature is added.

2.4 Package Description

The following table provides the physical details of ATWINC3400 devices.

Table 2-2. ATWINC3400 QFN Package Information

Parameter	Value	Units	Tolerance
Package Size	6 x 6	mm	±0.1 mm
QFN Pad Count	48	-	-
Total Thickness	0.85	mm	+0.15 mm/-0.05 mm
QFN Pad Pitch	0.40	mm	-
Pad Width	0.20	mm	±0.05 mm
Exposed Pad size	4.7 x 4.7	mm	-

For drawing details, refer to [11. Package Outline Drawing](#)

3. Clocking

This section details the clocking sources of the ATWINC3400.

3.1 Crystal Oscillator

The following table provides the values of the ATWINC3400 crystal oscillator parameters.

Table 3-1. Crystal Oscillator Parameters

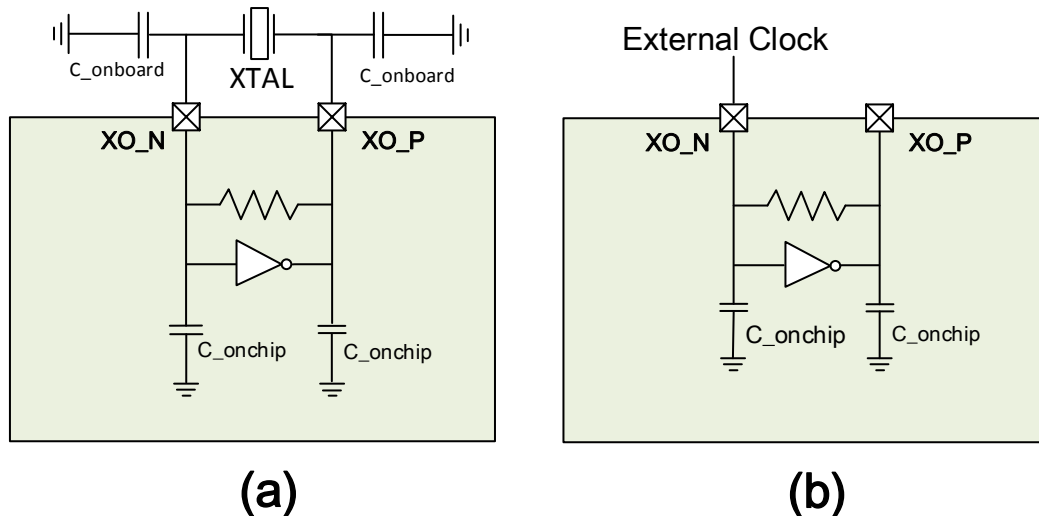
Parameter	Min.	Typ.	Max.	Unit
Crystal Resonant Frequency	-	26	-	MHz
Crystal Equivalent Series Resistance	-	50	-	Ohm
Stability - Initial Offset ¹	-100	-	100	ppm
Stability - Temperature and Aging	-25	-	25	ppm

Note: 1. Initial Offset must be calibrated to maintain ± 25 ppm in all operating conditions. This calibration is performed during final production testing.

The block diagram in the following figure (a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal. The XO has 5 pF internal capacitance on each terminal XO_P and XO_N. To bypass the crystal oscillator with an external reference, an external signal capable of driving 5 pF can be applied to the XO_N terminal as shown in figure (b).

The XO has 5 pF internal capacitance on each terminal XO_P and XO_N. This internal capacitance must be considered when calculating the external loading capacitance, c_{onboard} , for the XTAL.

Figure 3-1. ATWINC3400 XO Connections



The following table specifies the electrical and performance requirements for the external clock.

Table 3-2. Bypass Clock Specification

Parameter	Min.	Typ.	Max.	Unit	Comments
Oscillator frequency	-	26	-	MHz	Must drive 5 pF load at desired frequency
Voltage swing	0.5	-	1.2	V _{PP}	Must be AC coupled
Stability - Temperature and Aging	-25	-	+25	ppm	-
Phase Noise	-	-	-130	dBc/Hz	At 10 kHz offset
Jitter (RMS)	-	-	<1psec	psec	Based on integrated phase noise spectrum from 1 kHz to 1 MHz

3.2 Low-Power Oscillator

The ATWINC3400 requires an external 32.768 kHz clock to be used for sleep operation, which is provided through pin 28. The frequency accuracy of this external clock must be within ± 200 ppm. For Bluetooth Low Energy, an external oscillator is required for the Power Save mode, whereas on the Wi-Fi Power Save modes, software is used to switch between internal and external clock during boot-up.

4. CPU and Memory Subsystem

This chapter describes the Cortus APS3 32-bit processor and memory subsystem of the ATWINC3400.

4.1 Processor

The ATWINC3400 has two Cortus APS3 32-bit processors; one is used for Wi-Fi and the other is used for Bluetooth. In IEEE 802.11 mode, the processor performs many of the MAC functions, including but not limited to: association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes. In Bluetooth mode, the processor handles multiple tasks of the Bluetooth protocol stack.

4.2 Memory Subsystem

The APS3 core uses a 256 KB instruction/boot ROM (160 KB for IEEE 802.11 and 96 KB for Bluetooth) along with a 420 KB instruction RAM (128 KB for IEEE 802.11 and 292 KB for Bluetooth), and a 128 KB data RAM (64 KB for IEEE 802.11 and 64 KB for Bluetooth). In addition, the device uses a 160 KB shared/exchange RAM (128 KB for IEEE 802.11 and 32 KB for Bluetooth), accessible by the processor and MAC, which allows the processor to perform various data management tasks on the Tx and Rx data packets.

4.3 Nonvolatile Memory (eFuse)

The ATWINC3400A devices have 768 bits of nonvolatile eFuse memory that can be read by the CPU after device reset. The eFuse is partitioned into six 128-bit banks (Bank 0 - Bank 5). Each bank has the same bitmap (see the following figure). The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general purpose software dependent bits, or reserved for future use. Currently, the Bluetooth address is derived from the Wi-Fi MAC address such that Bluetooth address = Wi-Fi MAC address + 1.

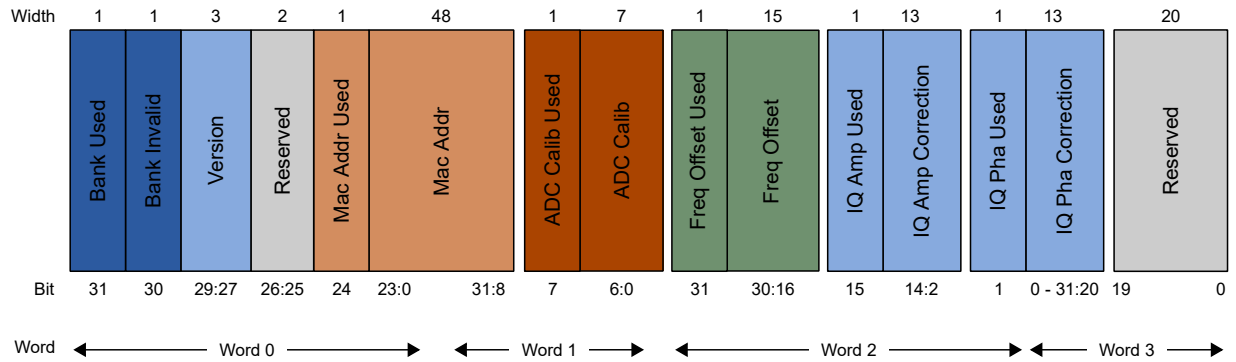
Note that Bank 0 and Bank 1 should be skipped for programming, i.e., Bank 0 and Bank 1 must not be programmed with any values and only *Bank Invalid* bit has to be programmed. This non-volatile One-Time Programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming; for example, if the MAC address is currently programmed in Bank 3 and MAC address has to be changed, the below steps would have to be followed:

1. Contents of Bank 3 has to be invalidated by programming *Bank Invalid* bit.
2. Bank 4 has to be programmed with the new MAC address along with the values of *ADC Calib* (if used from bank 3), *frequency offset* (from bank 3), *IQ Amp correction* (from bank 3) and *IQ Pha correction* (from bank 3) and programmed. The used bit field for the corresponding bit field should also be programmed.
3. Contents of Bank 4 has to be validated by programming the Bank used bit field of Bank 4.

By default, all the ATWINC3400A devices are programmed with IQ Amp and IQ Phase fields of Bank 2.

In IC variants, where MAC address is assigned, the MAC address bit field is programmed in Bank 2. Refer [1. Ordering Information and IC Marking](#) for more information.

Figure 4-1. Bitmap for ATWINC3400A eFuse Bank



Note: The bit map has been updated with bit fields IQ Amp correction and IQ Pha Correction fields from FW version 1.4 onwards. Previously these bit fields were reserved for future use. For customers using FW older than 1.4, IQ Amp correction and IQ Pha Correction bit fields will not be used by the FW.

5. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC), and Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

5.1 MAC

The ATWINC3400 MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

The dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, a Frame Check Sequence (FCS) engine checks the Cyclic Redundancy Check (CRC) of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, and WPA2 CCMP-AES security requirements.

The Control functions, which have real-time requirements, are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability through the processor. Examples of hardwired control logic modules are:

- The channel access control module: implements EDCA/HCCA, Beacon Tx control, interframe spacing, and so on
- Protocol timer module: responsible for the Network Access vector, back-off timing, timing synchronization function, and slot management
- MAC Protocol Data Unit (MPDU) handling module, aggregation/de-aggregation module, and block ACK controller: implements the protocol requirements for burst block communication
- Tx/Rx control Finite State Machine (FSM): coordinates data movement between PHY and MAC interface, cipher engine, and the Direct Memory Access (DMA) interface to the Tx/Rx FIFOs

The following are the characteristics of MAC functions implemented solely in software on the microprocessor:

- Functions with high memory requirements or complex data structures. Examples include association table management and power-save queuing
- Functions with low computational load or without critical real-time requirements. Examples include authentication and association
- Functions that require flexibility and upgradeability. Examples include beacon frame processing and QoS scheduling

5.1.1 Features

The ATWINC3400 IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- Advanced IEEE 802.11n Features:
 - Transmission and reception of aggregated MPDUs (A-MPDU)
 - Transmission and reception of aggregated MSDUs (A-MSDU)
 - Immediate block acknowledgment
 - Reduced Interframe Spacing (RIFS)
- IEEE 802.11i and WPA Security with Key Management:
 - WEP 64/128
 - WPA-TKIP
 - 128-bit WPA2 CCMP (AES)
- Advanced Power Management:
 - Standard IEEE 802.11 Power Save mode

- RTS-CTS and CTS-Self Support
- Either STA or AP Mode in the Infrastructure Basic Service Set Mode

5.2 PHY

The ATWINC3400 WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in Single Stream mode with 20 MHz bandwidth. The advanced algorithms are used to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as Fast Fourier Transform (FFT), filtering, Forward Error Correction (FEC) that is a Viterbi decoder, frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

5.2.1 Features

The IEEE 802.11 PHY supports the following functions:

- Single Antenna 1x1 Stream in 20 MHz Channels
- Supports IEEE 802.11b DSSS-CCK Modulation: 1, 2, 5.5, and 11 Mbps
- Supports IEEE 802.11g OFDM Modulation: 6, 9, 12, 18, 24, 36, 48, and 54 Mbps
- Supports IEEE 802.11n HT Modulations MCS0-7, 20 MHz, 800 and 400 ns Guard Interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2 Mbps⁽¹⁾
- IEEE 802.11n Mixed Mode Operation
- Per Packet Tx Power Control
- Advanced Channel Estimation/Equalization, Automatic Gain Control, CCA, Carrier/Symbol Recovery and Frame Detection

Note:

1. Short GI is currently not supported by Firmware. The datasheet will be updated when the feature is supported.

6. Bluetooth Low Energy

The Bluetooth subsystem implements all the mission critical real-time functions. It encodes/decodes HCI packets, constructs baseband data packages; and manages and monitors the connection status, slot usage, data flow, routing, segmentation, and buffer control. The Bluetooth subsystem supports Bluetooth Low Energy modes of operation.

Coexistence Mechanism

The ATWINC3400 supports simultaneous usage of both Bluetooth Low Energy and Wi-Fi via a coexistence mechanism that allows the protocols to share the same radio. The radio defaults to Wi-Fi usage until a Bluetooth Low Energy event occurs (such as connection or advertising), in which case the radio is gracefully switched over for Bluetooth Low Energy use. For the duration of the Bluetooth Low Energy event, the radio is switched back and forth between Wi-Fi and Bluetooth Low Energy as demanded by the Bluetooth Low Energy activity, before returning to Wi-Fi until the next Bluetooth Low Energy event.

7. Radio

This section describes the properties and characteristics of the ATWINC3400 and Wi-Fi radio transmit and receive performance capabilities of the IC.

The performance measurements are taken after RF matching network; the RF performance is assured for room temperature of 25°C with a derating of 2-3 dB at boundary conditions.

Measurements were taken under typical conditions: VBATT=3.3V; VDDIO=3.3V; temperature: +25°C

Table 7-1. Features and Properties

Feature	Radio	Description
Part Number	-	ATWINC3400
Standard	Wi-Fi	IEEE 802.11 b/g/n, Wi-Fi Compliant
	Bluetooth	Bluetooth 5.0 Compliant
Host Interface	-	SPI
Dimension	-	6 x 6 x 0.85 mm
Number of channels	Wi-Fi	11 for North America and 13 for Europe and Japan
	Bluetooth	40
Modulation	Wi-Fi	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM /64-QAM, 16-QAM, QPSK, BPSK
	Bluetooth	GFSK
Data Rate	Wi-Fi	802.11b: 1, 2, 5.5, 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
	Bluetooth	1 Mbps
Data Rate (20 MHz, normal GI, 800 ns)	Wi-Fi	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps
Data Rate (20 MHz, short GI, 400 ns) ⁽¹⁾	Wi-Fi	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2 Mbps
Operating temperature	-	-40 to +85°C

Note:

- Short GI is currently not supported by Firmware. The datasheet will be updated when the feature is supported.

7.1 WLAN Transmitter Performance

The radio performance is tested under the following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C

The following table provides the ATWINC3400 transmitter performance.

Table 7-2. IEEE 802.11 Transmitter Performance Characteristics

Parameter	Description	Minimum	Typical	Max.	Unit
Frequency	-	2,412	-	2,484	MHz

.....continued

Parameter	Description	Minimum	Typical	Max.	Unit
Output power	802.11b 1 Mbps	-	16.7 ⁽¹⁾	-	dBm
	802.11b 11 Mbps	-	17.5 ⁽¹⁾	-	
	802.11g OFDM 6 Mbps	-	18.3 ⁽¹⁾	-	
	802.11g OFDM 54 Mbps	-	13.0 ⁽¹⁾	-	
	802.11n HT20 MCS 0 (800ns GI)	-	17.5 ⁽¹⁾	-	
	802.11n HT20 MCS7 (800ns GI)	-	12.5 ⁽¹⁾⁽²⁾	-	
Tx power accuracy	-	-	±1.5 ⁽²⁾	-	dB
Carrier suppression	-	-	30.0	-	dBc
Harmonic output power (Radiated, Regulatory mode)	2 nd	-	-	-41	dBm/MHz
	3 rd	-	-	-41	

Note:

1. Measured at IEEE 802.11 specification compliant EVM/Spectral mask.
2. Typical output power shall be 10 dBm only for channel-10 (2.457 GHz). Values mentioned in the preceding table are applicable for all the other channels.
3. Measured after RF matching network.
4. Operating temperature range is -40°C to +85°C. RF performance ensured at room temperature of 25°C with a 2-3 dB change at boundary conditions.

7.2 WLAN Receiver Performance

The radio performance is tested under the following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp = 25°C

The following table provides the receiver performance characteristics for the ATWINC3400.

Table 7-3. IEEE 802.11 Receiver Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412	-	2,484	MHz
Sensitivity 802.11b	1 Mbps DSSS	-	-95.0	-	dBm
	2 Mbps DSSS	-	-94.0	-	
	5.5 Mbps DSSS	-	-90.0	-	
	11 Mbps DSSS	-	-86.0	-	

.....continued					
Parameter	Description	Min.	Typ.	Max.	Unit
Sensitivity 802.11g	6 Mbps OFDM	-	-90.0	-	dBm
	9 Mbps OFDM	-	-89.0	-	
	12 Mbps OFDM	-	-87.0	-	
	18 Mbps OFDM	-	-85.0	-	
	24 Mbps OFDM	-	-82.0	-	
	36 Mbps OFDM	-	-79.0	-	
	48 Mbps OFDM	-	-75.0	-	
	54 Mbps OFDM	-	-73.0	-	
Sensitivity 802.11n (BW=20 MHz, 800ns GI)	MCS 0	-	-89.0	-	dBm
	MCS 1	-	-87.0	-	
	MCS 2	-	-84.0	-	
	MCS 3	-	-82.0	-	
	MCS 4	-	-78.0	-	
	MCS 5	-	-75.0	-	
	MCS 6	-	-73.0	-	
	MCS 7	-	-71.0	-	
Maximum receive signal level	1-11 Mbps DSSS	-	0	-	dBm
	6-54 Mbps OFDM	-	0	-	
	MCS 0 - 7 (800ns GI)	-	0	-	
Adjacent channel rejection	1 Mbps DSSS (30 MHz offset)	-	50	-	dB
	11 Mbps DSSS (25 MHz offset)	-	43	-	
	6 Mbps OFDM (25 MHz offset)	-	40	-	
	54 Mbps OFDM (25 MHz offset)	-	25	-	
	MCS 0 – 20 MHz BW (25 MHz offset)	-	40	-	
	MCS 7 – 20 MHz BW (25 MHz offset)	-	20	-	

7.3 Bluetooth Transmitter Performance

The transmitter performance is tested under the following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp: 25°C
- Measured after RF matching network.

The following table provides the Bluetooth transmitter performance characteristics for the ATWINC3400 .

Table 7-4. Bluetooth Transmitter Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,402	-	2,480	MHz

.....continued					
Parameter	Description	Min.	Typ.	Max.	Unit
Output power	Bluetooth Low Energy (GFSK)	-	3.3	3.8	dBm
In-band spurious emission (Bluetooth Low Energy)	N+2 (Image frequency)	-	-33	-	
	N + 3 (Adjacent to image frequency)	-	-32	-	
	N-2	-	-48	-	
	N-3	-	-47	-	

7.4 Bluetooth Receiver Performance

The receiver performance is tested under the following conditions:

- VBAT = 3.3V
- VDDIO = 3.3V
- Temp: 25°C
- Measured after RF matching network

The following table provides the Bluetooth receiver performance characteristics for the ATWINC3400.

Table 7-5. Bluetooth Receiver Performance Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,402	-	2,480	MHz
Sensitivity (ideal Tx)	Bluetooth Low Energy (GFSK)	-	-92.5	-	dBm
Maximum receive signal level	Bluetooth Low Energy (GFSK)	-	-2	-	
Interference performance (Bluetooth Low Energy)	Co-channel	-	9	-	dB
	adjacent + 1 MHz	-	-4	-	
	adjacent - 1 MHz	-	-2	-	
	adjacent + 2 MHz(image frequency)	-	-24	-	
	adjacent - 2 MHz	-	-25	-	
	adjacent + 3 MHz (adjacent to image)	-	-27	-	
	adjacent - 3 MHz	-	-27	-	
	adjacent + 4 MHz	-	-28	-	
	adjacent - 4 MHz	-	-27	-	
	adjacent +5 MHz	-	-27	-	
	adjacent - 5 MHz	-	-27	-	

8. External Interfaces

The ATWINC3400A external interfaces include:

- I²C for control
- SPI for control and data transfer
- UART for debug
- General Purpose Input/Output pins⁽¹⁾

Note:

1. Usage of the GPIO functionality is not supported by the WINC15x0 FW. The datasheet will be updated once the support for this feature is added.

8.1 Interfacing with the Host Microcontroller

This section describes interfacing the ATWINC3400A module with the host microcontroller. The interface is comprised of a slave SPI and additional control signals, as shown in the following figure. For more information on SPI interface specification and timing, refer to the SPI Interface. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 8-1. Interfacing with Host Microcontroller

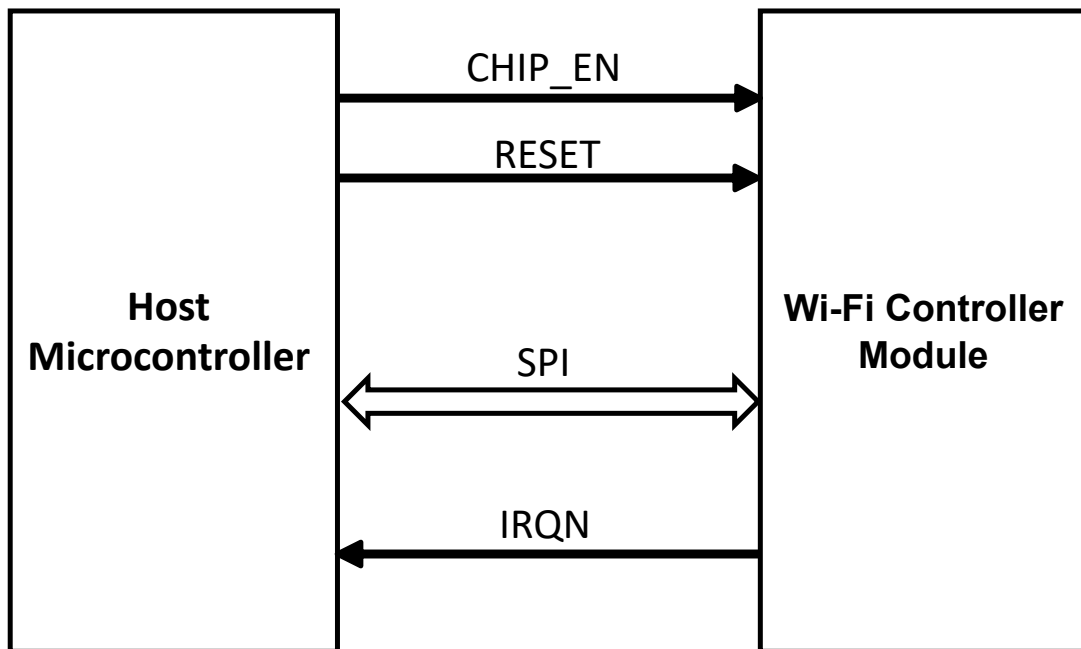


Table 8-1. Host Microcontroller Interface Pins

Pin Number	Pin Name
13	RESETN
27	CHIP_EN
30	SPI_SCK
31	SPI_MISO
32	SPI_SSN
34	SPI_MOSI

.....continued	
Pin Number	Pin Name
40	IRQN

8.2 I²C Slave Interface

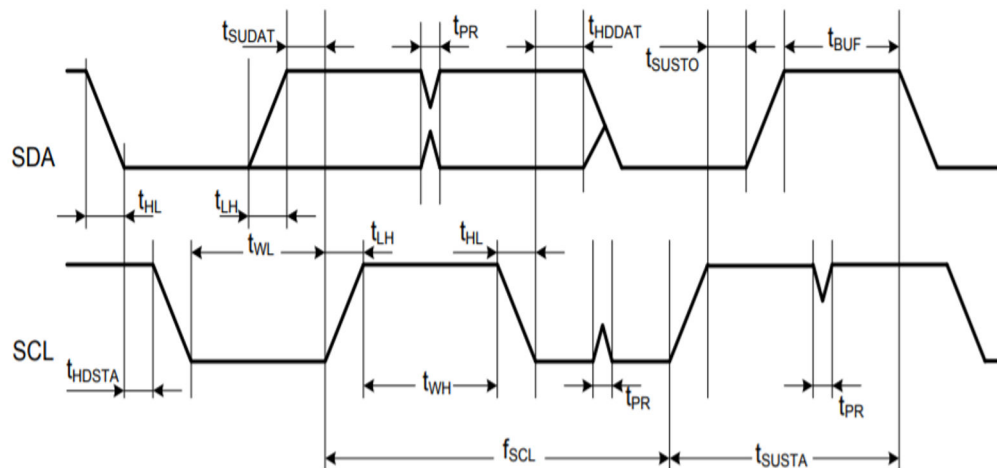
The I²C slave interface, used primarily for control by the host processor, is a two-wire serial interface consisting of a serial data line (SDA) on Pin 16 and a serial clock line (SCL) on Pin 17. I²C slave responds to the seven bit address value 0x60. The ATWINC3400 I²C supports I²C bus version 2.1 - 2000 and can operate in Standard mode (with data rates up to 100 Kb/s) and Fast mode (with data rates up to 400 Kb/s).

The I²C slave is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages.

8.2.1 I²C Slave Timing

The I²C slave timing diagram for the ATWINC3400 IC is shown in the following figure.

Figure 8-2. I²C Slave Timing Diagram



The following table provides the I²C slave timing parameters for the ATWINC3400 IC.

Table 8-2. I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	-
SCL Low Pulse Width	t_{WL}	1.3	-	μs	-
SCL High Pulse Width	t_{WH}	0.6	-		-
SCL, SDA Fall Time	t_{HL}	-	300	ns	-
SCL, SDA Rise Time	t_{LH}	-	300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6	-	μs	-
START Hold Time	t_{HDSTA}	0.6	-		-
SDA Setup Time	t_{SUDAT}	100	-	ns	-

.....continued

Parameter	Symbol	Min.	Max.	Units	Remarks
SDA Hold Time	t_{HDDAT}	0	-	ns	Slave and master default
		40	-	μ s	Master Programming Option
STOP Setup Time	t_{SUSTO}	0.6	-	μ s	-
Bus Free Time Between STOP and START	t_{BUF}	1.3	-		-
Glitch Pulse Reject	t_{PR}	0	50	ns	-

8.3 SPI Slave Interface

8.3.1 Overview

The ATWINC3400 has a Serial Peripheral Interface (SPI) that operates as an SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 and Bluetooth Low Energy data. The SPI pins are mapped as shown in the following table. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following Reset when pin 8 (SPI_CFG) is tied to VDDIO.

Table 8-3. SPI Interface Pin Mapping

Pin #	SPI function
8	SPI_CFG: Must be tied to VDDIO
32	SSN: Active-Low Slave Select
34	MOSI(RXD): Serial Data Receive
30	SCK: Serial Clock
31	MISO(TXD): Serial Data Transmit

When the SPI is not selected, that is, when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial-slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO, and SCK pins of the ATWINC3400 have internal programmable pull-up resistors. These resistors should be programmed to be disabled; otherwise, if any of the SPI pins are driven to a low level while the ATWINC3400 is in the low-power Sleep state, the current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption.

8.3.2 SPI Timing

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

Table 8-4. SPI Slave Modes

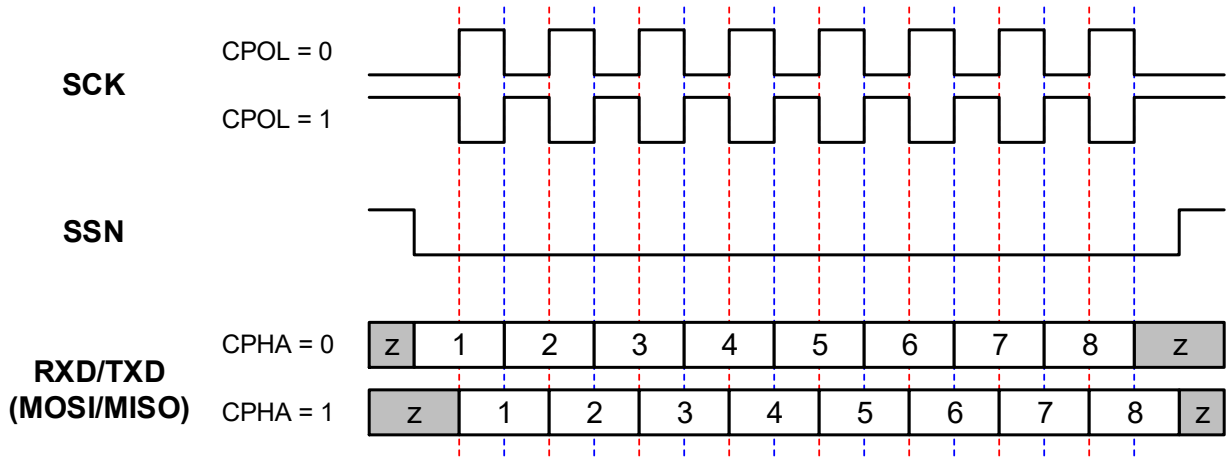
Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0

.....continued		
Mode	CPOL	CPHA
3	1	1

Note: The ATWINC3400A firmware uses “SPI MODE 0” to communicate with the host.

The red lines in the following figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Figure 8-3. SPI Slave Clock Polarity and Clock Phase Timing



The SPI timing is provided in the following figure and table.

Figure 8-4. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)

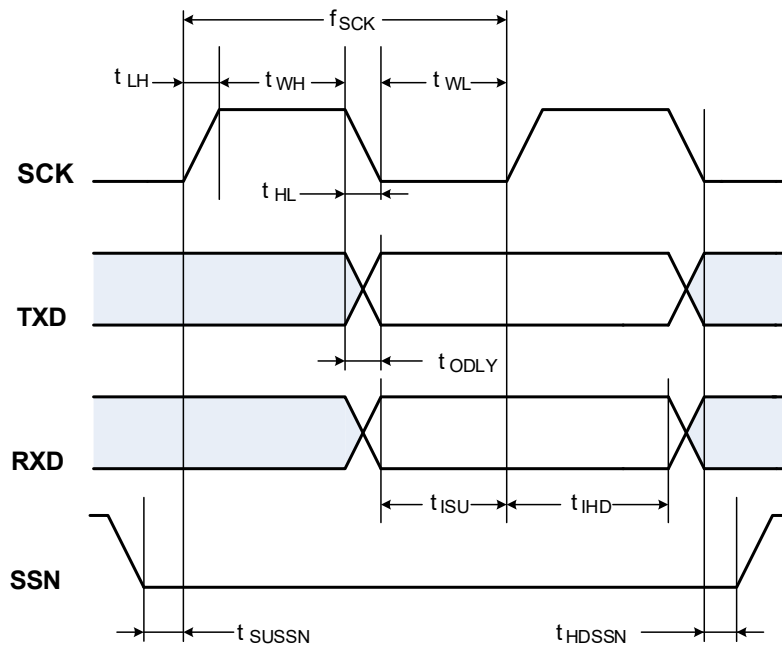


Table 8-5. SPI Slave Timing Parameters¹

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency ²	f_{SCK}	—	48	MHz

.....continued				
Parameter	Symbol	Min.	Max.	Units
Clock Low Pulse Width	t_{WL}	4	—	ns
Clock High Pulse Width	t_{WH}	5	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay ³	t_{ODLY}	4	9 from SCK fall	
RXD Input Setup Time	t_{ISU}	1	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	3	—	
SSN Input Hold Time	t_{HDSSN}	5.5	—	

Note:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design, actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15 pF output loading. Under all conditions, $t_{LH} + t_{WH} + t_{HL} + t_{WL}$ must be less than or equal to $1/f_{SCK}$.

8.4 UART Interface

The ATWINC3400 supports the Universal Asynchronous Receiver/Transmitter (UART) interface, Wi-Fi and Bluetooth Low Energy interfaces should be used for debug purposes only. Wi-Fi UART pins are available on pins 22 (TXD) and 23 (RXD). Bluetooth Low Energy UART pins are available on pins 14 (TXD) and 15 (RXD). The UART is compatible with the RS-232 standard.

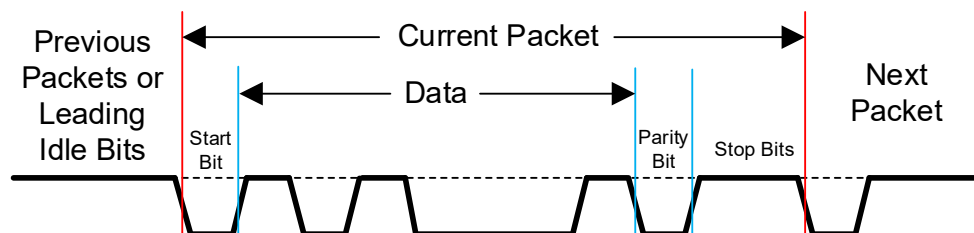
The default configuration for accessing the Wi-Fi UART interface of ATWINC3400A is listed below:

- Baud rate: 460800
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of the UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Figure 8-5. Example of UART RX or TX Packet



9. Power Management

9.1 Power Architecture

The ATWINC3400 uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. This architecture is shown in the following figure. The Power Management Unit (PMU) has a DC/DC Converter that converts VBATT to the core supply used by the digital and RF/AMS blocks. The table below shows the typical values for the digital and RF/AMS core voltages. The PA and eFuse are supplied by dedicated LDOs, and the VCO is supplied by a separate LDO structure.

The power connection in the power architecture figure below provides a conceptual framework for understanding the ATWINC3400 power architecture. For more details, refer to reference design (e.g., power supply connections, including power isolation of the supplies used by the digital and RF/AMS blocks).

Figure 9-1. Power Architecture

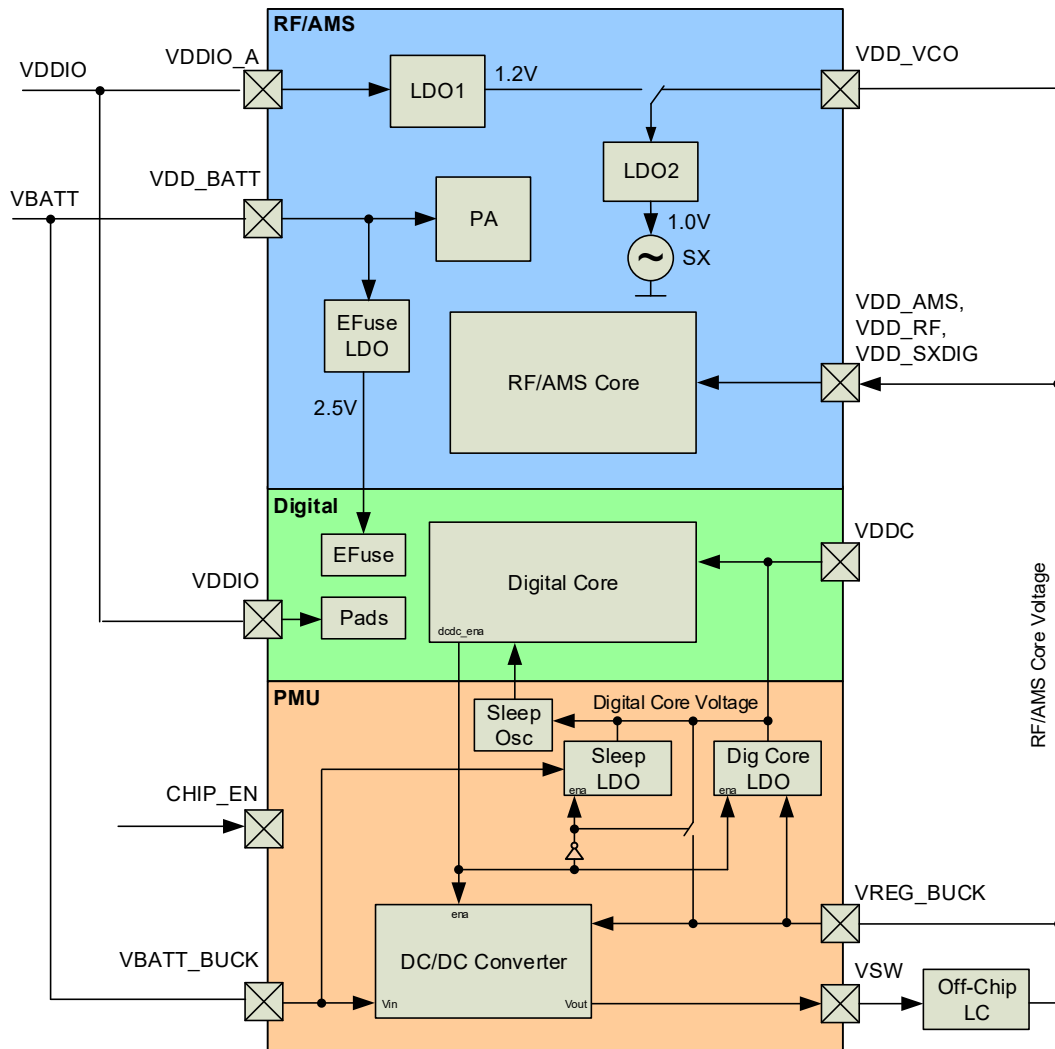


Table 9-1. PMU Output Voltages

Parameter	Typical
RF/AMS Core Voltage (VREG_BUCK)	1.3V

.....continued	
Parameter	Typical
Digital Core Voltage (VDDC)	1.1V

9.2 Power Consumption

9.2.1 Description of Device States

The ATWINC3400 has several device states, based on the state of the IEEE 802.11 and Bluetooth subsystems. It is possible for both subsystems to be active at the same time. To simplify the device power consumption breakdown, the following basic states are defined. One subsystem can be active at a time:

- WiFi_ON_Transmit – Device actively transmits IEEE 802.11 signal
- WiFi_ON_Receive – Device actively receives IEEE 802.11 signal
- BT_ON_Transmit – Device actively transmits Bluetooth signal
- BT_ON_Receive – Device actively receives Bluetooth signal
- Doze – Device is powered on but it does not actively transmit or receive data
- Power_Down – Device core supply is powered off

9.2.2 Controlling Device States

The following table shows different device states and their power consumption for the ATWINC3400. The device states can be switched using the following:

- CHIP_EN – Device pin (pin #27) used to enable or disable the DC/DC converter
- VDDIO – I/O supply voltage from external supply

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To change from the ON states to Power_Down state, connect the RESETN and CHIP_EN pin to logic low (GND) by following the power-down sequence mentioned in [Figure 9-2](#). When VDDIO is OFF and CHIP_EN is low, the chip is powered off with no leakage.

Table 9-2. Device States Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption ⁽¹⁾	
			I _{VBAT}	I _{VDDIO}
ON_WiFi_Transmit	802.11b 1 Mbps	16.7	271 mA	24 mA
	802.11b 11 Mbps	17.5	265 mA	24 mA
	802.11g 6 Mbps	18.3	275mA	24 mA
	802.11g 54 Mbps	13.0	235 mA	24 mA
	802.11n MCS 0	17.5	272 mA	24 mA
	802.11n MCS 7	12.5	232 mA	24 mA
ON_WiFi_Receive	802.11b 1 Mbps	N/A	63.9 mA	23.7 mA
	802.11b 11 Mbps	N/A	63.9 mA	23.7 mA
	802.11g 6 Mbps	N/A	63.9 mA	23.7 mA
	802.11g 54 Mbps	N/A	63.9 mA	23.7 mA
	802.11n MCS 0	N/A	63.9 mA	23.7 mA
	802.11n MCS 7	N/A	63.9 mA	23.7 mA
ON_BT_Transmit	BLE 1 Mbps	3.3	79.37 mA	23.68 mA

.....continued

Device State	Code Rate	Output Power (dBm)	Current Consumption ⁽¹⁾	
			I _{VBAT}	I _{VDDIO}
ON_BT_Receive	BLE 1 Mbps	N/A	51.36 mA	23.68 mA
Doze (Bluetooth Low Energy Idle)	N/A	N/A	53 mA ⁽²⁾	
Doze (Bluetooth Low Energy Low Power)	N/A	N/A	1 mA ⁽²⁾	
Power_Down	N/A	N/A	10.5 μ A ⁽²⁾	

Note:

1. Conditions: VBAT = 3.3V, VDDIO = 3.3V, at 25°C.
2. Current consumption mentioned for these states is the sum of current consumed in VDDIO and VBAT voltage rails.

9.2.3 Restrictions for Power States

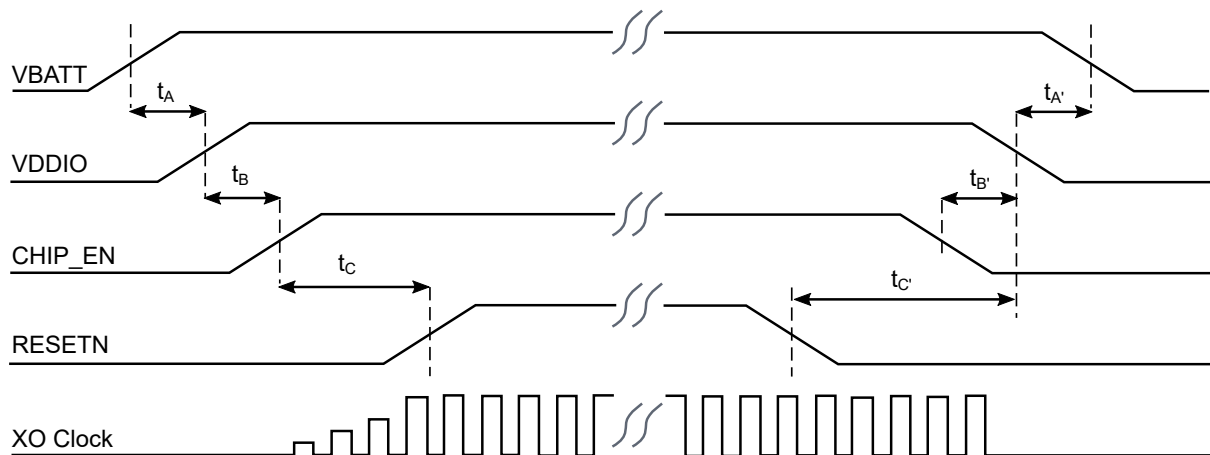
When power is not supplied to the device (DC/DC converter output and VDDIO are OFF, at ground potential), voltage cannot be applied to the ATWINC3400 pins because each pin contains an ESD diode from the pin to supply. This diode turns on when voltage higher than one diode-drop is supplied to the pin.

If voltage must be applied to the signal pads when the chip is in a low-power state, the VDDIO supply must be ON, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning ON, do not apply voltage that is more than one diode-drop below the ground to any pin.

9.2.4 Power-Up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWINC3400.

Figure 9-2. Power-Up/Down Sequence



The following table provides power-up/down sequence timing parameters.

Table 9-3. Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t _A	0	-	ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or connected together. VDDIO must not rise before VBAT.

.....continued

Parameter	Min.	Max.	Units	Description	Notes
t _B	0	-	ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.
t _C	5	-	ms	CHIP_EN rise to RESETN rise	This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.
t _{A'}	0	-	ms	VDDIO fall to VBAT fall	VBAT and VDDIO fall simultaneously or connected together. VBAT must not fall before VDDIO.
t _{B'}	0	-	ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.
t _{C'}	0	-	ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.

9.2.5 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents the digital I/O pin states corresponding to the device power modes.

Table 9-4. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull-Up/Down Resistor (96 kOhm)
Power_Down: core supply OFF	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply and hard reset ON	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply ON, device out of reset and not programmed	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/ On_Receive: core supply ON, device programmed by firmware	High	High	High	Programmed by firmware for each pin: enabled or disabled	Opposite of Output Driver state	Programmed by firmware for each pin: enabled or disabled

10. Electrical Characteristics

This chapter provides an overview of the electrical characteristics of the ATWINC3400.

10.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings for the ATWINC3400.

Table 10-1. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
VDDIO	I/O supply voltage	-0.3	5.0	V
VBAT	Battery supply voltage	-0.3	5.0	
V _{IN}	Digital input voltage	-0.3	VDDIO	
V _{AIN}	Analog input voltage	-0.3	1.5	
V _{ESDHBM}	Electrostatic discharge Human Body Model (HBM)	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
T _A	Storage temperature	-65	150	°C
-	Junction temperature	-	125	
-	RF input power	-	23	dBm

1. V_{IN} corresponds to all the digital pins.
2. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
 - 2.1. The Class 1 pins include all the pins (both analog and digital).
 - 2.2. The Class 2 pins include all digital pins only.
 - 2.3. V_{ESDHBM} is ±1 kV for Class 1 pins. V_{ESDHBM} is ±2 kV for Class 2 pins.



Stresses beyond those listed under “Absolute Maximum Ratings” cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods affects the device reliability.

10.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for the ATWINC3400.

Table 10-2. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDDIO	I/O supply voltage ⁽¹⁾	2.7	3.3	3.6	V
VBAT	Battery supply voltage ^{(2),(3)}	3.0	3.3	4.2	V
-	Operating temperature	-40	-	85	°C

Note:

1. I/O supply voltage is applied to the VDDIO pin.
2. Battery supply voltage is applied to the VBAT pin.
3. The ATWINC3400 is functional across this range of voltages; however, optimal RF performance is assured for VBAT 3.3V.

10.3 DC Characteristics

The following table provides the DC characteristics for the ATWINC3400 digital pads.

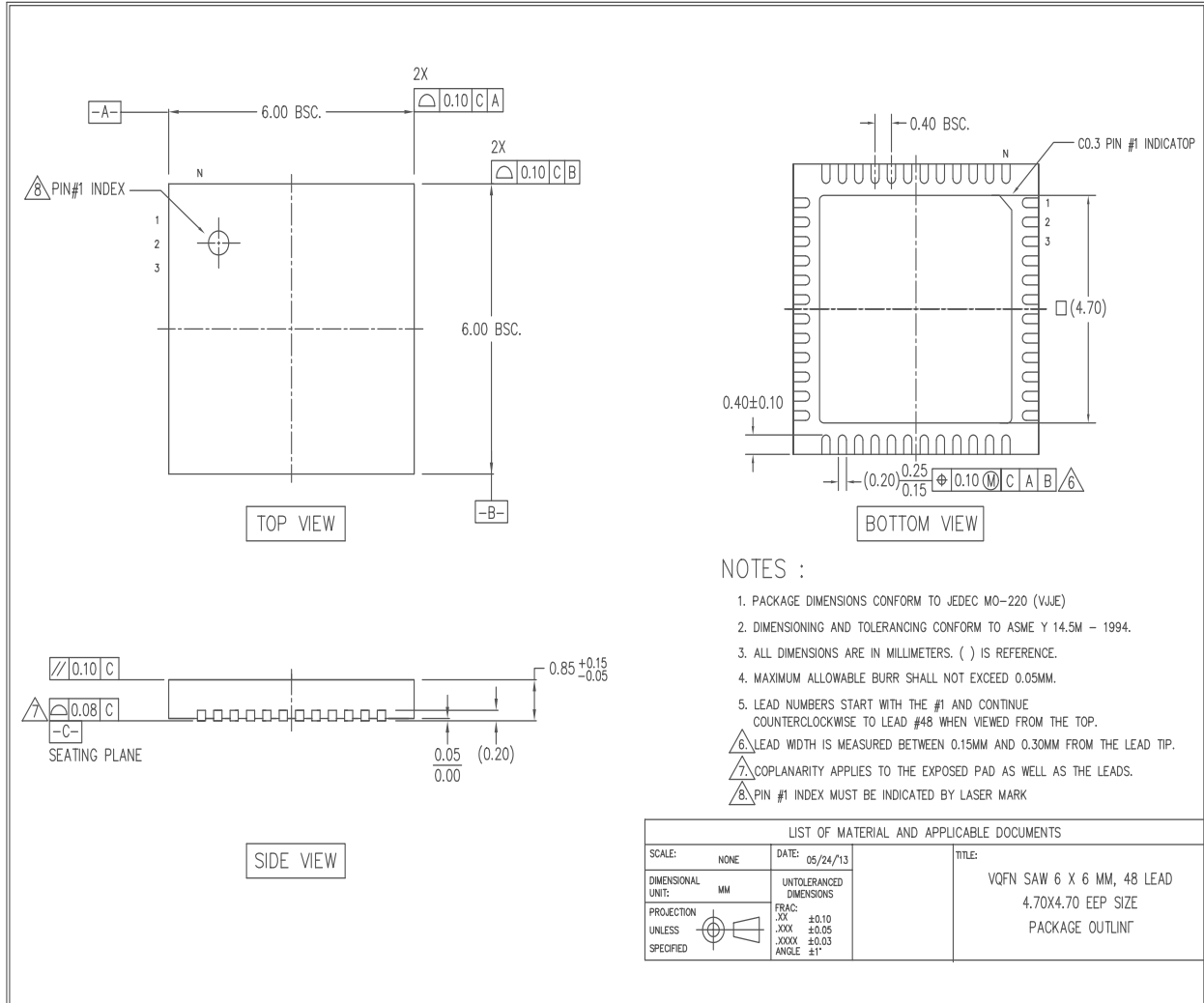
Table 10-3. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	-0.30	-	0.60	V
V_{IH}	Input High Voltage	VDDIO-0.60	-	VDDIO+0.30	
V_{OL}	Output Low Voltage	-	-	0.45	
V_{OH}	Output High Voltage	VDDIO-0.50	-	-	
-	Output Load Capacitance	-	-	20	pF
-	Digital Input Load Capacitance	-	-	6	

11. Package Outline Drawing

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

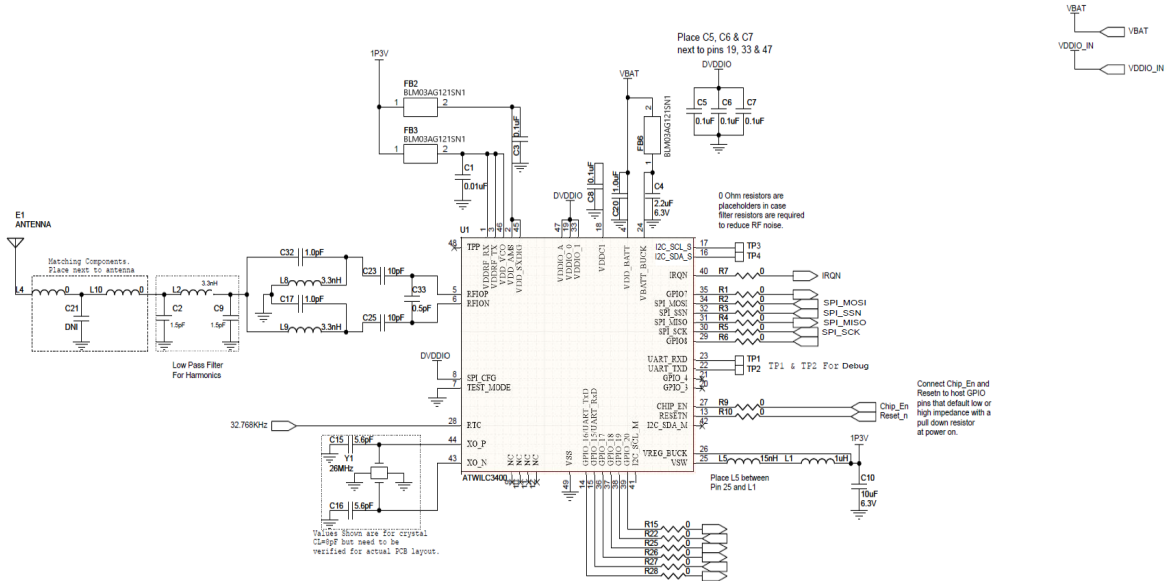
Figure 11-1. ATWINC3400 QFN Package Outline Drawings - Top , Bottom and Side View



12. Reference Design

The ATWINC3400 schematics is shown in this section.

Figure 12-1. Reference Schematic



Note:

1. Add test points for I2C_SCL(17) and I2C_SDA(16) pins.
2. Add test points for UART_TxD(22) and UART_RxD(23) pins.

The following table provides the reference Bill of Material (BoM) details for the ATWINC3400A reference design with SPI as host interface.

Table 12-1. ATWINC3400A Reference Bill of Materials for SPI Operation

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number
1	1	C1	0.01 uF	CAP,CER,0.01 uF, 10%,X5R, 0201,10V,-55-125C	Murata	GRM033R61A103KA01D
2	5	C3,C5,C6, C7,C8	0.1 uF	CAP,CER,0.1 uF, 10%,X5R, 0201,6.3V,-55-125C	Murata	GRM033R60J104KE19D
3	1	C4	2.2 uF	CAP,CER,2.2 uF, 10%,X5R, 0402,6.3V,-55-85C	TDK	C1005X5R0J225K
4	1	C20	1.0 uF	CAP,CER,1.0 uF, 10%,X5R, 0402,6.3V,-55-85C	Murata	GRM155R60J105KE19D
5	1	C10	10 uF	CHIP MONO 0402 10uF 6.3V +-20% X5R	Murata	GRM155R60J106ME44D
6	2	C15,C16	5.6 pF	CHIP MONO 0201 5.6 pF 25V +-0.5 pF C0G	Murata	GRM0335C1E5R6DA01D

.....continued

Item	Quantity	Reference	Value	Description	Manufacturer	Part Number
7	2	C17,C32	1.0 pF	CAP,CER,1.0 pF, +/-0.1 pF,NPO, 0201,25V,-55-125C	Murata	GRM0335C1E1R0BA01D
8	2	C23,C24	10 pF	CAP,CER,10 pF, +/-0.5 pF,NPO, 0201,25V,-55-125C	TDK	C0603C0G1E100D030BA
9	1	C33	0.5 pF	CAP,CER,0.5 pF, +/-0.1 pF,NPO, 0201,25V,-55-125C	Murata	GRM0335C1ER50BA01D
10	2	C2,C9	1.5 pF	CAP,CER,1.5 pF, +/-0.25 pF,COG, 0201,25V,-55-125C	Murata	GRM0335C1H1R5CA01
11	1	C21	DNI	RESISTOR,Thick Film,4.7K,5%,0201	Vishay	CRCW0201-472J
12	1	E1	2450AT18A100	Antenna, ceramic, 2.4-2.5 GHz, 50Ω	Johanson	2450AT18A100
13	3	FB2,FB3,FB6	BLM03AG121SN1	FERRITE,120Ω @100 MHz,200 mA, 0201,-55-125C	Murata	BLM03AG121SN1
14	1	L1	1 uH	POWER INDUCTOR,1 uH, 20%,950 mA,250 mΩ, 0603,shielded,-40-85 c	Murata	LQM18PN1R0MFRL
15	1	L5	15 nH	INDUCTOR,Multilayer, 15 nH,5%,450 mA,Q=8@100 MHz, 0402	Murata	LQG15HS15NJ02D
16	3	L2,L8,L9	3.3 nH	Inductor,3.3 nH,0.2 nH,Q=14@500 MHz,SRF=8 GHz, 0201,-55-125C	Murata	LQP03TN3N3C02D
17	15	L4, L10,R1,R2 ,R3,R4,R5 ,R6,R7,R1 5,R22,R25 ,R26,R27, R28	0	RESISTOR,Thick Film,0Ω,0201	Panasonic	ERJ-1GN0R00C
18	1	TP1,TP2,TP3,TP4	DNI	Test Point,Surface Mount,0.030"sq		30X30_SM_TEST_POINT
19	1	U1	ATWINC3400A	IC, SOC, WiFi Bluetooth & FM Combo, 48QFN	Microchip	ATWINC3400A-MU

.....continued						
Item	Quantity	Reference	Value	Description	Manufacturer	Part Number
20	1	Y1	26 MHz	CRYSTAL,26 MHz,CL=8 pF,15 ppm,-40-85C,ESR=60,2.5x2 mm	Taitien	A0183-X-001-3

13. Design Considerations

13.1 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board should have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias.
- To avoid electromagnetic field blocking, keep any large metal objects as far away from the antenna as possible.
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise or signals within the 2.4 GHz to 2.5 GHz frequency band away from the antenna, and shield those components if possible. Any noise radiated from the host board in this frequency band degrades the sensitivity of the chip.

13.1.1 Power and Ground

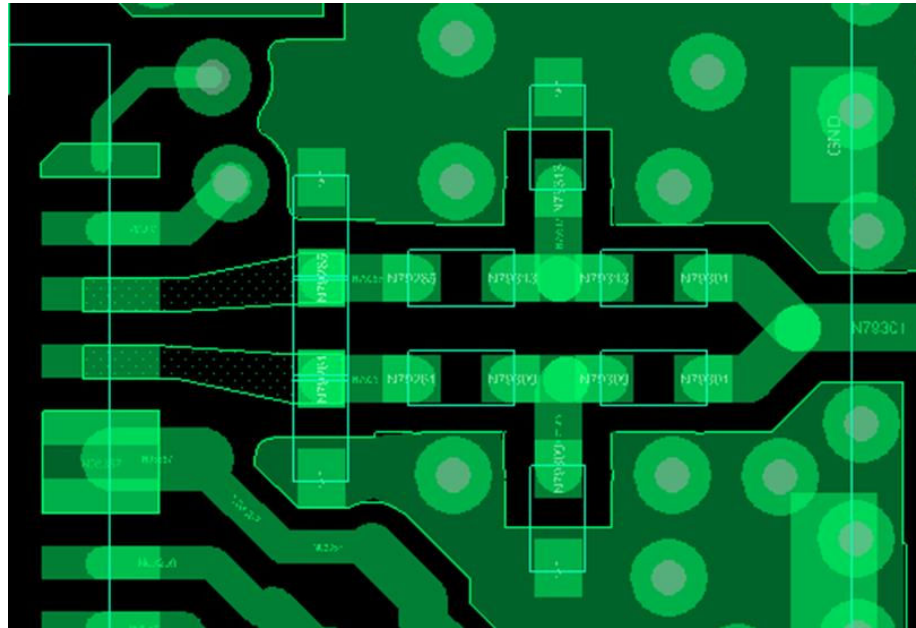
- Dedicate the layer immediately below the layer containing the RF traces from the ATWINC3400A for ground. Ensure that, this ground plane does not get broken up by routes.
- Power traces can be routed on all layers except the ground layer.
- Power supply routes must be heavy copper fill planes to insure low inductance.
- The power pins of the ATWINC3400A must have a via directly to the power plane, close to the power pin.
- Decoupling capacitors must have a via next to the capacitor pin and this via must be directly connected to the power plane and avoid long trace for this connection.
- The ground pad of the decoupling capacitor must have a via directly to the ground plane.
- Each decoupling capacitor must have its own via directly to the ground plane and directly to the power plane next to the pad.
- The decoupling capacitors must be placed as close as possible to the pin that it is filtering.

13.1.2 RF Traces and Components

The RF trace from RFIOP (Pin #5) and RFION (Pin #6) of the ATWINC3400A to the balun must be 50Ω differential controlled impedance. The route from the balun to the antenna connector must be a 50Ω controlled impedance trace. This trace must be routed in reference to the ground plane. This ground reference plane must extend entirely under the ATWINC3400A QFN package and to the sides of these routes.

- Discuss with the PCB vendor to get the available PCB stack-ups and determine the trace dimensions for achieving 50Ω single ended controlled impedance.
- Do not have any signal traces below/adjacent to the RF trace in the PCB.
- Ensure that, the RF traces from ATWINC3400A to the antenna is as short as possible to reduce path losses and to mitigate the trace from picking-up noise.
- Place guard ground vias on either side of the RF trace running from module to the antenna feed point, in the PCB.
- Do not use thermal relief pads for the ground pads of all components in the RF path. These component pads must be completely filled with GND copper polygon. Place individual vias to the GND pads of these components.
- It is recommended to have a 3x3 grid of ground vias solidly connecting the exposed ground paddle of the ATWINC3400A to the ground plane on the inner/other layers of the PCB. This acts as a good ground and thermal conduction path for the ATWINC3400A.
- Ensure that, all digital signals that may be toggling while the ATWINC3400A active are placed as far away from the antenna as possible.
- Ensure to place the matching components and balun as close to the RFIOP and RFION pins as possible (these C33, C23, C25, C17, C32, L8, and L9 in the reference schematic).
The following figure shows the placement and routing of these components.

Figure 13-1. Placement and Routing of Balun and Matching Components



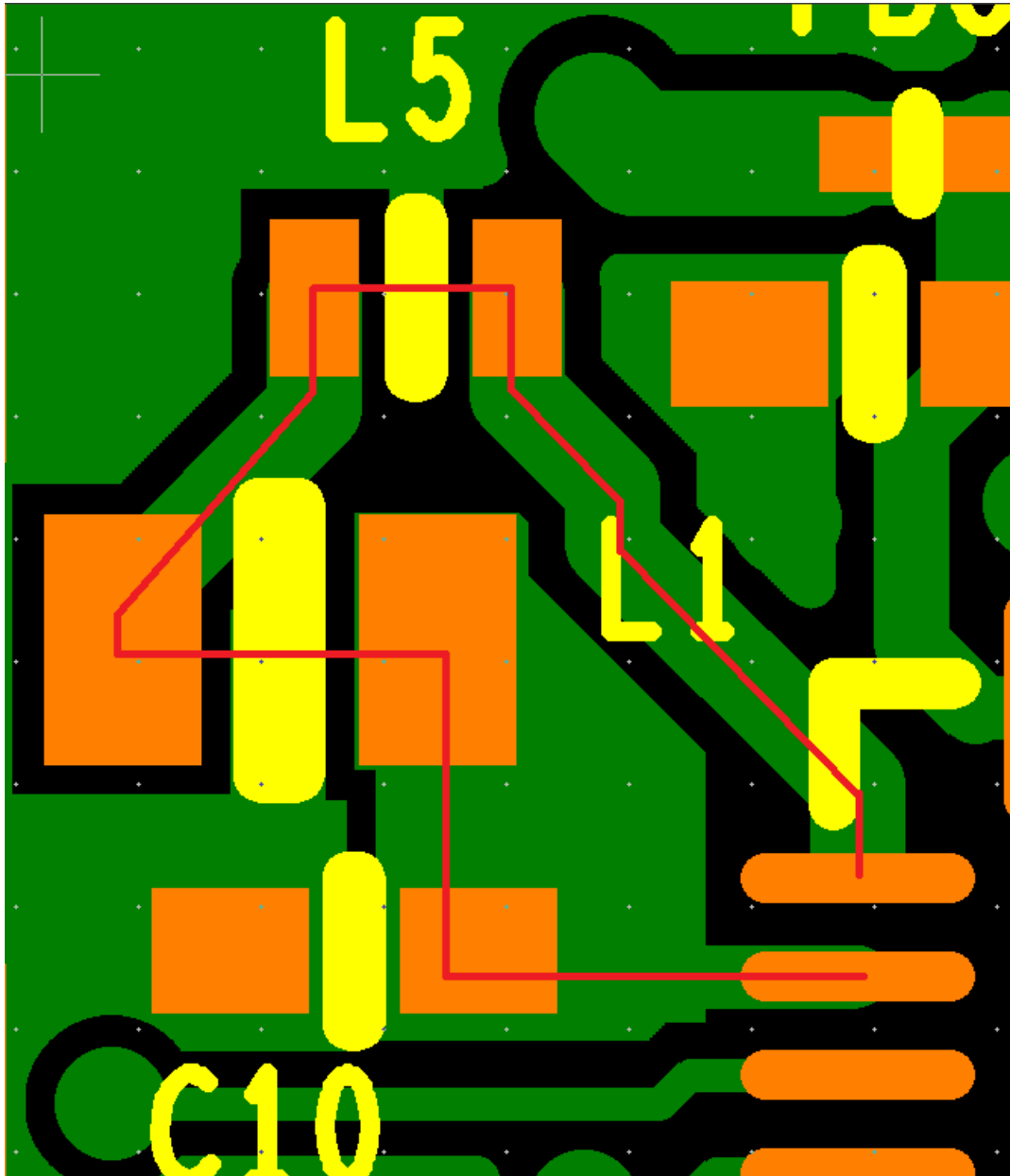
13.1.3 Power Management Unit

The ATWINC3400A contains an on-chip switching regulator, which regulates the VBAT supply for supplying to rest of the device. It is crucial to place and route the components associated with this circuit correctly to ensure proper operation and especially to reduce any radiated noise, which can be picked up by the antenna and can severely reduce the receiver sensitivity. The external components for the PMU consist of two inductors, $L5 = 15 \text{ nH}$ and $L1 = 1 \text{ } \mu\text{H}$ and a capacitor, $C10 = 10 \text{ } \mu\text{F}$. These components must be placed as close as possible to ATWINC3400A pin #25.

The smaller inductor, $L5$, must be placed closest to pin #25. Current flows from pin #25, through $L5$, then $L1$, and then through $C10$ to ground and back to the center ground paddle of the ATWINC3400A package. Place components to have a current loop that is small as possible. Make sure that there is a ground via to the inner ground plane right next to the ground pin of $C10$. The ground return path must be extremely low inductance. Failure to provide a short, heavy ground return between the capacitor and the ATWINC3400A ground pad results in incorrect operation of the on-chip switching regulator. The following figure shows an example placement and routing of these components.

In the following figure, the trace which creates the loop is highlighted in red.

Figure 13-2. Placement and Routing of PMU Components



13.1.4 Ground

The center ground pad of the device must be solidly connected to the ground plane by using a 3 x 3 grid of vias. These ground vias must surround the perimeter of the pad. One of these ground vias must be in the center pad as close as possible to pins #5 (RFIOP) and #6 (RFION). This Ground via serves as the RF ground return path. Also, there must be a ground via in the center pad as close as possible to pin #25 (VSW). This is the ground return for the PMU.

13.2 Sensitive Traces

13.2.1 Signals

The following signals are very sensitive to noise and you must take care to keep them as short as possible and keep them isolated from all other signals by routing them far away from other traces or using ground to shield them.

Ensure that, they are also isolated from noisy traces on the layers above them and below them:

- XO_N
- XO_P
- RFIOP
- RFION

13.2.2 Supplies

The following power supply pins for the ATWINC3400A are sensitive to noise and care should be taken to isolate the routes to these pins from other noisy signals both on the same layer as the route and on layers above and below.

Use ground between these sensitive signals to isolate them from other signals. It is important that the decoupling capacitors for these supplies are placed as close to the ATWINC3400A pin as possible. This is necessary to reduce the trace inductance between the capacitor and ATWINC3400A power pin to an absolute minimum:

- VDDRF_RX (pin #1)
- VDDRF_TX (pin #3)
- VDD_AMS (pin #2)
- VDD_SXDIG (pin #45)
- VDD_VCO (pin #46)

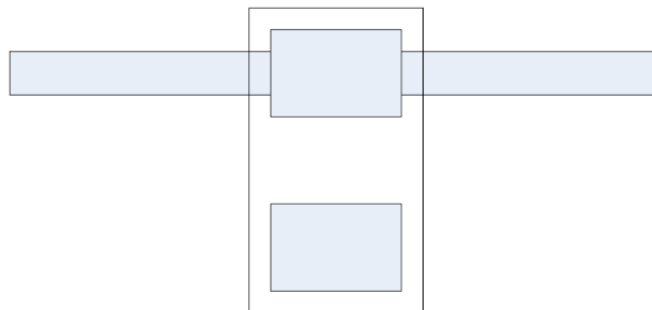
Additionally, while the VDDC (pin #18) and VBAT_BUCK (pin #24) supplies are not sensitive to picking up noise, they are noise generating supplies. Therefore, be sure to keep the decoupling capacitors for these supply pins as close as possible to the VDDC and VBAT_BUCK pins and make sure that the routes for these supplies stay far away from sensitive pins and supplies.

13.3 Additional Suggestions

Ensure that traces route directly through the pads of all filter capacitors and not by a stub route.

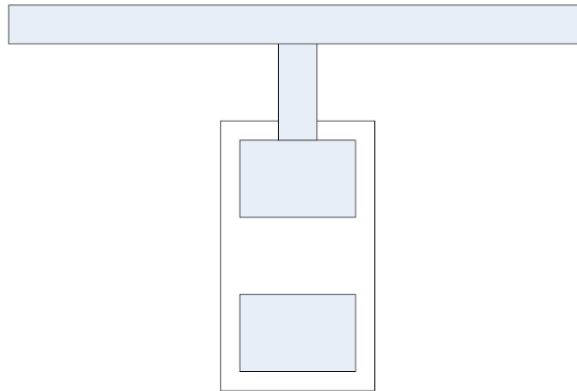
The following figure shows the correct way to route through a capacitor pad.

Figure 13-3. Correct Routing Through Capacitor Pad



The following figure shows a stub route to the capacitor pad. This should be avoided, as it adds additional impedance in series with the capacitor.

Figure 13-4. Incorrect Stub Route To Capacitor Pad



13.4 Interferers

One of the biggest problem with RF receivers is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there is no noisy circuitry placed anywhere near the antenna or the RF traces. All noise generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna. Also, make sure that no traces route underneath the RF portion of the ATWINC3400A. Also, make sure that no traces route underneath any of the RF traces from the antenna to the ATWINC3400A input. This applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current flows on the ground plane and couple into the RF traces.

13.5 Antenna

The following guidelines can be used for selecting an antenna:

- Choose an antenna that covers the frequency band 2.400 GHz to 2.500 GHz and is designed for a 50 Ω feed point.
- Follow the antenna vendor's recommendations for pad dimensions, the spacing from the pad to the ground reference plane, and the spacing from the edges of the pad to the ground fill on the same layer as the pad.
- Ensure that the antenna matching components are placed as close as to the antenna pad as possible.

13.6 Reflow Profile Information

For information on reflow process guidelines, refer to the [Solder Reflow Recommendation Application Note \(DS00233\)](#).

14. Reference Documentation

For further study, refer the following documents:

Table 14-1. Reference Documents

Title	Content
Getting Started Guide for ATWINC3400 Wi-Fi using SAMD21 Xplained Pro	Provides details for how to evaluate the ATWINC3400 Network controller Module.
ATWINC3400 IEEE 802.11 b/g/n Network Controller Module with Integrated Bluetooth	ATWINC3400 Module Datasheet
ATWINC3400 Wi-Fi/BLE Network Controller - Software Design Guide	Integration guide with a clear description of high-level architecture, an overview on how to write networking application, list all API, parameters, and structures. Describes features of the device and handshaking protocols between device and host MCU, with flow/sequence/state diagram, timing.
ATWINC3400 BLE Profiles Application User Guide	User's Guide with BLE profile application, and running the applications with the WINC3400 Module.
ATWINC3400 BLE Provisioning - Setup and Usage	Provides details for how to run ATWINC3400 Bluetooth® Low Energy (BLE) Provisioning demo from out-of-box conditions.
Solder Reflow Recommendation application note (DS00233D)	Provides more information on Reflow Process guidelines.
ATWINC3400A/ATWINC3400-MR110xA Errata	This document details on the anomalies identified in the ATWINC3400A family of devices.
ATWINC3400A Reference Design Package	Reference Design Package contains the design collaterals (Schematics, Bill of Materials, PCB design source files, Gerber) of the module, evaluation boards, and its associated boards for ATWINC3400A which should help a user to get started with their design.

Note:

1. For a complete listing of development-support tools and documentation, visit <http://www.microchip.com/wwwproducts/en/ATWINC3400> or refer to the customer support section to locate the nearest Microchip field representative.

15. Document Revision History

Revision	Date	Section	Description
A	04/2020	Document	<ul style="list-style-type: none"> Initial Revision Updated from Atmel to Microchip Template. Assigned a new Microchip document number. Previous version is Atmel 42396 revision C.

Atmel Revision History Information

Table 15-1. Rev C - 07/2015

Section	Changes
In 9.2.1 and 9.2.2	Modified to add new current consumption numbers, update state names and corrected some typos
in 8.1.1	Fixed typos for SPI Slave interface timing
	Fixed typos for battery supply name: changed from VBAT to VBATT
in 9.1	Corrected PMU output voltages
in 11.2	Updated reference schematic drawing
	Replaced Bluetooth with BLE throughout the document, updated content accordingly
	Removed PCM functionality
in 9.1	Updated power architecture drawing
	Updated operating temperature in the feature list
in 9.2.2	Corrected current in Power_Down state in Table 9-2
	Miscellaneous minor formatting and content corrections

Table 15-2. Rev B - 03/2015

Section	Changes
in 1 and 2.4 respectively	Ordering information (Table 1-1) and QFN Package Information (Table 2-2) have been corrected.

Table 15-3. Rev A - 02/2015

Section	Changes
	Initial document release.

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