ATA8710

Sub-GHz ASK/FSK RF Transmitter with Integrated MCU and 20 Kbytes Flash Program Memory

Introduction

The ATA8710 is a highly integrated, low-power UHF ASK/FSK RF transmitter with an integrated AVR® microcontroller.

The ATA8710 is partitioned into three sections: an RF front-end, digital baseband and the low-power 8-bit AVR microcontroller. The product is designed for the ISM frequency bands from 310 MHz to 318 MHz, 418 MHz to 477 MHz, and 836 MHz to 956 MHz. The external part count is kept to a minimum due to the very high level of integration in this device. By combining outstanding RF performance with highly sophisticated baseband signal processing, robust wireless communication can be easily achieved. The transmit path uses a closed-loop fractional-N modulator with Gauss shaping and preemphasis functionality for high data rates.

The ATA8710 implements a flexible service configuration concept and supports up to 15 channels. These channels are grouped into five service configurations with three channels each. Three of the five service configurations are stored in EEPROM. Two service configurations are in the SRAM to allow on-the-fly modifications during IDLEMode via SPI commands or application software, which is in Flash. The 1024-byte EEPROM stores the transmitter configuration. The SPI interface enables external control and device reconfiguration.

Use the internal microcontroller with 20 Kbytes Flash program memory to add custom extensions to the embedded firmware. In addition, the debugWIRE and ISP interfaces are available for programming purposes.

Features

- AVR Microcontroller Core with 20 Kbytes of User Program Flash, 1 Kbyte SRAM and 24 Kbytes RF Library in Firmware (ROM)
- Supported Frequency Ranges:
  - Low-band 310 MHz to 318 MHz, 418 MHz to 477 MHz
  - High-band 836 MHz to 956 MHz
  - 315.00 MHz/433.92 MHz/868.30 MHz and 915.00 MHz with one 24.305 MHz crystal
- Low Current Consumption: 9.4 mA/13.8 mA (Low-band, P_{out} = 6 dBm/10 dBm)
- Typical OFFMode Current of 5 nA (Maximum 600 nA at VS = 3.6V and T = 85°C)
- Programmable Output Power: -12 dBm to +14.5 dBm (0.4 dB Step)
- Supports the 0 dBm Class of ARIB STD-T96
- ASK Shaping to Reduce Spectral Bandwidth of Modulated PA Output Signal
- Programmable Channel Frequency with Fractional-N Phase-Locked Loop (PLL):
  - 93 Hz resolution for low band
  - 185 Hz resolution for high band
- FSK deviation: ±0.375 kHz to ±93 kHz
- Supported Data Rate in Buffered Mode: 0.5 Kbit/s to 80 Kbit/s (120 Kbit/s NRZ)
- Flexible Service Configuration Concept with On-The-Fly (OTF) Modification (in IDLEMode) of SRAM Service Parameters (Data Rate etc.)
  - Each service consists of:
    - One service-specific configuration part
    - Three channel-specific configuration parts

  - Three service configurations are in EEPROM
  - Two service configurations are located in SRAM and can be modified via SPI or embedded application software
- Programmable Clock Output Derived from Crystal Frequency
- 1024-byte EEPROM Data Memory for Transmitter Configuration
- SPI Interface for TX Data Access and Transmitter Configuration
- 500-Kbit SPI Data Rate for Short Periods on SPI Bus and Host Controller
- Configurable EVENT Signal Indicates the Status of the IC to an External Microcontroller
- Automatic Antenna Tuning At TX Center Frequency for Loop Antenna
- Power-up (Typical 1.5 ms OFFMode -> TXMode)
- Non-byte Aligned Data Transmission
- Software Customization
- Antenna Diversity with an Internal SPDT Switch
- Supply Voltage Range: 1.9V to 3.6V
- Temperature Range: -40°C to +85°C
- ESD Protection at All Pins (±4 kV HBM, ±200V MM, ±750V FCDM)
- Small 5x5 mm QFN32 Package with 0.5 mm Pitch
- Suitable for Applications Governed by EN 300 220 and FCC Part 15, Title 47, such as:
  - Remote control system
  - Home and building automation
  - Wireless sensor networks
  - Weather stations
  - Battery-operated remote controls
  - Smoke detectors
  - Wireless alarm and security systems

Table of Contents

1. Quick References

1.1 Reference Documentation

For more details, refer to the following documents:

- *ATA8710 User's Guide*

1.2 Acronyms and Abbreviations

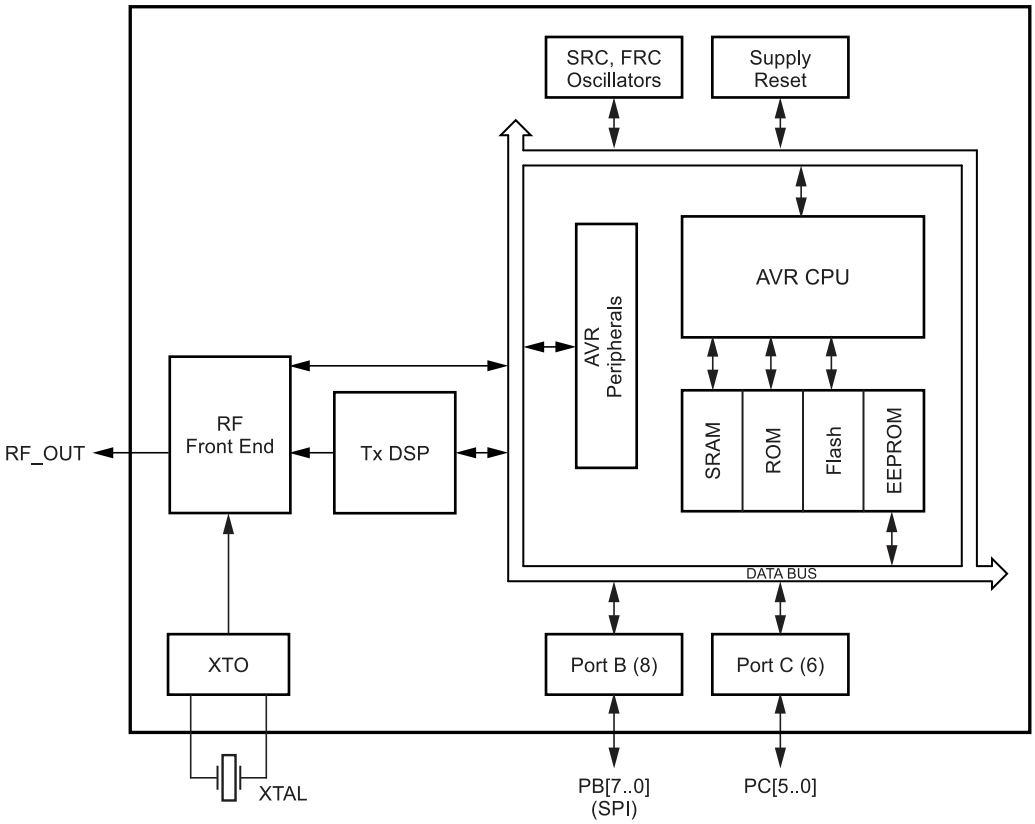
Table 1-1. Acronyms and Abbreviations

Acronyms and Abbreviations	Description
ASK	Amplitude Shift Keying
CPU	Central Processing Unit
DSP	Digital Signal Processing
EEPROM	Electrically Erasable Programmable Read-only Memory
FIFO	First In First Out
FSK	Frequency Shift Keying
IC	Integrated Circuit
ISP	In-system Programming
LDO	Low-dropout
NC	Not Connected
NRZ	Non-return-to-zero
OOK	On-off Keying
OTF	On-the-fly
PA	Power Amplifier
RF	Radio Frequency
ROM	Read-only Memory
SPDT	Single Pole Double Throw
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TX	Transmitter/Transmit
UHF	Ultra-High Frequency
VCO	Voltage Controlled Oscillator
XTAL	Crystal
XTO	Crystal Oscillator

2. System Overview

The following figure illustrates an overview of the main functional blocks of the ATA8710. Perform external control through the SPI pins SCK, MOSI, MISO and NSS on port B. The configurations in the EEPROM and firmware in the ROM define a large portion of the functionality and are processed by the AVR. An SPI command can trigger the AVR to configure the hardware according to the settings stored in the EEPROM. Internal events such as “Start of Telegram” or “FIFO empty” are signaled to an external microcontroller on pin 28 (PB6/EVENT).

Figure 2-1. Circuit Overview



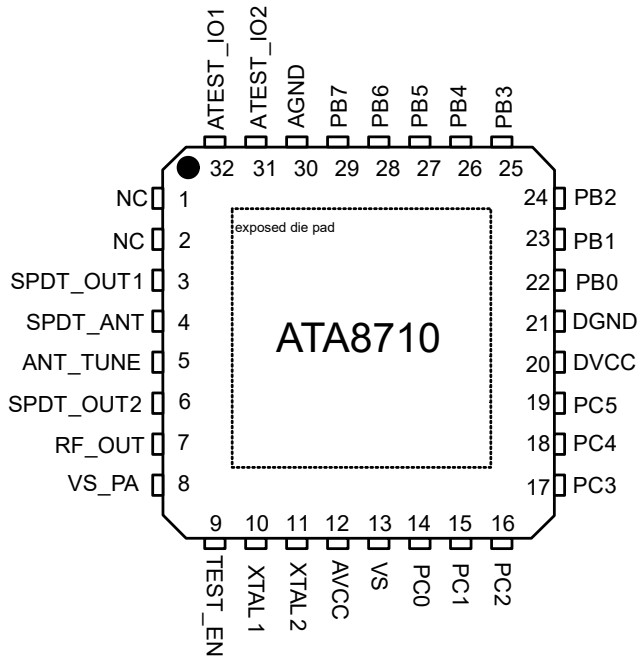
During the start-up of service, the relevant part of the EEPROM content is copied to the SRAM. This allows faster access by the AVR during the subsequent processing steps and eliminates the need to write to the EEPROM during runtime because parameters can be modified directly in the SRAM. As a consequence, the user does not need to observe the EEPROM read/write cycle limitations.

It is important to note that all PWRON and NPWRON pins (PC1-PC5, PB4, PB7) are active in OFFMode. This means that even if the ATA8710 is in OFFMode and DVCC voltage is switched off, the power management circuitry within the ATA8710 biases these pins with VS.

AVR ports can be used as button inputs, LED drivers, EVENT pins, switching control for additional SPDT switches, general-purpose digital inputs, or wake-up inputs, and so on. Some functionality of these ports is already implemented in the firmware and can be activated by adequate EEPROM configurations. Other functionality is available only through custom software residing in the 20 Kbytes Flash program memory.

2.1 Pinout Diagram

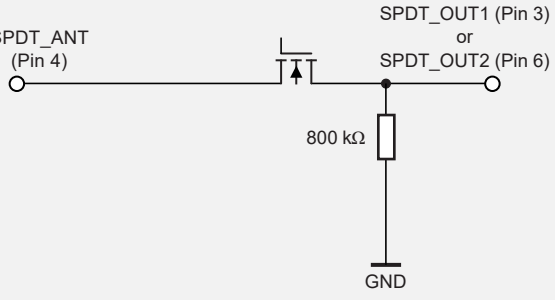
Figure 2-2. Pin Diagram



Note: The exposed die pad is connected to the internal die.

2.1.1 Pinout Description

Table 2-1. Pin Description

Pin No.	Pin Name	Type	Equivalent Circuit	Description
1	NC	—	—	—
2	NC	—	—	—
3	SPDT_OUT1	Analog		Output for the power to the antenna
4	SPDT_ANT	Analog		RF power to be routed to either SPDT_OUT1 or SPDT_OUT2

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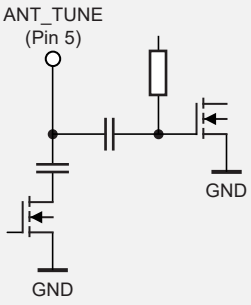
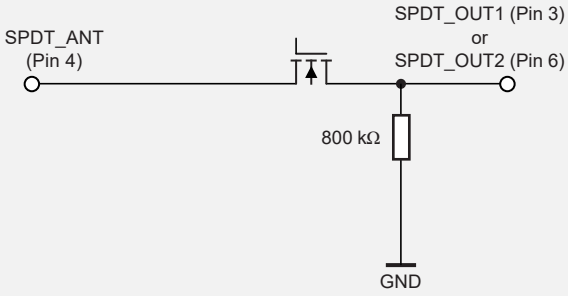
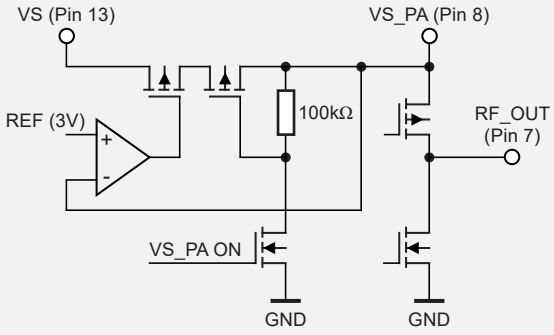
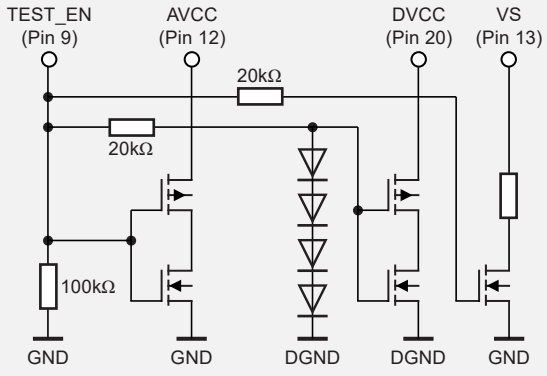
Pin No.	Pin Name	Type	Equivalent Circuit	Description
5	ANT_TUNE	Analog		Antenna tuning input
6	SPDT_OUT2	Analog	See also circuit pin 3 and pin 4 	Output for the power to the antenna
7	RF_OUT	Analog		Power amplifier output
8	VS_PA	Analog		Power amplifier supply, connect to VS
9	TEST_EN	—		Test enable, connected to GND in application

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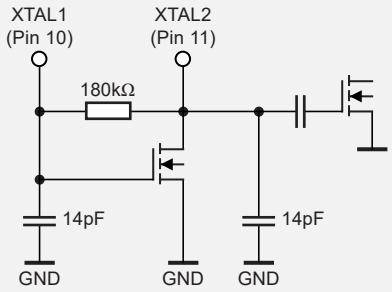
Pin No.	Pin Name	Type	Equivalent Circuit	Description	
10	XTAL1	Analog		Crystal oscillator pin 1 (input)	
11	XTAL2	Analog		Crystal oscillator pin 2 (output)	
12	AVCC	Analog	See 5.8 ESD Protection Circuits	RF front-end supply regulator output	
13	VS	Analog	See 5.8 ESD Protection Circuits and pins 7, 8 and 9	Main supply voltage input	
14	PC0	Digital	—	Main	AVR® Port C0
				Alternate	PCINT8/NRESET/ DebugWIRE
15	PC1	Digital	—	Main	AVR® Port C1
				Alternate	NPWRON1/PCINT9/ EXT_CLK
16	PC2	Digital	—	Main	AVR® Port C2
				Alternate	NPWRON2/PCINT10
17	PC3	Digital	—	Main	AVR® Port C3
				Alternate	NPWRON3/ PCINT11/TxD
18	PC4	Digital	—	Main	AVR® Port C4
				Alternate	NPWRON4/PCINT12/ INT0/TMDI/RxD
19	PC5	Digital	—	Main	AVR® Port C5
				Alternate	NPWRON5/PCINT13
20	DVCC	—	See 5.8 ESD Protection Circuits	Digital supply voltage regulator output	
21	DGND	—	See 5.8 ESD Protection Circuits	Digital ground	
22	PB0	Digital	—	Main	AVR® Port B0
				Alternate	PCINT0/CLK_OUT
23	PB1	Digital	—	Main	AVR® Port B1
				Alternate	PCINT1/SCK
24	PB2	Digital	—	Main	AVR® Port B2
				Alternate	PCINT2/MOSI (SPI Host Out Client In)
25	PB3	Digital	—	Main	AVR® Port B3
				Alternate	PCINT3/MISO (SPI Host In Client Out)

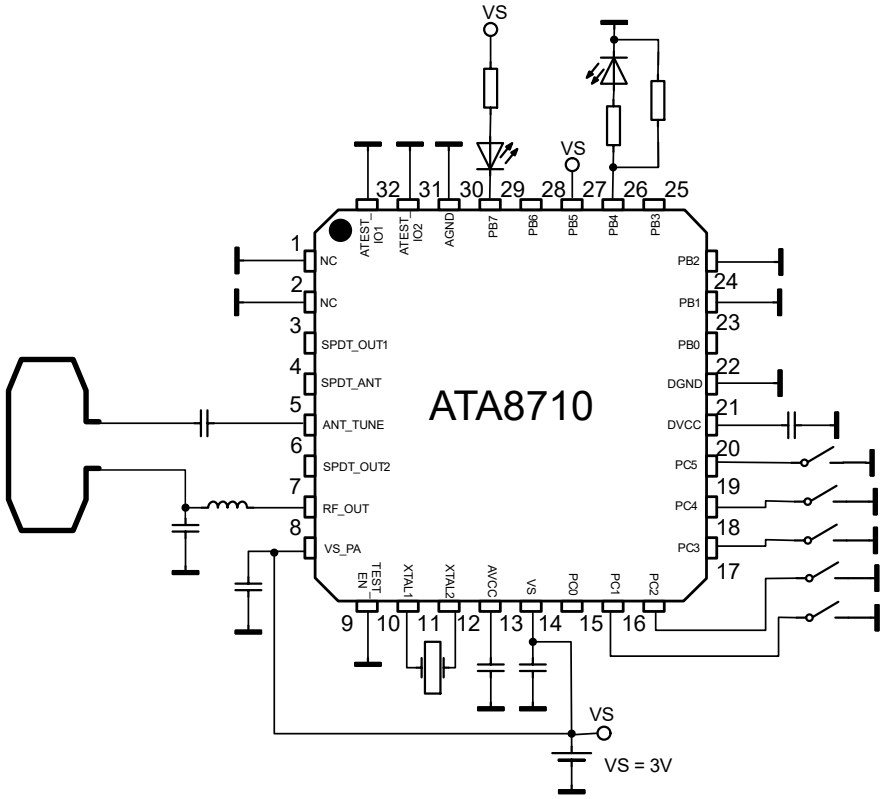
.....continued

Pin No.	Pin Name	Type	Equivalent Circuit	Description	
26	PB4	Digital	—	Main	AVR® Port B4
				Alternate	PWRON/PCINT4/ LED1 (strong high side driver)
27	PB5	Digital	—	Main	AVR® Port B5
				Alternate	PCINT5/INT1/NSS
28	PB6	Digital	—	Main	AVR® Port B6
				Alternate	PCINT6/EVENT (firmware controlled external micro-controller event flag)
29	PB7	Digital	—	Main	AVR® Port B7
				Alternate	NPWRON6/ PCINT7/ LED0 (strong low side driver)
30	AGND	—	See 5.8 ESD Protection Circuits	Analog ground	
31	ATEST_IO2	—	—	RF front-end test I/O 2 connected to GND in application	
32	ATEST_IO1	—	—	RF front-end test I/O 1 connected to GND in application	
—	GND	—	See 5.8 ESD Protection Circuits	Ground/backplane on the exposed die pad	

2.2 Typical Application Schematic

2.2.1 Typical 3V Stand-Alone Application

Figure 2-3. Typical 3V Stand-Alone Application



The preceding figure illustrates a stand-alone application circuit running from a 3V lithium cell. The ATA8710 stays in OFFMode until one of the NPWRON ports, PC1-PC5, is pulled to ground level, waking up the circuit. The NPWRON ports, PC1-PC5, have internal 50 kΩ pull-up resistors and can be left open if not used.

The 20 Kbytes Flash user application software and the firmware in the 24 Kbytes ROM control the ATA8710 transmitter.

In this application, PB7 connects to an LED. Alternatively, an additional wake-up button can be used on PB7 instead of an LED. An LED can also be connected to PB4. However, note the additional pull-down resistor connected in parallel that is needed to prevent transverse currents in OFFMode. This particular case only applies to PB4 because of its active input characteristics (PWRON).

3. System Functional Description

3.1 Overview

3.1.1 Service-Based Concept

The ATA8710 is a highly configurable UHF transmitter. An internal 1024-byte EEPROM stores the configuration. The firmware controls the system. General chip-wide settings are loaded from the EEPROM to the hardware registers during system initialization. During start-up, the specific settings are loaded from the EEPROM or SRAM to the current service in the SRAM, and from there to the corresponding hardware registers.

A complete configuration set of the transmitter is called “service” and includes RF settings, modulation settings and telegram handling information. Each service contains three channels that differ in the RF transmit frequencies.

The ATA8710 supports five services that are configurable in various ways to meet customer requirements. Three service configurations located in the EEPROM space are fixed configurations and must be unchanged during runtime.

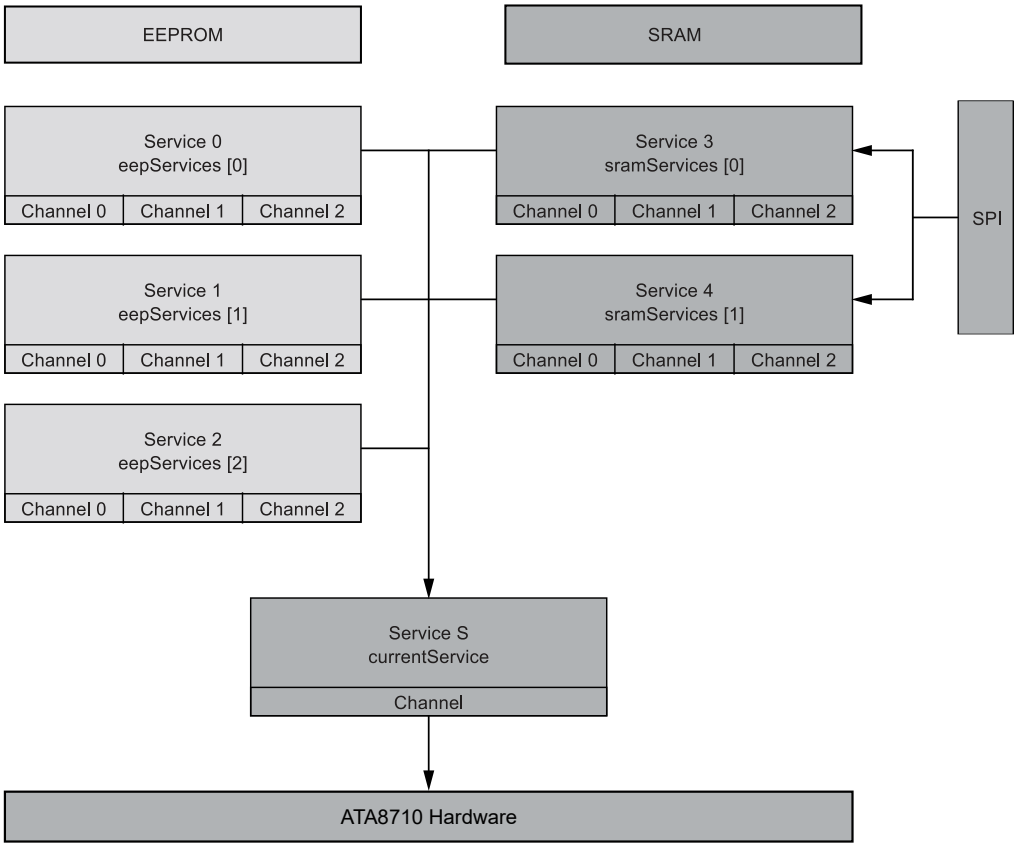
Two service configurations are located in the SRAM space and can be modified by the user’s software in a Flash application or by an SPI command during IDLEMode.

A service consists of:

- One service-specific configuration part
- Three channel-specific configuration parts

The following figure illustrates an overview of the service-based concept.

Figure 3-1. Service-Based Concept Overview

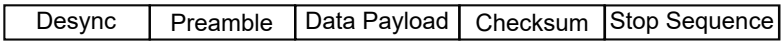


3.1.2 Supported Telegrams

3.1.2.1 Telegram Structure

The ATA8710 supports the transmission of a wide variety of telegrams and protocols. Generally, no special structure is required for a telegram to be transmitted by the ATA8710. However, designated hardware and software features are built-in for the blocks depicted in the following figure. Therefore, using this structure or parts of it can increase the robustness of the broadcast.

Figure 3-2. Telegram Structure



Desync:

The de-synchronization (Desync) is usually a coding violation with a length of several symbols that should provoke a defined restart of the receiver. The use of a de-synchronization leads to more deterministic receiver behavior, reducing the required preamble length, which can be favorable in timing-critical and energy-critical applications.

Preamble:

The preamble is a pattern sent before the actual data payload to synchronize the receiver and provide the starting point of the payload. A very regular pattern (for example, 1-0-1-0...) is recommended for synchronization (“wake-up pattern, WUP”) while a unique, well-defined pattern of up to 32 symbols is required to mark the start of the data payload (“start frame identifier, SFID” or “start bit”). The WUP is also called a pre-burst. In polling scenarios, the WUP can be tens or hundreds of ms long.

Data Payload:

The data payload contains the actual information content of the telegram. It can be NRZ or Manchester-coded. The length of the payload is application-dependent, typically 1-64 bytes.

Checksum:

A checksum can be calculated across the data payload to verify that the correct data is received. A typical example is an 8-bit CRC checksum. Up to 255 data bits at the beginning of the payload can be excluded from the CRC calculation.

Stop Sequence:

The stop sequence is a short data pattern (typically 2 to 6 symbols) to mark the end of the telegram. A coding violation can prevent additional (non-deterministic) data from being received.

3.1.2.2 NRZ and Manchester Coding

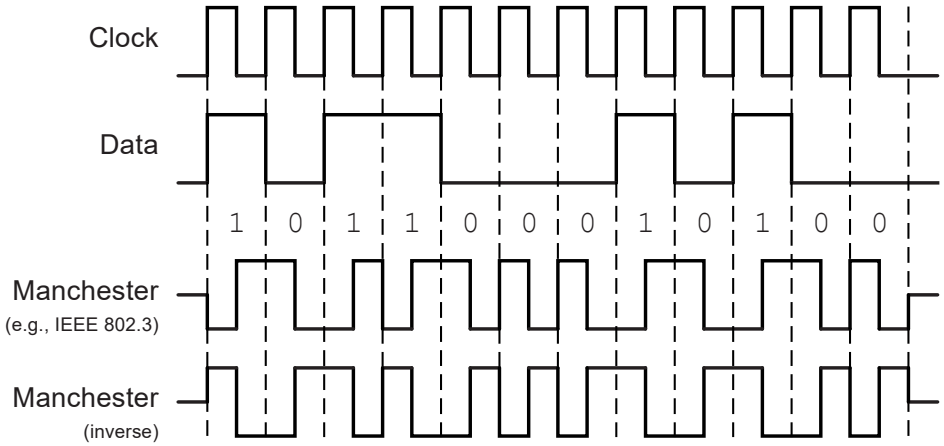
In this document:

- Data bit – Represents the smallest unit of binary data being communicated
- Data bit rate – The rate at which data bits change value
- Symbols – Sub-unit of binary data bit. Used when multiple symbols define a data bit
- Symbol rate – The rate at which symbols change value

The ATA8710 supports the following coding methods:

- Manchester coding – Implements two symbols per data bit. A symbol transition from ‘0’ to ‘1’ is defined as a ‘1’ data bit, and a symbol transition from ‘1’ to ‘0’ is defined as a ‘0’ data bit when following the Manchester coding convention specified in IEEE 802.3. For more details, see the following figure.
- Non-return-to-zero (NRZ) coding – Is a straightforward implementation, that is, one symbol represents one bit.

Figure 3-3. Manchester Code

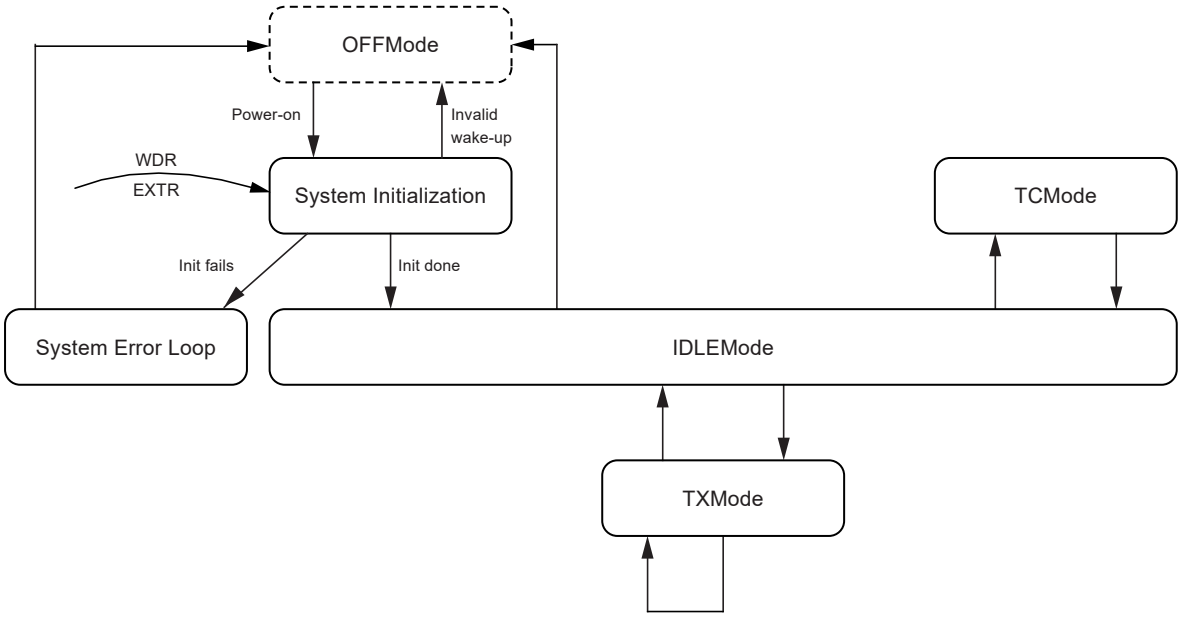


Manchester coding has many advantages, such as simple clock recovery, no DC component, and error detection by code violation. Drawbacks are the coding/decoding effort and the increased symbol rate, which is twice the data rate.

3.2 Operating Modes Overview

This section gives an overview of the operating modes supported by the ATA8710 (see the following figure).

Figure 3-4. Operating Modes Overview



After connecting the supply voltage to the VS pin, the ATA8710 always starts in OFFMode and all of the internal circuits are disconnected from the power supply. Therefore, no SPI communication is supported. Activate the PWRON pin or one of the NPWRONx pins to wake up the ATA8710, triggering the power-on sequence. After the system initialization, the ATA8710 reaches the IDLEMode.

The IDLEMode is the basic system mode supporting SPI communication and transitions to all other operating modes. There are two options of the IDLEMode requiring configuration in the EEPROM settings:

- IDLEMode(RC) with low power consumption using the fast RC (FRC) oscillator for processing
- IDLEMode(XTO) with an active crystal oscillator for high accuracy clock output or timing measurements

The Transmit mode (TXMode) enables data transmission using the selected service/channel configurations. It is usually enabled by the SPI command “Set System Mode” or directly after power-on when selected in the EEPROM setting.

The Tune and Check mode (TCMode) offers calibration and self-checking functionality for the VCO and FRC oscillators and antenna tuning. Activate this TCMode via the SPI command “Calibrate and Check.” When selected in the EEPROM settings, tune and check tasks are also used during system initialization after power-on.

The following table provides the relations between the operating modes and their corresponding power supplies, clock sources and sleep mode settings.

Table 3-1. Operating Modes versus Power Supplies and Oscillators

Operation Mode	AVR® Sleep Mode	DVCC	AVCC	XTO	SRC	FRC
OFFMode	—	off	off	off	off	off
IDLEMode(RC)	Active mode	on	off	off	on	on
	Power-down(1)		off	off	on	off
IDLEMode(XTO)	Active mode		on	on	on	off
	Power-down(1)		on	on	on	off
TXMode	Active mode		on	on	on	off

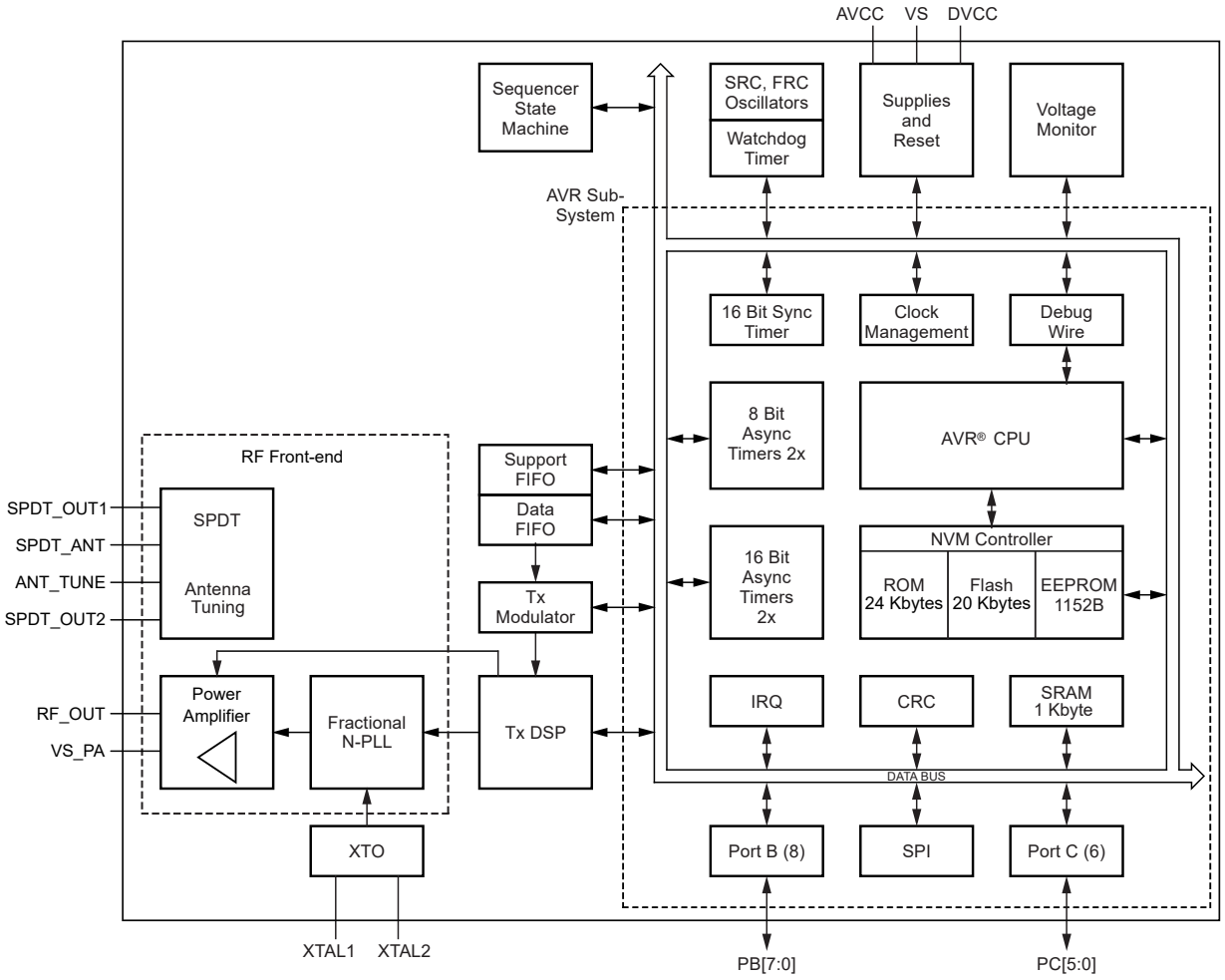
Note:

1. During IDLEMode(RC) and IDLEMode(XTO), the AVR® microcontroller enters sleep mode to reduce the current consumption. The Sleep mode of the microcontroller section can be defined in the EEPROM. The power-down mode is recommended for keeping the current consumption low.

4. Hardware

The ATA8710 consists of an analog front-end, digital signal processing blocks (DSP), an 8-bit AVR sub-system and various supply modules such as oscillators and power regulators. The following figure illustrates a hardware block diagram of the ATA8710.

Figure 4-1. Block Diagram



In the TXMode, the fractional-N PLL generates the TX frequency. The power amplifier (PA) generates an RF output power signal programmable from -10 dBm to +14 dBm at RF_OUT. Perform the FSK modulation by changing the frequency setting of the fractional-N PLL dynamically with the TX digital signal processing (TX DSP). Digital pre-emphasis and digital Gauss filtering can be activated in the TX DSP to achieve higher data rates or reduce occupied bandwidth. The ASK modulation is performed by switching the power amplifier on and off. An ASK shaping filter is available to minimize the transmitted bandwidth of the modulated PA output signal. When enabled, the shaping filter is activated at the start and end of an FSK transmission.

With the Single Pole Double Throw (SPDT) switch, the RF signal from RF_OUT can be routed to two separate antennas (each tuned to a different desired frequency) through SPDT_OUT1 or SPDT_OUT2.

An adjustable capacitor and an RF level detector on ANT_TUNE are used to tune the center frequency of loop antennas to reduce tolerances and capacitive proximity effects.

An AVR CPU controls the system with a 24-KB firmware ROM, 20-KB user Flash, 1024-byte EEPROM, 1024-byte SRAM and other peripherals for the transmitter operation. Two GPIO ports, PB[7:0] and PC[5:0], are available for external digital connections. For example, as an alternate function, the SPI interface is connected to port B. The

EEPROM configuration and SPI commands control the ATA8710, and the firmware in the ROM determines the main functional behavior. Most of the configurations can be modified by the EEPROM settings. The firmware running on the AVR gives access to the hardware functionality. Extensions to this firmware can be added in the 20 KB of Flash memory. The TX DSP registers are addressed directly and accessible from the AVR. A sequencer state machine is included to perform TX path operations (such as enable, disable), which require a defined timing parallel to the AVR program execution.

The power management contains low-dropout (LDO) regulators and reset circuits for the supply voltages, VS, AVCC, and DVCC, of the ATA8710. In the OFFMode, all the supply voltages, AVCC and DVCC, are switched off to achieve very low current consumption. Activate the PWRON pin or one of the NPWRON[6:1] pins to power up the ATA8710 LDOs because they are still active in the OFFMode. The AVCC domain can be switched on and off independently from DVCC. The ATA8710 includes two idle modes. In the IDLEMode(RC), only the DVCC voltage regulator, the FRC and SRC oscillators are active, and the AVR uses a power-down mode to achieve low current consumption. In the IDLEMode(XTO), the AVCC voltage domain and the XTO are additionally activated.

An integrated watchdog timer is available to restart the ATA8710 when it is not served within the configured time-out period.

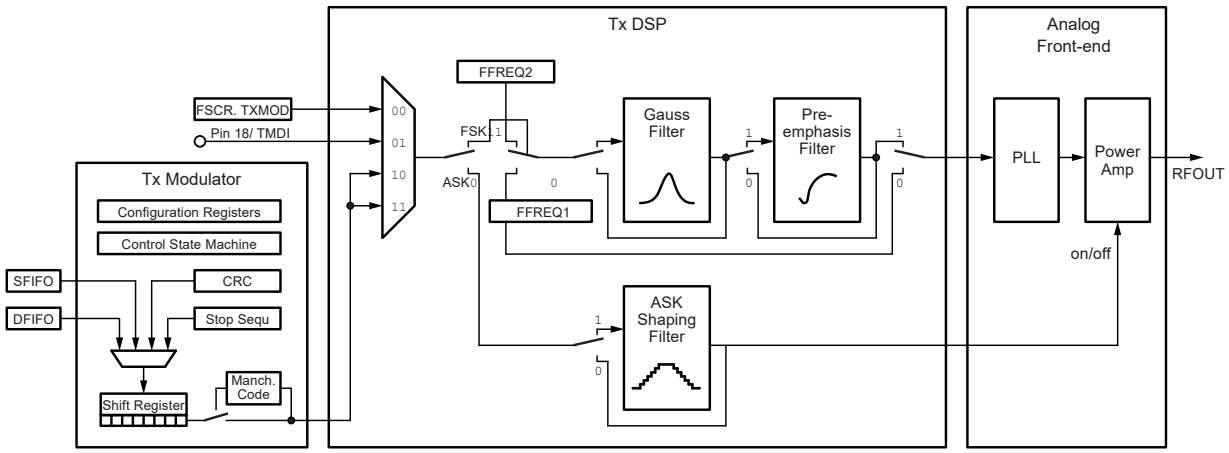
4.1 Transmit Path

The ATA8710 integrates a transmitter that is capable of sending data with various options:

- Frequency bands 310 MHz to 318 MHz, 418 MHz to 477 MHz, 836 MHz to 956 MHz
- Data rates up to 80 Kbit/s Manchester or 120 Ksym/s NRZ in buffered and transparent mode
- ASK or FSK modulation
- Transparent or buffered mode
- ASK shaping filter
- Gauss-shaping digital filter

This section describes the integrated hardware blocks to perform the transmit functionality. The following figure illustrates a block diagram of the transmit data path.

Figure 4-2. Transmit Data Path



There are three ways to select the transmission data source:

1. Using a register bit
2. Using the transparent input pin 18 (TMDI)
3. Using the TX modulator that fetches the data from the DFIFO and SFIFO

If the ASK/OOK modulation is selected, the data stream can directly switch the power amplifier on and off. The PLL frequency synthesizer sets the transmitted carrier frequency.

If the FSK modulation is selected, the data stream switches between the two frequencies generated by the PLL frequency synthesizer; the power amplifier is constantly on. Use power ramping (ASK shaping) during the initial

carrier turn-on and turn-off to reduce spectral harmonics. Enable digital Gauss shaping to reduce the occupied bandwidth. For data rates above 20 kHz Manchester or 40 kHz NRZ-coding, a digital pre-emphasis filter must be enabled to compensate for the PLL loop filter.

4.2 AVR Controller

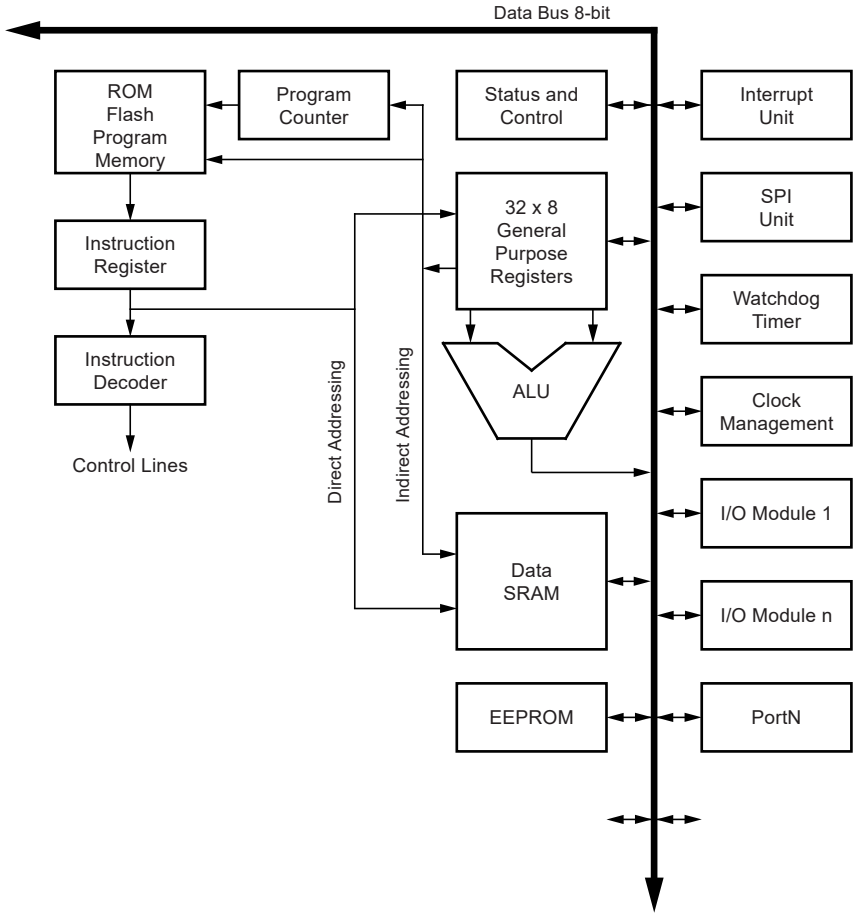
4.2.1 AVR Controller Sub-System

The AVR controller sub-system consists of the AVR CPU core, its program memory and a data bus with data memory and peripheral blocks attached. The transmit path also has its user interfaces connected to the data bus.

4.2.2 CPU Core

The primary function of the CPU core is to ensure correct program execution. For this reason, the CPU core must be able to access memories, perform calculations, control peripherals and handle interrupts.

Figure 4-3. Overview of Architecture



To maximize performance and parallelism, the AVR uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While executing one instruction, the next instruction is prefetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system reprogrammable Flash memory and ROM.

The fast-access register file contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows a single-cycle arithmetic and logic unit (ALU) operation. In a typical ALU operation, two operands are output from the register file, the operation is executed, and the result is stored back in the register file, in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for Look-up Tables in the Flash program memory. Referred to as ‘X,’ ‘Y’ and ‘Z’ registers, these higher 16-bit function registers are described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The program flow is provided by conditional and unconditional jump and call instructions directly addressing the entire address space. As a result, most AVR instructions have a single 16-bit word format. In addition, every program memory address contains a 16- or 32-bit instruction.

The program memory space is divided into two sections, the boot program section and the application program section. Both sections have dedicated Lock bits for write and read/write protection. In addition, the Store Program Memory (SPM) instruction that writes into the application Flash memory section must reside in the boot program section.

During interrupts and subroutine calls, the return address of the program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM; the stack size is, thus, only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the Stack Pointer (SP) in the reset routine before executing the subroutines or interrupts. The SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has control registers in the I/O space with an additional global interrupt enable bit in the status register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority as per their interrupt vector position. The lower the interrupt vector address, the higher the priority.

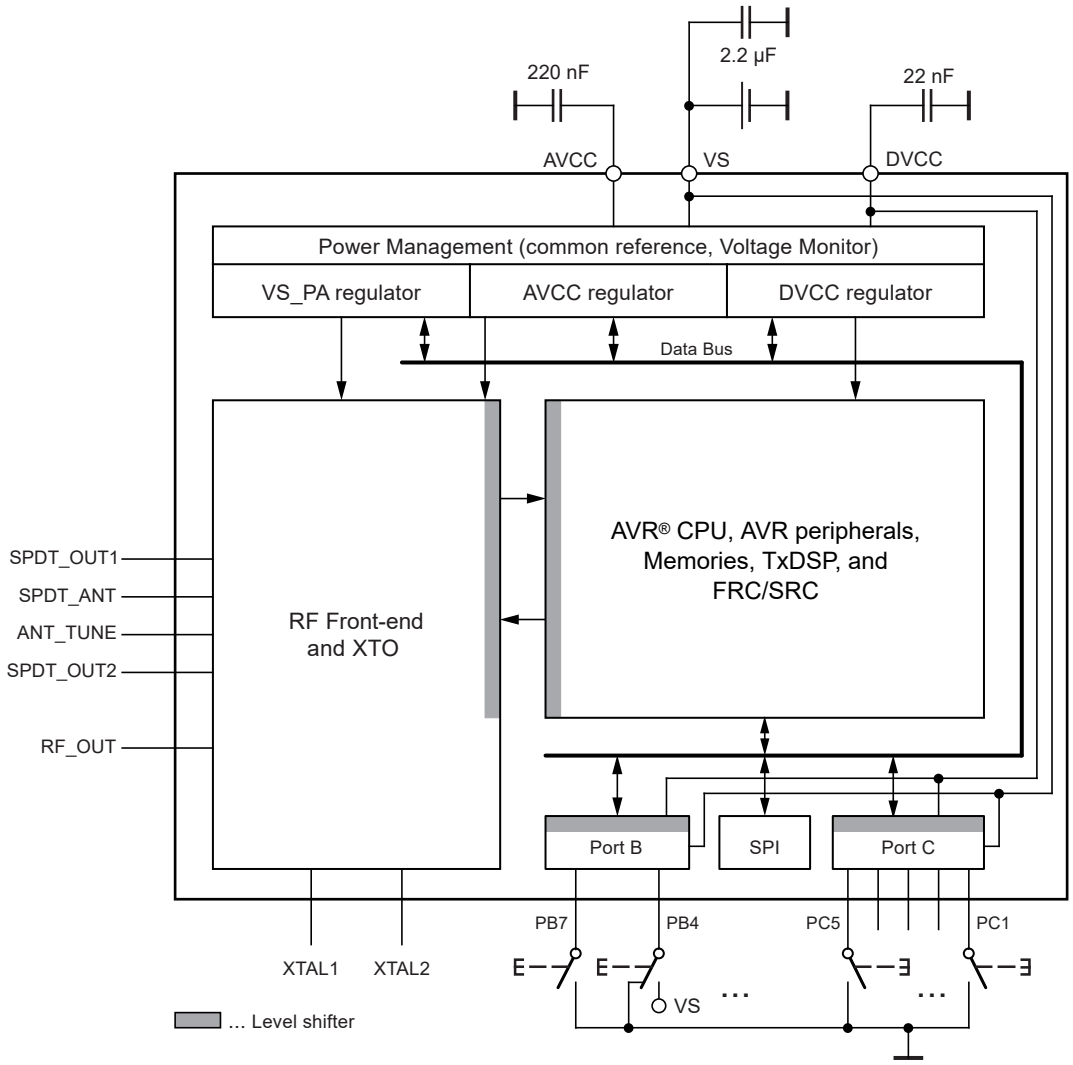
The I/O memory space contains 64 addresses for CPU peripheral functions as control registers, SPI, and other I/O functions. The I/O memory can be accessed directly or as the data space locations following the register file, 0x20-0x5F. In addition, the circuit has extended I/O space from 0x60-0x1FF, and SRAM, where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

4.3 Power Management

The IC has the following power domains:

1. VS – Unregulated battery voltage input. This must be from 1.9V to 3.6V.
2. DVCC – Internally regulated digital supply voltage. The typical value is 1.35V.
3. AVCC – Internally regulated RF front-end and XTO supply. The typical value is 1.85V.

Figure 4-4. Power Supply Management



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Junction temperature	T_j	—	+150	°C
Storage temperature	T_{stg}	-55	+125	°C
Ambient temperature	T_{amb}	-40	+85	°C
Supply voltage	V_{VS}	-0.3	4.0	V
Supply voltage PA (1.9-3.6V application)	V_{VS_PA}	-0.3	4.0	V
ESD (Human Body Model) all pins	HBM	-4	+4	kV
ESD (Machine Model) all pins	MM	-200	+200	V
ESD (Field-Induced Charged-Device Model) all pins	FCDM	-750	+750	V
Maximum RF amplitude at pin 5 (ANT_TUNE)(1)	ANTTUNE	—	4.0	V_p
Maximum peak voltage at pin 4 (SPDT_ANT)(1)	SPDTANT	-0.3	VS + 0.3	V
Maximum peak voltage at pin 3 (SPDT_OUT1)(1)	SPDTOUT1	-0.3	VS + 0.3	V
Maximum peak voltage at pin 6 (SPDT_OUT2)(1)	SPDTOUT2	-0.3	VS + 0.3	V

Note:

1. Customer application needs to be adequately designed.

⚠ CAUTION Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Thermal Resistance

Table 5-2. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal Resistance, Junction Ambient, Soldered according to JEDEC	R_{th_JA}	35	K/W

5.3 Supply Voltages and Current Consumption

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C and a typical process unless otherwise specified. Crystal oscillator frequency, f_{XTO}, = 24.305 MHz.

Table 5-3. Supply Voltages and Current Consumption

No.	Parameters	Test Conditions		Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
1.00	Supply voltage range (VS)	3V application(2)		13	V_{VS}	1.9	3.0	3.6	V	A
1.05	Supply voltage rise time	—		13	V_{VS_rise}	—	—	1	V/µs	D
1.10	Supply voltage range (VS_PA)	3V application(2)		8	V_{VS_PA}	1.9	3	3.6	V	A
1.20	OFFMode current consumption	3V application(2)		8, 13	—	—	—	—	—	—
		T_{amb} = 25°C			$I_{OFFMode\_3V}$	—	5	150	nA	B
		T_{amb} = 85°C						600	nA	B
1.30	IDLEMode(RC) current consumption	SRC active, AVR® in power-down mode, temperature range -40°C to +65°C		13	$I_{IDLEMode(RC)}$	—	50	90	µA	B
1.40	IDLEMode(XTO) current consumption	XTO active, AVR® in Power-down mode		13	$I_{IDLEMode(XTO)}$	—	250	400	µA	B
1.60	IDLEMode(XTO) current consumption	With active CLK_OUT $f_{XTO}/6$ = 4.05 MHz $C_{LOAD\_CLK\_OUT}$ = 10 pF V_{VS} = 3.6V AVR® running with $f_{XTO}/4$ = 6.076 MHz		13, 22	$I_{IDLEMode(XTO)\_CLK\_OUT2}$	—	1.3	2.5	mA	B
2.00	TXMode current consumption (V_{VS} = 3V)	P_{out} = +6 dBm(2)	f_{RF} = 315 MHz	7, 8, 13	I_{TXMode}	—	8.9	11	mA	B
			f_{RF} = 433.92 MHz				9.4	12		B
			f_{RF} = 868.3 MHz				11.5	14.5		B
			f_{RF} = 915 MHz				11.7	15		B
		P_{out} = +10 dBm(2)	f_{RF} = 315 MHz				13.1	17		B
			f_{RF} = 433.92 MHz				13.8	18.5		B
			f_{RF} = 868.3 MHz				17.4	22.5		B
			f_{RF} = 915 MHz				17.4	23		B
		P_{out} = +14 dBm(2)	f_{RF} = 315 MHz				24.3	33		B
			f_{RF} = 433.92 MHz				26.3	36		B
			f_{RF} = 868.3 MHz				32.7	45		B
			f_{RF} = 915 MHz				33.5	46		B

Notes:

1. Type indicates the following:
   - A = 100% tested
   - B = 100% correlation tested
   - C = Characterized on samples
   - D = Design parameter Pin number in brackets means that they are measured matched to 50Ω on the application board
2. Standard EEPROM settings are used.

5.4 RF Transmit Characteristics

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C and a typical process unless otherwise specified. Crystal oscillator frequency, f_{XTO}, = 24.305 MHz.

Table 5-4. RF Transmit Characteristics(2)

No.	Parameters	Test Conditions		Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
Frequency Ranges and Frequency Resolution of PLL										
TXMode Transmit Characteristics										
10.00	Output power range	T_{amb} = 25°C		7	P_{Range}	-12	—	+14.5	dBm	B
10.10	Output power programming steps	Optimum load impedance for each power step. Up to two times higher steps for fixed load impedance.		7	ΔP_{OUT}	—	0.4	—	dB	C
10.20	Output power at 6 dBm	T_{amb} = 25°C using 6 dBm matching FEPAC = 35 (low-band) FEPAC = 36 (high-band)		7	P_{out_6dBm}	-1.5 dB	6	+1.5 dB	dBm	B
10.30	Output 2nd harmonic at 6 dBm	T_{amb} = 25°C, using 6 dBm matching	315 MHz, FEPAC = 35	7	$HM2_{6dBm}$	—	-30	—	dBc	C
			433.92 MHz, FEPAC = 35				-36			C
			868.3 MHz, FEPAC = 36				-35			C
			915 MHz, FEPAC = 36				-35			C
10.40	Output 3rd harmonic at 6 dBm	T_{amb} = 25°C, using 6 dBm matching	315 MHz, FEPAC = 35	7	$HM3_{6dBm}$	—	−33	—	dBc	C
			433.92 MHz, FEPAC = 35				-41			C
			868.3 MHz, FEPAC = 36				-58			C
			915 MHz, FEPAC = 36				-58			C
10.50	TXMode current consumption at 6 dBm	6 dBm matching	315 MHz, FEPAC = 35	7, 8, 13	I_{TXMode_6dBm}	—	8.7	11	mA	B
			433.92 MHz, FEPAC = 35				9.1	12		B
			868.3 MHz, FEPAC = 36				11.5	14.5		B
			915 MHz, FEPAC = 36				11.7	15		B
10.60	Output power at 10 dBm	T_{amb} = 25°C using 10 dBm matching FEPAC = 46 (low-band) FEPAC = 47 (high-band)		7	P_{out_10dBm}	-1.5 dB	10	+1.5 dB	dBm	B
10.70	Output 2nd harmonic at 10 dBm	T_{amb} = 25°C, using 10 dBm matching	315 MHz, FEPAC = 46	7	$HM2_{10dBm}$	—	-24	—	dBc	C
			433.92 MHz, FEPAC = 46				-28			C
			868.3 MHz, FEPAC = 47				-24			C
			915 MHz, FEPAC = 47				-27			C

.....continued

No.	Parameters	Test Conditions		Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
10.80	Output 3rd harmonic at 10 dBm	T_{amb} = 25°C, using 10 dBm matching	315 MHz, FEPAC = 46	7	$HM3_{10dBm}$	—	-25	—	dBc	C
			433.92 MHz, FEPAC = 46				-34			C
			868.3 MHz, FEPAC = 47				-50			C
			915 MHz, FEPAC = 47				-55			C
10.90	TXMode current consumption at 10 dBm	10 dBm matching	315 MHz, FEPAC = 46	7, 8, 13	I_{TXMode_10dBm}	—	13.1	17	mA	B
			433.92 MHz, FEPAC = 46				13.8	18.5		B
			868.3 MHz, FEPAC = 47				17.4	22.5		B
			915 MHz, FEPAC = 47				17.4	23		B
11.00	Output power at 14 dBm	T_{amb} = 25°C using 14 dBm matching FEPAC = 56 (low-band) FEPAC = 57 (high-band)		7	P_{out_14dBm}	-1.5 dB	14	+1.5 dB	dBm	B
11.10	Output 2nd harmonic at 14 dBm	T_{amb} = 25°C, using 14 dBm matching	315 MHz, FEPAC = 56	7	$HM2_{14dBm}$	—	-30	—	dBc	C
			433.92 MHz, FEPAC = 56				-30			C
			868.3 MHz, FEPAC = 57				-24			C
			915 MHz, FEPAC = 57				-24			C
11.20	Output 3rd harmonic at 14 dBm	T_{amb} = 25°C, using 14 dBm matching	315 MHz, FEPAC = 56	7	$HM3_{14dBm}$	—	-30	—	dBc	C
			433.92 MHz, FEPAC = 56				-31			C
			868.3 MHz, FEPAC = 57				-50			C
			915 MHz, FEPAC = 57				-51			C
11.30	TXMode current consumption at 14 dBm	14 dBm matching	315 MHz, FEPAC = 56	7, 8, 13	I_{TXMode_14dBm}	—	24.3	33	mA	B
			433.92 MHz, FEPAC = 56				26.3	36		B
			868.3 MHz, FEPAC = 57				32.7	45		B
			915 MHz, FEPAC = 57				33.5	46		B
11.40	Output power change 1 full temperature and supply voltage range	Low-band	V_{VS} = 3.0V	7	$\Delta P_{TambVs2}$	-1.5	—	+1.5	dB	C
		High-band 0 to ≤10 dBm P = P_{out} + ΔP	V_{VS} = 1.9V to 3.6V			-5.5	—	+2.5		C
11.50	Output power change 2 full temperature and supply voltage range	High-band > 10 dBm to 14 dBm P = P_{out} + ΔP	V_{VS} = 3.0V	7	$\Delta P_{TambVs2}$	-3	—	+1.5	dB	C
			V_{VS} = 2.1V to 3.6V			-6		+3		C
11.60	Spurious emission	Low-band	at ±f_{XTO}	7	SP_{TX}	—	-80	-65	dBc	B
			at ±f_{AVR} (f_{XTO}/4)				-85	-65		C
			at ± f_{CLK_OUT} (f_{XTO}/6)				-80	-65		C
		High-band	at ±f_{XTO}				-72	-60		B
			at ±f_{AVR} (f_{XTO}/4)				-85	-60		C
			at ± f_{CLK_OUT} (f_{XTO}/6)				-78	-60		C

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
11.70	TX transparent data rate in Manchester and NRZ mode	Manchester mode	18, 7	$DR_{TX\_TM\_MAN}$	—	—	80	Kbit/s	B
		NRZ mode Pre-emphasis enabled for symbol rates higher than 40 Kbits		$DR_{TX\_TM\_NRZ}$	—	—	160	Ksym/s	B
11.80	TX buffered data rate in Manchester and NRZ mode	Manchester mode	—	$DR_{TX\_BUF\_MAN}$	—	—	80	Kbit/s	B
		NRZ mode		$DR_{TX\_BUF\_NRZ}$			120	Ksym/s	B
11.90	TX buffered data rate programming step in Manchester and NRZ mode	AVR running with $f_{XTO}/4$	7	ΔDR_{BUF}	—	—	1	%	D
Antenna Tuning and SPDT in TXMode									
12.00	Antenna tuning capacitor range	FEAT.ANTN(3:0) = 0 to 15	5	C_{TUNE_RANGE}	4	—	9	pF	B
12.10	Antenna tuning capacitor resolution	4 bits controlled with RF front-end register FEAT.ANT(3:0) available	5	C_{TUNE_RES}	—	0.16	0.2	pF	C
12.20	Antenna tuning series resistance	The series resistance influences the quality factor of the loop antenna and causes radiated TX power losses	5	$C_{TUNE\_SRESIST}$	—	2.5	4	Ω	C
12.30	Antenna tuning maximum RF amplitude	If higher levels occur in the application, an external capacitor to GND is needed to reduce the amplitude.	5	$C_{TUNE\_RFAMP\_MAX}$	—	—	3	Vp	D
12.40	Insertion loss SPDT_ANT to SPDT_OUT2	Low-band	4, 6	IL_{Switch_TX2}	—	0.5	1.1	dB	C
		High-band				0.7	1.2		
12.42	Insertion loss SPDT_ANT to SPDT_OUT1	Low-band	4, 3	IL_{Switch_TX1}	—	0.7	1.1	dB	C
		High-band				1.0	1.4		
12.45	Maximum peak voltage on SPDT_ANT (pin 4)	—	4	$V_{PEAK\_SPDT\_ANT}$	-0.3	—	VS + 0.3	V	D
12.50	Maximum peak voltage on SPDT_OUT2 (pin 6)	—	6	$V_{PEAK\_SPDT\_TX\_OUT2}$	-0.3	—	VS + 0.3	V	D
12.55	Maximum peak voltage on SPDT_OUT1 (pin 3)	—	3	$V_{PEAK\_SPDT\_TX\_OUT2}$	-0.3	—	VS + 0.3	V	D
12.60	1 dB compression point	Low-band	6	CP1dB_TX2	14.5	16	—	dBm	D
		High-band			14.5	16			
12.65	1 dB compression point	Low-band	3	CP1dB_TX1	13.5	15	—	dBm	D
		High-band			9.5	11			

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)

Notes:

1. Type indicates the following:
   - A = 100% tested
   - B = 100% correlation tested
   - C = Characterized on samples
   - D = Design parameter Pin number in brackets means that they are measured matched to 50Ω on the application board
2. Standard EEPROM settings are used.

5.5 Oscillators and CLK_OUT

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances, quartz parameters C_m = 4 fF and C0 = 1 pF unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C and a typical process unless otherwise specified. Crystal oscillator frequency, f_{XTO}, = 24.305 MHz.

Table 5-5. Oscillator and CLK_OUT Characteristics(2)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
13.00	CLK_OUT equivalent internal capacitance	Used for current calculation	13, 22	C_{CLK}	—	7.5	10	pF	C
13.10	Supply current increase CLK_OUT active	Calculation can be applied to all operation modes except OFFMode	13	ΔI_{CLK}	$(C_{CLK} + C_{LOAD\_CLK\_OUT}) \times V_{VS} \times f_{OUT}$			A	C
13.30	XTO frequency range	—	10, 11	f_{XTO}	23.8	24.305	26.2	MHz	C
13.40	XTO pulling due to internal capacitance and XTO tolerance	C_m = 4 fF T_{amb} = 25°C	10, 11	ΔF_{XTO1}	-10	—	+10	ppm	B
13.50	XTO pulling due to temperature and supply voltage	C_m = 4 fF T_{amb} = -40°C to +85°C	10, 11	ΔF_{XTO2}	-4	—	+4	ppm	B
13.60	Maximum C_0 of XTAL	XTAL parameter	10, 11	C_{0_max}	—	1	2	pF	D
13.70	XTAL, C_m motional capacitance	XTAL parameter	10, 11	C_m	—	4	10	fF	D
13.80	XTAL, real part of XTO impedance at start-up	C_m = 4 fF C_0 = 1 pF	10, 11	R_{m_start1}	950	—	—	Ω	B
13.90	XTAL, real part of XTO impedance at start-up	C_m = 4 fF C_0 = 1 pF T_{amb} < 85°C	10, 11	R_{e_start2}	1100	—	—	Ω	B
14.00	XTAL, maximum Rm after start-up	XTAL parameter	10, 11	R_{m_max}	—	—	110	Ω	D
14.10	Internal load capacitors	Including ESD and package capacitance. XTAL must be specified for 7.5 pF load capacitance (incl. 1 pF PCB capacitance per pin)	10, 11	C_{L1}, C_{L2}	13.3	14	14.7	pF	B
14.20	Slow RC oscillator frequency	can be calibrated to ±2% accuracy with f_{XTO}	22	f_{SRC}	-12%	125	+12%	kHz	A
14.30	Fast RC oscillator frequency	can be calibrated to ±2% accuracy with f_{XTO}	22	f_{FRC}	-5%	6.36	+5%	MHz	A

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)

Notes:

1. Type indicates the following:
   - A = 100% tested
   - B = 100% correlation tested
   - C = Characterized on samples
   - D = Design parameter Pin number in brackets means that they are measured matched to 50Ω on the application board.
2. Standard EEPROM settings are used.

5.6 I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9V to 3.6V over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C and a typical process unless otherwise specified. Crystal oscillator frequency, f_{XTO}, = 24.305 MHz.

Table 5-6. I/O Port Characteristics(2)

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
15.00	Input low voltage	PC0 to PC5 PB0 to PB7	14-19, 22-29	V_{IL}	-0.3	—	0.2 x V_{VS}	V	A
15.05	Input low leakage current I/O pin	PC0 to PC5 PB0 to PB7	14-19, 22-29	I_{IL}	—	—	-1	µA	A
15.10	Input high voltage	PC0 to PC5 PB0 to PB7	14-19, 22-29	V_{IH}	0.8 x V_{VS}	—	V_{VS} + 0.3	V	A
15.15	Input high leakage current I/O pin	PC0 to PC5 PB0 to PB7	14-19, 22-29	I_{IH}	—	—	1	µA	A
15.20	Output low voltage	I_{OL} = 0.2 mA	14-19, 22-29	V_{OL_3V}	—	—	0.1 x V_{VS}	V	A
15.30	Output high voltage	I_{OH} = -0.2 mA	14-19, 22-29	V_{OH_3V}	0.9 x V_{VS}	—	—	V	A
15.40	I/O pin pull-up resistor	OFFMode: see port B and port C	14-19, 22-29	R_{PU}	30	50	70	kΩ	A
15.50	Output low voltage for strong LED low-side driver (PB7)	Configurable on pin PB7 I_{LOAD} = 1.5 mA	29	V_{OL_STR1}	—	—	0.1 x V_{VS}	V	A
15.60	Output high voltage for strong LED high-side driver (PB7, PB4)	Configurable on pin PB7 and PB4 I_{LOAD} = -1.5 mA	26, 29	V_{OH_STR1}	0.9 x V_{VS}	—	—	V	A

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
15.70	Output low voltage for strong ISP low-side driver (PB3)	Activated in ISP mode, T_{amb} = -40°C to +65°C, I_{OL} = 1.7 mA, V_{VS} > 2.5V	25	V_{OL_STR2}	—	—	0.1 x V_{VS}	V	B
15.80	Output high voltage for strong ISP high-side driver (PB3)	Activated in ISP mode, T_{amb} = -40°C to +65°C, I_{OL} = 1.7 mA, V_{VS} > 2.5V	25	V_{OH_STR2}	0.9 x V_{VS}	—	—	V	B
15.90	CLK_OUT output frequency	XTO, FRC or SRC related clock $f_{CLK\_OUT} = f_{OSC}/(2*CLKOD)$	22	f_{CLK_OUT}	—	—	4.5	MHz	B
16.00	CLK_OUT duty cycle	$C_{LOAD\_CLK\_OUT}$ = 10 pF f_{CLK_OUT} = 4.5 MHz	22	DTY_{CLK_OUT}	45	—	55	%	A
16.10	I/O pin output delay time (rising edge)	3V application C_{Load} = 10 pF	14-19, 22-29	$T_{del\_rise\_3V}$	13.6	17.5	22.4	ns	D
16.20	I/O pin rise time (0.1 x V_{VS} to 0.9 x V_{VS})	3V application C_{Load} = 10 pF	14-19, 22-29	T_{rise_3V}	20.7	23.9	28.4	ns	D
16.30	I/O pin slew rate (rising edge)	3V application C_{Load} = 10 pF	14-19, 22-29	$T_{sr\_rise\_3V}$	0.115	0.100	0.084	V/ns	D
16.40	I/O pin output delay time (falling edge)	3V application C_{Load} = 10 pF	14-19, 22-29	$T_{del\_fall\_3V}$	13.7	17.4	22.7	ns	D
16.50	I/O pin fall time (0.9 x V_{VS} to 0.1 x V_{VS})	3V application C_{Load} = 10 pF	14-19, 22-29	T_{fall_3V}	16.2	19.2	22.5	ns	D
16.60	I/O pin slew rate (falling edge)	3V application C_{Load} = 10 pF	14-19, 22-29	$T_{sr\_fall\_3V}$	0.148	0.125	0.106	V/ns	D

Notes:

1. Type indicates the following:
   - A = 100% tested
   - B = 100% correlation tested
   - C = Characterized on samples
   - D = Design parameter Pin number in brackets means that they are measured matched to 50Ω on the application board.
2. Standard EEPROM settings are used.

5.7 Hardware Timings

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to + 85°C, V_{VS} =1.9V to 3.6V over all process tolerances. Typical values are given at V_{VS} = 3V, T_{amb} = 25°C and a typical process unless otherwise specified. Crystal oscillator frequency, f_{XTO}, = 24.305 MHz.

Table 5-7. Hardware Timing Characteristics(2)

No.	Parameters	Test Conditions		Pin	Symbol	Min.	Typ.	Max.	Unit	Type(1)
17.00	Start-up Time XTO	AVCC already enabled and ready C_0 < 1.5 pF 4 fF < C_m < 15 fF	R_m < 110Ω	10, 11	T_{Start_XTO}	90	130	250	µs	B
			R_m < 800Ω					1500	µs	C
17.10	Erase and Write EEPROM	using ISP commands or SPI commands “Write EEPROM”		14, 23, 24, 25	$T_{EE\_ER\_WR}$	—	—	10	ms	B
17.20	Erase Only EEPROM	using ISP commands		14, 23, 24, 25	T_{EE_ER}	—	—	5	ms	B
17.30	Write Only EEPROM	using ISP commands		14, 23, 24, 25	T_{EE_WR}	—	—	5	ms	B
17.50	System Initialization Start-up Time	PWRON = 1 or NPWRON = 0 to INTERNAL RESET removal		13, 20	$T_{SYSINIT1}$	80	—	200	µs	B

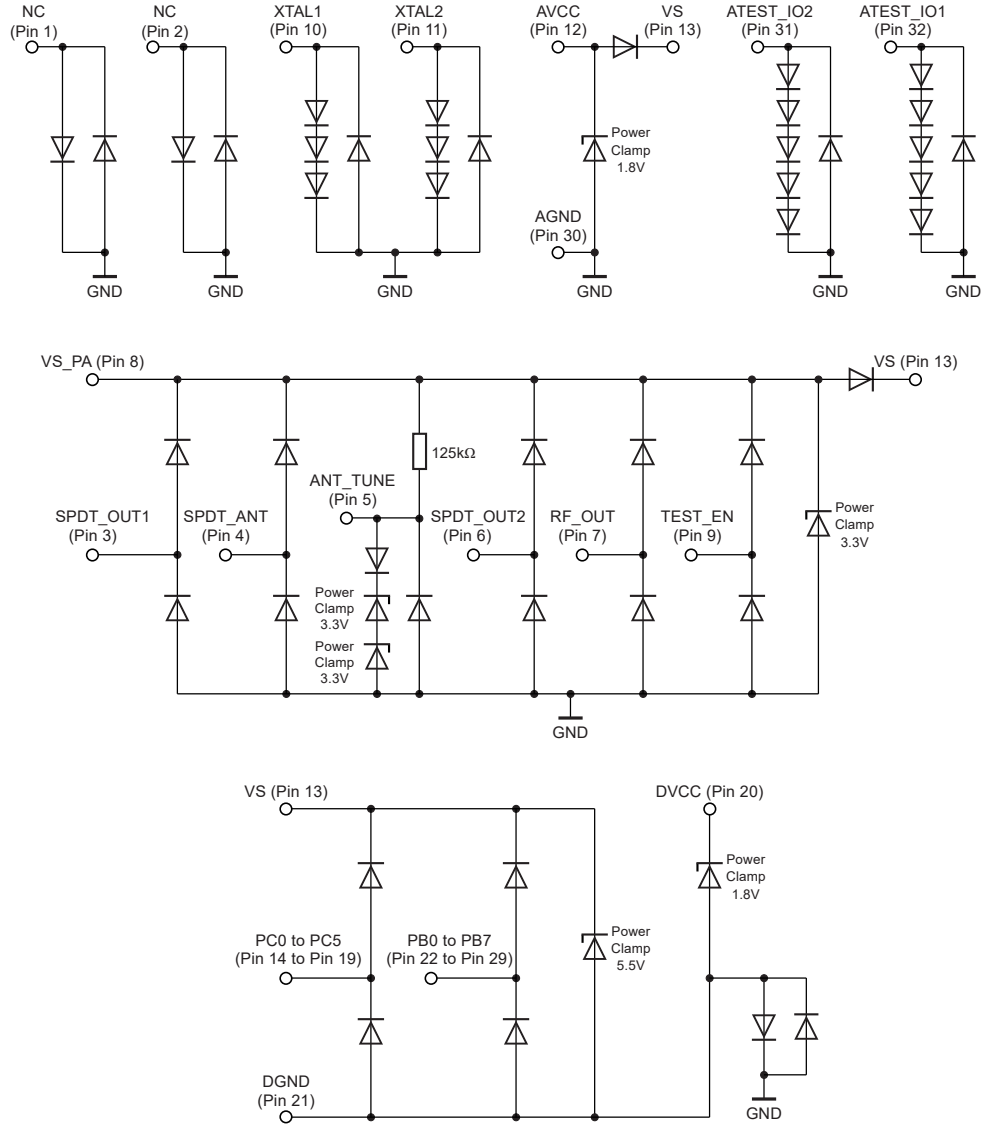
Notes:

1. Type indicates the following:
   - A = 100% tested
   - B = 100% correlation tested
   - C = Characterized on samples
   - D = Design parameter Pin number in brackets means that they are measured matched to 50Ω on the application board
2. Standard EEPROM settings are used.

5.8 ESD Protection Circuits

GND is the exposed die pad of the ATA8710, which is internally connected to AGND (pin 30). The following figure illustrates that all Zener diodes (marked as power clamps) are realized with dynamic clamping circuits and not physical Zener diodes. Therefore, DC currents are not clamped to the shown voltages.

Figure 5-1. ATA8710 ESD Protection Circuit



6. Ordering Information

The following table provides the ordering details of the ATA8710.

Table 6-1. Ordering Information

Ordering Number	Package	Description
ATA8710-GHQW	QFN32	5 mm x 5 mm, 6k tape and reel, PB-free, 20 Kbytes Flash program memory

7. Package Information

Note: For the most current package drawings, refer to the Microchip Packaging Specification at www.microchip.com/packaging.

Figure 7-1. ATA8710 Packaging Dimension

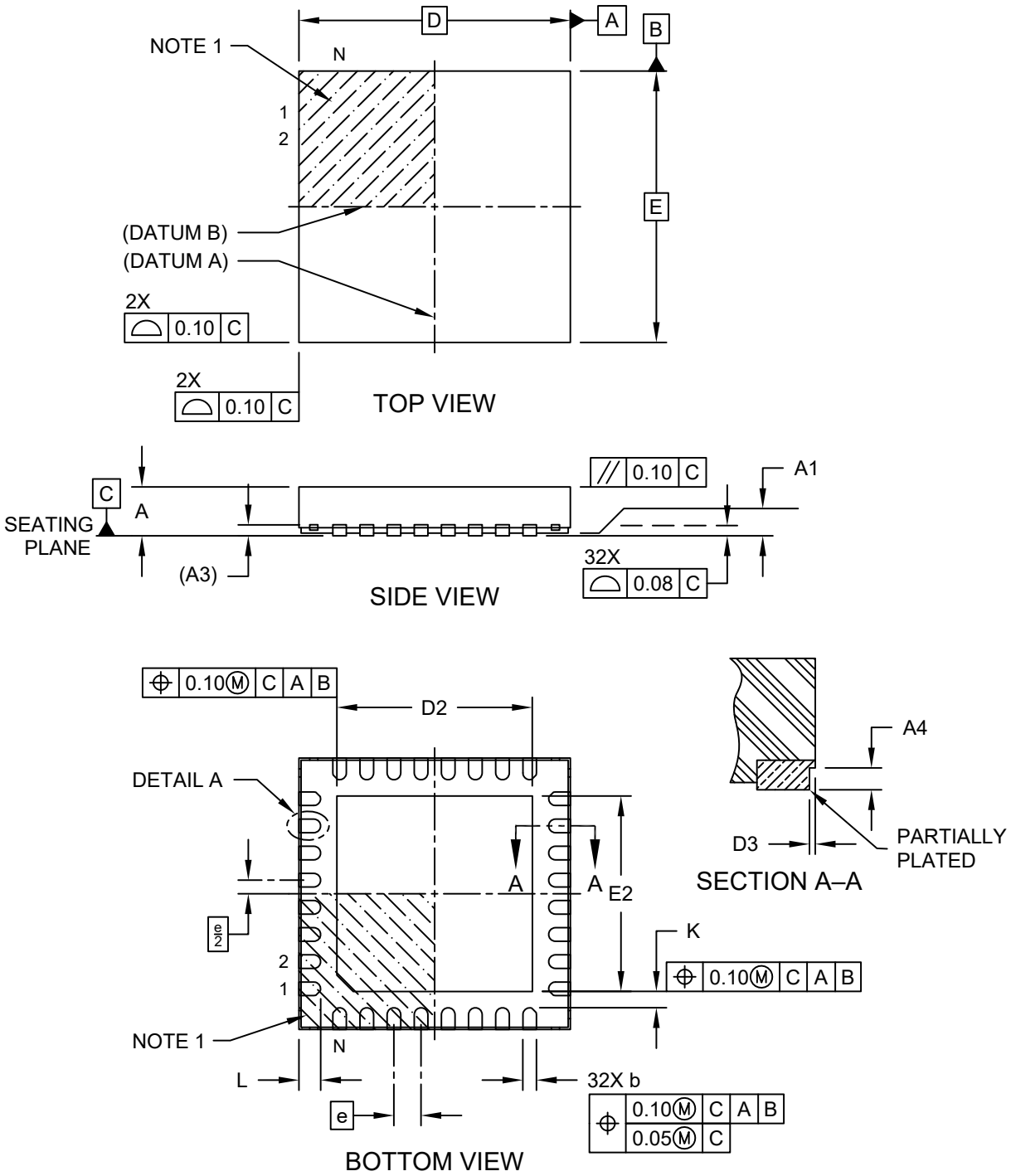
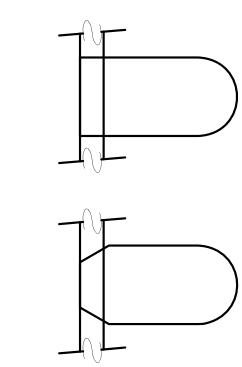
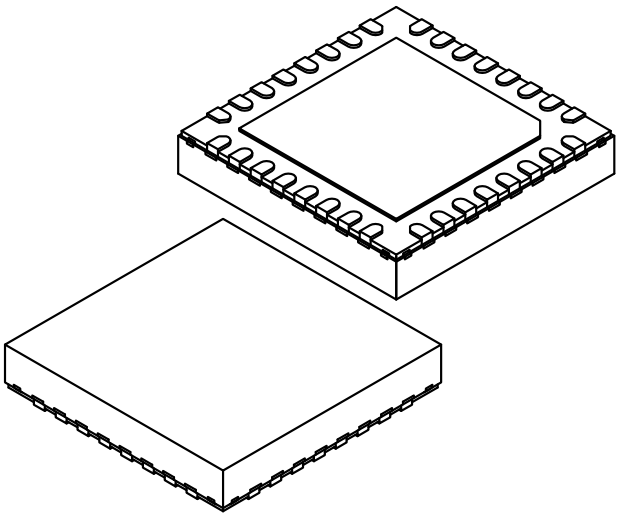


Figure 7-2. ATA8710 Packaging Outline Drawing



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Width	D3	-	-	0.085
Wettable Flank Step Cut Depth	A4	0.10	-	0.19

Dimensions D3 and A4 above apply to all new products released after November 1, and all products shipped after January 1, 2019, and supersede dimensions D3 and A4 below.
No physical changes are being made to any package; this update is to align cosmetic and tolerance variations from existing suppliers.

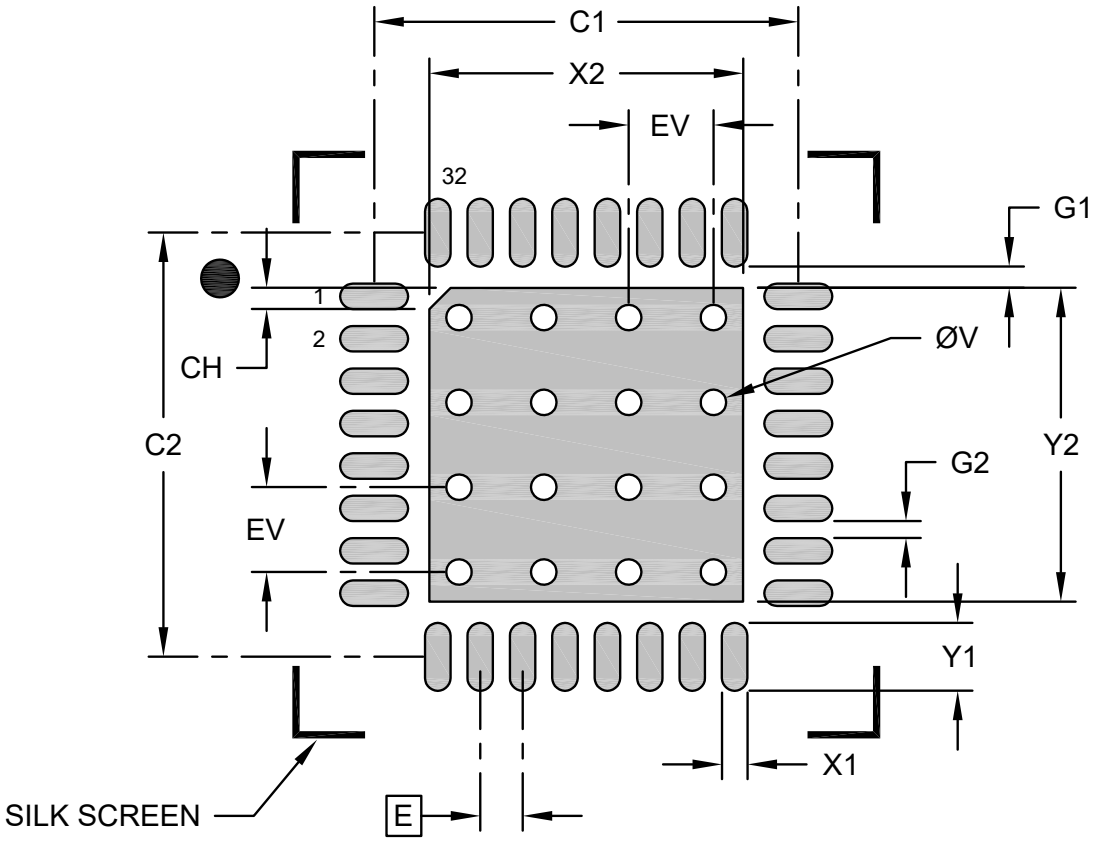
Wettable Flank Step Length	D3	0.035	0.06	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Figure 7-3. ATA8710 – Recommended Land Pattern



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Exposed Pad 45° Corner Chamfer	CH		0.25	
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.80
Contact Pad to Center Pad (X32)	G1	0.25		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

8. Document Revision History

Revision	Date	Section	Description
A	09/2021	Document	Initial revision

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