



# AT27C512R

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## 512-Kbit (64K x 8) One-Time Programmable, Read-Only Memory

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### Features

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- Fast Read Access Time: 45 ns
- Low-Power CMOS Operation:
  - 100  $\mu$ A maximum standby
  - 20 mA maximum active at 5 MHz
- 5V  $\pm$  10% Supply
- High Reliability CMOS Technology:
  - 2,000V ESD protection
  - 200 mA latch-up immunity
- Rapid Programming Algorithm – 100  $\mu$ s/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Industrial Temperature Range: -40°C to +85°C
- Green Package Options (Lead-free/Halide-free/RoHS compliant)

### Packages

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- 32-Lead PLCC and 28-Lead PDIP

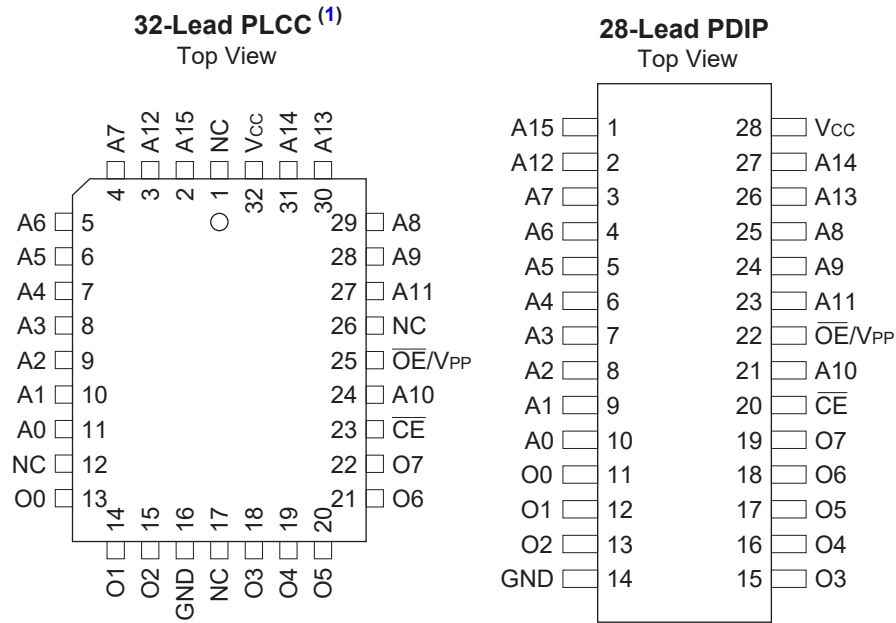
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### 1. Package Types (not to scale)



**Note:**

1. PLCC package pins 1, 12, 17 and 26 are not connected.

## 2. Pin Description

The description of the pins are listed in [Table 2.1](#).

**Table 2-1. Pin Description**

Name	32-Lead PLCC	28-Lead PDIP	Function
A0 - A15	2-11; 24; 27-31	1-10; 21; 23-27	Address Inputs
O0 - O7	13-15; 18-22	11-13; 15-19	Outputs
$\overline{CE}$	23	20	Chip Enable
$\overline{OE}/V_{PP}$	25	22	Output Enable/Program Supply
NC	1; 12; 17; 26	—	Not Connected
$V_{CC}$	32	28	Device Power Supply
GND	16	14	Ground

### 3. Description

The Microchip AT27C512R is a low-power, high-performance, 524,288-bit, One-Time Programmable, Read-Only memory (OTP EPROM) organized as 65,536 words of 8 bits each. It requires only one 5V power supply in normal Read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed-reducing WAIT states on high-performance microprocessor systems.

The Microchip-scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically only 8 mA in Active mode and less than 10  $\mu$ A in Standby mode.

The AT27C512R is available in a choice of industry-standard, JEDEC-approved, PDIP and PLCC packages. All devices feature two-line control ( $\overline{CE}$ ,  $\overline{OE}$ ) to give designers the flexibility to prevent bus contention.

With 64 Kbyte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

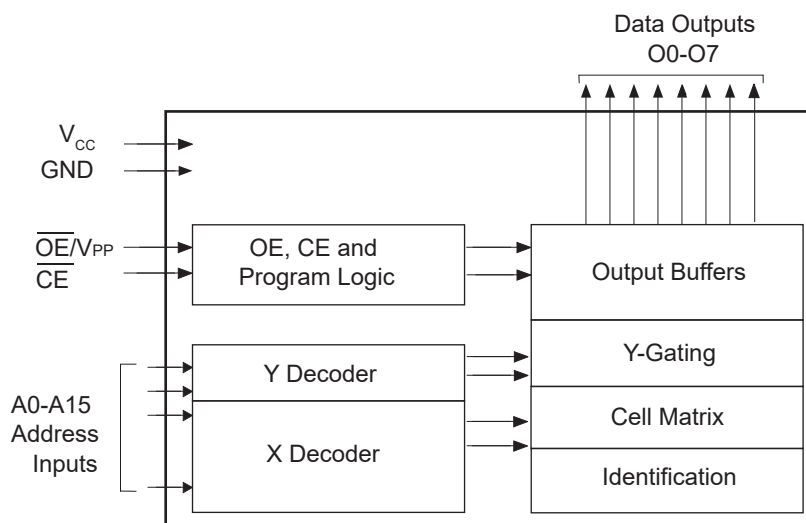
The AT27C512R has additional features to ensure high-quality and efficient production use. The rapid programming algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100  $\mu$ s/byte. The integrated product identification code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages.

### 3.1 System Considerations

Switching between active and standby conditions via the chip enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu$ F, high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the  $V_{CC}$  and ground terminals of the device as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu$ F bulk electrolytic capacitor should be utilized and again connected between the  $V_{CC}$  and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

### 3.2 Block Diagram

Figure 3-1. Block Diagram



## 4. Electrical Characteristics

### 4.1 Absolute Maximum Ratings

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with respect to ground	-2.0V to +14.0V <sup>(1)</sup>
V <sub>PP</sub> supply voltage with respect to ground	-2.0V to +14.0V <sup>(1)</sup>

**Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note:**

1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V<sub>CC</sub> +0.75V DC, which may overshoot to +7.0V for pulses of less than 20 ns.

### 4.2 DC and AC Operating Range

**Table 4-1. DC and AC Operating Range**

Mode/Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	Outputs
Read	V <sub>IL</sub>	V <sub>IL</sub>	Ai	D <sub>OUT</sub>
Output disable	V <sub>IL</sub>	V <sub>IH</sub>	X <sup>(1)</sup>	High-Z
Standby	V <sub>IH</sub>	X <sup>(1)</sup>	X <sup>(1)</sup>	High-Z
Rapid program <sup>(2)</sup>	V <sub>IL</sub>	V <sub>PP</sub>	Ai	D <sub>IN</sub>
PGM inhibit	V <sub>IH</sub>	V <sub>PP</sub>	X <sup>(1)</sup>	High-Z
Product identification <sup>(4)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	A9 = V <sub>H</sub> <sup>(3)</sup> , A0 = V <sub>IH</sub> or V <sub>IL</sub> A1-A15 = V <sub>IL</sub>	Identification code

**Notes:**

1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
2. Refer to programming characteristics.
3. V<sub>H</sub> = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V<sub>IL</sub>), except A9, which is set to V<sub>H</sub>, and A0, which is toggled low (V<sub>IL</sub>) to select the manufacturer’s identification byte and high (V<sub>IH</sub>) to select the device code byte.

**Table 4-2. DC and AC Operating Conditions for Read Operation**

AT27C512R		-45	-70
Operating Temperature (Case)	Industrial Temperature Range	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Supply		5V ± 10%	5V ± 10%

### 4.3 DC and Operating Characteristics for Read Operation

Table 4-3. DC and Operating Characteristics for Read Operation

Parameter	Symbol	Minimum	Maximum	Units	Condition	
Input Load Current	$I_{LI}$	—	$\pm 1$	$\mu A$	Industrial	$V_{IN} = 0V$ to $V_{CC}$
Output Leakage Current	$I_{LO}$	—	$\pm 5$	$\mu A$	Industrial	$V_{OUT} = 0V$ to $V_{CC}$
$V_{CC}^{(1)}$ Standby Current	$I_{SB}$	—	100	$\mu A$	$I_{SB1}$ (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$	
			1	mA	$I_{SB2}$ (TTL), $\overline{CE} = 2.0$ to $V_{CC} + 0.5V$	
$V_{CC}$ Active Current	$I_{CC}$	—	20	mA	$f = 5$ MHz, $I_{OUT} = 0$ mA, $\overline{CE} = V_{IL}$	
Input Low Voltage	$V_{IL}$	-0.6	0.8	V		
Input High Voltage	$V_{IH}$	2.0	$V_{CC} + 0.5$	V		
Output Low Voltage	$V_{OL}$	—	0.4	V	$I_{OL} = 2.1$ mA	
Output High Voltage	$V_{OH}$	2.4	—	—	$I_{OH} = -400$ $\mu A$	

**Note:**

- $V_{CC}$  must be applied simultaneously with or before  $\overline{OE}/V_{PP}$ , and removed simultaneously with or after  $\overline{OE}/V_{PP}$ .

### 4.4 AC Characteristics for Read Operation

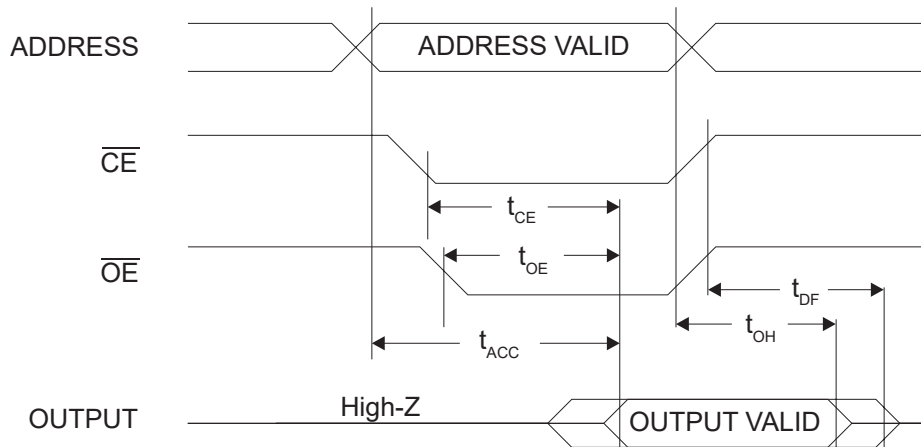
Table 4-4. AC Characteristics for Read Operation

Parameter	Symbol	-45		-70		Units	Condition
		Minimum	Maximum	Minimum	Maximum		
Address to Output Delay	$t_{ACC}^{(1)}$	—	45	—	70	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
$\overline{CE}$ to Output Delay	$t_{CE}^{(1)}$	—	45	—	70	ns	$\overline{OE}/V_{PP} = V_{IL}$
$\overline{OE}/V_{PP}$ to Output Delay	$t_{OE}^{(1)}$	—	20	—	30	ns	$\overline{CE} = V_{IL}$
$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First	$t_{DF}^{(1)}$	—	20	—	25	ns	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float, Whichever Occurred First
Output hold from address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ , whichever occurred first	$t_{OH}$	7	—	7	—	ns	Output hold from address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ , whichever occurred first

**Note:**

- See [Figure 4-1](#).

**Figure 4-1. AC Waveform for Read Operation**

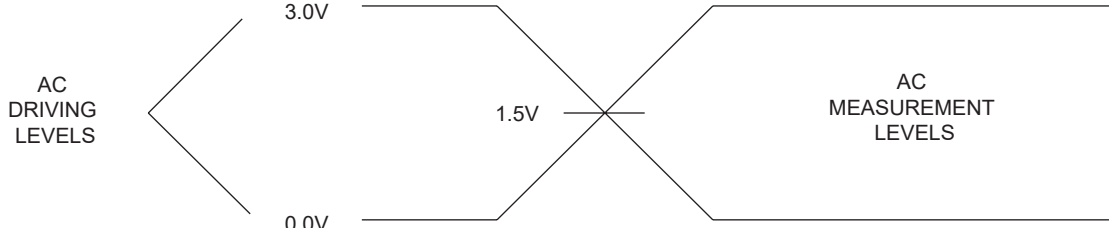


**Notes:**

1. Timing measurement reference level is 1.5V for -45 devices. Input AC drive levels are  $V_{IL} = 0.0V$  and  $V_{IH} = 3.0V$ . Timing measurement reference levels for all other speed grades are  $V_{OL} = 0.8V$  and  $V_{OH} = 2.0V$ . Input AC drive levels are  $V_{IL} = 0.45V$  and  $V_{IH} = 2.4V$ .
2.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
3.  $\overline{OE}/V_{PP}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
4. This parameter is only sampled, and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

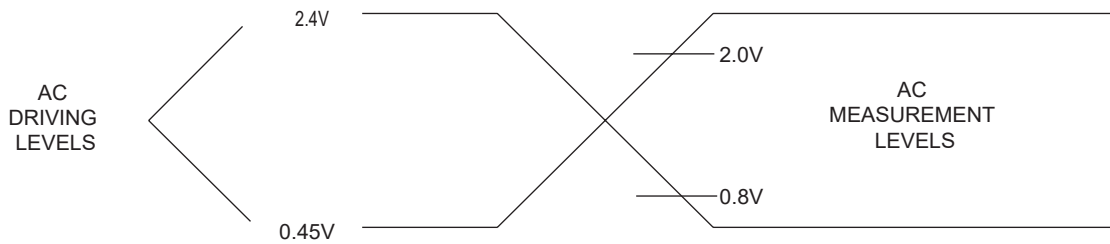
**Figure 4-2. Input Test Waveforms and Measurement Levels**

For -45 devices only:



$t_R, t_F < 5$  ns (10% to 90%)

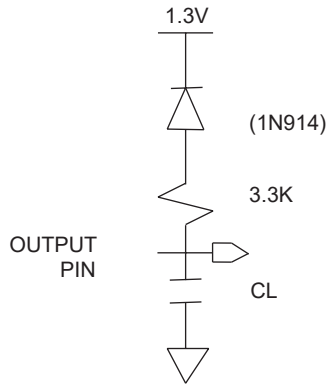
For -70 devices:



$t_R, t_F < 20$  ns (10% to 90%)



**Figure 4-3. Output Test Load**

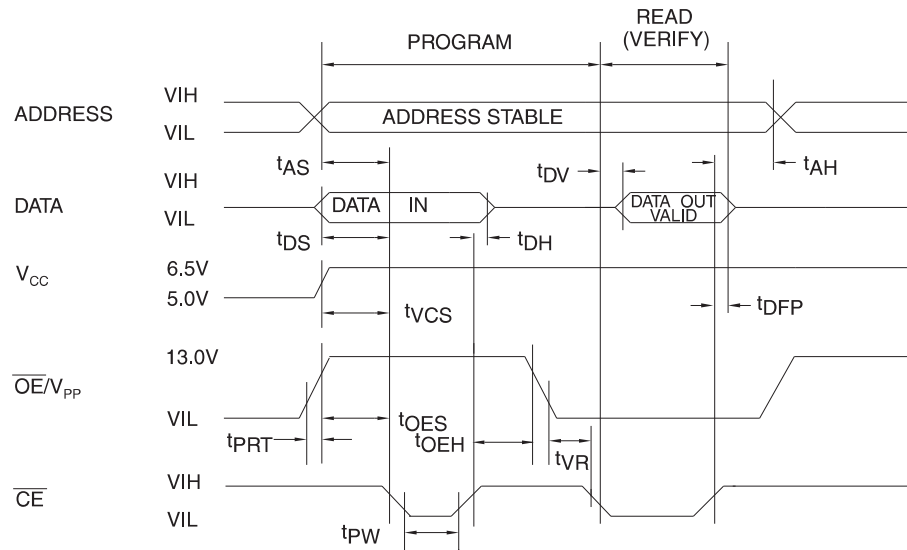


**Note:**

1. CL = 100 pF including jig capacitance, except for the -45 devices, where CL = 30 pF.

## 4.5 Programming waveforms

**Figure 4-4. Programming Waveforms**



**Notes:**

1. The input timing reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device, but must be accommodated by the programmer.
3. When programming the AT27C512R, a 0.1  $\mu$ F capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients.

## 4.6 DC Programming Characteristics

Table 4-5. DC Programming Characteristics <sup>(1)</sup>

Parameter	Symbol	Limits		Units	Test Conditions
		Minimum	Maximum		
Input Load Current	$I_{LI}$	—	$\pm 10$	$\mu A$	$V_{IN} = V_{IL}, V_{IH}$
Input Low Level	$V_{IL}$	-0.6	0.8	V	—
Input High Level	$V_{IH}$	2.0	$V_{CC} + 1$	V	—
Output Low Voltage	$V_{OL}$	—	0.4	V	$I_{OL} = 2.1 \text{ mA}$
Output High Voltage	$V_{OH}$	2.4	—	V	$I_{OH} = -400 \mu A$
$V_{CC}$ Supply Current (Program and Verify)	$I_{CC2}$	—	25	mA	—
$\overline{OE}/V_{PP}$ Current	$I_{PP2}$	—	25	mA	$\overline{CE} = V_{IL}$
A9 Product Identification Voltage	$V_{ID}$	11.5	12.5	V	—

**Note:**

1.  $T_A = +25 \pm 5^\circ C$ ,  $V_{CC} = 6.5 \pm 0.25V$ ,  $\overline{OE}/V_{PP} = 13.0 \pm 0.25V$ .

## 4.7 AC Programming Characteristics

Table 4-6. AC Programming Characteristics <sup>(1)</sup>

Parameter	Symbol	Limits		Units	Test conditions
		Minimum	Maximum		
Address Setup Time	$t_{AS}$	2	—	$\mu s$	Input rise and fall times (10% to 90%) 20 ns Input pulse levels 0.45V to 2.4V Input timing reference level 0.8V to 2.0V Output timing reference level 0.8V to 2.0V
$\overline{OE}/V_{PP}$ Setup Time	$t_{OES}$	2	—	$\mu s$	
$\overline{OE}/V_{PP}$ Hold Time	$t_{OEH}$	2	—	$\mu s$	
Data Setup Time	$t_{DS}$	2	—	$\mu s$	
Address Hold Time	$t_{AH}$	0	—	$\mu s$	
Data Hold Time	$t_{DH}$	2	—	$\mu s$	
$\overline{CE}$ High to Output Float Delay <sup>(3)</sup>	$t_{DFP}$	0	130	ns	
$V_{CC}$ Setup Time	$t_{VCS}$	2	—	$\mu s$	
$\overline{CE}$ Program Pulse Width <sup>(4)</sup>	$t_{PW}$	95	105	$\mu s$	
Data Valid From $\overline{CE}$ <sup>(3)</sup>	$t_{DV}$	—	1	$\mu s$	
$\overline{OE}/V_{PP}$ Recovery Time	$t_{VR}$	2	—	$\mu s$	
$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming	$t_{PRT}$	50	—	ns	

**Notes:**

1.  $T_A = +25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $\overline{OE}/V_{PP} = 13.0 \pm 0.25\text{V}$ .
2.  $V_{CC}$  must be applied simultaneously with or before  $\overline{OE}/V_{PP}$  and removed simultaneously with or after  $\overline{OE}/V_{PP}$ .
3. This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.
4. Program pulse width tolerance is  $100 \mu\text{s} \pm 5\%$ .

## 4.8 Electrical Specifications

### 4.8.1 Pin Capacitance

Table 4-7. Pin Capacitance<sup>(1,2)</sup>

Symbol	Typical	Maximum	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0\text{V}$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0\text{V}$

**Notes:**

1. Typical values for nominal supply voltage. This parameter is only sampled, and is not 100% tested.
2.  $f = 1 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$

## 4.9 Integrated Product Identification Code

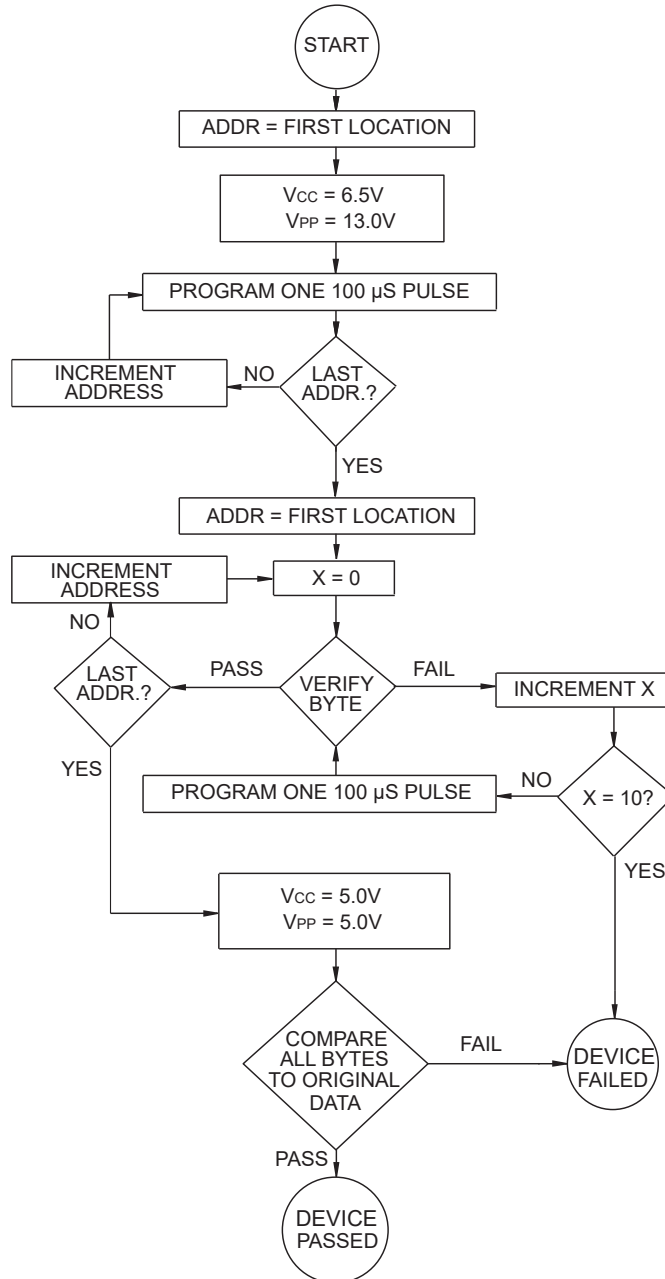
Table 4-8. Integrated Product Identification Code

Codes	Pins									Hex data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device type	1	0	0	0	0	1	1	0	1	0D

## 5. Rapid Programming Algorithm

A 100  $\mu\text{s}$   $\overline{\text{CE}}$  pulse width is used to program. The address is set to the first location.  $V_{\text{CC}}$  is raised to 6.5V and  $\overline{\text{OE}}/V_{\text{PP}}$  is raised to 13.0V. Each address is first programmed with one 100  $\mu\text{s}$   $\overline{\text{CE}}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100  $\mu\text{s}$  pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $\overline{\text{OE}}/V_{\text{PP}}$  is then lowered to  $V_{\text{IL}}$  and  $V_{\text{CC}}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

**Figure 5-1. Rapid Programming Algorithm**



**6. Packaging Information**

**6.1 Package Marking Information**

**AT27C512R: Package Marking Information**

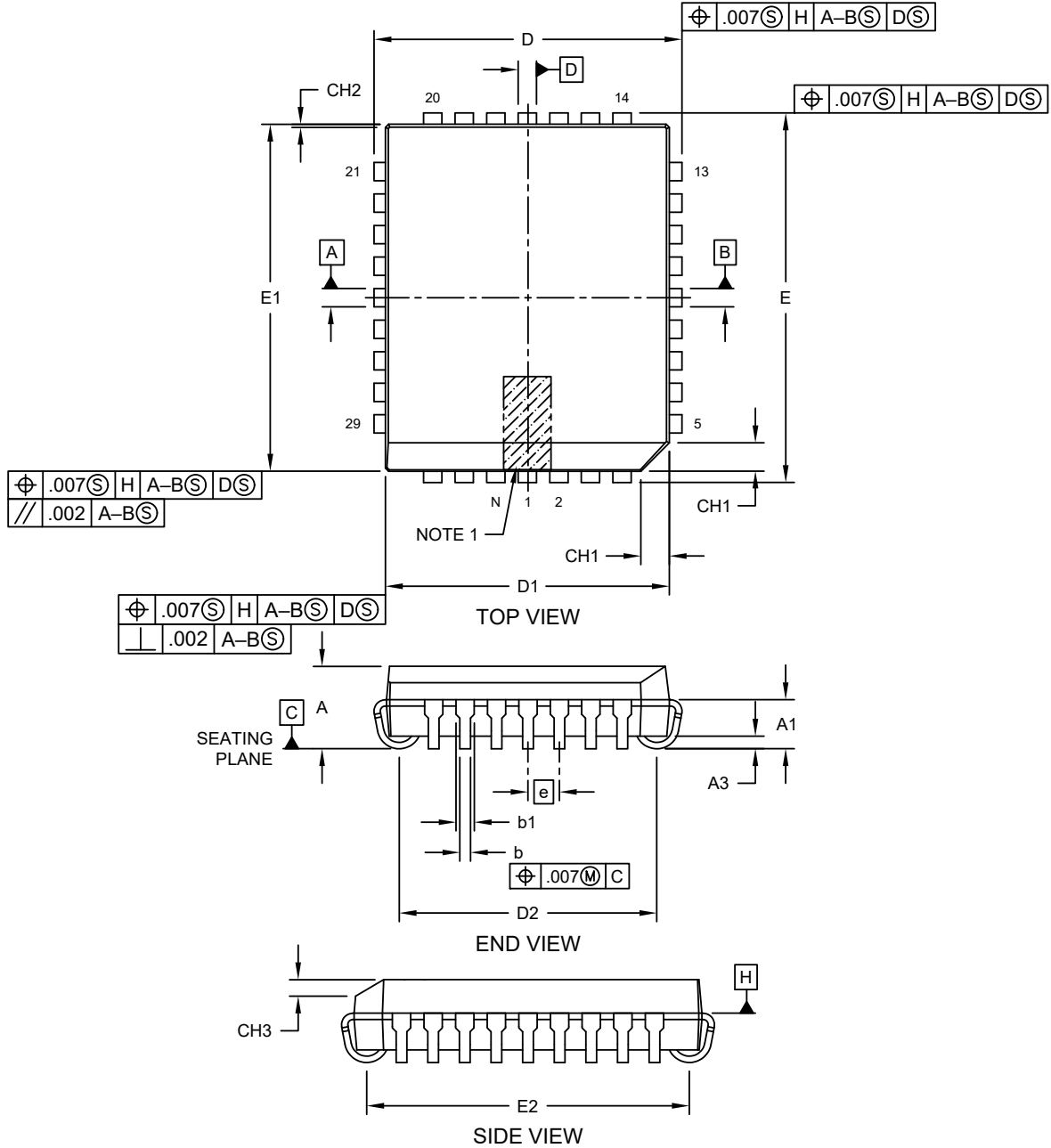
28-Lead PDIP		32-Lead PLCC	
<p>Topside</p> <div style="border: 1px solid black; padding: 5px; width: 80px; margin: 0 auto;"> <p style="text-align: center;">                     ATMEL                      AT27C512R                      %%U-34A04B                      YYWWNNN                 </p> </div>	<p>Backside</p> <div style="border: 1px solid black; width: 80px; height: 80px; margin: 0 auto;"></div>	<p>Topside</p> <div style="border: 1px solid black; padding: 5px; width: 80px; margin: 0 auto;"> <p style="text-align: center;">                     ●                      ATMEL                      AT27C512R                      %%U-34A04B                      YYWWNNN                 </p> </div>	<p>Backside</p> <div style="border: 1px solid black; width: 80px; height: 80px; margin: 0 auto;"></div>

Note: no backside markings

		%% = Access Time	
		45: 45 ns 70: 70 ns	
	<b>Lot Trace Code</b>		
	YWWNNN: Lot Trace Code Y: Year, WW: Work Week NNN = Assembly Trace Code		

**32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]**

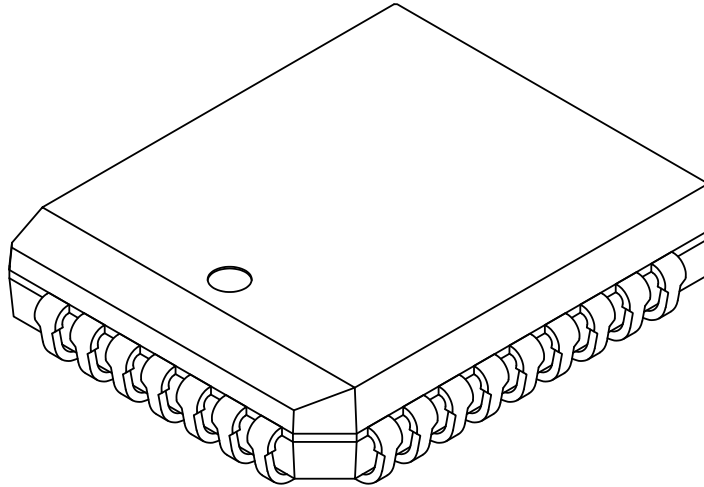
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-023 Rev C Sheet 1 of 2

### 32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	32		
Pitch	e	.050 BSC		
Pins along Length	ND	7		
Pins along Width	NE	9		
Overall Height	A	.125	.132	.140
Contact Height	A1	.060	.0775	.095
Standoff §	A3	.015	-	-
Corner Chamfer	CH1	.042	.045	.048
Chamfers	CH2	-	-	.020
Side Chamfer Height	CH3	.023	.026	.029
Overall Length	D	.485	.490	.495
Overall Width	E	.585	.590	.595
Molded Package Length	D1	.447	.450	.453
Molded Package Width	E1	.547	.550	.553
Footprint Length	D2	.376	.411	.446
Footprint Width	E2	.476	.511	.546
Lead Thickness	c	.008	.010	.013
Upper Lead Width	b1	.026	.029	.032
Lower Lead Width	b	.013	.017	.021

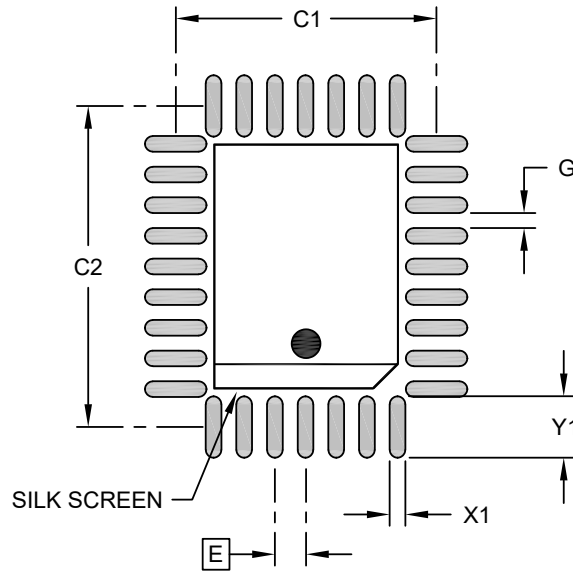
**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-023 Rev C Sheet 2 of 2

### 32-Lead Plastic Leaded Chip Carrier (L) - Rectangle [PLCC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



#### RECOMMENDED LAND PATTERN

		Units	INCHES		
		Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		.050 BSC		
Contact Pad Spacing	C1			.425	
Contact Pad Spacing	C2			.524	
Contact Pad Width (X32)	X1				.026
Contact Pad Length (X32)	Y1				.100
Contact Pad to Center Pad (X28)	G		.008		

**Notes:**

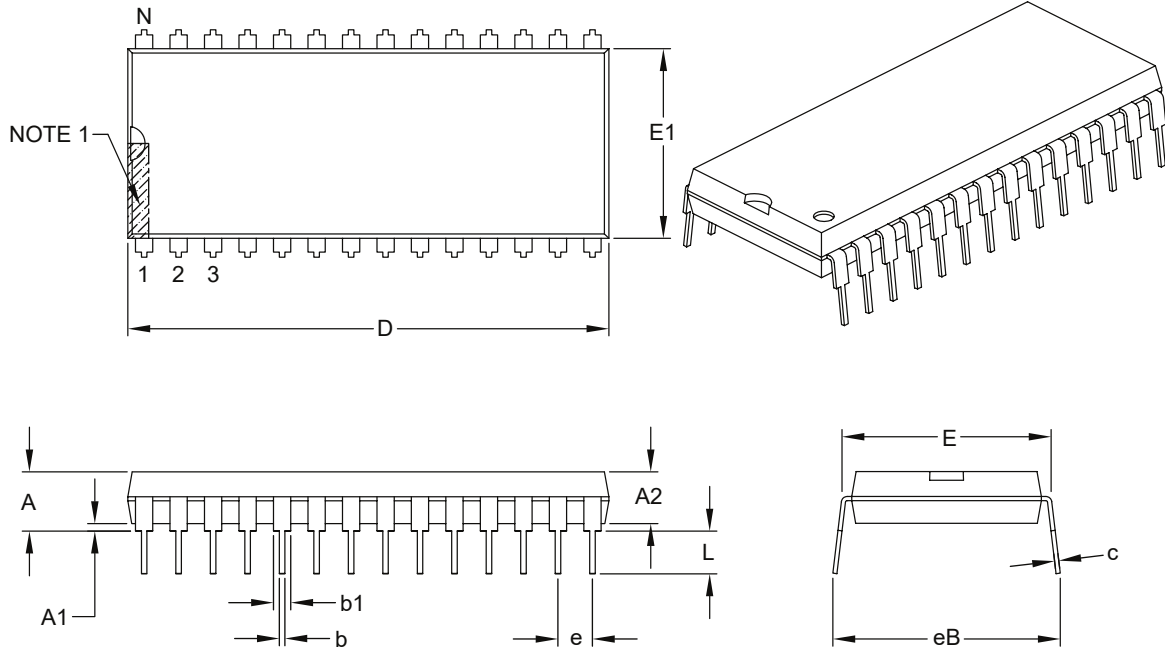
1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2023 Rev C



### 28-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.380	–	1.565
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.022
Overall Row Spacing §	eB	–	–	.700

**Notes:**

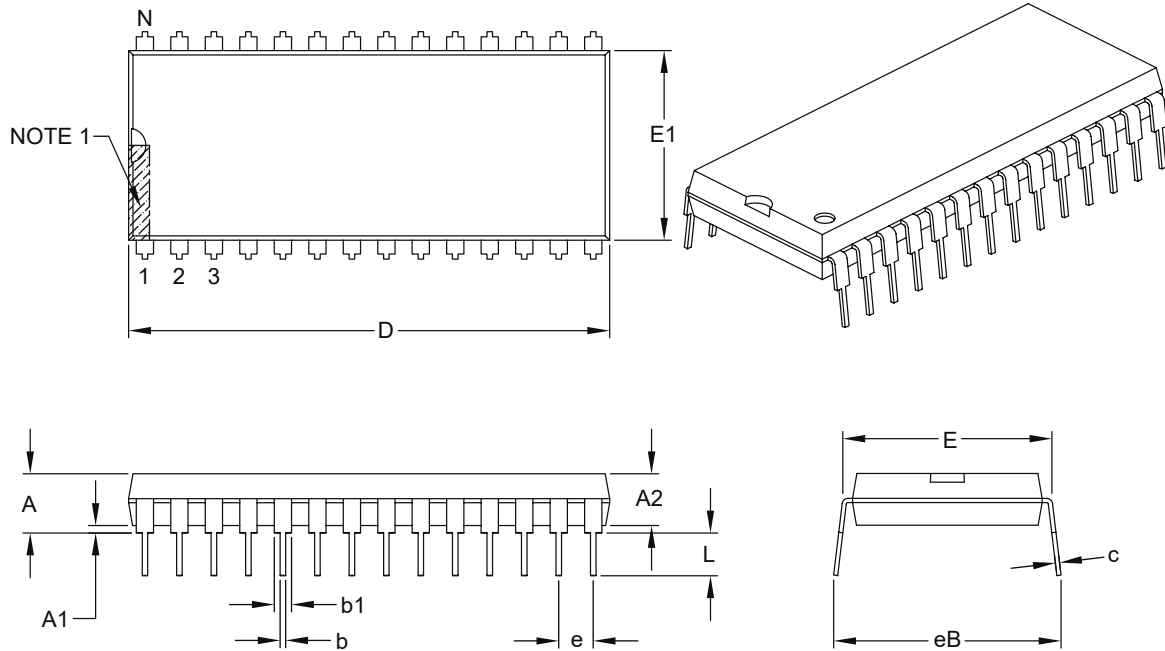
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-079B

### 28-Lead Plastic Dual In-Line (PI) – 600 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.380	–	1.565
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.022
Overall Row Spacing §	eB	–	–	.700

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-079B

## **7. Revision History**

### **Revision A (December 2022)**

Updated to the Microchip template. Microchip DS20006752A replaces Atmel document 0015. Updated Part Marking Information. Updated section content throughout for clarification.

### **Atmel Document 0015 Revision Q (October 2011)**

Correct pinout note.

### **Atmel Document 0015 Revision P (April 2011)**

Remove TSOP and SOIC packages; Add lead finish to ordering information.

### **Atmel Document 0015 Revision O (December 2007)**

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## Microchip Information

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### The Microchip Website

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Microchip provides online support via our website at [www.microchip.com/](http://www.microchip.com/). This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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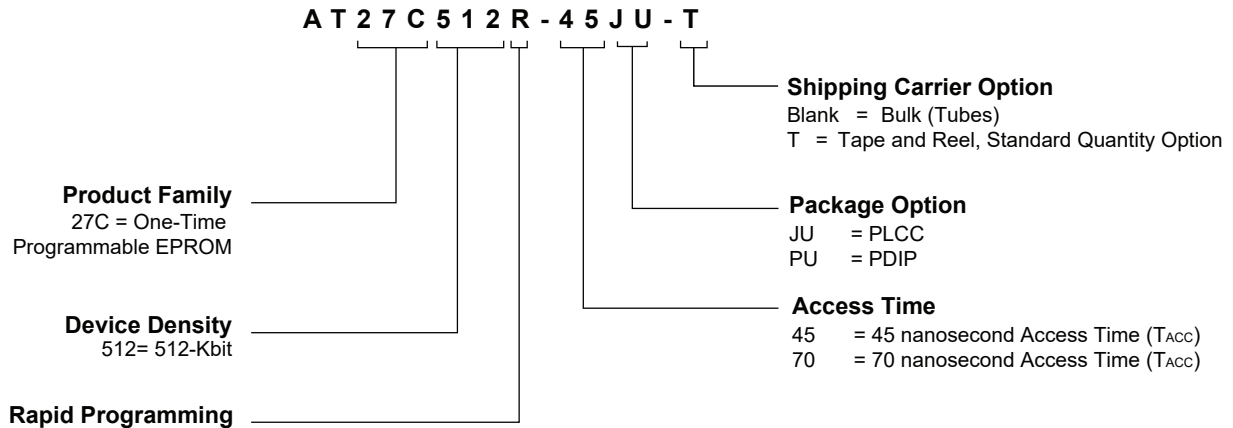
- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: [www.microchip.com/support](http://www.microchip.com/support)

## Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Examples

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Device Grade
AT27C512R-45JU	PLCC	L	JU	Bulk (Tubes)	Industrial Temperature (-40°C to +85°C)
AT27C512R-70JU	PLCC	L	JU	Bulk (Tubes)	
AT27C512R-45PU	PDIP	P	PU	Bulk (Tubes)	
AT27C512R-70PU	PDIP	P	PU	Bulk (Tubes)	
AT27C512R-45JU-T	PLCC	L	JU	Tape and Reel	
AT27C512R-70JU-T	PLCC	L	JU	Tape and Reel	

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ISBN: 978-1-6683-1778-5

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