AT25M01

SPI Serial EEPROM 1 Mbits (131,072 x 8)

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1):
  - Data sheet describes mode 0 operation
- Low-Voltage Operation:
  - 1.7V (V_{CC} = 1.7V to 5.5V)
- Industrial Temperature Range: -40°C to +85°C
- 20 MHz Clock Rate (5V)
- 256-Byte Page Mode
- Block Write Protection:
  - Protect 1/4, 1/2 or entire array
- Write-Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-Timed Write Cycle within 5 ms Maximum
- ESD Protection > 4,000V
- High Reliability:
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Green (Lead-free/Halide-free/RoHS Compliant) Package Options
- Die Sale Options: Wafer Form and Bumped Wafers

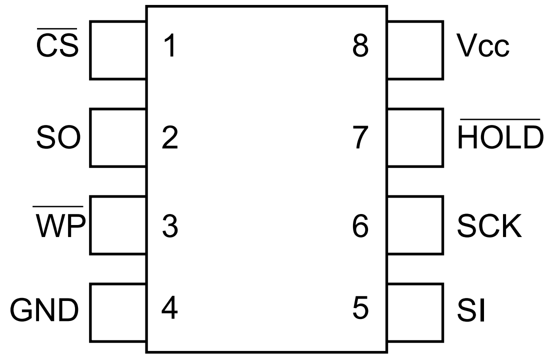
Packages

- 8-Lead SOIC, 8-Lead SOIJ and 8-Ball WLCSP

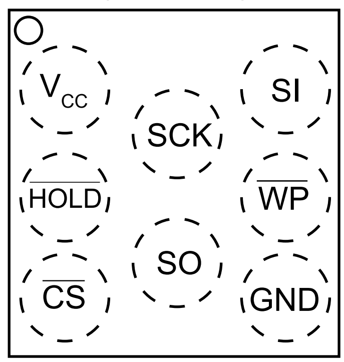
Table of Contents

1. Package Types (not to scale)

8-Lead SOIC/SOIJ
(Top View)



8-Ball WLCSP
(Top View)



2. Pin Description

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

Name	8-Lead SOIC	8-Lead SOIJ	8-Ball WLCSP	Function
$\overline{\text{CS}}$	1	1	A5	Chip Select
SO	2	2	B4	Serial Data Output
$\overline{\text{WP}}$(1)	3	3	C3	Write-Protect
GND	4	4	C5	Ground
SI	5	5	C1	Serial Data Input
SCK	6	6	B2	Serial Data Clock
$\overline{\text{HOLD}}$(1)	7	7	A3	Suspends Serial Input
V_{CC}	8	8	A1	Device Power Supply

Note:

1. The Write-Protect ($\overline{\text{WP}}$) and Hold ($\overline{\text{HOLD}}$) pins should be driven high or low as appropriate.

2.1 Chip Select ($\overline{\text{CS}}$)

The AT25M01 is selected when the Chip Select ($\overline{\text{CS}}$) pin is low. When the device is not selected, data will not be accepted via the Serial Data Input (SI) pin, and the Serial Output (SO) pin will remain in a high-impedance state.

To ensure robust operation, the $\overline{\text{CS}}$ pin should follow V_{CC} upon power-up. It is therefore recommended to connect $\overline{\text{CS}}$ to V_{CC} using a pull-up resistor (less than or equal to 10 kΩ). After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

2.2 Serial Data Output (SO)

The Serial Data Output (SO) pin is used to transfer data out of the AT25M01. During a read sequence, data is shifted out on this pin after the falling edge of the Serial Data Clock (SCK).

2.3 Write-Protect ($\overline{\text{WP}}$)

The Write-Protect ($\overline{\text{WP}}$) pin will allow normal read/write operations when held high. When the $\overline{\text{WP}}$ pin is brought low and the WPEN bit is set to a logic '1', all write operations to the STATUS register are inhibited. $\overline{\text{WP}}$ going low while $\overline{\text{CS}}$ is still low will interrupt a write operation to the STATUS register. If the internal write cycle has already been initiated, $\overline{\text{WP}}$ going low will have no effect on any write operation to the STATUS register. The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the STATUS register is set to a logic '0'. This will allow the user to install the AT25M01 in a system with the $\overline{\text{WP}}$ pin tied to ground and still be able to write to the STATUS register. All $\overline{\text{WP}}$ pin functions are enabled when the WPEN bit is set to a logic '1'.

2.4 Ground (GND)

The ground reference for the Device Power Supply (V_{CC}). The Ground (GND) pin should be connected to the system ground.

2.5 Serial Data Input (SI)

The Serial Data Input (SI) pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the Serial Data Clock (SCK).

2.6 Serial Data Clock (SCK)

The Serial Data Clock (SCK) pin is used to synchronize the communication between a master and the AT25M01. Instructions, addresses or data present on the Serial Data Input (SI) pin is latched in on the rising edge of SCK, while output on the Serial Data Output (SO) pin is clocked out on the falling edge of SCK.

2.7 Suspend Serial Input ($\overline{\text{HOLD}}$)

The Suspend Serial Input ($\overline{\text{HOLD}}$) pin is used in conjunction with the Chip Select ($\overline{\text{CS}}$) pin to pause the AT25M01. When the device is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{\text{HOLD}}$ pin must be brought low while the Serial Data Clock (SCK) pin is low. To resume serial communication, the $\overline{\text{HOLD}}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{\text{HOLD}}$). Inputs to the Serial Data Input (SI) pin will be ignored while the Serial Data Output (SO) pin will be in the high-impedance state.

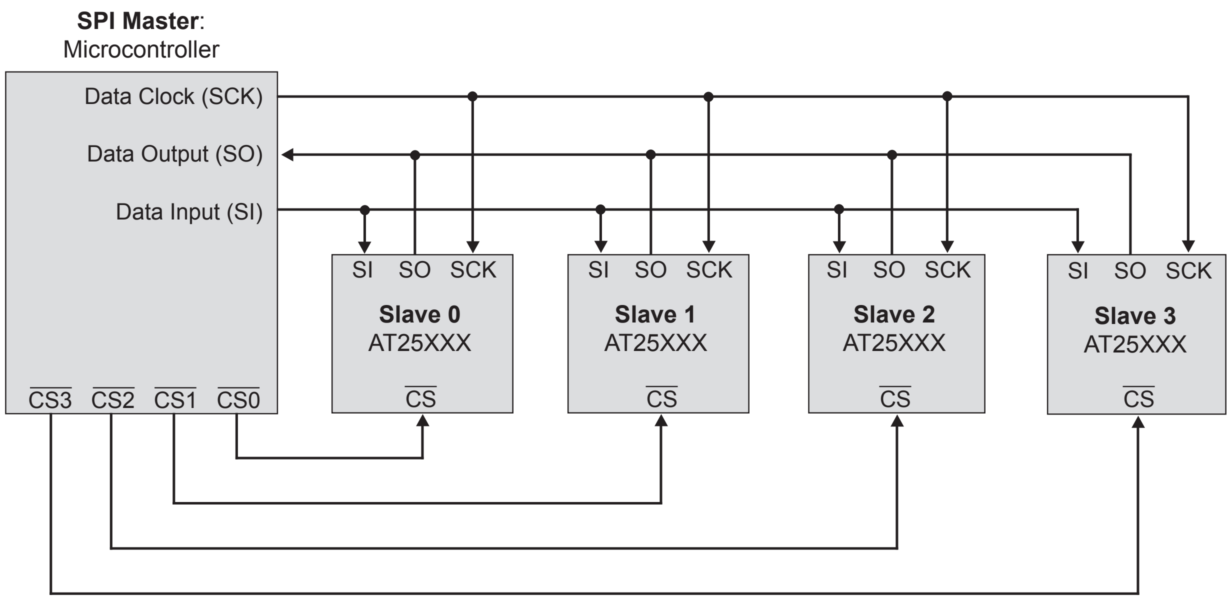
2.8 Device Power Supply (V_{CC})

The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

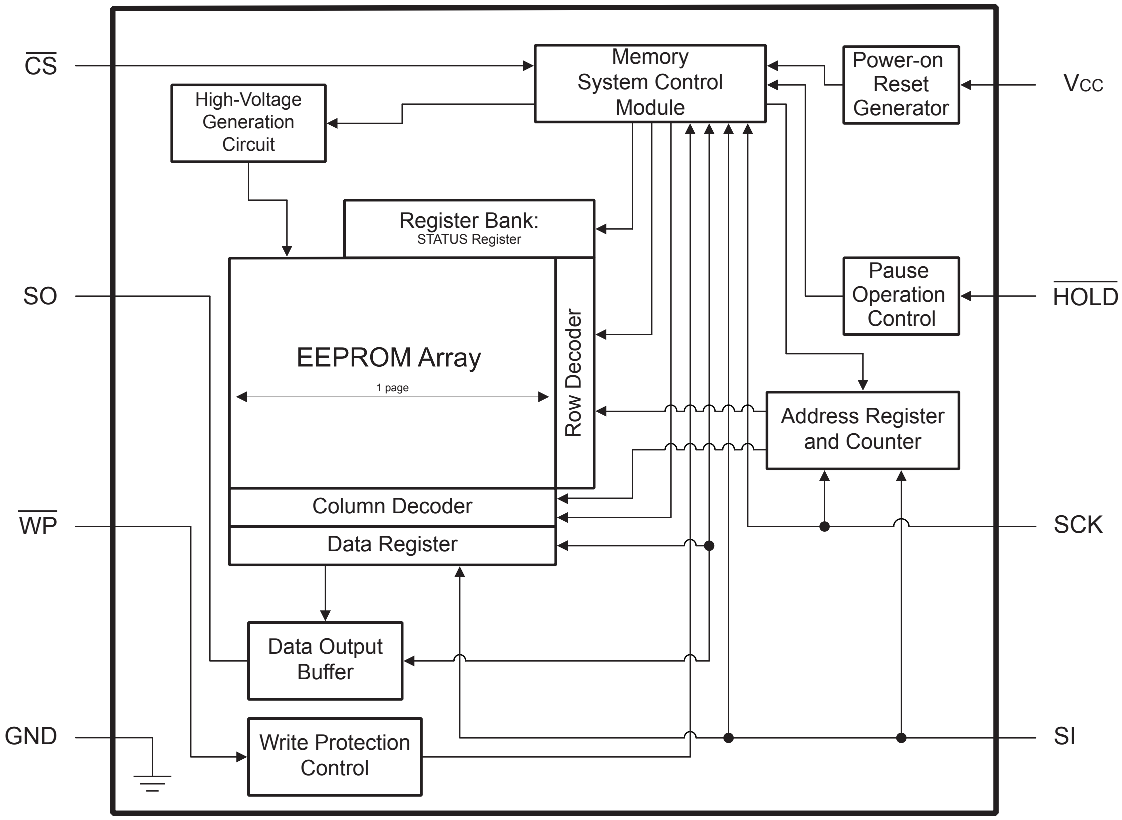
3. Description

The AT25M01 provides 1,048,576 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 131,072 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The device is available in space-saving 8-lead SOIC, 8-lead SOIJ and 8-ball WLCSP packages. All packages operate from 1.7V to 5.5V.

3.1 SPI Bus Master Connections to Serial EEPROMs



3.2 Block Diagram



4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Operating temperature	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
V_{CC}	6.25V
DC output current	5.0 mA
ESD protection	> 4 kV

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

AT25M01		
Operating Temperature (Case)	Industrial Temperature Range	-40°C to +85°C
V_{CC} Power Supply	Low-Voltage Grade	1.7V to 5.5V

4.3 DC Characteristics

Table 4-2. DC Characteristics[1]

Parameter	Symbol	Minimum	Typical	Maximum	Units	Conditions
Supply Voltage	V_{CC1}	1.7	—	5.5	V	
Supply Voltage	V_{CC2}	2.5	—	5.5	V	
Supply Voltage	V_{CC3}	4.5	—	5.5	V	
Supply Current	I_{CC1}	—	7.0	10.0	mA	V_{CC} = 5.0V at 20 MHz, SO = Open, Read
Supply Current	I_{CC2}	—	5.0	7.0	mA	V_{CC} = 5.0V at 10 MHz, SO = Open, Read, Write
Supply Current	I_{CC3}	—	2.2	3.5	mA	V_{CC} = 5.0V at 1 MHz, SO = Open, Read, Write
Standby Current	I_{SB1}	—	0.2	3.0	μA	V_{CC} = 1.7V, $\overline{CS}$ = V_{CC}

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Parameter	**Symbol**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**	
Standby Current	I_{SB2}	—	0.4	3.0	µA	V_{CC} = 2.5V, $\overline{CS}$ = V_{CC}	
Standby Current	I_{SB3}	—	2.0	5.0	µA	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}	
Input Leakage	I_{IL}	-3.0	—	3.0	µA	V_{IN} = 0V to V_{CC}	
Output Leakage	I_{OL}	-3.0	—	3.0	µA	V_{IN} = 0V to V_{CC}, T_A = 0°C to +70°C	
Input Low-Voltage	V_{IL}(2)	-1.0	—	V_{CC} x 0.3	V		
Input High-Voltage	V_{IH}(2)	V_{CC} x 0.7	—	V_{CC} + 0.5	V		
Output Low-Voltage	V_{OL1}	—	—	0.4	V	3.6V ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA
Output High-Voltage	V_{OH1}	V_{CC} - 0.8	—	—	V	3.6V ≤ V_{CC} ≤ 5.5V	I_{OH} = -1.6 mA
Output Low-Voltage	V_{OL2}	—	—	0.2	V	1.7V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA
Output High-Voltage	V_{OH2}	V_{CC} - 0.2	—	—	V	1.7V ≤ V_{CC} ≤ 3.6V	I_{OH} = -100 µA

Note:

1. Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = 1.7V to 5.5V (unless otherwise noted).
2. V_{IL} min and V_{IH} max are reference only and are not tested.

4.4 AC Characteristics

Table 4-3. AC Characteristics(1)

Parameter	Symbol	Minimum	Maximum	Units	Conditions
SCK Clock Frequency	f_{SCK}	0	20	MHz	V_{CC} = 4.5V to 5.5V
		0	10	MHz	V_{CC} = 2.5V to 5.5V
		0	5	MHz	V_{CC} = 1.7V to 5.5V
Input Rise Time	t_{RI}	—	15	ns	V_{CC} = 4.5V to 5.5V
		—	40	ns	V_{CC} = 2.5V to 5.5V
		—	80	ns	V_{CC} = 1.7V to 5.5V

...........continued

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Input Fall Time	t_{FI}	—	15	ns	V_{CC} = 4.5V to 5.5V
		—	40	ns	V_{CC} = 2.5V to 5.5V
		—	80	ns	V_{CC} = 1.7V to 5.5V
SCK High Time	t_{WH}	20	—	ns	V_{CC} = 4.5V to 5.5V
		40	—	ns	V_{CC} = 2.5V to 5.5V
		80	—	ns	V_{CC} = 1.7V to 5.5V
SCK Low Time	t_{WL}	20	—	ns	V_{CC} = 4.5V to 5.5V
		40	—	ns	V_{CC} = 2.5V to 5.5V
		80	—	ns	V_{CC} = 1.7V to 5.5V
$\overline{\text{CS}}$ High Time	t_{CS}	100	—	ns	V_{CC} = 4.5V to 5.5V
		100	—	ns	V_{CC} = 2.5V to 5.5V
		200	—	ns	V_{CC} = 1.7V to 5.5V
$\overline{\text{CS}}$ Setup Time	t_{CSS}	100	—	ns	V_{CC} = 4.5V to 5.5V
		100	—	ns	V_{CC} = 2.5V to 5.5V
		200	—	ns	V_{CC} = 1.7V to 5.5V
$\overline{\text{CS}}$ Hold Time	t_{CSH}	100	—	ns	V_{CC} = 4.5V to 5.5V
		100	—	ns	V_{CC} = 2.5V to 5.5V
		200	—	ns	V_{CC} = 1.7V to 5.5V
Data In Setup Time	t_{SU}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.7V to 5.5V
Data In Hold Time	t_{H}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.7V to 5.5V
$\overline{\text{HOLD}}$ Setup Time	t_{HD}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.7V to 5.5V
$\overline{\text{HOLD}}$ Hold Time	t_{CD}	5	—	ns	V_{CC} = 4.5V to 5.5V
		10	—	ns	V_{CC} = 2.5V to 5.5V
		20	—	ns	V_{CC} = 1.7V to 5.5V

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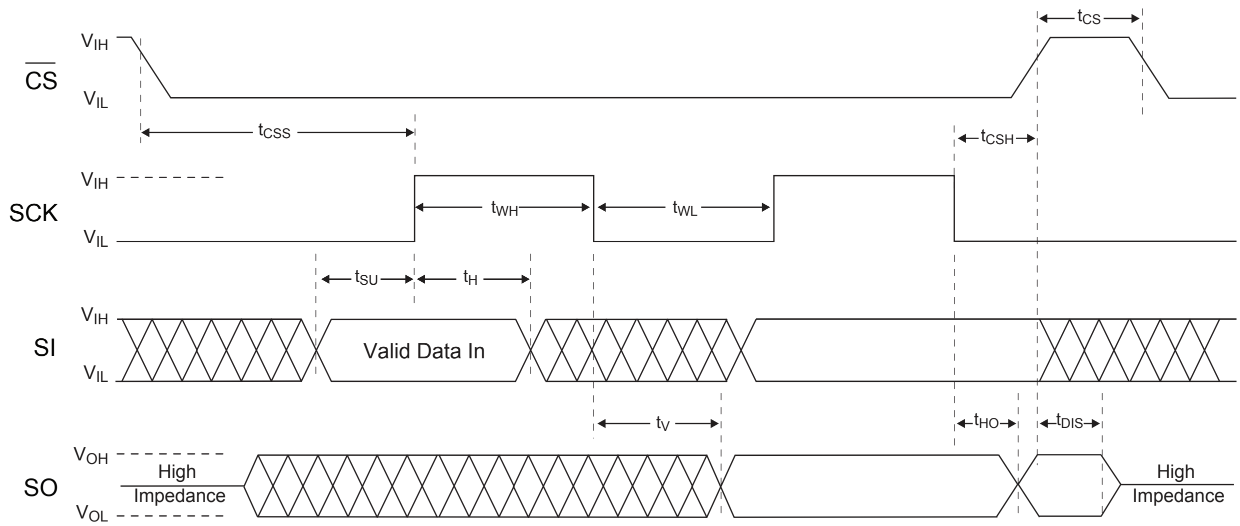
Parameter	Symbol	Minimum	Maximum	Units	Conditions
Output Valid	t_V	0	20	ns	V_{CC} = 4.5V to 5.5V
		0	40	ns	V_{CC} = 2.5V to 5.5V
		0	80	ns	V_{CC} = 1.7V to 5.5V
Output Hold Time	t_{HO}	0	—	ns	V_{CC} = 4.5V to 5.5V
		0	—	ns	V_{CC} = 2.5V to 5.5V
		0	—	ns	V_{CC} = 1.7V to 5.5V
$\overline{\text{HOLD}}$ to Output Low Z	t_{LZ}	0	25	ns	V_{CC} = 4.5V to 5.5V
		0	50	ns	V_{CC} = 2.5V to 5.5V
		0	100	ns	V_{CC} = 1.7V to 5.5V
$\overline{\text{HOLD}}$ to Output High Z	t_{HZ}	—	25	ns	V_{CC} = 4.5V to 5.5V
		—	50	ns	V_{CC} = 2.5V to 5.5V
		—	100	ns	V_{CC} = 1.7V to 5.5V
Output Disable Time	t_{DIS}	—	25	ns	V_{CC} = 4.5V to 5.5V
		—	50	ns	V_{CC} = 2.5V to 5.5V
		—	100	ns	V_{CC} = 1.7V to 5.5V
Write Cycle Time	t_{WC}	—	5	ms	V_{CC} = 4.5V to 5.5V
		—	5	ms	V_{CC} = 2.5V to 5.5V
		—	5	ms	V_{CC} = 1.7V to 5.5V

Note:

1. Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = As Specified, C_L = 1 TTL Gate and 30 pF (unless otherwise noted).

4.5 SPI Synchronous Data Timimg



4.6 Electrical Specifications

4.6.1 Power-Up Requirements and Reset Behavior

During a power-up sequence, the V_{CC} supplied to the AT25M01 should monotonically rise from GND to the minimum V_{CC} level, as specified in Table 4-1, with a slew rate no faster than 0.1 V/µs.

4.6.1.1 Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT25M01 includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any instructions until the V_{CC} level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the V_{CC} supply has reached a stable value greater than or equal to the minimum V_{CC} level. Additionally, once the V_{CC} is greater than or equal to the minimum V_{CC} level, the bus master must wait at least t_{PUP} before sending the first instruction to the device. See Table 4-4 for the values associated with these power-up parameters.

Table 4-4. Power-Up Conditions[(1)]

Symbol	Parameter	Min.	Max.	Units
t_{PUP}	Time required after V_{CC} is stable before the device can accept instructions	100	—	µs
V_{POR}	Power-on Reset Threshold Voltage	—	1.5	V
t_{POFF}	Minimum time at V_{CC} = 0V between power cycles	500	—	ms

Note:

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the V_{CC} level supplied to the AT25M01 drops below the maximum V_{POR} level specified, it is recommended that a full-power cycle sequence be performed by first driving the V_{CC} pin to GND in less than 1 ms, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

4.6.1.2 Pin Capacitance

Table 4-5. Pin Capacitance[1,2]

Symbol	Test Condition	Max.	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note:
1. This parameter is characterized but is not 100% tested in production.
2. Applicable over recommended operating range from: T_A = 25°C, f_{SCK} = 1.0 MHz, V_{CC} = 5.0V (unless otherwise noted).

4.6.1.3 EEPROM Cell Performance Characteristics

Table 4-6. EEPROM Cell Performance Characteristics

Operation	Test Condition	Min.	Max.	Units
Write Endurance[1]	T_A = 25°C, V_{CC} = 5.0V, Page Write mode	1,000,000	—	Write Cycles
Data Retention[1]	T_A = 55°C	100	—	Years

Note:
1. Performance is determined through characterization and the qualification process.

4.6.1.4 Software Reset

The SPI interface of the AT25M01 can be reset by toggling the $\overline{CS}$ input. If the $\overline{CS}$ line is already in the active state, it must complete a transition from the inactive state (≥V_{IH}) to the active state (≤V_{IL}) and then back to the inactive state (≥V_{IH}) without sending clocks on the SCK line. Upon completion of this sequence, the device will be ready to receive a new opcode on the SI line.

4.6.1.5 Device Default State at Power-Up

The AT25M01 default state upon power-up consists of:

- Standby Power mode
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state
- Write Enable Latch (WEL) bit in the STATUS register = `0`
- $\overline{\text{Ready}}$/Busy bit in the STATUS register = `0`, indicating the device is ready to accept a new command
- Device is not selected
- Not in Hold condition
- WPEN, BP1 and BP0 bits in the STATUS register are unchanged from their previous state due to the fact that they are nonvolatile values

4.6.1.6 Device Default Condition

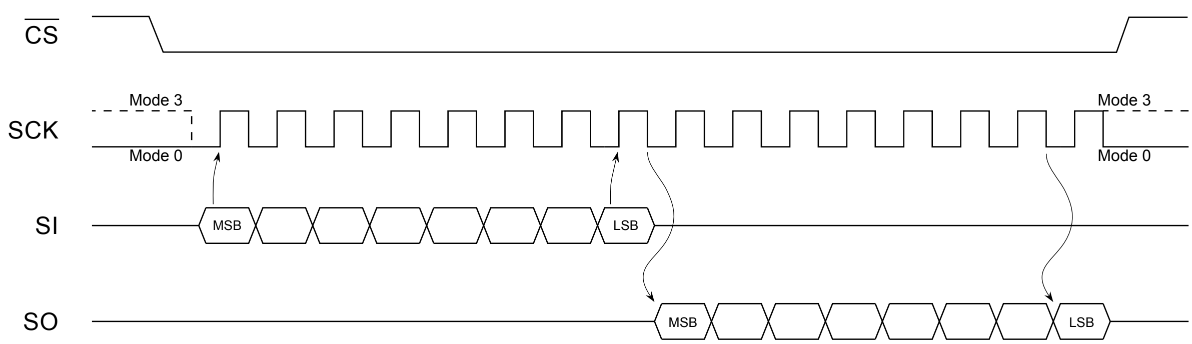
The AT25M01 is shipped from Microchip to the customer with the EEPROM array set to an all FFh data pattern (logic ‘`1`’ state). The Write-Protect Enable bit in the STATUS register is set to logic ‘`0`’ and the Block Write-Protection bits in the STATUS register are set to logic ‘`0`’.

5. Device Operation

The AT25M01 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI Master. The SPI Master communicates with the AT25M01 via the SPI bus which is comprised of four signal lines: Chip Select ($\overline{CS}$), Serial Data Clock (SCK), Serial Data Input (SI) and Serial Data Output (SO).

The SPI protocol defines a total of four modes of operation (Mode 0, 1, 2 or 3) with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus. The AT25M01 supports the two most common modes, SPI Modes 0 and 3. With SPI Modes 0 and 3, data is always latched in on the rising edge of SCK and always output on the falling edge of SCK. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the inactive state (when the SPI Master is in Standby mode and not transferring any data). SPI Mode 0 is defined as a low SCK while $\overline{CS}$ is not asserted (at V_{CC}) and SPI Mode 3 has SCK high in the inactive state. The SCK Idle state must match when the $\overline{CS}$ is deasserted both before and after the communication sequence in SPI Mode 0 and 3. The figures in this document depict Mode 0 with a solid line on SCK while $\overline{CS}$ is inactive and Mode 3 with a dotted line.

Figure 5-1. SPI Mode 0 and Mode 3



5.1 Interfacing the AT25M01 on the SPI Bus

Communication to and from the AT25M01 must be initiated by the SPI Master device, such as a microcontroller. The SPI Master device must generate the serial clock for the AT25M01 on the Serial Data Clock (SCK) pin. The AT25M01 always operates as a slave due to the fact that the SCK is always an input.

5.1.1 Selecting the Device

The AT25M01 is selected when the Chip Select ($\overline{CS}$) pin is low. When the device is not selected, data will not be accepted via the Serial Data Input (SI) pin, and the Serial Data Output (SO) pin will remain in a high-impedance state.

5.1.2 Sending Data to the Device

The AT25M01 uses the SI pin to receive information. All instructions, addresses and data input bytes are clocked into the device with the Most Significant bit (MSb) first. The SI pin samples on the first rising edge of the SCK line after the $\overline{CS}$ has been asserted.

5.1.3 Receiving Data from the Device

Data output from the device is transmitted on the SO pin, with the MSb output first. The SO data is latched on the first falling edge of SCK after the instruction has been clocked into the device, such as the Read from Memory Array (`READ`) and Read STATUS Register (`RDSR`) instructions. See 7. Read Sequence for more details.

5.2 Device Opcodes

5.2.1 Serial Opcode

After the device is selected by driving $\overline{\text{CS}}$ low, the first byte will be received on the SI pin. This byte contains the opcode that defines the operation to be performed. Refer to Table 6-1 for a list of all opcodes that the AT25M01 will respond to.

5.2.2 Invalid Opcode

If an invalid opcode is received, no data will be shifted into AT25M01 and the SO pin will remain in a high-impedance state until the falling edge of $\overline{\text{CS}}$ is detected again. This will reinitialize the serial communication.

5.3 Hold Function

The Suspend Serial Input ($\overline{\text{HOLD}}$) pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. The Hold mode, however, does not have an effect on the internal write cycle. Therefore, if a write cycle is in progress, asserting the $\overline{\text{HOLD}}$ pin will not pause the operation and the write cycle will continue to completion.

The Hold mode can only be entered while the $\overline{\text{CS}}$ pin is asserted. The Hold mode is activated by asserting the $\overline{\text{HOLD}}$ pin during the SCK low pulse. If the $\overline{\text{HOLD}}$ pin is asserted during the SCK high pulse, then the Hold mode will not be started until the beginning of the next SCK low pulse. The device will remain in the Hold mode as long as the $\overline{\text{HOLD}}$ pin and $\overline{\text{CS}}$ pin are asserted.

While in Hold mode, the SO pin will be in a high-impedance state. In addition, both the SI pin and the SCK pin will be ignored. The Write-Protect ($\overline{\text{WP}}$) pin, however, can still be asserted or deasserted while in the Hold mode.

To end the Hold mode and resume serial communication, the $\overline{\text{HOLD}}$ pin must be deasserted during the SCK low pulse. If the $\overline{\text{HOLD}}$ pin is deasserted during the SCK high pulse, then the Hold mode will not end until the beginning of the next SCK low pulse.

If the $\overline{\text{CS}}$ pin is deasserted while the $\overline{\text{HOLD}}$ pin is still asserted, then any operation that may have been started will be aborted and the device will reset the WEL bit in the STATUS register back to the logic ‘`0`’ state.

Figure 5-2. Hold Mode

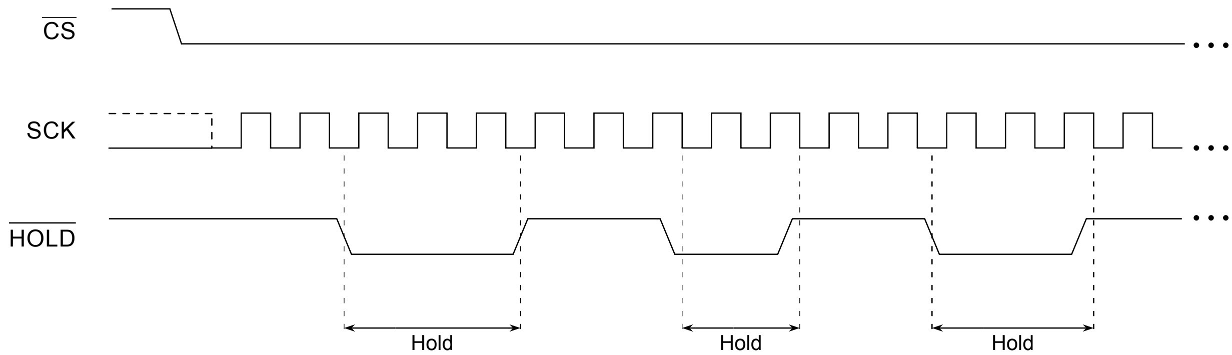
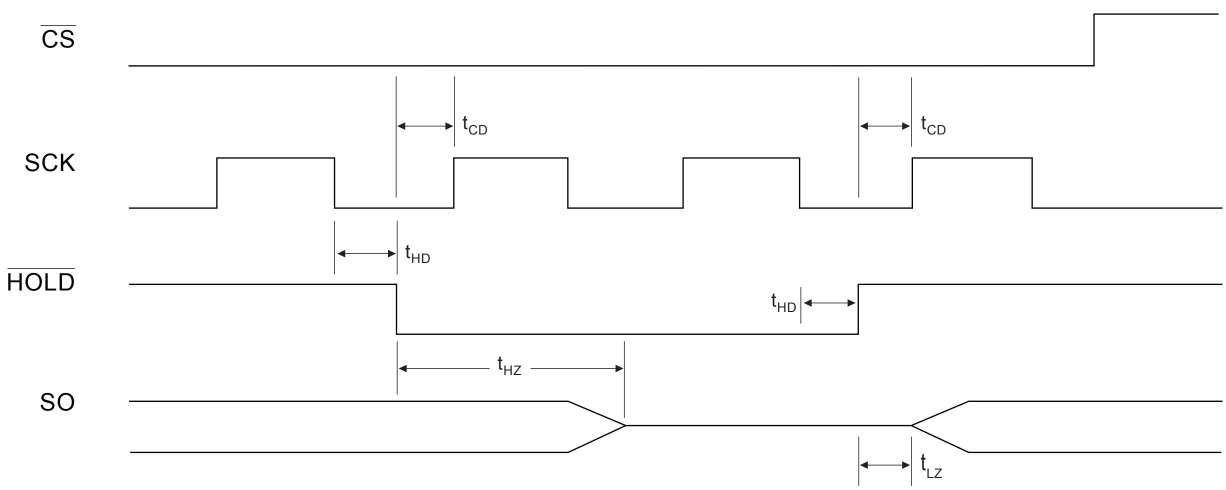


Figure 5-3. Hold Timing



5.4 Write Protection

The Write-Protect ($\overline{WP}$) pin will allow normal read and write operations when held high. When the $\overline{WP}$ pin is brought low and WPEN bit is a logic '1', all write operations to the STATUS register are inhibited. The $\overline{WP}$ pin going low while $\overline{CS}$ is still low will interrupt a Write STATUS Register (WRSR). If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the STATUS register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the STATUS register is a logic '0'. This will allow the user to install the AT25M01 device in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the STATUS register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to a logic '1'.

6. Device Commands and Addressing

The AT25M01 is designed to interface directly with the synchronous Serial Peripheral Interface (SPI). The AT25M01 utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 6-1. All instructions, addresses and data are transferred with the MSb first and start with a high-to-low $\overline{\text{CS}}$ transition.

Table 6-1. Instruction Set for the AT25M01

Instruction Name	Instruction Format	Operates On	Operation Description
`WREN`	`0000 X110`	STATUS Register	Set Write Enable Latch (WEL)
`WRDI`	`0000 X100`	STATUS Register	Reset Write Enable Latch (WEL)
`RDSR`	`0000 X101`	STATUS Register	Read STATUS Register
`WRSR`	`0000 X001`	STATUS Register	Write STATUS Register
`READ`	`0000 X011`	Memory Array	Read from Memory Array
`WRITE`	`0000 X010`	Memory Array	Write to Memory Array

6.1 STATUS Register Bit Definition and Function

The AT25M01 includes an 8-bit STATUS register. The STATUS register bits modulate various features of the device as shown in Table 6-2 and Table 6-3. These bits can be changed by specific instructions that are detailed in the following sections.

Table 6-2. STATUS Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEL	$\overline{\text{RDY}}$/BSY

Table 6-3. STATUS Register Bit Definition

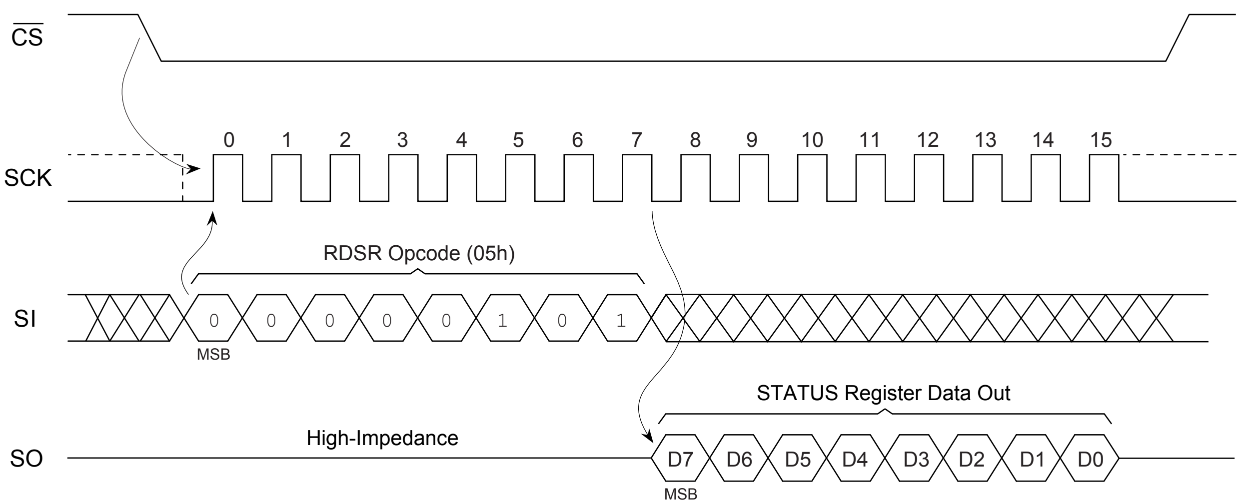
Bit	Name		Type	Description	
7	WPEN	Write-Protect Enable	R/W	`0`	See Table 6-5 (Factory Default)
				`1`	See Table 6-5 (Factory Default)
6:4	RFU	Reserved for Future Use	R	`0`	Reads as zeros when the device is not in a write cycle
				`1`	Reads as ones when the device is in a write cycle
3:2	BP1 BP0	Block Write Protection	R/W	`00`	No array write protection (Factory Default)
				`01`	Quarter array write protection (see Table 6-4)
				`10`	Half array write protection (see Table 6-4)
				`11`	Entire array write protection (see Table 6-4)
1	WEL	Write Enable Latch	R	`0`	Device is not write enabled (Power-up Default)
				`1`	Device is write enabled

..........continued					
Bit	**Name**		**Type**	**Description**	
0	RDY/BSY	Ready/Busy Status	R	0	Device is ready for a new sequence
				1	Device is busy with an internal operation

6.2 Read STATUS Register (RDSR)

The Read STATUS Register (RDSR) instruction provides access to the STATUS register. The ready/busy and write enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection (BP1, BP0) bits indicate the extent of memory array protection employed. The STATUS register is read by asserting the CS pin, followed by sending in a 05h opcode on the SI pin. Upon completion of the opcode, the device will return the 8-bit STATUS register value on the SO pin.

Figure 6-1. RDSR Waveform



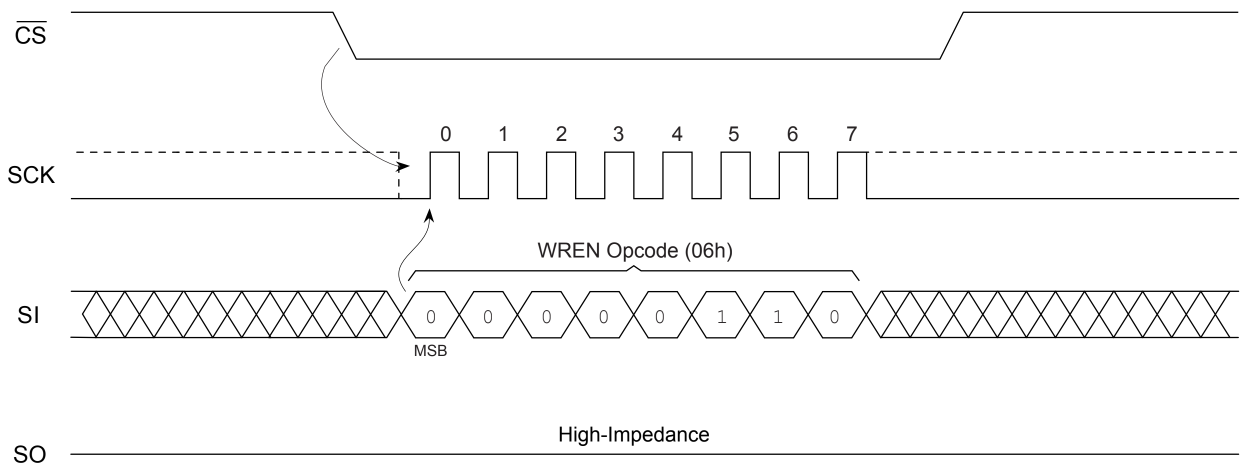
6.3 Write Enable (WREN) and Write Disable (WRDI)

Enabling and disabling writing to the STATUS register and EEPROM array is accomplished through the Write Enable (WREN) instruction and the Write Disable (WRDI) instruction. These functions change the status of the WEL bit in the STATUS register.

6.3.1 Write Enable Instruction (WREN)

The Write Enable Latch (WEL) bit of the STATUS register must be set to a logic '1' prior to each Write STATUS Register (WRSR) and Write to Memory Array (WRITE) instructions. This is accomplished by sending a WREN (06h) instruction to the AT25M01. First, the CS pin is driven low to select the device and then a WREN instruction is clocked in on the SI pin. Then the CS pin can be driven high and the WEL bit will be updated in the STATUS register to a logic '1'. The device will power-up in the Write Disable state (WEL = 0).

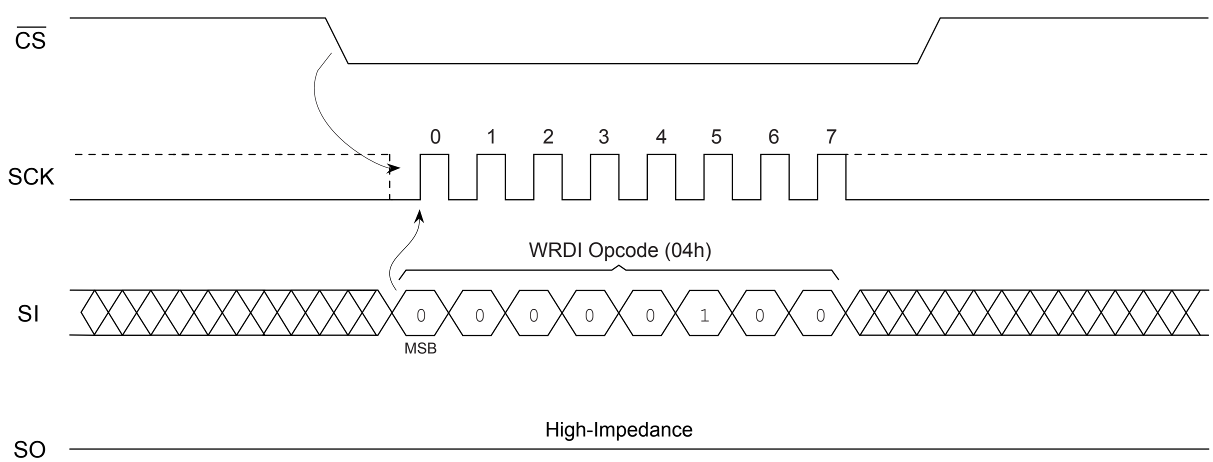
Figure 6-2. WREN Timing



6.3.2 Write Disable Instruction (`WRDI`)

To protect the device against inadvertent writes, the Write Disable (`WRDI`) instruction (opcode 04h) disables all programming modes by setting the WEL bit to a logic '`0`'. The `WRDI` instruction is independent of the status of the $\overline{\text{WP}}$ pin.

Figure 6-3. WRDI Timing



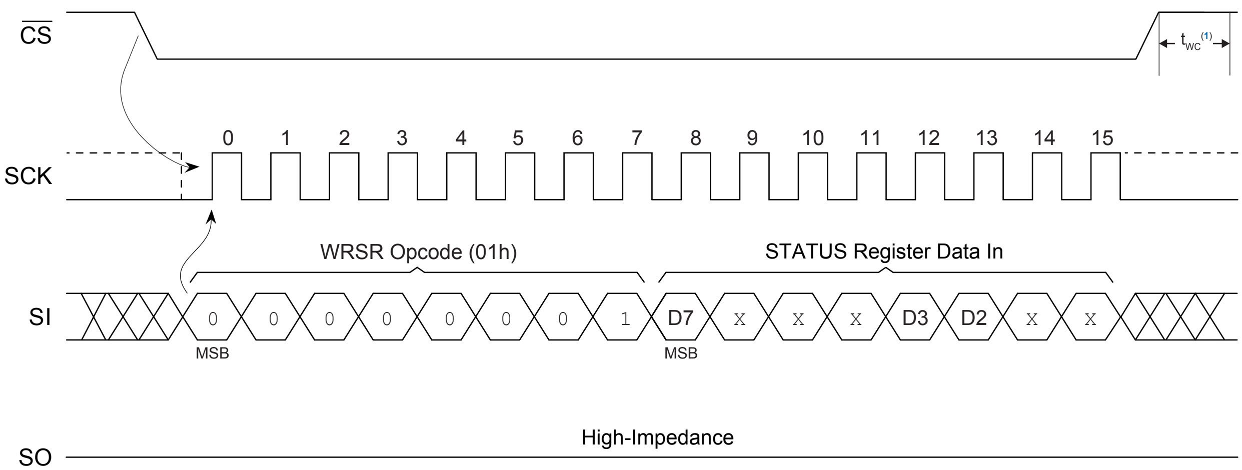
6.4 Write STATUS Register (`WRSR`)

The Write STATUS Register (`WRSR`) instruction enables the SPI Master to change selected bits of the STATUS register. Before a `WRSR` instruction can be initiated, a `WREN` instruction must be executed to set the WEL bit to logic '`1`'. Upon completion of a `WREN` instruction, a `WRSR` instruction can be executed.

Note: The `WRSR` instruction has no effect on bit 6, bit 5, bit 4, bit 1 and bit 0 of the STATUS register. Only bit 7, bit 3 and bit 2 can be changed via the `WRSR` instruction. These modifiable bits are the Write-Protect Enable (WPEN) and Block Protect (BP1, BP0) bits. These three bits are nonvolatile bits that have the same properties and functions as regular EEPROM cells. Their values are retained while power is removed from the device.

The AT25M01 will not respond to commands other than a `RDSR` after a `WRSR` instruction until the self-timed internal write cycle has completed. When the write cycle is completed, the WEL bit in the STATUS register is reset to logic '0'.

Figure 6-4. WRSR Waveform



Note:

1. This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of $\overline{CS}$ after a valid sequence.

6.4.1 Block Write-Protect Function

The `WRSR` instruction allows the user to select one of four possible combinations as to how the memory array will be inhibited from writing through changing the Block Write-Protect bits (BP1, BP0). The four levels of array protection are:

- None of the memory array is protected.
- Upper quarter (¼) address range is write-protected meaning the highest order address bits are read-only.
- Upper half (½) address range is write-protected meaning the highest order address bits are read-only.
- All of the memory array is write-protected meaning all address bits are read-only.

The Block Write Protection levels and corresponding STATUS register control bits are shown in Table 6-4.

Table 6-4. Block Write-Protect Bits

Level	STATUS Register Bits		Write-Protected/Read-Only Address Range
	BP1	BP0	AT25M01
0	0	0	None
1(1/4)	0	1	18000h – 1FFFFh
2(1/2)	1	0	10000h – 1FFFFh
3(All)	1	1	00000h – 1FFFFh

6.4.2 Write-Protect Enable Function

The WRSR instruction also allows the user to enable or disable the Write-Protect ($\overline{WP}$) pin through the use of the Write-Protect Enable (WPEN) bit. When the WPEN bit is set to logic '0', the ability to write the EEPROM array is dictated by the values of the Block Write-Protect (BP1, BP0) bits. The ability to write the STATUS register is controlled by the WEL bit. When the WPEN bit is set to logic '1', the STATUS register is read-only.

Hardware Write Protection is enabled when both the $\overline{WP}$ pin is low and the WPEN bit has been set to a logic '1'. When the device is Hardware Write-Protected, writes to the STATUS register, including the Block Write-Protect, WEL and WPEN bits and to the sections in the memory array selected by the Block Write-Protect bits are disabled. When Hardware Write Protection is enabled, writes are only allowed to sections of the memory that are not block-protected.

Hardware Write Protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is a logic '0'. When Hardware Write Protection is disabled, writes are only allowed to sections of the memory that are not block-protected. Refer to Table 6-5 for additional information.

Note: When the WPEN bit is Hardware Write-Protected, it cannot be set back to a logic '0' as long as the $\overline{WP}$ pin is held low.

Table 6-5. WPEN Operation

WPEN	$\overline{WP}$ Pin	WEL	Protected Blocks	Unprotected Blocks	STATUS Register
0	x	0	Protected	Protected	Protected
0	x	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
x	High	0	Protected	Protected	Protected
x	High	1	Protected	Writable	Writable

7. Read Sequence

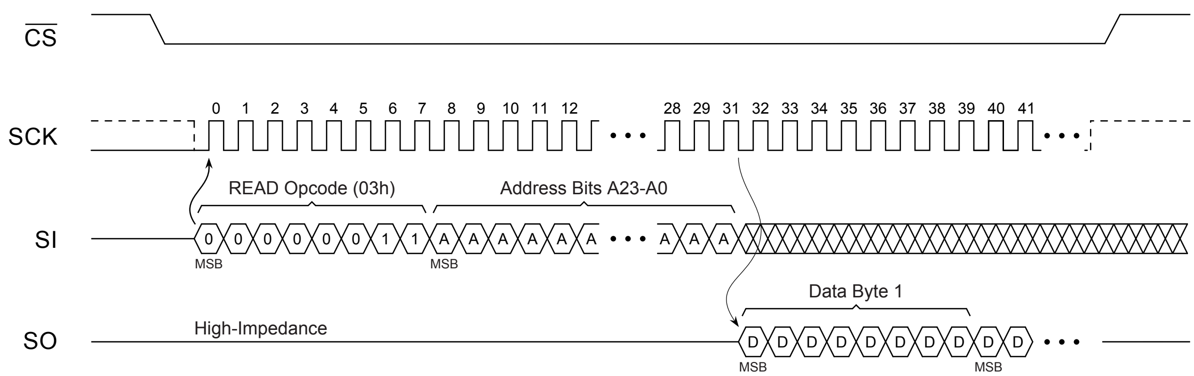
Reading the AT25M01 via the SO pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the `READ` (03h) instruction is transmitted via the SI line followed by the 24-bit address to be read. Refer to Table 7-1 for the address bits for AT25M01.

Table 7-1. AT25M01 Address Bits

Address	AT25M01
A_N	A_{16}—A_0
Don't Care Bits	A_{23}—A_{17}

Upon completion of the 24-bit address, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest-order address bit is reached, the address counter will rollover to the lowest-order address bit allowing the entire memory to be read in one continuous read cycle regardless of the starting address.

Figure 7-1. Read Waveform



8. Write Sequence

In order to program the AT25M01, two separate instructions must be executed. First, the device *must be write enabled* via the Write Enable (`WREN`) instruction. Then, one of the two possible write sequences described in this section may be executed.

Note: If the device is not Write Enabled (`WREN`), the device will ignore the `WRITE` instruction and will return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ assertion is required to re-initiate communication.

The address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the `RDSR` instruction. Refer to Table 8-1 for the address bits for AT25M01.

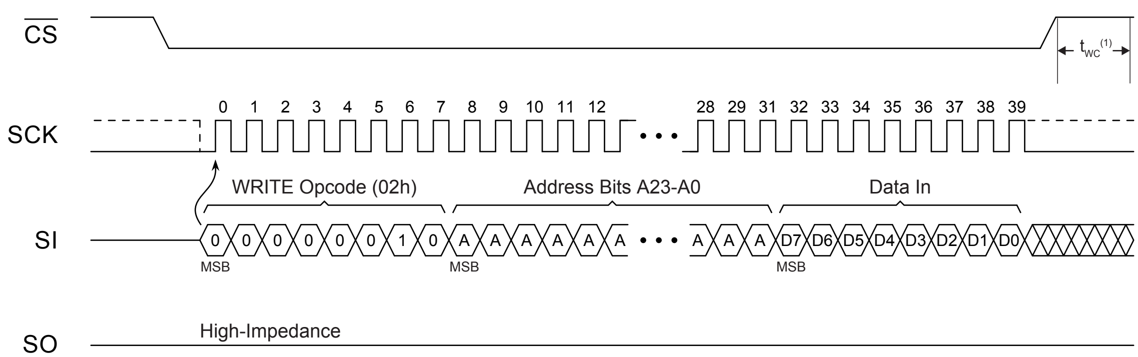
Table 8-1. AT25M01 Address Bits

Address	AT25M01
A_N	A_{16}—A_0
Don't Care Bits	A_{23}—A_{17}

8.1 Byte Write

A byte write requires the following sequence and is depicted in Figure 8-1. After the $\overline{CS}$ line is pulled low to select the device, the `WRITE` (02h) instruction is transmitted via the SI line followed by the 24-bit address and the data (D7-D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low time (Mode 0) and SCK high time (Mode 3) immediately after clocking in the D0 (LSB) data bit. The AT25M01 is automatically returned to the Write Disable state (STATUS register bit WEL = `0`) at the completion of a write cycle.

Figure 8-1. Byte Write

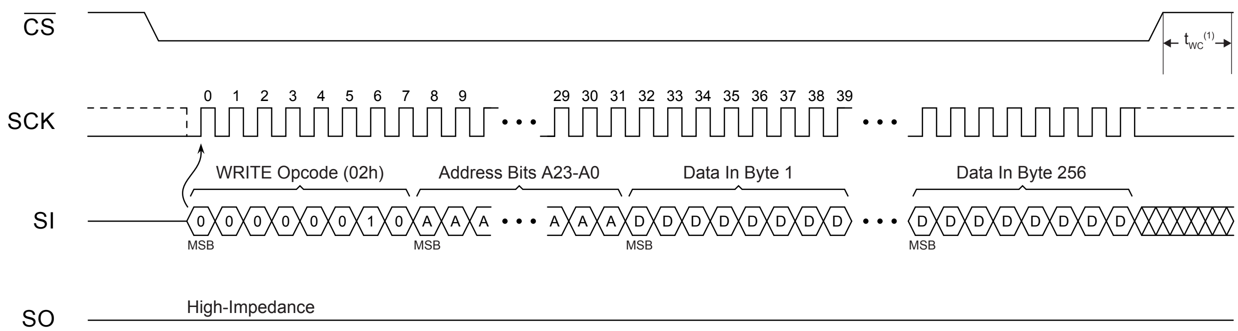


Note:
1. This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of $\overline{CS}$ after a valid sequence.

8.2 Page Write

A page write sequence allows up to 256 bytes to be written in the same write cycle, provided that all bytes are in the same row of the memory array. Partial page writes of less than 256 bytes are allowed. After each byte of data is received, the eight lowest order address bits are internally incremented following the receipt of each data byte. The higher order address bits are not incremented and retain the memory array page location. If more bytes of data are transmitted that what will fit to the end of that memory row, the address counter will rollover to the beginning of the same row. Nevertheless, creating a rollover event should be avoided as previously loaded data in the page could become unintentionally altered. The AT25M01 is automatically returned to the Write Disable state (WEL = `0`) at the completion of a write cycle.

Figure 8-2. Page Write



Note:

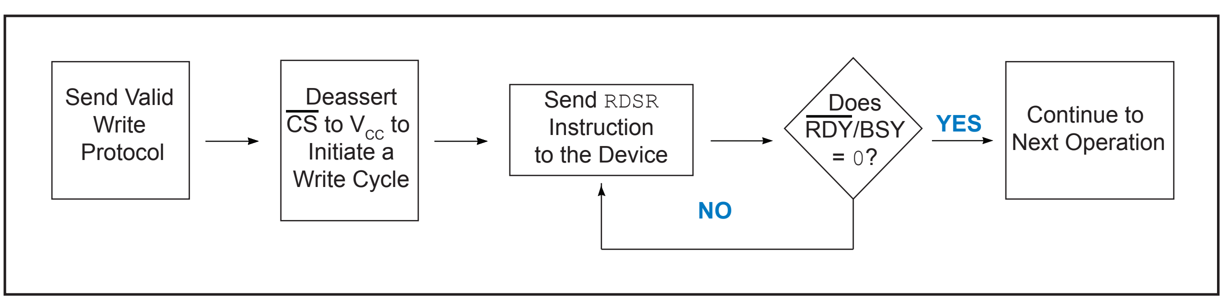
1. This instruction initiates a self-timed internal write cycle (t_{WC}) on the rising edge of $\overline{CS}$ after a valid sequence.

8.3 Polling Routine

A polling routine can be implemented to optimize time-sensitive applications that would not prefer to wait the fixed maximum write cycle time (t_{WC}). This method allows the application to know immediately when the write cycle has completed to start a subsequent operation.

Once the internally-timed write cycle has started, a polling routine can be initiated. This involves repeatedly sending Read STATUS Register (`RDSR`) instruction to determine if the device has completed its self-timed internal write cycle. If the $\overline{RDY}$/BSY bit (bit 0 of STATUS register) = `1`, the write cycle is still in progress. If bit 0 = `0`, the write cycle has ended. If the $\overline{RDY}$/BSY bit = `1`, repeated `RDSR` commands can be executed until the $\overline{RDY}$/BSY bit = `0`, signaling that the device is ready to execute a new instruction. Only the Read STATUS Register (`RDSR`) instruction is enabled during the write cycle.

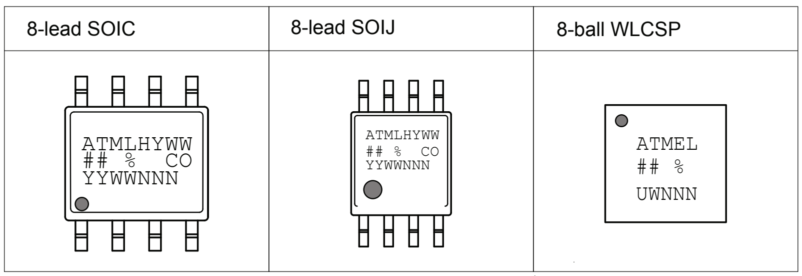
Figure 8-3. Polling Flowchart



9. Packaging Information

9.1 Package Marking Information

AT25M01: Package Marking Information



Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation	
AT25M01	Truncation Code ##: 5G

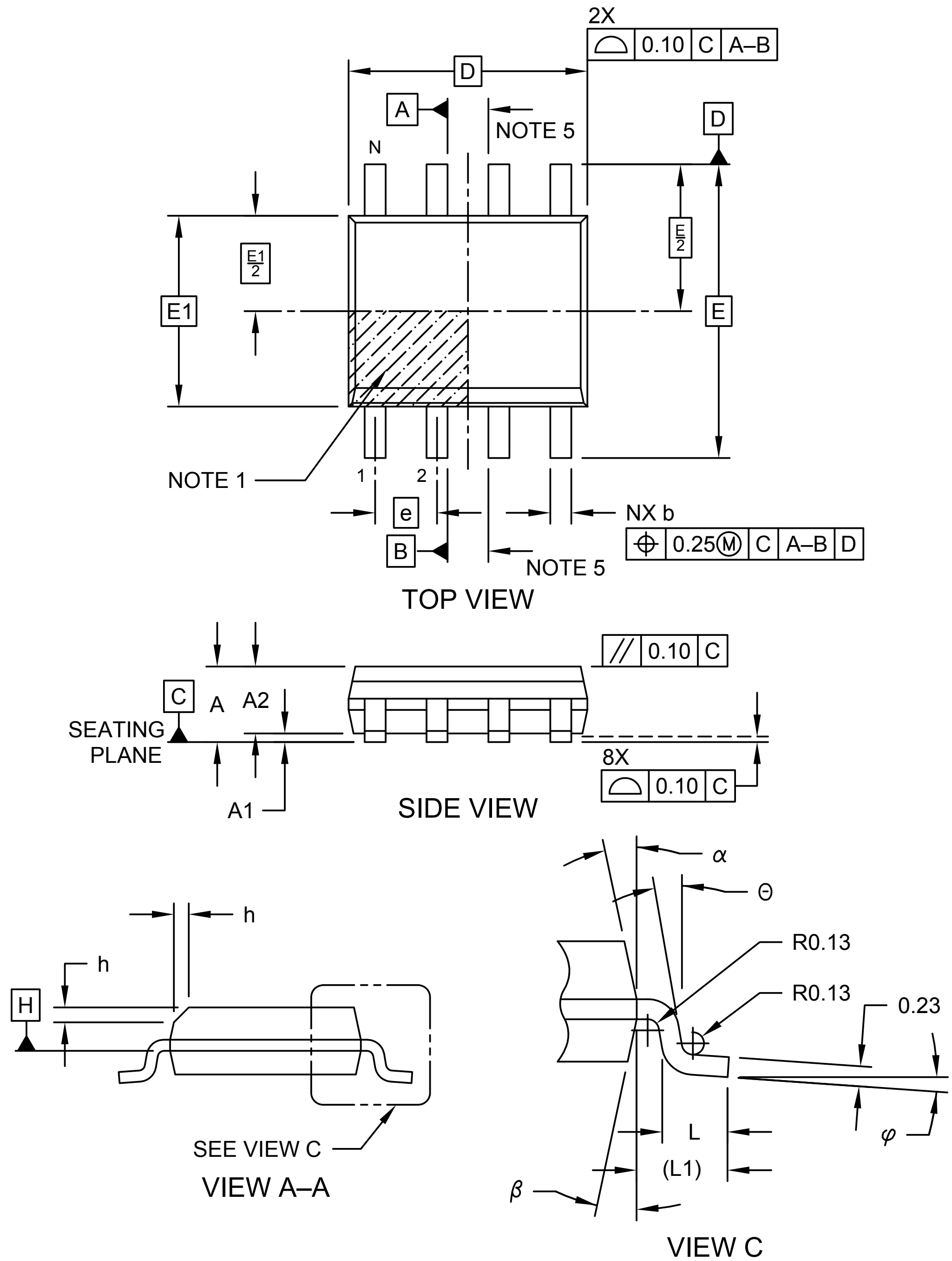
Date Codes					**Voltages**
YY = Year		Y = Year		WW = Work Week of Assembly	% = Minimum Voltage
16: 2016	20: 2020	6: 2016	0: 2020	02: Week 2	M: 1.7V min
17: 2017	21: 2021	7: 2017	1: 2021	04: Week 4	
18: 2018	22: 2022	8: 2018	2: 2022	...	
19: 2019	23: 2023	9: 2019	3: 2023	52: Week 52	

Country of Origin	**Device Grade**	**Atmel Truncation**
CO = Country of Origin	H or U: Industrial Grade	AT: Atmel ATM: Atmel ATML: Atmel

Lot Number or Trace Code
NNN = Alphanumeric Trace Code (2 Characters for Small Packages)

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

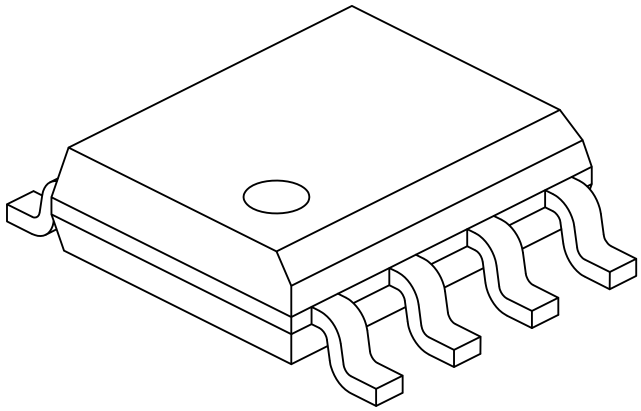
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

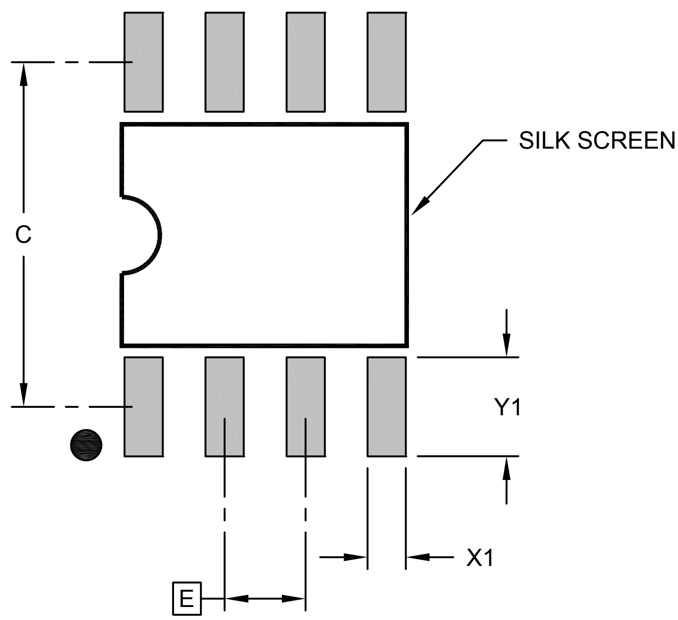
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

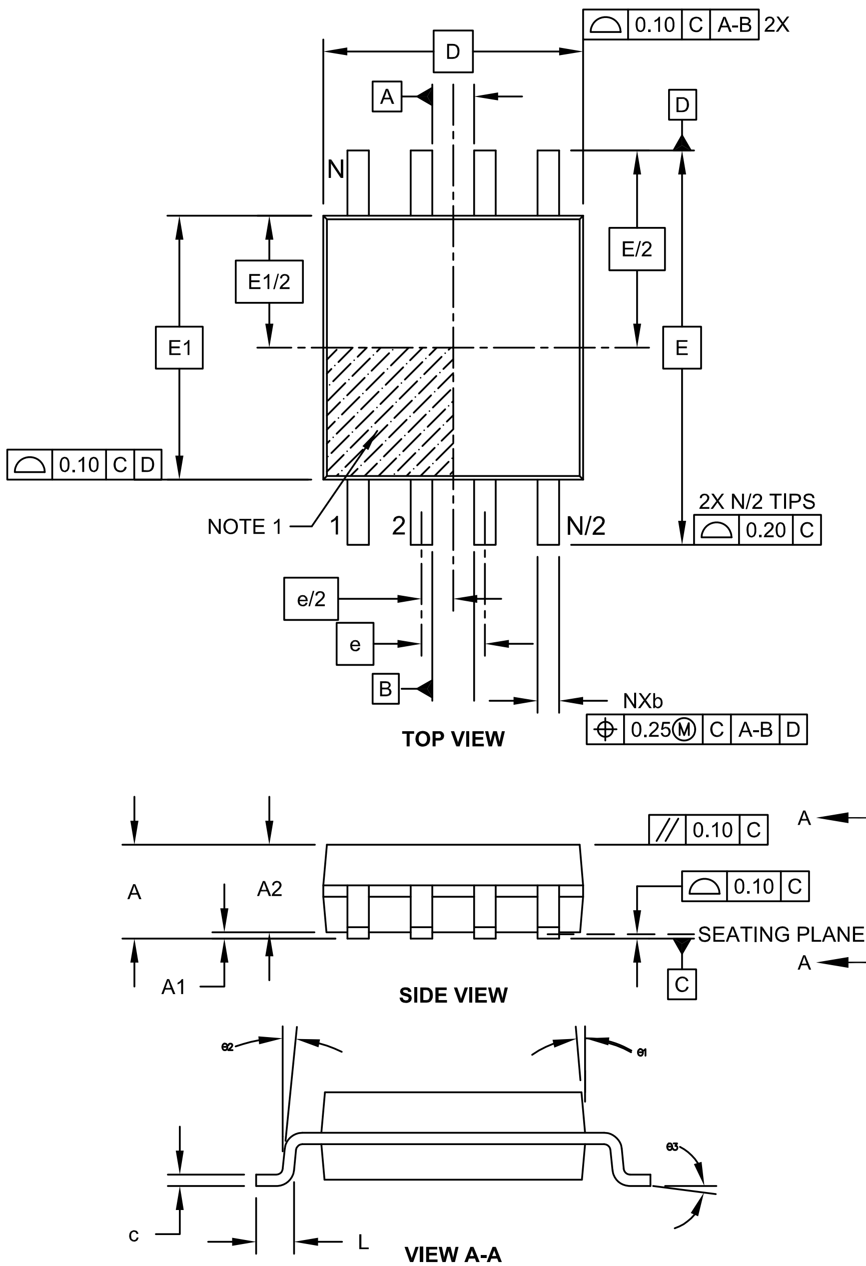
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

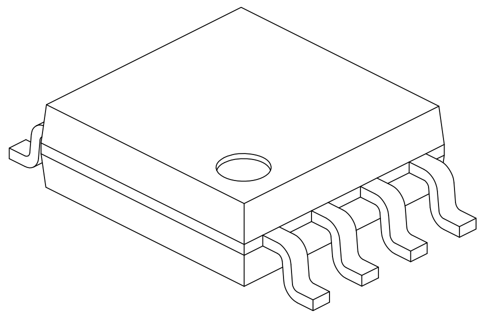
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-056C Sheet 1 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	1.77	-	2.03
Standoff §	A1	0.05		0.25
Molded Package Thickness	A2	1.75	-	1.98
Overall Width	E	7.94 BSC		
Molded Package Width	E1	5.25 BSC		
Overall Length	D	5.26 BSC		
Foot Length	L	0.51	-	0.76
Lead Thickness	c	0.15	-	0.25
Lead Width	b	0.36	-	0.51
Mold Draft Angle	Θ1	-	-	15°
Lead Angle	Θ2	0°	-	8°
Foot Angle	Θ3	0°	-	8°

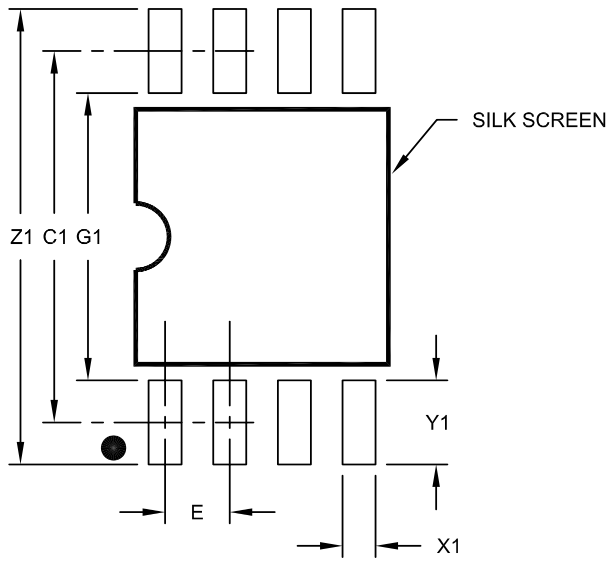
Notes:

1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

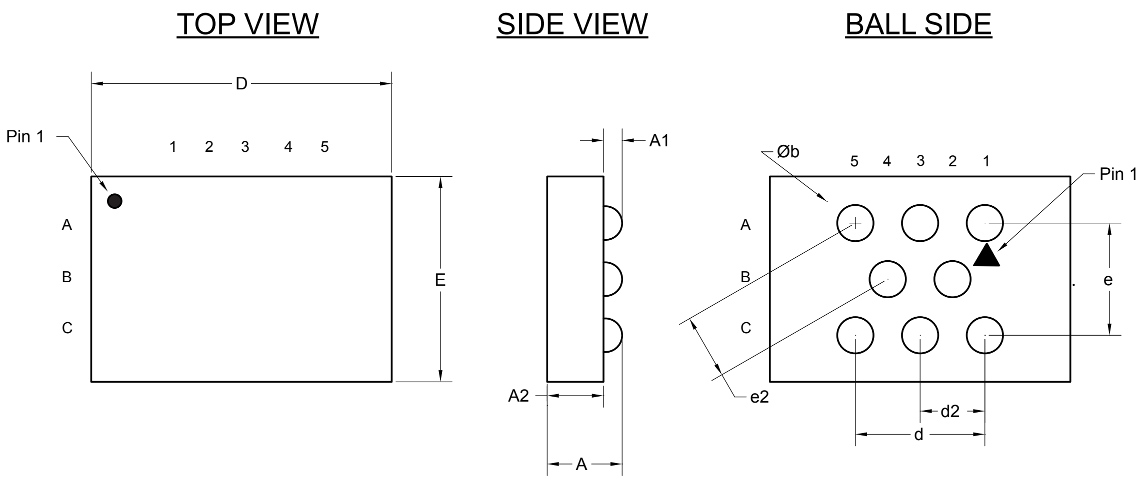
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Overall Width	Z1			9.00
Contact Pad Spacing	C1		7.30	
Contact Pad Width (X8)	X1			0.65
Contact Pad Length (X8)	Y1			1.70
Distance Between Pads	G1	5.60		
Distance Between Pads	G	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2056C



Note: Dimensions are not to scale

PIN ASSIGNMENT MATRIX

	1	2	3	4	5
A	V_{CC}	n/a	$\overline{\text{HOLD}}$	n/a	$\overline{\text{CS}}$
B	n/a	SCK	n/a	SO	n/a
C	SI	n/a	$\overline{\text{WP}}$	n/a	GND

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	TYP	MAX	NOTE
A	0.460	0.499	0.538	
A1	0.164	-	0.224	
A2	0.280	0.305	0.330	
E	Contact Microchip for details			
e		0.867		
e2		0.500		
d		1.000		
d2		0.500		
D	Contact Microchip for details			
b	0.239	0.269	0.299	

07/19/2015

	TITLE	GPC	DRAWING NO.	REV.
	8U-7, 8-ball (5x3 Array) Wafer Level Chip-Scale Package (WLCSP)	GXG	8U-7	D

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

10. Revision History

Revision A (July 2019)

Updated to Microchip template. Microchip DS20006226 replaces Atmel document 8823. Updated Part Marking Information. Added ESD rating. Removed lead finish designation. Added POR recommendations section. Updated trace code format in package markings. Updated section content throughout for clarification. Changed EIAJ SOIC package name to SOIJ. Updated the SOIC and SOIJ package drawings to the Microchip equivalents.

Atmel Document 8823 Revision E (May 2016)

Correct ordering information WLCSP note.

Atmel Document 8823 Revision D (July 2015)

Update the t_{RI} and t_{FI} maximum values, part markings page, and the 8S1 and 8U-7 package drawings.

Atmel Document 8823 Revision C (January 2015)

Correct the Write Timing figure. Update the 8S2 and 8U-7 package drawings, the ordering information section, and the disclaimer page.

Atmel Document 8823 Revision B (March 2013)

Add part marking. Update data sheet status from advance to complete. Update footers and Atmel fax number.

Atmel Document 8823 Revision A (January 2012)

Initial document release.

The Microchip Website

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
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Technical support is available through the web site at: http://www.microchip.com/support

Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

A T 2 5 M 0 1 - S S H M - B

Product Family
25 = Standard SPI Serial EEPROM

Device Density
M01 = 1 Megabit

Shipping Carrier Option
B = Bulk (Tubes)
T = Tape and Reel

Operating Voltage
M = 1.7V to 5.5V

Package Device Grade or Wafer/Die Thickness
H or U = Industrial Temperature Range (-40ºC to 85ºC)
11 = 11mil Wafer Thickness

Package Option
SS = SOIC
S = SOIJ
U = WLCSP
WWU = Wafer Unsawn

Examples:

Device	Package	Package Drawing Code	Package Option	Shipping Carrier Option	Device Grade
AT25M01-SSHM-B	SOIC	SN	SS	Bulk (Tubes)	Industrial Temperature (-40°C to 85°C)
AT25M01-SSHM-T	SOIC	SN	SS	Tape and Reel	
AT25M01-SHM-B	SOIJ	SM	S	Bulk (Tubes)	
AT25M01-SHM-T	SOIJ	SM	S	Tape and Reel	
AT25M01-UUM-T	WLCSP	8U-7	U	Tape and Reel	

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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ISBN: 978-1-5224-4753-5

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