ATWINC15x0

ATWINC15x0-MR210xB IEEE® 802.11 b/g/n SmartConnect IoT Module

Introduction

The ATWINC15x0-MR210xB is a low power consumption 802.11 b/g/n IoT (Internet of Things) module,specifically optimized for low power IoT applications. The module integrates Power Amplifier (PA), Low-Noise Amplifier (LNA), Switch, Power Management, and a printed antenna or a micro co-ax (u.FL) connector for an external antenna resulting in a small form factor (21.7 x 14.7 x 2.1 mm) design. It is interoperable with various vendors' 802.11 b/g/n access points. This module provides SPI ports to interface with a host controller.

The references to the ATWINC15x0-MR210xB module include the module devices listed in the following:

- ATWINC1500-MR210PB
- ATWINC1500-MR210UB
- ATWINC1510-MR210PB
- ATWINC1510-MR210UB

Features

- IEEE® 802.11 b/g/n 20 MHz (1x1) solution
- Single spatial stream in 2.4 GHz ISM band
- Integrated Transmit/Receive switch
- Integrated PCB antenna or u.FL micro co-ax connector for external antenna
- Superior sensitivity and range via advanced PHY signal processing
- Advanced equalization and channel estimation
- Advanced carrier and timing synchronization
- Wi-Fi® Direct (supported till firmware release 19.5.2)
- Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 security
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgment
- On-chip memory management engine to reduce host load
- SPI host interface
- Operating temperature range from -40°C to +85°C. RF performance at room temperature of 25ºC with a 2-3 db change at boundary conditions
- I/O operating voltage of 2.7V to 3.6V
- Built-in 26 MHz crystal
- Integrated Flash memory for system software

- Power Save modes
  - 4 µA Power-Down mode typical at 3.3V I/O
  - 380 µA Doze mode with chip settings preserved (used for beacon monitoring)[1]
  - On-chip low power sleep oscillator
  - Fast host wake-up from Doze mode by a pin or SPI transaction
- Fast Boot options
  - On-chip boot ROM (Firmware instant boot)
  - SPI flash boot
  - Low-leakage on-chip memory for state variables
  - Fast AP re-association (150 ms)
- On-chip Network stack to offload MCU
  - Integrated Network IP stack to minimize host CPU requirements
  - Network features TCP, UDP, DHCP, ARP, HTTP, TLS, and DNS
  - Hardware accelerators for Wi-Fi and TLS security to improve connection time
- Hardware accelerator for IP checksum
- Hardware accelerators for OTA security
- Small footprint host driver
- Wi-Fi Alliance® certifications for Connectivity and Optimizations
  - ID: WFA61069

Note: For information on module power modes, refer to Power Consumption.

Table of Contents

1. Ordering Information and Module Marking

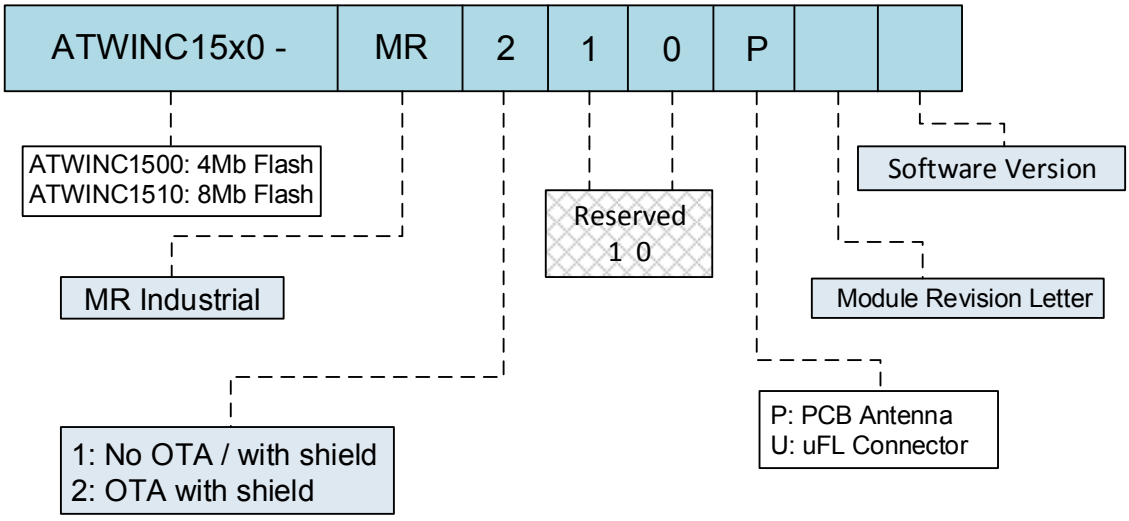
Following table describes the ordering details for the ATWINC15x0-MR210xB modules.

Table 1-1. Ordering Details

Model Number	Ordering Code	Package Dimension	No. of Pins	Description	Regulatory Certification
ATWINC1500-MR210PB	ATWINC1500-MR210PB1952	21.7 x 14.7 x 2.1 mm	28	Certified Module with ATWINC1500B chip (4Mb Flash) and PCB printed antenna	FCC, ISED, CE
ATWINC1500-MR210UB	ATWINC1500-MR210UB1952	21.7 x 14.7 x 2.1 mm	28	Certified Module with ATWINC1500B chip (4Mb Flash) and u.FL connector	FCC, ISED
ATWINC1510-MR210PB	ATWINC1510-MR210PB1952	21.7 x 14.7 x 2.1 mm	28	Certified Module with ATWINC1510B chip (8Mb Flash) and PCB printed antenna	FCC, ISED, CE
ATWINC1510-MR210UB	ATWINC1510-MR210UB1952	21.7 x 14.7 x 2.1 mm	28	Certified Module with ATWINC1510B chip (8Mb Flash) and u.FL connector	Planned

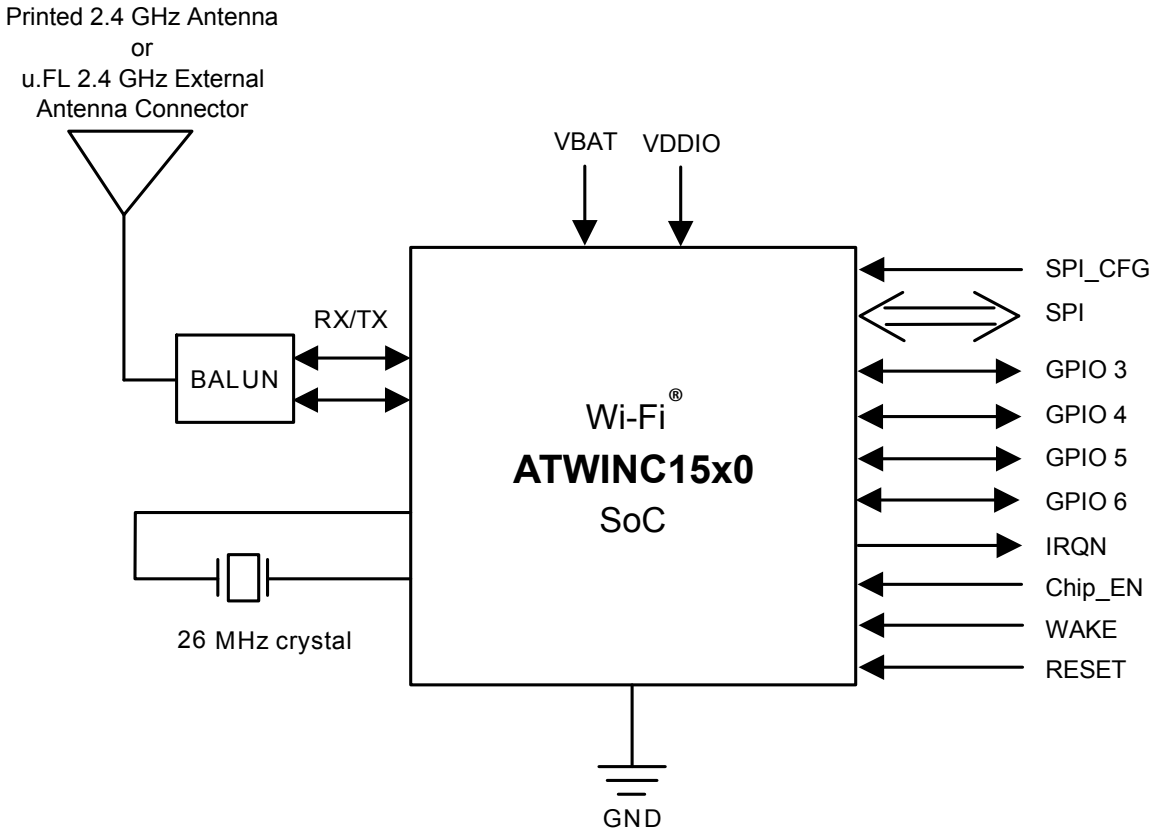
Following figure illustrates the ATWINC15x0-MR210xB modules' marking information.

Figure 1-1. Marking Information



2. Block Diagram

Figure 2-1. ATWINC15x0-MR210xB Module Block Diagram



3. Pin Description

Figure 3-1. Pin Diagram

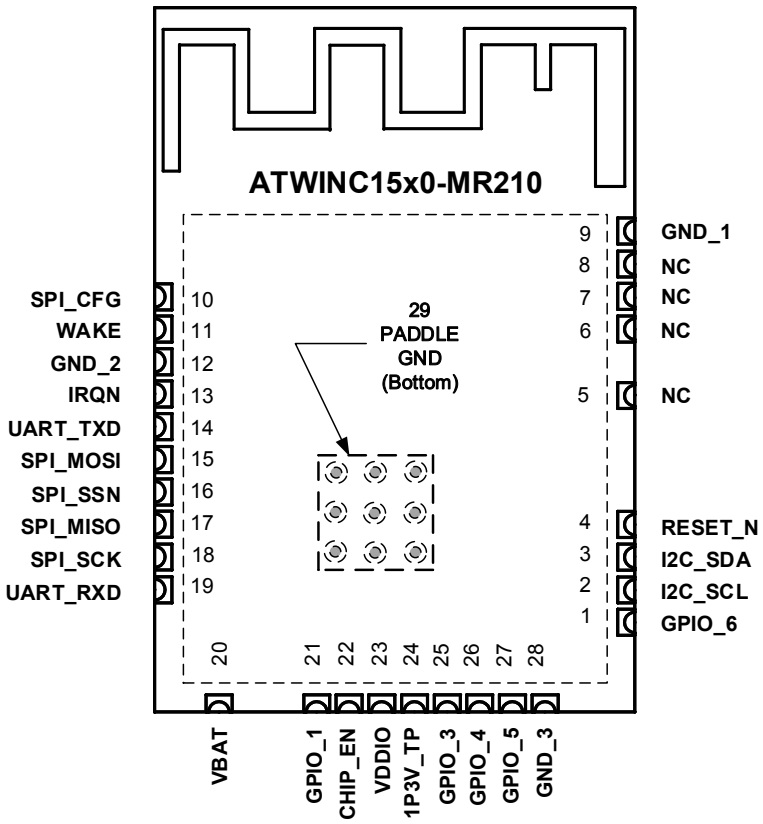


Table 3-1. ATWINC15x0-MR210xB Pin Description

Pin #	Name	Type	Description	Programmable Pull Up Resistor
1	GPIO_6	I/O	General purpose I/O.	Yes
2	I2C_SCL	I/O	I2C Slave Clock. Currently used only for development debug. Leave unconnected.	Yes
3	I2C_SDA	I/O	I2C Slave Data. Currently used only for development debug. Leave unconnected.	Yes
4	RESET_N	I	Active-Low Hard Reset. When this pin is asserted low, the module will be placed in the reset state. When this pin is asserted high, the module will be out of reset and will function normally. Connect to a host output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull down resistor to ensure a low level at power-up.	No
5	NC	-	No connect.	

Pin #	Name	Type	Description	Programmable Pull Up Resistor
6	NC	-	No connect.	
7	NC	-	No connect.	
8	NC	-	No connect.	
9	GND_1	-	GND.	
10	SPI_CFG	I	Tie to VDDIO through a 1MΩ resistor to enable the SPI interface.	No
11	WAKE	I	Host Wake control. Can be used to wake-up the module from Doze mode. Connect to a host GPIO.	Yes
12	GND_2	-	GND.	
13	IRQN	O	ATWINC15x0-MR210xB Device Interrupt output. Connect to host interrupt input pin.	Yes
14	UART_TXD	O	UART Transmit Output from ATWINC15x0-MR210xB Added debug.	Yes
15	SPI_RXD	I	SPI MOSI (Master Out, Slave In) pin.	Yes
16	SPI_SSN	I	SPI Slave Select. Active-low.	Yes
17	SPI_TXD	O	SPI MISO (Master In, Slave Out) pin.	Yes
18	SPI_SCK	I	SPI Clock.	Yes
19	UART_RXD	I	UART Receive input to ATWINC15x0-MR210xB. Added debug.	Yes
20	VBATT	-	Battery power supply.	
21	GPIO_1/RTC	I	General Purpose I/O / RTC.	Yes
22	CHIP_EN	I	Module enable. High level enables the module; low level places module in Power-Down mode. Connect to a host output that defaults low at power-up. If the host output is tri-stated, add a 1MΩ pull down resistor to ensure a low level at power-up.	No
23	VDDIO	-	I/O Power Supply. Must match host I/O voltage.	
24	1P3V_TP	-	1.3V VDD Core Test Point. Decouple with 10µF, and 0.01µF to GND.	
25	GPIO_3	I/O	General purpose I/O.	
26	GPIO_4	I/O	General purpose I/O.	Yes
27	GPIO_5	I/O	General purpose I/O.	Yes
28	GND_3	-	GND.	
29	PADDLE GND	-	GND.	

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Absolute maximum ratings for the ATWINC15x0-MR210xB modules are listed below.

Table 4-1. Conditions

Symbol	Description	Min.	Max.	Unit
VBATT	Input supply voltage	-0.3	5.0	V
VDDIO	I/O voltage	-0.3	4.2	V
Operating Temperature		-40	+85	ºC

⚠ CAUTION

Stresses listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Unit
VBATT	3.0	3.3	4.2	V
VDDIO	2.7	3.3	3.6	V

Note: 1. Test Conditions: -40ºC - +85ºC

5. CPU and Memory Subsystems

5.1 Processor

The ATWINC15x0-MR210xB modules have a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to the association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

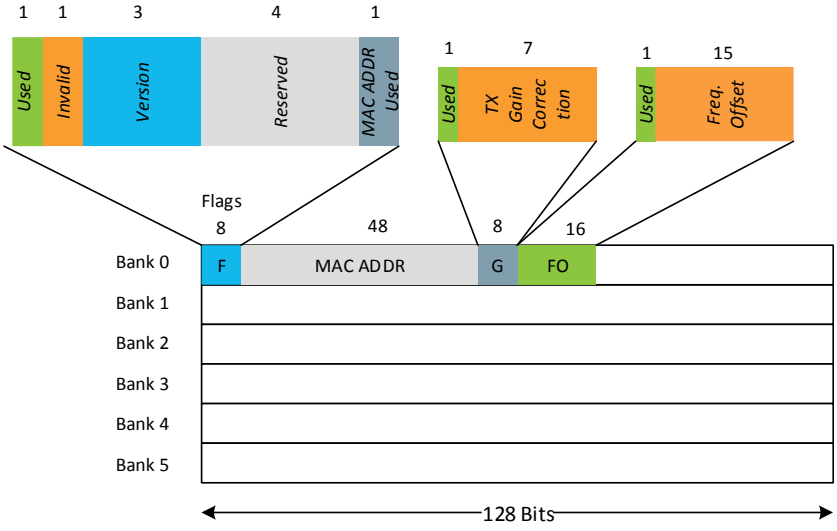
5.2 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 160KB instruction RAM and a 64KB data RAM. The ATWINC15x0-MR210xB modules come populated with either 4Mb or 8Mb of Flash memory depending on the module model that is ordered. This memory can be used for system software. See Table 1-1 for more information. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

5.3 Non-volatile Memory (eFuse)

The ATWINC15x0-MR210xB modules have 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bitmap (see following figure). The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming; for example, if the MAC address has to be changed, Bank 1 has to be programmed with the new MAC address along with the values of TX gain correction and frequency offset if they are used and programmed in Bank 0. The contents of Bank 0 have to be invalidated in this case by programming the invalid bit in the Bank 0. This will allow the firmware to use the MAC address. By default, all the ATWINC15x0-MR210xB modules are programmed with the MAC address and the frequency offset bits of Bank 0.

Figure 5-1. eFuse Bitmap



6. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

6.1 MAC

6.1.1 Description

The ATWINC15x0-MR210xB MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, and WPA2 CCMP-AES.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

6.1.2 Features

The ATWINC15x0-MR210xB IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate Block Acknowledgment
  - Reduced Interframe Spacing (RIFS)

- Support for IEEE802.11i and WFA security with key management:
  - WEP 64/128
  - WPA-TKIP
  - 128-bit WPA2 CCMP (AES)
- Advanced power management:
  - Standard 802.11 Power Save Mode
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode

6.2 PHY

6.2.1 Description

The ATWINC1500B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions that include FFT, filtering, FEC (Viterbi decoder), frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment, and automatic gain control.

6.2.2 Features

The ATWINC1500B IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

6.3 Radio

This section presents information describing the properties and characteristics of the ATWINC15x0-MR210xB and Wi-Fi radio transmit and receive performance capabilities of the device.

The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is guaranteed for room temperature of 25ºC with a derating of 2-3dB at boundary conditions.

Measurements were taken under typical conditions: VBATT=3.3V; VDDIO=3.3V; temperature: +25ºC

Table 6-1. Features and Properties

Feature	Description
Part Number	ATWINC15x0-MR210xB
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant

Feature	Description
Host Interface	SPI
Dimension	21.7 x 14.7 x 2.1 mm
Frequency Range	2.412GHz ~ 2.472GHz (2.4GHz ISM Band)
Number of Channels	11 for North America, and 13 for Europe
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM /64-QAM,16-QAM, QPSK, BPSK
Data Rate	802.11b: 1, 2, 5.5, 11Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz, normal GI, 800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz, short GI, 400ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Operating temperature	-40 to +85ºC
Storage temperature	-40 to +125 ºC
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

6.3.1 Receiver Performance

Table 6-2. Receiver Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency		2,412		2,472	MHz
Sensitivity 802.11b	1Mbps DSS		-95		dBm
	2Mbps DSS		-90		
	5.5Mbps DSS		-92		
	11Mbps DSS		-86		
Sensitivity 802.11g	6Mbps OFDM		-90		
	9Mbps OFDM		-89		
	12Mbps OFDM		-88		
	18Mbps OFDM		-85		
	24Mbps OFDM		-83		
	36Mbps OFDM		-80		
	48Mbps OFDM		-76		
	54Mbps OFDM		-74		

Parameter	Description	Minimum	Typical	Maximum	Unit
Sensitivity 802.11n (BW=20MHz)	MCS 0		-89		
	MCS 1		-87		
	MCS 2		-85		
	MCS 3		-82		
	MCS 4		-77		
	MCS 5		-74		
	MCS 6		-72		
	MCS 7		-70.5		
Maximum Receive Signal Level	1-11Mbps DSS		0		
	6-54Mbps OFDM		0		
	MCS 0 – 7		0		
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)		50		dB
	11Mbps DSS (25MHz offset)		43		
	6Mbps OFDM (25MHz offset)		40		
	54Mbps OFDM (25MHz offset)		25		
	MCS 0 – 20MHz BW (25MHz offset)		40		
	MCS 7 – 20MHz BW (25MHz offset)		20		
Cellular Blocker Immunity	776-794MHz CDMA		-14		dBm
	824-849MHz GSM		-10		
	880-915MHz GSM		-10		
	1710-1785MHz GSM		-15		
	1850-1910MHz GSM		-15		
	1850-1910MHz WCDMA		-24		
	1920-1980MHz WCDMA		-24		

6.3.2 Transmitter Performance

Table 6-3. Transmitter Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency	—	2,412	—	2,472	MHz
Output Power[1-2] ON_Transmit	802.11b 1Mbps	—	17.5	—	dBm
	802.11b 11Mbps	—	18.5	—	
	802.11g 6Mbps	—	17.5	—	
	802.11g 54Mbps	—	16	—	

Parameter	Description	Minimum	Typical	Maximum	Unit
	802.11n MCS 0	—	17.0	—	
	802.11n MCS 7	—	14.5	—	
TX Power Accuracy	—	—	±1.5 [2]	—	dB
Carrier Suppression	—	—	30.0	—	dBc
Harmonic Output Power	2nd	—		-41	dBm/MHz
	3rd	—	—	-41	

Note:

1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured after RF matching network.
3. Operating temperature range is -40°C to +85°C. RF performance guaranteed at room temperature of 25°C with a 2-3dB change at boundary conditions.
4. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
5. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the Host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via Host implementation.

7. External Interfaces

7.1 Interfacing with the Host Microcontroller

This section describes interfacing the ATWINC15x0-MR210xB module with the host microcontroller. The interface is comprised of a slave SPI and additional control signals, as shown in the following figure. For more information on SPI interface specification and timing, refer to the SPI Interface. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 7-1. Interfacing with Host Microcontroller

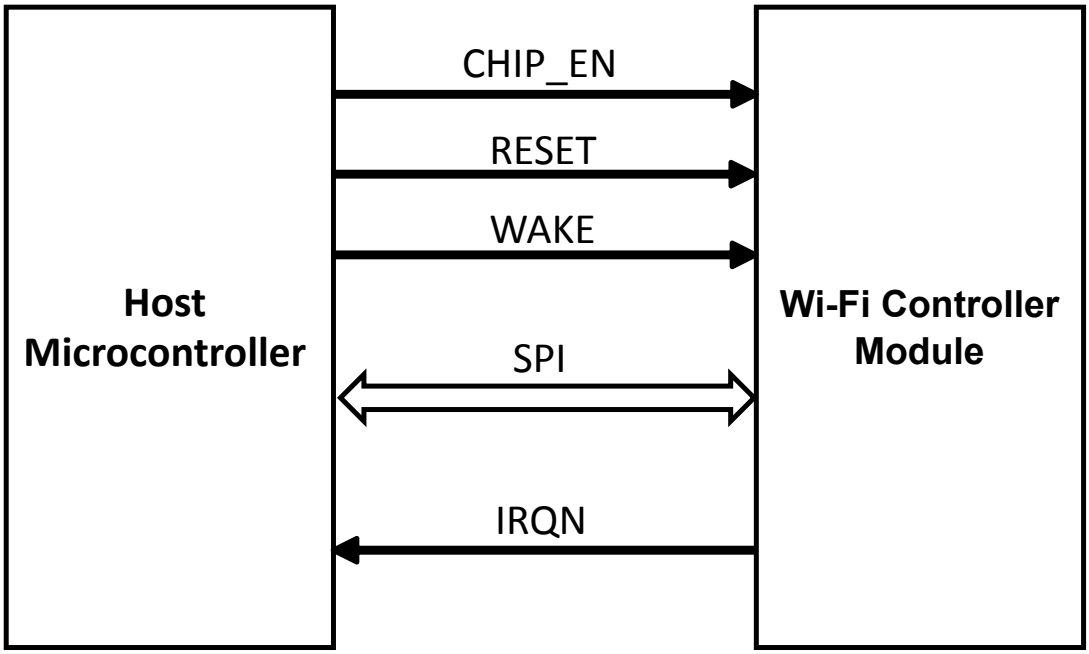


Table 7-1. Host Microcontroller Interface Pins

Pin Number	Function
4	RESET_N
11	WAKE
13	IRQ_N
22	CHIP_EN
16	SPI_SSN
15	SPI_MOSI
17	SPI_MISO
18	SPI_SCK

Related Links

SPI Interface

7.2 SPI Interface

7.2.1 Overview

The ATWINC15x0-MR210xB has a Serial Peripheral Interface (SPI) that operates as an SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in the following table. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

Table 7-2. SPI Interface Pin Mapping

Pin #	SPI function
10	CFG: Must be tied to VDDIO
16	SSN: Active-Low Slave Select
15	MOSI(RXD): Serial Data Receive
18	SCK: Serial Clock
17	MISO(TXD): Serial Data Transmit

When the SPI is not selected, that is, when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO, and SCK pins of the ATWINC15x0-MR210xB have internal programmable pull-up resistors. These resistors should be programmed to be disabled; otherwise, if any of the SPI pins are driven to a low level while the ATWINC15x0-MR210xB is in the low power sleep state, the current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

Related Links

Programmable Pull Up Resistors

7.2.2 SPI Timing

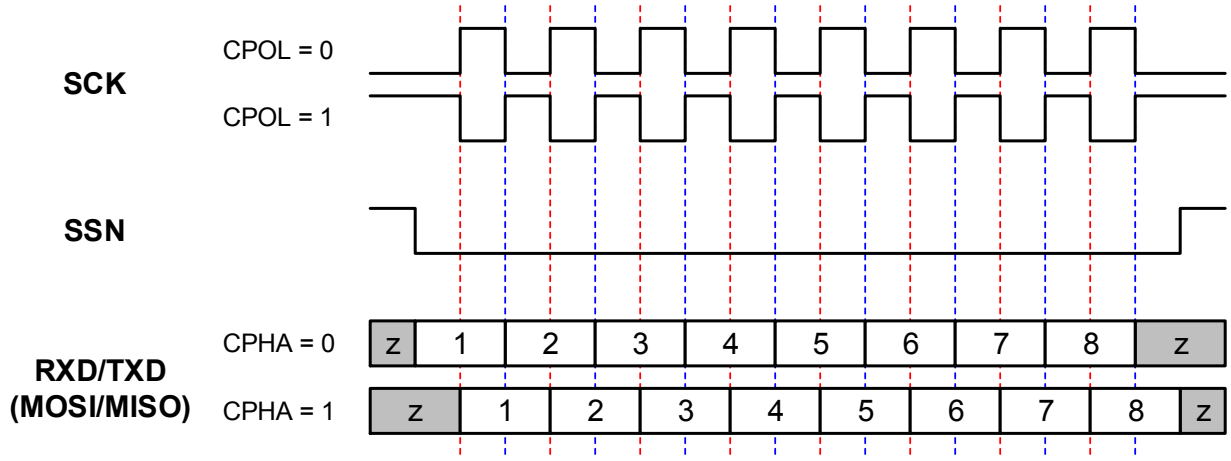
The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

Table 7-3. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

The red lines in the following figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Figure 7-2. SPI Slave Clock Polarity and Clock Phase Timing



The SPI timing is provided in the following figure and table.

Figure 7-3. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)

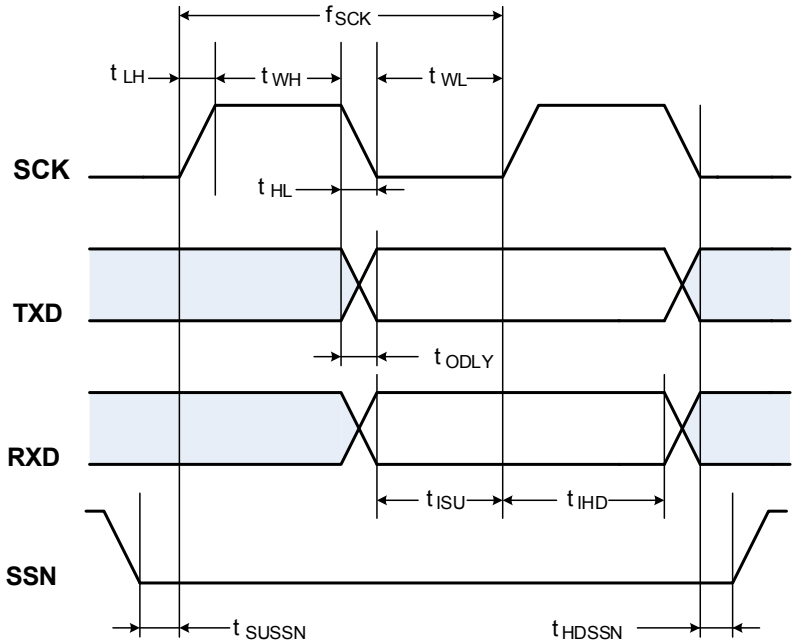


Table 7-4. SPI Slave Timing Parameters[1]

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency[2]	f_{SCK}	—	48	MHz
Clock Low Pulse Width	t_{WL}	4	—	ns
Clock High Pulse Width	t_{WH}	5	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	

Parameter	Symbol	Min.	Max.	Units
TXD Output Delay[3]	t_{ODLY}	4	9 from SCK fall 12.5 from SCK rise	
RXD Input Setup Time	t_{ISU}	1	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	3	—	
SSN Input Hold Time	t_{HDSSN}	5.5	—	

Note:

1. Timing is applicable to all SPI modes
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design, actual maximum clock frequency can be lower and depends on the specific PCB layout
3. Timing based on 15pF output loading

7.3 UART Interface

The ATWINC15x0-MR210xB supports the Universal Asynchronous Receiver/Transmitter (UART) interface. This interface should be used for debug purposes only. The UART is available on pins 14 and 19. The UART is compatible with the RS-232 standard, and the ATWINC15x0-MR210xB operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

The default configuration for accessing the UART interface of ATWINC15x0-MR210xB is mentioned below:

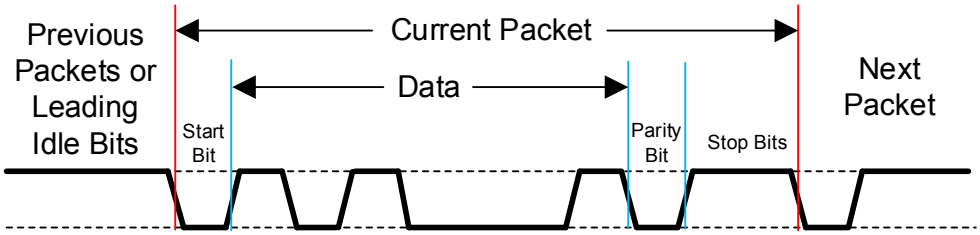
- Baud rate: 115200
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of the UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Important: UART2 supports RTS and CTS flow control. The UART RTS and UART CTS MUST be connected to the host MCU UART and enabled for the UART interface to be functional.

Figure 7-4. Example of UART RX of TX Packet



8. Power Consumption

8.1 Description of Device States

The ATWINC15x0-MR210xB has several device states:

- ON_Transmit – Device is actively transmitting an 802.11 signal. Highest output power and nominal current consumption.
- ON_Receive – Device is actively receiving an 802.11 signal. Lowest sensitivity and nominal current consumption.
- ON_Doze – Device is ON but is neither transmitting nor receiving
- Power_Down – Device core supply off (Leakage)
- IDLE connect – Device is connected with 1 DTIM beacon interval

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – Device pin (pin #22) used to enable DC/DC Converter
- VDDIO – I/O supply voltage from external supply
  In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state CHIP_EN has to change between high and low (GND) voltage. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see Restrictions for Power States).

8.2 Current Consumption in Various Device States

Table 8-1. Current Consumption

Device State	Code Rate	Output power, dBm	Current Consumption [1]	
			IVBATT	IVDDIO
ON_Transmit	802.11b 1Mbps	17.5	268mA	22mA
	802.11b 11Mbps	18.5	264mA	22mA
	802.11g 6Mbps	17.5	269mA	22mA
	802.11g 54Mbps	16.0	266mA	22mA
	802.11n MCS 0	17.0	268mA	22mA
	802.11n MCS 7	14.5	265mA	22mA
ON_Receive	802.11b 1Mbps	N/A	61mA	22mA
	802.11b 11Mbps	N/A	61mA	22mA
	802.11g 6Mbps	N/A	61mA	22mA
	802.11g 54Mbps	N/A	61mA	22mA
	802.11n MCS 0	N/A	61mA	22mA
	802.11n MCS 7	N/A	61mA	22mA

Device State	Code Rate	Output power, dBm	Current Consumption [1]	
			IVBATT	IVDDIO
ON_Doze	N/A	N/A	380µA	<10µA
Power_Down	N/A	N/A	<0.5µA	<3.5µA

Note:

1. Measured conditions: VBATT @ 3.3V, VDDIO@ 3.3V, temp. 25°C.

8.3 Restrictions for Power States

When no power is supplied to the device, for example, the DC/DC Converter output and VDDIO are both off (at ground potential), a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when a voltage higher than one diode drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low-power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode drop below ground to any pin.

8.4 Power-up/down Sequence

The power-up/down sequence for ATWINC15x0-MR210xB is shown in the Following Figure. The timing parameters are provided in following the table.

Figure 8-1. Power Up/Down Sequence

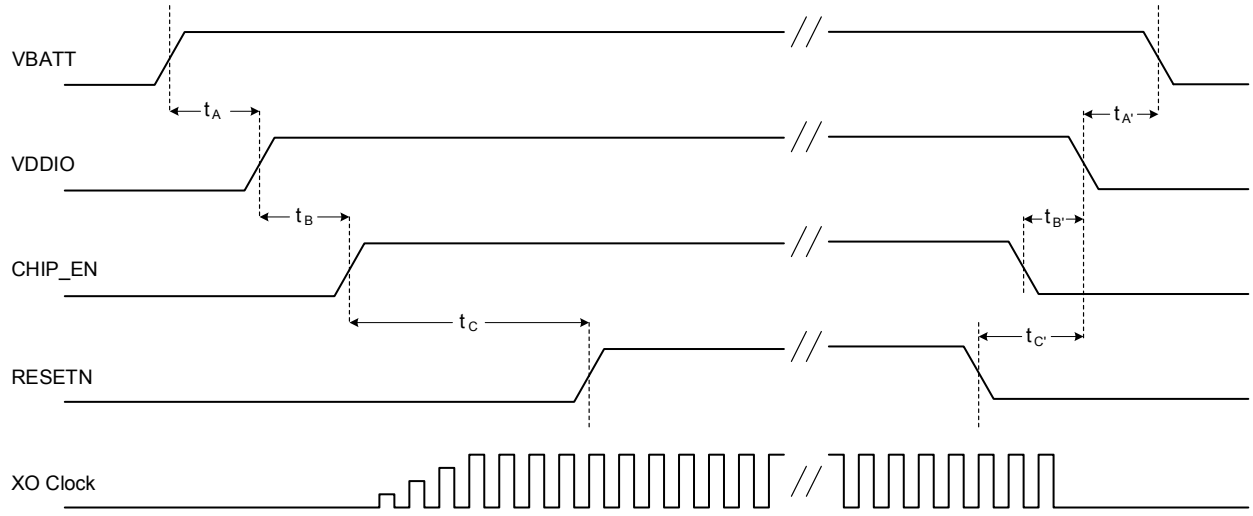


Table 8-2. Power-up/down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied

Parameter	Min.	Max.	Units	Description	Notes
					together. VDDIO must not rise before VBATT.
t_B	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5		ms	CHIP_EN rise to RESETN rise	This delay is needed because the XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0		ms	VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0		ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0		ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

8.5 Digital I/O Pin Behavior During Power-up Sequences

The following table represents digital I/O Pin states corresponding to device power modes.

Table 8-3. Digital I/O Pin Behavior in Different Device States

Device state	VDDIO	CHIP_EN	RESETN	Output driver	Input driver	Pull up/down resistor (96kΩ)
Power-Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-on Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, the device is out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On Sleep/ On Transmit/ On Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

8.6 Module Reset

If a module reset is performed, the RESETN pin must be pulsed low for a minimum of 1µ second.

9. Notes On Interfacing to the ATWINC15x0-MR210xB

9.1 Programmable Pull Up Resistors

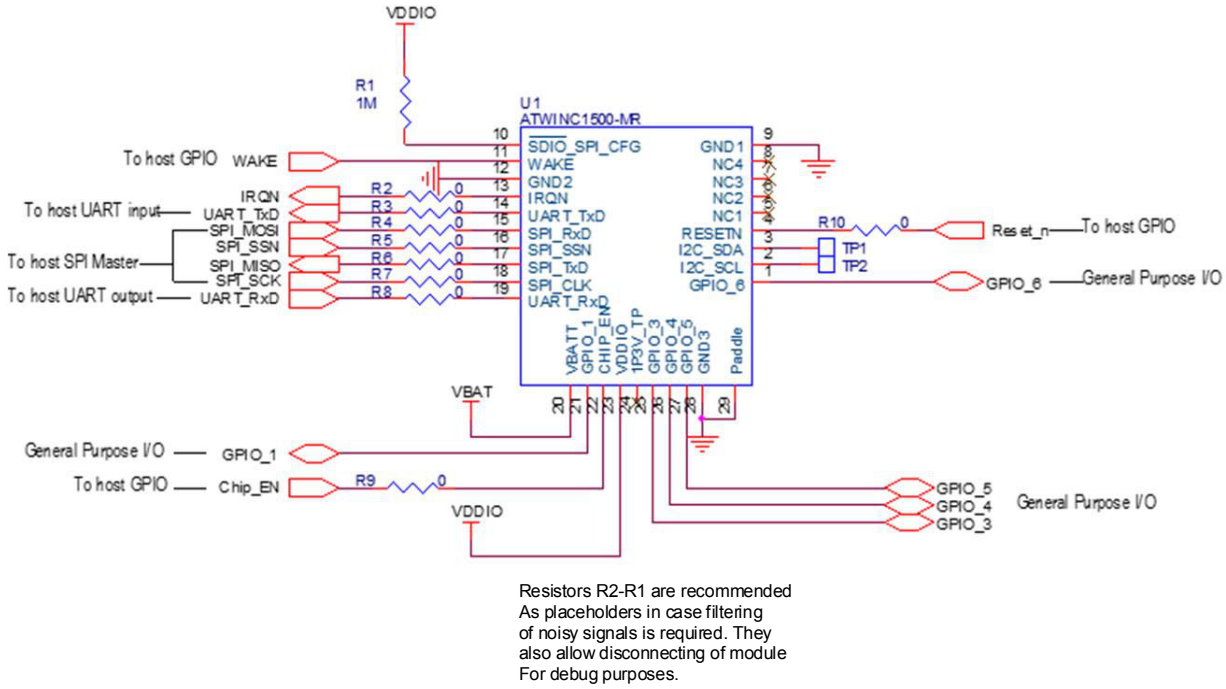
The ATWINC15x0-MR210xB provides programmable pull up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating, which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused module pin on the ATWINC15x0-MR210xB should leave these pull up resistors enabled so the pin will not float. The default state at power-up is for the pull up resistor to be enabled. However, any pin that is used should have the pull up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATWINC15x0-MR210xB is in the low power sleep state, current will flow from the VDDIO supply through the pull up resistors, increasing the current consumption of the module. Since the value of the pull up resistor is approximately 100KΩ, the current through any pull up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current through each pull up resistor that is driven low would be approximately 3.3V/100K = 33µA. Pins which are used and have had the programmable pull up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

10. Schematic Design Information

This section provides schematic information for reference. Application schematics for SPI are provided in the following figure. Module design information such as module schematics can be obtained under an NDA from Microchip. These schematics are applicable to the ATWINC1500-MR210PB, ATWINC1510-MR210PB and the ATWINC1500-MR210UB modules.

10.1 Application Schematic

Figure 10-1. SPI Application Schematic



Note: Add 10uF and 0.01uF decoupling capacitors between the pin 24 (1P3V_TP) and GND.

11. Module Drawing

This section provides information about the module package outline drawings.

Figure 11-1. Module Drawing - ATWINC15x0-MR210PB (unit = mm)

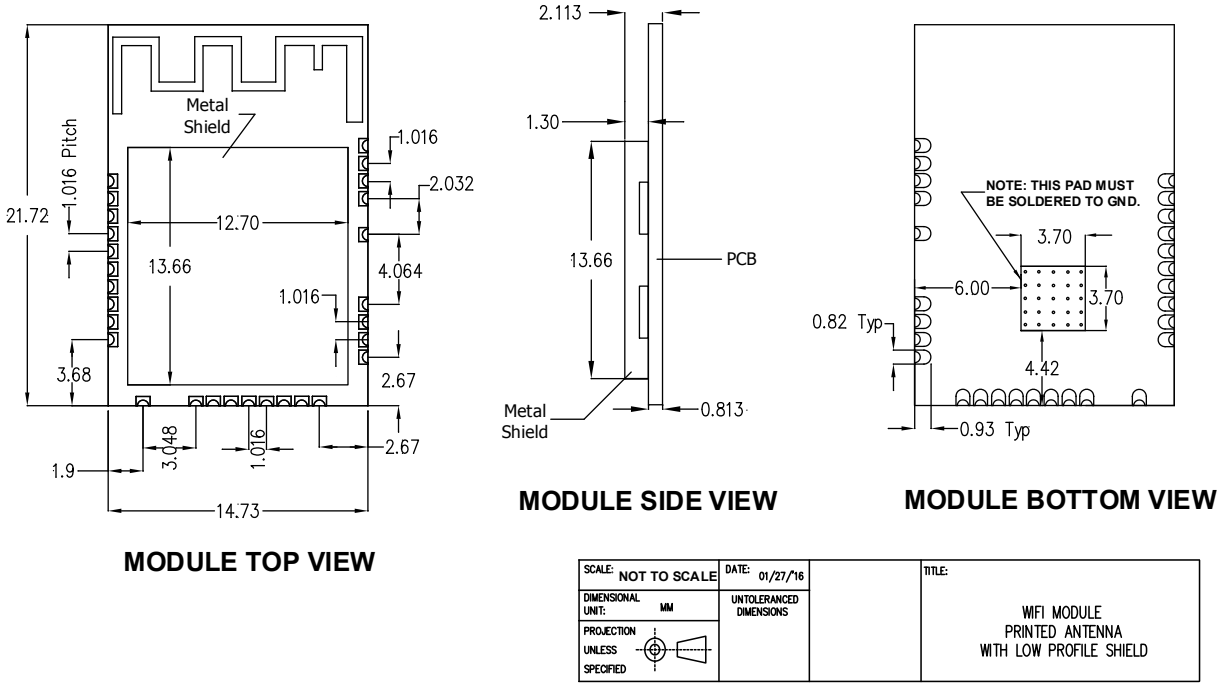
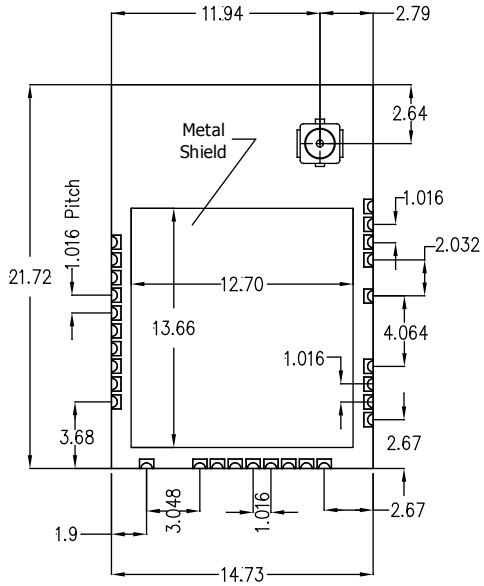
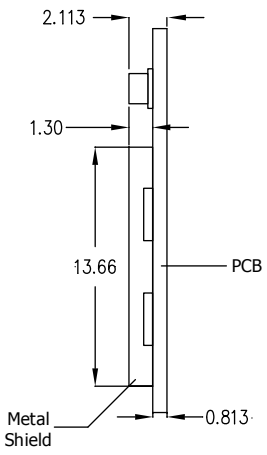


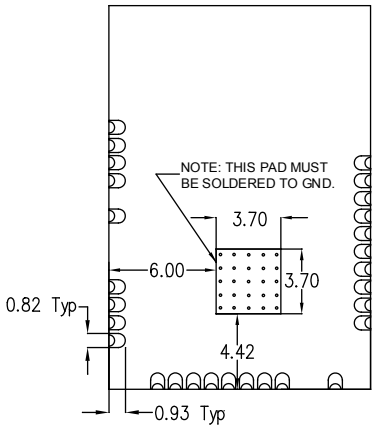
Figure 11-2. Module Drawings – ATWINC15x0-MR210UB (unit = mm)



MODULE TOP VIEW



MODULE SIDE VIEW



MODULE BOTTOM VIEW

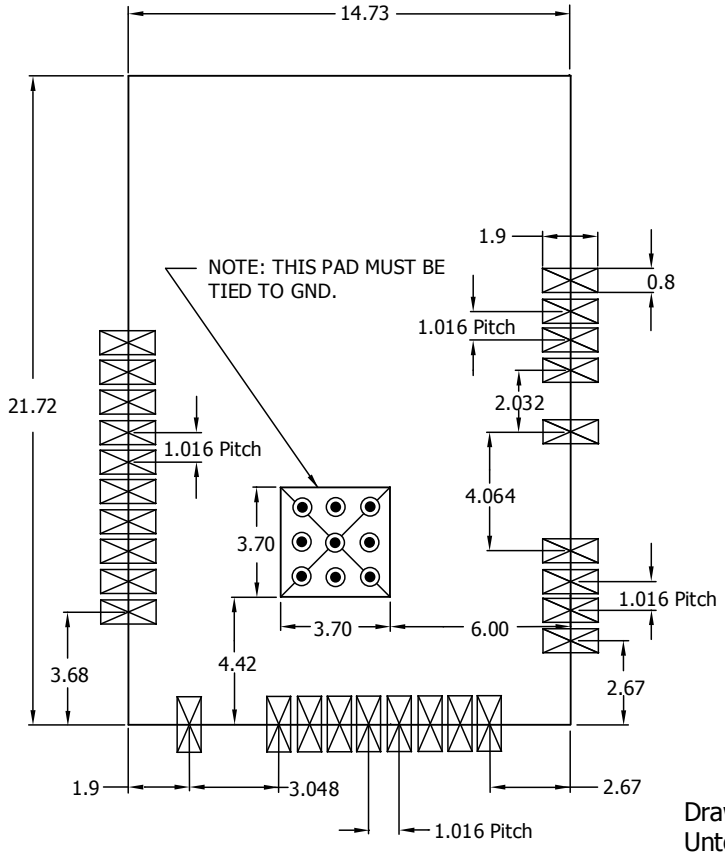
SCALE: NOT TO SCALE	DATE: 12/04/'15	Rev. 2	TITLE: WIFI MODULE uFL ANTENNA WITH LOW PROFILE SHIELD
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS		
PROJECTION UNLESS SPECIFIED			

11.1 Module Footprint

This section provides the outline drawing for the recommended footprint for the ATWINC15x0-MR210xB module. It is imperative that the center Ground Pad is provided, with an array of vias to provide for a good ground and thermal transfer for the ATWINC15x0-MR210xB module.

This footprint is applicable to the ATWINC15x0-MR210xB module devices.

Figure 11-3. Module Solder Pad Footprint (unit = mm).



SOLDER PAD FOOTPRINT

Drawing not to scale.
Untoleranced dimensions.
Units=mm.

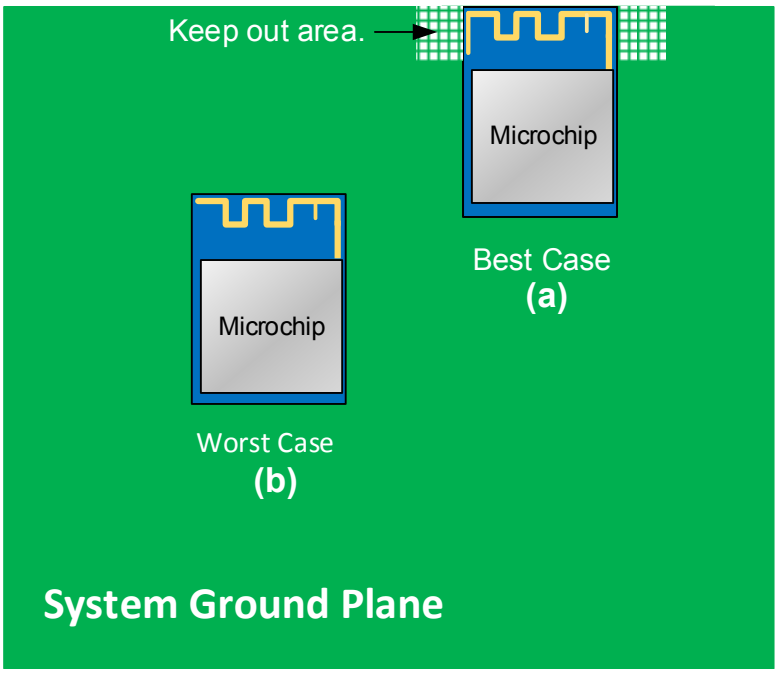
12. Design Considerations

This section provides the guidelines on placement and routing to achieve the best performance.

12.1 ATWINC15x0-MR210PB Placement and Routing Guidelines

- The module must be placed on the main board – the printed antenna area must overlap with the carrier board. The portion of the module containing the antenna should not go outside the edge of the main board. The antenna is designed to work properly when it is sitting directly on top of a 1.5mm thick printed circuit board.
- If the module is placed at the edge of the main board, a minimum 22mm by 5mm area directly under the antenna must be clear of all metal on all layers of the board. “In-land” placement is acceptable; however deepness of keep-out area must grove to: module edge to main board edge plus 5mm. DO NOT PLACE THE MODULE IN THE MIDDLE OF THE MAIN BOARD OR FAR AWAY FROM THE MAIN BOARD EDGE.
- Keep away from the antenna, as far as possible, large metal objects to avoid electromagnetic field blocking
- Do not enclose the antenna within a metal shield
- Keep any components which may radiate noise or signals within the 2.4GHz-2.5GHz frequency band as far away from the antenna as possible, or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.

Figure 12-1. ATWINC15x0-MR210PB Placement Reference



12.2 Printed PCB Antenna Performance of ATWINC15x0-MR210PB

The printed PCB antenna on the ATWINC15x0-MR210PB is a meandered Inverted F Antenna (IFA). The antenna is fed via matching network, which is matched for the module installed on a 1.5mm thick main

board. Main board thickness deviation by ±1mm changes RX/TX performance by ±1dB maximum, referring to RX/TX performance with a default antenna matching network and installed on 1.5mm thick main board.

Measured peak antenna gain is -0.3dBi.

Antenna Radiation Pattern

Following figures illustrate the Antenna Radiation Patterns.

Figure 12-2. Antenna Radiation Pattern when Phi = 0 degree

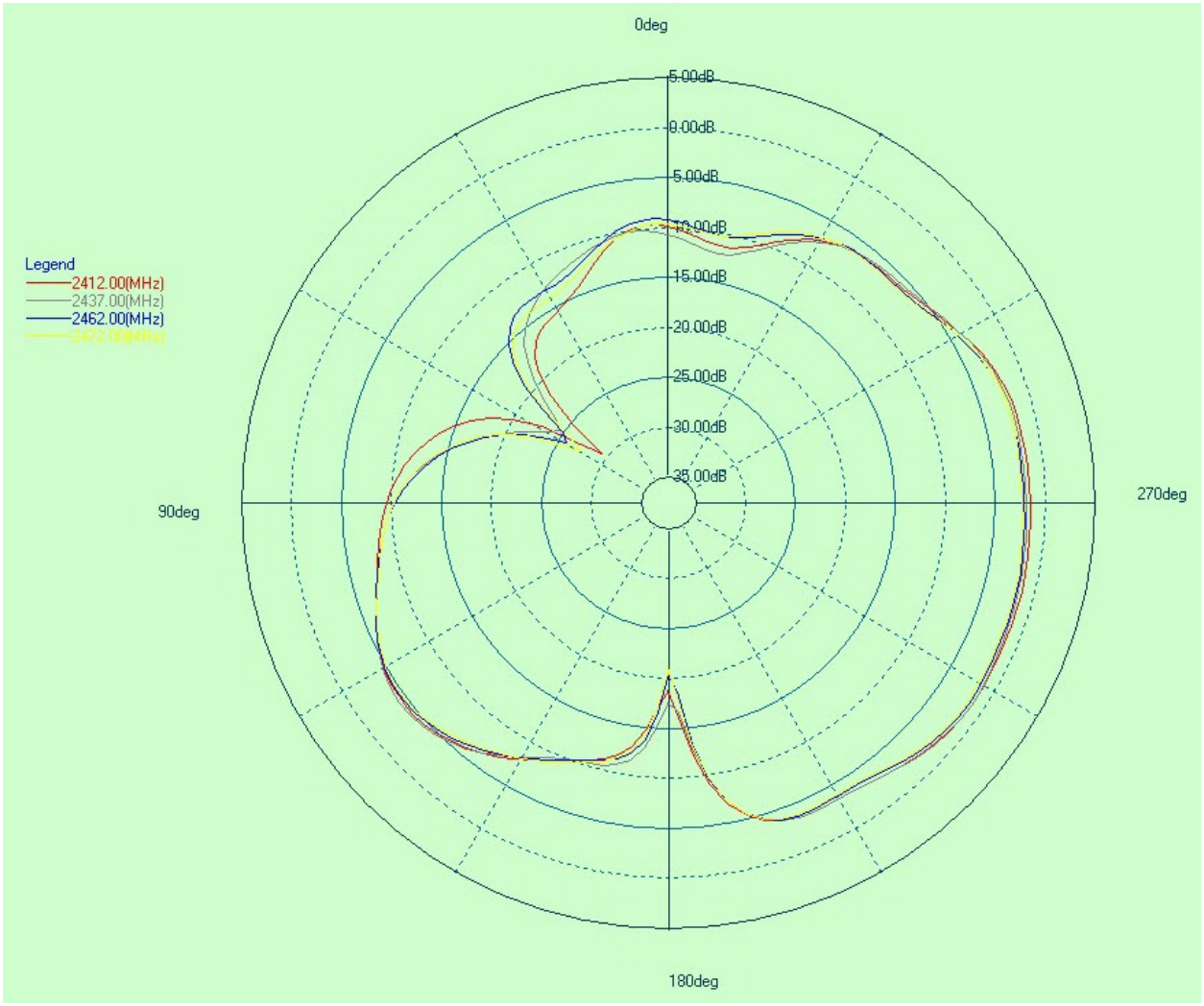


Figure 12-3. Antenna Radiation Pattern when Phi = 90 degree

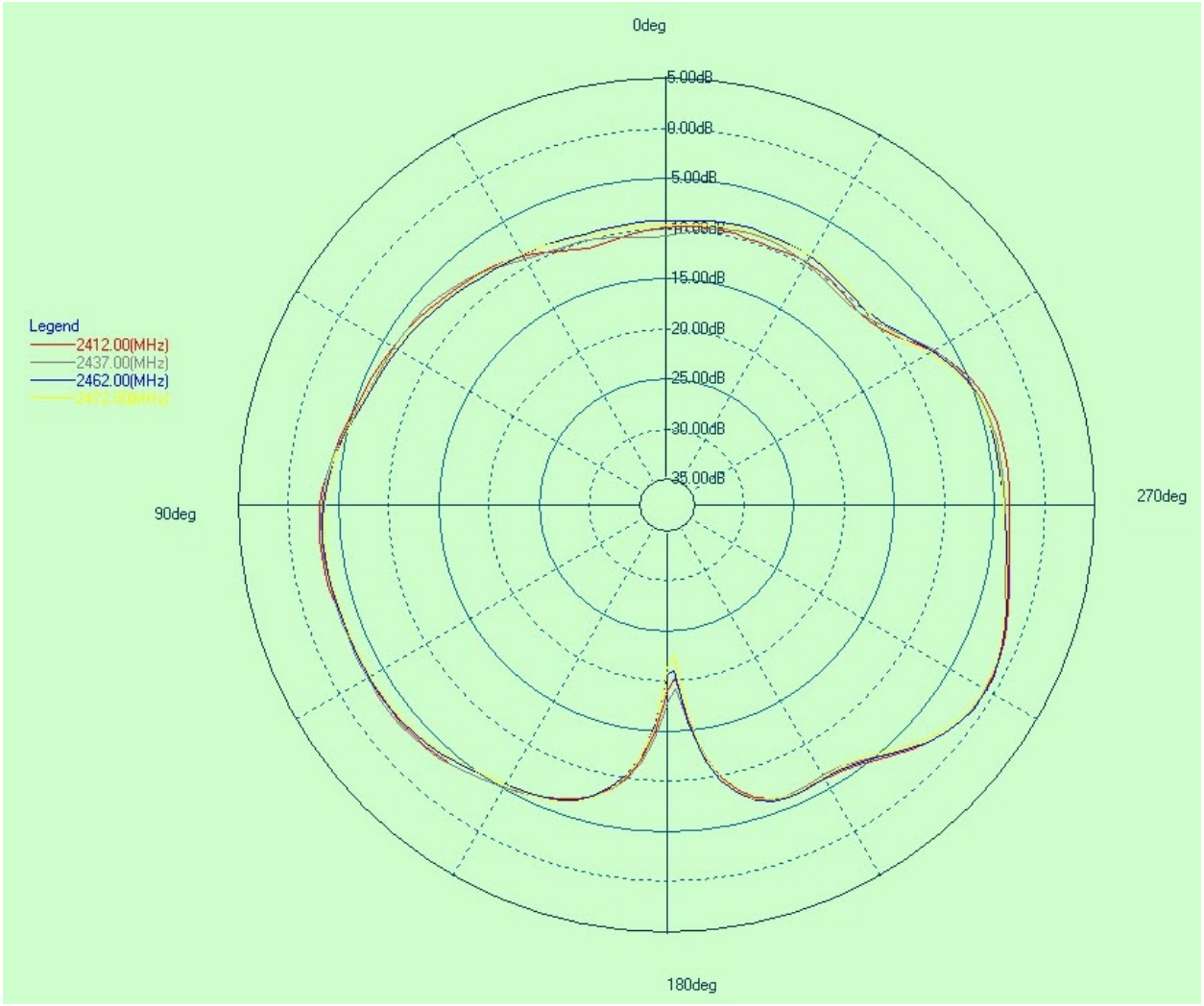
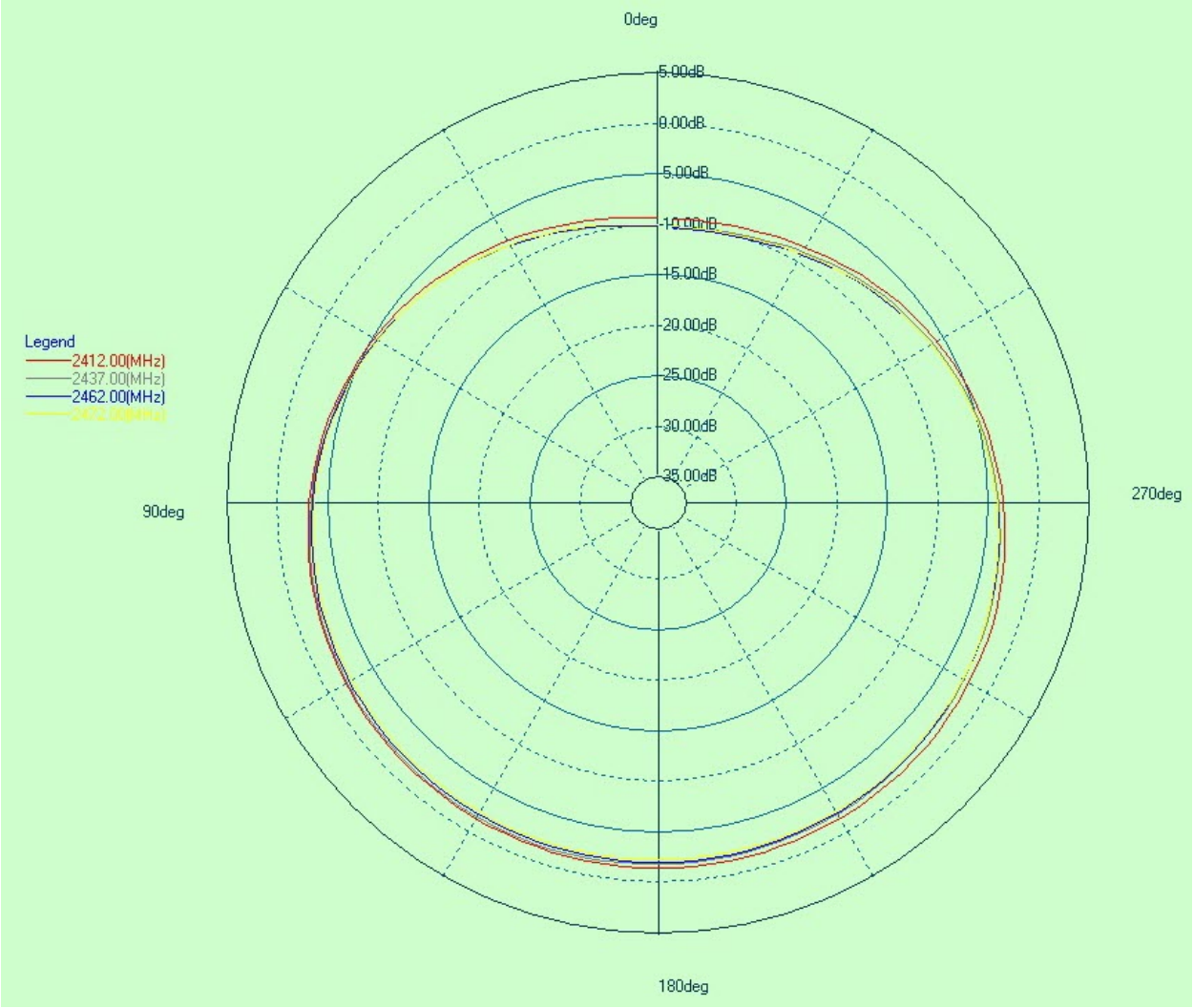


Figure 12-4. Antenna Radiation Pattern when Theta = 90 degree



12.3 ATWINC15x0-MR210UB Placement and Routing Guidelines

The ATWINC15x0-MR210UB module has an Ultra Small Miniature RF Connector (u.FL) for the external antenna.

The choice of antenna is limited to the antenna types for which the module was tested and approved. For a list of tested and approved antennas that may be used with the module, refer to the respective country in Regulatory Approval.

An approved and tested antenna type is shown in the following table.

Table 12-1. Tested External Antenna Type

Antenna Type	Gain
Whip Antenna	2.2dBi

12.3.1 Recommended External Antenna for ATWINC15x0-MR210UB

Whip Antenna (Part number: RN-SMA-4) along with a 10cm length RF cable assembly (u.FL to SMA) has been used for the certification of ATWINC15x0-MR210UB. It is recommended to use the same or similar external antenna in design.

12.4 Module Assembly Considerations

The ATWINC15x0-MR210xB modules are assembled with an EMI Shield to ensure compliance with EMI emission and immunity rules. The EMI shield is made of a tin-plated steel (SPTE) and is not hermetically sealed. Solutions like IPA and similar solvents can be used to clean the ATWINC15x0-MR210xB module. However, cleaning solutions that contain acid should never be used on the module.

The ATWINC15x0-MR210xB modules are manufactured without any conformal coating applied. It is the customer's responsibility if a conformal coating is specified and/or applied to the ATWINC15x0-MR210xB module.

13. Reflow Profile Information

This chapter provides guidelines for reflow processes in getting the Microchip module soldered to the customer's design.

13.1 Storage Condition

13.1.1 Moisture Barrier Bag Before Opening

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH.

The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

13.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, <30%.

13.2 Solder Paste

Sn-Ag-Cu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance. Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V Type 3, no clean paste.

13.3 Stencil Design

The recommended stencil is laser-cut, stainless steel type with a thickness of 100µm to 130µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25µm larger than the top can be utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

13.4 Printing Process

The printing process requires no significant changes compared to Sn/Pb solder. Any guidelines recommended by the paste manufacturers to accommodate paste specific characteristics should be followed. Post-print inspection and paste volume measurement is very critical to ensure good print quality and uniform paste.

13.5 Baking Conditions

This module is rated at MSL level 3. After a sealed bag is opened, no baking is required within 168 hours so long as the devices are held at ≤30°C/60% RH or stored at <10% RH.

The module will require baking before mounting if:

- The sealed bag has been open for >168 hours
- Humidity Indicator Card reads >10%
- SIPs need to be baked for 8 hours at 125°C

13.6 Soldering and Reflow Condition

The optimization of the reflow process is the most critical factor to be considered for lead-free soldering. The development of an optimal profile should take into account the paste characteristics, the size of the board, the density of the components, the mix of the larger and smaller components, and the peak temperature requirements of the components. An optimized reflow process is the key to ensuring a successful lead-free assembly and achieves high yield and long term solder joint reliability.

Temperature Profiling

Temperature profiling should be performed for all new board designs by attaching thermocouples at the solder joints, on the top surface of the larger components, and at multiple locations of the boards. This is to ensure that all components are heated to a temperature above the minimum reflow temperatures and the smaller components do not exceed maximum temperature limit. The SnAgCu solder alloy melts at ~217°C, so the reflow temperature peak at joint level should be 15 to 20°C higher than melting temperature. The targeted solder joint temperature for the Sn-Ag-Cu solder should be ~235°C. For larger or sophisticated boards with a large mix of components, it is also important to ensure that the temperature difference across the board is less than 10 degrees to minimize board warpage. The maximum temperature at the component body should not exceed the MSL3 qualification specification.

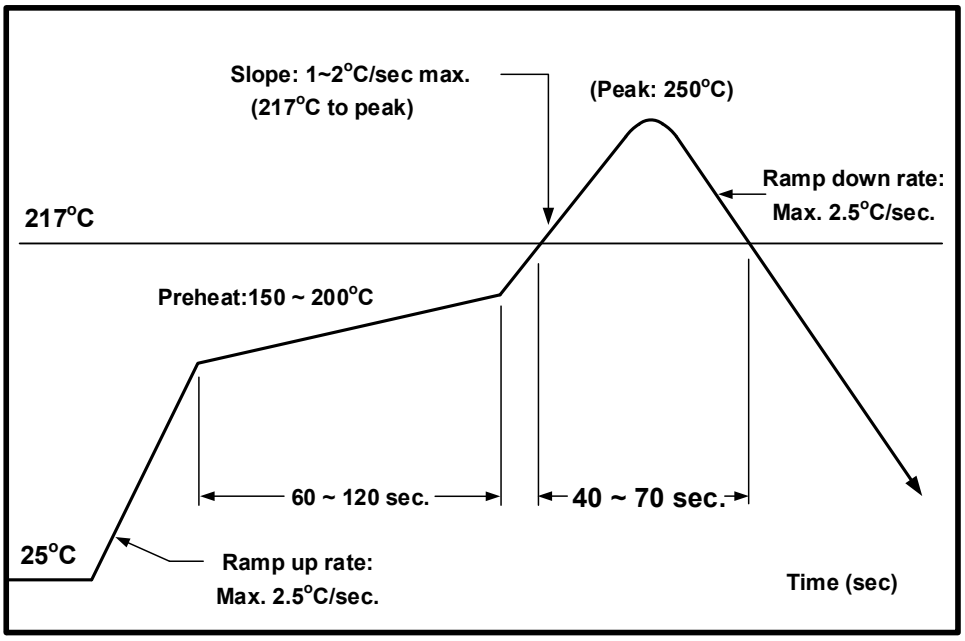
13.6.1 Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere should be used for lead-free assembly. Nitrogen atmosphere has shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items should also be observed in the reflow process:

1. Some recommended pastes include:
   - NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu
   - SENJU N705-GRN3360-K2-V Type 3, no clean paste.
2. Allowable reflow soldering iterations:
   - Three times based on the following reflow soldering profile (refer following Figure).
3. Temperature profile:
   - Reflow soldering shall be done according to the following temperature profile (refer to the following figure).
   - Peak temperature: 250°C.

Figure 13-1. Solder Reflow Profile



Cleaning

The exposed ground paddle helps to self-align the module, avoiding pad misalignment. The use of no clean solder pastes is recommended. Full drying of no-clean paste fluxes as a result of the reflow process must be ensured. This may require longer reflow profiles and/or peak temperatures toward the high end of the process window as recommended by the solder paste vendor. It is believed that uncured flux residues could lead to corrosion and/or shorting in accelerated testing and possibly the field.

Rework

Rework is to remove the mounted SIP package and replace with a new unit. It is recommended that once an ATWINC15x0-MR210xB Module has been removed it should never be reused. During the rework process, the mounted module and PCB are heated partially, and the module is removed. It is recommended to pay attention to heat-proof the proximity of the mounted parts and junctions and use the best nozzle for rework that is suited to the module size.

14. Regulatory Approval

Regulatory Approvals received.

ATWINC1500-MR210PB

- United States/FCC ID: 2ADHKATWINC1500
- Canada
  - IC: 20266-WINC1500PB
  - HVIN: ATWINC1500-MR210PB
- Europe - CE

ATWINC1510-MR210PB

- United States/FCC ID: 2ADHKATWINC1510
- Canada
  - IC: 20266-ATWINC1510
  - HVIN: ATWINC1510-MR210PB
- Europe - CE

ATWINC1500-MR210UB

- United States/FCC ID: 2ADHKATWINC1500U
- Canada
  - IC: 20266-WINC1500UB
  - HVIN: ATWINC1500-MR210UB

14.1 United States

The ATWINC1500-MR210PB, ATWINC1510-MR210PB and ATWINC1500-MR210UB modules have received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product, or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Verification or Declaration of Conformity) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).

14.1.1 Labeling And User Information Requirements

The ATWINC1500-MR210PB, ATWINC1510-MR210PB and ATWINC1500-MR210UB modules have been labeled with its own FCC ID number, and if the FCC ID is not visible when the module is installed

inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label should use the following wording:

For the ATWINC1500-MR210PB:

Contains Transmitter Module FCC ID: 2ADHKATWINC1500

or

Contains FCC ID: 2ADHKATWINC1500

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For the ATWINC1510-MR210PB:

Contains Transmitter Module FCC ID: 2ADHKATWINC1510

or

Contains FCC ID: 2ADHKATWINC1510

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For the ATWINC1500-MR210UB:

Contains Transmitter Module FCC ID: 2ADHKATWINC1500U

or

Contains FCC ID: 2ADHKATWINC1500U

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

The user's manual for the finished product should include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) https://apps.fcc.gov/oetcf/kdb/index.cfm.

14.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification.

In the end product, the antenna(s) used with this transmitter must be installed to provide a separation distance of at least 6.5 cm from all persons and must not be co-located or operation in conjunction with any other antenna or transmitter. User and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying the RF exposure compliance.

14.1.3 Approved Antenna Types

To maintain modular approval in the United States, only the antenna types that have been tested shall be used. It is permissible to use different antenna provided the same antenna type and antenna gain (equal to or less than) is used. An antenna type comprises antennas having similar in-band and out-of-band radiation patterns.

Testing the ATWINC1500-MR210UB module was performed with the antenna types listed in Table 12-1.

14.1.4 Helpful Web Sites

Federal Communications Commission (FCC): http://www.fcc.gov

FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB)

https://apps.fcc.gov/oetcf/kdb/index.cfm

14.2 Canada

The ATWINC1500-MR210PB, ATWINC1510-MR210PB and ATWINC1500-MR210UB modules have been certified for use in Canada under Innovation, Science, and Economic Development Canada (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

14.2.1 Labeling and User Information Requirements

Labeling Requirements (from RSP-100 - Issue 11, Section 3): The host product shall be properly labeled to identify the module within the host device.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number of the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:

For the ATWINC1500-MR210PB:

Contains IC: 20266-WINC1500PB

For the ATWINC1510-MR210PB:

Contains IC: 20266-ATWINC1510

For the ATWINC1500-MR210UB module:

Contains IC: 20266-WINC1500UB

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 4, November 2014): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device complies with Industry Canada's license exempt RSS standard(s). Operation is subject to the following two conditions:

(1) This device may not cause interference, and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Guidelines on Transmitter Antenna for License Exempt Radio Apparatus:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établisse-ment d'une communication satisfaisante.

Immediately following the above notice, the manufacturer shall provide a list of all antenna types approved for use with the transmitter, indicating the maximum permissible antenna gain (in dBi) and required impedance for each.

14.2.2 Transmitter Antenna (From Section 8.3 RSS-GEN, Issue 4, November 2014)

User manuals for transmitters equipped with detachable antennas shall also contain the following notice in a conspicuous location:

This radio transmitter (identify the device by certification number, or model number if Category II) has been approved by Industry Canada to operate with the antenna types listed below with the maximum permissible gain and required antenna impedance for each antenna type indicated.

Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Le présent émetteur radio (identifier le dispositif par son numéro de certification) a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

14.2.3 RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radiocommunication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The installation of the transmitter must ensure that the antenna has a separation distance of at least 6.5 cm from all persons or compliance must be demonstrated according to the ISED SAR procedures.

14.2.4 Helpful Web Sites

Innovation, Science and Economic Development Canada (ISED): http://www.ic.gc.ca/

14.3 Europe

The ATWINC15x0-MR210PB module is a Radio Equipment Directive (RED) assessed radio module that is CE marked and has been manufactured and tested with the intention of being integrated into a final product.

The ATWINC15x0-MR210PB module has been tested to RED 2014/53/EU Essential Requirements for Health and Safety (Article (3.1(a)), Electromagnetic Compatibility (EMC) (Article 3.1(b)), and Radio (Article 3.2), which is summarized in the following European Compliance Testing table.

The ETSI provides guidance on modular devices in the "*Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the RED 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment*" document available at http://www.etsi.org/deliver/etsi_eg/203300_203399/203367/01.01.01_60/eg_203367v010101p.pdf.

Note: To maintain conformance to the testing listed in the following European Compliance Testing table the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified. When integrating a radio module into a completed product, the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

14.3.1 Labeling and User Information Requirements

The label on the final product that contains the ATWINC15x0-MR210PB module must follow CE marking requirements.

Table 14-1. European Compliance Testing (ATWINC15x0-MR210PB)

Certification	Standards	Article	Laboratory	Report Number	Date
Safety	EN60950-1:2006/A11:2009/ A1:2010/ A12:2011/A2:2013	[3.1(a)]	TUV Rheinland, Taiwan	10059657 001	2017-02-20
Health	EN300328 V1.9.1/ EN62311:2008			50068130 002	2017-02-20
EMC	EN301489-1 V1.9.2	[3.1(b)]		10058459 002	2017-02-20
	EN301489-17 V2.2.1				
	EN301489-1 V2.1.1 EN301489-1 V2.2.0			10058459 003	2017-05-25
	EN301489-17 V3.1.1 EN301489-17 V3.2.0				
Radio	EN300328 V1.9.1	(3.2)		50068130 002	2017-02-20
	EN300328 V2.1.1			50068130 003	2017-05-26

14.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1, when non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

The European Compliance Testing listed in the preceeding table was performed using the integral chip antenna.

14.3.2.1 Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type ATWINC15x0-MR210PB is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity for this product is available at http://www.microchip.com/design-centers/wireless-connectivity/.

14.3.3 Helpful Websites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: http://www.ecodocdb.dk/.

Additional helpful web sites are:

- Radio Equipment Directive (2014/53/EU): https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/red_en
- European Conference of Postal and Telecommunications Administrations (CEPT): http://www.cept.org

- European Telecommunications Standards Institute (ETSI): http://www.etsi.org
- The Radio Equipment Directive Compliance Association (REDCA): http://www.redca.eu/

14.4 Other Regulatory Information

- For information about other countries' jurisdictions not covered here, refer to http://www.microchip.com/design-centers/wireless-connectivity
- Should other regulatory jurisdiction certification be required by the customer, or the customer needs to recertify the module for other reasons, contact Microchip for the required utilities and documentation

15. Reference Documentation and Support

15.1 Reference Documents

The following table provides the set of collateral documents to ease integration and device ramp.

Table 15-1. Reference Documents

Title	Content
ATWINC1500 MU Device Datasheet	Datasheet for the ATWINC1500 SmartConnect Wi-Fi component. For more details, contact a Microchip sales representative.
Platform Getting Started Guide	Details on how to evaluate the WINC15X0 Network Controller Module.
Flash Memory Download Procedure	Details the download procedures of firmware, root certificate, gain table values, etc.
ATWINC1500 Wi-Fi Network Controller Software Design Guide	Integration guide with a clear description of High-level Arch, an overview on how to write a networking application, list all APIs, parameters, and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, and timing.
Software Programming Guide (ATWINC15x0)	Details the flow chart and how to use each API to implement all generic use cases (for example, start AP, start STA, provisioning, UDP, TCP, HTTP, TLS, p2p, errors management, connection/ transfer recovery mechanism/state diagram) - usage and sample application note.

Note: A Design Files Package is available under NDA. For more details, contact a Microchip sales representative.

For a complete listing of development-support tools and documentation, visit www.microchip.com, or refer to the customer support section on options to locate the nearest Microchip field representative.

16. Document Revision History

Note: The datasheet revision is independent of the die revision (Revision bit in the Device Identification register of the Device Service Unit, DSU.DID.REVISION) and the device variant (last letter of the ordering number).

Rev B - 12/2017

Section	Changes
Introduction	Editorial updates.
Features	Editorial updates.
Regulatory Approvals	Revised the content of certifications.
Reference Documents	Updated Table 15-1.

Rev A - 02/2017

Section	Changes
Document	• Change of document style. • Change the name to incorporate all the ATWINC15x0-MR210xB module family. • New Microchip document number. Previous version was Atmel document 42502 rev. B.
Product Description	• Added description information indicating that the document content is relevant to all WINC1500 Module models unless noted. • Changed SSL references to TLS. • Removed WAPI security. • Removed UART as host interface. • Editorial updates.
Product Features	• Removed WAPI security. • Removed UART and I^2C as host interfaces. • Removed Bluetooth coexistance interface. • Replaced SSL with TLS. • Added 26 MHz crystal. • Removed: (4KB flash – less than 1KB RAM).
Order Information and Module Marking	• Revised Ordering table. • Revised Marking information. Figure.
Block Diagram	• Revised Block Diagram figure.
Pin Description	• Revised Pin Description drawing. • Editorial updates.

Section	Changes
Electrical Specifications	• Revised VDDIO maximum voltage in table 4.1 and added max temperatures. • Revised table 4-2 to include Recommended operating temperature.
CPU and Memory Subsystems	• Editorial update.
WLAN Subsystem RADIO	• Added text regarding performance derating at cold temperature. • Features table revisions and changes: – Corrected the package height – Revised Storage temperature • Added performance test conditions to the performance tables. • Revised the Receive performance in table 6-2. • Revised the 802.11b mode Transmit performance numbers in table 6-3. • Revised Transmit performance Footnotes. • Changed max frequency to 2.472GHz. • Editorial updates.
External Interfaces	• Revised SPI timing information in table 7-3. • Removed Bluetooth Coexistance section. • Removed SDIO. • Editorial updates.
Power Consumption	• Added Module Reset section for reset duration. • Editorial updates.
ATWINC15x0-MR210PB Placement and Routing Guidelines	• Added text for antenna types used in test and an associated table. • Revised Co-Ax connector type.
Schematic Design Information	• Removed SDIO schematic. • Editorial updates.
Module Drawings	• Updated module drawing figures and figure titles. • Added section with footprint drawing.
Design Considerations	• Added sections for Module design and assembly considerations, and module PCB placement.
Reflow Profile Information	• Revised reflow profile picture to be clearer.

Section	Changes
	• Editorial updates.
Certification Notices	• Added section for Agency Certification notices (now under Regulatory Approvals with Rev. B).
Agency Regulatory Approvals	• Added back Agency Approval section. • Revised content of certifications.
Reference Documents	• Moved Design File Package to a separate paragraph below the table to remove web availability aspect and to contact sales.

Rev B - 02/2016

Document	• Updated copyright date to 2016. • Updated footers.
Module Outline Drawing	• Revised Module outline drawings to show Ground pad to be soldered. • Pulled out Footprint drawing as this is covered in the Module drawing.
WLAN Subsystem Radio	• Revised Transmit Performance Table 6-3.
Power Consumption	• Revised current table references in Table 8-1.
Schematic Design Information	• Updated Schematics Section 11 text and figures Figure 11-1 and Figure 11-2.
Reflow Profile Information	• Revised section 12 Reflow Profile Information.
Reference Documents	• Updated Document Reference table to include the ATWINC1500-MU datasheet.

Rev A - 07/2015

Document	Updated due to changes in the ATWINC1500 from Rev A to Rev B.
Description	• Updated model revisions to rev B. • Corrected Package dimensions.
Features	• Added Hardware Accelerator content to features list.
Pinout Information	• Updated reference schematic.

	• New pin list adds GPIO's 3,4,5 and 6.
CPU and Memory Subsystems	• Increased Memory from 182KB to 160KB.
External Interfaces	• Improved and corrected description of Coexistence interface. • Editorial updates.
Power Consumption	• Updated power numbers and description, added high-power and low-power modes.
WLAN Subsystem Radio	• Updated Performance numbers.

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