
PIC18-Q41 Family Programming Specification

Introduction

This programming specification describes a SPI-based programming method for the PIC18-Q41 family of microcontrollers. [Programming Algorithms](#) describes the programming commands, programming algorithms and electrical specifications used in that particular programming method. [Appendix B](#) contains individual part numbers, device identification values, pinout and packaging information, and Configuration Bytes.

**Important:**

- This is a SPI-compliant programming method with 8-bit commands.
- The low-voltage entry code is now 32 clocks and MSb first, unlike earlier PIC18 devices, which had 33 clocks and LSb first.

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1. Overview

1.1 Programming Data Flow

Nonvolatile Memory (NVM) programming data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage In-Circuit Serial Programming (ICSP) interface. Data can be programmed into the Program Flash Memory (PFM), Data EEPROM Memory, dedicated “User ID” locations and the Configuration Bytes.

1.2 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in the table below. For pin locations and packaging information, refer to the table in [Appendix B](#).

Table 1-1. PIN DESCRIPTIONS DURING PROGRAMMING

Pin Name	During Programming		
	Function	Pin Type	Pin Description
ISCPCLK	ICSPCLK	I	Clock Input – Schmitt Trigger Input
ISCPDAT	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
MCLR/V _{PP}	Program/Verify mode	I ⁽¹⁾	Program Mode Select
V _{DD}	V _{DD}	P	Power Supply
V _{SS}	V _{SS}	P	Ground
Legend: I = Input, O = Output, P = Power Note: <ol style="list-style-type: none"> The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to the MCLR input. Since the MCLR is used for a level source, MCLR does not draw any significant current. 			

1.3 Hardware Requirements

1.3.1 High-Voltage ICSP Programming

In High-Voltage ICSP mode, the device requires two programmable power supplies: one for V_{DD} and one for the MCLR/V_{PP} pin.

1.3.2 Low-Voltage ICSP Programming

In Low-Voltage ICSP mode, the device can be programmed using a single V_{DD} source in the device operating range. The MCLR/V_{PP} pin does not have to be brought to programming voltage, but can instead be left at the normal operating voltage.

1.3.2.1 Single-Supply ICSP Programming

The device's LVP Configuration bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled). The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the MCLR/V_{PP} pin is raised to V_{IHH}. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and can be used to program the device.



Important:

- The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IH} to the \overline{MCLR}/V_{PP} pin.
- While in Low-Voltage ICSP mode, \overline{MCLR} is always enabled, regardless of the MCLRE bit. Also, the \overline{MCLR} pin can no longer be used as a general purpose input.

1.4 Write and/or Erase Section

Erasing or writing is selected according to the command used to begin operation (see [Table 3-1](#)). The terminologies used in this document, related to erasing/writing to the program memory, are defined in the table below.

Table 1-2. PROGRAMMING TERMS

Term	Definition
Programmed Cell	A memory cell at logic '0'
Erased Cell	A memory cell at logic '1'
Erase	Change memory cell from a '0' to a '1'
Write	Change memory cell from a '1' to a '0'
Program	Generic erase and/or write

1.4.1 Erasing Memory

Memory is erased by 128-word pages or in bulk, where 'bulk' includes many subsets of the total memory space. The duration of the data memory erase is determined by the size of data memory. All Bulk ICSP Erase commands have minimum V_{DD} requirements, which are higher than the Page Erase and Write requirements.

Page erasing pertains to PFM and User ID memory only. Configuration and data memory should be erased by the Bulk Erase command. For self-write operations, each byte write to data memory includes an automatic erase cycle for the location about to be programmed.

1.4.2 Writing Memory

Memory is written one word at a time. The duration of the write is determined internally.

Note: The size of the word is 16 bits for the Program Flash Memory and is 8 bits for the EEPROM, but the same 24-bit payload is used for both memory regions.

2. Memory Map

This section provides details about how the program memory and EEPROM are organized for this device.

Figure 2-1. Program and Data EEPROM Memory Map

Rev. 02-08
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Address	Device		
	PIC18Fx4Q41	PIC18Fx5Q41	PIC18Fx6Q41
00 0000h to 00 3FFFh	Program Flash Memory (8KW) ⁽¹⁾	Program Flash Memory (16 KW) ⁽¹⁾	Program Flash Memory (32 KW) ⁽¹⁾
00 4000h to 00 7FFFh	Not Present ⁽²⁾		
00 8000h to 00 FFFFh			
01 0000h to 01 FFFFh		Not Present ⁽²⁾	
02 0000h to 1F FFFFh			
20 0000h to 20 003Fh	User IDs (32 Words) ⁽³⁾		
20 0040h to 2B FFFFh	Reserved		
2C 0000h to 2C 00FFh	Device Information Area (DIA) ^(3,5)		
2C 0100h to 2F FFFFh	Reserved		
30 0000h to 30 0009h	Configuration Bytes ⁽³⁾		
30 000Ah to 37 FFFFh	Reserved		
38 0000h to 38 01FFh	Data EEPROM (512 Bytes)		
38 0200h to 3B FFFFh	Reserved		
3C 0000h to 3C 0009h	Device Configuration Information ^(3,4,5)		
3C 000Ah to 3F FFFBh	Reserved		
3F FFFCh to 3F FFFDh	Revision ID (1 Word) ^(3,4,5)		
3F FFFEh to 3F FFFFh	Device ID (1 Word) ^(3,4,5)		

Note 1: Storage Area Flash is implemented as the last 128 Words of User Flash, if enabled.

2: The addresses do not roll over. The region is read as '0'.

3: Not code-protected.

4: Hard-coded in silicon.

5: This region cannot be written by the user and it's not affected by a Bulk Erase.

2.1 User ID Location

A user may store identification information (User ID) in 32 designated locations. The User ID locations are mapped to 20 0000h-20 003Fh. Each location is 16 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

2.2 Device/Revision ID

The 16-bit Device ID Word is located at 3F FFFEh and the 16-bit Revision ID is located at 3F FFFCh. These locations are read-only and cannot be erased or modified. See [DEVICE ID](#) and [REVISION ID](#) registers for more details.

2.3 Device Configuration Information (DCI)

The Device Configuration Information (DCI) is a dedicated region in the memory that holds information about the device which is useful for programming and bootloader applications. The data stored in this region are read-only and cannot be modified/erased. Refer to the table below for complete DCI table addresses and description.

Table 2-1. DEVICE CONFIGURATION INFORMATION

Address	Name	Description	Value			Units
			PIC18F04/14Q41	PIC18F05/15Q41	PIC18F06/16Q41	
3C 0000h	ERSIZ	Erase Page Size	128			Words
3C 0002h	WLSIZ	Number of write latches per row	0			Words
3C 0004h	URSZ	Number of user erasable pages	128	256	512	Pages
3C 0006h	EESIZ	Data EEPROM memory size	512			Bytes
3C 0008h	PCNT	Pin Count	14/20	14/20	14/20	Pins

2.4 Configuration Bytes

The devices have ten Configuration Bytes, starting at address, 30 0000h. Configuration bits enable or disable specific features, placing these controls outside the normal software process, and they establish configured values prior to the execution of any software.

In terms of programming, these important Configuration bits should be considered:

1. LVP: Low-Voltage Programming Enable bit

- 1 = ON: Low-Voltage Programming is enabled. $\overline{\text{MCLR}}/\text{V}_{\text{PP}}$ pin function is $\overline{\text{MCLR}}$. MCLRE Configuration bit is ignored.
- 0 = OFF: High voltage on $\overline{\text{MCLR}}/\text{V}_{\text{PP}}$ must be used for programming.

It is important to note that the LVP bit cannot be written (to '0') while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state. For more information, refer to the [Low-Voltage Programming \(LVP\) Mode](#) section.

2. MCLRE: Master Clear ($\overline{\text{MCLR}}$) Enable bit

- If LVP = 1: RA3 pin function is $\overline{\text{MCLR}}$
- If LVP = 0
 - 1 = RA3 pin is $\overline{\text{MCLR}}$

- 0 = RA3 pin function is a port-defined function
3. **$\overline{\text{CP}}$: User NVM Program Memory Code Protection bit**
- 1 = OFF: User NVM code protection is disabled
 - 0 = ON: User NVM code protection is enabled

For more information on code protection, see [Code Protection](#).

2.5 Device ID

Name: DEVICEID
Address: 3F FFEh

Device ID Register

Bit	15	14	13	12	11	10	9	8
	DEV[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q
Bit	7	6	5	4	3	2	1	0
	DEV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bits 15:0 – DEV[15:0] Device ID

Device	Device ID
PIC18F04Q41	7540h
PIC18F05Q41	7500h
PIC18F06Q41	7580h
PIC18F14Q41	7520h
PIC18F15Q41	74E0h
PIC18F16Q41	7560h

2.6 Revision ID

Name: REVISIONID
Address: 3F FFFCh

Revision ID Register

Bit	15	14	13	12	11	10	9	8
	1010[3:0]				MJRREV[5:2]			
Access	R	R	R	R	RO	RO	RO	RO
Reset	1	0	1	0	q	q	q	q
Bit	7	6	5	4	3	2	1	0
	MJRREV[1:0]		MNRREV[5:0]					
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	q	q	q	q	q	q	q	q

Bits 15:12 – 1010[3:0] Read as 'b1010

These bits are fixed with value 'b1010 for all devices in this family.

Bits 11:6 – MJRREV[5:0] Major Revision ID

These bits are used to identify a major revision. (A0, B0, C0, etc.).

Revision A = 'b00 0000

Bits 5:0 – MNRREV[5:0] Minor Revision ID

These bits are used to identify a minor revision.

Revision A0 = 'b00 0000

3. Programming Algorithms

3.1 Program/Verify Mode

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted MSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK pins are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state, all I/Os are automatically configured as high-impedance inputs and the Program Counter (PC) is cleared.

3.1.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different modes of entering Program/Verify mode via high voltage:

- V_{PP}-First Entry mode
- V_{DD}-First Entry mode

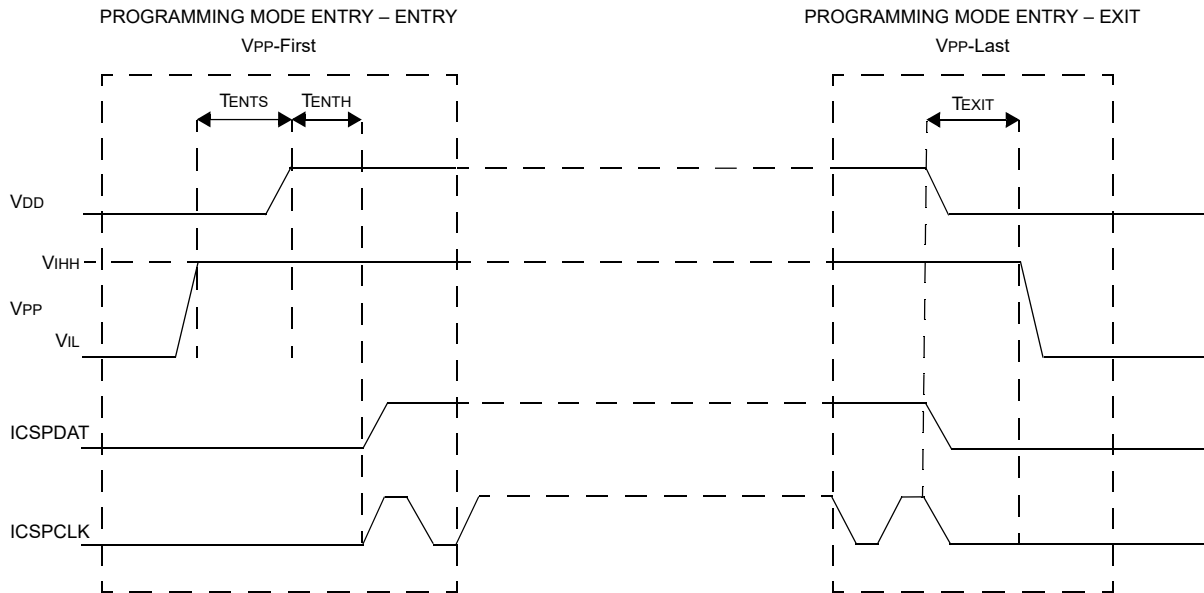
3.1.1.1 V_{PP}-First Entry Mode

To enter Program/Verify mode via the V_{PP}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to V_{IHH}.
3. Raise the voltage on V_{DD} from 0V to the desired operating voltage.

The V_{PP}-First Entry mode prevents the device from executing code prior to entering Program/Verify mode. For example, when the Configuration Byte has already been programmed to have $\overline{\text{MCLR}}$ disabled (MCLRE = 0), the Power-up Timer disabled ($\overline{\text{PWRTE}}$ = 0) and the internal oscillator selected, the device will execute code immediately. V_{PP}-First Entry mode is strongly recommended as it prevents user code from executing. See the timing diagram in [Figure 3-1](#).

Figure 3-1. Programming Entry and Exit Modes – V_{PP}-First and Last



3.1.1.2 V_{DD}-First Entry Mode

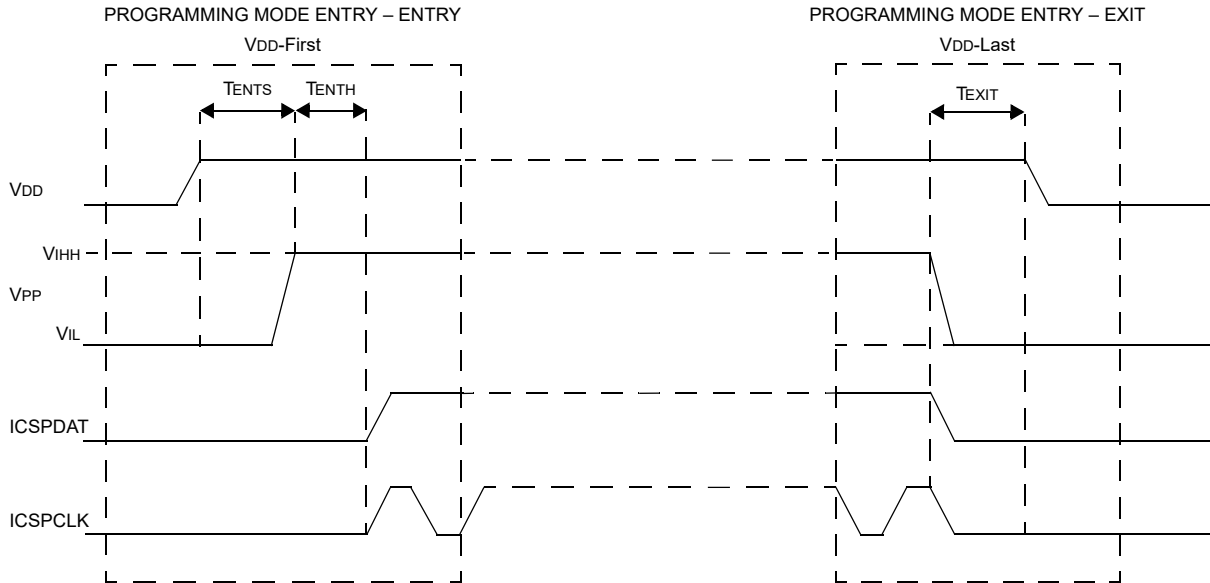
To enter Program/Verify mode via the V_{DD}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.

2. Raise the voltage on V_{DD} from 0V to the desired operating voltage.
3. Raise the voltage on \overline{MCLR} from V_{DD} or below to V_{IH} .

The V_{DD} -First Entry mode is useful for programming the device when V_{DD} is already applied, for it is not necessary to disconnect V_{DD} to enter Program/Verify mode. See the timing diagram in [Figure 3-2](#).

Figure 3-2. Programming Entry and Exit Modes – V_{DD} -First and Last



3.1.1.3 Program/Verify Mode Exit

To exit Program/Verify mode, lower \overline{MCLR} from V_{IH} to V_{IL} . V_{PP} -First Entry mode should use V_{PP} -Last Exit mode (see [Figure 3-1](#)). V_{DD} -First Entry mode should use V_{DD} -Last Exit mode (see [Figure 3-2](#)).

3.1.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the devices to be programmed using V_{DD} only, without high voltage. When the LVP bit in the Configuration Byte register is set to '1', the Low-Voltage ICSP Programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. \overline{MCLR} is brought to V_{IL} .
2. A **32-bit key sequence** is presented on $ICSPDAT$, clocked by $ICSPCLK$. The LSB of the pattern is a "don't care x". The Program/Verify mode entry pattern detect hardware verifies only the first 31 bits of the sequence and the last clock is required before the pattern detect goes active.

The key sequence is a specific 32-bit pattern, '32'h4d434850' (more easily remembered as **MCHP** in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the Most Significant Byte must be shifted in first. Once the key sequence is complete, \overline{MCLR} must be held at V_{IL} for as long as Program/Verify mode is to be maintained. For Low-Voltage Programming timing, see [Figure 3-3](#) and [Figure 3-4](#).

Figure 3-3. LVP Entry (Powering Up)

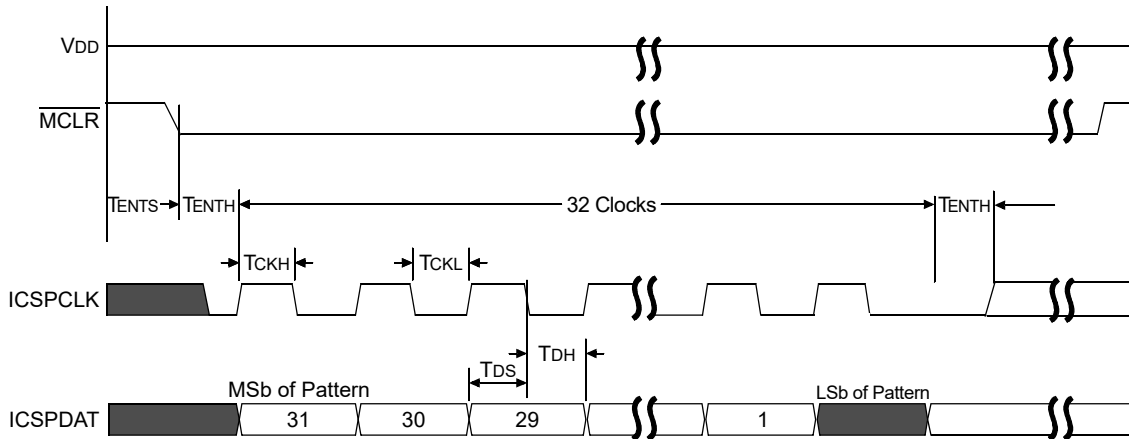
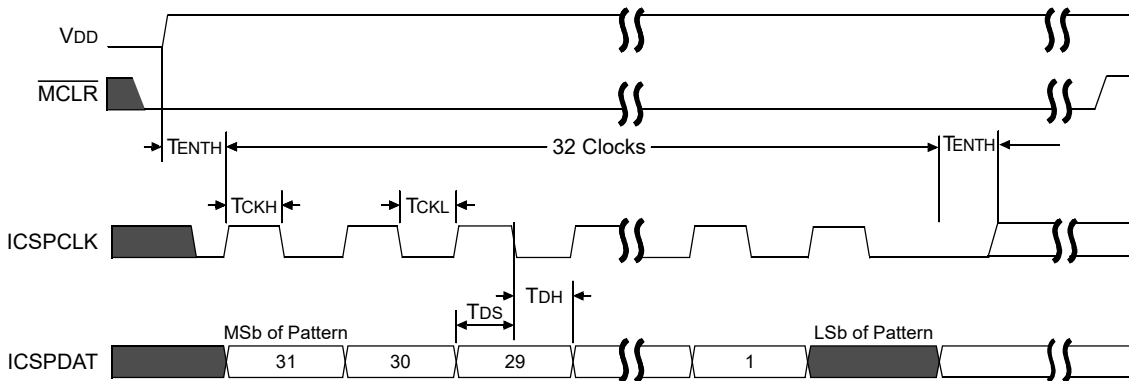


Figure 3-4. LVP Entry (Powered)



Exiting Program/Verify mode is done by raising $\overline{\text{MCLR}}$ from below V_{IL} to V_{IH} level (or higher, up to V_{DD}).



Important:

To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

3.1.3 Program/Verify Commands

Once a device has entered ICSP Program/Verify mode (using either high-voltage or LVP entry), the programming host device may issue six commands to the microcontroller, each eight bits in length. The commands are summarized in [Table 3-1](#). The commands are used to erase or program the device based on the location of the Program Counter (PC).

Some of the 8-bit commands also have an associated data payload (such as Load PC Address and Read Data from NVM).

If the host device issues an 8-bit command byte that has an associated data payload, the host device is responsible for sending an additional 24 clock pulses (for example, three 8-bit bytes) in order to send or receive the payload data associated with the command.

The payload field size is used so as to be compatible with many 8-bit SPI-based systems. Within each 24-bit payload field, the first bit transmitted is always a Start bit, followed by a variable number of Pad bits, followed by the useful data payload bits and ending with one Stop bit. The useful data payload bits are always transmitted, Most Significant bit (MSb) first.

When the programming device issues a command that involves a host to microcontroller payload (for example, Load PC Address), the Start, Stop and Pad bits should all be driven by the programmer to '0'. When the programming host device issues a command that involves microcontroller to host payload data (for example, Read Data from NVM), the Start, Stop and Pad bits should be treated as "don't care" bits and the values should be ignored by the host.

When the programming host device issues an 8-bit command byte to the microcontroller, the host should wait a specified minimum amount of delay (which is command-specific) prior to sending any additional clock pulses (associated with either a 24-bit data payload field or the next command byte).

Table 3-1. ICSP™ Command Set Summary⁽¹⁾

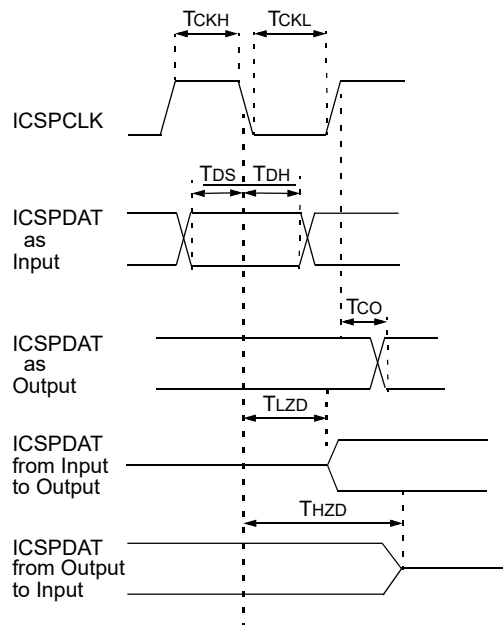
Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb ... LSb)	Hex			
Load PC Address	1000 0000	80	Yes	T _{DLY}	Payload Value = PC
Bulk Erase	0001 1000	18	Yes	T _{ERAB}	The payload carries the information of the regions that need to be bulk erased.
Page Erase Program Memory	1111 0000	F0	No	T _{ERAS}	The page addressed by the MSbs of the PC is erased; LSbs are ignored
Read Data from NVM	1111 11J0	FC/FE	Yes	T _{DLY}	Data output '0' if code-protect is enabled: J = 0: PC is unchanged; J = 1: PC = PC + n ⁽²⁾ after reading
Increment Address	1111 1000	F8	No	T _{DLY}	PC = PC + n ⁽²⁾
Program Data	11J0 0000	C0/E0	Yes	T _{PROG}	Payload value = Data Word; J = 0: PC is unchanged; J = 1: PC = PC + n after writing



Important:

1. All clock pulses for both the 8-bit commands and the 24-bit payload fields are generated by the host programming device. The microcontroller does not drive the ICSPCLK line. The ICSPDAT signal is a bidirectional data line. For all commands and payload fields, except the Read Data from NVM payload, the host programming device continuously drives the ICSPDAT line. Both the host programmer device and the microcontroller should latch received ICSPDAT values on the falling edge of the ICSPCLK line. When the microcontroller receives ICSPDAT line values from the host programmer, the ICSPDAT values must be valid a minimum of T_{DS} before the falling edges of ICSPCLK and should remain valid for a minimum of T_{DH} after the falling edge of ICSPDAT. See [Figure 3-5](#).
2. PC is incremented by $n = 1$ for data memory, Configuration Bytes and $n = 2$ for all other regions.

Figure 3-5. Clock and Data Timing



3.1.3.1 Program Data

The Program Data command is used to program one NVM word (for example, one 16-bit instruction word for program memory/User ID memory or one 8-bit data for a Data EEPROM Memory address). The payload data are written into program or EEPROM memory immediately after the Programming Data command is issued (see [Programming Algorithms](#)). Depending on the value of bit 5 of the command, the PC may or may not be incremented (see [Table 3-1](#)).

Figure 3-6. Program Data (Program Memory and User IDs)

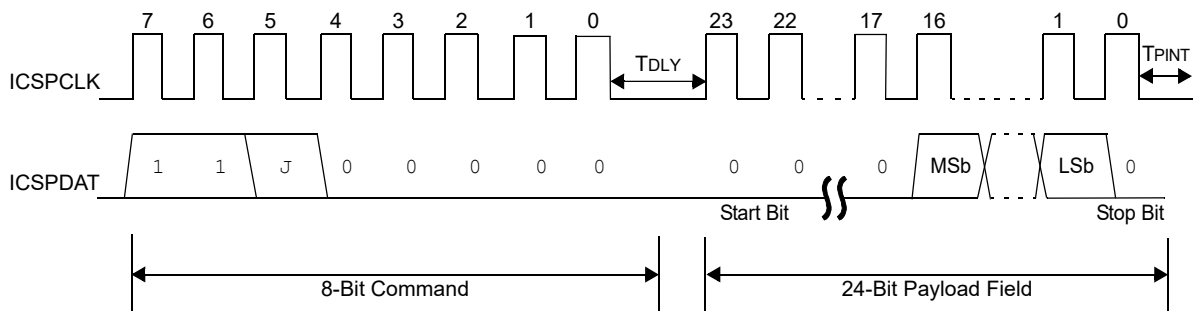
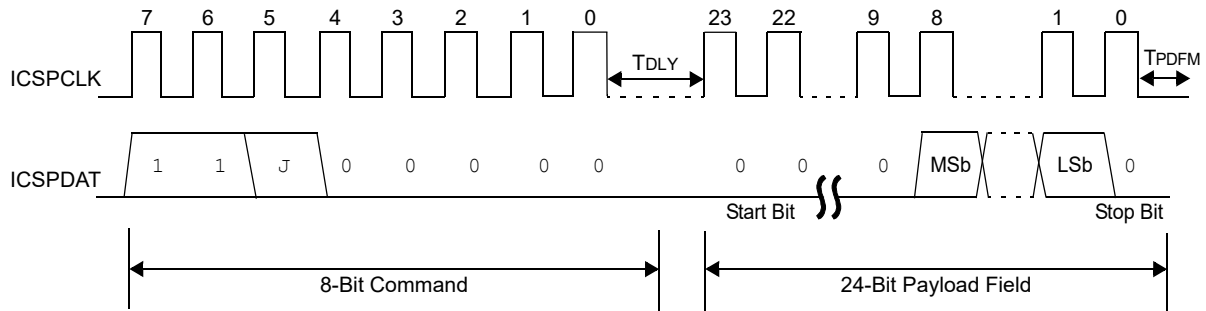


Figure 3-7. Program Data (DATA EEPROM and Configuration Bytes)



3.1.3.2 Read Data from NVM

The Read Data from the NVM command will transmit data bits out of the current PC address. The ICSPDAT pin will go into Output mode on the first falling edge of the ICSP data payload clock and it will revert to Input mode (high-impedance) after the 24th falling edge of the ICSP data payload clock. The Start and Stop bits are only one-half of a bit time wide; therefore, they should be ignored by the host programmer device, since the latched value may be indeterminate. Additionally, the host programmer device should only consider the MSb to LSb payload bits as valid and should ignore the values of the Pad bits. If the memory region is code-protected (CP or DP), the data will be read as zeros (see Figure 3-8 and Figure 3-9). Depending on the value of bit 1 of the command, the PC may or may not be incremented (see Table 3-1). The Read Data from the NVM command can be used to read data for Program Flash Memory (see Figure 3-8) or the Data EEPROM Memory (see Figure 3-9).

Figure 3-8. Read Data from NVM (PFM and User IDs)

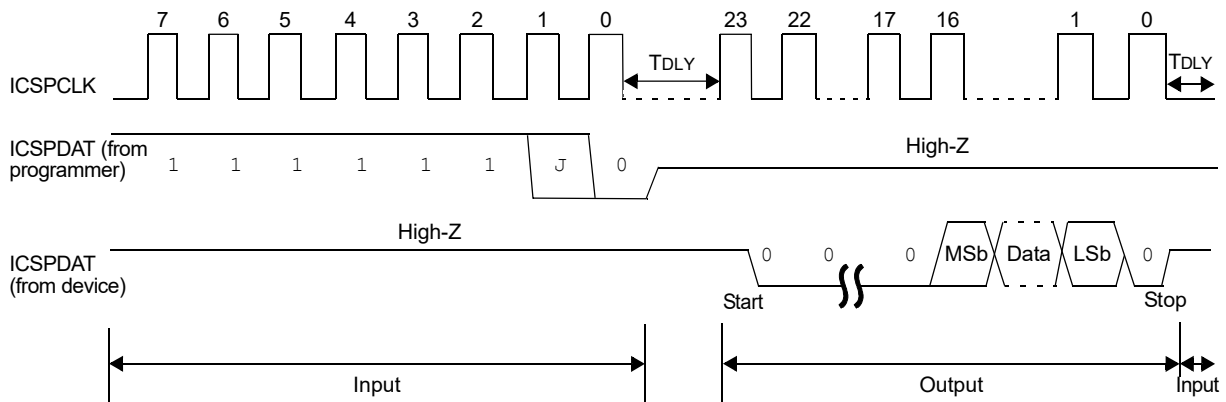
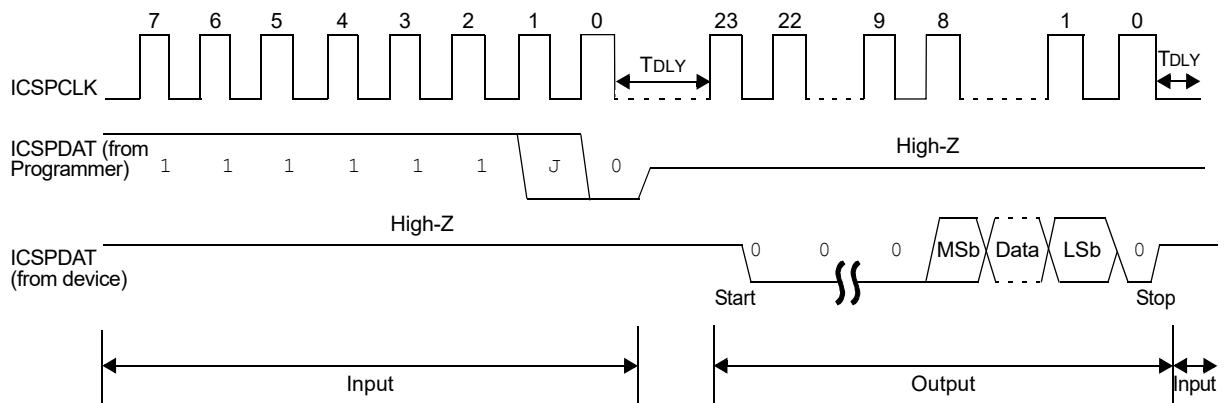


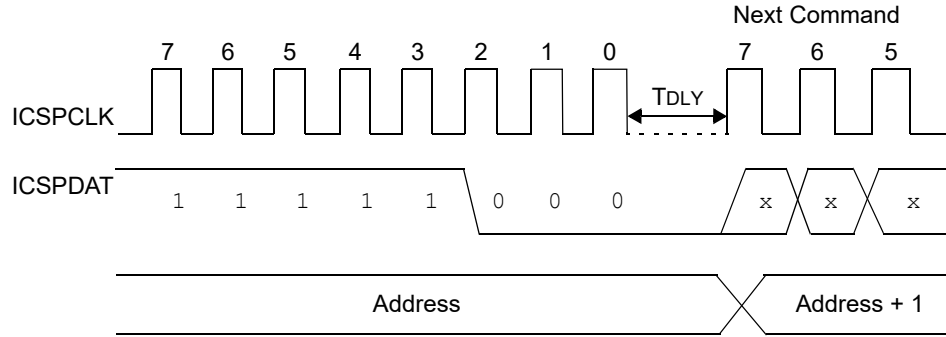
Figure 3-9. Read Data from NVM (DATA EEPROM and Configuration Bytes)



3.1.3.3 Increment Address

The address is incremented when this command is received. Depending on the current value of the Program Counter, the increment varies. If the PC points to PFM, then the PC is incremented by 2; if the PC points to the Data EEPROM or Configuration Space, then it is incremented by 1. It is not possible to decrement the address. To reset the Program Counter, the user must use the Load PC Address command.

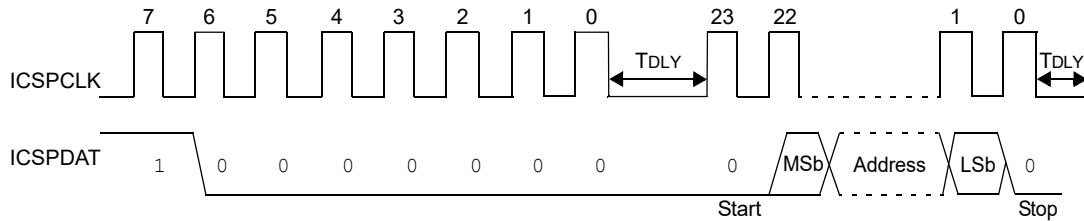
Figure 3-10. Increment Address



3.1.3.4 Load PC Address

The PC value is set using the supplied data. The address indicates the memory location (PFM or Data EEPROM Memory or Configuration memory) to be accessed (see [Figure 3-11](#)).

Figure 3-11. Load PC Address



3.1.3.5 Bulk Erase

The Bulk Erase command is used to completely erase different memory regions. The area selection is a bit field in the payload.

By setting the following bits of the payload, the corresponding memory regions can be bulk erased. Setting multiple bits is valid.

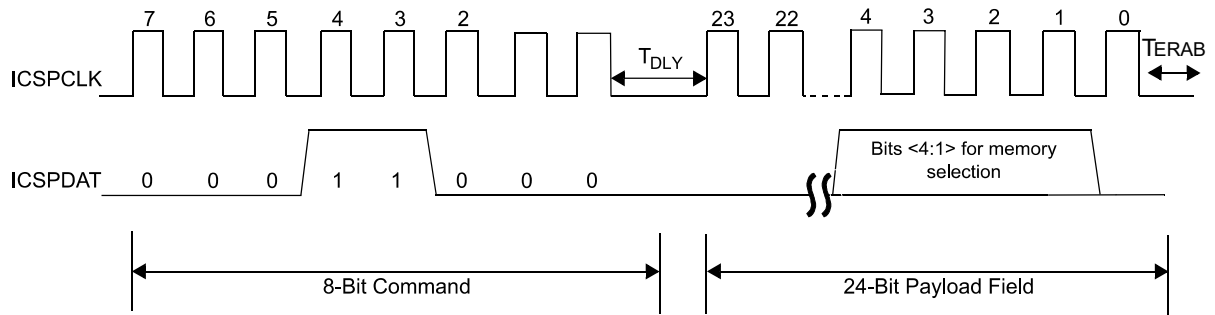
1. Bit 1: Data EEPROM
2. Bit 2: Flash memory
3. Bit 3: User ID memory
4. Bit 4: Configuration memory



Important: If the device is code-protected and a Bulk Erase command for the configuration memory is issued, all other regions are also bulk erased.

After receiving the Bulk Erase command, the erase will complete after the time interval, T_{ERAB} . See [Figure 3-12](#) for Bulk Erase command structure.

Figure 3-12. Bulk Erase Memory

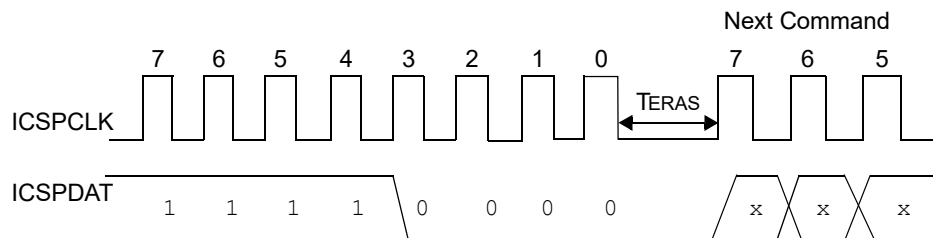


3.1.3.6 Page Erase Program Memory

The Page Erase Program Memory command will erase an individual page based on the current address of the Program Counter. If the program memory is code-protected, the Page Erase Memory command will be ignored. The Bulk Erase command must be used to erase code-protected memory.

The Flash memory page defined by the current PC will be erased. The user must wait T_{ERAS} for erasing to be complete (see Figure 3-13). Page Erase may be used for program memory and User ID regions only. Configuration and data regions must be erased with the Bulk Erase method.

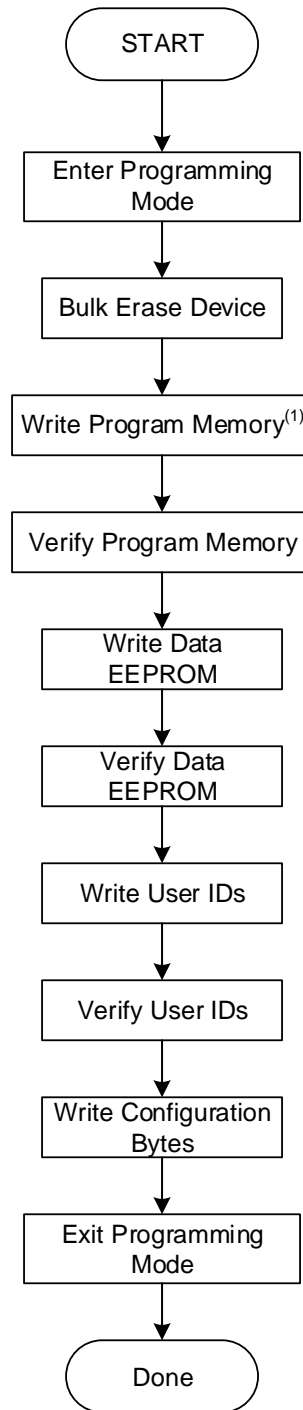
Figure 3-13. Page Erase Memory



3.2 Programming Algorithms

The Program Flash Memory and User ID are programmed one word at a time. The EEPROM memory and Configuration regions are programmed one byte at a time.

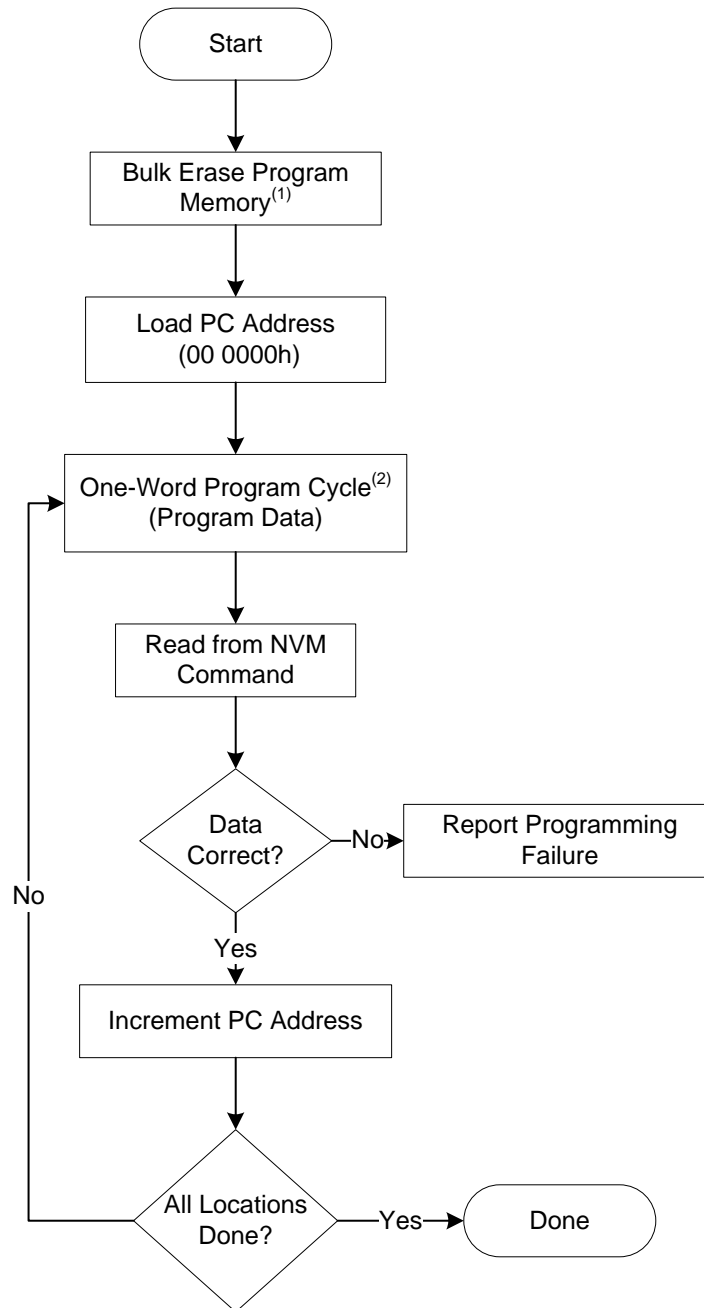
Figure 3-14. Device Program/Verify Flowchart



Note:

1. See [Figure 3-15](#).
2. See [Figure 3-17](#).

Figure 3-15. Program Memory Flowchart



Note:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. If the device is code-protected or must be completely erased, then Bulk Erase the device per [Figure 3-18](#).

Figure 3-16. One-Word Program Cycle

Program Cycle
(For programming Data, EEPROM, User ID and Configuration Bytes)

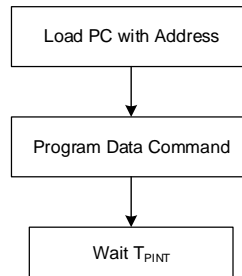
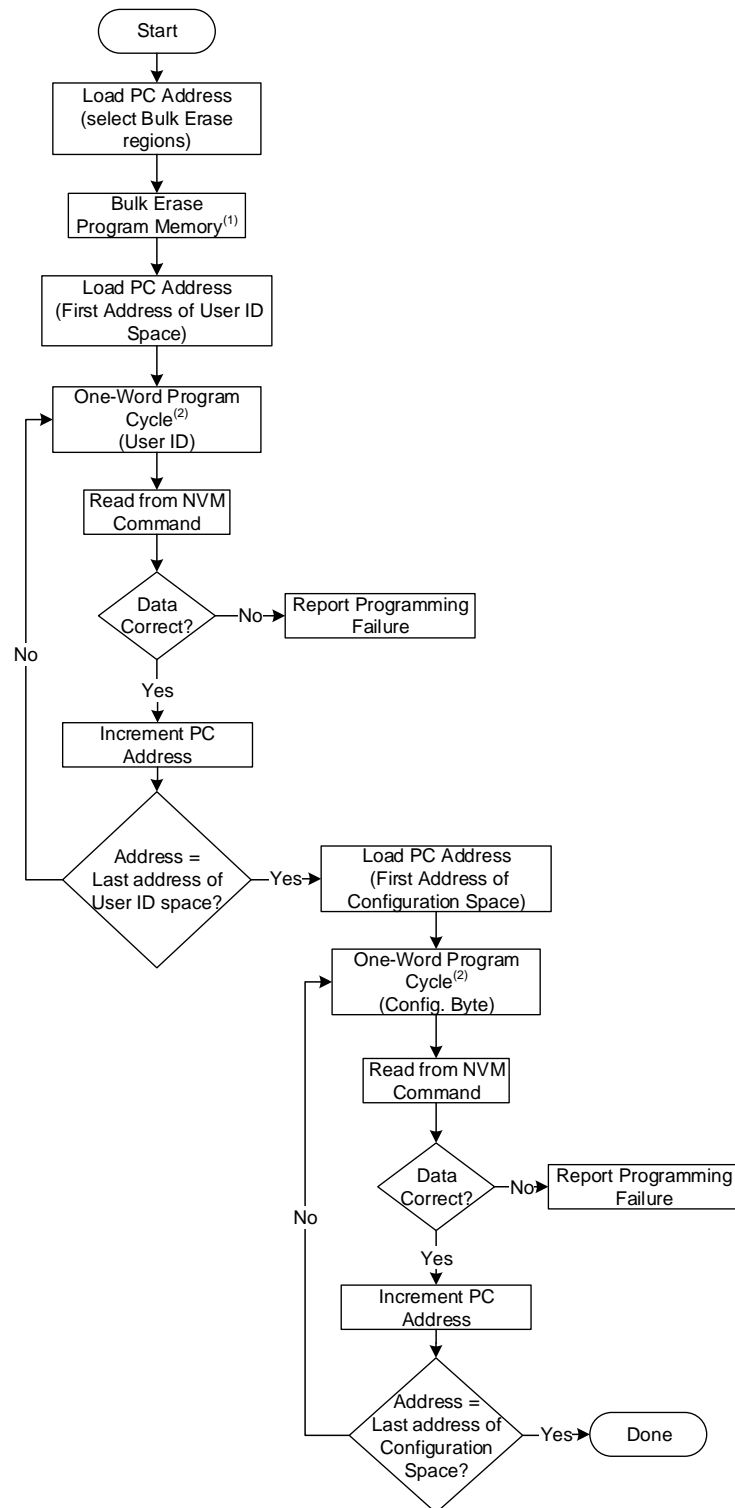


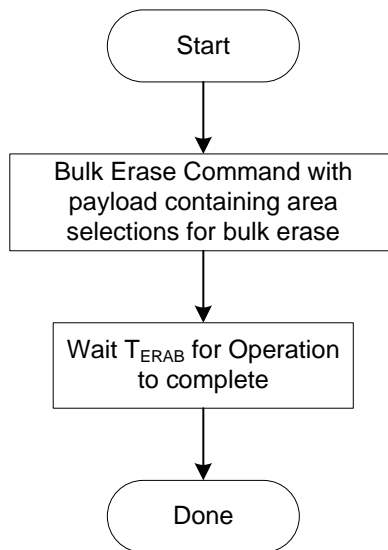
Figure 3-17. User ID and Configuration Memory Program Flowchart



Note:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. See [Figure 3-16](#).

Figure 3-18. Bulk Erase Flowchart



3.3 Code Protection

Code protection is controlled using the \overline{CP} bit. When code protection is enabled, all program memory and Data EEPROM locations read as '0'. Further programming is disabled for the program memory and Data EEPROM until a Bulk Erase operation is performed on the configuration memory region. Program memory and Data EEPROM can still be programmed and read during program execution.

The User ID locations and Configuration Bytes can be programmed and read out regardless of the code protection settings.

The only way to disable code protection is to use the Bulk Erase Program Memory command with bit 4 of the payload set to '1'. This will clear the disable code protection and also erase all the memory locations.

3.4 Hex File Usage

3.4.1 Embedding Configuration Information in the Hex File

To allow portability of code, a programmer is required to read the Configuration Byte locations from the Hex file. If Configuration Byte information is not present in the Hex file, then a simple warning message should be issued. Similarly, when saving a Hex file, all Configuration Byte information should be included. An option to not include the Configuration Byte information may be provided. When embedding Configuration Byte information in the Hex file, it should start at address 30 0000h.



Important:

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

3.4.2 Embedding Data EEPROM Information in the Hex File

To allow portability of code, a programmer is required to read the Data EEPROM information from the Hex file. If Data EEPROM information is not present, a simple warning message should be issued. Similarly, when saving a Hex file, all Data EEPROM information must be included. An option to not include the Data EEPROM information may be provided. When embedding Data EEPROM information in the Hex file, it should start at address 38 0000h.



Important:

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

3.5 CRC Checksum Computation

Unlike older PIC[®] devices, the Microchip toolchain runs a 32-bit CRC calculation on the entire Hex file to calculate its checksum. The checksum uses the standard CRC-32 algorithm with the polynomial 0x4C11DB7

$(x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1)$.

4. Electrical Specifications

Refer to the device-specific data sheet for absolute maximum ratings.

Table 4-1. AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at +25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
Programming Supply Voltages and Currents						
V _{DD}	Supply Voltage (V _{DDMIN} , V _{DDMAX})	1.80	—	5.50	V	(Note 1)
V _{PEW}	Read/Write and Page Erase Operations	V _{DDMIN}	—	V _{DDMAX}	V	
V _{BE}	Bulk Erase Operations	V _{BORMAX}	—	V _{DDMAX}	V	(Note 2)
I _{DDI}	Current on V _{DD} , Idle	—	—	1.0	mA	
I _{DDP}	Current on V _{DD} , Programming	—	—	10	mA	
V_{PP}						
I _{PP}	Current on MCLR/V _{PP}	—	—	600	μA	
V _{IHH}	High Voltage on MCLR/V _{PP} for Program/Verify Mode Entry	7.9	—	9.0	V	
T _{VHHR}	MCLR Rise Time (V _{IL} to V _{IHH}) for Program/Verify Mode Entry	—	—	1.0	μs	
I/O Pins						
V _{IH}	(ICSPCLK, ICSPDAT, MCLR/V _{PP}) Input High Level	0.8 V _{DD}	—	V _{DD}	V	
V _{IL}	(ICSPCLK, ICSPDAT, MCLR/V _{PP}) Input Low Level	V _{SS}	—	0.2 V _{DD}	V	
V _{OH}	ICSPDAT Output High Level	V _{DD} -0.7	—	—	V	I _{OH} = 3 mA, V _{DD} = 3.0V
V _{OL}	ICSPDAT Output Low Level	—	—	V _{SS} + 0.6	V	I _{OL} = 6 mA, V _{DD} = 3.0V
Programming Mode Entry and Exit						
T _{ENTS}	Programing Mode Entry Setup Time: ICSPCLK, ICSPDAT Setup Time before V _{DD} or MCLR↑	100	—	—	ns	
T _{ENTH}	Programing Mode Entry Hold Time: ICSPCLK, ICSPDAT Hold Time before V _{DD} or MCLR↑	1	—	—	ms	
Serial Program/Verify						
T _{CKL}	Clock Low Pulse Width	100	—	—	ns	
T _{CKH}	Clock High Pulse Width	100	—	—	ns	
T _{DS}	Data in Setup Time before Clock↓	100	—	—	ns	
T _{DH}	Data in Hold Time after Clock↓	100	—	—	ns	
T _{CO}	Clock↑ to Data Out Valid (during a Read Data command)	0	—	80	ns	
T _{LZD}	Clock↓ to Data Low-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T _{HZD}	Clock↓ to Data High-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T _{DLY}	Data Input not Driven to Next Clock Input (delay required between command/data or command/command)	1.0	—	—	μs	
T _{ERAB}	Bulk Erase Cycle Time	—	—	11	ms	Program, Config and ID
T _{ERAS}	Page Erase Cycle Time	—	—	11	ms	
T _{PDFM}	Internally Timed DFM (EEPROM) Programming Operation Time	—	—	11	ms	EEPROM Memory and Configuration Bytes
T _{PINT}	Internally Timed Programming Operation Time	—	—	75	μs	Program Memory and Configuration Bytes

.....continued

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at +25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
T _{EXIT}	Time Delay when Exiting Program/Verify Mode	1	—	—	μs	

Note:

1. Bulk erased devices default to Brown-out Reset enabled with BORV = 11 (low trip point). V_{DDMIN} is the V_{BOR} threshold (with BORV = 1) when performing Low-Voltage Programming on a bulk erased device to ensure that the device is not held in Brown-out Reset.
2. The hardware requires V_{DD} to be above the BOR threshold, at the ~1.9V nominal setting, in order to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bits settings. Refer to the microcontroller device data sheet specifications for min./typ./max. limits of the V_{BOR} level.

5. APPENDIX A: Revision History

Doc Rev.	Date	Comments
C	03/2020	Updated Table 6-1 package code information.
B	10/2019	Updated Table 4-1 - T_{PINT} from 50 μ s to 75 μ s.
A	09/2019	Initial document release.

6. APPENDIX B

This section provides information about the Device IDs and Pinout Descriptions

Table 6-1. Programming Pin Locations By Package Type

Device	Package	Package Code	V _{DD}	V _{SS}	MCLR		ICSPCLK		ICSPDAT	
			PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC18F04Q41 PIC18F05Q41 PIC18F06Q41	14-Pin SOIC	SL	1	14	4	RA3	12	RA1	13	RA0
	14-Pin TSSOP	ST	1	14	4	RA3	12	RA1	13	RA0
PIC18F14Q41 PIC18F15Q41 PIC18F16Q41	20-Pin PDIP	P	1	20	4	RA3	18	RA1	19	RA0
	20-Pin SOIC	SO	1	20	4	RA3	18	RA1	19	RA0
	20-Pin SSOP	SS	1	20	4	RA3	18	RA1	19	RA0
	20-Pin VQFN	REB	18	17	1	RA3	15	RA1	16	RA0

Note:

The most current package drawings are located in the Microchip Packaging Specification, DS00000049 (<http://www.microchip.com/packaging>). The drawing numbers listed above do not include the current revision designator, which is added at the end of the number.

6.1 CONFIG1

Name: CONFIG1
Address: 30 0000h

Configuration Byte 1

Bit	7	6	5	4	3	2	1	0
		RSTOSC[2:0]				FEXTOSC[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	1	1		1	1	1

Bits 6:4 – RSTOSC[2:0] Power-up Default Value for COSC

This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

Value	Description
111	EXTOSC operating per FEXTOSC bits
110	HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1. Resets COSC/NOSC to b'110'.
101	LFINTOSC
100	SOSC
011	Reserved
010	EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
001	Reserved
000	HFINTOSC with HFFRQ = 64 MHz and CDIV = 1:1. Resets COSC/NOSC to b'110'.

Bits 2:0 – FEXTOSC[2:0] External Oscillator Mode Selection

Value	Description
111	ECH (external clock) above 8 MHz
110	ECM (external clock) for 500 kHz to 8 MHz
101	ECL (external clock) below 500 kHz
100	Oscillator not enabled
011	Reserved (do not use)
010	HS (crystal oscillator) above 4 MHz
001	XT (crystal oscillator) above 500 kHz, below 4 MHz
000	LP (crystal oscillator) optimized for 32.768 kHz

6.2 CONFIG2

Name: CONFIG2
Address: 30 0001h

Configuration Byte 2

Bit	7	6	5	4	3	2	1	0
	FCMENS	FCMENP	FCMEN		CSWEN		PR1WAY	CLKOUTEN
Access	R/W	R/W	R/W		R/W		R/W	R/W
Reset	1	1	1		1		1	1

Bit 7 – FCMENS Fail-Safe Clock Monitor Enable - Secondary XTAL Enable

Value	Description
1	Fail-Safe Clock Monitor enabled; timer will flag FSCMS bit and OSFIF interrupt on SOSC failure
0	Fail-Safe Clock Monitor disabled

Bit 6 – FCMENP Fail-Safe Clock Monitor Enable - Primary XTAL Enable

Value	Description
1	Fail-Safe Clock Monitor enabled; timer will flag FSCMP bit and OSFIF interrupt on EXTOSC failure
0	Fail-Safe Clock Monitor disabled

Bit 5 – FCMEN Fail-Safe Clock Monitor Enable

Value	Description
1	Fail-Safe Clock Monitor enabled
0	Fail-Safe Clock Monitor disabled

Bit 3 – CSWEN Clock Switch Enable

Value	Description
1	Writing to NOSC and NDIV is allowed
0	The NOSC and NDIV bits cannot be changed by user software

Bit 1 – PR1WAY PRLOCKED One-Way Set Enable

Value	Description
1	PRLOCKED bit can be cleared and set only once; Priority registers remain locked after one clear/set cycle
0	PRLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 0 – CLKOUTEN Clock Out Enable

If FEXTOSC = HS, XT, LP, then this bit is ignored.

Otherwise:

Value	Description
1	CLKOUT function is disabled; I/O function on OSC2
0	CLKOUT function is enabled; F _{OSC} /4 clock appears at OSC2

6.3 CONFIG3

Name: CONFIG3
Address: 30 0002h

Configuration Byte 3

Bit	7	6	5	4	3	2	1	0
	BOREN[1:0]		LPBOREN	IVT1WAY	MVECEN	PWRTS[1:0]		MCLRE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	1	1	1

Bits 7:6 – BOREN[1:0] Brown-out Reset Enable

When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit.

Value	Description
11	Brown-out Reset enabled, SBOREN bit is ignored
10	Brown-out Reset enabled while running, disabled in Sleep; SBOREN is ignored
01	Brown-out Reset enabled according to SBOREN
00	Brown-out Reset disabled

Bit 5 – LPBOREN Low-Power BOR Enable

Value	Description
1	Low-Power Brown-out Reset is disabled
0	Low-Power Brown-out Reset is enabled

Bit 4 – IVT1WAY IVTLOCK One-Way Set Enable

Value	Description
1	IVTLOCK bit can be cleared and set only once; IVT registers remain locked after one clear/set cycle
0	IVTLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 3 – MVECEN Multivector Enable

Value	Description
1	Multivector is enabled; vector table used for interrupts
0	Legacy interrupt behavior

Bits 2:1 – PWRTS[1:0] Power-up Timer Selection

Value	Description
11	PWRT is disabled
10	PWRT is set at 64 ms
01	PWRT is set at 16 ms
00	PWRT is set at 1 ms

Bit 0 – MCLRE Master Clear (\overline{MCLR}) Enable

Value	Condition	Description
x	If LVP = 1	RA3 pin function is MCLR
1	If LVP = 0	MCLR pin is MCLR
0	If LVP = 0	MCLR pin function is port defined function

6.4 CONFIG4

Name: CONFIG4
Address: 30 0003h

Configuration Byte 4

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{XINST}}$		LVP	STVREN	PPS1WAY	$\overline{\text{ZCD}}$	BORV[1:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	1		1	1	1	1	1	1

Bit 7 – $\overline{\text{XINST}}$ Extended Instruction Set Enable

Value	Description
1	Extended Instruction Set and Indexed Addressing mode disabled (Legacy mode)
0	Extended Instruction Set and Indexed Addressing mode enabled

Bit 5 – LVP Low-Voltage Programming Enable

The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state.

Value	Description
1	Low-Voltage Programming enabled. $\text{MCLR}/\text{V}_{\text{PP}}$ pin function is MCLR . MCLRE Configuration bit is ignored.
0	HV on $\text{MCLR}/\text{V}_{\text{PP}}$ must be used for programming

Bit 4 – STVREN Stack Overflow/Underflow Reset Enable

Value	Description
1	Stack Overflow or Underflow will cause a Reset
0	Stack Overflow or Underflow will not cause a Reset

Bit 3 – PPS1WAY PPSLOCKED One-Way Set Enable

Value	Description
1	The PPSLOCKED bit can only be set once after an unlocking sequence is executed; once PPSLOCK is set, all future changes to PPS registers are prevented
0	The PPSLOCKED bit can be set and cleared as needed (unlocking sequence is required)

Bit 2 – $\overline{\text{ZCD}}$ ZCD Disable

Value	Description
1	ZCD disabled, ZCD can be enabled by setting the ZCDSEN bit of ZCDCON
0	ZCD always enabled, $\text{PMDx}[\text{ZCDMD}]$ bit is ignored

Bits 1:0 – BORV[1:0] Brown-out Reset Voltage Selection⁽¹⁾

Value	Description
11	Brown-out Reset Voltage (V_{BOR}) set to 1.90V
10	Brown-out Reset Voltage (V_{BOR}) set to 2.45V
01	Brown-out Reset Voltage (V_{BOR}) set to 2.7V
00	Brown-out Reset Voltage (V_{BOR}) set to 2.85V

Note:

1. The higher voltage setting is recommended for operation at or above 16 MHz.

6.5 CONFIG5

Name: CONFIG5
Address: 30 0004h

Configuration Byte 5

Bit	7	6	5	4	3	2	1	0
		WDTE[1:0]				WDTCP5[4:0]		
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	1	1	1	1	1

Bits 6:5 – WDTE[1:0] WDT Operating Mode

Value	Description
11	WDT enabled regardless of Sleep; SEN bit in WDTCON0 is ignored
10	WDT enabled while Sleep = 0, suspended when Sleep = 1; SEN bit in WDTCON0 is ignored
01	WDT enabled/disabled by SEN bit in WDTCON0
00	WDT disabled, SEN bit in WDTCON0 is ignored

Bits 4:0 – WDTCP5[4:0] WDT Period Select

WDTCP5	WDTCON0[WDTPS] at POR			Typical Time Out (F _{IN} = 31 kHz)	Software Control of WDTPS?
	Value	Divider Ratio			
11111	01011	1:65536	2 ¹⁶	2s	Yes
11110 to 10011	11110 to 10011	1:32	2 ⁵	1 ms	No
10010	10010	1:8388608	2 ²³	256s	No
10001	10001	1:4194304	2 ²²	128s	No
10000	10000	1:2097152	2 ²¹	64s	No
01111	01111	1:1048576	2 ²⁰	32s	No
01110	01110	1:524288	2 ¹⁹	16s	No
01101	01101	1:262144	2 ¹⁸	8s	No
01100	01100	1:131072	2 ¹⁷	4s	No
01011	01011	1:65536	2 ¹⁶	2s	No
01010	01010	1:32768	2 ¹⁵	1s	No
01001	01001	1:16384	2 ¹⁴	512 ms	No
01000	01000	1:8192	2 ¹³	256 ms	No
00111	00111	1:4096	2 ¹²	128 ms	No
00110	00110	1:2048	2 ¹¹	64 ms	No
00101	00101	1:1024	2 ¹⁰	32 ms	No
00100	00100	1:512	2 ⁹	16 ms	No
00011	00011	1:256	2 ⁸	8 ms	No
00010	00010	1:128	2 ⁷	4 ms	No
00001	00001	1:64	2 ⁶	2 ms	No
00000	00000	1:32	2 ⁵	1 ms	No

6.6 CONFIG6

Name: CONFIG6
Address: 30 0005h

Configuration Byte 6

Bit	7	6	5	4	3	2	1	0
			WDTCCS[2:0]			WDTCWS[2:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 5:3 – WDTCCS[2:0] WDT Input Clock Selector

Value	Condition	Description
x	WDTE = 00	These bits have no effect
111	WDTE ≠ 00	Software control
110 to 011	WDTE ≠ 00	Reserved
010	WDTE ≠ 00	WDT reference clock is the SOSC
001	WDTE ≠ 00	WDT reference clock is the 31.25 kHz MFINTOSC
000	WDTE ≠ 00	WDT reference clock is the 31.0 kHz LFINTOSC

Bits 2:0 – WDTCWS[2:0] WDT Window Select

WDTCWS	WDTCON1[WINDOW] at POR			Software Control of WINDOW	Keyed Access Required?
	Value	Window Delay Percent of Time	Window Opening Percent of Time		
111	111	n/a	100	Yes	No
110	110	n/a	100		
101	101	25	75		
100	100	37.5	62.5	No	Yes
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

6.7 CONFIG7

Name: CONFIG7
Address: 30 0006h

Configuration Byte 7

Bit	7	6	5	4	3	2	1	0
			DEBUG	SAFEN	BBEN	BBSIZE[2:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit 5 – DEBUG Debugger Enable

Value	Description
1	Background debugger disabled
0	Background debugger enabled

Bit 4 – SAFEN Storage Area Flash (SAF) Enable⁽¹⁾

Value	Description
1	SAF is disabled
0	SAF is enabled

Bit 3 – BBEN Boot Block Enable⁽¹⁾

Value	Description
1	Boot Block is disabled
0	Boot Block is enabled

Bits 2:0 – BBSIZE[2:0] Boot Block Size Selection⁽²⁾

Table 6-2. Boot Block Size

BBEN	BBSIZE	End Address of Boot Block	Boot Block Size (words)		
			PIC18Fx4Q41	PIC18Fx5Q41	PIC18Fx6Q41
1	xxx	–	–		
0	111	00 03FFh	512		
0	110	00 07FFh	1024		
0	101	00 0FFFh	2048		
0	100	00 1FFFh	4096		
0	011	00 3FFFh	–	8192	
0	010	00 7FFFh	–		16384
0	001	00 FFFFh	–		
0	000	01 FFFFh	–		

Note:

- Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.
- BBSIZE[2:0] bits can only be changed when BBEN = 1. Once BBEN = 0, BBSIZE[2:0] can only be changed through a Bulk Erase.

6.8 CONFIG8

Name: CONFIG8
Address: 30 0007h

Configuration Byte 8

Bit	7	6	5	4	3	2	1	0
	WRTAPP				WRTSAF	WRTD	WRTC	WRTB
Access	R/W				R/W	R/W	R/W	R/W
Reset	1				1	1	1	1

Bit 7 – WRTAPP Application Block Write Protection⁽¹⁾

Value	Description
1	Application Block is NOT write-protected
0	Application Block is write-protected

Bit 3 – WRTSAF Storage Area Flash (SAF) Write Protection^(1,2)

Value	Description
1	SAF is NOT write-protected
0	SAF is write-protected

Bit 2 – WRTD Data EEPROM Write Protection⁽¹⁾

Value	Description
1	Data EEPROM is NOT write-protected
0	Data EEPROM is write-protected

Bit 1 – WRTC Configuration Register Write Protection⁽¹⁾

Value	Description
1	Configuration registers are NOT write-protected
0	Configuration registers are write-protected

Bit 0 – WRTB Boot Block Write Protection^(1,3)

Value	Description
1	Boot Block is NOT write-protected
0	Boot Block is write-protected

Note:

1. Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.
2. Applicable only if $\overline{\text{SAFEN}} = 0$.
3. Applicable only if $\overline{\text{BBEN}} = 0$.

6.9 CONFIG9

Name: CONFIG9
Address: 30 0008h

Configuration Byte 9

Bit	7	6	5	4	3	2	1	0
								$\overline{\text{CP}}$
Access								R/W
Reset								1

Bit 0 – $\overline{\text{CP}}$ User Program Flash Memory and Data EEPROM Code Protection

Value	Description
1	User Program Flash Memory and Data EEPROM code protection are disabled
0	User Program Flash Memory and Data EEPROM code protection are enabled

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