



# PIC16(L)F153XX

## Cost-Effective 8 to 48 Pins Microcontroller Product Brief

### Description

PIC16(L)F153XX microcontrollers feature Intelligent Analog, Core Independent Peripherals (CIPs) and communication peripherals combined with eXtreme Low-Power (XLP) for a wide range of general purpose and low-power applications. The family features PWMs, multiple communication, temperature sensor and memory features like Memory Access Partition (MAP) and Device Information Area (DIA). The products are offered in a broad range of pin counts from 8 to 48 pins, to support customers in various applications.

### Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Timers:
  - 8-bit (TMR2) with Hardware Limit Timer (HLT) Extension
  - 16-bit (TMR0/1)
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Variable prescaler selection
  - Variable window size selection
  - All sources configurable in hardware or software
- Programmable Code Protection

### Memory

- Up to 28 KB Flash Program Memory
- Up to 2 KB Data SRAM Memory
- Direct, Indirect and Relative Addressing modes
- Memory Access Partition (MAP):
  - Write protect
  - Customizable Partition
- Device Information Area (DIA)

### Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF153XX)
  - 2.3V to 5.5V (PIC16F153XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### Power-Saving Functionality

- Doze mode:
  - Ability to run CPU core slower than the system clock
- Idle mode:
  - Ability to halt CPU core while internal peripherals continue operating
- Sleep mode:
  - Lowest power consumption
- Peripheral Module Disable (PMD):
  - Ability to disable hardware module to minimize power consumption of unused peripherals

### eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

### Digital Peripherals

- Four Configurable Logic Cells (CLCs):
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and Falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
- Two Capture/Compare/PWM (CCP) modules
- Four 10-bit PWMs
- Numerically Controlled Oscillator (NCO):
  - Generates true linear frequency control and increased frequency resolution
  - Input Clock: 0 Hz < f<sub>NCO</sub> < 32 MHz
  - Resolution: f<sub>NCO</sub>/220
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O

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- Communication:
  - Up to two EUSART, RS-232, RS-485, LIN compatible
  - Up to two SPI
  - Two I<sup>2</sup>C, SMBus, PMBus™ compatible
- Up to 44 I/O Pins
  - Individually programmable pull-ups slew rate control Interrupt-on-Change with edge-select

## Analog Peripherals

- Analog-to-Digital Converter (ADC):
  - 10-bit with up to 43 external channels
  - Conversion available during Sleep
- Two Comparator:
  - Low-Power/High-Speed mode
  - Fixed Voltage Reference at (non)inverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output level

## Flexible Oscillator Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 32 MHz
  - $\pm 1\%$  at calibration (nominal)
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOCS)
- External Oscillator Block with:
  - Three crystal/resonator modes up to 20 MHz
  - Three external clock modes up to 20 MHz
  - Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripherals clock stops
  - Oscillator Start-up Timer (OST)
  - Ensures stability of crystal oscillator sources

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**TABLE 1: PIC16(L)F153XX FAMILY TYPES**

| Device                      | Data Sheet Index | Program Flash Memory (KW) | Program Flash Memory (KB) | Storage Area Flash (B) | Data SRAM (bytes) | I/O Pins | 10-Bit ADC | 5-Bit DAC | Comparator | 8-Bit/ (with HLT) Timer | 16-Bit Timer | Window Watchdog Timer | CCP/10-Bit PWM | CWG | NCO | CLC | Zero Cross Detect | Temperature Sensor | Memory Access Partition | Device Information Area | EUSART/ I <sup>2</sup> C/SPI | Peripheral Pin Select | Peripheral Module Disable | Debug <sup>(1)</sup> |
|-----------------------------|------------------|---------------------------|---------------------------|------------------------|-------------------|----------|------------|-----------|------------|-------------------------|--------------|-----------------------|----------------|-----|-----|-----|-------------------|--------------------|-------------------------|-------------------------|------------------------------|-----------------------|---------------------------|----------------------|
| <a href="#">PIC16F15313</a> | (C)              | 2                         | 3.5                       | 224                    | 256               | 6        | 5          | 1         | 1          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 1/1                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15323</a> | (C)              | 2                         | 3.5                       | 224                    | 256               | 12       | 11         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 1/1                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15324</a> | (D)              | 4                         | 7                         | 224                    | 512               | 12       | 11         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/1                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15325</a> | (B)              | 8                         | 14                        | 224                    | 1024              | 12       | 11         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/1                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15344</a> | (D)              | 4                         | 7                         | 224                    | 512               | 18       | 17         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/1                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15345</a> | (B)              | 8                         | 14                        | 224                    | 1024              | 18       | 17         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/1                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15354</a> | (A)              | 4                         | 7                         | 224                    | 512               | 25       | 24         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/2                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15355</a> | (A)              | 8                         | 14                        | 224                    | 1024              | 25       | 24         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/2                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15356</a> | (E)              | 16                        | 28                        | 224                    | 2048              | 25       | 24         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/2                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15375</a> | (F)              | 8                         | 14                        | 224                    | 1024              | 36       | 35         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/2                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15376</a> | (E)              | 16                        | 28                        | 224                    | 2048              | 36       | 35         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/2                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15385</a> | (F)              | 8                         | 14                        | 224                    | 1024              | 44       | 43         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/2                          | Y                     | Y                         | I                    |
| <a href="#">PIC16F15386</a> | (E)              | 16                        | 28                        | 224                    | 2048              | 44       | 43         | 1         | 2          | 1                       | 2            | Y                     | 2/4            | 1   | 1   | 4   | Y                 | Y                  | Y                       | Y                       | 2/2                          | Y                     | Y                         | I                    |

**Note 1:** I - Debugging integrated on chip.

**Data Sheet Index:**

- A:** Future Release [PIC16\(L\)F15354/5 Data Sheet, 28-Pin](#)
- B:** Future Release [PIC16\(L\)F15325/45 Data Sheet, 14/20-Pin](#)
- C:** Future Release [PIC16\(L\)F15313/23 Data Sheet, 8/14-Pin](#)
- D:** Future Release [PIC16\(L\)F15324/44 Data Sheet, 14/20-Pin](#)
- E:** Future Release [PIC16\(L\)F15356/76/86 Data Sheet, 28/40/48-Pin](#)
- F:** Future Release [PIC16\(L\)F15375/85 Data Sheet, 40/48-Pin](#)

**Note:** For other small form-factor package availability and marking information, visit [www.microchip.com/packaging](http://www.microchip.com/packaging) or contact your local sales office.

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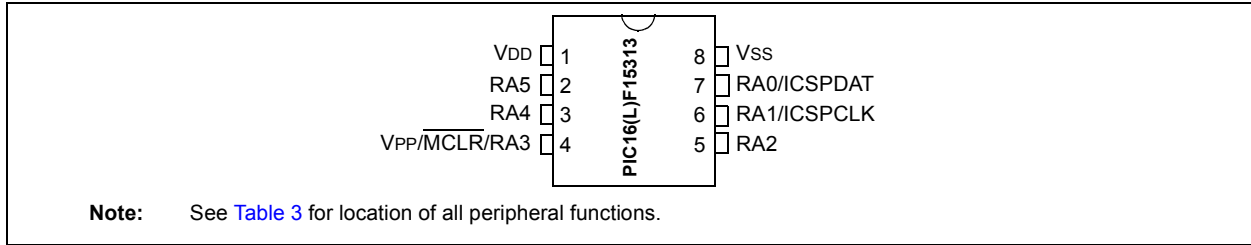
**TABLE 2: PACKAGES**

| Device         | (S)PDIP | SOIC | SSOP | TSSOP | (U)DFN<br>(3x3) | QFN<br>(4x4) | QFN<br>(6x6) | UQFN<br>(4x4) | TQFP | QFN<br>(8x8) | UQFN<br>(5x5) | UQFN<br>(6x6) |
|----------------|---------|------|------|-------|-----------------|--------------|--------------|---------------|------|--------------|---------------|---------------|
| PIC16(L)F15313 | X       | X    | —    | —     | X               | —            | —            | —             | —    | —            | —             | —             |
| PIC16(L)F15323 | X       | X    | —    | X     | —               | X            | —            | X             | —    | —            | —             | —             |
| PIC16(L)F15324 | X       | X    | —    | X     | —               | X            | —            | X             | —    | —            | —             | —             |
| PIC16(L)F15325 | X       | X    | —    | X     | —               | X            | —            | X             | —    | —            | —             | —             |
| PIC16(L)F15344 | X       | X    | X    | —     | —               | X            | —            | X             | —    | —            | —             | —             |
| PIC16(L)F15345 | X       | X    | X    | —     | —               | X            | —            | X             | —    | —            | —             | —             |
| PIC16(L)F15354 | X       | X    | X    | —     | —               | —            | X            | X             | —    | —            | —             | —             |
| PIC16(L)F15355 | X       | X    | X    | —     | —               | —            | X            | X             | —    | —            | —             | —             |
| PIC16(L)F15356 | X       | X    | X    | —     | —               | —            | X            | X             | —    | —            | —             | —             |
| PIC16(L)F15375 | X       | —    | —    | —     | —               | —            | —            | —             | X    | X            | X             | —             |
| PIC16(L)F15376 | X       | —    | —    | —     | —               | —            | —            | —             | X    | X            | X             | —             |
| PIC16(L)F15385 | —       | —    | —    | —     | —               | —            | —            | —             | X    | —            | —             | X             |
| PIC16(L)F15386 | —       | —    | —    | —     | —               | —            | —            | —             | X    | —            | —             | X             |

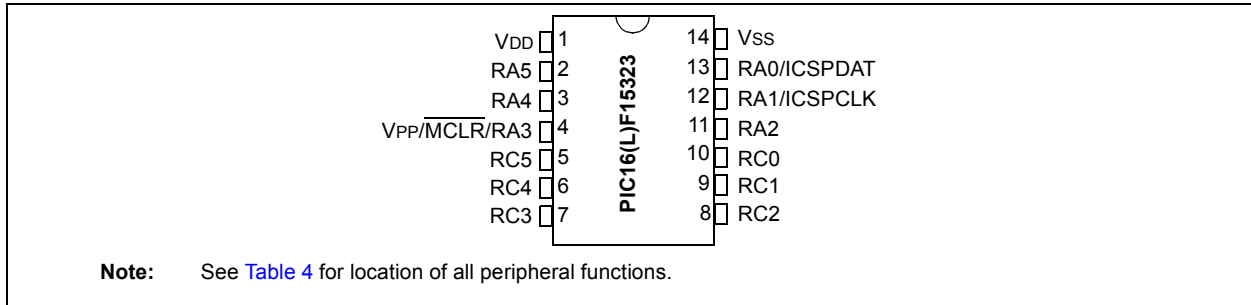
**Note:** Pin details are subject to change.

## PIN DIAGRAMS

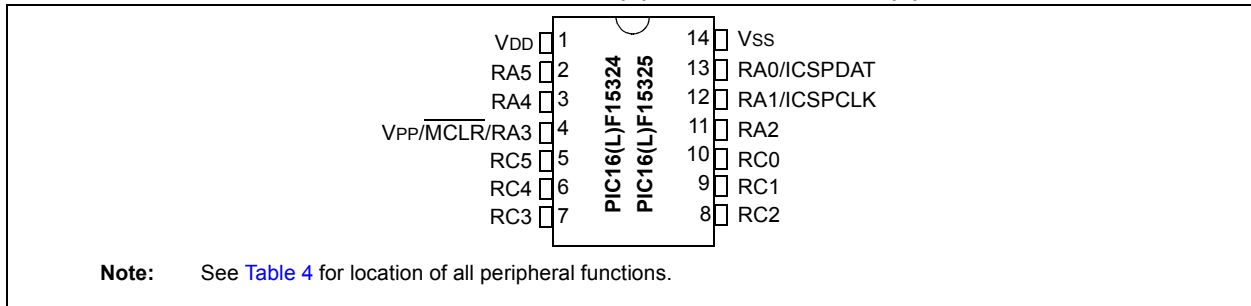
**FIGURE 1: 8-PIN PDIP, SOIC, MSOP, FOR PIC16(L)F15313**



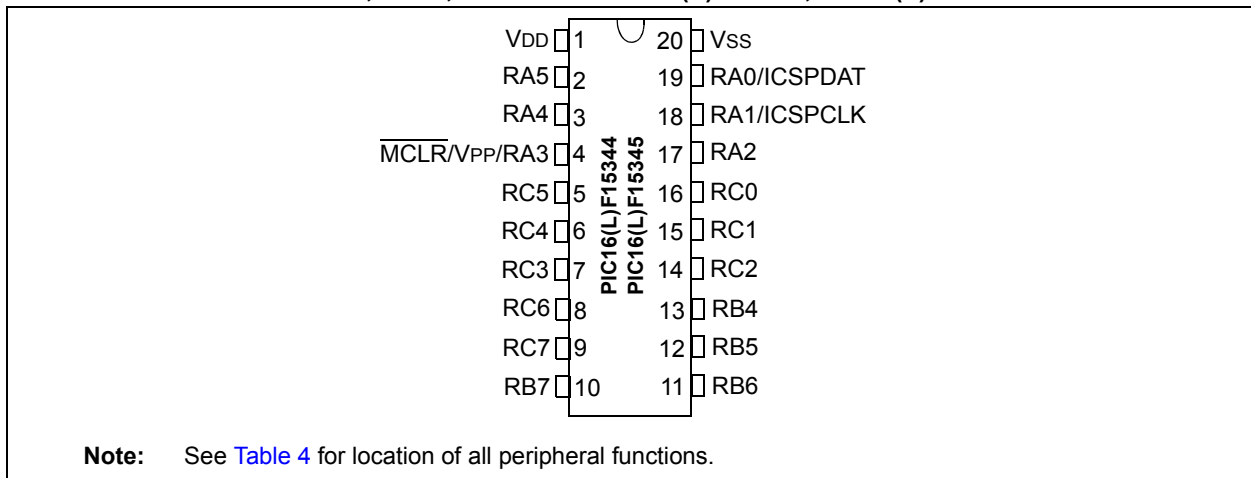
**FIGURE 2: 14-PIN PDIP, SOIC, TSSOP FOR PIC16(L)F15323**



**FIGURE 3: 14-PIN PDIP, TSSOP FOR PIC16(L)F15324 AND PIC16(L)F15325**



**FIGURE 4: 20-PIN PDIP, SOIC, SSOP FOR PIC16(L)F15344, PIC16(L)F15345**



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FIGURE 5: 28-PIN PDIP, SOIC, SSOP FOR PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356

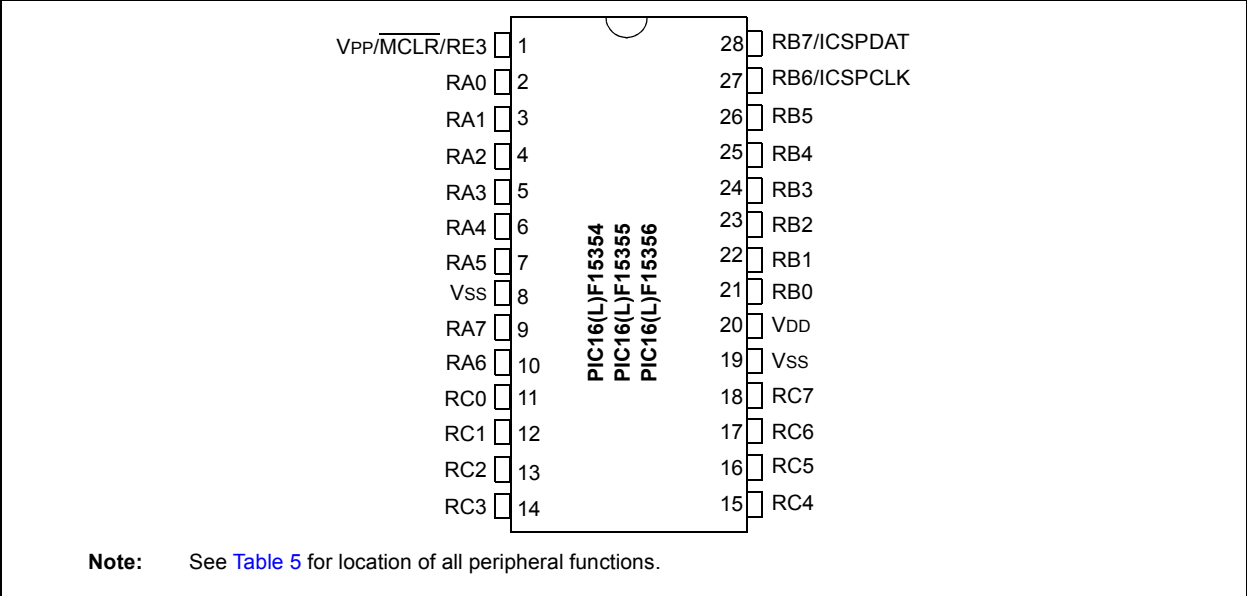
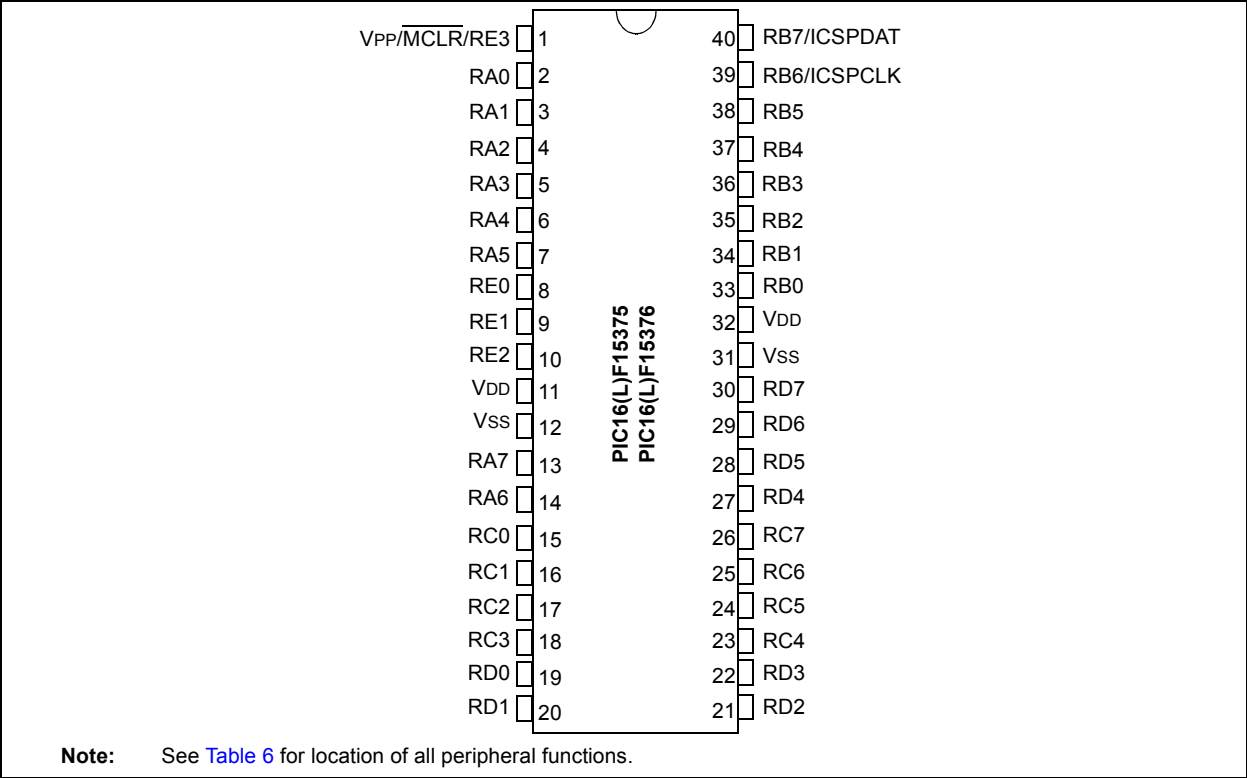
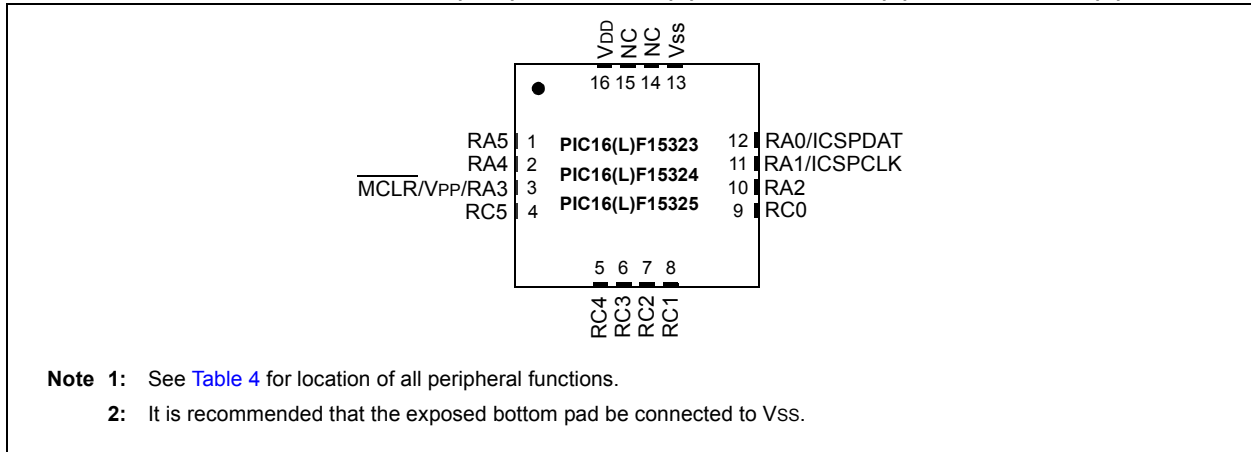


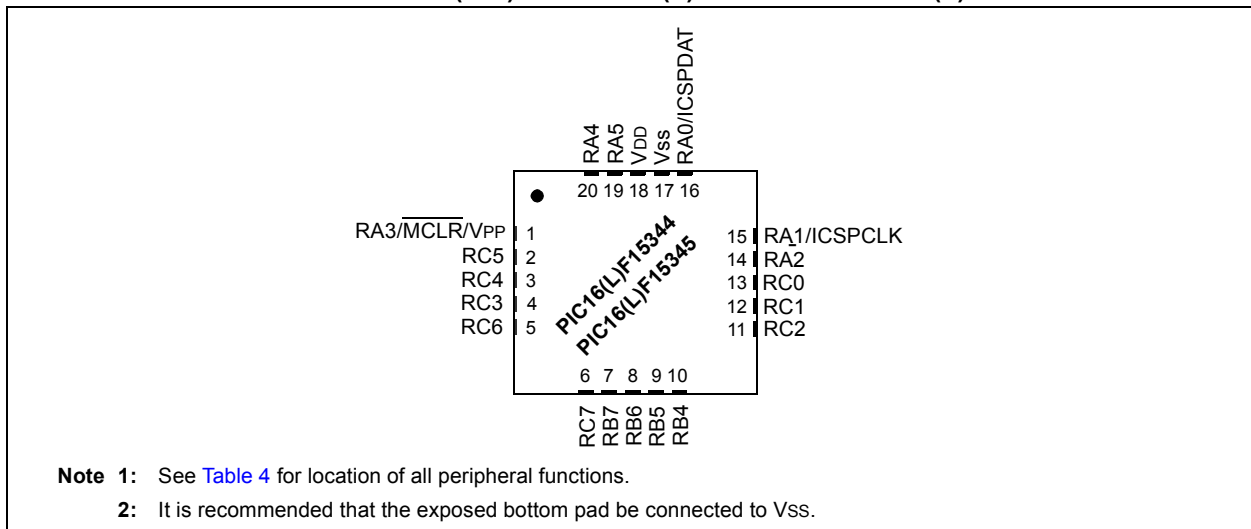
FIGURE 6: 40-PIN PDIP FOR PIC16(L)F15375, PIC16(L)F15376



**FIGURE 7: 16-PIN QFN/UQFN (4X4) FOR PIC16(L)F15323, PIC16(L)F15324, PIC16(L)F15325**



**FIGURE 8: 20-PIN QFN/UQFN (4x4) FOR PIC16(L)F15344 AND PIC16(L)F15345**



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FIGURE 9: 28-PIN UQFN (4X4) FOR PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356

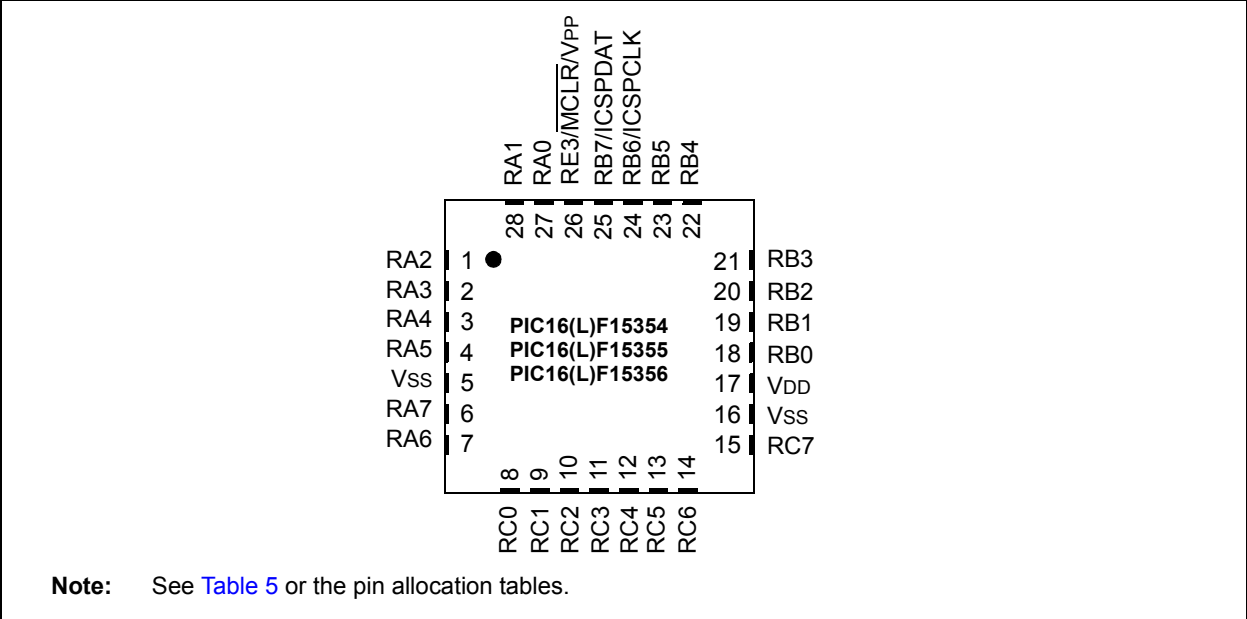
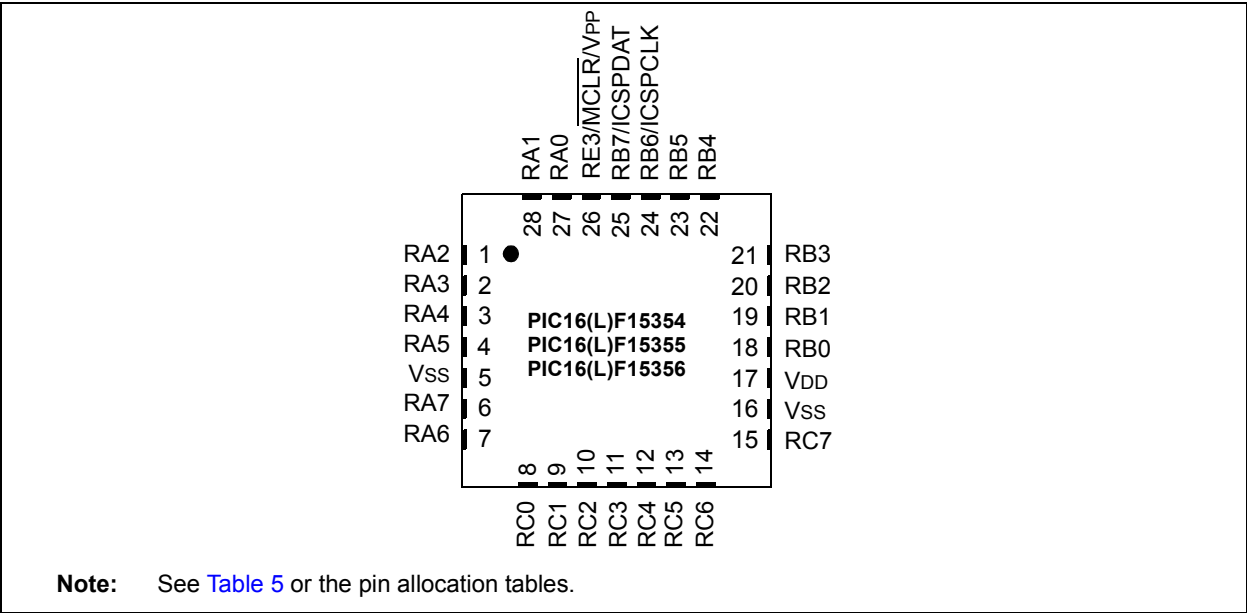
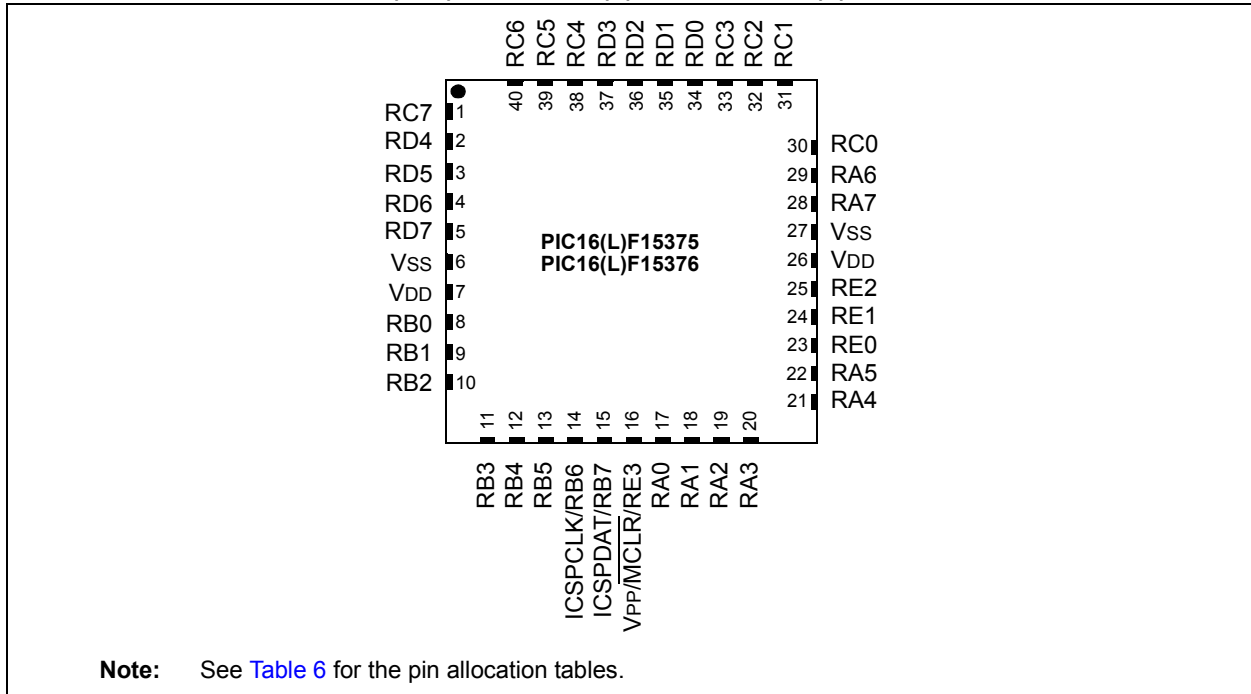


FIGURE 10: 28-PIN QFN (6X6) FOR PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356

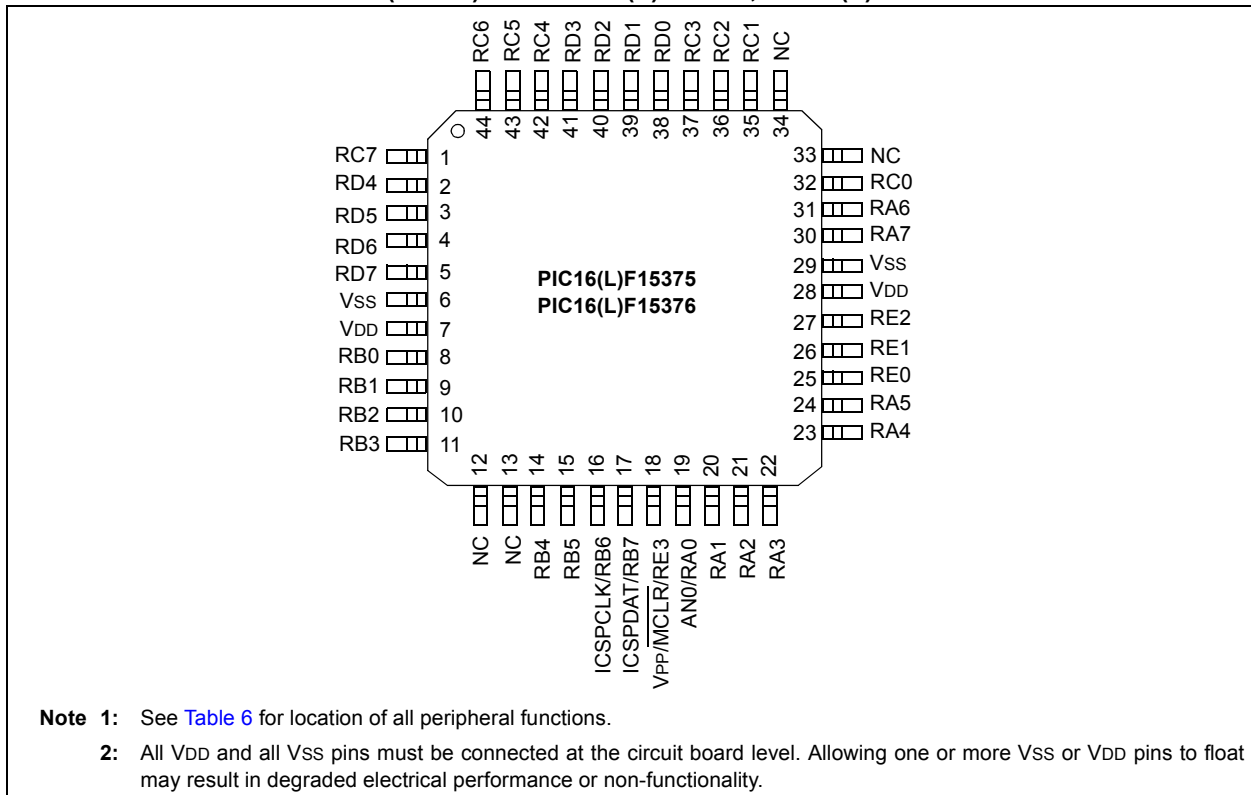




**FIGURE 11: 40-PIN UQFN (5X5) FOR PIC16(L)F15375, PIC16(L)F15376**

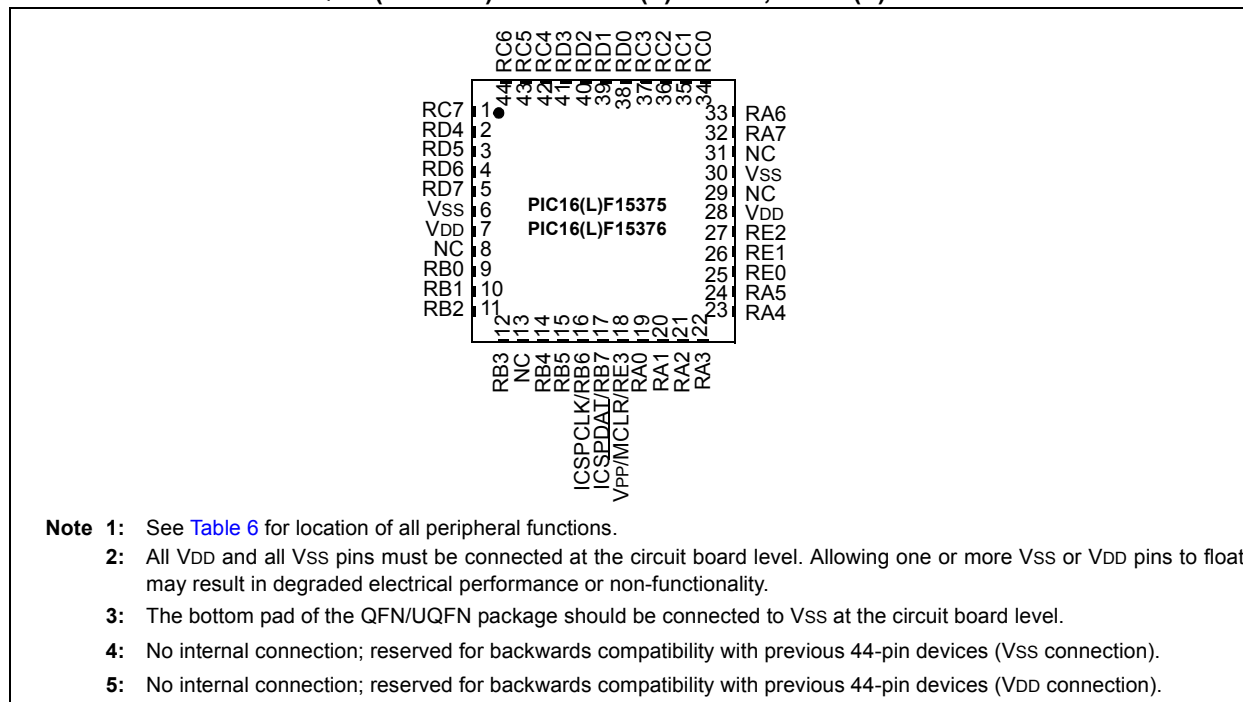


**FIGURE 12: 44-PIN TQFP (10X10) FOR PIC16(L)F15375, PIC16(L)F15376**

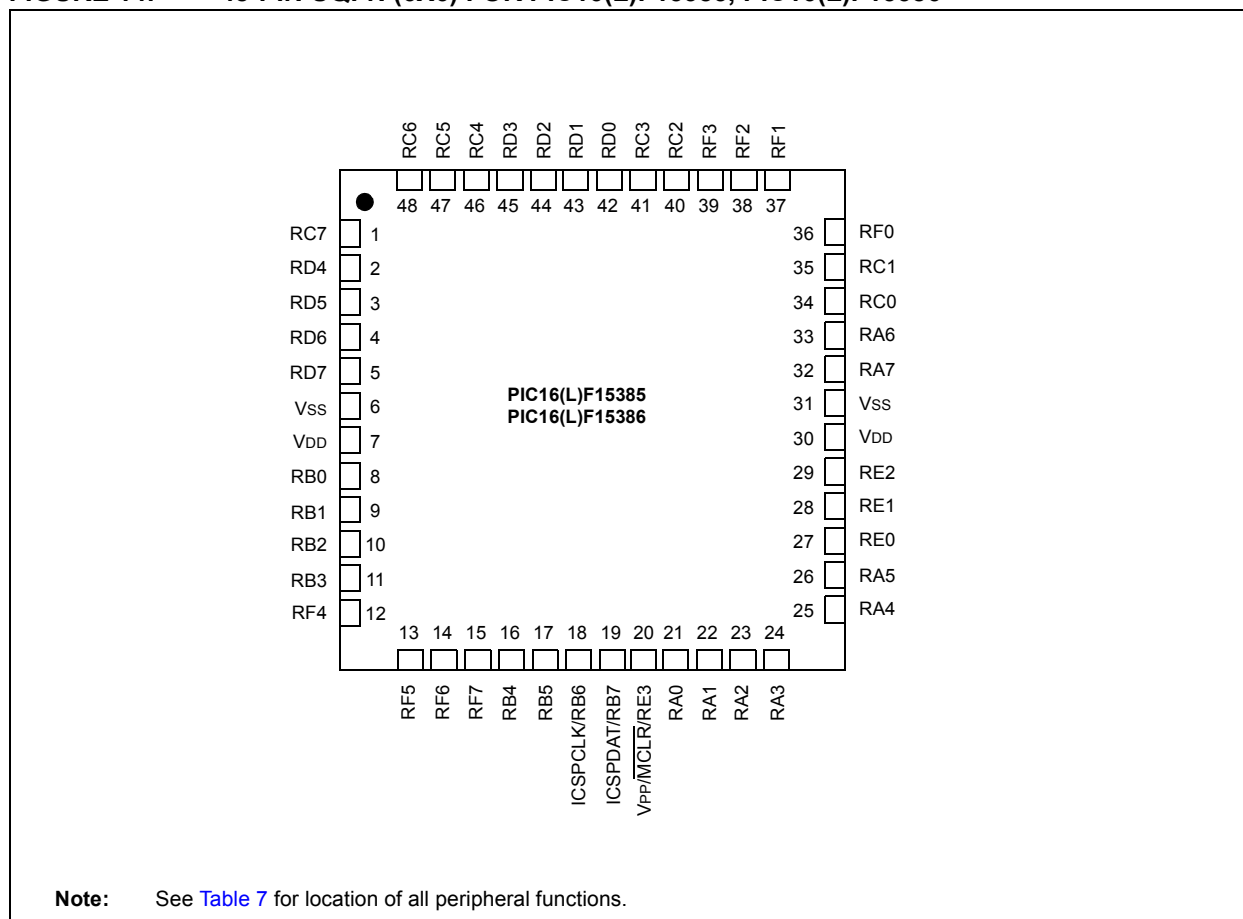


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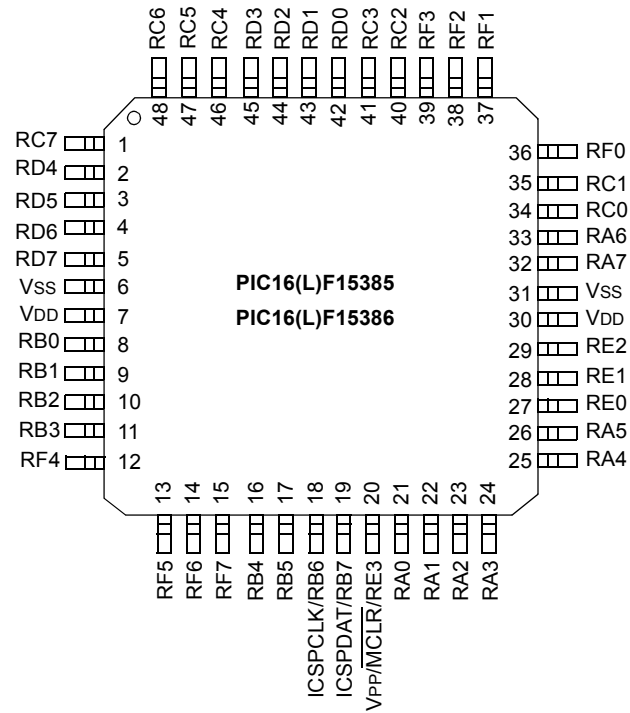
**FIGURE 13: 44-PIN QFN (8X8X0.9) FOR PIC16(L)F15375, PIC16(L)F15376**



**FIGURE 14: 48-PIN UQFN (6X6) FOR PIC16(L)F15385, PIC16(L)F15386**



**FIGURE 15: 48-PIN TQFP (7X7) FOR PIC16(L)F15385, PIC16(L)F15386**



**Note:** See [Table 7](#) for location of all peripheral functions.

## PIN ALLOCATION TABLES

**TABLE 3: 8-PIN ALLOCATION TABLE (PIC16(L)F15313)**

| I/O I <sup>(2)</sup> | 8-Pin PDIP/SOIC/MSOP | ADC                          | Reference         | Comparator | NCO     | DAC                  | Timers                                                         | CCP                                        | PWM  | CWG                 | MSSP                                                     | ZCD  | EUSART               | CLC                   | CLKR | Interrupt                   | Pull-up | Basic                   |
|----------------------|----------------------|------------------------------|-------------------|------------|---------|----------------------|----------------------------------------------------------------|--------------------------------------------|------|---------------------|----------------------------------------------------------|------|----------------------|-----------------------|------|-----------------------------|---------|-------------------------|
| RA0                  | 7                    | ANA0                         | —                 | C1IN0+     | —       | DAC1OUT              | —                                                              | —                                          | —    | —                   | —                                                        | —    | TX/CK <sup>(1)</sup> | CLCIN3 <sup>(1)</sup> | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT      |
| RA1                  | 6                    | ANA1                         | V <sub>REF+</sub> | C1IN0-     | —       | DA1 <sub>REF+</sub>  | T0CKI <sup>(1)</sup>                                           | —                                          | —    | —                   | SSP1CLK <sup>(1),(4)</sup><br>SSP1DAT <sup>(1),(4)</sup> | —    | RX/DT <sup>(1)</sup> | CLCIN2 <sup>(1)</sup> | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK      |
| RA2                  | 5                    | ANA2                         | V <sub>REF-</sub> | —          | —       | DAC1 <sub>REF-</sub> | —                                                              | —                                          | —    | CWG1 <sup>(1)</sup> | SSP1CLK <sup>(1),(4)</sup><br>SSP1DAT <sup>(1),(4)</sup> | ZCD1 | —                    | —                     | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                       |
| RA3                  | 4                    | —                            | —                 | —          | —       | —                    | —                                                              | —                                          | —    | —                   | SSP1SS <sup>(1)</sup>                                    | —    | —                    | CLCIN0 <sup>(1)</sup> | —    | IOCA3                       | Y       | MCLR<br>V <sub>PP</sub> |
| RA4                  | 3                    | ANA4                         | —                 | C1IN1-     | —       | —                    | T1G <sup>(1)</sup><br>SOSCO                                    | —                                          | —    | —                   | —                                                        | —    | —                    | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2          |
| RA5                  | 2                    | ANA5<br>ADACT <sup>(1)</sup> | —                 | —          | —       | —                    | T1CKI <sup>(1)</sup><br>T2IN <sup>(1)</sup><br>SOSCIN<br>SOSCI | CCP1 <sup>(1)</sup><br>CCP2 <sup>(1)</sup> | —    | —                   | —                                                        | —    | —                    | CLCIN1 <sup>(1)</sup> | —    | IOCA5                       | Y       | CLKIN<br>OSC1<br>EIN    |
| V <sub>DD</sub>      | 1                    | —                            | —                 | —          | —       | —                    | —                                                              | —                                          | —    | —                   | —                                                        | —    | —                    | —                     | —    | —                           | —       | V <sub>DD</sub>         |
| V <sub>SS</sub>      | 8                    | —                            | —                 | —          | —       | —                    | —                                                              | —                                          | —    | —                   | —                                                        | —    | —                    | —                     | —    | —                           | —       | V <sub>SS</sub>         |
| OUT <sup>(2)</sup>   | —                    | —                            | —                 | C1OUT      | NCO1OUT | —                    | TMR0                                                           | CCP1                                       | PWM3 | CWG1A               | SDO1                                                     | —    | DT1 <sup>(3)</sup>   | CLC1OUT               | CLKR | —                           | —       | —                       |
|                      | —                    | —                            | —                 | C2OUT      | —       | —                    | —                                                              | CCP2                                       | PWM4 | CWG1B               | SCK1                                                     | —    | CK1                  | CLC2OUT               | —    | —                           | —       | —                       |
|                      | —                    | —                            | —                 | —          | —       | —                    | —                                                              | —                                          | PWM5 | CWG1C               | SCL1 <sup>(3),(4)</sup>                                  | —    | TX1                  | CLC3OUT               | —    | —                           | —       | —                       |
|                      | —                    | —                            | —                 | —          | —       | —                    | —                                                              | —                                          | PWM6 | CWG1D               | SDA1 <sup>(3),(4)</sup>                                  | —    | —                    | CLC4OUT               | —    | —                           | —       | —                       |

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV<sub>L</sub> register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

**TABLE 4: 14/16/20-PIN ALLOCATION TABLE (PIC16(L)F15323, PIC16(L)F15324, PIC16(L)F15325, PIC16(L)F15344, PIC16(L)F15345)**

| I/O(2) | 14-Pin PDIP/SSOP | 16-Pin QFN/UQFN | 20-Pin PDIP/SSOP | 20-Pin QFN | ADC                          | Reference         | Comparator       | NCO | DAC                  | Timers                                          | CCP  | PWM | CWG                 | MSSP                                                     | ZCD  | EUSART                 | CLC                                                    | CLKR | Interrupt                   | Pull-up | Basic                   |
|--------|------------------|-----------------|------------------|------------|------------------------------|-------------------|------------------|-----|----------------------|-------------------------------------------------|------|-----|---------------------|----------------------------------------------------------|------|------------------------|--------------------------------------------------------|------|-----------------------------|---------|-------------------------|
| RA0    | 13               | 12              | 19               | 16         | ANA0                         | —                 | C1IN0+           | —   | DAC1OUT              | —                                               | —    | —   | —                   | —                                                        | —    | —                      | —                                                      | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT      |
| RA1    | 12               | 11              | 18               | 15         | ANA1                         | V <sub>REF+</sub> | C1IN0-           | —   | DA1 <sub>REF+</sub>  | T0CKI <sup>(1)</sup>                            | —    | —   | —                   | —                                                        | —    | —                      | —                                                      | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK      |
| RA2    | 11               | 10              | 17               | 14         | ANA2                         | V <sub>REF-</sub> | —                | —   | DAC1 <sub>REF-</sub> | —                                               | —    | —   | CWG1 <sup>(1)</sup> | —                                                        | ZCD1 | —                      | CLCIN0 <sup>(1),(6)</sup>                              | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                       |
| RA3    | 4                | 3               | 4                | 1          | —                            | —                 | —                | —   | —                    | —                                               | —    | —   | —                   | —                                                        | —    | —                      | —                                                      | —    | IOCA3                       | Y       | MCLR<br>V <sub>PP</sub> |
| RA4    | 3                | 2               | 3                | 20         | ANA4                         | —                 | C1IN1-           | —   | —                    | T1G <sup>(1)</sup><br>SOSCO                     | —    | —   | —                   | —                                                        | —    | —                      | —                                                      | —    | IOCA4                       | Y       | CLKOUT<br>OSC2          |
| RA5    | 2                | 1               | 2                | 19         | ANA5                         | —                 | —                | —   | —                    | T1CKI <sup>(1)</sup><br>T2IN<br>SOSCIN<br>SOSCI | —    | —   | —                   | —                                                        | —    | —                      | CLCIN3 <sup>(1),(5)</sup>                              | —    | IOCA5                       | Y       | CLKIN<br>OSC1<br>EIN    |
| RC0    | 10               | 9               | 16               | 13         | ANC0                         | —                 | C2IN0+           | —   | —                    | —                                               | —    | —   | —                   | SSP1CLK <sup>(1),(5)</sup><br>SSP1DAT <sup>(1),(5)</sup> | —    | —                      | —                                                      | —    | IOCC0                       | Y       | —                       |
| RC1    | 9                | 8               | 15               | 12         | ANC1                         | —                 | C1IN1-<br>C2IN1- | —   | —                    | —                                               | —    | —   | —                   | SSP1CLK <sup>(1),(5)</sup><br>SSP1DAT <sup>(1),(5)</sup> | —    | —                      | CLCIN2 <sup>(1),(5)</sup>                              | —    | IOCC1                       | Y       | —                       |
| RC2    | 8                | 7               | 14               | 11         | ANC2                         | —                 | C1IN2-<br>C2IN2- | —   | —                    | —                                               | —    | —   | —                   | —                                                        | —    | —                      | —                                                      | —    | IOCC2                       | Y       | —                       |
| RC3    | 7                | 6               | 7                | 4          | ANC3                         | —                 | C1IN3-<br>C2IN3- | —   | —                    | —                                               | CCP2 | —   | —                   | SSP1SS <sup>(5)</sup>                                    | —    | —                      | CLCIN1 <sup>(1),(6)</sup><br>CLCIN0 <sup>(1),(5)</sup> | —    | IOCC3                       | Y       | —                       |
| RC4    | 6                | 5               | 6                | 3          | ANC4                         | —                 | —                | —   | —                    | —                                               | —    | —   | —                   | SSP2CLK <sup>(1),(5)</sup><br>SSP2DAT <sup>(1),(5)</sup> | —    | TX1/CK1 <sup>(5)</sup> | CLCIN1 <sup>(1),(5)</sup>                              | —    | IOCC4                       | Y       | —                       |
| RC5    | 5                | 4               | 5                | 2          | ANC5                         | —                 | —                | —   | —                    | —                                               | CCP1 | —   | —                   | SSP1CLK <sup>(1),(5)</sup><br>SSP1DAT <sup>(1),(5)</sup> | —    | RX1/DT1 <sup>(5)</sup> | —                                                      | —    | IOCC5                       | Y       | —                       |
| RC6    | —                | —               | 8                | 5          | ANC6                         | —                 | —                | —   | —                    | —                                               | —    | —   | —                   | SSP1SS1 <sup>(6)</sup>                                   | —    | —                      | —                                                      | —    | IOCC6                       | Y       | —                       |
| RC7    | —                | —               | 9                | 6          | ANC7                         | —                 | —                | —   | —                    | —                                               | —    | —   | —                   | —                                                        | —    | —                      | —                                                      | —    | IOCC7                       | Y       | —                       |
| RB4    | —                | —               | 13               | 10         | ANB4<br>ADACT <sup>(1)</sup> | —                 | —                | —   | —                    | —                                               | —    | —   | —                   | SSP1CLK <sup>(1),(6)</sup><br>SSP1DAT <sup>(1),(6)</sup> | —    | —                      | CLCIN2 <sup>(1),(6)</sup>                              | —    | IOCB4                       | —       | —                       |
| RB5    | —                | —               | 12               | 9          | ANB5                         | —                 | —                | —   | —                    | —                                               | —    | —   | —                   | SSP2CLK <sup>(1),(6)</sup><br>SSP2DAT <sup>(1),(6)</sup> | —    | RX1/DT1 <sup>(6)</sup> | CLCIN3 <sup>(1),(6)</sup>                              | —    | IOCB5                       | —       | —                       |

**PIC16(L)F153XX**

**TABLE 4: 14/16/20-PIN ALLOCATION TABLE (PIC16(L)F15323, PIC16(L)F15324, PIC16(L)F15325, PIC16(L)F15344, PIC16(L)F15345)**

| I/O <sup>(2)</sup> | 14-Pin PDIP/SOIC/TSSOP | 16-Pin QFN/UQFN | 20-Pin PDIP/SOIC/SSOP | 20-Pin QFN | ADC  | Reference | Comparator | NCO     | DAC | Timers | CCP  | PWM  | CWG   | MSSP                                                     | ZCD | EUSART                 | CLC     | CLKR | Interrupt | Pull-up | Basic           |
|--------------------|------------------------|-----------------|-----------------------|------------|------|-----------|------------|---------|-----|--------|------|------|-------|----------------------------------------------------------|-----|------------------------|---------|------|-----------|---------|-----------------|
| RB6                | —                      | —               | 11                    | 8          | ANB6 | —         | —          | —       | —   | —      | —    | —    | —     | SSP1CLK <sup>(1),(6)</sup><br>SSP1DAT <sup>(1),(6)</sup> | —   | —                      | —       | —    | IOCB6     | Y       | —               |
| RB7                | —                      | —               | 10                    | 7          | ANB7 | —         | —          | —       | —   | —      | —    | —    | —     | SSP2CLK <sup>(1),(6)</sup><br>SSP2DAT <sup>(1),(6)</sup> | —   | TX1/CK1 <sup>(6)</sup> | —       | —    | IOCB7     | Y       | —               |
| V <sub>DD</sub>    | 1                      | 16              | 1                     | 18         | —    | —         | —          | —       | —   | —      | —    | —    | —     | —                                                        | —   | —                      | —       | —    | —         | —       | V <sub>DD</sub> |
| V <sub>SS</sub>    | 14                     | 13              | 20                    | 17         | —    | —         | —          | —       | —   | —      | —    | —    | —     | —                                                        | —   | —                      | —       | —    | —         | —       | V <sub>SS</sub> |
| OUT <sup>(2)</sup> | —                      | —               | —                     | —          | —    | —         | C1OUT      | NCO1OUT | —   | TMR0   | CCP1 | PWM3 | CWG1A | SDO1<br>SDO2                                             | —   | DT1 <sup>(3)</sup>     | CLC1OUT | CLKR | —         | —       | —               |
|                    | —                      | —               | —                     | —          | —    | —         | C2OUT      | —       | —   | —      | CCP2 | PWM4 | CWG1B | SCK1<br>SCK2                                             | —   | CK1                    | CLC2OUT | —    | —         | —       | —               |
|                    | —                      | —               | —                     | —          | —    | —         | —          | —       | —   | —      | —    | PWM5 | CWG1C | SCL1 <sup>(3),(4)</sup><br>SCL2 <sup>(3),(4)</sup>       | —   | TX1                    | CLC3OUT | —    | —         | —       | —               |
|                    | —                      | —               | —                     | —          | —    | —         | —          | —       | —   | —      | —    | PWM6 | CWG1D | SDA1 <sup>(3),(4)</sup><br>SDA2 <sup>(3),(4)</sup>       | —   | —                      | CLC4OUT | —    | —         | —       | —               |

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.
  - 5: For 14 and 16-pin package only.
  - 6: For 20-pin package only.

**TABLE 5: 28-PIN ALLOCATION TABLE (PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356)**

| I/O <sup>(2)</sup> | 28-Pin PDIP/SSOP | 28-Pin (U)QFN | ADC                          | Reference | Comparator       | NCO | DAC      | Timers              | CCP                 | PWM | CWG                 | MSSP                                             | ZCD  | EUSART                    | CLC                   | CLKR | Interrupt                   | Pull-up | Basic             |
|--------------------|------------------|---------------|------------------------------|-----------|------------------|-----|----------|---------------------|---------------------|-----|---------------------|--------------------------------------------------|------|---------------------------|-----------------------|------|-----------------------------|---------|-------------------|
| RA0                | 2                | 27            | ANA0                         | —         | C1IN0-<br>C2IN0- | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | —                         | CLCIN0 <sup>(1)</sup> | —    | IOCA0                       | Y       | —                 |
| RA1                | 3                | 28            | ANA1                         | —         | C1IN1-<br>C2IN1- | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | —                         | CLCIN1 <sup>(1)</sup> | —    | IOCA1                       | Y       | —                 |
| RA2                | 4                | 1             | ANA2                         | —         | C1IN0+<br>C2IN0+ | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA2                       | Y       | —                 |
| RA3                | 5                | 2             | ANA3                         | VREF+     | C1IN1+           | —   | DACREF+  | —                   | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA3                       | Y       | —                 |
| RA4                | 6                | 3             | ANA4                         | —         | —                | —   | —        | T0CKI               | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA4                       | Y       | —                 |
| RA5                | 7                | 4             | ANA5                         | —         | —                | —   | —        | T1G <sup>(1)</sup>  | —                   | —   | —                   | SSP1SS <sup>(1)</sup>                            | —    | —                         | —                     | —    | IOCA5                       | Y       | —                 |
| RA6                | 10               | 7             | ANA6                         | —         | —                | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA6                       | Y       | CLKOUT            |
| RA7                | 9                | 6             | ANA7                         | —         | —                | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA7                       | Y       | CLKIN             |
| RB0                | 21               | 18            | ANB0                         | —         | C2IN1+           | —   | —        | —                   | —                   | —   | CWG1 <sup>(1)</sup> | SSP2SS <sup>(1)</sup>                            | ZCD1 | —                         | —                     | —    | INT <sup>(1)</sup><br>IOCB0 | Y       | —                 |
| RB1                | 22               | 19            | ANB1                         | —         | C1IN3-<br>C2IN3- | —   | —        | —                   | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCB1                       | Y       | —                 |
| RB2                | 23               | 20            | ANB2                         | —         | —                | —   | —        | —                   | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCB2                       | Y       | —                 |
| RB3                | 24               | 21            | ANB3                         | —         | C1IN2-<br>C2IN2- | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB3                       | Y       | —                 |
| RB4                | 25               | 22            | ANB4<br>ADACT <sup>(1)</sup> | —         | —                | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB4                       | Y       | —                 |
| RB5                | 26               | 23            | ANB5                         | —         | —                | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB5                       | Y       | —                 |
| RB6                | 27               | 24            | ANB6                         | —         | —                | —   | —        | —                   | —                   | —   | —                   | —                                                | —    | TX2<br>CK2 <sup>(1)</sup> | CLCIN2 <sup>(1)</sup> | —    | IOCB6                       | Y       | ICDCLK<br>ICSPCLK |
| RB7                | 28               | 25            | ANB7                         | —         | —                | —   | DAC1OUT2 | —                   | —                   | —   | —                   | —                                                | —    | RX2<br>DT2 <sup>(1)</sup> | CLCIN3 <sup>(1)</sup> | —    | IOCB7                       | Y       | ICDDAT<br>ICSPDAT |
| RC0                | 11               | 8             | ANC0                         | —         | —                | —   | —        | SOSCO<br>T1CKI      | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC0                       | Y       | —                 |
| RC1                | 12               | 9             | ANC1                         | —         | —                | —   | —        | SOSCI               | CCP2 <sup>(1)</sup> | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC1                       | Y       | —                 |
| RC2                | 13               | 10            | ANC2                         | —         | —                | —   | —        | —                   | CCP1 <sup>(1)</sup> | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC2                       | Y       | —                 |
| RC3                | 14               | 11            | ANC3                         | —         | —                | —   | —        | T2IN <sup>(1)</sup> | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCC3                       | Y       | —                 |
| RC4                | 15               | 12            | ANC4                         | —         | —                | —   | —        | —                   | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCC4                       | Y       | —                 |

**PIC16(L)F153XX**

**TABLE 5: 28-PIN ALLOCATION TABLE (PIC16(L)F15354, PIC16(L)F15355, PIC16(L)F15356) (CONTINUED)**

| I/O <sup>(2)</sup> | 28-Pin PDIP/SSOP | 28-Pin (U)QFN | ADC  | Reference | Comparator | NCO     | DAC | Timers | CCP  | PWM  | CWG            | MSSP                   | ZCD | EUSART                    | CLC     | CLKR | Interrupt | Pull-up | Basic                   |
|--------------------|------------------|---------------|------|-----------|------------|---------|-----|--------|------|------|----------------|------------------------|-----|---------------------------|---------|------|-----------|---------|-------------------------|
| RC5                | 16               | 13            | ANC5 | —         | —          | —       | —   | —      | —    | —    | —              | —                      | —   | —                         | —       | —    | IOCC5     | Y       | —                       |
| RC6                | 17               | 14            | ANC6 | —         | —          | —       | —   | —      | —    | —    | —              | —                      | —   | TX1<br>CK1 <sup>(1)</sup> | —       | —    | IOCC6     | Y       | —                       |
| RC7                | 18               | 15            | ANC7 | —         | —          | —       | —   | —      | —    | —    | —              | —                      | —   | RX1<br>DT1 <sup>(1)</sup> | —       | —    | IOCC7     | Y       | —                       |
| RE3                | 1                | 26            | ANE3 | —         | —          | —       | —   | —      | —    | —    | —              | —                      | —   | —                         | —       | —    | IOCE3     | Y       | MCLR<br>V <sub>PP</sub> |
| VDD                | 20               | 17            | —    | —         | —          | —       | —   | —      | —    | —    | —              | —                      | —   | —                         | —       | —    | —         | —       | VDD                     |
| VSS                | 8                | 16            | —    | —         | —          | —       | —   | —      | —    | —    | —              | —                      | —   | —                         | —       | —    | —         | —       | VSS                     |
| VSS                | 19               | 5             | —    | —         | —          | —       | —   | —      | —    | —    | —              | —                      | —   | —                         | —       | —    | —         | —       | VSS                     |
| VSEL0              | 19               | 17            | —    | —         | —          | —       | —   | —      | —    | —    | —              | —                      | —   | —                         | —       | —    | —         | —       | —                       |
| OUT <sup>(2)</sup> | —                | —             | —    | —         | C1OUT      | NCO1OUT | —   | TMR0   | CCP1 | PWM3 | CWG1A<br>CWG2A | SDO                    | —   | DT <sup>(3)</sup>         | CLC1OUT | CLKR | —         | —       | —                       |
|                    | —                | —             | —    | —         | C2OUT      | —       | —   | —      | CCP2 | PWM4 | CWG1B<br>CWG2B | SCK                    | —   | CK                        | CLC2OUT | —    | —         | —       | —                       |
|                    | —                | —             | —    | —         | —          | —       | —   | —      | —    | PWM5 | CWG1C<br>CWG2C | SCL <sup>(3),(4)</sup> | —   | TX                        | CLC3OUT | —    | —         | —       | —                       |
|                    | —                | —             | —    | —         | —          | —       | —   | —      | —    | PWM6 | CWG1D<br>CWG2D | SDA <sup>(3),(4)</sup> | —   | —                         | CLC4OUT | —    | —         | —       | —                       |

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.



**TABLE 6: 40/44-PIN ALLOCATION TABLE (PIC16(L)F15375, PIC16(L)F15376)**

| I/O <sup>(2)</sup> | 40-Pin PDIP | 40-Pin UQFN | 44-Pin QFN | 44-Pin TQFP | ADC                          | Reference | Comparator       | NCO | DAC      | Timers                        | CCP                 | PWM | CWG                 | MSSP                                             | ZCD  | EUSART                    | CLC                   | CLKR | Interrupt                   | Pull-up | Basic             |
|--------------------|-------------|-------------|------------|-------------|------------------------------|-----------|------------------|-----|----------|-------------------------------|---------------------|-----|---------------------|--------------------------------------------------|------|---------------------------|-----------------------|------|-----------------------------|---------|-------------------|
| RA0                | 2           | 17          | 19         | 19          | ANA0                         | —         | C1IN0-<br>C2IN0- | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | CLCIN0 <sup>(1)</sup> | —    | IOCA0                       | Y       | —                 |
| RA1                | 3           | 18          | 20         | 20          | ANA1                         | —         | C1IN1-<br>C2IN1- | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | CLCIN1 <sup>(1)</sup> | —    | IOCA1                       | Y       | —                 |
| RA2                | 4           | 19          | 21         | 21          | ANA2                         | —         | C1IN0+<br>C2IN0+ | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA2                       | Y       | —                 |
| RA3                | 5           | 20          | 22         | 22          | ANA3                         | VREF+     | C1IN1+           | —   | DACREF+  | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA3                       | Y       | —                 |
| RA4                | 6           | 21          | 23         | 23          | ANA4                         | —         | —                | —   | —        | T0CKI <sup>(1)</sup>          | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA4                       | Y       | —                 |
| RA5                | 7           | 22          | 24         | 24          | ANA5                         | —         | —                | —   | —        | T1G <sup>(1)</sup>            | —                   | —   | —                   | SSP1SS <sup>(1)</sup>                            | —    | —                         | —                     | —    | IOCA5                       | Y       | —                 |
| RA6                | 14          | 29          | 33         | 31          | ANA6                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA6                       | Y       | CLKOUT            |
| RA7                | 13          | 28          | 32         | 30          | ANA7                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA7                       | Y       | CLKIN             |
| RB0                | 33          | 8           | 9          | 8           | ANB0                         | —         | C2IN1+           | —   | —        | —                             | —                   | —   | CWG1 <sup>(1)</sup> | SSP2SS <sup>(1)</sup>                            | ZCD1 | —                         | —                     | —    | INT <sup>(1)</sup><br>IOCB0 | Y       | —                 |
| RB1                | 34          | 9           | 10         | 9           | ANB1                         | —         | C1IN3-<br>C2IN3- | —   | —        | —                             | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCB1                       | Y       | —                 |
| RB2                | 34          | 10          | 11         | 10          | ANB2                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCB2                       | Y       | —                 |
| RB3                | 36          | 11          | 12         | 11          | ANB3                         | —         | C1IN2-<br>C2IN2- | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB3                       | Y       | —                 |
| RB4                | 37          | 12          | 14         | 14          | ANB4<br>ADACT <sup>(1)</sup> | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB4                       | Y       | —                 |
| RB5                | 38          | 13          | 15         | 15          | ANB5                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB5                       | Y       | —                 |
| RB6                | 39          | 14          | 16         | 16          | ANB6                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | TX2<br>CK2 <sup>(1)</sup> | CLCIN2 <sup>(1)</sup> | —    | IOCB6                       | Y       | ICDCLK<br>ICSPCLK |
| RB7                | 40          | 15          | 17         | 17          | ANB7                         | —         | —                | —   | DAC1OUT2 | —                             | —                   | —   | —                   | —                                                | —    | RX2<br>DT2 <sup>(1)</sup> | CLCIN3 <sup>(1)</sup> | —    | IOCB7                       | Y       | ICDDAT<br>ICSPDAT |
| RC0                | 15          | 30          | 34         | 32          | ANC0                         | —         | —                | —   | —        | SOSCO<br>T1CKI <sup>(1)</sup> | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC0                       | Y       | —                 |
| RC1                | 16          | 31          | 35         | 35          | ANC1                         | —         | —                | —   | —        | SOSCI                         | CCP2 <sup>(1)</sup> | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC1                       | Y       | —                 |
| RC2                | 17          | 32          | 36         | 36          | ANC2                         | —         | —                | —   | —        | —                             | CCP1 <sup>(1)</sup> | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC2                       | Y       | —                 |
| RC3                | 18          | 33          | 37         | 37          | ANC3                         | —         | —                | —   | —        | T2IN <sup>(1)</sup>           | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCC3                       | Y       | —                 |
| RC4                | 23          | 38          | 42         | 42          | ANC4                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCC4                       | Y       | —                 |

**TABLE 6: 40/44-PIN ALLOCATION TABLE (PIC16(L)F15375, PIC16(L)F15376) (CONTINUED)**

| I/O <sup>(2)</sup> | 40-Pin PDIP | 40-Pin UQFN | 44-Pin QFN | 44-Pin TQFP | ADC  | Reference | Comparator | NCO | DAC | Timers | CCP | PWM | CWG | MSSP                                             | ZCD | EUSART                    | CLC | CLKR | Interrupt | Pull-up | Basic                   |
|--------------------|-------------|-------------|------------|-------------|------|-----------|------------|-----|-----|--------|-----|-----|-----|--------------------------------------------------|-----|---------------------------|-----|------|-----------|---------|-------------------------|
| RC5                | 24          | 39          | 43         | 43          | ANC5 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | IOCC5     | Y       | —                       |
| RC6                | 25          | 40          | 44         | 44          | ANC6 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | TX1<br>CK1 <sup>(1)</sup> | —   | —    | IOCC6     | Y       | —                       |
| RC7                | 26          | 1           | 1          | 1           | ANC7 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | RX1<br>DT1 <sup>(1)</sup> | —   | —    | IOCC7     | Y       | —                       |
| RD0                | 19          | 34          | 38         | 38          | AND0 | —         | —          | —   | —   | —      | —   | —   | —   | SSP2CLK <sup>(1)</sup><br>SSP2DAT <sup>(1)</sup> | —   | —                         | —   | —    | —         | —       | —                       |
| RD1                | 20          | 35          | 39         | 39          | AND1 | —         | —          | —   | —   | —      | —   | —   | —   | SSP2CLK <sup>(1)</sup><br>SSP2DAT <sup>(1)</sup> | —   | —                         | —   | —    | —         | —       | —                       |
| RD2                | 21          | 36          | 40         | 40          | AND2 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RD3                | 22          | 37          | 41         | 41          | AND3 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RD4                | 27          | 2           | 2          | 2           | AND4 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RD5                | 28          | 3           | 3          | 3           | AND5 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RD6                | 29          | 4           | 4          | 4           | AND6 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RD7                | 30          | 5           | 5          | 5           | AND7 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RE0                | 8           | 23          | 25         | 25          | ANE0 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RE1                | 9           | 24          | 26         | 26          | ANE1 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RE2                | 10          | 25          | 27         | 27          | ANE2 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |
| RE3                | 1           | 16          | 18         | 18          | ANE3 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | IOCE3     | Y       | MCLR<br>V <sub>PP</sub> |
| VDD                | 11          | 26          | 7          | 7           | —    | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | VDD                     |
| VDD                | 32          | 7           | 28         | 28          | —    | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | VDD                     |
| VSS                | 12          | 27          | 6          | 6           | —    | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | VSS                     |
| VSS                | 31          | 6           | 30         | 29          | —    | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | VSS                     |
| VSEL0              | 31          | 6           | 6          | 6           | —    | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | —                       |

**TABLE 6: 40/44-PIN ALLOCATION TABLE (PIC16(L)F15375, PIC16(L)F15376) (CONTINUED)**

| I/O <sup>(2)</sup> | 40-Pin PDIP | 40-Pin UQFN | 44-Pin QFN | 44-Pin TQFP | ADC | Reference | Comparator | NCO     | DAC | Timers | CCP  | PWM  | CWG            | MSSP                                               | ZCD | EUSART            | CLC     | CLKR | Interrupt | Pull-up | Basic |
|--------------------|-------------|-------------|------------|-------------|-----|-----------|------------|---------|-----|--------|------|------|----------------|----------------------------------------------------|-----|-------------------|---------|------|-----------|---------|-------|
| OUT <sup>(2)</sup> | —           | —           | —          | —           | —   | —         | C1OUT      | NCO1OUT | —   | TMR0   | CCP1 | PWM3 | CWG1A<br>CWG2A | SDO1<br>SDO2                                       | —   | DT <sup>(3)</sup> | CLC1OUT | CLKR | —         | —       | —     |
|                    | —           | —           | —          | —           | —   | —         | C2OUT      | —       | —   | —      | CCP2 | PWM4 | CWG1B<br>CWG2B | SCK1<br>SCK2                                       | —   | CK1<br>CK2        | CLC2OUT | —    | —         | —       | —     |
|                    | —           | —           | —          | —           | —   | —         | —          | —       | —   | —      | —    | PWM5 | CWG1C<br>CWG2C | SCK1 <sup>(3),(4)</sup><br>SCL2 <sup>(3),(4)</sup> | —   | TX1<br>TX2        | CLC3OUT | —    | —         | —       | —     |
|                    | —           | —           | —          | —           | —   | —         | —          | —       | —   | —      | —    | PWM6 | CWG1D<br>CWG2D | SDA1 <sup>(3),(4)</sup><br>SDA2 <sup>(3),(4)</sup> | —   | —                 | CLC4OUT | —    | —         | —       | —     |

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All digital output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLV register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

**TABLE 7: 48-PIN ALLOCATION TABLE (PIC16(L)F15385, PIC16(L)F15386)**

| I/O <sup>(2)</sup> | 48-Pin UQFN/TQFP | ADC                          | Reference | Comparator       | NCO | DAC      | Timers                        | CCP                 | PWM | CWG                 | MSSP                                             | ZCD  | EUSART                    | CLC                   | CLKR | Interrupt                   | Pull-up | Basic             |
|--------------------|------------------|------------------------------|-----------|------------------|-----|----------|-------------------------------|---------------------|-----|---------------------|--------------------------------------------------|------|---------------------------|-----------------------|------|-----------------------------|---------|-------------------|
| RA0                | 21               | ANA0                         | —         | C1IN0-<br>C2IN0- | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | CLCIN0 <sup>(1)</sup> | —    | IOCA0                       | Y       | —                 |
| RA1                | 22               | ANA1                         | —         | C1IN1-<br>C2IN1- | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | CLCIN1 <sup>(1)</sup> | —    | IOCA1                       | Y       | —                 |
| RA2                | 23               | ANA2                         | —         | C1IN0+<br>C2IN0+ | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA2                       | Y       | —                 |
| RA3                | 24               | ANA3                         | VREF+     | C1IN1+           | —   | DACREF+  | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA3                       | Y       | —                 |
| RA4                | 25               | ANA4                         | —         | C1IN1-           | —   | —        | T0CKI <sup>(1)</sup>          | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA4                       | Y       | —                 |
| RA5                | 26               | ANA5<br>ADACT                | —         | —                | —   | —        | T1G <sup>(1)</sup>            | —                   | —   | —                   | SSP1SS <sup>(1)</sup>                            | —    | —                         | —                     | —    | IOCA5                       | Y       | —                 |
| RA6                | 33               | ANA6                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA6                       | Y       | CLKOUT            |
| RA7                | 32               | ANA7                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCA7                       | Y       | CLKIN             |
| RB0                | 8                | ANB0                         | —         | C2IN1+           | —   | —        | —                             | —                   | —   | CWG1 <sup>(1)</sup> | SSP2SS <sup>(1)</sup>                            | ZCD1 | —                         | —                     | —    | INT <sup>(1)</sup><br>IOCB0 | Y       | —                 |
| RB1                | 9                | ANB1                         | —         | C1IN3-<br>C2IN3- | —   | —        | —                             | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCB1                       | Y       | —                 |
| RB2                | 10               | ANB2                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCB2                       | Y       | —                 |
| RB3                | 11               | ANB3                         | —         | C1IN3-<br>C2IN3- | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB3                       | Y       | —                 |
| RB4                | 16               | ANB4<br>ADACT <sup>(1)</sup> | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB4                       | Y       | —                 |
| RB5                | 17               | ANB5                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCB5                       | Y       | —                 |
| RB6                | 18               | ANB6                         | —         | —                | —   | —        | —                             | —                   | —   | —                   | —                                                | —    | TX2<br>CK2 <sup>(1)</sup> | CLCIN2 <sup>(1)</sup> | —    | IOCB6                       | Y       | ICDCLK<br>ICSPCLK |
| RB7                | 19               | ANB7                         | —         | —                | —   | DAC1OUT2 | —                             | —                   | —   | —                   | —                                                | —    | RX2<br>DT2 <sup>(1)</sup> | CLCIN3 <sup>(1)</sup> | —    | IOCB7                       | Y       | ICDDAT<br>ICSPDAT |
| RC0                | 34               | ANC0                         | —         | —                | —   | —        | SOSCO<br>T1CKI <sup>(1)</sup> | —                   | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC0                       | Y       | —                 |
| RC1                | 35               | ANC1                         | —         | —                | —   | —        | SOSCI                         | CCP2 <sup>(1)</sup> | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC1                       | Y       | —                 |
| RC2                | 40               | ANC2                         | —         | —                | —   | —        | —                             | CCP1 <sup>(1)</sup> | —   | —                   | —                                                | —    | —                         | —                     | —    | IOCC2                       | Y       | —                 |
| RC3                | 41               | ANC3                         | —         | —                | —   | —        | T2IN <sup>(1)</sup>           | —                   | —   | —                   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —    | —                         | —                     | —    | IOCC3                       | Y       | —                 |

**TABLE 7: 48-PIN ALLOCATION TABLE (PIC16(L)F15385, PIC16(L)F15386) (CONTINUED)**

| I/O <sup>(2)</sup> | 48-Pin UQFN/TQFP | ADC  | Reference | Comparator | NCO | DAC | Timers | CCP | PWM | CWG | MSSP                                             | ZCD | EUSART                    | CLC | CLKR | Interrupt | Pull-up | Basic                   |
|--------------------|------------------|------|-----------|------------|-----|-----|--------|-----|-----|-----|--------------------------------------------------|-----|---------------------------|-----|------|-----------|---------|-------------------------|
| RC4                | 46               | ANC4 | —         | —          | —   | —   | —      | —   | —   | —   | SSP1CLK <sup>(1)</sup><br>SSP1DAT <sup>(1)</sup> | —   | —                         | —   | —    | IOCC4     | Y       | —                       |
| RC5                | 47               | ANC5 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | IOCC5     | Y       | —                       |
| RC6                | 48               | ANC6 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | TX1<br>CK1 <sup>(1)</sup> | —   | —    | IOCC6     | Y       | —                       |
| RC7                | 1                | ANC7 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | RX1<br>DT1 <sup>(1)</sup> | —   | —    | IOCC7     | Y       | —                       |
| RD0                | 42               | AND0 | —         | —          | —   | —   | —      | —   | —   | —   | SSP2CLK <sup>(1)</sup><br>SSP2DAT <sup>(1)</sup> | —   | —                         | —   | —    | —         | Y       | —                       |
| RD1                | 43               | AND1 | —         | —          | —   | —   | —      | —   | —   | —   | SSP2CLK <sup>(1)</sup><br>SSP2DAT <sup>(1)</sup> | —   | —                         | —   | —    | —         | Y       | —                       |
| RD2                | 44               | AND2 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RD3                | 45               | AND3 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RD4                | 2                | AND4 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RD5                | 3                | AND5 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RD6                | 4                | AND6 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RD7                | 5                | AND7 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RE0                | 27               | ANE0 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RE1                | 28               | ANE1 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RE2                | 29               | ANE2 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RE3                | 20               | ANE3 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | IOCE3     | Y       | MCLR<br>V <sub>PP</sub> |
| RF0                | 36               | ANF0 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RF1                | 37               | ANF1 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RF2                | 38               | ANF2 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RF3                | 39               | ANF3 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RF4                | 12               | ANF4 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RF5                | 13               | ANF5 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RF6                | 14               | ANF6 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| RF7                | 15               | ANF7 | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | —                       |
| V <sub>DD</sub>    | 30               | —    | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | Y       | V <sub>DD</sub>         |
| V <sub>DD</sub>    | 7                | —    | —         | —          | —   | —   | —      | —   | —   | —   | —                                                | —   | —                         | —   | —    | —         | —       | V <sub>DD</sub>         |

**TABLE 7: 48-PIN ALLOCATION TABLE (PIC16(L)F15385, PIC16(L)F15386) (CONTINUED)**

| I/O <sup>(2)</sup> | 48-Pin UQFN/TQFP | ADC | Reference | Comparator | NCO     | DAC | Timers | CCP  | PWM  | CWG            | MSSP                                               | ZCD | EUSART            | CLC     | CLKR | Interrupt | Pull-up | Basic           |
|--------------------|------------------|-----|-----------|------------|---------|-----|--------|------|------|----------------|----------------------------------------------------|-----|-------------------|---------|------|-----------|---------|-----------------|
| V <sub>SS</sub>    | 6                | —   | —         | —          | —       | —   | —      | —    | —    | —              | —                                                  | —   | —                 | —       | —    | —         | —       | V <sub>SS</sub> |
| V <sub>SS</sub>    | 31               | —   | —         | —          | —       | —   | —      | —    | —    | —              | —                                                  | —   | —                 | —       | —    | —         | —       | V <sub>SS</sub> |
| VSEL0              | —                | —   | —         | —          | —       | —   | —      | —    | —    | —              | —                                                  | —   | —                 | —       | —    | —         | —       | —               |
| OUT <sup>(2)</sup> | —                | —   | —         | C1OUT      | NCO1OUT | —   | TMR0   | CCP1 | PWM3 | CWG1A<br>CWG2A | SDO1<br>SDO2                                       | —   | DT <sup>(3)</sup> | CLC1OUT | CLKR | —         | —       | —               |
|                    | —                | —   | —         | C2OUT      | —       | —   | —      | CCP2 | PWM4 | CWG1B<br>CWG2B | SCK1<br>SCK2                                       | —   | CK1<br>CK2        | CLC2OUT | —    | —         | —       | —               |
|                    | —                | —   | —         | —          | —       | —   | —      | —    | PWM5 | CWG1C<br>CWG2C | SCK1 <sup>(3),(4)</sup><br>SCL2 <sup>(3),(4)</sup> | —   | TX1<br>TX2        | CLC3OUT | —    | —         | —       | —               |
|                    | —                | —   | —         | —          | —       | —   | —      | —    | PWM6 | CWG1D<br>CWG2D | SDA1 <sup>(3),(4)</sup><br>SDA2 <sup>(3),(4)</sup> | —   | —                 | CLC4OUT | —    | —         | —       | —               |

- Note**
- 1: This is a PPS re-mappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
  - 2: All digital output signals shown in this row are PPS re-mappable. These signals may be mapped to output onto one of several PORTx pin options.
  - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
  - 4: These pins are configured for I<sup>2</sup>C logic levels. PPS assignments to the other pins will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I<sup>2</sup>C specific or SMBUS input buffer thresholds.

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